Technological Parameters and Edge Fringing Capacitance in GaN Schottky Barrier Diodes: Monte Carlo Simulations

B. Orfao
Applied Physics Department
University of Salamanca
Salamanca
beatrizorfao@usal.es

B.G. Vasallo
Applied Physics Department
University of Salamanca
Salamanca
bgvasallo@usal.es

D. Moro-Melgar
ACST GmbH
ACST GmbH
Hanau, Germany
diego.moro-melgar@acst.de

M. Zaknoune
Institut d'Electronique de
Microélectronique et de
Nanotechnologie
France
mohammed.zaknoune@univ-lille.fr

G.Di Gioia
Institut d'Electronique de
Microélectronique et de
Nanotechnologie
France

M. Samnouni
Institut d'Electronique de
Microélectronique et de
Nanotechnologie
France
mohammed.samnouni@univ-lille.fr

S. Pérez
Applied Physics Department
University of Salamanca
Salamanca
susana@usal.es

T. González
Applied Physics Department
University of Salamanca
Salamanca
tomasg@usal.es

J. Mateos
Applied Physics Department
University of Salamanca
Salamanca
javierm@usal.es

2021 13th Spanish Conference on Electron Devices (CDE) | 978-1-6654-4452-1/21/$31.00 ©2021 IEEE | DOI: 10.1109/CDE52135.2021.9455727

***Abstract*—Schottky barrier diodes (SBDs) with realistic geometries have been studied by means of a 2-D ensemble Monte Carlo simulator. The non-linearity of the Capacitance-Voltage (C-V) characteristic is the most important parameter for optimizing SBDs as frequency multipliers. In this paper, by changing the values of several technological parameters, we analyze their influence on the edge fringing capacitance in a GaN SBD. We have found that the parameters related with the dielectric used for the passivation and the lateral extension of the epilayer significantly affect the fringing capacitance, thus increasing the value of the total capacitance above the ideal one.**

***Keywords*—Edge effects, Monte Carlo, Schottky Barrier Diodes, permittivity, dielectric, fringing capacitance**

I. INTRODUCTION

The nonlinearity of the *C-V* characteristic is the key parameter for optimizing the THz performance of Schottky Barrier Diodes (SBDs) operating as frequency multipliers [1]. To analyze *C*, analytical and numerical models have to be used, since experimental data are not easily available. For high-frequency applications, where the anode surface needs to be significantly reduced, the intrinsic capacitance *C* dramatically deviates from its ideal value due to 2-D edge fringing effects and a deep analysis becomes imperative. For example, the size of the SBDs must be as small as 0.16 μm^2 in order to obtain a low enough capacitance of around 0.5 fF and reach operation frequencies above 1 THz [2].

Apart from that, the properties of GaN, such as a wide gap (3.4 eV) and a high electron mobility, make it a good candidate for the fabrication of SBDs for high-power applications at high frequency, however, its surface must be passivated in order to avoid unwanted effects due to interface traps. The aim of this work is to analyze the influence of several technological parameters on the *C-V* characteristic of GaN SBDs, in particular on the contribution associated to edge effects (EEs).

II. MODEL

The edge capacitance per unit length, C_{EE} has been modelled using the dimensionless parameter β, as $C_{EE}= \beta \cdot \varepsilon_{SC}$, where ε_{SC} is the dielectric constant of the semiconductor (8.9 in GaN) [3]. C_{EE} is the contribution to the total capacitance that indicates the deviation from the ideal capacitance. For the calculation of C_{EE} in realistic topologies, a semiclassical

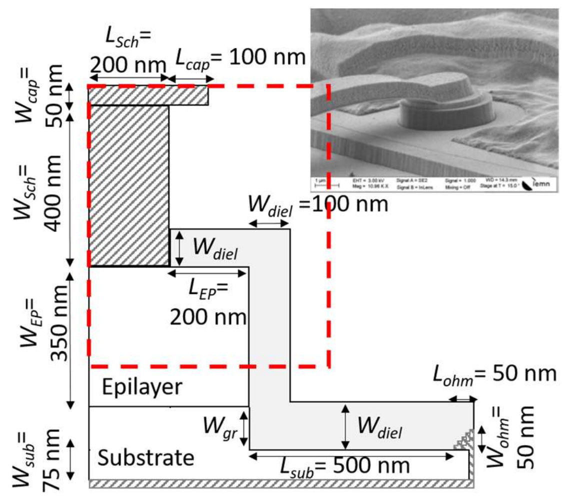

Fig. 1 Schematic topology of the 2-D MC simulated SBDs. Inset: SEM image of a real SBD fabricated at the Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN). The red dashed rectangular zone is the region represented in Fig. 3.

ensemble MC simulator of carrier transport self-consistently coupled with a 2-D Poisson solver has been used [4]. Γ_1, U, and Γ_3 valleys are considered to form the conduction band of GaN [5-6]. Interaction with ionized impurities, dislocations, polar and nonpolar optical phonon, acoustic phonon, and intervalley scattering are included in the GaN model. For simplicity, surface-charge effects are neglected, thus a surface-charge density equal to zero (σ=0) is considered at the semiconductor-dielectric interfaces. To account for such effects, a dynamic surface-charge model requiring more computational effort would be necessary [7]; still, the model used in this work is sufficient to evidence the importance of the EEs in the capacitance.

The geometry of the MC simulated structure is shown in Fig. 1, which includes the nominal values of the different geometrical parameters. The topology is based on fabricated planar SBDs as that shown in the inset [8]. The layer structure consists of a highly-doped substrate with doping N_S=5×10^{18} cm^{-3} and an epilayer with doping N_E=3×10^{17} cm^{-3}. The Schottky contact is placed on the top of the epilayer. The thickness of the epilayer (W_{EP}) and substrate (W_{sub}) has been optimized in previous studies, being the epilayer thick enough to avoid that the depletion region reaches the substrate. Simulations with different values of some of the geometrical parameters have been carried out in order to find the optimal configuration to reduce EEs. Air, SiO_2, Silicon nitride (Si_3N_4)

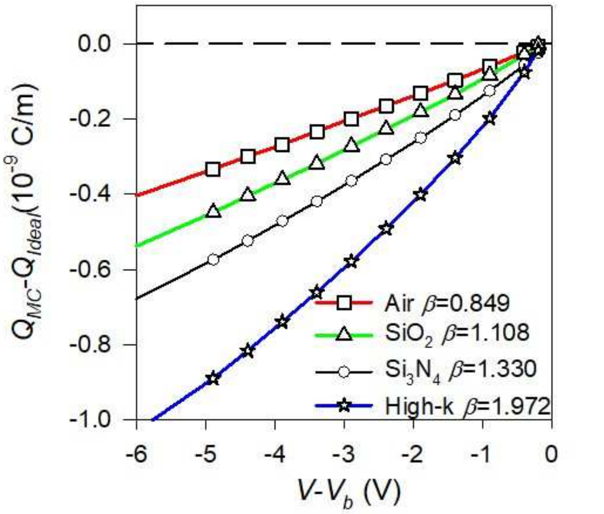

Fig. 2 Difference between the depleted charge obtained from MC simulations and the ideal charge (Q_{MC}-Q_{Ideal}) vs. V-V_b. The EEs parameter β is calculated from the slope of this representation. For the calculation we use reverse-bias points far from flat-band conditions, where there is a linear behavior.

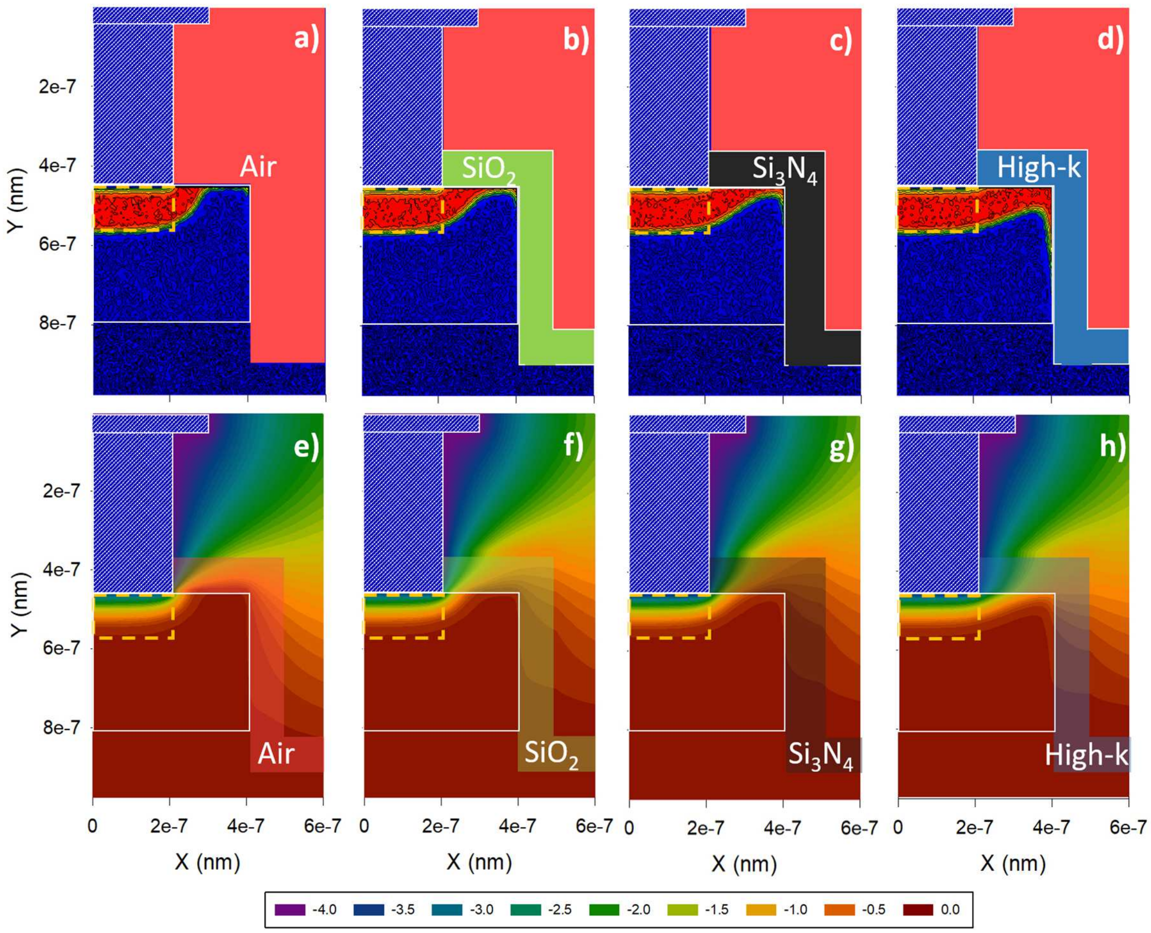

Fig. 3 Map of the local contribution to the total capacitance per unit length, calculated as the variation of the electron charge per unit length between flat-band conditions and the bias point V-V_b=-4.0V, divided by the voltage difference, for different dielectric constants: (a) air, (b) SiO_2, (c) silicon nitride and (d) a high-k dielectric. The red color represents the region where the electron charge is modified by the bias. The potential profile for the bias point V-V_b =-4.0V is also represented for the same dielectrics: (e) air, (f) SiO_2, (g) silicon nitride and (h) a high-k dielectric. The geometrical parameters of the diode are those in Fig.1. Only the dashed rectangular zone in Fig. 1 is represented. The yellow dashed rectangular zone indicates the ideal depletion region, so the EEs region can be identified as the part of the depletion region outside this area.

and a high-k dielectric (e.g. ZrO_2), with dielectric constants of 1.0, 3.9, 7.5 and 25.0, respectively, have been considered as passivation dielectrics (in grey in Fig. 1) in the simulations in order to study their influence on EEs. Air is considered above the dielectric in the (rectangular) simulation domain.

The total depleted charge per unit length can be expressed (as a function of the applied voltage, V) as:

$$Q(V)=Q_{Ideal}(V)+\beta\cdot\varepsilon_{SC}\cdot(V-V_b), \quad (1)$$

with $Q_{Ideal}(V)=-L_{Sch}\cdot q\cdot N_E\cdot W(V)$, being L_{Sch} the size of the Schottky contact, q the electron charge, N_E the doping level of the epilayer, $W(V)$ the depth of the depletion region and V_b the built-in voltage of the Schottky contact [6]. The depth of the depletion region is given by:

$$W(V) = \sqrt{\frac{2\cdot\varepsilon_{SC}\cdot(V_b-V)}{q\cdot N_E}}\ . \quad (2)$$

The first term in Eq. (1) is the ideal charge depleted by the Schottky contact, while the second one corresponds to the EEs depleted charge (Q_{EE}), at the origin of C_{EE}. MC simulations allow us to obtain the total depleted charge, Q_{MC}, so that the β parameter is calculated from the slope of $Q_{EE}=Q_{MC}-Q_{Ideal}$ vs. $V-V_b$, as illustrated in Fig. 2. As observed, for reverse bias, Q_{EE} exhibits the expected linear behavior with $V-V_b$, which changes when approaching flat-band conditions. Thus, β is calculated from the slope for high enough V in the reverse-bias region where the dependence is linear.

III. Results

The influence of the dielectric material used for the passivation (grey area in Fig. 1) is observed in Figs. 2 and 3, which evidence that Q_{EE} is more significant for the dielectrics with a higher permittivity. Fig. 3 shows the local contribution to the total capacitance and the potential profile in the region where EEs are relevant. Red color in Figs. 3 (a)-(d) means change in electron concentration with applied voltage. As observed, EEs are more pronounced for higher dielectric permittivity of the passivation material. A higher dielectric constant allows a more pronounced penetration of the electric field in the epilayer region at the right of the Schottky contact, as observed in the potential profiles of Figs. 3 (e)-(h), which in turn leads to a larger charge depletion at the origin of EEs. Thus, higher values of β are expected for higher dielectric constant of the passivation material, as we will confirm in the following.

Apart from the dielectric material, we have studied how β is affected by the values of other technological parameters. Firstly (results not shown here), we have checked that β is not affected by the size of the Schottky contact *(L_{Sch})*, the size of the ohmic contact (L_{ohm} and W_{ohm}), and the length L_{cap}.

Then, we have modified the thickness of the dielectric, W_{diel}. Fig. 4 shows β vs. W_{diel} (from 25 nm to 200 nm) for different dielectrics. We have found that, as expected, EEs increase with W_{diel} and the permittivity of the dielectric. Two values of the distance between the ohmic contact and the epilayer, L_{sub}=200nm and 500 nm, have been considered. The results indicate that β is not affected by this parameter. In the case of air, β is obviously constant with W_{diel}. When W_{diel}=0 nm, the value corresponding to the air is obtained for all the dielectrics.

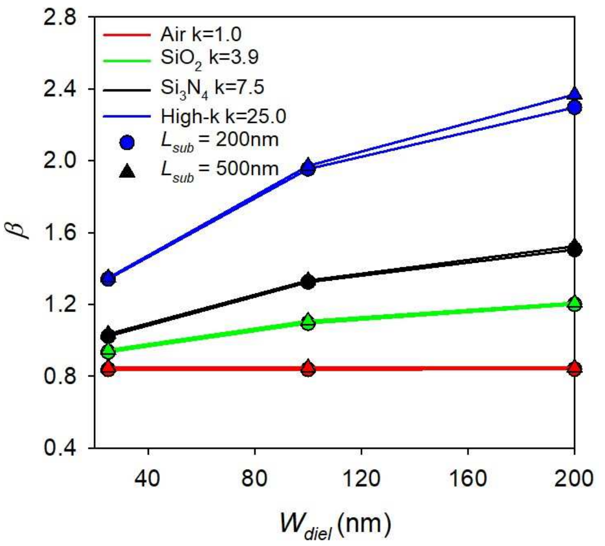

Fig. 4 Dependence of the β parameter on W_{diel} for two values of L_{sub} (200nm and 500nm) and different dielectrics: air (red), silicon nitride (black), silicon dioxide (green) and a high-k dielectric (blue).

On the other hand, the effect of the epilayer lateral extension, L_{EP}, is also important. The values obtained for β as a function of L_{EP} from 0 nm to 200 nm are represented in Fig. 5 when considering W_{diel}=100 nm. For long enough L_{EP}, β remains almost constant, but when L_{EP} is shorter than a given length, β significantly decreases. This geometrical limit depends on the dielectric: the higher the permittivity the higher the value at which L_{EP} starts decreasing. Indeed, for the considered values of L_{EP}, the corner length is not reached in the case of the high-k dielectric. The minimum value of the EEs parameter is reached at L_{EP}=0 nm, not being suppressed in any case, and this value depends on the dielectric.

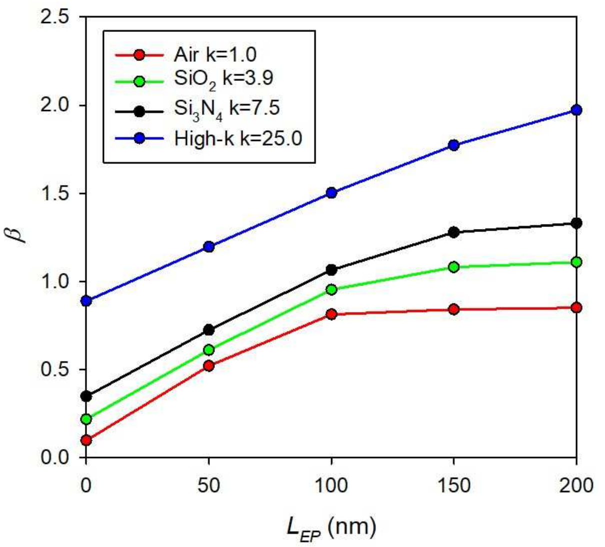

Fig. 5 The β parameter calculated for different dielectrics and W_{diel}=100nm versus L_{EP}.

Finally, the lateral profiles of potential and carrier concentration just below the Schottky contact up to the epilayer corner at $V-V_b$=-4.0V, represented in Fig. 6, illustrate in more detail the influence of the dielectrics. As mentioned before in the discussion of Fig. 3, a higher dielectric constant of the passivation material facilitates a stronger penetration of the electric field in the lateral extension of the epilayer (both in vertical and horizontal direction), as clearly observed in the potential profiles of Fig. 6 in the horizontal direction. As a result, a more pronounced depletion takes place. In the cases shown in Fig. 6, and as observed in Fig. 3, the top of the epilayer is completely depleted when the high-k dielectric is considered, nearly fully depleted in the case of silicon nitride, while for air, at about 100 nm from the edge of the epilayer, the nominal electron concentration of 3×10^{17} cm^{-3} is reached.

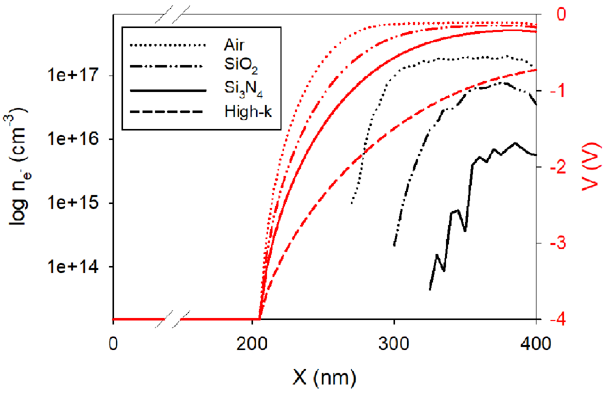

Fig. 6 Horizontal profiles of potential (red) and carrier concentration (black) at the top of the semiconductor (in the vicinity of the interface with the dielectric) from the Schottky contact to the corner of the epilayer for different dielectrics using the technological parameters of Fig. 1 at $V\text{-}V_b$=-4.0V.

Despite of the negative effects on the EEs capacitance of a passivation material with high permittivity, the deeper penetration of the electric field in the lateral extension of the epilayer is accompanied by lower values of the electric field (smaller slope of the potential observed in Fig. 6), which is positive to increase the breakdown voltage of the SBD.

IV. Conclusions

The characterization of EEs capacitance is important in SBDs, mainly when decreasing the diode size in order to reach high frequency operation. The results obtained in this work allow us to conclude that the selection of the passivation dielectric and some technological parameters, like the width of the dielectric or lateral extension of the epilayer, is important because it affects the EEs parameter and therefore the capacitance. These results allow to optimize the topology of the SBDs, always taking into account the restrictions that the technological process imposes on the fabrication of the devices.

Acknowledgment

This work was supported in part by Spanish MINECO and FEDER under Project TEC2017-83910-R and in part by the Junta de Castilla y León and FEDER under Project SA254P18. The work of B. Orfao was supported by the Junta de Castilla y León.

References

[1] J. T. Louhi, "The capacitance of a small circular Schottky diode for submillimeter wavelengths," IEEE Microw. Guided Wave Lett., vol. 4, no. 4, pp. 107–108, Apr. 1994.

[2] A. Maestrini, L. Gatilova, J. Treuttel, Y. Jin, A. Cavanna, J. Valentin, T. Vacelet, A. Féret, S. Caroopen, G. Gay, S. Mignoni, J-M. Krieg, P. De Maagt, C. Goldstein, "Terahertz Schottky Mixers for Atmospheric and Planetary Sciences", Infrared Millimeter and Terahertz Waves (IRMMW-THz) 2019 44th International Conference on, pp. 1-2, 2019.

[3] D. Moro-Melgar, A. Maestrini, J. Treuttel, L. Gatilova, T. González, B. G. Vasallo, and Javier Mateos, "Monte Carlo Study of 2-D Capacitance Fringing Effects in GaAs Planar Schottky Diodes," IEEE Trans. on Electron. Dev., vol. 63, no. 10, pp. 3900-3907, October 2016.

[4] J. Mateos et al., "Effect of the T-gate on the performance of recessed HEMTs, A Monte Carlo analysis," Semicond. Sci. Technol., vol. 14, no. 9, p. 864, 1999.

[5] M. V. Fischetti, "Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures. I. Homogeneous transport," IEEE Trans. Electron Devices, vol. 38, no. 3, p. 634–649, Oct. 1991.

[6] S. García "Comparative Monte Carlo analysis of InP- and GaN-based Gunn diodes," J. Appl. Phys., vol. 115, Oct. 2014, Art. no. 044510.

[7] B. Orfao, B. G. Vasallo, D. Moro-Melgar, S. Pérez, J. Mateos and T. González, "Analysis of Surface Charge Effects and Edge Fringing Capacitance in Planar GaAs and GaN Schottky Barrier Diodes" IEEE Trans. on Electron. Dev., vol. 67, no. 9, pp. 3530-3535, Sept. 2020.

[8] G. Di Gioia, V.K. Chinni, M. Zegaoui, Y. Cordier, A. Maestrini, J. Treuttel, G. Ducournau, Y. Roelens, M. Zaknoune, "GaN Schottky diode for high power THz generation using multiplier principle", 43rd Workshop on Compound Semiconductor Devices and Integrated Circuits, WOCSDICE 2019, Cabourg, France, 2019.