Diamond Field-Effect Transistors With V_2O_5-Induced Transfer Doping: Scaling to 50-nm Gate Length

Kevin G. Crawford, James D. Weil, Pankaj B. Shah, Dmitry A. Ruzmetov, Mahesh R. Neupane, Khamsouk Kingkeo, A. Glen Birdwell, and Tony G. Ivanov

***Abstract*— We report on the fabrication and measurement of hydrogen-terminated diamond field-effect transistors (FETs) incorporating V_2O_5 as a surface acceptor material to induce transfer doping. Comparing a range of gate lengths down to 50 nm, we observe inversely scaling peak output current and transconductance. Devices exhibited a peak drain current of ~700 mA/mm and a peak transconductance of ~150 mS/mm, some of the highest reported thus far for a diamond metal semiconductor FET (MESFET). Reduced sheet resistance of the diamond surface after V_2O_5 deposition was verified by four probe measurement. These results show great potential for improvement of diamond FET devices through scaling of critical dimensions and adoption of robust transition metal oxides such as V_2O_5.**

***Index Terms*— 2-D hole gas (2DHG), diamond metal semiconductor field-effect transistor (MESFET), drain-induced barrier lowering (DIBL), electronic devices, gate length, power, radio frequency (RF), surface transfer doping, V_2O_5.**

I. Introduction

INTEREST in the diamond material system for electronic applications has rapidly increased in recent years, becoming a global scale area of interest. With its ultrawide band-gap of 5.47 eV, extremely high thermal conductivity of >20 W cm^{-1} K^{-1} and intrinsically high breakdown field of 10 MV/cm, diamond is a promising candidate in achieving next-generation high-power electronic devices [1]–[4]. Progress in this area has been typically hindered by the lack of mature doping techniques and on-going development of novel fabrication strategies to overcome the challenges in working with diamond [5]. The U.S. Army Research Laboratory is investing in the development of surface transfer-doped diamond field-effect transistors (FETs) for radio frequency (RF) and power applications [6]–[8]. Surface transfer doping offers an alternative to substitutional doping that alleviates the challenges of introducing impurity dopants into diamond's tightly packed carbon lattice. Historically, spontaneous accumulation of volatile atmospheric adsorbents on the hydrogen-terminated diamond surface when exposed to air has provided the necessary surface acceptor states for transfer doping [1], [9]. However, this method of transfer doping is highly sensitive to environmental conditions such as temperature, humidity, and molecular composition of the adsorbents [8], [9]. More recent results demonstrate enhanced surface transfer doping utilizing high electron affinity transition metal oxides, such as V_2O_5. When in intimate contact with the hydrogen-terminated diamond surface, these high electron affinity materials will prompt the transfer of electrons from the diamond, acting as an electron accepter. This process leaves behind corresponding holes within the diamond, forming a 2-D hole gas (2DHG) beneath the surface [8], [10], [11]. This approach of encapsulation with a transition metal oxide has been incorporated into our diamond metal semiconductor FET (MESFET) designs, improving output current density and stability of devices. By reducing gate length (L_g), peak output current and transconductance are improved significantly.

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II. Experimental

A single crystal diamond sample with (100) surface orientation and 4 mm $\times$ 4 mm dimensions was obtained from Element Six. The substrate was first cleaned in H_2SO_4:NHO_3, to remove any metallic and organic contaminants, and then hydrogen terminated in a CVD diamond growth reactor. The substrate was then coated with 100 nm thermally evaporated Au as a sacrificial layer both to form ohmic contacts and to protect the hydrogen-terminated surface. Electrical isolation of devices was performed by patterning and etching the Au sacrificial layer between regions using a KI_2 solution. At this point, the exposed diamond surface is treated in O_2 plasma to remove hydrogen termination in these areas. Probe pads consisting of Ti/Au were written and deposited to overlap the Au ohmic metal and provide a more robust contact. The source–drain region of each device was then patterned and etched using a KI_2 solution with carefully controlled dilution and temperature. Gate dimensions of 50, 100, 200, 400, and 800 nm were defined by e-beam lithography and a metal gate-stack of Al/Pt/Au 50/25/45 nm was deposited. A similar process flow can be found in [6]. Each device had two gates with a combined width of 50 μm and a

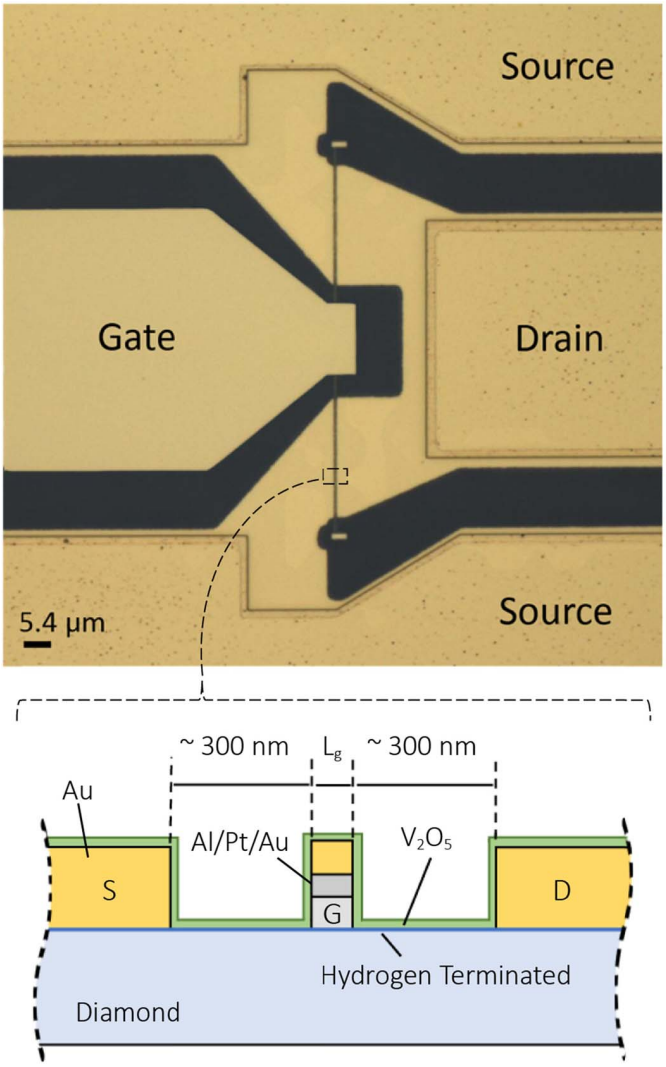

Fig. 1. Optical image of a diamond MESFET and pictorial cross section of the channel.

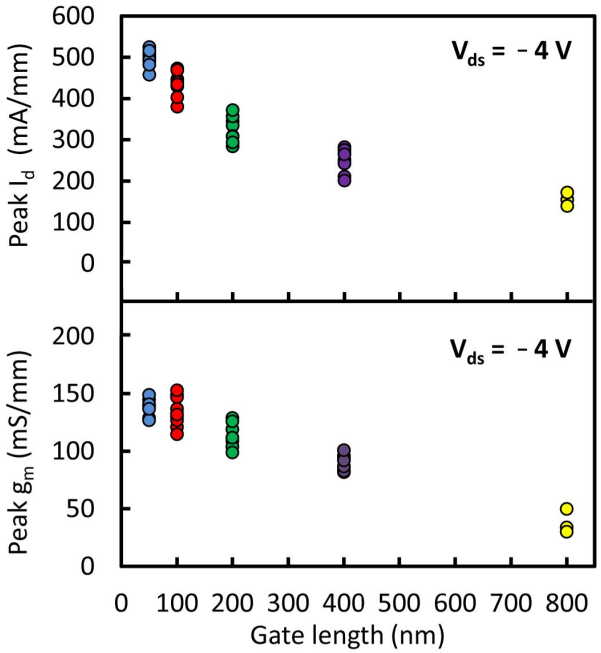

Fig. 2. Summary of peak output current and transconductance for 37 devices of various gate lengths. $V_{ds} = -4$ V, $V_{gs} = -3$ V.

spacing of ~300 nm from gate to source/drain. Dimensions were verified by scanning electron microscopy (SEM). The substrate was then encapsulated with 40 nm V_2O_5 by thermal evaporation, provided by Blue Wave Semiconductors Inc. A 350 °C *in situ* anneal was performed prior to deposition to drive off atmospheric molecules from the diamond surface. Evidence suggests this anneal step is crucial for stability of the V_2O_5 work function [8]. Fig. 1 shows an optical image and cross section of one FET device.

III. Results

Plots of peak drain current and transconductance for 37 devices with gate lengths ranging from 50 to 800 nm are shown in Fig. 2. DC characterization was carried out using GGB Industries ground-signal-ground probes with 50-μm pitch and a Keysight B1500 parametric analyzer. Measurement of peak values were taken at $V_{ds} = -4$ V and $V_{gs} = -3$ V. A clear trend between reduced gate length and increased current (I_d)/transconductance (g_m) is observed, with small dispersion between data points indicating good yield across the substrate relative to what is typically observed on hydrogen-terminated diamond. The highest I_d and g_m values plotted are 525 mA/mm and 153 mS/mm, respectively. Four probe measurement of a van der Pauw (VDP) structure on the substrate showed a reduction in sheet resistance from 14.2 to 6.8 kΩ/□ after deposition of V_2O_5, a decrease consistent with other such reported results [11], [12]. Measurement of the V_2O_5 film resistance via an isolation structure on the substrate showed ~20 GΩ/mm.

Fig. 3 shows normalized I–V output characteristics for four FET devices with gate lengths of 50, 100, 200, and 400 nm. Peak output current at $V_{gs} = -3$ V and $V_{ds} = -4$ V for each device scaled inversely with gate length, ranging from ~500 to ~270 mA/mm, due to reduced L_g resulting in a decreased depletion region beneath the Al gate contact [13]. Likewise, OFF-state behavior significantly worsens as L_g moves toward smaller dimensions due to a reduced ability to deplete the diamond 2DHG.

Gate leakage for the 50-nm device at peak output current was ~1 μA/mm. A sharp increase in gate current was observed when attempting to reach the pinch-off state, increasing to ~4.8 mA/mm at $V_{gs} = 2$ V. This effect was permanent, resulting in increased gate leakage for any subsequent sweeps. Although the exact mechanism is unclear, this could be related to hot carrier injection in which carriers gain sufficient energy to overcome the potential barrier formed by the diamond:Al interface [14]. Other reported work has suggested the formation of a native oxide under the Al contact, evidenced by a TEM cross section of the gate showing a 7-nm amorphous layer between the Al and diamond [15]. In this instance, the gate interface may have been compromised to some extent by the preanneal of 350 °C used in the deposition of V_2O_5. Further work will be needed to investigate. This may be improved by incorporation of a high-quality gate dielectric, as shown here [16].

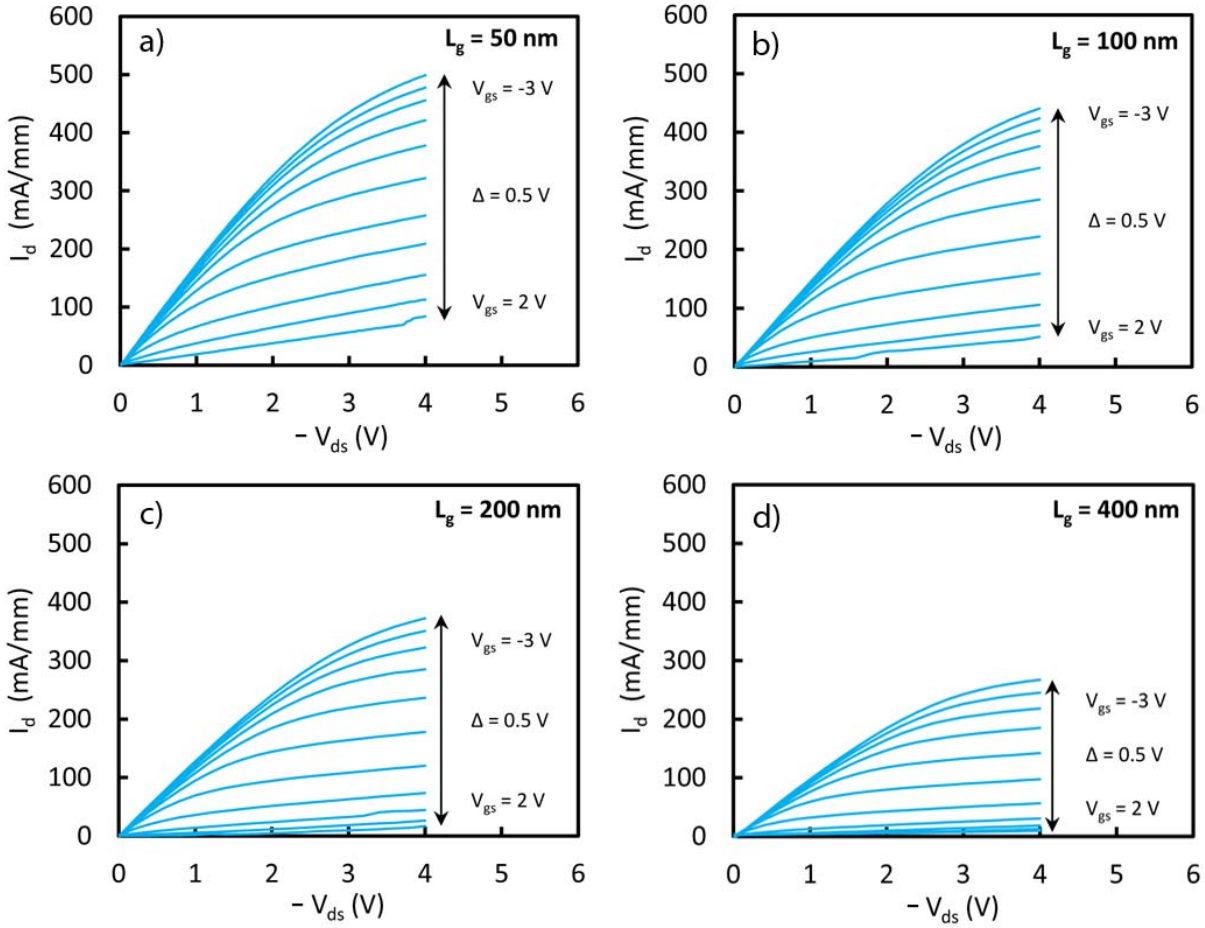

Fig. 3. *I–V* output plots for devices of four different gate lengths of (a) 50, (b) 100, (c) 200, and (d) 400 nm. $V_{gs} = 2$ to -3 V and $V_{ds} = 0$ to -4 V.

Fig. 4 shows transfer characteristics for the same four FET devices shown in Fig. 3, with gate lengths of 50, 100, 200, and 400 nm. Again, transconductance is seen to scale inversely with gate length. Although g_m is similar between the 100- and 50-nm gated devices at ∼140 mS/mm, some instability can be seen in the trace for the smaller gate length. Increasing L_g beyond 100 nm showed reduced transconductance, down to ∼100 mS/mm and with a flatter distribution for the 400-nm gate. Interestingly, measurements shown in Fig. 4 exhibit higher peak drain current than those in Fig. 3. This phenomenon was consistent and repeatable, in which sweeping the gate voltage at a constant drain bias would produce higher drain current than the reverse. This effect is potentially related to charge trapping. By satisfying trap states with a constant value of V_{ds}, a small increase in output current is seen.

A summary of extracted parameters for each device discussed is displayed in Table I. Values for ON-resistance (R_{ON}) were calculated from the linear low-field region of each device at $V_{gs} = -3$ V. Contact resistance (R_c) and sheet resistance (R_{sheet}) were measured from TLM and VDP structures on the substrate. From this, access resistance (R_{access}) was determined by the dimensions of the device. The resistance beneath the gate contact (R_{ch}) was calculated as

$$R_{ch} = R_{ON} - (2R_c + 2R_{access}) \quad (1)$$

TABLE I
SUMMARY OF EXTRACTED PARAMETERS FOR EACH GATE LENGTH

L_g (nm)	50	100	200	400
R_{on} (Ω.mm)	6	6.8	7.7	10.4
R_c (Ω.mm)	0.9			
R_{sheet} (Ω/□)	6813			
R_{access} (Ω.mm)	2.04			
R_{ch} (Ω.mm)	0.1	0.92	1.82	4.42
$I_{d\ peak}$ (mA/mm)	500	450	380	270
$g_{m\ peak}$ (mS/mm)	141	138	125	100
V_{th} (V)	1.51	0.96	0.69	0.28

This assumes contact resistance is identical between contacts and access resistance is mirrored on either side of the gate due to the self-aligned nature of the fabrication process used. Threshold voltage (V_{th}) was extrapolated from the linear region of the transfer characteristics in Fig. 4. As L_g moves toward lower values, an increase in V_{th} is observed as channel pinch-off becomes harder to achieve. In this instance, V_{th} is more representative of the ON–OFF ratio for smaller devices that do not pinch-off. These values are relatively in close agreement for a V_2O_5-doped MOSFET with L_g of 250 nm, reported

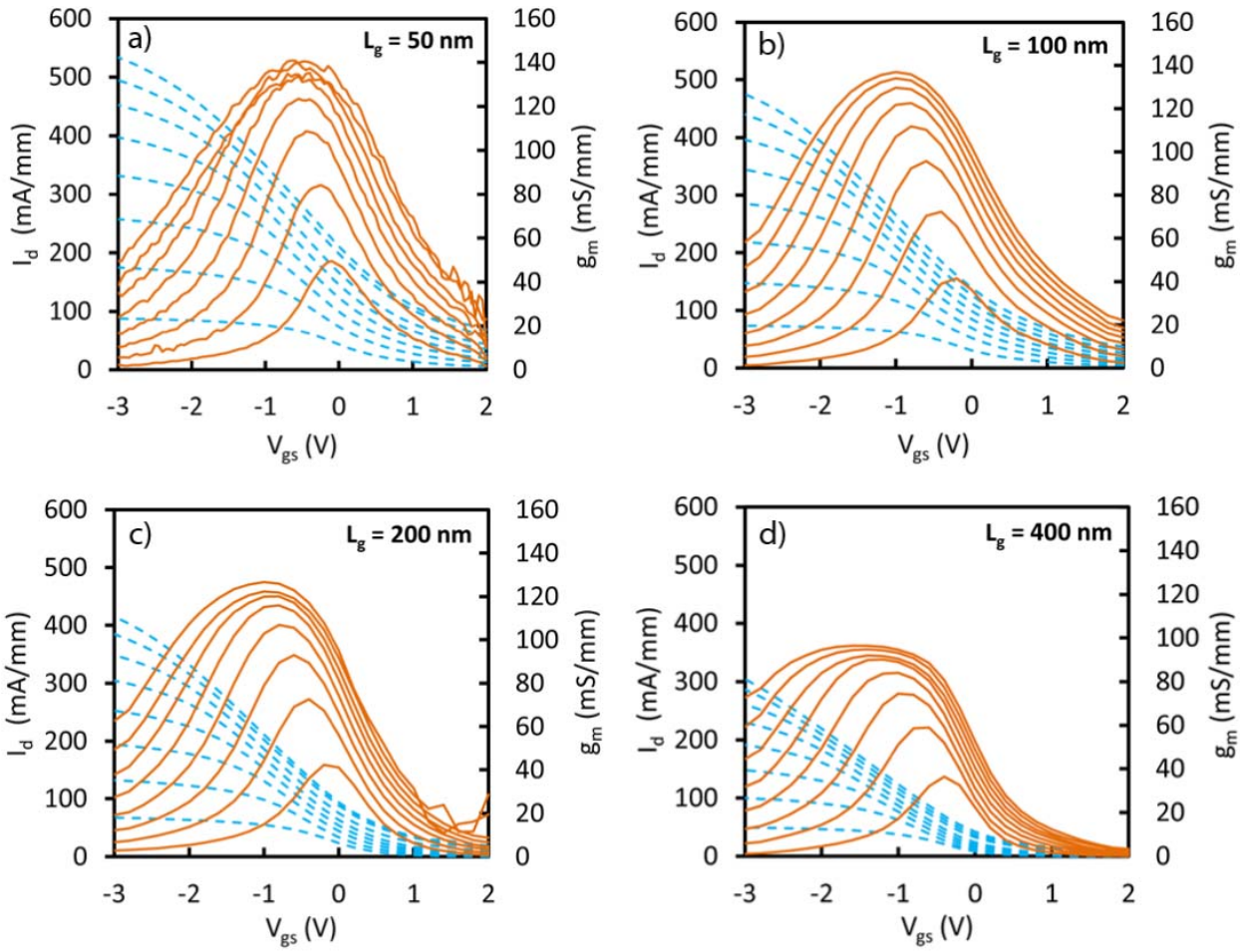

Fig. 4. Transfer characteristics for devices of four different gate lengths of (a) 50, (b) 100, (c) 200, and (d) 400 nm. $V_{gs} = 2$ to -3 V, $V_{ds} = 0$ to -4 V. Dashed line shows I_d and solid line shows g_m.

here [17]. While the substrate for this MOSFET exhibited lower sheet resistance, ON-resistance was notably higher due to increased contact and access resistance.

A capacitance–voltage curve (C–V) was taken for a 400-nm gate length device, plotted in Fig. 5. Arrows indicate the direction of the sweep. Maximum gate capacitance was measured at 1.15 μF/cm^2 for $V_g = -3$ V. A relatively small hysteresis shift between sweeps indicates a moderate amount of charge trapping at the gate:diamond interface. This may be influenced by the hydrogen termination, resulting in an increased density of states at the surface if hydrogen is lost. Defects within either the diamond surface or the gate material may also impact trapping.

Equation (2) shows the relationship between R_{ON} and effective mobility (μ_{eff}) [18], [19], where C_g is the measured gate capacitance and R_{sd} is the sum of contact and access resistances. For a capacitance of 1.15 μF/cm^2 extracted from a 400-nm L_g device, effective mobility can be estimated as 23.5 cm^2 V^{-1} s^{-1}. Ideally, a much larger gate length would provide greater accuracy when calculating effective mobility in this manner due to uniformity of carriers beneath the gate. As such, the calculated value remains an estimate.

$$R_{ON} = \frac{L_g}{W_g \times \mu_{eff} \times C_g \times (V_{gs} - V_{th})} + R_{sd} \quad (2)$$

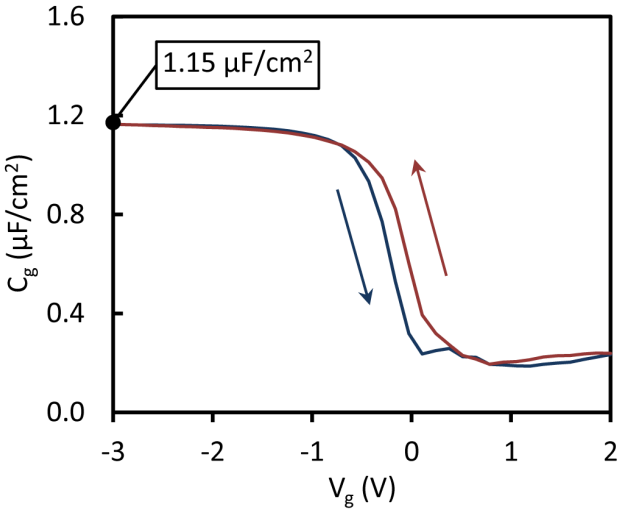

Fig. 5. C–V measurement for a device of $L_g = 400$ nm. $V_g = -3$ to 2 V. Arrows indicate direction of the sweep.

For traditionally doped semiconductors, in which resistivity remains relatively consistent across the substrate, sheet hole density (p) can then be determined by the following equation:

$$\mu_{eff} = \frac{1}{qpR_{sheet}} \quad (3)$$

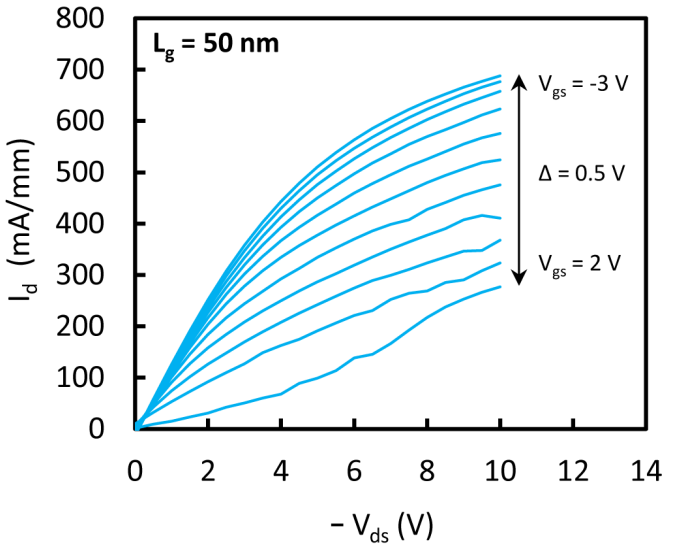

Fig. 6. *I–V* output for a 50-nm gate device. $V_{ds} = 0$ to -10 V and $V_{gs} = -3$ to 2 V.

Taking the measured value for R_{sheet} and the electron charge constant q (1.6×10^{-19} C), sheet hole density is then estimated as 3.9×10^{13} cm^{-2}. These values for carrier density and mobility are within the typical ranges reported for transition metal oxide doping of hydrogen-terminated diamond [8]. However, the value for carrier density calculated from (3) is an approximation due to the probable difference in sheet resistance between the access regions and beneath the gate contact. In a transfer-doped diamond MESFET, the electron accepting medium (in this case V_2O_5) is not present under the gate. Therefore, while unknown, the carrier density beneath the gate is very likely to differ from that of the access regions.

Further biasing a 50-nm device to $V_{ds} = -10$ V achieved a peak drain output of ~700 mA/mm (Fig. 6). OFF-state performance significantly worsens as the small gate length struggles to modulate the high current. These values for drain current are substantially higher than those reported elsewhere for a diamond V_2O_5 FET [17], [20], [21]. Both I_d saturation and channel pinch-off could not be achieved prior to gate failure. In this instance, performance is limited by gate instability and short channel effects as evidenced by the change in V_{th} with decreased gate length. As L_g is reduced, the device turns on at a more positive gate voltage. This is in part due to the relatively small access regions resulting in trapezoidal regions at both the source and drain forming a channel below the depletion region of the small gate contact. In a planar FET, decreasing gate length also results in drain-induced barrier lowering (DIBL) [22]. This effect is further exacerbated by increased drain voltage, as can be seen for $V_{gs} = 2$ V in Fig. 6. An example of DIBL is shown in Fig. 7. At these small dimensions, increasing drain bias can result in V_{ds}-induced shift of V_{th} for the device. As V_{ds} increases further, the drain will have a growing influence on the OFF-state performance. A comparative study of MESFET devices on diamond, down to 50-nm gate length, has previously been reported [23]. In that work, the smallest device exhibited

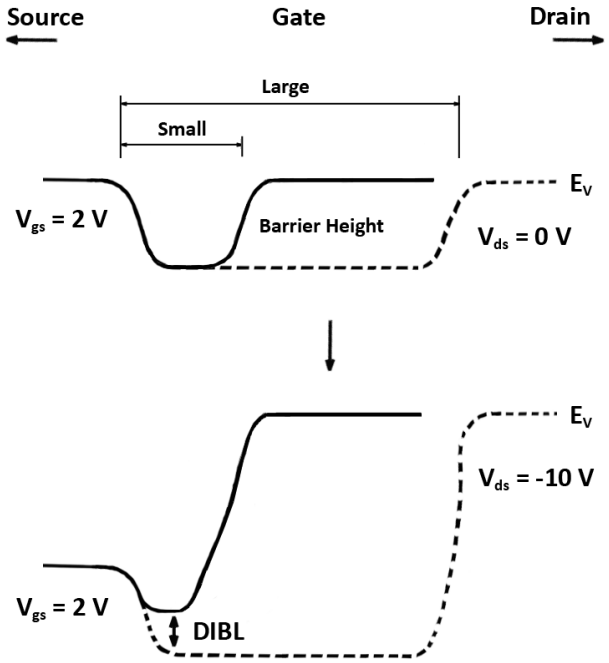

Fig. 7. Diagrammatic example of DIBL, showing smaller (solid line) and larger (dashed line) gate lengths. For the small gate length, increasing drain bias will begin to reduce the potential barrier formed by the gate.

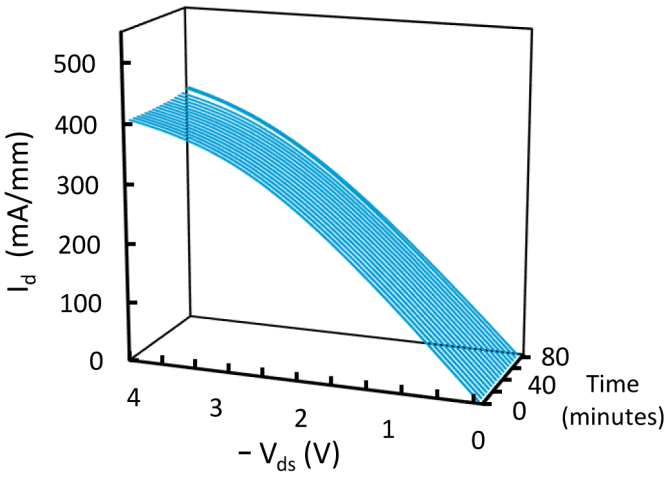

Fig. 8. *I–V* output for a 200-nm L_g device, 17 iterations of $V_{ds} = -4$ V, $V_{gs} = -3$ V with 5-min intervals.

better control of the OFF-state leakage current. However, this was likely due to the significantly larger access regions and lower carrier density which resulted in 54% lower peak drain current.

To demonstrate stability of the V_2O_5-induced transfer doping with repeat measurement, a device of 200-nm L_g was swept 17 times at intervals of 5 min between sweeps. Plotted in Fig. 8, at peak I_d ($V_{ds} = -4$ V, $V_{gs} = -3$ V) a standard deviation of 3.1 mA/mm was observed. This stability of the V_2O_5-doped channel under electric fields is highly promising and was also suggested here [21].

Prior work has demonstrated the hygroscopic nature of transition metal oxides such as V_2O_5, resulting in reduced work function of the material over time when exposed to

ambient atmosphere [8], [24]. To observe any degradation in transfer doping of the diamond, sheet resistance measurements were taken over a period of 11 days while the sample was periodically moved between a probe station and N_2 box. The results showed a 12% increase in sheet resistance over the time period measured. This effect of reduced transfer doping efficiency for V_2O_5 and MoO_3 has been discussed here [8], with an observed reduction in carrier concentration of the diamond due to the oxides degrading work function in ambient air. Hermetic encapsulation of the transition metal oxide to isolate from atmosphere is thus recommended to maintain conductivity.

IV. Conclusion

Diamond FETs with V_2O_5 as a transfer doping medium and a range of gate lengths down to 50 nm were fabricated and characterized. We observe a significant improvement in peak output current up to ∼700 mA/mm and a peak transconductance of ∼150 mS/mm, when compared to what has been reported thus far. Due to encapsulation with V_2O_5, device stability with repeat measurement is achieved. However, isolation of the oxide film from atmosphere is still required. This work demonstrates the performance gains which can be achieved through scaling of critical dimensions and adoption of transition metal oxides for the production of diamond FET devices. Further work will look to improve upon gate formation and combat short channel effects, which have a detrimental impact on OFF-state performance at such small gate lengths.

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