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Modified T-type topology of three-phase multi-level inverter for photovoltaic systems

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ABSTRACT

In this article, a three-phase multilevel neutral-point-clamped inverter with a modified t-type structure of switches is proposed. A pulse width modulation (PWM) scheme of the proposed inverter is also developed. The proposed topology of the multilevel inverter has the advantage of being simple, on the one hand since it does contain only semiconductors in reduced number (corresponding to the number of required voltage levels), and no other components such as switching or flying capacitors, and on the other hand, the control scheme is much simpler and more suitable for variable frequency and voltage control. The performances of this inverter are analyzed through simulations carried out in the MATLAB/Simulink environment on a three-phase inverter with 9 levels. In all simulations, the proposed topology is connected with R-load or RL-load without any output filter.

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1. INTRODUCTION

Multilevel inverters are currently preferred over conventional two or three level inverters due to their proven advantages [1]-[3]. In fact, multilevel inverters offer the advantage of reducing the voltage constraints applied to power semiconductors, which allows these inverters to be able to transfer higher powers with dv/dt and di/dt much lower than those obtained with two or three level inverters [2]-[4]. Also, multilevel inverters allow reducing electromagnetic interference (EMI) and total harmonic distortion (THD) of the output signals, which allows to reduce the size of the output filter [5]-[7]. Certainly, multilevel inverters also have some disadvantages such as: the number of semiconductors and/or voltage sources (isolated or not) necessary for the operation of these inverters, which increases with the required number of voltage levels [6], [8]. Also, some structures of multi-level inverters require the use of other components such as capacitors or transformers [9]-[11], which leads to a more complex structure and an increase of the overall price of the inverter. In the literature of multilevel inverters, several structures are proposed to improve the three classic topologies mentioned above. The improvements concern, on the one hand, to reducing the number of components and switches required, and on the other hand, to reducing stress on the switches [12].

Generally, multilevel inverters are classified into three categories: neutral-point-clamped (NPC) inverters, flying capacitor (FC) inverters, and multi-cell multilevel (ML) inverters. NPC inverters are the

most widely used multilevel inverter topology in high power applications [13]. However, in this type of circuit diagram, the power losses are asymmetrically distributed between the power switches, which lead to a limitation (due to the most heavily used switches) of the power capability at the output of the inverter. For this reason, improvements are made on the basic NPC topology to overcome this drawback by using clamping diodes to balance the converter. In the active neutral-point-clamped (ANPC) topology, the clamping diodes are replaced by transistors with antiparallel diodes for providing a controllable pathway for neutral current [14]-[18]. The structure of multilevel flying capacitor inverters suffers from several disadvantages which limit its use in practice; among these major drawbacks we can cite: the need for capacitor with sufficient value for each voltage level and need for charging circuit for each flying capacitor with complicated procedures for balancing voltage [19]. The Multi-cell multi-level inverters are based on the use of cascaded power cells. The different cells are controlled in a way to have all the configurations allowing producing the required output voltage levels. For this category of converters, a distinction is made between multi-cell cascade h-bridge (CHB) topologies, which require isolated power supply for each basic cell, and modular multi-level converters (MMC) whose cells share the same direct current (DC) voltage source [20]. The major advantage of multicellular topologies is that they are modular, which makes it easier to design and maintain. However, they require a great number of active and passive components. Also, there is the problem of unbalanced voltages across capacitors.

The problem with the majority of the structures proposed above remains in the fact that the switches are generally dependent between them (to generate a determined level of voltage); this increases the complexity of the control for applications requiring root mean square (RMS) value variation of the output voltage [21]-[24]. This article presents a new topology of multi-level inverter switches. This topology needs as many voltage sources connected in series as the levels required [25]. This is why this solution is suitable for solar systems since the batteries and photovoltaic panels are necessarily connected in series to have sufficient voltage for the DC bus.

2. MODIFIED T-TYPE STRUCTURE OF THE INVERTER

The modified T-type topology proposed in this work, is inspired by the basic sub-module shown in Figure 1(a). The neutral is fixed at point N, the output (point A) is connected to $+V_{dc}$ or N or $-V_{dc}$ when S_H or S_0 or SL is on, respectively. Figure 1(b) shows the scheme of an inverter with 5 levels, the performed modification to the switches S_{H1} and S_{L1}, is justified by the fact that these switches must withstand negative voltages when switch S_{H2} or S_{L2} are on. Figure 1(c) shows the proposed structure for 2_{k+1} level inverter. Each voltage source is associated with a switch. The number of voltage levels in this structure can therefore be simply increased by adding pairs of voltage sources and associated switches. It should be noted that for symmetry reasons number of voltage sources must be pair. The switches (S_{H1}, $S_{H2,}$ … S_{H2k+1}) are used to have positive voltages, and (S_{L1}, $S_{L2,}$ … S_{L2k+1}) for negative voltages; while the S_0 switch is closed to have the zero level. Figure 1(d) shows the nine-level three-phase inverter wiring used for simulations. All the switches (except those corresponding to extreme levels ±4 V_{dc}) must be bidirectional.

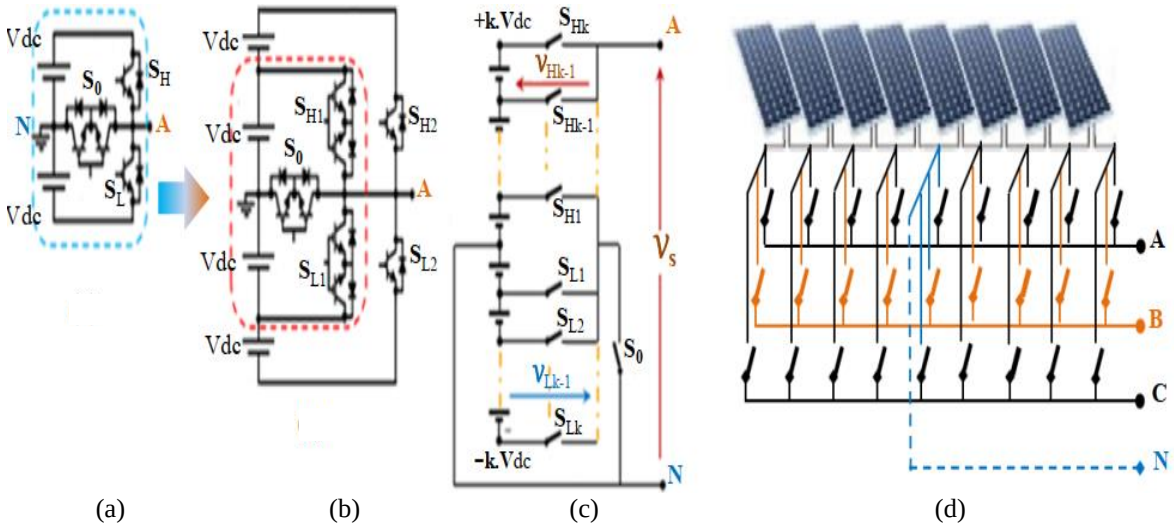


Figure 1. Modified T-type structure (only one phase is presented): (a) T-type sub-module: three-level inverter, (b) five-level inverter, (c) structure of (2k+1) level inverter, (d) nine-level three-phase inverter

2.1. Switches control strategy

Table 1 illustrates the states of the switches to obtain the different possible voltage levels for a nine levels inverter. It may be noted that always only one switch is closed at a time. All The switches except S_{H2k+1} and S_{L2k+1} must be bidirectional voltage, because, once a switch is closed, it imposes a negative voltage on the other open switches. Table 2 gives the different voltages applied to the blocked switches. It is clear that, each switch must withstand a forward voltage equal to twice the voltage of the switched level, and a maximum reverse voltage (for the switch (S_0) connected to the neutral point) equal to the voltage corresponding to the maximum level.

Table 1. Voltage levels and corresponding closed switch of proposed-nine-level inverter

Switch ON	S_{H4}	S_{H3}	S_{H2}	S_{H1}	S_0	S_{L1}	S_{L2}	S_{L3}	S_{L4}
Output voltage	$4V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	0	V_{dc}	$-2V_{dc}$	$-3V_{dc}$	$-4V_{dc}$

Table 2. Voltages applied to each switch used in the proposed structure (case of a 9-level inverter)

Switch ON	Switch Voltage								
	S_{H4}	S_{H3}	S_{H2}	S_{H1}	S_0	S_{L1}	S_{L2}	S_{L3}	S_{L4}
S_{H4}	0	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$7V_{dc}$	$8V_{dc}$
S_{H3}	V_{dc}	0	$-V_{dc}$	$-2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$7V_{dc}$
S_{H2}	$2V_{dc}$	V_{dc}	0	$-V_{dc}$	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$
S_{H1}	$3V_{dc}$	$2V_{dc}$	V_{dc}	0	V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$
S_0	$4V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	0	V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$
S_{L1}	$5V_{dc}$	$4V_{dc}$	$3V_{dc}$	$2V_{dc}$	$-V_{dc}$	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
S_{L2}	$6V_{dc}$	$5V_{dc}$	$4V_{dc}$	$3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	0	V_{dc}	$2V_{dc}$
S_{L3}	$7V_{dc}$	$6V_{dc}$	$5V_{dc}$	$4V_{dc}$	$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	0	V_{dc}
S_{L4}	$8V_{dc}$	$7V_{dc}$	$6V_{dc}$	$5V_{dc}$	$-4V_{dc}$	$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	0

The control strategy of this inverter consists of closing one switch corresponding to the required voltage level. The switches are closed according to the sequence shown in Figure 2 (full arrow to increase the voltage level and empty arrow to decrease it). It should be noted that all the switches (according to the control sequence mentioned above and Table 2 of voltages applied to the switches) have a voltage not exceeding V_{dc} before and after switching, this greatly reduces the voltage constraints on the switches used in this topology.

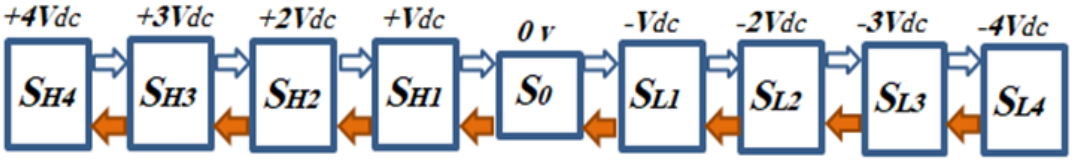
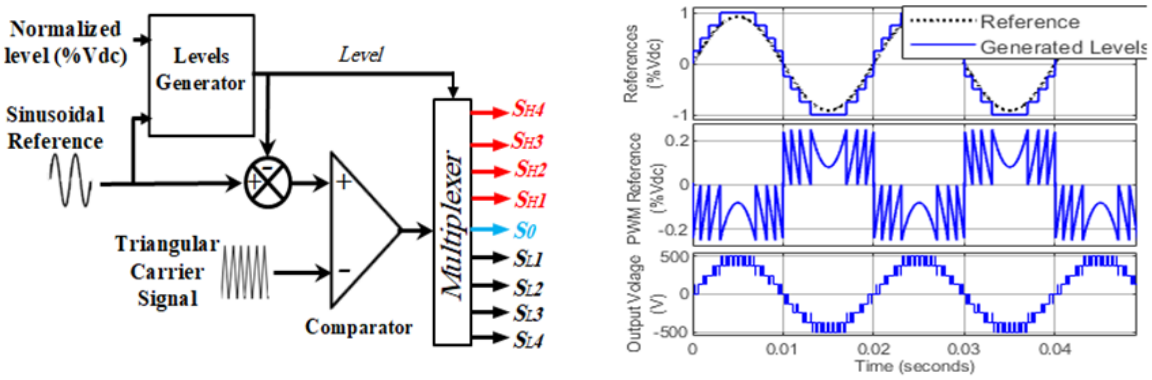


Figure 2. Switch control sequence and output voltage corresponding to the closed switch (case of a 9-level inverter)

2.2. Multilevel PWM scheme

There are many techniques for pulse width modulation; the multi-carrier-based sinusoidal pulse-width modulation (MSPWM) technique (based on the use of multiple carriers) is one of the most generally used modulation methods for multi-level structures. The hybrid multilevel pulse width modulation (HMPWM) consisting of a combination of modified MSPWM and the fundamental frequency modulation (FFM) is a novel technique proposed in [1]. In this article, a single-carrier modulation is used, to achieve the pulse width modulation (PWM) control. The proposed scheme of used PWM is shown in Figure 3(a). It can be seen that it is much simpler to implement this control since it utilizes just comparators and a multiplexer (no phase shifters). The use of multiplexer is justified since in this proposed topology only one switch is ON at any time. This proposed scheme has also the advantage of varying (via the peak value) the root mean square (RMS) amplitude of reference sin wave voltage (in the entire range from 0 to $k \times V_{dc}$) without any modification of the structure. Figure 3(b) shows the different signals obtained according to the proposed modulation scheme. The multiplexer is used to control the switches according to required voltage level as shown in Table 1.



(a) (b)

Figure 3. PWM scheme: (a) proposed block diagram, (b) levels, reference, and output signals

3. SIMULATION RESULTS AND PERFORMANCES EVALUATION

The following simulations of the proposed inverter in this article are performed using MATLAB/Simulink. Table 3 summarizes the simulation parameters. These simulations are performed for a nine-level, nine-switch three-phase voltage inverter used without output filter. The performance evaluation of the proposed multi-level inverter is based on the comparison of the output current electromagnetic interference total harmonic distortions (THDs), in different situations, in particular, for different loads and PWM frequencies. The switching frequencies are chosen not to be high in order to reduce the power losses in the semiconductor components. The output voltage of the inverter must have frequency and RMS voltage fixed by the sinusoidal reference signal. Figure 4 and Figure 5 show the simulation results of the line-to-line voltages, the output currents, and the THD for different loads. All simulations are performed for RMS line reference voltage in the following order: 600 V, 500 V, and 400 V.

It is clear that 2 kHz of PWM frequency is sufficient to obtain less than 0.6% of absorbed current THD, and this is achieved without output filter. By using Fourier analysis, Figure 6 shows that output voltage harmonics are rejected towards high frequencies; this explains the relatively low THD of line current since the inductive loads have low-pass filter behavior.

Table 3. Simulation parameters

Parameters	Values
MATLAB sample time (Ts)	0.5 e-5 s
DC source voltage (Vdc)	125 V
PWM frequency	None/2 kHz
Load active power (reactive power)	30 kVA (cosφ: 0.97-0.6)
Load nominal voltage (RMS)	600 V
Load nominal frequency	50 Hz

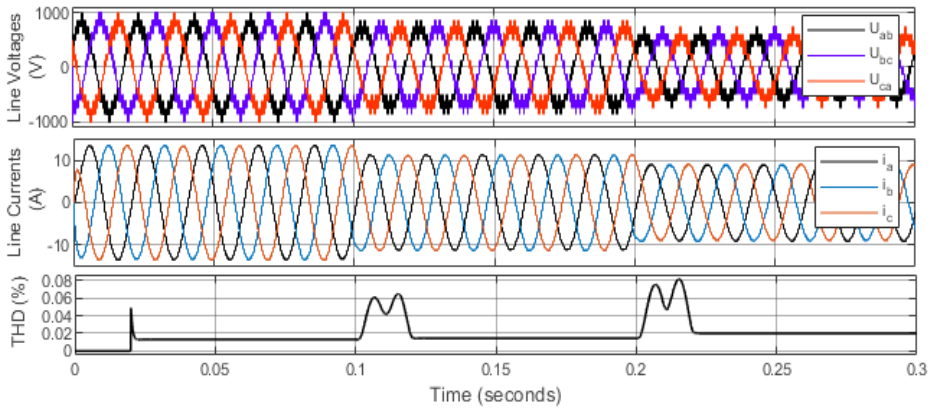


Figure 4. Simulation results of line voltages, line currents and THD (cosφ=0.97, PWM frequency 2 kHz)

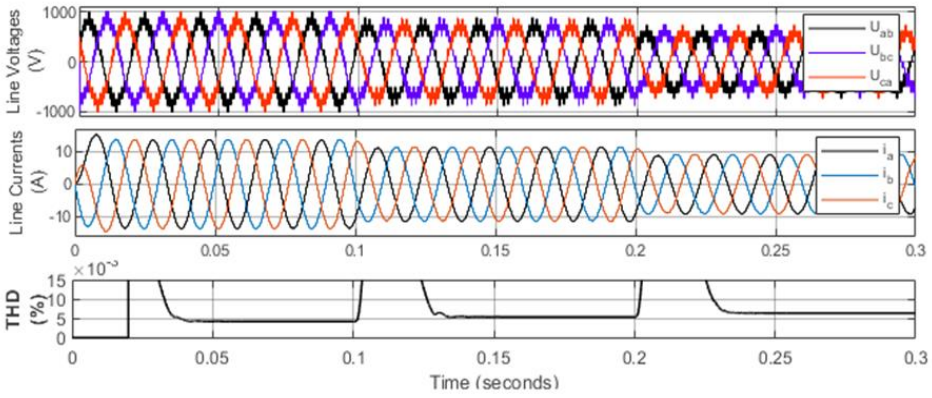


Figure 5. Simulation results of line voltages, line currents and THD (cosφ=0.6, PWM frequency 2 kHz)

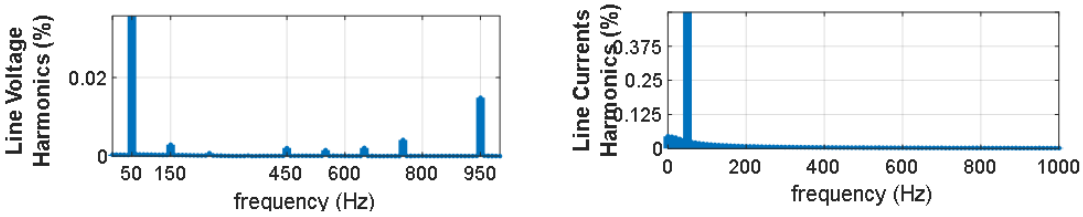


Figure 6. Line voltages and currents spectrums with 2 kHz PWM frequency

Without PWM, Figure 7 shows the simulation results of the line-to-line voltages, the output currents, and the THD. Although the frequency spectrum of the output voltages contains odd harmonic components (from the third harmonic); the use of the multi-level inverter for strongly inductive loads (the case of the load with power factor of 0.6 used in simulation) allows filtering of the absorbed currents and therefore does not necessarily require any output filter as shown in Figure 8. In the case of resistive or weakly inductive loads, an output filter is mandatory; but the design of the output filter is relatively very small compared to conventional inverters for the same power involved.

The terminal voltages of semiconductors (in the off state) in the proposed structure, never exceed voltage of the elementary level (V_{dc}) at switching times. This is illustrated in the example of Figure 9, where current and voltage across S_{H2} switch are represented. It can be seen that all the switching operations are carried out at either voltage $+V_{dc}$ or $-V_{dc}$, which decreases the constraints on the semiconductors and the switching time, and consequently switching losses. In fact, the use of a high number of levels makes it possible to reduce at the same time the stresses applied to the semiconductors and the switching losses by operating at low switching frequency (PWM frequency of a few hundred hertz).

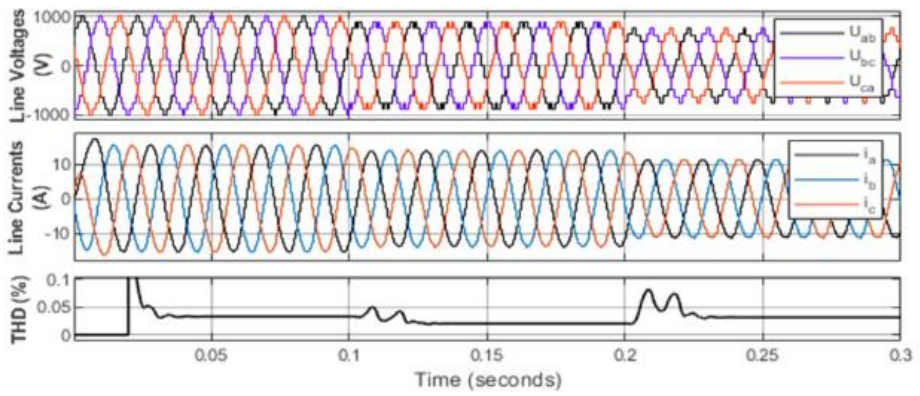


Figure 7. Simulation results of line voltages, line currents and THD (cosφ=0.6, without PWM)

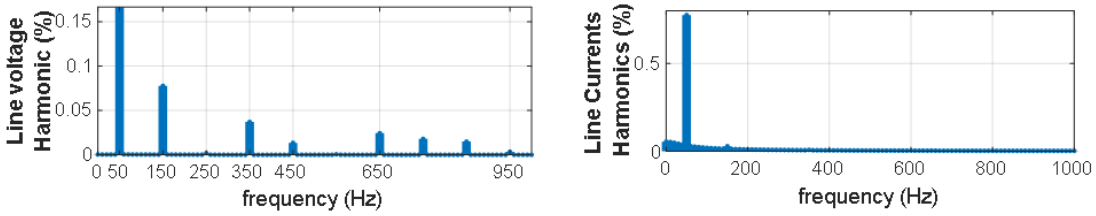


Figure 8. Line voltages and currents spectrums without PWM (load: cosφ=0.6)

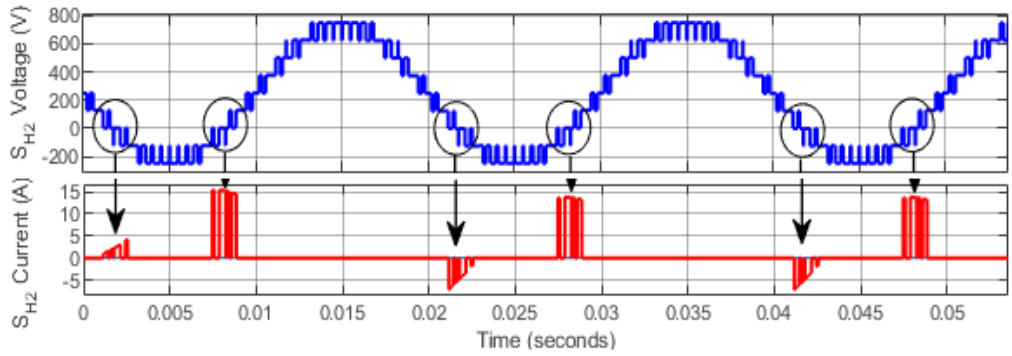


Figure 9. Voltage applied to the switch S_{H3} before and after switching

4. CONCLUSION

In this article, the proposed topology of a multi-level three-phase inverter has been presented. The design of this structure was developed from basic sub-modules. Compared to conventional multi-level inverters, this structure has the following advantages: i) only requires switches (no additional components such as capacitors, clamping diodes), ii) the number of switches is reduced (equal to the required number of levels for each phase), iii) the voltage stresses on the switches and commutation losses are reduced, and iv) the control logic is simple and does not present additional complexities when increasing the number of levels. The major disadvantage of this structure is that the sizing of the switches is not the same for the maximum reverse voltage (V_{RRM}). In fact, some switches (depending on their location in the proposed structure) must be bidirectional in voltage or must withstand the total voltage of the DC bus; but on the other hand, each switch is only activated for one or two time intervals per period of the fundamental signal.

The switches control strategy was developed using a single modulating triangular signal. The proposed scheme makes it possible to control the switches with or without PWM on the one hand, and to vary the RMS value of the output voltage of the inverter. The simulation results have proved the advantages of the proposed topology and the proposed modulation method. Since the proposed structure requires as many voltage sources as required levels, this structure is particularly suitable for use in photovoltaic panel systems, where generally the PV strings are composed of a large number of PV in series. The advantage of choosing a high number of levels makes it possible to reduce the PWM frequency or even eliminate it, thereby improving the performance of the inverter. Finally, our next work consists of the energy study of the structure of the voltage sources string (constituted by the PVs) used with the proposed multilevel inverter, in order to improve the efficiency of the assembly (PVs-proposed multilevel inverter).

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