



This is the **accepted version** of the article:

Ruiz, Ana; Seoane, Natalia; Claramunt, Sergi; [et al.]. «Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability». Applied Physics Letters, Vol. 114, issue 9 (March 2019), art. 93502. DOI 10.1063/1.5090855

This version is available at https://ddd.uab.cat/record/249164 under the terms of the $\bigcirc^{\mbox{\footnotesize IN}}$ license

Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability

A. Ruiz¹, N. Seoane², S. Claramunt¹, A. García-Loureiro², M. Porti¹, C. Couso¹, J. Martin-Martinez¹, M. Nafria¹

¹Electronic Engineering Department, Universitat Autònoma de Barcelona, Barcelona 08193, Spain ² CITIUS, Universidade de Santiago de Compostela, Santiago de Compostela 15782, Spain Electronic address: ana.ruiz@uab.cat

Abstract— A more realistic approach to evaluate the impact of polycrystalline metal gates on the MOSFET variability is presented. 2D experimental workfunction maps of a polycrystalline TiN layer were obtained with Kelvin Probe Force Miscroscopy with nanometer resolution. These data were the input of a device simulator, which allowed to evaluate the effect of the workfunction fluctuations on MOSFET performance variability. We have demonstrated that in the modelling of TiN workfunction variability not only the different workfunctions of the grains but also the grain boundaries should be included.

Index Terms— KPFM, polycrystalline metal gate, variability, MOSFET.

THE continuous scaling of MOSFET dimensions has led to The continuous scaling of Moor E. the introduction of high-k/metal gate stacks in recent technological nodes. However, high-k dielectric polycrystallization has already been shown to be a variability source in ultrascaled MOSFETs affecting its electrical properties¹⁻⁵. Metal gates were also introduced with high-k dielectrics because they have several advantages compared to polysilicon^{6,7}. However, depending on the growth temperature, metals become polycrystalline, leading to grains with different sizes and orientations. Since the grains workfunction (WF) depends on their orientation⁸, the random distribution of grains (with their corresponding WF) results also in variations in the metal WF and threshold voltage variability (TVV)⁹⁻¹¹. Therefore, it is critical to understand the origin of this variability in order to select the best fabrication process and materials that can reduce it.

Some works have already evaluated the impact of the grain orientation induced workfunction variation (WFV) on the variability of MOSFETs. In Ref. 11, for example, it was experimentally demonstrated that the TVV of a MOSFET is affected by the grain size. However, since this study was performed at device level, the individual impact of the WFV on the device properties cannot be separated from other sources as random dopant fluctuation (RDF) or line edge roughness (LER). Other works have evaluated the TVV by means of simulation and statistical models that make assumptions that could be unrealistic 9,10.

In this work, a more realistic approach which relies on 2D experimental WF maps obtained with Kelvin Probe Force Microscopy (KPFM) is proposed to study the impact of metal polycrystallization on the electrical parameters of MOSFETs.

From KPFM measurements, the metal gate WF fluctuations are determined at the nanoscale. This information is then introduced into a device simulator to analyze the impact of the metal granularity on the variability of the device electrical properties.

Experimental data were obtained from a sample containing a 100 nm thick TiN layer grown by continuous e-gun evaporation of metallic Ti over a HfO2/Si substrate. The formation of TiN was ensured by passing the Ti atoms through a reactive nitrogen-enriched atmosphere, at a nitrogen partial pressure of 8·10⁻⁴ mbars. The structure of the TiN layer was determined by X-Ray Diffraction (XRD) using a Panalytical X'PERT PRO with the CuK_{α} line in Bragg-Brentano geometry. The morphological and electrical properties of the polycrystalline metal layer have been measured with a Nano-Observer AFM (from Concept Scientific Instruments), which allows bimodal single pass AM-KPFM measurements to obtain simultaneously topographical and sample-tip contact potential difference (CPD) 2D maps with nanometer resolution^{12,13}. Note that although FM-KPFM usually offers a better resolution than AM-KPFM¹⁴⁻¹⁶, bimodal single pass AM-KPFM measurements, thanks to the smaller tip sample distance, can offer comparable resolution to lift mode FM-KPFM^{14,17,18}. The first flexural eigenmode resonance frequency of the cantilever (f1 = 61.3 kHz) was used to track the topography. The feedback to measure the CPD of the sample works at a frequency around the second eigenmode resonance frequency of the cantilever^{15,19} (f2 = 380 kHz, high enough to avoid any KPFM signal dependence on the frequency²⁰). An internal algorithm selects the working frequency that maximizes the signals used to nullify the electrically driving oscillation, improving the sensitivity of the measurements. Since the ratio f2/f1 is typically 6.2, selfexcitation of second eigenmode through the 6th-harmonic of the first eigenmode is not present in the measurements, minimizing cross-talk between topography and CPD image²¹.

To obtain the CPD image, the tip is biased at VAC = 1 V while the TiN layer is directly connected to ground. Since the CPD data correspond to the difference between the WF of the tip and the metal layer, assuming a constant value of the tip WF during the experiment, the measured CPD variations are related to the WF fluctuations of the metal layer. Therefore, the CPD image provides information of the local value of the WF of the metal. In our case, KPFM images were obtained in air and using a highly doped 20 Si tip (radius $<10\,$ nm) from AppNano.

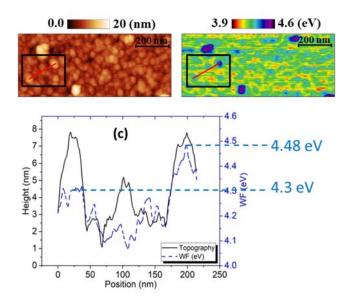


Fig. 1. Topography (a) and WF (b) maps obtained with KPFM on a TiN layer (850 nm x 290 nm). (c) Topographical (continuous line) and WF (dashed line) profile across the line plotted in Fig. 1.a-b.

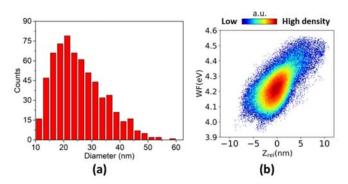


Fig. 2. (a) Histogram showing the distribution of nanocrystals diameter. The average diameter is 25.4 nm. (b) Relationship between the WF and topography (Z-axis relative position, $Z_{\rm rel}$) map pixel by pixel. Color map shows the density of points for each region. $Z_{\rm rel}$ is defined as the Z-position with respect to Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level. The general trend is that depressed areas (regions with low $Z_{\rm rel}$) show lower WF.

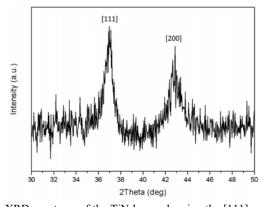


Fig. 3. XRD spectrum of the TiN layer, showing the [111] and [200] orientations of TiN.

Fig. 1a presents a 850 nm x 290 nm topographical image of the TiN layer obtained with KPFM at a scanning rate of 0.2 Hz. Note that it shows a granular structure, which has been attributed to the polycrystallization of the metal layer: grains (Gs) are related to individual (or a cluster of) randomly oriented nanocrystals separated by grain boundaries (GBs, depressions in the topographical image)². A statistical analysis of the Gs diameter has been done using the image analysis software Gwyddion²². Fig. 2a shows a histogram of the grain diameter suggesting an average diameter (Gdiameter) of ~25.4 nm. These results are compatible with values already reported, which point out a large range of diameters, depending on the growth conditions of the layer^{9,10}.

The effect of the metal polycrystallization on the nanoscale WF of the layer was investigated based on the CPD image. Fig. 1b shows the measured WF at the same surface region as in Fig. 1a, suggesting that the WF is not uniform. A granular pattern, as also observed in Ref. 23, overlaps with that of the topographical image. Since the tip WF is not known and absolute values of WF are also very sensitive to ambient conditions²⁰, it has been assumed that the average value of the CPD image is 4.22 eV, which corresponds to the average WF of a TiN metal gate obtained from experimental devices²⁴, and only relative variations will be considered. This assumption does not affect the conclusions of the work because we are interested on the impact of the WF fluctuations on the MOSFET variability.

Fig. 1c shows a topographical (continuous line) and WF (dashed line) profile across the line plotted in Fig. 1a and 1b (inside the black square). Note that, in general, the positions with lower WF are located along the topographical depressions, though Gs with very low WF can also be found. This qualitative observation is verified statistically in Fig. 2b, where the dependence of the WF with the Z-axis relative position (Z_{rel}, defined as the Z-position with respect to the Zaxis mean value of the image, which has been arbitrarily considered to be the zero-reference level) of all the pixels in Fig. 1 is shown. The color scale of Fig. 2b indicates the density of sites with a given WF and Z_{rel}. This figure suggests that, instead of discrete WF values, there is continuous WF distribution that spans from ~4.0 eV to ~4.5 eV. The depressed areas (low Z_{rel}) tend to show lower WF than hillocks. Since depressed areas are associated to GBs (as shown in Fig. 1a and 1c)^{2,23}, the results indicate that Gs tend to have a higher WF value.

In addition to the WF difference between GBs and Gs, the WF of Gs show also a continuous distribution. This distribution can be associated to, on the one hand, a non-homogeneous WF in the G or intra-G variability (see for example the G located at ~200 nm in Fig. 1c) and, on the other, to differences in the WFs between Gs (inter-G variability). To evaluate this inter-G variability, we have considered the maximum value of WF as metric parameter (the same conclusions would have been drawn if the average WF would have been considered instead). Grains with different maximum WF values are measured, as in Ref. 23. As an example, Fig. 1c shows two Gs with a similar height and different maximum WF values (4.30 and 4.48 eV), whose

difference is ~200 meV. This result is compatible with the presence of two grain orientations, [111] and [200], with 0.2 eV⁹ WF difference. The presence of crystals with 2 orientations is further supported by XRD analysis. The XRD spectrum of the TiN layer (Fig. 3) reveals the presence of two peaks, corresponding to aforementioned orientations, being the [111] orientation dominant over the other. However, the KPFM map suggests a continuous distribution of values that spans from ~4.29 eV for low WF values to ~4.5 eV for high WF values²³, within the WFs range of the two crystal orientations. A continuous distribution of WFs is also observed for GBs. In this case, however, WFs range from 4.0 to 4.1 eV, so the WF difference between grains and GBs ranges between ~200 meV and ~500 meV.

The data obtained from KPFM images (WF at the nanoscale) adds new information on the properties of the polycrystalline metal layer compared to the data used in previous works to simulate WFV. Besides the presence of different grain orientations, we have observed that they do not show discrete WF values, but a continuous range of them (due to inter- and/or intra-G variability). Moreover, the presence of GBs with lower WF values is also observed (which were not considered in previous works). Such variations could also affect the electrical characteristics and variability of semiconductor devices and, therefore, they should be taken into account. In order to demonstrate this, the nanoscale information experimentally obtained with KPFM is introduced in a device simulator to study the variability of MOSFETs (due to the WF fluctuations in the metal gate).

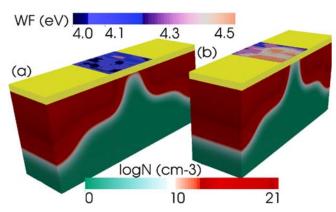


Fig. 4. TiN metal gate experimental profiles that produce the highest (a) and lowest (b) off-currents when considered as the metal gate of a 50 nm gate length Si MOSFET. The electron concentration inside the device, at V_G =0.0 V and V_D =50 mV, is also shown.

To evaluate the impact of the nanoscale WF fluctuations on the device electrical characteristics, a 3D in-house built finite-element drift-diffusion device simulator²⁵ was used. For simplicity, a WxL= 50x50 nm² gate area n-type Si MOSFET with a HfO₂/SiO₂ gate stack was considered. The gate WF value (4.22 eV) and Source/Drain doping were obtained from the appropriate scaling and calibration of a 67 nm effective gate length MOSFET experimental device²⁴. From maps as those shown in Fig. 1, 100 different 50 nm x 50 nm metal gate maps (without overlapping) were obtained and introduced in the device simulator, so that an ensemble of 100 different WF

maps (and, therefore, device configurations) were analyzed. Fig. 4 shows 2 extreme examples of device configurations. Fig. 4a corresponds to a device with very low TiN WF values (mainly occupied with GBs), while Fig. 4b corresponds to a device mainly occupied with Gs with WF values ranging from ~4.29 to ~4.5 eV. The corresponding statistical analysis of the 100 MOSFETs electrical characteristics is presented in Fig. 5 for the off-current (IOFF), subthreshold slope (SS), threshold voltage (V_T) and on-current (I_{ON}) at a low drain bias of 50 mV. The mean value and standard deviation (σ) of the distributions are also indicated in this figure. The V_T, I_{OFF} and SS histograms are clearly asymmetric with behaviors far from the commonly assumed Gaussian distributions, with skewness values $\sim \pm 1$, because of the unbalanced grain WF probabilities. A correlation between Gs/GBs distributions and electrical characteristics of the device can be found, showing, for example, that higher values of WF (as in Fig. 4b) lead to MOSFETs with higher V_T and lower I_{OFF}. Then, from the I_{OFF} and V_T histograms in Fig. 5, it can be concluded that the probability of occurrence of Gs with extreme high WF values (4.5 eV), is extremely low.

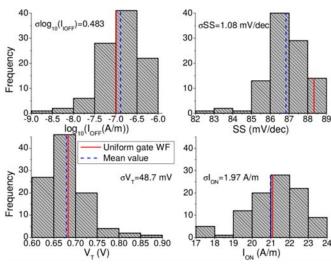


Fig. 5. Distributions of I_{OFF} , SS, V_T and I_{ON} due to the experimentally observed WFV for a 50 nm gate length Si MOSFET at a drain bias of 50 mV. The mean value and standard deviation (σ) of the statistical ensembles are indicated, together with the values obtained for a device with a uniform gate WF (set to 4.22 eV).

To perform a fair comparison between our WF variability results and those previously published by Wang et. al. 26 , corresponding to a 35 nm gate length (GL) MOSFET, the ratio $G_{diameter}$ /GL needs to be used 27 . When comparing results with a similar $G_{diameter}$ /GL value of 0.5, our predicted σ V_T (\sim 49 mV) is around 10% lower than that reported by Wang. These large variability values explain why WFV is currently considered one of the major sources of variability impacting device's performance. However, most of the previously TiN WFV published studies $^{26-29}$ assume that TiN has only two possible WF values spanning 0.2 eV with probabilities of

occurrence 60% and 40%30. Our results demonstrate that such assumption is quite simplistic since in real materials GBs may be present. We have observed a maximum excursion in V_T values of 0.28 V (see Fig. 5), being the mean V_T of the distribution, 0.68 V, a value lower than the one obtained for a device with a gate only composed of Gs with extreme low WF values of 4.29 eV (0.75 V). This indicates a heavy influence of the GBs (with WF values ~ 4.0 eV) in the statistical distribution. Note that, the gate of the device that exhibits the highest off-current (see Fig. 4a) is mainly occupied by GBs and Gs with WF values ranging from ~4.0 to ~4.3 eV. Therefore, the influence of the GBs should not be disregarded when modelling metal gate WFV.

In summary, the impact of the metal gate polycrystallization on the variability of MOSFET devices has been studied using a combination of 2D experimental WF maps obtained with KPFM and a device simulator. The KPFM shows WF variations between Gs and GBs (being the WF lower in the GBs). Though two crystal orientations are observed (supported by XRD data), a continuous distribution of WFs is measured. Regions of the WF images have been mapped onto the gate of a MOSFET, to evaluate the device I_D-V_G curves. This procedure is a more realistic approach for the analysis of the device-to-device variability (due to the presence of different grain orientations) since nanoscale differences of the metal WF are considered from direct experimental data. Though TiN layers have been considered as case study, the proposed methodology can be extended to any metal layer (polycrystalline or not) and growth conditions, since the electrical properties only depend on the WF.

This work has been partially supported by the Spanish AEI and ERDF (TEC2016-75151-C3-1-R, TEC2014-53909-REDT and RYC-2017-23312).

- ¹ K. Shubhakar, K.L. Pey, S.S. Kushvaha, S.J. O'Shea, N. Raghavan, M. Bosman, M. Kouda, K. Kakushima, and H. Iwai, Appl. Phys. Lett. 98, 072902
- V. Iglesias, M. Porti, M. Nafría, X. Aymerich, P. Dudek, T. Schroeder, and G. Bersuker, Appl. Phys. Lett. 97, 262906 (2010).
- ³ C. Couso, M. Porti, J. Martin-Martinez, A.J. Garcia-Loureiro, N. Seoane, and M. Nafria, IEEE Electron Device Lett. 38, 637 (2017).
- ⁴ O. Pirrotta, L. Larcher, M. Lanza, A. Padovani, M. Porti, M. Nafría, and G. Bersuker, J. Appl. Phys. 114, 134503 (2013).
- ⁵ K. Murakami, M. Rommel, B. Hudec, A. Rosová, K. Hušeková, E. Dobročka, R. Rammula, A. Kasikov, J.H. Han, W. Lee, S.J. Song, A. Paskaleva, A.J. Bauer, L. Frey, K. Fröhlich, J. Aarik, and C.S. Hwang, ACS Appl. Mater. Interfaces 6, 2486 (2014).
- ⁶ A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, K. Matsuo, T. Shibata, Y.

- Tsunashima, K. Suguro, and T. Arikado, IEEE Trans. Electron Devices 48, 1604 (2001).
- W.P. Bai, S.H. Bae, H.C. Wen, S. Mathew, L.K. Bera, N. Balasubramanian, N. Yamada, M.F. Li, and D.L. Kwong, IEEE Electron Device Lett. 26, 231 (2005).
- ⁸ H. Dadgour, K. Endo, D. Vivek, and K. Banerjee, Tech. Dig. Int. Electron Devices Meet. IEDM 3, 5 (2008).
- ⁹ H.F. Dadgour, K. Endo, V.K. De, and K. Banerjee, IEEE Trans. Electron Devices 57, 2515 (2010).
- 10 N.M. Idris, A. Brown, J. Watling, and A. Asenov, Ultim. Integr. Silicon 165
- (2010). ¹¹ K. Ohmori, T. Matsuki, D. Ishikawa, T. Morooka, T. Aminaka, Y. Sugita, T. Chikyow, K. Shiraishi, Y. Nara, and K. Yamada, Tech. Dig. - Int. Electron Devices Meet. IEDM (2008).
- ¹² V. Iglesias, M. Lanza, K. Zhang, A. Bayerl, M. Porti, M. Nafría, X. Aymerich, G. Benstteter, Z.Y. Shen, and G. Bersuker, Appl. Phys. Lett. 99, 103510 (2011).
- ¹³ T. Berthold, G. Benstetter, W. Frammelsberger, R. Rodríguez, and M. Nafría, Thin Solid Films 584, 310 (2015).
- ¹⁴ J.L. Garrett, D. Somers, and J.N. Munday, J. Phys. Condens. Matter 27, 214012 (2015).
- ¹⁵ S.A. Burke, J.M. Ledue, Y. Miyahara, J.M. Topple, S. Fostner and P. Grütter, Nanotechnology, 20, 264012 (2009).
- ¹⁶ T. Glatzel, S. Sadewasser, and M.C. Lux-Steiner, Appl. Surf. Sci. 210, 84
- (2003).

 T. Ouisse, M. Stark, F. Rodrigues-Martins, B. Bercu, S. Huant, and J. Carron Mater. Phys. 71, 205404 (200 Chevrier, Phys. Rev. B - Condens. Matter Mater. Phys. 71, 205404 (2005).
- ¹⁸ T. Ouisse, F. Martins, M. Stark, S. Huant, and J. Chevrier, Appl. Phys. Lett. 88, 043102 (2006).
- ¹⁹ Y. Miyahara, J. Topple, Z. Schumacher, and P. Grutter, Phys. Rev. Appl. 4, 054011 (2015).
- ²⁰ C. Baumgart, A. Müller, F. Müller, and H. Schmidt, Phys. Status Solidi A 208, 777 (2011).
- ²¹ G. Li, B. Mao, F. Lan, and L. Liu, Rev. Sci. Instrum. **83**, 113701 (2012).
- ²² D. Nečas and P. Klapetek, www.gwyddion.net.
- ²³ C.I. Enriquez-Flores, E. Cruz-Valeriano, A. Gutierrez-Peralta, J.J. Gervacio-Arciniega, E. Ramírez-Álvarez, E. Leon-Sarabia, and J. Moreno-Palmerin, Surf. Eng. 34, 660 (2018).
- ²⁴ A.J. García-Loureiro, K. Kalna, and A. Asenov, AIP Conf. Proc. 780, 239 (2005).
- ²⁵ A.J. Garcia-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez, and K. Kalna, IEEE Trans. Comput. Des. Integr. Circuits Syst. 30,
- ²⁶ X. Wang, A.R. Brown, N. Idris, S. Markov, G. Roy, and A. Asenov, IEEE Trans. Electron Devices 58, 2293 (2011).
- ²⁷ D. Nagy, G. Indalecio, A.J. García-Loureiro, M.A. Elmessary, K. Kalna, and N. Seoane, IEEE Trans. Electron Devices 64, 5263 (2017).
- ²⁸ S.M. Nawaz and A. Mallik, IEEE Electron Device Lett. **37**, 958 (2016).
- ²⁹ R. Saha, B. Bhowmick, and S. Baishya, IEEE Trans. Electron Devices **64**, 969 (2017).
- 30 H.F. Dadgour, K. Endo, V.K. De, and K. Banerjee, IEEE Trans. Electron Devices 57, 2504 (2010).