Experimental verification of memristor-based material implication NAND operation

M. Maestro, J. Martin-Martinez, A. Crespo-Yepes, M. Escudero, R. Rodriguez, M. Nafria, X. Aymerich and A. Rubio

Abstract— Memristors are being considered as promising devices for highly dense memory systems as well as the potential basis of new computational paradigms. In this scenario, and in relation with data processing, one of the more specific and differential logic functions is the material implication logic also named as IMPLY logic. Many papers have been published in this framework but few of them are related with experimental works using real memristor devices. In the paper authors show the verification of the IMPLY function by using Ni/HfO_2/Si manufactured devices and laboratory measurements. The proper behavior of the IMPLY structure (2 memristors) has been shown. The paper also verifies the proper operation of a two-steps IMPLY-based NAND gate implementation, showing the electrical behavior of the circuit in a cycling operation. A new procedure to implement a NAND gate that requires only one step is experimentally shown as well.

Index Terms— IMPLY function, material implication, memristive circuits, memristors, NAND gate implementation, resistive switching.

I. Introduction

Memristors, firstly introduced in 1971 by L. Chua [1] and later revisited by the research group of S. Williams from HP Labs in 2008 [2], present very advantageous characteristics such as fast operation, high scalability and low power consumption [3]–[11] as well as non-volatility. These features have attracted the interest of the scientific community to study memristors as potential candidates to implement complex memory blocks [3], [11], neuromorphic systems [12], [13], analog and digital processing circuits [14]–[19] and in-memory computation systems [20], [21]. In this sense, one of the most innovative and interesting applications of memristors is data computing. Memristors introduce new paradigms to implement logic computing, not based on the traditional Von Neumann architecture where the data are separately stored in memory and processed in a processor, but overlapping them in the same structure [21], [22]. In this sense, memristor-based material implication (IMPLY) logic gate was proposed in [14] as a 'stateful' logic where the data can be processed and stored in the same element. Several works have explored the use of material implication for logic applications. In [23], several strategies for arithmetic operations with memristors-based structures are described and the design of an adder and a multiplier is presented. In [24] the authors also examine the use of memristors to design different types of adders. In [25], a design methodology of the IMPLY logic family, including some design requirements to support the IMPLY logic family are described. However, these and most of the works presented in the literature are only based on simulations and a lack of experimental works related to material implication logic implemented with real devices is observed. Between the very few experimental works presented in the literature, in [26] a study of material implication-based gates is done, but using SiOx-based memristors and it is only focused on the IMPLY gate. Therefore, experimental works to finally demonstrate the functionality of the material implication-based logic circuits and to verify the promising results expected from simulations are still needed. Thus, in this paper, a deeper experimental investigation to contribute to the final validation of the use of material implication as a new paradigm of computing architecture is performed.

Usage of memristors in IMPLY gates can be shown thanks to the Resistive Switching (RS) phenomenon which takes place in Metal-Insulator-Semiconductor or Metal-Insulator-Metal (MIS/MIM) structures and consists in successive changes between two different resistance states of the dielectric named Low Resistance State (LRS) and High Resistance State (HRS), showing a memristive behavior. Unipolar resistive switching in MIS memristors can be described by thermochemical processes [27]. First change from HRS to LRS is possible due to the growth of a conductive filament along the insulator region, connecting top electrode and bottom electrode. Filament formation is governed by the temperature and field-induced generation of defects [28]. On the contrary, in LRS-HRS change, the previously formed filament is partially destroyed limiting the conduction between the top electrode and the bottom electrode. This process is controlled by thermally enhanced diffusion of top electrode atoms induced by local joule heating [28]. The HRS and LRS states can be related with the two Boolean values implicated in

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digital operations, '0' and '1', allowing the implementation of logic gates with memristors in which material implication is based [26].

Section II describes the composition of the experimental devices employed in the work and we revisit the principles of the IMPLY function [14]. In section III, the IMPLY and NAND logic gates with memristors [29] are experimentally demonstrated on fabricated MIS-memristors. Moreover, in section IV a new procedure to perform the NAND logic operation is proposed, which reduces the number of sequential steps from 2 [14] to 1 as proposed in previous works [20]. Other memristor-based NAND implementations can be found in the literature but with more complex architectures [30] or with more than 2 steps operation procedure [19]. The procedure to improve NAND gate implementation can be extended to perform other logic gates, with the subsequent saving of the computing time. Finally, section V concludes with a summary of the main results.

II. MEMRISTORS DESCRIPTION

Fabricated memristors used in this work are Ni/HfO_2/Si MIS devices based on (100) n-type CZ silicon wafers with resistivity between 0.007Ωcm and 0.013Ωcm [31]. After standard wafer cleaning, a wet thermal oxidation process was done at 1100ºC leading to a 200nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the high-k deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in Hf(5%) were performed. Subsequently, 20nm-thick HfO_2 layers were grown by atomic layer deposition (ALD) using Tetrakis (dimethylamido)-hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. The deposition temperature was 225ºC. The top metal electrode, consisting of a 200nm-thick Ni layer, was deposited by magnetron sputtering. The resulting structures are square cells of 5x5μm². A schematic cross-section of the final device structure is shown in Fig. 1.

In Fig. 2, typical I-V characteristic of a memristor is depicted. Voltages at which samples change from HRS to LRS (V_{SET}) and from LRS to HRS (V_{RESET}) and current at LRS (I_{LRS}, I_{ON}) and at HRS (I_{HRS}, I_{OFF}) are also indicated. In these samples, which present both bipolar and unipolar behavior, the unipolar type with negative voltage polarity to trigger set and reset processes gives the best endurance results of the RS phenomenon [32], [33]. More than 3000 cycles of negative switching can be reached [32]. During SET process, current was limited to 250μA to guarantee good functionality of the memristor. An analysis of the energies involved in the triggering of the set and reset

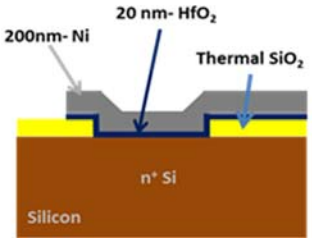


Fig. 1. Cross-section of the memristor device used in this work.

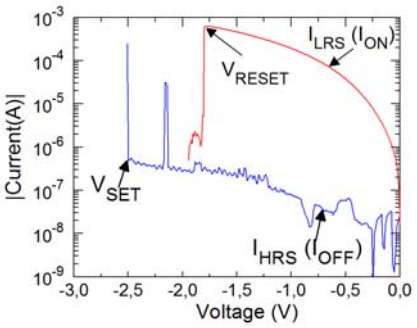


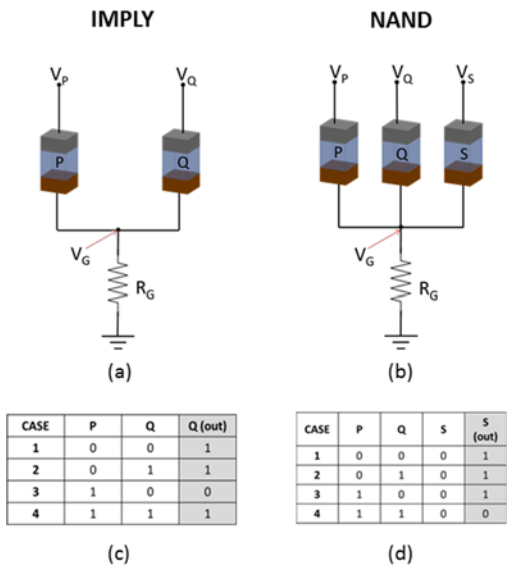
Fig. 2. Typical I-V characteristic of the memristors used in this work. Voltage polarity to provoke Set and Reset processes is negative.

mechanisms, which are of the order of pJ and μJ, respectively, can be found in [34]. On the other hand, the stability and variability of these samples has been previously presented in [32], [33]. Cycle-to-cycle variability, in voltages and currents, seems to be important, although, not so relevant for the gate functionality. Despite the fact that the goal of this paper is not the study of variability implications, device-to-device variability has been also observed to decrease gate operation success percentages. To perform all the measurements presented in this work, 15 samples were used.

In the memristor samples employed in this work, initially, approximately 20 cycles changing successively between LRS and HRS were performed on each memristor, in order to achieve a stable behavior of the conductive filament generation/destruction. After this previous forming process, successive changes between the HRS and LRS in the cell can be performed with set and reset voltages and currents in a reduced range of values. When memristor is at HRS (see Fig. 2), there is a low current flow, I_{OFF}, due to the fact that the conductive filament is partially broken and, digitally, this state is associated to a '0' Boolean value. On the contrary, when memristor is at LRS (Fig. 2) a significant current flow, I_{ON}, is allowed through the conductive filament. In this case, this state is associated to the Boolean value '1'. In this work, instead of evaluating the memristor resistance, we have considered the values of I_{OFF} and I_{ON} currents (measured at -0.8V) as a measure of the '0' and '1' logic states, respectively, for an easier understanding of the experimental results. Therefore, the maximum value of memristor current to be considered as '0' has been stablished at 0.1μA, whereas the minimum value achievable for the current to be '1' state has been 10μA.

III. MEMRISTORS-BASED LOGIC GATES DESCRIPTION

Fig. 3 (a) schematically shows an IMPLY gate, where two memristors (P and Q) have their bottom electrodes connected to a resistance (R_G), which has the other terminal grounded. Top electrodes of memristors are used to apply operational voltages, V_{COND} and V_{IMPLY} (in the literature this voltage is labeled as V_{SET}, however to avoid misunderstanding with V_{SET} in Fig. 2, V_{IMPLY} is considered instead), in order to implement the IMPLY truth table



CASE	P	Q	Q (out)
1	0	0	1
2	0	1	1
3	1	0	0
4	1	1	1

(c)

CASE	P	Q	S	S (out)
1	0	0	0	1
2	0	1	0	1
3	1	0	0	1
4	1	1	0	0

(d)

Fig. 3. (a) IMPLY and (b) NAND gates schematic circuits. (c) IMPLY and (d) NAND gates truth tables

shown in Fig. 3(c). The gate operates as 'P implies Q' or 'if P then Q', being the state of Q the output of the gate. The possible combinations of the initial logic states of memristors P and Q result in four different cases, as it is indicated in the table. In case 1, for example, both memristors must be initially at HRS, i.e. '0' logic state, then, when the proper voltage values are applied to the memristors, Q state changes to LRS because the voltage drop across it is enough to provoke such resistance change. On the contrary, the state of P remains unaltered keeping '0' logic state since its voltage drop is below the voltage necessary to originate a resistance state change. For the rest of the cases, no state change is provoked in any of the memristors. Applying the same operational voltage values as in case 1, initial logic states are kept accomplishing the truth table in Fig. 3(c). A detailed circuital analysis of the IMPLY gate can be found in [15].

The IMPLY gate can be the basis to implement other logic gates. Fig. 3(b) shows the schematics of a NAND gate. The structure is similar to the IMPLY gate but, in this case, a third memristor (S), biased with V_S, is added to P and Q of the IMPLY gate as indicated in the Fig. 3(b) [25]. The output of the NAND cell is stored in the state of memristor S. The truth table of the NAND gate is indicated in Fig. 3(d). Note that R_G value has been 1MΩ, in order to accomplish the relation $R_{ON}<R_G<R_{OFF}$ as indicated in [14]. R_{ON} and R_{OFF} have been in average lower than 50kΩ and larger than 50MΩ, respectively.

IV. Experimental Verification of the IMPLY and NAND Gates

A. Experimental setup

For all the measurements, a semiconductor parameter analyzer (SPA) Agilent 4156C has been used to applied the operation voltages and register the current through memristors. For every memristor involved in the logic gate, source measurement units (SMUs) have been connected (2 SMUs for IMPLY case and 3 for NAND case). Additionally, a voltage source unit (VMU) was connected to monitor the voltage V_G. For the initialization step, voltage ramps were separately applied to every memristor to switch memristors to '0' or '1' state according to the case. Then, to perform the operation step, constant voltages were simultaneously applied to the memristors involved in such a step. After several attempts, trying different voltages values, finally the chosen operation voltages have been V_{COND} = -2V and V_{IMPLY} = -4V, which are the ones that produce the better IMPLY gate performance in most of the analyzed gate cases. Eventually, the final states of memristors were measured applying a small voltage ramp up to -0.8V.

B. IMPLY logic gate

For the IMPLY experimental measurements using the circuit shown in Fig. 3(a), one of the cases from 1 to 4 of the truth table (Fig. 3(c)) is selected. Memristors P and Q are initialized to those states corresponding to the selected case, that is '0' (memristor at HRS) or '1' (memristor at LRS). Operation voltages (V_P and V_Q) are applied to change the initial Q state (for case 1) or to keep it for the rest of the cases. Operational voltages applied to memristors do not depend on the considered case. For our devices, the voltage applied to P is $V_P = V_{COND}$ = -2V and $V_Q = V_{IMPLY}$ = -4V to Q. Currents through P and Q and the voltage, V_G, are now measured to verify the memristors states, both before and after the voltage application.

Fig. 4 shows states of the memristors for the four IMPLY cases (from top to bottom, case 1 to case 4). The states of P and Q before (initial states) and after (final states) operation are shown expressed in terms of the current flowing through the devices (equivalent to the devices' resistances). We can observe that the truth table is accomplished correctly.

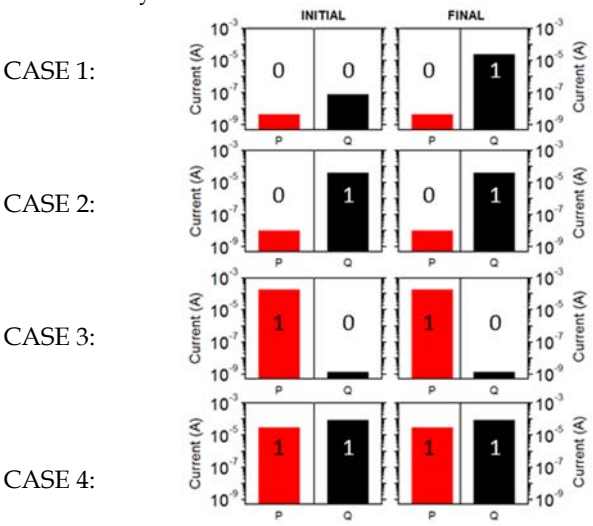


Fig. 4. Initial and final states of memristors P and Q involved in the IMPLY Logic Gate. Q final state corresponds to the output of the gate.

C. NAND logic gate

A NAND gate has also been verified using the circuit

shown in Fig. 3(b). Similarly, as for the IMPLY gate, after the initial forming cycles of each memristor, a particular case of the NAND truth table is selected. Then, the three memristors are initialized to the corresponding states (Fig. 3(d)). In this case, the procedure consists of two different sequential steps (Fig. 5). In the first step, an IMPLY operation between memristors P and S is performed, whose operation voltages are $V_P = V_{COND} = -2V$ and $V_S = V_{IMPLY} = -4V$. Once the required S state is reached (S′), subsequently, a second IMPLY operation, between Q and S (at S′ state) takes place applying $V_Q = V_{COND} = -2V$ and $V_S = V_{IMPLY} = -4V$. This final state of S (S′′) is established as the output of NAND gate.

Fig. 6 shows the experimental four NAND cases successfully performed (from top to bottom cases 1-4). Initial and final states are depicted for each memristor. An additional S state (intermediate state, after the first operation step) is included to confirm that the first IMPLY operation between memristors P and S has been successful.

Besides the single NAND cases measurements, successive measurements of the four NAND cases have also been performed. After each operation, a new case is chosen randomly and later the experimental procedure above mentioned to analyze the NAND gate is followed. Fig. 7 shows memristors states (initial and final) for several successful cycles for each of the four NAND cases (case 1-case 4 from top to bottom). As in Fig. 6, intermediate S

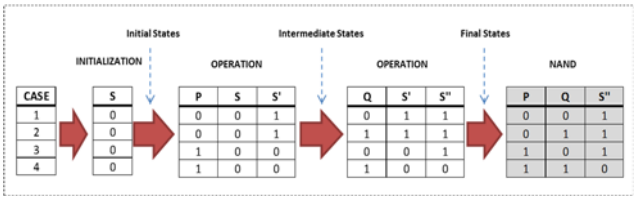


Fig. 5. Schematic sequence flow for NAND measurements involving two IMPLY operation steps.

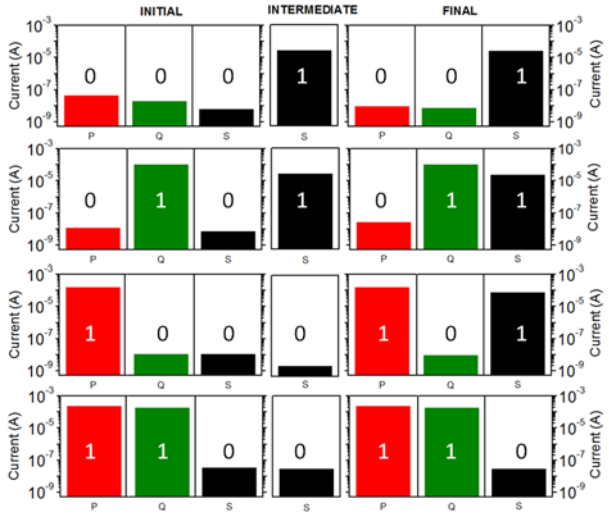


Fig. 6. NAND implementation with two IMPLY operation steps. The first one is between memristors P and S with the output state stored in the S. The second IMPLY operation is between Q and S, being the initial state of S the output of the previous IMPLY operation. After the first operation step, state of S is included to verify that the first IMPLY operation is well-performed.

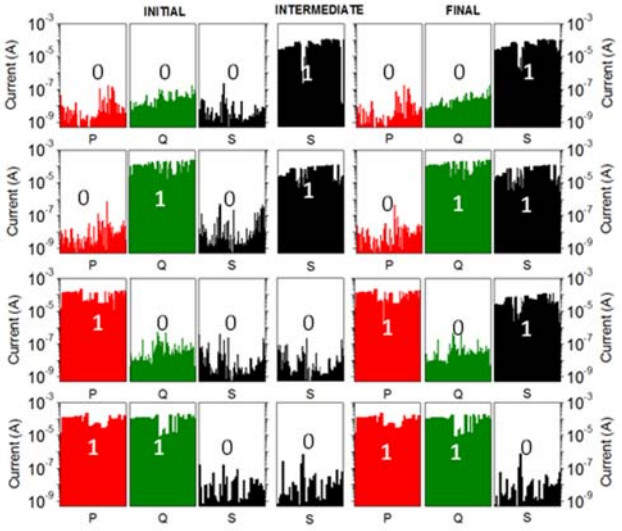


Fig. 7. NAND implementation, with continuous sequence of operation with two IMPLY operation steps. Intermediate state of memristor S is included showing that the first operation step was performed correctly.

state is included to corroborate that the first operation step occurs successfully. In this continuous logic evaluation experiment the effect of the cycle-to-cycle variability of the devices is observed, showing a stochastic fluctuation of the current, but keeping the validity of the logic operation in all the cases. Although in some cycles current at '0' and '1' states overpass the forbidden region (current values above and below 0.1μA and 10μA respectively), the successive performance (with a percentage of success of around 80%) of such a gate has been demonstrated.

So far, IMPLY and NAND logic gates have been experimentally demonstrated using High-k MIS structures as memristors, by using standard procedures [25]. In the next section, the NAND gate performance is improved, using only one operation step instead of two.

V. A NEW NAND OPERATION

This new NAND operation proposed a procedure with only one operation step where the three memristors (P, Q and S) are simultaneously biased. Unlike previous procedures, an additional voltage, V_{COND2}, has been applied.

A. Theoretical circuit analysis

First, a circuit analysis taking into account the three memristors has been done. Considering the memristors of the circuit shown in Fig. 3(b) behave as three resistances (R_P, R_Q, and R_S) and applying Kirchhoff's current law at V_G node, the voltage at node G is:

$$V_G = \frac{R_G R_Q R_S V_P + R_G R_P R_S V_Q + R_G R_P R_Q V_S}{R_P R_Q (R_S + R_G) + R_G R_S (R_Q + R_P)} \quad (1)$$

V_G takes different values depending on the particular NAND case, since initial memristor states differ from one case to another. Remember that when the initial state of the memristor is '0', the memristor resistance is high

(R_{OFF}). On the other hand, if the memristor state is '1', then the memristor resistance is low (R_{ON}). The value of R_G should be $R_{ON} < R_G < R_{OFF}$ with at least one order of magnitude difference between R_{ON} and R_G and between R_G and R_{OFF}. For each NAND case, we will evaluate the relation between V_P, V_Q and V_S that must be fulfilled to get the suitable V_G value that implements each NAND case in only one operation step.

In the case 1 of the NAND truth table (Fig. 3(d)), initial resistance value of memristors P, Q and S should be R_{OFF} ('0' logic state) and, at the end, S resistance should change to R_{ON}. Voltage drop in P, Q and S can be calculated as V_X-V_G (being V_X the voltage at the top electrode of each memristor). Then, if operational voltages applied to P and Q were V_{COND1} while for S was V_{IMPLY}, with $V_{IMPLY}>V_{COND1}$, (2) would be obtained (substituting these values in (1) and simplifying). Considering the resistance relation described in the last paragraph, V_G would be negligible.

$$V_G = \frac{R_G V_{IMPLY} + 2R_G V_{COND1}}{R_{off} + 3R_G} \approx 0 \quad (2)$$

Then, since $V_G \approx 0$, voltage drops across P and Q would be approximately V_{COND1}, and across S almost V_{IMPLY}. This would provoke the S resistance change from R_{OFF} ('0') to R_{ON} ('1'), while P and Q remain the same state ('0') with resistance R_{OFF}.

In case 2, resistances of memristors P, Q and S should be R_{OFF}, R_{ON} and R_{OFF} respectively and, as before, S resistance should change to R_{ON}. If P and Q were biased at V_{COND2} and S with V_{IMPLY}; V_G would be given by (3). Taking into account the memristor resistance values, V_G would be negligible again. The voltage drops through P, Q and S would be V_{COND2}, V_{COND2} and V_{IMPLY} respectively (with $V_{IMPLY} > V_{COND2}$) provoking the change of the S resistance from R_{OFF} to R_{ON} and modifying the stored logic state from '0' to '1'. As expected, P and Q would remain in the same initial state.

$$V_G = \frac{R_G R_{on} V_{IMPLY} + (R_G R_{on} + R_G R_{off}) V_{COND2}}{(R_{off} + 2R_G) R_{on} + R_G R_{off}} \approx 0 \quad (3)$$

Similarly occurs in case 3. Since P and Q are supposed to be interchangeable and initial states are $R_P=R_{ON}$, $R_Q=R_{OFF}$ and $R_S=R_{OFF}$, V_G follows the same equation, (3). Therefore, voltage drops across memristors, considering $V_P = V_Q = V_{COND2}$ and $V_S = V_{IMPLY}$, would be the same as in case 2 giving the correct final memristors states.

Finally, in case 4, initial states of memristors P, Q and S are equal to R_{ON}, R_{ON} and R_{OFF}, respectively and S resistance should not change. If voltages applied to P and Q were V_{COND1} and $V_S = V_{IMPLY}$, V_G would be given by the expression in (4).

$$V_G = \frac{R_G R_{on} V_{IMPLY} + 2R_G R_{off} V_{COND1}}{(R_{off} + R_G) R_{on} + 2R_G R_{off}} \approx V_{COND1} \quad (4)$$

In this case, voltage drops at the memristors differ from the rest of cases. In both P and Q the voltage drop would be zero, while for S the voltage drop would be V_{IMPLY}-$V_{COND1} < V_{IMPLY}$. Thus, all memristors would maintain its initial state value. Therefore, NAND truth table (Fig. 3(d)) implementation in a single step is theoretically demonstrated.

B. Experimental verification

As in section IV, the SPA has been used to apply the operation voltages and register the current through the memristors in order to initialize them and perform the operation step. After individually performing each case of NAND gate function under different applied voltages, finally, it has been found that the values that allow successful functionality of the NAND are againV_{COND1} = -2V, V_{COND2} = 0V and V_{IMPLY} = -4V. For the measurement of final states of memristor a voltage ramp up to -0.8V has been applied.

Fig. 8 graphically shows the proposed sequence to perform the NAND gate in only one operation step. Firstly, all memristors are initialized (initial states). Later, the unique operation step takes place applying the adequate voltages to P, Q and S memristor simultaneously according to the case. The voltage selection was controlled by programming the proper voltages to the terminals for each logic case. Finally, the memristors state is read to verify the correct gate behavior. The initialization and evaluation of memristors states is also done when the standard NAND procedure is used. However, the number of operation steps performed to provoke the NAND gate output is different: with the standard procedure two operation steps are required (first an IMPLY operation between P and S memristors and, secondly, another IMPLY operation between Q and S memristor). With this new NAND operation, only one operation step, where the three memristors are involved at the same time, is done, instead of the two operation steps of the standard procedure. Table I shows the combination of the operation voltages, which are applied simultaneously and verify the required relationships. This provokes an S-output that corresponds to the NAND truth table.

TABLE I
EXPERIMENTAL VOLTAGES APPLIED SIMULTANEOUSLY TO THE NAND CIRCUIT TO PROVOKE THE DIFFERENT CASES OF THE NAND OUTPUT IN ONLY ONE OPERATION STEP.

CASE	V_P (V)	V_Q (V)	V_S (V)
1	-2	-2	-4
2	0	0	-4
3	0	0	-4
4	-2	-2	-4

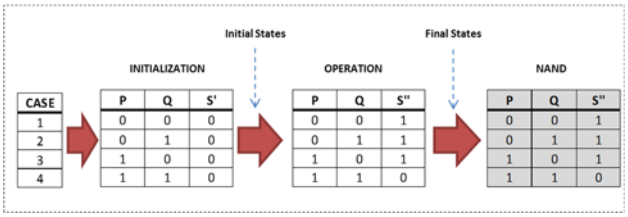


Fig. 8. Schematic flow sequence of one operation step procedure for NAND logic gate.

The experimental results obtained following previous procedure are presented in Fig. 9, where initial and final memristor states are depicted for all NAND cases. Intermediate states (shown when two sequential steps were required, Fig. 6) do not appear because in this case, only one operation step is needed. These results demonstrate that memristor-based NAND operation is possible using uniquely one step. Successive operations were also performed to obtain randomly, on the same gate, the different logic cases of the NAND gate, with only one operation step.

Fig. 10 shows initial and final memristors states for all NAND cases in a successive operation measurement. As in two-step NAND (Fig. 7) several '0' states are in the forbidden region (current reaching values of 1μA). However, since current values at '1' are mostly above 10μA, the successive performance of one-step NAND has been also performed. Also mention that only the successful cycles have been included being the success percentage around 80%. How to handle the memristor dispersion is one of the next tasks to be addressed in future works.

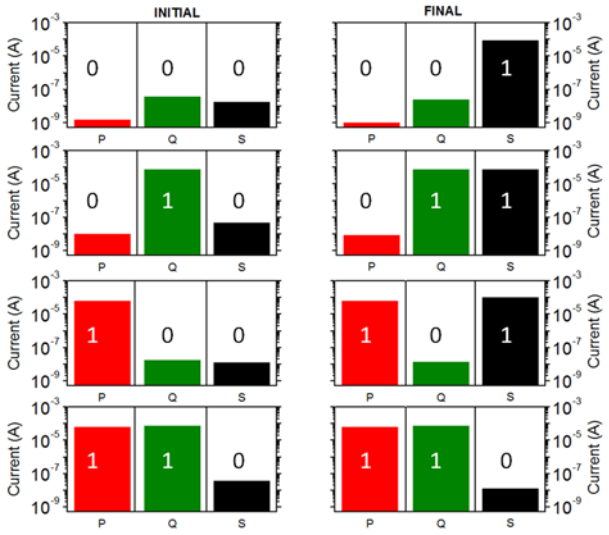


Fig. 9. NAND implementation with only one IMPLY operation step.

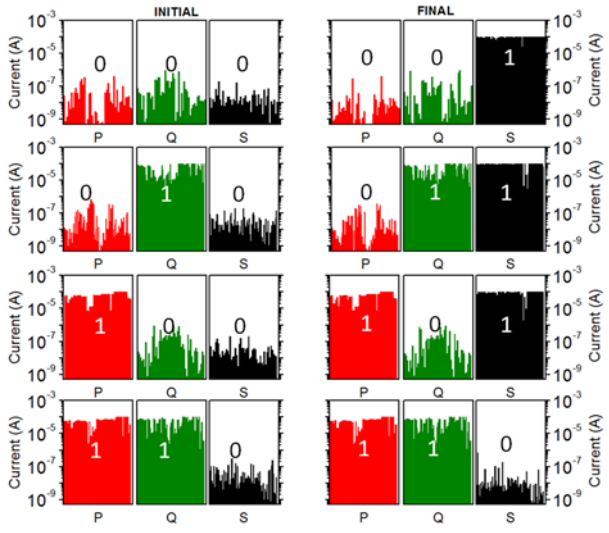


Fig. 10. Successive operations of the NAND gate with only one operation step. Cycle-to-cycle device variability is observed.

VI. Conclusions

In this paper, memristor-based IMPLY and NAND logic gates have been experimentally demonstrated using Ni/HfO_2/Si manufactured devices. Successive NAND operations (for all four input cases) have been also successfully performed, showing the operation correctness even in the presence of the inherent cycle-to-cycle device fluctuations. Additionally, a new procedure to operate the NAND gate has been proposed, which requires only one step, reducing the computing time when compared to previous IMPLY-based implementations (that requires two steps). This technique requires a third operational voltage for the NAND structure, though in the shown case this additional voltage is GND.

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