

A 90-GHz Asymmetrical Single-Pole Double-Throw Switch with >19.5 -dBm 1-dB Compression Point in Transmission Mode Using 55-nm Bulk CMOS Technology

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Abstract—The millimeter-wave (mm-wave) single-pole double-throw (SPDT) switch designed in bulk CMOS technology has limited power-handling capability in terms of 1-dB compression point (P1dB) inherently. This is mainly due to the low threshold voltage of the switching transistors used for shunt-connected configuration. To solve this issue, an innovative approach is presented in this work, which utilizes a unique passive ring structure. It allows a relatively strong RF signal passing through the TX branch, while the switching transistors are turned on. Thus, the fundamental limitation for P1dB due to reduced threshold voltage is overcome. To prove the presented approach is feasible in practice, a 90-GHz asymmetrical SPDT switch is designed in a standard 55-nm bulk CMOS technology. The design has achieved an insertion loss of 3.2 dB and 3.6 dB in TX and RX mode, respectively. Moreover, more than 20 dB isolation is obtained in both modes. Because of using the proposed passive ring structure, a remarkable P1dB is achieved. No gain compression is observed at all, while a 19.5 dBm input power is injected into the TX branch of the designed SPDT switch. The die area of this design is only 0.26 mm².

Index Terms—Bulk CMOS, millimeter-wave (mm-wave), RFIC, Silicon-Germanium (SiGe), switch.

I. INTRODUCTION

THE single-pole double-throw (SPDT) switch is perhaps the most indispensable building block in a time-division multiplexing (TDD) system, which enables sharing of a single antenna for both TX and RX [1]. The design of a high-performance SPDT switch is a complicated task, which involves several trade-offs among, insertion loss (IL), isolation (ISO), 1-dB compression point (P1dB) and cost. Traditionally, the SPDT switches are designed in III/V technologies, such as Gallium Arsenide (GaAs) [2]. However, the relatively high fabrication cost and limited integration capability are of concern. To solve these issues,

tremendous efforts have been made in the last couple of decades for silicon-based switches design, from sub-GHz all the way into sub-THz [3]-[20]. For a switch design operating below 60 GHz, SOI and bulk CMOS technologies are the most popular ones due to their relatively lower fabrication costs of mass production. Several novel design approaches have been presented in the literature [3]-[9], just to name a few. When the operating frequency is pushed to above 60 GHz, a few problems still remain for silicon-based SPDT switch design, especially bulk CMOS-based designs. One of the critical issues is the limited power-handling capability in terms of 1-dB compression point (P1dB).

As the state-of-the-art E- and W-band power amplifiers (PAs) designed in bulk CMOS technology can achieve more than 15-dBm saturation power with a simple 2-way differential power combining [21]-[22], the P1dB of a SPDT switch must be significantly higher than this value, which is currently not available. Most bulk CMOS-based SPDT switches operating in millimeter-wave (mm-wave) region have a P1dB around 13 dBm only [10], [12]-[15], [18]-[20], which is not sufficient to be used along with the above-mentioned PAs to form a highly integrated T/R module. Thus, it is obvious to ask if it is possible to design mm-wave SPDT switches with an enhanced P1dB in bulk CMOS technology. To address this issue, an innovative passive-inspired design approach will be presented in this work.

The rest of this paper is organized as follows. In Section II, the classical design techniques for P1dB enhancement are overviewed. In Section III, the concept of using the proposed approach for asymmetrical SPDT switch design is explored. The detailed device-level implementation is shown in Section IV. The measurement results are given in Section V and the conclusions are finally drawn in Section VI.

II. OVERVIEW OF DESIGN APPROACHES FOR ENHANCED POWER-HANDLING CAPABILITY

Regardless of the operation frequency of the SPDT switch, one of the limiting factors for achieving an enhanced P1dB is the reduced threshold voltage (V_{TH}) of MOSFETs, which has been very well documented in [3], [5], [6], [17]. This is particularly true for the designs that only utilize the

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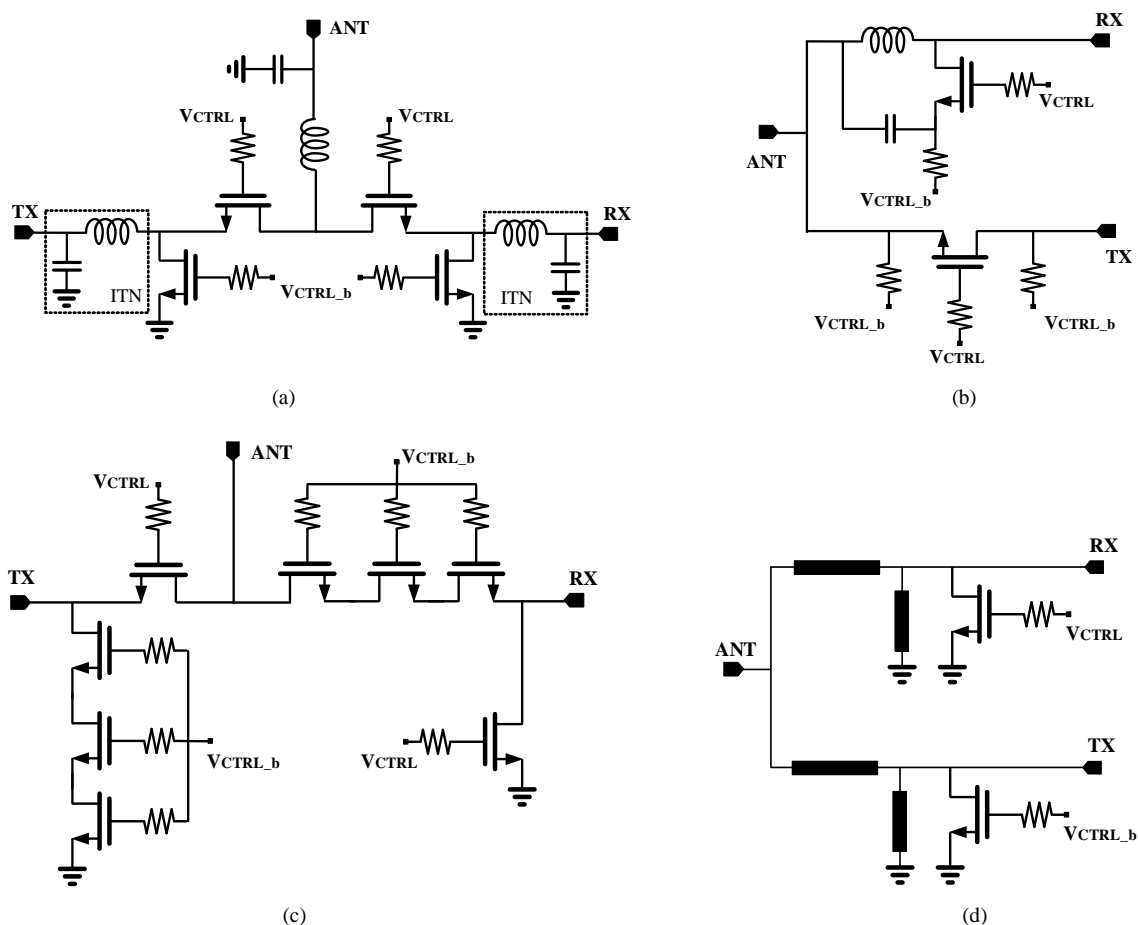


Fig. 1. Overview of the classical SPDT switch structures in the literature, (a) impedance transformation network, (b) asymmetrical structure, (c) asymmetrical structure with stacked transistors and (d) symmetrical structure with “shunt-connected” switching transistors only.

so-called shunt-connected transistors. As the active device is continuously scaled for mm-wave circuit design, the values of V_{TH} and breakdown voltage are getting lower and lower. As a result, the P1dB related issue becomes more and more severe. This is particularly true for the designs that are implemented in bulk CMOS technology. Thus, a simple but effective design approach must be proposed to improve the power-handling capability in a low-cost way.

As far as SPDT switch design is concerned, it could be categorized into two parts. One is an active-inspired design and another is a passive-inspired one. The former has been used as the driving force for several years. Many classical design techniques, such as negative control voltage and AC-floating bias [6], have been extensively used to improve the P1dB of the bulk CMOS-based design. However, both techniques require using of special physical treatments, such as Deep N-well (DNW) technology, which results in additional fabrication costs. Another classical design approach is to use a combination of the stacked transistor with negative bias voltage. Although this approach can be used in SOI CMOS-based designs, it cannot be simply transferred into bulk CMOS-based design due to the physical limitation of MOSFET. Additionally, the design of a negative control voltage generator is not straightforward and it might significantly increase die area overhead [23].

To further understand the principles of how to improve the power-handling capability for SPDT switch design, four classical design approaches are overviewed in Fig. 1. As can be seen in Fig. 1(a), the concept of using an impedance transformation network (ITN) for symmetrical SPDT switch design is presented [3]. However, this approach results in an inherent design trade-off between P1dB and ISO for a symmetrical SPDT switch. In order to obtain both high P1dB and ISO for a SPDT switch, an asymmetrical structure is used. A typical asymmetrical SPDT structure is given in Fig. 1(b) [6], [13]. Utilizing the design flexibility obtained from the asymmetrical structure, the performance of P1dB and ISO can be optimized separately. If a DNW or SOI technology is available, the P1dB could be even further enhanced by stacking of multiple transistors, as demonstrated in Fig. 1(c) [5]. It is noted that although using asymmetrical structures for SPDT switch design have successfully demonstrated a great performance improvement at 30 GHz and below, none of these techniques might be fully functional, if the operation frequency is further pushed into E- and W-band. This is mainly because all these classical approaches use series-connected transistors, which may severely affect the overall performance of a SPDT switch operating beyond 60 GHz. The series-connected transistors not only add loss to the ON-state of a switch, but

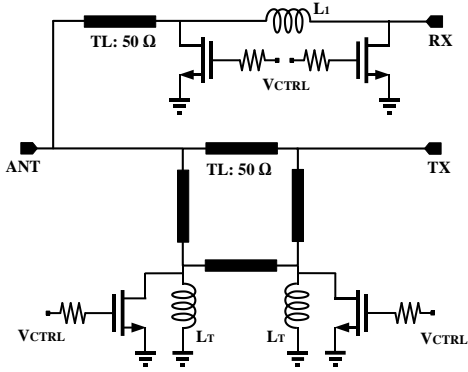


Fig. 2. The schematic of the designed asymmetrical SPDT switch. Note: All TLs are quarter-wavelength TLs.

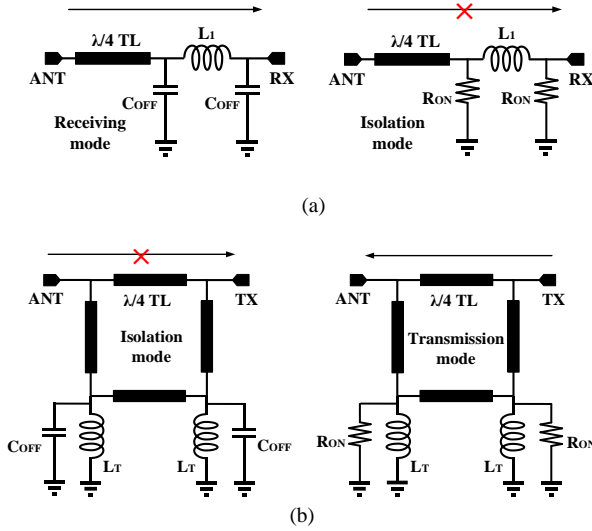


Fig. 3. Operation principles of the proposed asymmetrical SPDT switch, (a) RX branch, and (b) TX branch.

also cause capacitive feed through in the OFF-state of a switch [10], [12]. For this reason, most mm-wave switches use shunt-connected transistors only. A classical structure for symmetrical SPDT design operating beyond 60 GHz is given in Fig. 1(d) [8]. As illustrated, the shunt-connected transistors are used along with $\lambda/4$ -wavelength TLs to provide high-impedance nodes. However, the drawback of only using shunt-connected transistors for SPDT switch design has been very well documented in the literature [17], which is the significantly constrained P1dB. According to the calculated data presented in [17], a 3.6-dBm transmitted RF signal could potentially turn on the OFF-state switching transistors implemented in standard 65-nm CMOS technology, although the actual value of P1dB is typically several decibels higher than this value. Thus, an innovative design approach is required to further enhance P1dB of the switch.

Since the limited P1dB is mainly constrained by active devices, it is worthwhile to explore a possible solution based on a passive-inspired approach [24]-[27], which is the motivation behind this work. An advantage of the passive-inspired approach is that it might be directly transferred to designs implemented in either SiGe or SOI

CMOS technologies as well and also can be used in conjunction with other techniques, such as negative control voltage, if it is required. Finally, as the passive-inspired approach is based on passive structures, it can be “scaled” to different operation frequencies by changing the physical dimensions of the passive structures.

III. THE CONCEPT OF THE PROPOSED ASYMMETRICAL SPDT SWITCH USING PASSIVE RING STRUCTURE

As discussed earlier, there are inherent trade-offs between P1dB and ISO/IL for symmetrical SPDT switch design. To enhance the P1dB of a switch without significantly deteriorating other design specifications, an asymmetrical structure has been presented in [6], [13]. Thus, this work is also focused on asymmetrical SPDT switch design. However, the design of an asymmetrical SPDT switch usually requires the use of series-connected switching transistors. As mentioned in Section II, there are issues with them at a very high frequency, such as 90 GHz. Thus, it is difficult to directly transfer the presented approach in [6] to a mm-wave SPDT switch design. To enable an asymmetrical design without using any series-connected transistors, an innovative passive structure is presented in this work. The simplified schematic is given in Fig. 2.

As can be seen, a classical double-shunted structure is used along with a $\lambda/4$ -wavelength TL in RX branch [8], [18], [28]-[29]. In theory, as the SPDT switch works in RX mode, the impedance looking into the TX port should be relatively high, so that the received RF signal at ANT port will not flow into TX branch. However, the impedance could be significantly lowered in practice due to parasitics of switching transistors and the limited Q-factor of the $\lambda/4$ -wavelength TLs. Consequently, the IL of the SPDT in RX mode would be deteriorated. Moreover, in this design, as the targeted P1dB is relatively high, sufficient ISO is required to ensure that the transmitted RF signal has minimized influence on RX branch. To achieve this goal, the double-shunted transistors along with an inductor L_1 are used to form a C-L-C network [8], [18], [28]-[29]. As a result, the ISO can be greatly enhanced.

For the TX branch, it utilizes four $\lambda/4$ -wavelength TLs to form a “ring resonator”. Additionally, the tuning inductors L_T are used along with the switching transistors. The parasitic capacitance (known as C_{OFF}) of the transistors together with L_T form a shunt LC tank that provides the required high impedance nodes by looking into the ground. The size of switching transistors can be determined straightforward using the approaches presented in [3], [20]. Once the size is determined, the value of L_T can be optimized accordingly to achieve a relatively high impedance at the designed frequency. Furthermore, in contrast to all conventional designs that required switching transistors to be turned OFF in TX mode, in this design, the switching transistors are turned ON in TX mode. Consequently, the fundamental design issue related to power-handling capability in terms of P1dB due to the reduced V_{TH} is simply

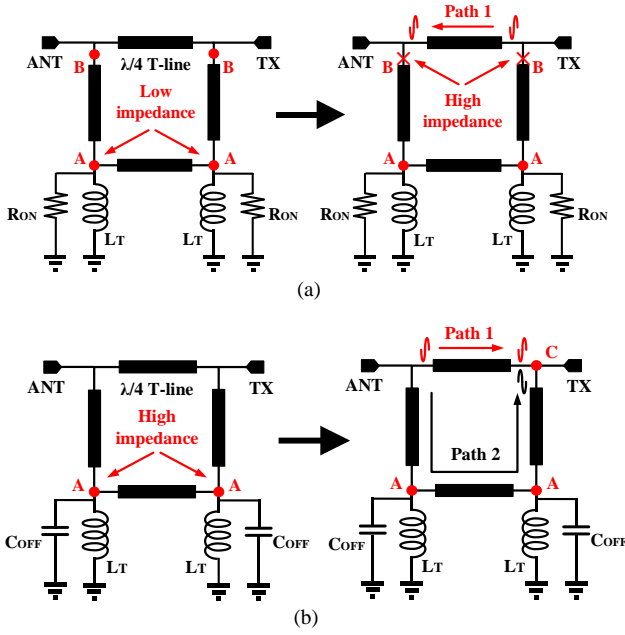


Fig. 4. Simplified models for the TX branch of the asymmetrical SPDT switch in different operation mode, (a) transmission, and (b) isolation.

overcome.

To further elaborate the presented approach for SPDT switch design, the simplified circuit models for the classical and the proposed approaches are compared in Fig. 3. As illustrated in Fig. 3(a), the circuit model for RX branch is given. In order to transmit a RF signal from ANT port to RX port, the shunt-connected transistors must be turned off to create a high-impedance path between RX port and ground. Moreover, to improve ISO between ANT and RX ports, the transistors have to be turned on to create a low-impedance path to the ground. The drawback of this approach has been explained earlier. As the expected RF signal that appeared at ANT port is not strong enough (around 0 dBm for most cases), the shunt-connected transistors should be able to handle it without any issue. However, the situation would be different in TX mode. To avoid the power-handling issue completely, an opposite mechanism is used for TX branch, which is given in Fig. 3(b). In TX mode, the shunt-connected transistors are tuned on; while in RX mode, they are turned off. As the transistors are turned on in TX mode, the power-handling capability of the switch could be significantly enhanced. On the other hand, the ISO between the ANT and TX ports of the presented design is realized by utilizing a signal canceling mechanism.

To further explore the insight of the presented concept, the simplified operating mechanisms of this design are given in Fig. 4. As shown in Fig. 4(a), the shunt transistors are turned on in TX mode. Thus, the impedance at the point A is relatively low and the impedance looking into point B is relatively high. As a result, the transmitted RF signal flows from TX port to ANT port through Path 1. On the other hand, as shown in Fig. 4(b), the isolation mode is realized, while the shunt transistors are turned off. In this case, the capacitor C_{OFF} along with the inductor L_T form an LC-network, which

presents a relatively high impedance at point A. As a result, two paths are created between the ANT and TX ports, namely Path 1 and Path 2. Their electrical lengths are $\lambda/4$ and $3\lambda/4$, respectively. As a rule of thumb, the RF signals traveling through these two paths will be having a 180° phase shift, while the signals are combined at point C, which results in a RF signal cancellation. This means that the RF signal cannot be traveled from the ANT to TX port. It thus indicates a good isolation. To prove the concept is sound in theory, a signal given in (1) is injected into the ANT port at isolation mode,

$$ANT_{SIG} = A \cos(\omega t + \theta_0) \quad (1)$$

where A , ω and θ_0 are the amplitude, angular frequency and phase of the injected signal, respectively. Then, the signal through the Path 1 and Path 2 can be expressed as,

$$ANT_{SIG_path1} = A_1 \cos(\omega t + \theta_0 - \frac{1}{4} \lambda \times \frac{2\pi}{\lambda}) \quad (2a)$$

$$ANT_{SIG_path2} = A_2 \cos(\omega t + \theta_0 - \frac{3}{4} \lambda \times \frac{2\pi}{\lambda}) \quad (2b)$$

By adding (2a) and (2b), the signal sensed at TX port is given in (3),

$$TX_{SIG} = (A_1 - A_2) \sin(\omega t + \theta_0) \quad (3)$$

As can be seen from (3), if the magnitude of the signals that pass through two paths are exactly the same, they will be completely canceled with each other. Consequently, there will be no signal leak through to the TX port. However, the parasitic effects due to the switching transistors and tuning inductance L_T will induce some additional phase shift, which deteriorates the ISO of the switch. So, the signal from the Path 2 can be rewritten as,

$$ANT_{SIG_path2} = A_2 \cos\left(\omega t + \theta_0 - \frac{3}{4} \lambda \times \frac{2\pi}{\lambda} - \theta_{LC}\right) \quad (4)$$

where the θ_{LC} is the phase delay due to the resulting parasitic LC tank. Substituting (4) into (3), the signal seen at TX port can be rearranged as,

$$TX'_{SIG} = A_1 \sin(\omega t + \theta_0) - A_2 \sin(\omega t + \theta_0 - \theta_{LC}) \quad (5)$$

The magnitude of TX'_{SIG} can be written as,

$$Mag = \sqrt{1 + (1 - \alpha)^2 - 2(1 - \alpha) \cos \theta_{LC}} \quad (6)$$

where $\alpha = (A_1 - A_2)/A_1$. After normalizing (6) with (2a), the normalized magnitude of TX'_{SIG} can be calculated and the results are plotted in Fig. 5. As mentioned, the magnitude of TX'_{SIG} represents isolation capability of the designed switch. As indicated in Fig. 5, the value of “Mag” of the designed switch is limited by two factors, α and θ_{LC} . The variable α indicates different insertion losses through the two different paths and the variable θ_{LC} represents additional phase induced by the LC tank. By carefully selecting the values of transistor and L_T , an optimized ISO can be achieved.

It is noted that an approach presented in [30] also uses the concept of ring resonator for SPDT switch design, which is

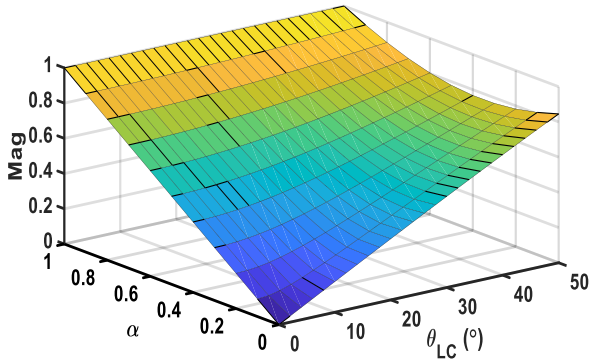


Fig. 5. Simulated adverse impact on ISO of the designed SPDT switch due to magnitude and phase errors through two paths.

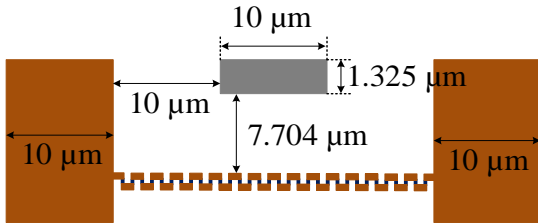


Fig. 6. Cross-section view of the implemented TL with physical dimensions. Note: The insertion loss in electromagnetic (EM) simulation is approximately 0.5 dB at 90 GHz for a $\lambda/4$ -TL.

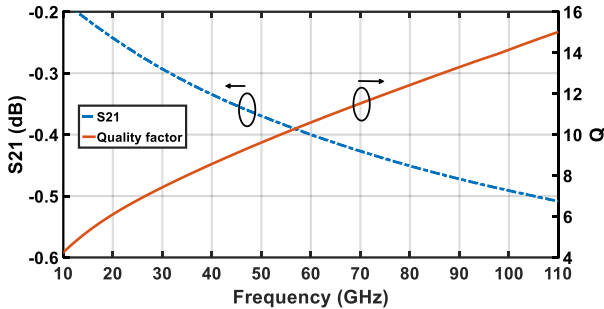
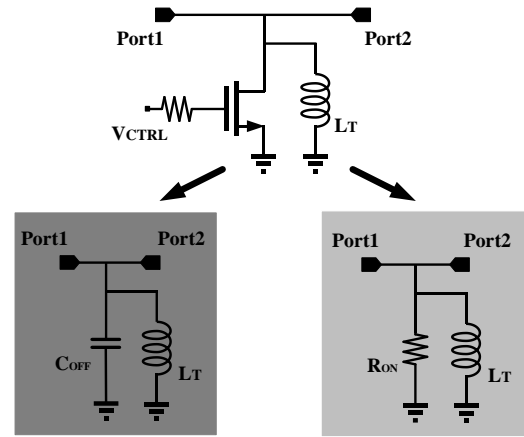
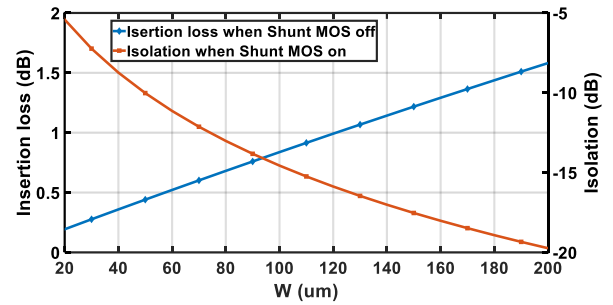


Fig. 7. EM simulated S21 and Q-factor of the designed TL.

implemented using discrete components and operates at a relatively low frequency. However, the principle behind that design is quite different from the one presented here. The ring resonator used in this work will improve not only P1dB but also isolation. In contrast, the one presented in [30] does not have such an improvement. Additionally, the design presented in [30] utilizes multiple ring resonators that could have a severe impact on insertion loss, if it is implemented on the lossy silicon substrate. Finally, it is also worthwhile to mention again that the ring-resonator-based structure is necessary for this design. Although using two $\lambda/4$ -TLs (instead of using four $\lambda/4$ -TLs to build the ring resonator) could also improve P1dB of a switch, it has limited isolation capability due to the signal-canceling mechanism. Based on our simulation, the obtained ISO is only around 10 dB across the interested frequency band.



(a)



(b)

Fig. 8. Evaluation of the impedance variations of the LC tank using a 2-port network, (a) test bench, and (b) simulation results with different switching transistor widths.

IV. DESIGN AND IMPLEMENTATION OF THE PRESENTED ASYMMETRICAL SPDT SWITCH

To verify the proposed passive-inspired concept for SPDT design is feasible in practice, a standard 55-nm bulk CMOS technology is selected in this work. This technology provides not only high-performance nMOSFET with f_t of 200 GHz, but also 8 metal layers with aluminum as the top thick-metal layer. As shown in Figs. 3 and 4, TLs are extensively used for the design. The cross-section view of the TL used in this design is given in Fig. 6. As can be seen, metal walls are constructed by stacking all metal layers and used for all TLs to avoid any unnecessary coupling. The TL is constructed using the topmost metal layer, which has a thickness of 1.325 μm , while the ground plane is implemented using a combination of M2 and M3, and M1 is reserved for DC only. The width of the signal path and the gap are both 10 μm for the 50- Ω TL. In addition, the height of the silicon substrate is 737 μm . The relative dielectric constant of SiO₂ is 4.1. Furthermore, the EM simulated insertion loss and Q-factor of the designed $\lambda/4$ -TL are shown in Fig. 7.

As mentioned in the last section, the tuning inductor L_T and C_{OFF} form an LC tank, which plays a critical role in TX branch design. Therefore, the size of the switching transistor needs to be carefully co-designed with the value of L_T . A simple 2-port network is used to evaluate the characteristics

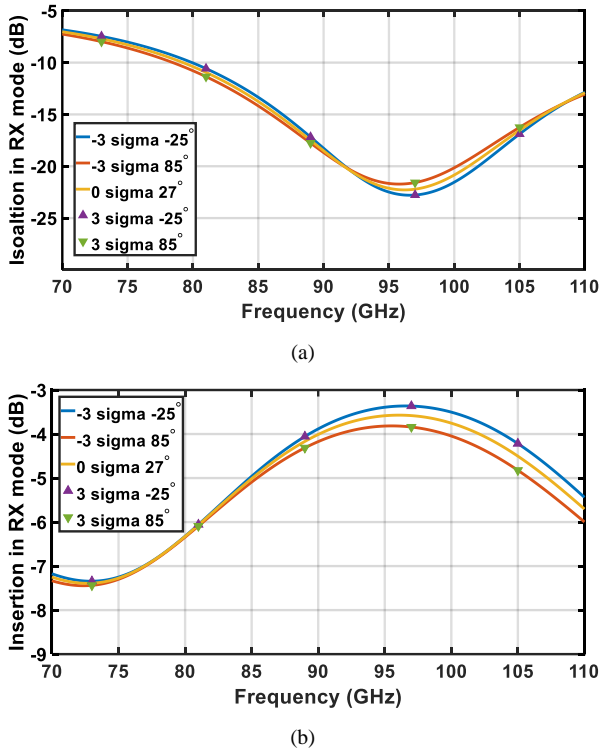


Fig. 9. Simulated frequency responses in of the asymmetrical SPDT switch in RX mode, (a) ISO, and (b) IL.

of the LC tank. The schematic is given in Fig. 8(a). The simulated results as a function of the width of the switching transistor are plotted in Fig. 8(b). Two design specifications, namely IL and ISO, are considered as benchmarks for performance evaluation here. It is noted that the presented IL and ISO here are mainly used to reflect the variations of the LC tank impedance, which are different from the IL and ISO used for a switch. In order to simplify the design procedure, an ideal lumped inductor with a Q-factor of 10 is used for the tuning inductor at the beginning of the design. Utilizing the simulation tools, the ISO (when switching transistor is on) and IL (when switching transistor is off) of the LC tank can be directly calculated and the value of the tuning inductor can be determined. Based on the obtained simulation results, a good trade-off between IL and ISO is achieved, while the width of the switching transistor is kept to be 100 μm (20 fingers are used). Furthermore, the value of L_T is selected to be 90 pH. It is implemented using a straight metal line. The inductor L_T along with the switching MOSFET forms a MOS-inductor LC tank. Based on the EM simulation, it provides 230 Ω and 12 Ω when nMOSFETs switch off and switch on, respectively. For RX branch design, the same sizes are used for the double-shunted transistors. The value of L_1 is determined to be 120 pH and it is implemented using a folded metal line.

On the other hand, there is a design trade-off between switching speed and IL as discussed in [17]. In this design, it should be noted that the switching transistors are turned on in TX mode, thus the insertion loss is insensitive to the gate resistance. The selection of the gate resistance value is

mainly considered for switching time and IL of RX branch. A 10-k Ω resistor gives an optimized solution in this design.

Finally, to further demonstrate the presented ring structure is useful for switch design in practice, the impact on frequency responses due to process and temperature variations are taken into consideration, including ± 3 Sigma for process variations with a temperature varied from -25°C to 85°C . The simulated results are given in Figs. 9. As can be seen, there is only marginal performance variation observed, which shows good reliability of the proposed design approach. It is noted that the simulations are only conducted in RX mode because the performance of the designed SPDT switch in this mode is reflected by the presented ring structure used at TX branch.

V. MEASUREMENT RESULTS AND DISCUSSIONS

To evaluate the performance of the presented asymmetrical SPDT switch, a prototype is fabricated. The die microphotograph is shown in Fig. 10. Excluding the testing pads, the die size is only $0.26 \times 0.98 \text{ mm}^2$. The measurement was conducted using on-wafer G-S-G probing up to 110 GHz by means of a vector network analyzer N5290A from Keysight™ and 100- μm pitch (GSG) Infinity Probes with 1-mm connectors from FormFactor™, Inc. The on-wafer calibration was made by using a conventional short-load-open-thru (SLOT) to move the reference plane from the connectors of the equipment to the tips of the RF probes. For comparison purposes, both the EM simulated and measured S-parameters are given.

Since the designed SPDT switch is asymmetrical, two different prototypes are fabricated in which RX and TX ports are terminated with a 50- Ω load, respectively. As a result, the performance can be evaluated using the standard test bench that is used for symmetrical SPDT switch characterization. To turn the switch into a TX mode, the TX branch needs to allow a RF signal to be delivered from TX port to ANT port. Meanwhile, the RX branch needs to provide an isolation between ANT port and RX port. To do so, the control voltage $V_{\text{CTRL}} = 0$ is applied. The frequency responses of the switch working in TX mode are shown in Fig. 11. As can be seen, at 90 GHz, the IL and ISO of this design are 3.2 dB and 28 dB, respectively. Both the input and output impedance matching are better than 10 dB.

To evaluate the performance of the switch in RX mode, the control voltage $V_{\text{CTRL}} = 1.2 \text{ V}$ is applied. In such a way, the TX branch provides isolation between ANT port and TX port. Meanwhile, the RX branch allows RF signal to pass through from ANT port to RX port. The measured frequency responses are given in Fig. 12. As illustrated, the IL and ISO are 3.6 dB and 20 dB at 90 GHz, respectively. Both the input and output matching are better than 15 dB. It is noted that there is a frequency shift between the measured and simulated results. This shift is likely to be caused by the fact that the values of the parasitic capacitance of nMOSFETs and L_T are under-estimated in EM simulation.

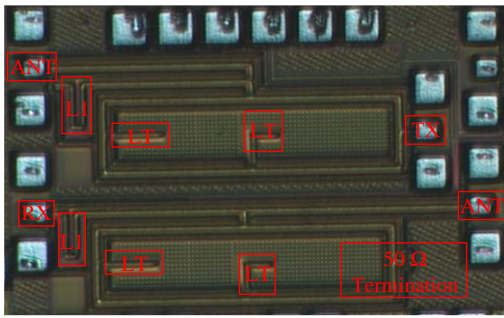
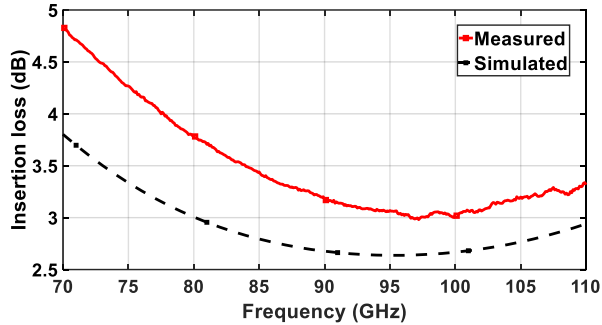
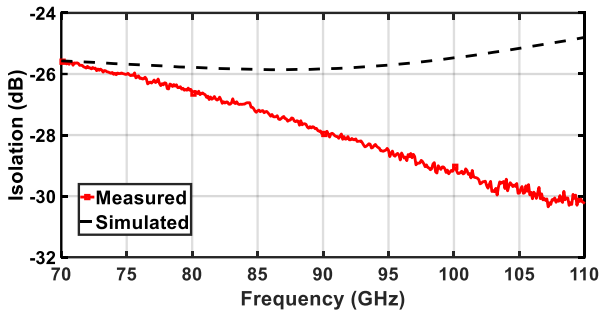


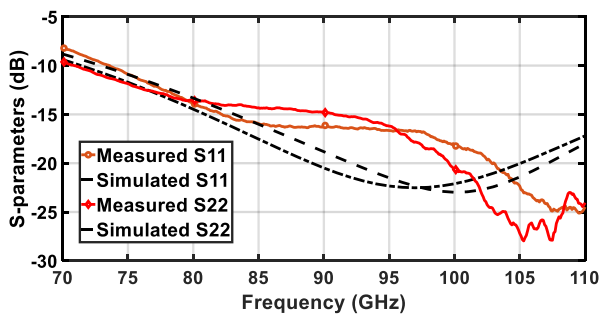
Fig. 10. Die microphotograph of the designed SPDT switch.



(a)



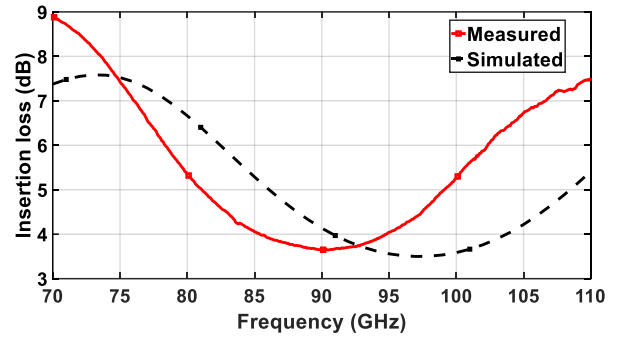
(b)



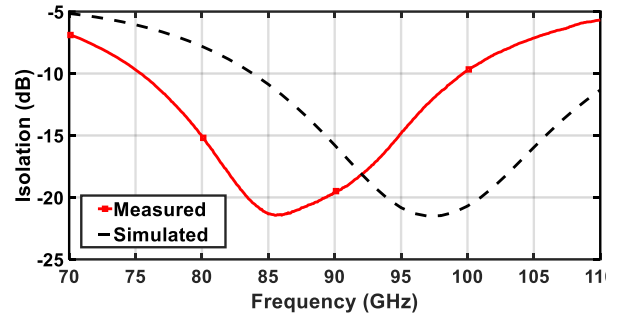
(c)

Fig. 11. Measured frequency responses of the designed SPDT switch in TX mode, (a) IL, (b) ISO and (c) input and output impedance matching. Note: IL is measured between TX and ANT ports, ISO is measured between RX and ANT ports only.

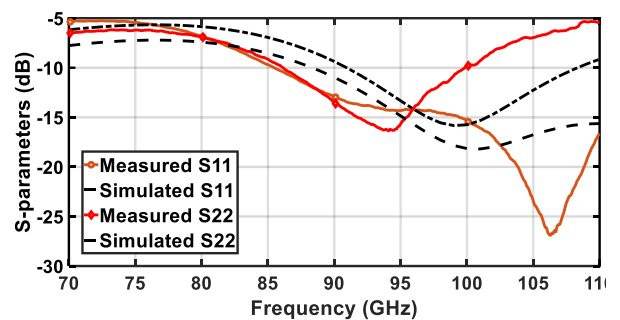
Due to the equipment limitation, the P1dB can only be evaluated at 87 GHz. Initial power measurements were made using the setup shown in Fig. 13. As can be seen, at the input side of the test bench, a signal generator E8257D from Keysight™ is used to generate a low-frequency signal, which is then fed into a frequency extension module



(a)



(b)



(c)

Fig. 12. Measured frequency responses of the designed asymmetrical SPDT switch in RX mode, (a) IL, (b) ISO and (c) input and output impedance matching. Note: IL is measured between RX and ANT ports, ISO is measured between TX and ANT ports only.

WR12SGX from Virginia Diode (VDI™). The WR12SGX is an E-band source module that could provide up to 16 dBm output power at 87 GHz. The signal source is then connected to a 0-30 dB adjustable attenuator along with a 78-87 GHz PA module. Both the attenuator and PA modules are from SAGE™. The PA module features a saturated output power of 25 dBm at 87 GHz. In order to monitor the input power level injected into the designed SPDT switches, a coupler with 30 dB coupling coefficient is used along with a U8489A power sensor from Keysight™. At the output side of the test bench, a 10-dB fixed attenuator is used along with the PM5B power meter from VDI™. Both the input and output power levels were calibrated to the probe tips. The measured P1dB and the IL as a function of input power for this design are given in Fig. 14. As can be seen, the measured power-handling capability is truly remarkable, no obvious

TABLE I
PERFORMANCE SUMMARY OF THE DESIGNED SPDT SWITCHES WITH THE OTHER STATE-OF-THE-ART DESIGNS

REF.	f_c (GHz)	Insertion loss (dB)	Isolation (dB)	P1dB (dBm)	Power consumption (mW)	Area (mm ²)	Tech. (nm)	Circuit structure
[9]	DC-43	3	50	19.6	0.0	0.0058	45 SOI	RF signal cancellation
[12]	DC-60	2.5	23	7	0.0	0.04	45 SOI	Series-shunt-connected FETs
[8]	50-70	1.5	25	13.5	0.0	0.28	90 CMOS	$\lambda/4$ -TL with shunt-connected FETs
[13]	50-67	1.9	20	10	0.0	0.6	90 CMOS	$\lambda/4$ -TL with shunt-connected FETs
[15]	58-85	1.8	22	10	0.0	0.015	65 CMOS	Transformer with shunt-connected FETs
[20]	50-94	3.3	27	15	0.0	0.24	90 CMOS	Travelling wave with shunt-connected FETs
[28]	60-110	3-4	25	10.5	0.0	0.3	90 CMOS	$\lambda/4$ -TL with shunt-connected FETs
[17]	73-110	1.1	22	17	5.9	0.213	90 SiGe	$\lambda/4$ -TL with shunt-connected FETs
[29]	75-110	4.5	48	11	0.0	0.33	90 CMOS	Leakage cancelation
[2]	77-120	1.8	20	19	0.0	0.75	50 GaAs HEMT	$\lambda/4$ -TL with shunt-connected FETs
[16]	77-110	1.4	19.3	19	8	0.14	90 SiGe	$\lambda/4$ -TL with shunt-connected FETs
[31]	92-98	2	20	n/a	4.8	n/a	130 InP HBT	$\lambda/4$ -TL with shunt-connected FETs
[32]	94-110	4.2	25	n/a	0.0	n/a	65 CMOS	$\lambda/4$ -TL with shunt-connected FETs
[19]	130-180	3.3	23.7	11.5*	0.0	0.0035	65 CMOS	Artificial resonator with shunt-connected FETs
[18]	140-220	3	20	8	0.0	0.29	45 SOI	$\lambda/4$ -TL with shunt-connected FETs
THIS WORK	85-95	3.2 (TX) 3.6 (RX)	>25 (TX) >20 (RX)	>19.5[^] (TX)	0.0	0.26	55 CMOS	Ring resonator with shunt-connected FETs

Note: * simulation results only, ^ due to the output power limitation of the PA module.

gain compression is observed, when a 19.5 dBm input power is injected into the TX port of the switch.

The performance summary of the presented asymmetrical SPDT switch is given in Table I and also compared with the other state-of-the-art designs. By observing the summarized data from different designs, some interesting results can be found. Firstly, as shown in the table, for the bulk CMOS switches operating beyond 90 GHz, it seems to have an IL around 3.5 dB, while the SiGe switches offer very competitive overall performance at W-band, especially IL, even comparing with the designs using more advanced III/V technologies, such as the ones presented in [2]. The downsides of SiGe-based solutions are the relatively high power consumption comparing with their counterparts in CMOS technology, which may be critical to enable them for power-constrained consumer electronics.

Secondly, the obtained P1dB of the different mm-wave CMOS-based designs seem to be quite similar regardless of operating frequency. As shown in [15] and [19], both designs are implementation in 65-nm CMOS technology. Although the operating frequency is different, the P1dB for both designs are limited to be approximately 10 dBm, which indicates that the limiting factor for P1dB is not the operation frequency. One of the possible ways to improve P1dB is to select a technology node with a relatively higher threshold

voltage. As demonstrated in [8], the P1dB may be improved by approximately 3 dB. However, other mm-wave circuits, such as amplifiers, have to be implemented using reduced threshold voltage for an improved performance. Thus, there is a fundamental contradictive choice to be made for mm-wave RF front-end design. As shown in [12], [18], the P1dB of a SPDT switch implemented in 45-nm SOI CMOS is further reduced to approx. 8 dBm. As can be seen from Table I, using the presented approach, the power-handling capability in terms of P1dB can be improved to a remarkable level, more than 20 dBm. To the best of our knowledge, this is the only silicon-based mm-wave SPDT switch, including those in SiGe and SOI technologies, that achieves a P1dB of more than 20 dBm without using any special physical treatment, such as high- V_{TH} devices and negative bias voltages, which usually either increase fabrication cost or design complexity.

Last but not least, as the presented design approach is purely based on a passive-inspired concept, it also offers other advantages. The idea presented in this work can be effectively used along with high- V_{TH} devices and negative bias voltage to eventually enable Watt-level silicon-based switch at mm-wave region. In addition, as TLs are used for the implementation of ring resonator to improve ISO of the

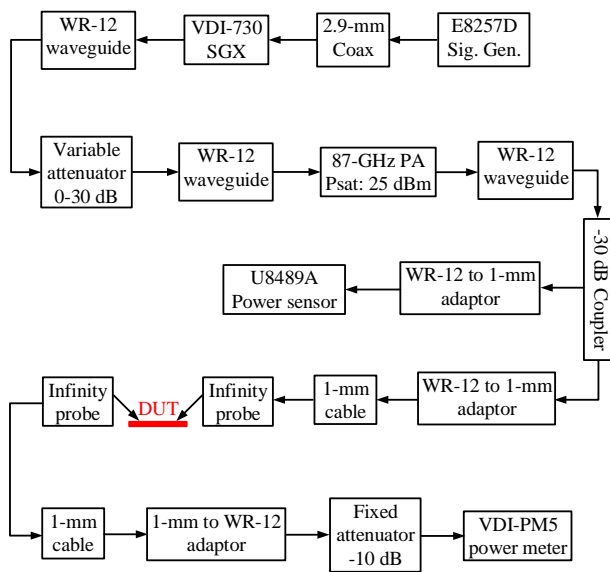


Fig. 13. The test bench used for P1dB measurements.

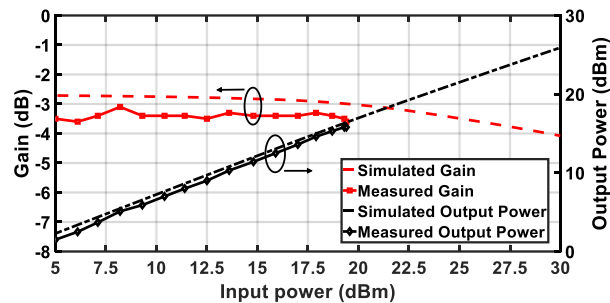


Fig. 14. The measured P1dB of the designed switch.

designed switch, the presented idea can also be used for different operation frequencies, as long as the implemented TLs have reasonable physical dimensions for on-chip implementation and the insertion losses are relatively low.

VI. CONCLUSIONS

A novel approach for mm-wave SPDT switch design with enhanced power-handling capability, especially P1dB, has been presented in this work. The presented approach is based on asymmetrical architecture. A passive ring structure is used to enable the use of ON-state switching transistors at TX mode, which results in a significantly enhanced P1dB. To prove the feasibility of using this approach for SPDT switch design, a prototype is implemented and fabricated in a standard 55-nm bulk CMOS technology. According to the measured results, the presented design can effectively enhance P1dB without compromising other performance. Therefore, it can be firmly concluded that the presented novel concept is effective for switch designs using shunt-connected transistors and breaks the fundamental limitation on P1dB of silicon-based SPDT switch due to active device scaling.

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