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Power-Synchronization Control for Ultra-Weak AC Networks: Comprehensive Stability and Dynamic Performance Assessment

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ABSTRACT Power-synchronization control (PSC) is a promising control strategy to improve the stability and performance of voltage-source converters (VSCs) in ultra-weak AC grids. However, evaluation of PSC to date has investigated performance only at single controller operating points, rather than holistically varying multiple controller gains. This paper develops a new methodology, based on small-signal eigenvalue analysis, to comprehensively analyze PSC-VSC stability. The maximum active power transfer of PSC is established across a broad range of controller tunings and the two-way and three-way couplings between the power-synchronization control, AC voltage control and high-pass current filter gains are quantified. A new stable tuning region is introduced, which represents the controller parameter space for stable operation. It is shown that PSC can achieve rated power transfer into an AC grid (short circuit ratio(SCR)=1) at multiple controller operating points, but dynamic performance varies significantly within this region. The robustness of this operating region to SCR changes is also investigated. The stability boundary and dynamic performance are validated using control hardware-in-the-loop experiments with a real-time digital simulator. Practical recommendations arising from this work are a set of controller gains that provide stability and good dynamic performance at high power transfer for ultra-weak grid-connected VSCs employing PSC.

INDEX TERMS Power-synchronization control, VSC, weak grids, small signal analysis.

I. INTRODUCTION

Renewable energy generation and energy storage are being integrated into power systems at an accelerating rate worldwide [1]. The preferred choice to interface these installations to an AC grid is the voltage-source converter (VSC) due to their good control performance and improved performance in weak AC grids [2], [3]. A weak grid is defined as a system with a short circuit ratio (SCR), $2 < SCR < 3$ [4]. Systems with $SCR < 2$ can therefore be referred to as ultra-weak (equivalent to the 'very low SCR' definition in [4]). These grid conditions present stability challenges for all VSCs and so continue to be studied in depth (e.g., in [6]–[21]). Vector current control (VCC) is the established standard for control of VSCs in strong grids due to the decoupled active and reactive power control and inherent current limiting capability. However, standard VCC becomes increasingly susceptible to low-frequency resonances and instability as the grid becomes weaker [4]–[6]. Enhancements of standard VCC and completely novel control structures have both been proposed to address instability in weak AC grids, but to date all proposed VSC control strategies remain vulnerable to some instabilities in ultra-weak grids. A dominant aspect contributing to instability is the controller synchronization method. For standard VCC, the converter-controller system is synchronized to the grid via the phase-locked loop (PLL), whose effect on stability is highlighted in e.g., [8]–[13]. The effect of some other aspects of the controller structure on stability in weak grid-connected VSCs was explored in [14]–[16], [19]. However, in these literature, a single controller gain has been investigated for its effect on system stability. There is limited investigation of the coupled effects of multiple controller parameters interacting at different tuning values. It is usually assumed that the

different time scales of control loops in a cascaded controller allow the effects of each loop to be considered separately [13]. However, the legitimacy of this assumption is not commonly tested by varying multiple control parameters simultaneously.

When considering the PLL as the chief cause of instability, improvements and modifications to standard vector current control have been proposed. For example, an artificial bus adds virtual impedance to the PLL in [12], [17], while the approach in [10] and [14] is to re-tune the PLL. Re-tuning approaches always result in a slower PLL, which produces a slower controller response and poor dynamic performance [8], [12], [18]. Other control strategies attempt to remove the PLL completely. A frequency synchronization control (FSC) method removes the PLL and appears to show improved stability in weak AC grids, but there is no inherent current-limiting capability [22]. A noteworthy control strategy proposed to eradicate the issue of PLL dynamics in weak AC grid-connected VSCs is power-synchronization control (PSC). PSC does not use a PLL to synchronize the controller to the grid but rather imitates the inherent synchronization of synchronous machines [6], [7]. Proponents of PSC claim that the maximum active power transfer in weak AC grids can be much higher than with standard VSC and the system damping is improved with this approach [23]. Case studies employing back-to-back VSCs between two weak AC grids and for the connection of wind farms to a weak grid using PSC have also shown good stability performance at high active power transfer and adequate fault-ride-through behavior [24], [25]. Transient performance was explored further in [26] to demonstrate that PSC can resynchronize with the grid within approximately one period of oscillation after a fault. Recently, a feedforward enhancement of PSC has also been proposed to address the poor performance of PSC in strong AC grids [27]. However, a full assessment of the effect of controller tuning variations on the steady-state and dynamic performance of PSC in weak AC grids has not yet been completed in the literature. In [28], a robust tuning method for the active power loop was proposed for a simplified model of PSC but the AC voltage control and high-pass filter tunings are neglected. Similarly, although [23] and [29] have examined the effect of the power synchronization and AC voltage control bandwidths on system damping pole and placement respectively, neither study examined the detailed interactions of these controller parameters nor used wide enough ranges of tunings to explore the full parameter space. It was also assumed that the precise grid conditions were known and constant. In all of these works, only a single controller tuning was used to assess stability, with this tuning determined by a trial and error process [7] or using a simplified model to analytically tune just one control loop [28]. In summary, it is clear from the above discussion that the research gap in the literature is (a) assessing the performance (including dynamic behavior) of PSC at a wide-range of controller tunings, and (b) evaluating the coupling between all PSC control parameters and the implications of these interactions for maximum power transfer, dynamic performance and system robustness.

In this paper, a new stability analysis approach is presented to determine the achievable active power limits of PSC as a function of two control parameters simultaneously. Small signal models are created at all distinct controller operating points using initial conditions tuned from a time-domain simulation. All control parameters which ensure stable operation are found to construct a stable tuning region for PSC for ultra-weak AC grids. This approach is also used to assess the robustness of PSC-based VSC and the implications for tuning in variable grids. Dynamic performance at tunings within the stable region is assessed to construct a secondary stability region of points where stability is maintained, and transient performance requirements are also met. The location of the boundary of the stable operating region and the dynamic performance are validated using control hardware-in-the-loop (CHiL) experiments with a real-time digital simulator (RTDS). This paper therefore makes the following contributions: 1) The bi-directional active power limits of a PSC-VSC in an ultra-weak AC grid (SCR = 1) are established across a wide range of controller parameters and bandwidths, 2) The impact of individual PSC controller gains on overall stability is quantified, 3) The two-way and three-way coupling between the active power control, AC voltage control and high-pass current filter are evaluated, and 4) all controller operating points of the PSC which maintain converter-controller stability and meet specific transient performance requirements at a given active power demand are quantified and validated using CHiL experiments. The approach detailed in this paper can be applied to any grid-connected PSC system to provide a description of the stable controller operating space, achievable power transfer limits and the controller dynamic performance, without the need for computationally-expensive time-domain simulations. This work therefore provides a fast, generalizable approach for analyzing PSC-controlled VSC systems under any operating parameters.

II. STUDY SYSTEM

Fig. 1 shows the topology of the grid-connected VSC system to be evaluated. The grid voltage is U_g, the voltage at the point of common coupling (PCC) is U_f and the converter voltage is U_c. R_n and L_n are the resistance and inductance of the AC grid and the VSC is connected via an RL filter with resistance R_c and inductance L_c. The AC grid is ultra-weak, with SCR = 1, and the full grid parameters are given in the Appendix. The power-synchronization control structure is also shown in Fig. 1. The power synchronization loop (PSL) acts on the active power error to produce a reference phase which is used to convert voltages and currents to the *dq*-frame. An AC voltage loop (AVL) with integral control is embedded to determine the *d*-axis converter voltage reference and a high-pass current filter (HPF) is employed to damp low-order harmonic resonances, which arise due to the very high reactance of the weak AC grid and decrease in frequency as the grid SCR decreases [5], [30]. The PCC voltage and converter current are low-pass

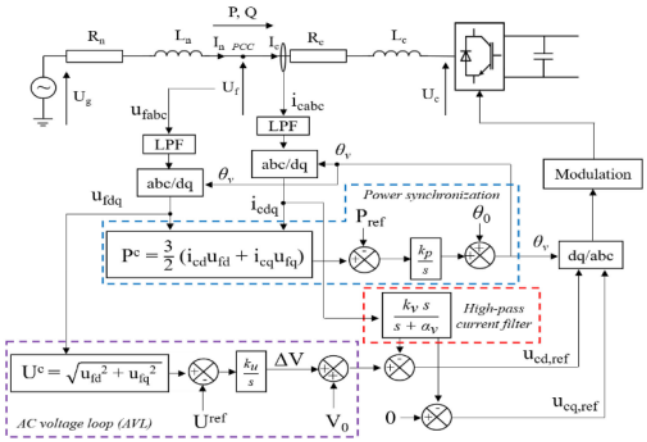

FIGURE 1. Grid-connected VSC test system with power-synchronization control.

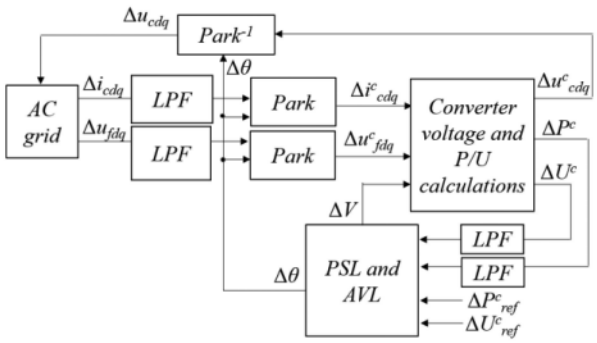

FIGURE 2. Connected small-signal model of AC grid system and PSC controller.

filtered before being transformed to the *dq*-frame. In fault conditions, a back-up PLL and current controller are employed to limit the converter current. Fault conditions are outside the scope of this paper and so, for clarity, these elements are not shown.

III. SMALL SIGNAL MODELLING AND VALIDATION

The system in Fig 1 has nonlinearities and so the governing equations are linearized in this section to produce a small signal stability model. Variables in the converter frame are denoted by the superscript '^{c}' and variables that have been low-pass filtered are marked with the superscript '^{f}'. The subscript '$_0$' is used to describe a steady-state linearization point.

A. SMALL-SIGNAL MODELLING

State-space models of the LCL-AC grid system and the PSC controller elements are constructed from the linearized system equations and connected as shown in Fig. 2. The linearized equations of the AC grid and RL filter are:

$$sL_c\Delta i_{cd} = \Delta u_{fd} - R_c\Delta i_{cd} - \Delta u_{cd} + \omega_g L_c\Delta i_{cq} \quad (1)$$

$$sL_c\Delta i_{cq} = \Delta u_{fq} - R_c\Delta i_{cq} - \Delta u_{cq} - \omega_g L_c\Delta i_{cd} \quad (2)$$

$$sL_n\Delta i_{nd} = -\Delta u_{fd} - R_n\Delta i_{nd} + \Delta u_{gd} + \omega_g L_n\Delta i_{nq} \quad (3)$$

$$sL_n\Delta i_{nq} = -\Delta u_{fq} - R_n\Delta i_{nq} + \Delta u_{gq} - \omega_g L_n\Delta i_{nd} \quad (4)$$

where, u_f is the PCC voltage, u_c is the converter voltage, u_g is the grid voltage, i_c is the converter current and i_n is the grid current. The corresponding state-space matrices and linearized Park and inverse Park transformations are described fully in [7].

The PSC control strategy, as described in detail in [6], [7], is shown in Fig. 1. Active power control and synchronization with the grid are provided by the power synchronization loop (PSL). The PSL acts on the power error to produce a reference angle, which is used as an input to the Park and inverse Park frame transformations. The linearized PSL control law is given in (5).

$$\Delta\theta_v = \frac{k_p}{s}\left(\Delta P^{cf} - \Delta P^{c}_{ref}\right) \quad (5)$$

where ΔP^{cf} is the active power (low-pass filtered) at the PCC in the converter frame, ΔP^{c}_{ref} is the active power reference, k_p is the PSL integral gain and $\Delta\theta_v$ is the controller reference angle. AC voltage control is used in this study to support the grid voltage of the ultra-weak AC grid. The linearized control law for the AC voltage loop (AVL) is,

$$\Delta V = \frac{k_u}{s}\left(\Delta U^{cf} - \Delta U^{c}_{ref}\right) \quad (6)$$

where, ΔU^{cf} is voltage magnitude (low-pass filtered) at the PCC in the converter frame, ΔU^{c}_{ref} is the AC voltage reference, k_u is the AVL integral gain and ΔV is the converter voltage reference deviation. In order to damp out the grid-frequency resonances in the system, a high-pass current filter is included to the converter voltage reference, such that the linearized converter voltage control law becomes:

$$\Delta u_{cd,ref} = \Delta V - H_{HP}(s)\,\Delta i^{c}_{cd} \quad (7)$$

$$\Delta u_{cq,ref} = -H_{HP}(s)\,\Delta i^{c}_{cq} \quad (8)$$

where, the high-pass current filter (HPF) is given in (9).

$$H_{HP}(s) = \frac{k_v s}{s + \alpha_v} \quad (9)$$

where k_v is the HPF gain and α_v is the HPF cut-off frequency. The state-space representations of the linearized PSC equations are given in the Appendix. All above mentioned equations are connected to the linearized grid model and the full small signal model is presented in Fig. 2.

B. SMALL-SIGNAL VALIDATION

A time-domain simulation of the full system in MATLAB/Simulink software is used to validate the small signal model developed in Section III-A. A step of 0.05 p.u. is applied to the active power and voltage references in the small signal and time domain models, as shown in Fig. 3. The

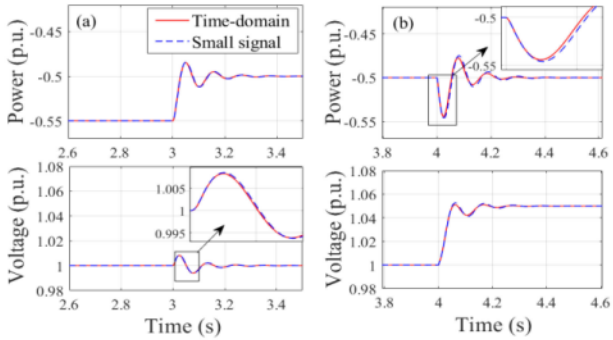

FIGURE 3. **Validation of small-signal model: response of active power and PCC voltage magnitude to a 0.05 p.u. step change (a) active power, and (b) PCC voltage magnitude.**

transient agreement between the small signal model and the time-domain model is very good and so the small signal model can be used for stability analysis with confidence.

IV. STABILITY ASSESSMENT METHODOLOGY

The complete active power limits for PSC-VSC can be determined by assessing system stability across a large range of controller operating points. The PSL and AVL controller bandwidths and the HPF gain should all be varied simultaneously. In this MIMO system, there is cross-coupling between the *d*- and *q*-axis control and so no single parameter can independently control or define the PSL and AVL controller bandwidths. However, there is a correlation between the integral gains, k_p and k_u, and the PSL and AVL bandwidths, and so these gains are used as substitutes for direct control of the respective bandwidths. The +/- 3dB bandwidth can then be calculated in MATLAB for each channel of the MIMO small-signal model to provide an estimate of the PSL and AVL channel bandwidths. At each unique controller tuning, the maximum active power that can be injected into the grid or the DC link is determined. Determination of the active power transfer limits for all controller tunings requires a new stability analysis approach, which can be based on eigenvalue analysis. Eigenvalue analysis has previously been used to assess the impact of only a single variable (one controller tuning or the active power level). The proposed method instead establishes the stability limits as three variables are changed (two controller tunings and the active power). A small signal model is created at each unique controller operating point and the eigenvalues of each of these models is examined to find the active power transfer limits at that controller tuning. This process is shown in Fig. 4 and should be repeated in both inverting and rectifying modes. The input to the process is ranges of k_p, k_u and k_v to be tested (from Table 2) and the output is a matrix of the active power transfer limit, P_{lim}, calculated at each set of controller gains.

To set each new controller tuning, the gains of two control parameters are simultaneously adjusted whilst all other parameters are kept constant. This produces comprehensive active power limits as a function of two controller tunings.

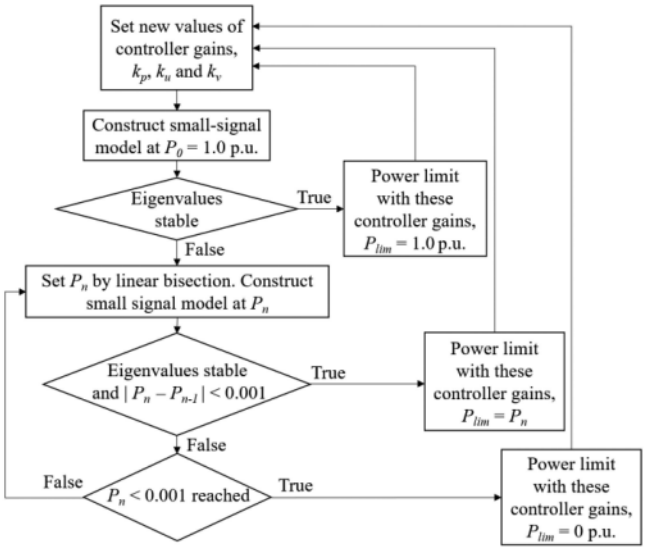

FIGURE 4. **Flowchart of the novel stability analysis methodology to determine active power limits at a broad range of controller tunings.**

TABLE 1. **Default Controller Tuning Parameters**

Controller element	Parameters	Value
PSL	k_p (rad/Ws)	2.5 x 10^{-7}
AVL	k_u	50
HPF	k_v (V/A)	60
	α_v (rad/s)	40

TABLE 2. **Operating Point Ranges**

Controller element	Gain	Parameter range	Equivalent bandwidth range
PSL	k_p	0.5 x 10^{-7} – 15 x 10^{-7}	$\omega_P \approx$ 0.5 – 100 Hz
AVL	k_u	0.1 – 1000	$\omega_U \approx$ 0.02 – 50 Hz
HPF	k_v	0 – 500	-

This is then repeated for all combinations of any two controller parameters. The controller gain values when a given loop is fixed are based on [7] and given in Table 1. Table 2 gives the gain and approximate controller bandwidth ranges (i.e., the +/- 3dB bandwidth calculated in MATLAB from the respective channel of the MIMO small-signal model) covered when varying a given loop, where ω_P is the approximate active power controller bandwidth and ω_U is the approximate AC voltage controller bandwidth.

A. ANALYSIS OF COUPLED EFFECTS OF MULTIPLE CONTROLLER GAINS

Performing sweeps across the controller tuning ranges in Table 2 produces a 3D surface corresponding to the maximum active power transfer that is achievable at a given controller operating point. As discussed in Section IV, the gains k_p

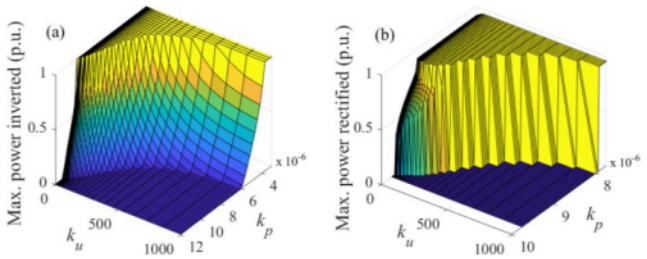

FIGURE 5. Maximum active power transfer with varying AVL and PSL bandwidths with VSC (a) inverting, and (b) rectifying.

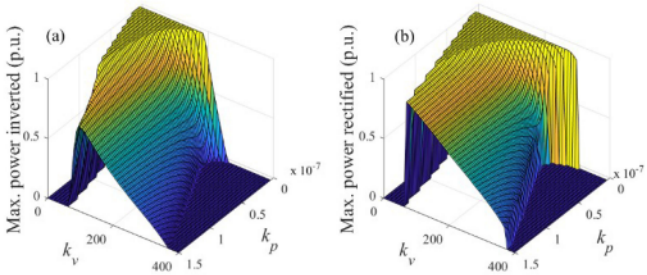

FIGURE 6. Maximum active power transfer with varying HPF gain and PSL bandwidth with VSC (a) inverting, and (b) rectifying.

and k_u are used as proxies for ω_P and ω_U, respectively. The parameter gain range for k_p is $0.5\text{x}10^{-7}$ – $15\text{x}10^{-7}$ rad/Ws, which corresponds to $\omega_P \approx 0.5$ – 100 Hz. The parameter gain range for k_u is 0.1 – 1000, which corresponds to $\omega_U \approx 0.02$ – 50 Hz. The surface in Fig. 5 represents the active power limit with varying PSL and AVL bandwidths. It can be seen that reducing both the PSL and AVL bandwidths increases the active power transfer limit. The result that slowing down the AVL increases stability appears in contrast with [23], which shows that increasing the AVL bandwidth increases the system damping. However, this is likely due to the HPF tuning, which has a significant effect on the system damping and can 'override' the impact of other loops in this respect. This is explored further in Section V-A. Fig. 6 shows the active power limit with changing HPF gain and PSL bandwidth and shows that the HPF gain must be within a narrow range (approx. $10 < k_v < 200$ V/A) to maintain system stability. If the HPF is well tuned and the PSL bandwidth is reduced, the active power can reach the limit determined by the converter rating in both inverting and rectifying modes (−1.0 p.u. and 0.95 p.u. respectively). Stability is more sensitive to HPF tuning if the PSL bandwidth is fast. Regions of high power transfer stability exist at both high and low PSL bandwidths, but for intermediate tunings corresponding to approximately $5 \text{ Hz} < \omega_P < 60$ Hz there is a reduction in achievable active power. The active power limit as a function of HPF gain and AVL bandwidth is shown in Fig. 7. Again, for maximum power transfer, the HPF gain must be within a range $\sim 10 < k_v < 200$ V/A to maximise the stable power limit. Similar to the pattern seen in Fig. 6, there is a region of reduced stability at intermediate AVL bandwidths, approximately $5 \text{ Hz} < \omega_U <$

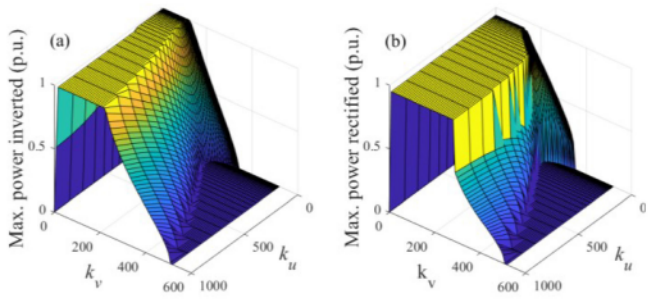

FIGURE 7. Maximum active power transfer with varying HPF gain and AVL bandwidth with VSC (a) inverting, and (b) rectifying.

35 Hz. All control loops have a similar qualitative impact in inverting and rectifying modes, but with slightly lower power transfer levels in rectifying mode due to the asymmetry of VSC systems in weak grids [31].

V. DISCUSSION

A. ANALYSIS OF THE EFFECTS OF INDIVIDUAL CONTROLLER GAINS

1) POWER SYNCHRONIZATION

As discussed in Section IV-A, slowing down the PSL improves stability and therefore increases the maximum active power transfer. However, when the HPF gain is too high, the stable power limit is reduced for $5 \text{ Hz} < \omega_P < 60$ Hz (Fig. 6). This suggests that two different modes of operation are possible. When the PSL is very slow, the controller effectively provides a fixed reference angle, thus emulating some of the behaviors normally associated with grid-forming converter control. With a fast PSL, the controller behaves as expected and provides a varying reference angle that is synchronized to the active power error. However, in general, PSC is limited to slow synchronization speeds for improved robustness, as is discussed further in Sections V-C.

2) HIGH-PASS CURRENT FILTER

The HPF has an optimum gain (k_v), which is between 10–200 V/A depending on the values of other controller parameters. This trade-off in gain occurs because, in the closed-loop system, the high-pass filter has a positive damping effect on the grid-frequency resonance (50 Hz) but introduces a lower frequency resonance near the filter cut-off frequency. This lower-frequency resonance becomes more dominant as the filter gain is increased, as shown in the closed-loop power response bode plots at varying k_v in Fig. 8(using a range of $0 < k_v < 150$ V/A, all other gains at the default values in Table 1). Fig. 5 and Fig. 6 also show that the system becomes increasingly sensitive to the HPF gain as the PSL or AVL bandwidths are increased. Therefore, if fast PSL or AVL dynamic performance is required, the HPF must be very carefully tuned. Dynamic performance is explored further in Section V-D.

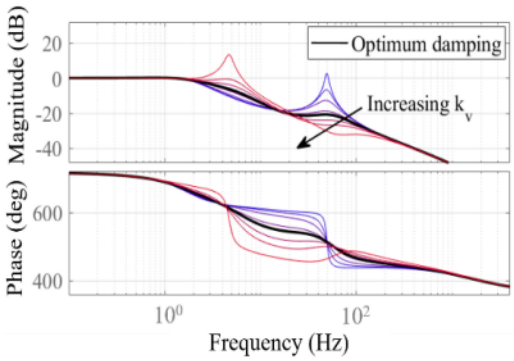

FIGURE 8. Bode diagram of the closed-loop power response with varying HPF gain, $0 < k_v < 150$ V/A (low k_v in blue and high k_v in red).

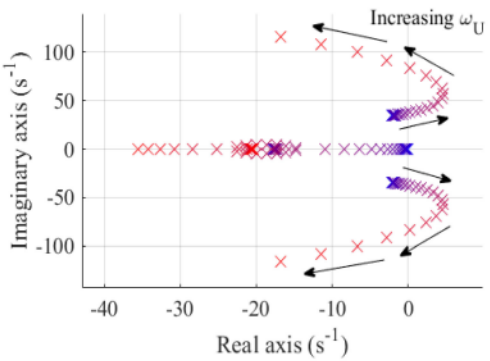

FIGURE 9. Pole map of controlled system with varying AVL gain. $0.1 < k_u < 1000$ (low k_u shown in blue and high k_u shown in red).

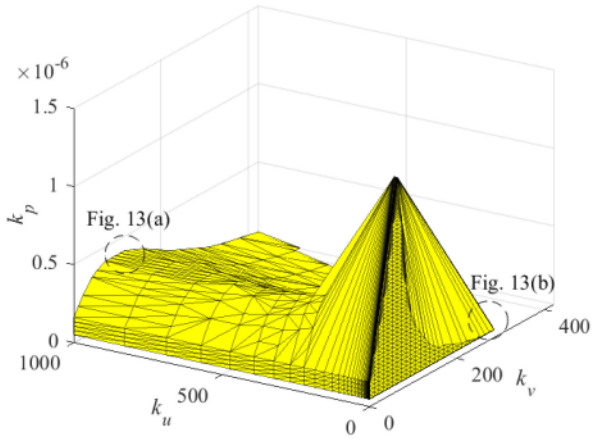

FIGURE 10. PSC parameters for stable operation at $-1.0 < P < 0.85$ p.u. in SCR = 1 AC grid.

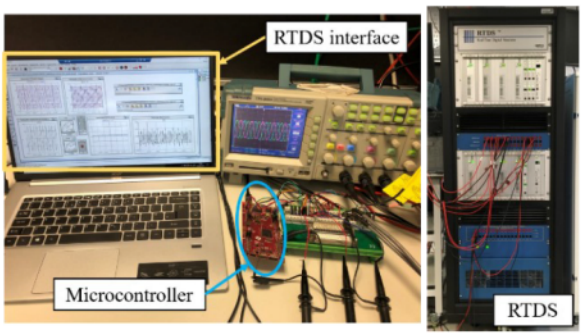

FIGURE 11. RTDS and control hardware-in-the-loop test setup.

3) AC VOLTAGE CONTROL

Very low and high AVL bandwidths can achieve high active power transfer and system stability. However, as with the PSL, there exists an intermediate range of AVL bandwidths at which the maximum active power transfer is reduced. This is due to the presence of a dominant pole pair, which moves towards the RHP and back again as AVL bandwidth increases. This destabilizing pole pair movement is shown in the pole map of the controlled system in Fig. 9.

B. STABLE TUNING REGIONS AND CHIL VALIDATION

Assessing stability over a broad controller operating region as described in Section IV gives a more thorough description of the controller interactions and stabilizing or destabilizing effects of all parts of the PSC control structure. This also indicates how PSC responds to tuning variations and gives a panoramic view of the whole parameter space that can be employed. This assessment gives an indication of performance away from the ideally-tuned design point, which reflects the suboptimal tuning that could arise if there are errors in parameter quantification of the AC system. This analysis can also be used to form a 3D volume, which represents all the stable controller operating points. It is proposed that this region is defined as:

All controller tunings which allow stable operation at active power transfer levels -1.0 *p.u* $< P <$ *0.85 p.u.*

The power limit of 0.85 p.u. in rectifying mode is chosen to correspond to the same overvoltage required for -1.0 p.u. power transfer, which is approximately 1.15 p.u. This stable tuning region is described in terms of the PSL and AVL bandwidths and the HPF gain and is shown in Fig. 10.

In order to validate the location of this stability boundary, CHiL experiments are performed using the RTDS and microcontroller setup shown in Fig. 11. The microcontroller is a TI C2000 Real-Time controller which is interfaced to the RTDS with the same inputs and outputs as would be received from the grid. The system is programmed via RSCAD and Simulink/C++ and a schematic of the CHiL connections and signal routings is shown in Fig. 12. To validate the stability boundary presented in Fig. 10, the controller tunings are perturbed at two controller operating points near to the stability boundary. The system is pushed from within the boundary (stable) to just outside the boundary (unstable). The three-phase PCC voltage and converter current waveforms for this experimental validation are shown in Fig. 13. Fig. 13(a) shows the instability produced in the PCC voltage and converter current when the PSL gain is increased (at operating point (a) on Fig. 10), and Fig. 13(b) shows the instability produced in the PCC voltage and converter current when the PSL gain is

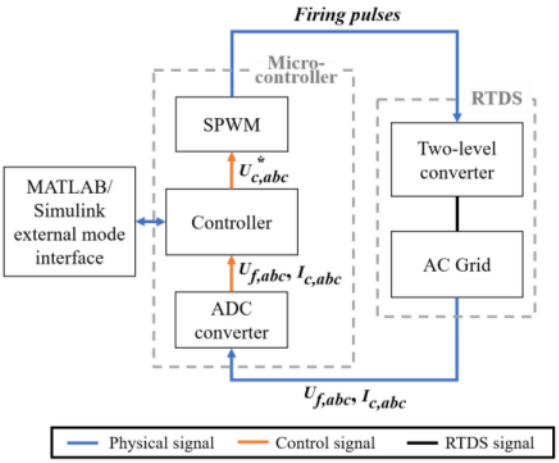

FIGURE 12. Schematic of the CHiL setup and signal routing between the microcontroller and RTDS.

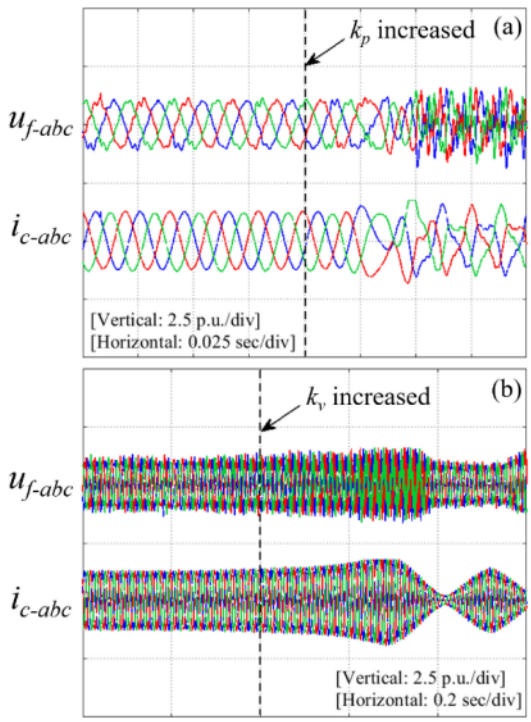

FIGURE 13. CHiL experimental results within (blue) and outside (red) the stable tuning region at points (a) and (b) marked on Fig. 10.

increased (at operating point (b) on Fig. 10). Table 3 gives the controller tunings at these validation points.

As seen in Section IV-A, stability is strongly dependent on correct tuning of the high-pass current filter. Choosing an appropriate value of k_v allows a much faster PSL to be employed. This speeds up the controller response but leads to a very large overshoot if the PSL is too fast. This effect can be seen in the power step responses at different values of k_p shown in Fig. 14. The non-minimum phase behavior of the system is also exacerbated as k_p is increased, as shown in the inset of Fig. 14. If dynamic performance is considered,

TABLE 3. Controller Parameters At Stability Boundary

Figure 10	Parameters within boundary (stable)	Parameters outside boundary (unstable)
(a)	$k_p = 3.5 \times 10^{-7}$ $k_v = 64$ $k_u = 1000$	$k_p = 4.5 \times 10^{-7}$ $k_v = 64$ $k_u = 1000$
(b)	$k_p = 0.5 \times 10^{-7}$ $k_v = 300$ $k_u = 1$	$k_p = 0.5 \times 10^{-7}$ $k_v = 320$ $k_u = 1$

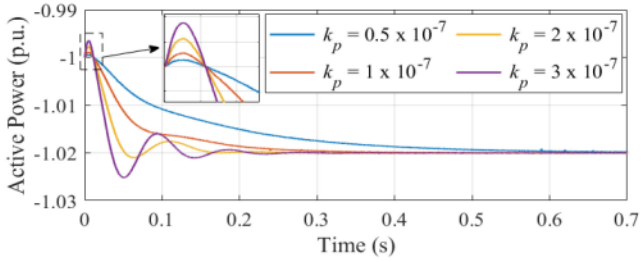

FIGURE 14. Active power response to a 0.02 p.u. step at $P = -1.0$ p.u., $k_v = 65$, $k_u = 50$ and varying k_p.

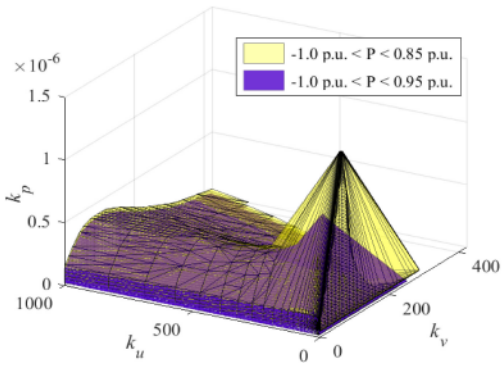

FIGURE 15. PSC parameters for stable operation at -1.0 p.u. $< P <$ 0.85 p.u. (yellow) and -1.0 p.u. $< P <$ 0.95 p.u. (purple).

this behavior will limit the maximum value of k_p, as will be explored further in Section V-D.

For different systems and power transfer requirements, the stable tuning region must be modified. If the converter voltage and apparent power are allowed to reach overrated limits of 1.2 p.u. and 1.35 p.u., respectively, then up to 0.95 p.u. rectifying power can be achieved. The stable tuning region for this higher power level is shown in Fig. 15. Points within this region are all combinations of PSL, AVL and HPF tunings which remain stable between -1.0 p.u. and 0.95 p.u. active power transfer. As expected, the stable operating region is reduced when the power level is increased. Regardless of the control method employed, the power transfer of VSCs in rectifying mode in an ultra-weak grid is ultimately limited by the reactive power requirement. Breaching this limit requires additional reactive compensator hardware, which is beyond the scope of this work.

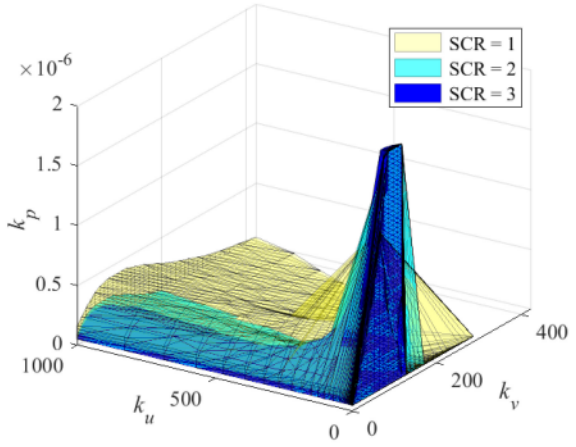

FIGURE 16. PSC parameters for stable operation at -1.0 p.u. $< P < 0.85$ p.u. in systems with varying grid strength, SCR = 1 (yellow), SCR = 2 (cyan) and SCR = 3 (blue).

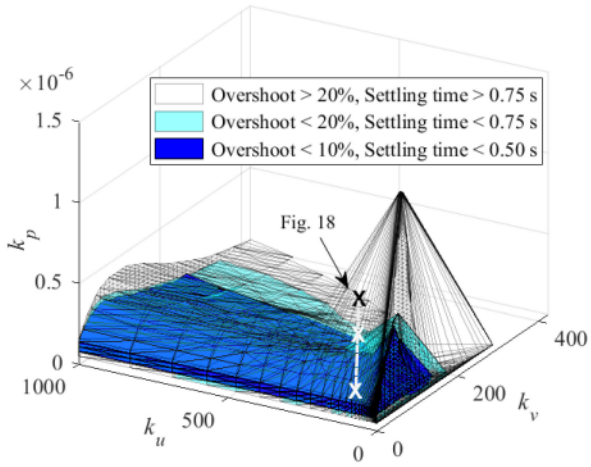

FIGURE 17. PSC parameters for stable operation at -1.0 p.u. $< P < 0.85$ p.u. (white), with 'moderate' transient performance (light blue) and with 'good' transient performance (dark blue) for a unit step change to the power reference.

C. ROBUSTNESS

The robustness of the stable tuning region under different SCRs should also be considered. This demonstrates the controller performance when the grid conditions are intentionally changed, but also crucially gives an indication of the system stability margin if parameter estimation for the grid is inaccurate, leading to sub-optimal controller tuning. The original stable region in Fig. 10 is replicated at different system SCR to assess this aspect. Fig. 16 shows the equivalent stable operating regions for SCR $=$ 1, 2 and 3. These regions have a significant region of overlap but, critically, none are perfectly coincident or contain all the stable controller operating points of another grid setting. Increasing the SCR increases the range of stable PSL bandwidths but decreases the overall stable operating space. Physically, this is because the PCC voltage is stiffer in a strong grid and the grid-forming converter behaves as another voltage source separated by only a small impedance. This is an inherently difficult operating condition and so the stable operating space becomes more limited as SCR increases. At higher SCR, the system is also more sensitive to the HPF tuning, with gains above $k_v \approx 150$ V/A causing significant destabilization. This shift of the stable operating space as grid impedance varies is a potential drawback to PSC as it is susceptible to instability if the grid conditions have not been accurately quantified and incorrect controller tunings chosen. In weak grids, very small changes in impedance result in a large difference in voltage angle and so small errors in parameter estimation have a significant impact on the system operating point. However, if tuned correctly, there is an adequate operating region for which PSC remains stable for SCR 1 to 3.

D. DYNAMIC PERFORMANCE

The parameter sweeps in Section IV and the stable tuning regions in Section V demonstrate that the PSC-VSC can maintain stability when tuned to a number of controller operating points. However, the analysis so far does not consider the differences in transient performance at each of the tunings within the stable parameter space. A second analysis which considers the controller operating region for stability and good transient performance should therefore be performed. New stable tuning regions are defined which meet the criteria used in Section V-C to form Fig. 10, but within which the response to a unit active power step meets certain dynamic requirements. Two levels of transient performance conditions are imposed on the overshoot (OS) and the 2% settling time (ST):

1) 'Moderate': OS $< 20\%$, ST < 0.75 s
2) 'Good': OS $< 10\%$, ST < 0.50 s

At the active power transfer levels -1.0 p.u. and 0.85 p.u., an active power step change is applied to small-signal models across the controller parameter space. Fig. 17 shows the Fig. 10 stable region and two dynamic performance regions with each of these 'moderate' and 'good' transient requirements imposed. All PSC tunings which maintain system stability between the power limits -1.0 and 0.85 p.u. and meet the above dynamic performance requirements for a unit step change to the power reference are contained in these inner dynamic performance regions. The stable tuning regions for 'moderate' and 'good' transient performance comprise a more limited range of controller operating points than for simple stability, as would be intuitively predicted. Fig. 18 shows time domain simulations at points within each of the stability regions in Fig. 17. Controller tunings at each of these validation points are shown in Table 4. The difference in dynamic performance produced by operating in each layer of the stable tuning regions can be clearly seen in Fig. 17. This method therefore provides a much faster way of assessing dynamic performance than computationally expensive time-domain simulations. Taking dynamic performance into account primarily reduces the acceptable range of PSL gains. This is due to the large overshoot that is caused by a very fast PSL, as was demonstrated in the step change responses in Fig. 14. PSC

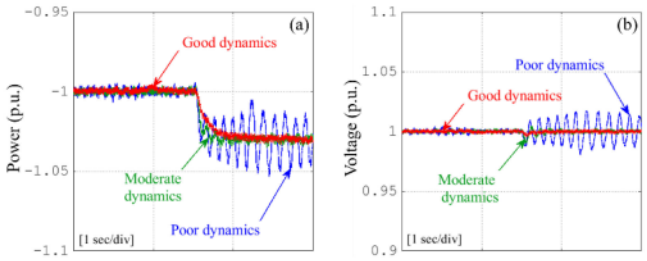

FIGURE 18. CHiL experimental results for dynamic performance validation: response of (a) converter active power and (b) PCC voltage to a step change in power demand at points marked 'X' on Fig. 17.

TABLE 4. Controller Parameters At Fig. 17 Marked Points

Controller parameters	Dynamic performance
$k_p = 1 \times 10^{-7}$, $k_v = 50$, $k_u = 50$	Good
$k_p = 2.5 \times 10^{-7}$, $k_v = 50$, $k_u = 50$	Moderate
$k_p = 5 \times 10^{-7}$, $k_v = 50$, $k_u = 50$	Poor

is therefore limited in the feasible synchronization and power response speeds it can provide. This also limits the possible applications of PSC because it will not be suitable in strong grids where voltage fluctuations are fast and thus a fast controller is essential. These dynamic performance criteria can also be applied to the higher power stable tuning region in Fig. 15. However, no controller operating points were found which could meet either the 'moderate' or 'good' transient behavior limitations at 0.95 p.u. rectifying power level.

VII. CONCLUSION

In this paper, a comprehensive evaluation of power-synchronization control has been performed at a more complete scope of controller operating points than previous works (only one operating point). The achievable active power transfer limits in both inverting and rectifying mode have been established across this range and the stable operating region has been quantified. The coupled impacts of the power synchronization loop, AC control loop and high-pass current filter gains have been assessed, revealing that the high-pass filter has the potential to increase the stable operating space if correctly tuned and that tuning of this gain is increasingly critical as the PSL or AVL bandwidths increase. The boundary of this stable operating space is validated with CHiL RTDS experiments. PSC is relatively robust to overestimations of the system SCR (i.e., underestimate of grid impedance) but less so to underestimations of SCR. Correct tuning of the HPF is critical to improve the robustness of PSC and overall PSC performance is better in weak grids than strong grids. Analysis across the whole stable tuning region has revealed a smaller operational envelope, which also provides good dynamic performance. This region has an upper limit on the PSL gain due to the large overshoot caused by a fast PSL. If the converter is overrated, a stable operating region exists such that transfer of 1.0 p.u. active power in inverting mode and 0.95 p.u. power in rectifying mode is possible. However, the dynamic performance at this very high rectifying power level is poor. The tuning recommendations arising from this work are that the HPF gain must be kept within a fairly narrow band, i.e., $10 < k_v < 200$V/A. This tuning is critical in stronger grids and with a fast PSL or AVL. In general, slowing down the PSL and AVL increases stability and achievable active power transfer.

APPENDIX

A. AC GRID PARAMETERS

AC grid rated voltage (RMS line) = 195 kV, AC grid rated power = 350 MW, AC grid frequency = 50 Hz, SCR = 1, X/R ratio = 10, AC grid inductance, $L_n = 344$ mH, AC grid resistance, $R_n = 10.86\ \Omega$, coupling inductance, $L_c = 69.2$ mH, coupling resistance, $R_c = 1.09\ \Omega$.

B. STATE SPACE SMALL-SIGNAL MODEL

The state-space form of the LCL-AC grid can be found in [7]. The PSL and AVL outer loops are combined into a single state space representation of the form:

$$\Delta\dot{x}_{OL} = B_{OL}\Delta u_{OL},\ \Delta y_{OL} = C_{OL}\Delta x_{OL} \tag{10}$$

with state, input and output vectors, $\Delta x_{OL} = [\Delta e_P\ \ \Delta e_U]^T$, $\Delta u_{OL} = [\Delta P^c_{ref}\ \ \Delta U^c_{ref}\ \ \Delta P^{cf}\ \ \Delta U^{cf}]^T$ and $\Delta y_{OL} = [\Delta\theta\ \ \Delta V\ ]^T$ respectively. The corresponding state-space matrices are,

$$B_{OL} = \begin{bmatrix} -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix},\ C_{OL} = \begin{bmatrix} k_p & 0 \\ 0 & k_u \end{bmatrix} \tag{11}$$

The converter voltage controller, including the high-pass current filter has the state-space form,

$$\begin{aligned} \Delta\dot{x}_{VC} &= A_{VC}\Delta x_{VC} + B_{VC}\Delta u_{VC},\ \Delta y_{VC} \\ &= C_{VC}\Delta x_{VC} + D_{VC}\Delta u_{VC} \end{aligned} \tag{12}$$

with input and output vectors, $\Delta u_{VC} = [\Delta V\ \ \Delta i^c_{cd}\ \ \Delta i^c_{cq}]^T$ and $\Delta y_{VC} = [\Delta u^c_{cd}\ \ \Delta u^c_{cq}]^T$ respectively. The corresponding state-space matrices are,

$$\begin{aligned} A_{VC} &= \begin{bmatrix} -\alpha_v & 0 \\ 0 & -\alpha_v \end{bmatrix},\ B_{VC} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \\ C_{VC} &= \begin{bmatrix} -k_v\alpha_v & 0 \\ 0 & -k_v\alpha_v \end{bmatrix},\ D_{VC} = \begin{bmatrix} 1 & k_v & 0 \\ 0 & 0 & k_v \end{bmatrix} \end{aligned} \tag{13}$$

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