The Investigation of Fabrication and Reliability of Solution-Processed High-k Dielectrics

溶液法高k介质在制备和稳定性中的研究

A Thesis Submitted to

University of Liverpool

in Partial Fulfillment of the Requirements for

the Degree of Doctor of Philosophy

in the Department of Electrical Engineering and Electronics

2020

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Abstract

Solution-processed high-*k* dielectrics have become a strong research focus in both academic and industrial fields. However, solution-processing brings poor film quality and stability. Increasing the reliability of solution-processed devices becomes challenging, especially those devices for nuclear and aerospace applications. To address this issue, this work focuses on the fabrication and reliability investigation of solution-processed high-*k* dielectrics and devices and provide an insight into their bias-stress (BS) and biased radiation stress (BRS) stability degradation.

In chapter 3, the annealing effects on the aqueous solution-processed AlO_x thin films were investigated. On-site radiation measurements were carried out to analyze the BS and BRS stability of AlO_x metal-oxide-semiconductor capacitors (MOSCAPs) under 92 Gy (SiO_2) γ-ray radiation. It was found that aqueous solution-processed AlO_x thin films with reduced impurities, low leakage current, and satisfied BS stability could be successfully formed at annealing temperature > 250 ºC. Compared to the Al_2O_3 thin films fabricated by atomic layer deposition (ALD), the BRS stability of aqueous solution-processed AlO_x thin films is mainly degraded by radiation-induced oxide traps related to the precursor impurities and loosely bonded oxygen. The findings of this chapter offer clear inspiration for achieving highly stable solution-processed high-*k* dielectrics working in harsh radiation environments.

In chapter 4, it is demonstrated that hydrogen peroxide (H_2O_2) is a strong oxidizer to improve the thin film quality and stabilities of solution-processed dielectrics. Their

interface trap density was reduced, and the BS stress stability of AlO_x MOSCAPs was improved. Furthermore, 7.5 M H2O2-AlOx MOSCAPs exhibit ignorable radiation-induced oxide and interface traps with total dose up to 42 Gy (SiO_2) through carrying out on-site measurements. The 7.5 M H_2O_2-AlO_x MOSCAPs also demonstrate the ability to recover after the bias was interrupted. The results demonstrate that employing H_2O_2 in the solution-process has significant potential to improve the stabilities of large-area electronics for nuclear and aerospace applications.

In chapter 5, the effects of lanthanum composition on the ambient air stability, BS stability and radiation hardness of the water-induced (WI) solution-processed ZrLaO thin films and InO_x/ZrLaO thin film transistors (TFTs) were investigated. The ZrLaO thin films with 10% La have remained stable under 5-weeks ambient air exposure and 1.44 kGy γ-ray irradiation. The $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs exhibited satisfied ambient air stability (10-days ambient air exposure) and radiation hardness (1.03 kGy irradiation). The optimized InO_x/ZrLaO TFT with 10 % La exhibited a low operating voltage of 4 V and a high I_{on}/I_{off} of around 2×10^6. Besides, their application in resistor-loaded inverters with a gain of 12 at 4 V was also demonstrated. The results represent a great step toward the achievement of low-cost, low-power consumption and large-area flexible electronics working in harsh radiation environments.

Keywords: Water induced (WI) solution-process; High-*k* gate dielectric; AlO_x; ZrLaO; Biased radiation stress (BRS) stability; On-site radiation measurements; Hydrogen peroxide (H_2O_2); Thin-film-transistor (TFT); Radiation hardness; Inverter.

摘要

溶液法的高 k 电介质已成为学术和工业领域的研究重点。然而，溶液法会带来较差的薄膜质量和稳定性。提高溶液法设备的可靠性变得具有挑战性，尤其是那些用于核和航空应用的设备。为了解决这个问题，本工作着重于溶液法的高 k 电介质和器件的制造和可靠性研究，并深入了解其偏压应力（BS）和偏压辐射应力（BRS）的稳定性退化。

在第 3 章中，研究了退火对水溶液法的氧化铝（AlO_x）薄膜的影响。采用原位技术分析了在 92 Gy（SiO_2）伽马射线辐射下 AlO_x 金属氧化物半导体电容（MOSCAPs）的 BS 和 BRS 稳定性。结果发现，在退火温度> 250 ºC 时，可以成功地通过水溶液法制备 AlO_x 薄膜，该薄膜具有较少的杂质，较低的漏电流和令人满意的 BS 稳定性。相较于原子层沉积（ALD）制备的 Al_2O_3 薄膜，水溶液法制备的 AlO_x 薄膜的 BRS 稳定性退化主要受辐射诱导的氧化物陷阱的影响，这与溶液法的 AlO_x 中的前驱物杂质和松散键合的氧有关。本章的发现为实现在辐射恶劣的环境中工作的高度稳定的溶液法高 k 电介质提供了明确的灵感。

在第 4 章中，证明了过氧化氢（H_2O_2）是一种强氧化剂，可以改善薄膜质量和溶液法电介质的稳定性。降低了它们的界面陷阱密度，提高了 AlO_x MOSCAP 的 BS 应力稳定性。此外，通过进行实时测试，7.5 M H_2O_2-AlO_x MOSCAP 在总剂量高达 42 Gy（SiO_2）情况下，表现出可忽略的辐射引发的氧化物和界面陷阱。7.5 M H_2O_2-AlO_x MOSCAP 还显示出在偏置被中断后恢复的能力。结果表明，在溶液法中使用 H_2O_2 具有显着的潜力，可提高用于核与航空航天应用的大面积电子设备的稳定性。

在第 5 章中，研究了 La 组成对水溶液法（WI）的（氧化锆掺杂氧化镧）ZrLaO 薄膜和 InO_x / ZrLaO 薄膜晶体管（TFT）的环境空气稳定性，BS 稳定性和抗辐射性的影响。La 含量为 10％的 ZrLaO 薄膜在 5 周的环境空气暴露下和 1.44 kGy 伽马射线辐照下保持稳定。$InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs 表现出令人满意的环境空气稳定性（环境空气暴露 10 天）和抗辐射性（1.03 kGy 辐射）。经过优化的 La 含量为 10％的 InO_x/ZrLaO TFT 具有 4 V 的低工作电压和大约 2×10^6 的高 I_{on}/I_{off}。此外，还展示了它们在电阻负载的反相器中的应用，该反相器在 4 V 时增益为 12。 这些结果是向着辐射恶劣的环境中工作的低成本，低功耗和大面积柔性电子设备迈出的重要一步。

关键字：水溶液法；高 *k* 栅极电介质；AlO_x；ZrLaO；偏压辐射应力（BRS）稳定性；原位辐射测试；过氧化氢（H_2O_2）；薄膜晶体管（TFT）；抗辐射性；反相器。

Acknowledgements

Firstly, I owe heartfelt thanks to my distinguished and cordial supervisor, Prof. Cezhou Zhao, for providing the Ph.D. study opportunity and supporting my idea of carrying out my Ph.D. study. He guided me with practical academic advice and feasible instructions, and enlightened me while I was confused during the writing. His thought-provoking comments and patiently encouragements are indispensable for my accomplishment of this thesis. Besides the suggestions and supervision in my academic research, his attitude towards living and learning also influences me. It is a great pleasure working with him. Without his dedicated assistance and insightful supervision, this thesis would have gone nowhere.

Secondly, I appreciate Dr. Chun Zhao for his professional and technical advice on my research work. He spent a lot of time revising my manuscript no matter how busy he was. My publications couldn't succeed without his help. Thirdly, I would like to thank Dr. Ivona Z. Mitrovic and Prof. Stephen Hall for encouraging me to expand my knowledge and helping me with my English express skills. They have offered help and support by all means. Fourthly, I am grateful to my supervisors Prof. Stephen Taylor and Prof. Paul R. Chalker for their patient instructions during my study visit to the University of Liverpool. I also appreciated Dr. Sang Lam and Dr. Yina Liu for sharing their knowledge in my research work, which give me many ideas to solve the problem in the Ph.D. study. Besides, I want to give my sincere gratitude to my senior fellows Dr.

Yifei Mu, Dr. Qifeng Lu, Dr. Ruize Sun, Dr. Jinjing Wu, who shared with me a lot of experience in experimenting, analyzing experimental results, writing articles and so on. They always encouraged me with their similar experience met during the Ph.D. study. Furthermore, many thanks to my comrades: Ms. Yanfei Qi, Mr. Chenguang Liu, Mr. Yutao Cai, Ms. Yinchao Zhao, Mr. Ruowei Yi, Ms. Miao Cui, Mr. Tianshi Zhao, Mr. Qihan Liu, Mr. Jiawei Ren, Mr. Zongjie Shen, Mr. Li Yin, Mr. Haibin Wang, Ms. Yi Sun, Mr. Ang Li, Mr. Yixin Cao, Mr. Qinan Wang, Ms. Yudan Yuan, Mr. Xiangfei Lin, Mr. Xianwei Geng, Mr. Jun Liu, Mr. Zitan Cheng, Mr. Minxue Gu, and Mr. Tao Song.

Last but not least, I need to give special thanks to my parents for their unconditional love and trust. They always stand with me, which gave me the power to complete a four-year Ph.D. study. I am deeply moved for their silent support and concerns. I want to express my heartfelt acknowledgment of all they gave me.

Yuxiao Fang

22/2/2020

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List of Publications

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JOURNAL ARTICLES

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[1] **Yuxiao Fang**, Chun Zhao, Stephen Hall, Ivona Z. Mitrovic, Wangying Xu, Li Yang, Tianshi Zhao, Qihan Liu, and Cezhou Zhao, "Aqueous solution-processed AlO_x dielectrics and their biased radiation response investigated by an on-site technique," *Radiat Phys Chem*, vol. 170, p. 108644, 2020. (1.86, Q2)

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List of Abbreviations and Acronyms

AFM	Atomic force microscopy
ALD	Atomic layer deposition
Al_2O_3/AlO_x	Aluminum oxide
$Al(NO_3)_3 \cdot xH_2O$	Aluminum nitrate hydrate
BS	Bias-stress
BRS	Biased radiation stress
CBO	Conduction band offset
C-f	Capacitance-frequency
C_{FB}	Flat-band capacitance
C_i	Areal capacitance
C_{it}	Interface trap capacitance
C_m	Measured capacitance
CMOS	Complementary Metal-Oxide-Semiconductor
C_{ox}	Oxide layer capacitance
C_s	Space charge capacitance
C-V	Capacitance-voltage
DI water	Deionized water
E-beam	Electron-beam
Eg	Bandgap width

EHPs	Electron-hole pairs
FT-IR	Fourier transform infrared spectroscopy
Ge	Germanium
G_m	Measured conductance
G_m-f	Conductance-frequency
Gy	Gray
ΔG	Gibbs free energy change
H^+	Proton
ΔH	Formation enthalpy
HF	Hydrofluoric acid
HfO_2/HfO_x	Hafnium oxide
High-*k*	High dielectric constant
H_2O_2	Hydrogen peroxide
IC	Integrated circuit
I-V	Current-voltage
I_{DS}	Drain current
I_{DS}-V_{DS}	Output characteristic
I_{DS}-V_{GS}	Transfer characteristic
I_{GS}	Gate current
In_2O_3/InO_x	Indium oxide
I_{off}	Off current

I_{on}	On current
IZO	Indium-zinc-oxide
J_{leak}-V	Leak current density-voltage
J_{leak}-E	Leak current density-electrical field
La_2O_3	Lanthanum oxide
MEC	Maximum equal criterion
M-O	Metal-oxide
M-OH	Hydrolyzed metal
M-O-M	Metal-oxide framework
MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
N_2	Nitrogen gas
NBS	Negative bias stress
NBRS	Negative biased radiation stress
N_{it}	Interface trap density
ΔN_{it}	Variation of interface trap density
NM	Noise margin
N_{ot}	Oxide trap density
ΔN_{ot}	Variation of oxide trap density
NO^{3-}	Nitrate group
O-H	Hydroxyl group

PBS	Positive bias stress
PBRS	Positive biased radiation stress
PCBM	[6,6]-phenyl-C_{61}-butyric acid methyl ester
PES	Polyethersulfone
RCA	Radio Corporation of America
RE	Rare earth
RILC	Radiation induced leakage current
R_{it}	Interface trap resistance
RMS	Root-mean-square
R_s	Series resistance
Si	Silicon
Si^-	Silicon dangling bond
SiO_2	Silicon dioxide
SS	Subthreshold swing
Ta_2O_5	Tantalum oxide
TFT	Thin film transistor
TGA-DSC	Thermogravimetric analysis-differential scanning calorimetry
TiO_2	Titanium oxide
TMA	$(Al(CH_3)_3)$
UV	Ultraviolet
V_{DS}	Drain voltage

V_{FB}	Flat-band voltage
ΔV_{FB}	Flat-band voltage shift
V_{GS}	Gate voltage
V_o	Oxygen vacancy
V_{TH}	Threshold voltage
ΔV_{TH}	Threshold voltage shift
WI	Water induced
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
γ–ray	Gamma-ray
Y_2O_3	Yttrium oxide
ZrO_2	Zirconium oxide

Chapter 1: Introduction

1.1 Review of high-*k* dielectrics

The transistor is one of the greatest inventions of the 20th century and laid the foundation for the birth of integrated circuits (ICs) later. In 1947, the world's first transistor was developed by a research group of Bell Labs in the United States. This transistor was based on germanium (Ge) and can amplify the signal 100 times. For early applications such as radios and telephones, the initial transistors were sufficient, but with the development of science and technology, the combination of smaller size and a larger number of transistors is required, which is IC. Consequently, in 1958, near the tenth anniversary of the invention of the transistor, the world's first IC was invented. It only consisted of a bipolar transistor, a capacitor, and three resistors. This invention successfully realized the integration of various electronic devices on a single semiconductor material. Although the first transistor had a quite large size, it had created a new era in the history of microelectronic technology. In 1960, a Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) device was successfully developed. It had the advantages of high reliability and low power consumption, which made it become the core part of the advanced digital ICs and continue to develop in the last 10 years at a surprising rate [1]. In 1962, the first thin thin-film transistor (TFT) was developed by Paul K. Weimer in RCA (Radio Corporation of America). TFT is a special type of MOSFET with similar structure and operation principles [2]. TFTs are made by

depositing an active semiconductor layer, a dielectric layer, and metallic contacts over a non-conducting substrate. Glass is a common substrate, because the primary application of TFTs is in liquid-crystal displays (LCDs). On the other hand, conventional MOSFET typically use semiconductor material as substrate, such as silicon wafers.

Most of the traditional TFT use thermally grown or vacuum-deposited SiO_2 (k = 3.9) as gate dielectrics, as SiO_2 has the advantages of high thermodynamic stability, large bandgap, and good reliability. However, using SiO_2 as the gate dielectric could lead to high operation voltages (> 20 V). In general, high operating voltage results in high power consumption and it is a critical barrier for portable, battery-powered TFT applications. Various gate insulators with large areal capacitances, including organic dielectrics, electrolyte dielectrics, and high-*k* oxide dielectrics have been explored to circumvent this bottleneck. Among these, high-*k* oxide dielectrics have received the most attention because of their large permittivity and the excellent heterogeneous interface with oxide-semiconductor active layers. TFT is a capacitance-based device, where the TFT source-drain current depends on the gate capacitance. The capacitance per unit area (C_i) can be simply expressed as

$$C_i = \frac{\varepsilon_0 \varepsilon_{ox} A}{t_{ox}} \tag{1-1}$$

where ε_0, ε_{ox} and t_{ox} is vacuum permittivity, dielectric constant, and dielectric thickness, respectively. For conventional SiO_2 dielectric, the dielectric constant $k = 3.9$. According to (1-1), in order to gain large capacitance density for low-voltage operation,

two options are available: (a) reduced dielectric thickness; or (b) enhanced dielectric constant of gate dielectric. Utilizing high-*k* dielectrics could achieve low operation voltage, low power consumption and low gate leakage current at the same time. By far, high-*k* metal oxide TFTs fabricated by conventional vacuum-based technologies have been well established and commercialized in a short period [3]. After considering many aspects, there are several criteria for selecting a suitable high-*k* oxide to serves as a gate dielectric. By far, high-*k* metal oxide TFTs fabricated by conventional vacuum-based technologies have been well established and commercialized in a short period [3]. After considering many aspects, there are several criteria for selecting a suitable high-*k* oxide to serves as a gate dielectric.

1. Appropriate *k* value

For next-generation gate dielectric applications, appropriate *k* should be chosen (> 10). Under the same areal capacitance, employing high-*k* dielectrics effectively increases physical thin film thickness (4 - 7 times) and reduces leakage current caused by tunnelling. Generally, for a material, the *k* value represents the polarizability under an applied electric field, which is related to the charge reorganization, including orientation, ionic, and electronic polarization [4]. It is noticeable that *k* value should not be too large (< 30) to avoid the formation of a 2D electric fringing field from the drain through the thick (physical) gate dielectric, which could lower the source to channel potential barrier and hence the threshold voltage (V_{TH}) [5].

Table 1-1. Dielectric constant (k), bandgap width (E_g), and conduction band offset (CBO) with Si of several high-k materials [6].

Materials	**Dielectric constant** ***k***	**Bandgap width** **E_g (eV)**	**Conduction band offset with Si (eV)**
Si	-	1.1	-
SiO_2	3.9	9	3.2
Al_2O_3	9	8.8	2.4
Y_2O_3	15	6	2.3
Ta_2O_5	22	4.4	0.35
HfO_2	25	5.8	1.4
ZrO_2	25	5.8	1.5
La_2O_3	30	6	2.3
TiO_2	80	3.5	0

2. Large bandgap width (E_g) and conduction band offset (CBO)

Large E_g and CBO suppress the tunnelling possibility, thus reduce the leakage current. As shown in Table 1-1, high-k oxide dielectrics exhibit narrower E_g and a smaller band offset than SiO_2, which is related to the electronegativity of high-k oxide dielectrics. Higher electronegativity brings a lower conduction band [7]. The requirements of energy band offset between high-k dielectric and semiconductor are indicated in Figure 1-1. Generally, for high-k dielectrics, the CBO should be >1eV with

the semiconductor to suppress the leakage current caused by the thermionic emission of electrons/holes into the dielectric bands. Therefore, E_g of an insulator should be >5 eV to guarantee sufficient CBO. The tradeoff between *k* and E_g can be found in Figure 1-2. As mentioned before, the *k* value should not be too large to avoid forming the 2D electric fringing field. Another reason is that, for some high-*k* materials (e.g. TiO_2), although the *k* values are >40, their E_g and CBO are too small to block the leakage current when serving as a gate dielectric of a TFT device. Take E_g and CBO into consideration; high-*k* metal oxide dielectrics with relative low *k* value have sometimes been adopted.

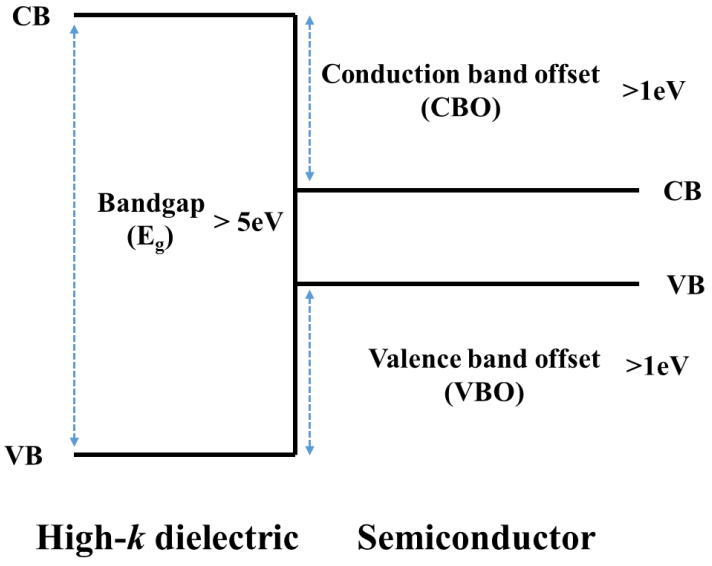

Figure 1-1. Requirements of energy band offset between high-*k* dielectric and semiconductor.

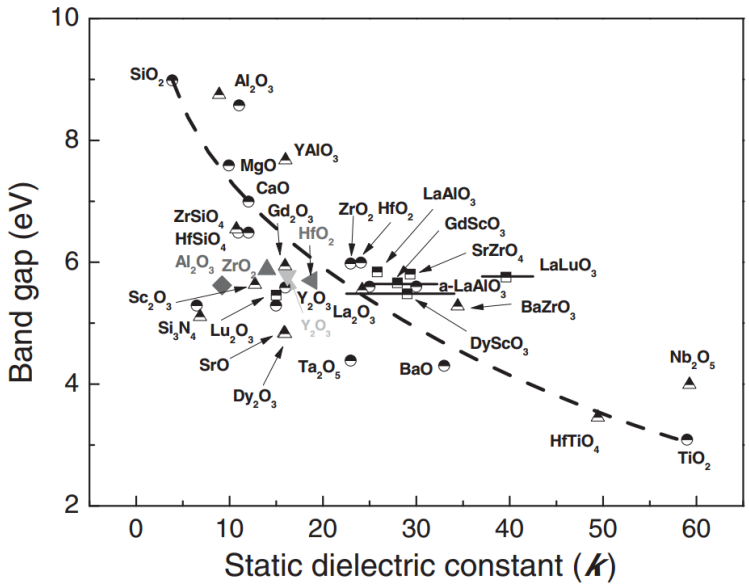

Figure 1-2. Bandgap versus static dielectric constant for different gate oxide materials [8].

3. The ability to suppress moisture absorption

High-*k* materials are inevitably exposed to moisture and air, especially those fabricated by solution-process. As a result, the resistance to moisture absorption is an important property for a high-*k* gate dielectric. The moisture absorption phenomenon in high-*k* oxides is the reaction between the solid oxide (M_mO_n) film and the gaseous state water (H_2O) in the air, as represented by (1-2) [9].

$$M_mO_n + H_2O(g) \rightleftharpoons M(OH)_n \tag{1-2}$$

The reaction speed is directly related to the Gibbs free energy change(ΔG) during the reaction. As shown in Figure 1-3, small ΔG represents the decreased system energy, indicating poor ability to suppress moisture absorption. Hafnium oxide (HfO_2) exhibits a small moisture absorption possibility with a positive G. While lanthanide oxide (La_2O_3) demonstrates the highest moisture absorption speed, which severely degrades

the reliability and stability of La_2O_3 based TFT devices. As a result, TFT devices based on high-k dielectrics with large negative ΔG need additional processing technologies to improve and stabilize the device properties.

4. Smooth surface morphology and low defect density

For a TFT device, the smooth surface morphology and low defect density of gate dielectrics are crucial to suppress the leakage current and improve device mobility and stability. The electrode and the semiconductor film sandwich a gate dielectric; the ideal dielectric should produce a smooth dielectric/semiconductor interface with low interface defect density. As the charge transport occurs nearby the interface, the interface defects can cause the scattering and trapping of the charge carriers, leading to the degradation of the TFT mobility and stability [10]. When it comes to the commercial application of TFT, long-term bias-stress (BS) stability is crucial. The charge trapping at/ near the dielectric/semiconductor interface induces the distortion of capacitance-voltage (C-V) curves and the shift of V_{TH}. It has been reported that a slight V_{TH} shift of 0.1 V for the driving transistor can induce luminance variations of the OLED pixels by ≈20% [11]. For solution-processed high-*k* oxides, common defects are oxygen vacancies, hydroxyl groups, and dangling bonds. The density of these defects is mainly determined by the fabrication process and post-treatment condition [12-15].

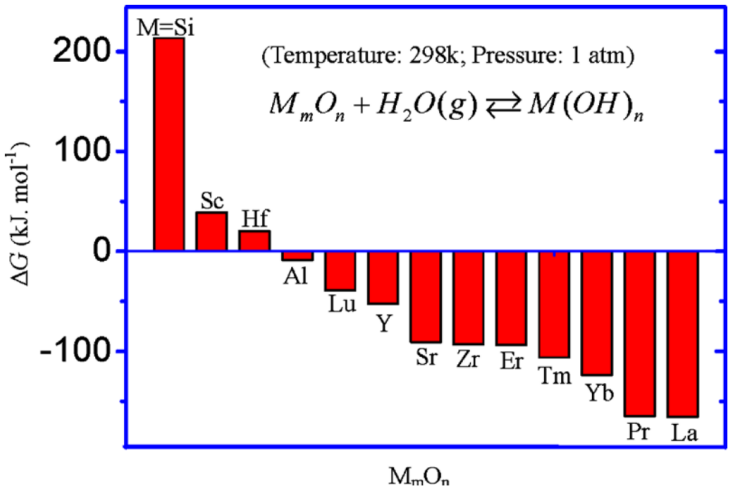

Figure 1-3. Gibbs energy changes (ΔG) for moisture absorption reactions in high-*k* oxides under standard conditions [9].

1.2 Review of solution-process

1.2.1 Overview

The deposition methods of high-*k* oxide are of great importance. Traditional vacuum-based methods such as chemical vapor deposition and sputtering require long processing time and high vacuum environments. The high-cost equipment, complex fabrication process, and relatively small area deposition limit the potential applications of vacuum-based techniques in large-area electronics. Over the past decade, the solution-processed thin film deposition technique for oxide materials has been well developed; it eliminates the vacuum deposition processes and replaces them with printable precursor materials [6, 16, 17]. Compared to traditional vacuum thin film deposition methods, solution-processes enable the fabrication of larger area flexible metal oxide TFTs due to advantages of simplicity, low-cost, roll-to-roll (R2R) capability,

atmospheric processing and high throughput [18, 19]. Thus, the solution-process has become a strong research focus in both academic and industrial fields. For industrial applications, Evonik Resource Efficiency GmbH has demonstrated the large-area processing of solution-processed metal oxide TFT backplanes and the integration in highly stable OLED displays [20]. Besides, emerging non-display applications (e.g. photodetectors, biosensors, and memory devices) based on solution-processed metal oxides are rapidly advancing [21, 22].

1.2.2 Sol-gel chemistry

Generally, to deposit solution-processed metal oxides, there are two routes, one is the nanoparticle-based process, and another one is metal salt-based sol-gel chemistry. When depositing metal oxide thin films using solution-process, materials are synthesized through a phase transformation from liquid precursors to a sol (colloidal suspension) and finally to a gel (network structure) [16]. As shown in Figure 1-4 (a) and (b), the solvent molecules transfer the metal cations into metal hydroxides (M-OH) through a hydrolysis reaction. Subsequently, the condensation reaction occurs to form metal oxide (M-O-M) frameworks through an oxolation reaction between metal hydroxides, which is exhibited in Figure 1-4 (c) [16]. Finally, a xerogel-like oxide film is formed by coating a sol-gel precursor solution onto substrates and thermally annealed at temperatures typically above 400 ^{o}C. High-temperature annealing has the function of

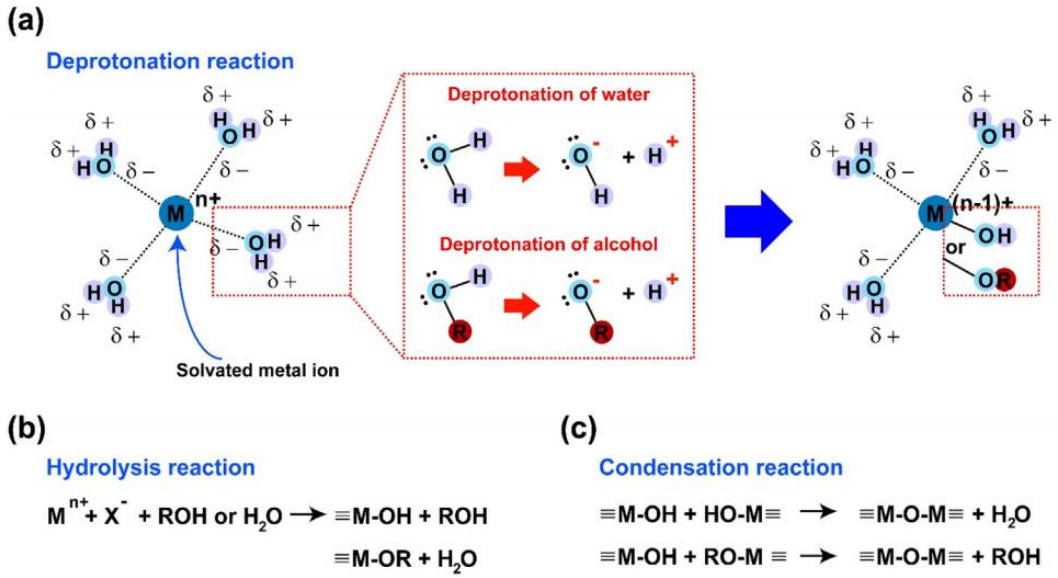

Figure 1-4. Sol-gel chemistry in metal oxide materials. **(a)** Schematic of reactions between metal ions and water/alcohol molecules. **(b)** Chemical reactions of hydrolysis and **(c)** chemical reactions of condensation [16].

completing the condensation reaction, removing chemical impurities/byproducts, and densifying the resultant oxide film [16].

1.2.3 Low-temperature processes

Though many solution-processed devices have demonstrated good device characteristics, high-temperature annealing (> 400 °C) is essential to form dense and no-pinhole films with a metal oxide framework. Simple low-temperature annealing is unacceptable because it results in large amounts of existing M-OH, which severely degrade the carrier transportation efficiency [23]. High-temperature annealing of solution-process limits the potential application of solution-processed materials on flexible substrates. Therefore, it is necessary to develop low-temperature solution-processed techniques to realise flexible and large-area oxide electronics fully. To lower

the annealing temperature, alkoxide precursors (see Chapter 1 Appendix for more information) [24], chemical combustion reaction (see Chapter 1 Appendix for more information) [25], UV/ plasma-assisted activation [26], and carbon-free WI route have been recognized as promising approaches [27].

In this work, the WI route has been utilized. Generally, organic solvents require constant thermal energy to break existing chemical bonds in specific organic species [28]. Besides, pinholes are easily formed among the thin film after the decomposition of organic solvent. Therefore, the organic solvent is the limitation of further lowering the fabrication temperature and improving the thin film quality. Deionized (DI) water is a suitable precursor solvent for low-temperature fabrication. It is reported that the coordination bond between the cation and neighboring aquo ion is an electrostatic reaction, which breaks more easily compared to covalent bonds in conventional organic-based precursors [29]. Therefore, dihydroxylation and condensation are achieved with sufficient annealing time when employing the WI route. In addition to applying water as a solvent, the selection of precursor metal salt is important to achieve a structurally dense oxide framework at low temperatures. Commonly used metal salts for oxide film fabrication mainly include chloride, acetate, fluoride, and nitrate. To clarify the thermal decomposition characteristic of each metal precursor, Yang et al. investigated thermogravimetric (TGA) results, as shown in Figure 1-5 [30]. Nitrate precursors are found to be decomposed at a lower temperature than other types of precursors.

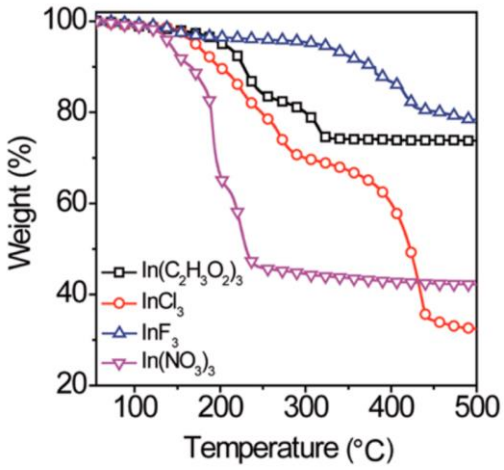

Figure 1-5. Thermogravimetric (TGA) analyses of diverse aqueous metal precursors: $In(C_2H_3O_2)_3$, $InCl_3$, InF_3, and $In(NO_3)_3$ [30].

In 2003, to combine the water solvent and metal nitrate precursor, Hwang et al. employed DI water as the precursor solvent and successfully fabricated oxide TFT at annealing temperature <200 ºC [31]. They demonstrated that $In(NO_3)_3$ can form $(In(OH_2)_6)^{3+}$ after dissolving in DI water, and metal oxide framework was easily formed at low temperature with this structure. Additionally, the decomposition temperature of HNO_3 is quite low, and the annealing temperature to transform precursor film into InO_x metal oxide can be as low as 160 ºC. The detailed stages of thin-film formation from nitrate precursors are demonstrated in Figure 1-6 [32]. On the other hand, post-treatment techniques are alternative selections to achieve low-temperature fabrication. Plasma assisted pretreatment [33], UV assisted photochemical activation [34], high-pressure annealing [35], and microwave annealing[36] have been demonstrated to effective eliminate defect states, improve dielectric film performance and reproducibility at low temperature.

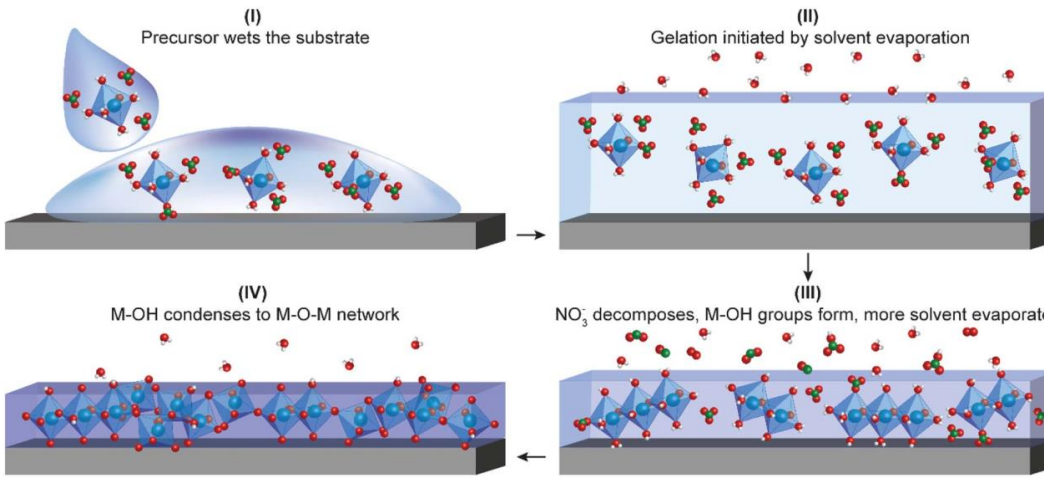

Figure 1-6. Stages of thin-film formation from solution precursors. **(I)** The substrate is wetted with an aqueous metal nitrate solution. Adequate wetting is achieved via substrate surface preparation treatments to remove organic contaminants and introduce polar functional groups to impart hydrophilicity. **(II)** The thin-film precursor gel is formed by the rapid evaporation of the excess solvent (H_2O, in this example). The resulting metal-nitrate gel must then be decomposed to form a metal oxide. **(III)** With the addition of energy (commonly thermal annealing), additional solvent is evaporated and nitrates decompose to HNO_3, NO_x, etc. Condensation is initiated, forming $M(OH)_x$ species. **(IV)** Once nitrates and solvent are removed, $M(OH)_x$ further condense to form the final metal oxide [32].

1.2.4 Deposition methods

Common solution-processed methods include dip-coating[37], spin-coating [38], spray-coating [39], bar coating [40] and inkjet-printing [41]. General information about these methods is listed in Table 1-2. Each technique has its advantages and disadvantages, including operational ease, precursor preparation, position accuracy, throughput efficiency, and R2R compatibility. As shown in Figure 1-7, the spin coating has been widely utilized to fabricate oxide dielectric due to its simple operation, good

reproducibility, high precision and easy integration with conventional micro-fabrication techniques [6]. This method requires very little precursor solution and is suitable for a wide range of solutions with different viscosity. By controlling the spin rate, solution viscosity, and temperature, films with different thicknesses from 10 to 5000 nm can be simply obtained. Furthermore, pretreatment can ensure good substrate surface hydrophilia, which ensures the quality of the formed film. Nevertheless, spin coating only utilizes 5-10 % of the precursor solution during the deposition process and is not compatible with R2R processing to integrate large TFT arrays.

Table 1-2. Various solution-processed thin-film deposition methods [42, 43].

Technique	**Spin coating**	**Spray coating**	**Bar coating**	**Inkjet printing**
Ink preparation	Simple	Moderate	Simple	Moderate
Ink waste	Significant	Considerable	Little	None
Speed	-	Fast	Medium	Medium
Noncontact processability	Yes	Yes	No	Yes
R2R compatibility	No	Yes	Yes	Yes

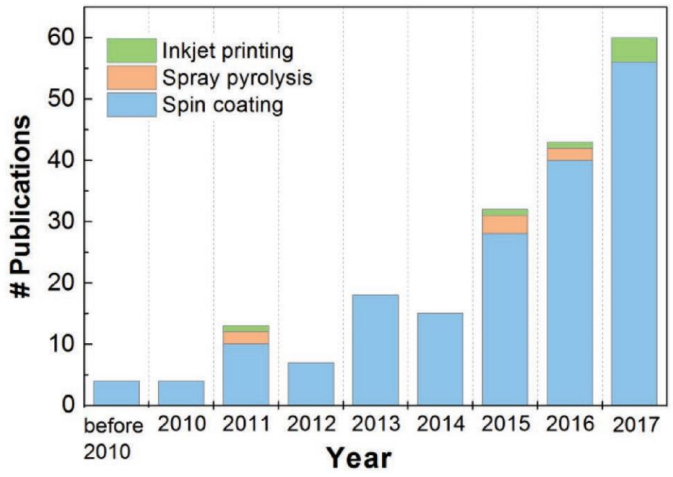

Figure 1-7. The constituent of publications based on different solution-processes, including inkjet printing, spray coating, and spin coating [6].

1.2.5 Solution-processed high-*k* oxides

After understanding the criteria of selecting high-*k* dielectrics (section 1.1) and the importance of solution-process, much effort has been devoted to developing solution-processed high-*k* dielectrics, such as Al_2O_3 [44], HfO_2 [45], ZrO_2 [46], and Ga_2O_3 [47]. Besides, the previously introduced low-temperature processing approaches (alkoxide precursors, chemical combustion, WI route) have been employed to produce high-*k* oxide dielectrics based flexible electronics. Among those promising candidates, Al_2O_3 is one of the most widely studied oxide dielectrics for oxide TFTs with a satisfying large bandgap of 8.8 eV and a relatively low dielectric constant of 9. It has the advantages of abundant in the earth, high breakdown field, good thermal and chemical stability, smooth surface, and excellent interface with oxide semiconductors [44, 48-52]. In 2015, Xu et al. demonstrated a facile and environmentally friendly solution-processed method

for depositing Al_2O_3 dielectrics [44]. This method combined the DI water solvent and metal nitrates precursor. Al_2O_3 fabricated at 300 °C through this method was used as the gate dielectric for solution-processed oxide TFTs. The Al_2O_3 based In_2O_3 and IZO TFT exhibited satisfied mobilities of 57.2 and 10.1 $cm^2V^{-1}s^{-1}$, respectively, as well as 4 V low operation. In 2017, the same group developed a low-temperature aqueous route to fabricate oxide TFTs with Al_2O_3 as dielectric and In_2O_3 and IZO as semiconductors [53]. The Al_2O_3 dielectric exhibited a low leakage current (2.9×10^{-7} Acm^{-2} at 1 $MVcm^{-1}$) and a dielectric constant of 8.6 with annealing temperature <250 °C. The In_2O_3/Al_2O_3 TFTs annealed <250 °C demonstrated high mobilities up to 30.88 cm^2 V^{-1} s^{-1} at a low operating voltage of 4 V.

ZrO_2 constitutes another class of most-studied solution-processed high-*k* oxide dielectrics, which has a large dielectric constant of 25, a wide bandgap of 5.8 eV, relatively low interface trap density, and suitable band alignment [10, 54, 55]. In 2011, Adamopoulos and co-workers demonstrated ZrO_2 dielectric fabricated by spray-coating [56]. The 400 ^oC annealed optimized Li-ZnO/ZrO_2 TFTs had 6 V operation voltage, 10^6 on/off current ratio, negligible hysteresis, and 85 cm^2 V^{-1} s^{-1} mobility. In 2016, Marks et al. successfully fabricated ZrO_2 dielectric through spry-combustion synthesis [57]. The ZrO_2 dielectric showed a low leakage current (10^{-7} A cm^{-2} at 2 MV cm^{-1}) and high areal capacitance (>600 nF cm^{-2}). The solution-processed IZO/ZrO_2 TFTs annealed at 250 and 300 °C exhibited mobilities of 12.1 and 45.5 cm^2 V^{-1} s^{-1}, respectively. In 2016, Shan and co-workers demonstrated the low-temperature fabrication of high-quality

ZrO_2 dielectrics via an aqueous route using zirconium nitrate and DI-water solution [46]. The In_2O_3/ZrO_2 TFTs annealed at 250 °C exhibited high mobility of 10.8 $cm^2 V^{-1} s^{-1}$, a small subthreshold swing of 75 mV dec^{-1}, and an on/off current ratio of 10^6, respectively. The p-type NiO/ZrO_2 TFTs produced at 250 °C exhibited an on/off current ratio of 10^5 and hole mobility of 4.8 $cm^2 V^{-1} s^{-1}$ [46]. By now, solution-processed low-temperature Al_2O_3 and ZrO_2 have been regarded as promising high-k dielectrics and can potentially apply flexible electronics.

1.3 Radiation effects on electronics

1.3.1 Overview

Advanced electronic circuits are essential for computing and controlling electronic devices in space or other radioactive environments [58-60]. They are widely applied in radiation detection sensors, satellite communication systems, nuclear power plants, and medical equipment. In addition, the development of solution-process makes the applications of large area and flexible radiation harsh electronics possible, such as large-area antenna arrays, whole-body-scanning X-ray detectors, and artificial skin on robots designed to operate in space [58]. These applications are unavoidably exposed to space-like radiation, which has a relatively low radiation dose rate at 10^{-4}-10^{-8} Gy/s (Si) [61, 62]. Therefore, electronic devices intended for harsh applications should provide exceptional levels of operational reliability, given that they are mission-critical and safety-critical. As mentioned before, SiO_2 has been the primary gate insulator since

MOS ICs were first developed. At present, the thickness of the SiO_2 gate is extremely thin. McGarrity reported that the gains in gate oxide hardening could be achieved merely by thinning the oxide without special processing [63]. Consequently, the devices with SiO_2 gate oxide have demonstrated excellent radiation hardness. However, the application of high-*k* dielectrics, especially solution-processed high-*k* dielectrics, degrades the radiation hardness of devices [58, 64-68]. The reason is that, with the same EOT, high-*k* dielectrics are much thicker, more defective, and contain a higher percentage of electron traps than SiO_2. Besides, compared to those high-*k* dielectrics fabricated by vacuum methods, solution-processed high-*k* dielectrics are even more thicker, they contain more precursor residual, chemical defect and metal hydroxyl. In this case, electron tunneling possibility is reduced and oxide trap charges may be more significant. However, very few works have reported the radiation response of solution-processed high-*k* dielectrics [58]. Therefore, the charge trapping behavior and long-term reliability of solution-processed microelectronics need to be investigated in detail.

The “radiation effects” are the processes of the interactions between high-energy particles and target materials. Various environments are likely to have a degrading effect on electronic devices and systems: space, nuclear reactors, nuclear weapons, and controlled fusion. In these harsh environments, various radiation sources are associated with different types of high-energy particles, including charged particle, neutron, and photon [69]. This work focused on the total dose effects on the high-*k* dielectrics and devices caused by γ-ray irradiation.

1.3.2 Photon irradiation-induced damage to materials

They are many types of radiating particle, including charged particles (see Chapter 1 Appendix for more information), neutrons (see Chapter 1 Appendix for more information) and photons. Photons are uncharged particles contained in X-rays and γ-rays. γ-ray is a type of electromagnetic radiation and is the product of nuclear reactions. It has greater energy compared to X-ray. Photons mainly interact with the existing electrons in materials. For photons with different energies, the mechanism of interaction with atoms is different, which can be divided into photoelectric effect, Compton scattering, and electron pair generation [70]. The photoelectric effect is related to the emission of photoelectrons. In this case, the energy of the incident photons is completely absorbed by the atom, and photoelectrons are then excited. Compton scattering is the inelastic scattering between photons and electrons. The incident photons transfer a part of their energy to the electrons, but these photons are not completely absorbed and are refracted at an angle. Due to the different refraction angles of photons, the energy transferred to the electrons varies over a wide range. Electron pair generation is the transmission of a photon into a pair of positive and negative electrons when passing through the material. Electron pair generation dominates the radiation effect when the photon energy is larger than 5 MeV.

Generally, radiation effects can be divided into displacement damage (see Chapter 1 Appendix for more information) and ionizing damage. In this work, a Cs^{137} radiation source with 662-keV energy is employed; the main mechanisms investigated are

photoelectric effects and Compton scattering, which belongs to the radiation-induced ionizing damage. Ionizing damage refers to the process that radiation particles pass through the material, interact with the electrons in the material, and transfer their energy to the electrons. If the energy obtained by the electron is more significant than its atom binding energy, the electron will break away from the nucleus and become a free electron; then the atom will be ionized into an ion. In general, for a microelectronic device, radiation induces electron-hole pairs (EHPs) among the material, especially gate oxide [71]. The motions of these radiation-induced EHPs caused by diffusion or applied electrical field could lead to various ionization effects on the device properties.

The effect of ionizing radiation is mainly determined by the energy absorbed by the electrons, regardless of the type of radiation. Therefore, ionizing radiation damage can be measured by the energy absorbed per unit volume of material. The commonly used units are rad or Gray (Gy), where 1 rad = 100 erg/g, 1 Gy = 1 J/kg = 100 rad. For a given dose, the charge released is dependent on the energy absorbed by the material. Therefore, the ionizing dose must specify an absorber, for example, 1 rad (Si), 1rad (SiO_2), 1 rad (GaAs), or the international (Si) unit system, 1 Gy (Si) and so on. According to the time scale of the ionization effect, the ionizing effect can be divided into the signal event effect (see Chapter 1 Appendix for more information) and the total dose effect.

The total dose effect is related to the cumulative dose absorbed during a certain exposure period. This effect becomes significant with the accumulation of radiation

dose. As long as the semiconductor device is exposed to the radiation environment, radiation effects will accumulate throughout the life of the electronic components. Consequently, total dose effect investigation is crucial for long-term applications, such as nuclear power reactor applications, space applications, and accelerator applications. For a MOS device, the total dose effect is mainly caused by the interaction between the gate dielectric and charged particles (low-energy electrons, protons, etc.), X-rays or γ-rays. Many research results have demonstrated that the total dose effect leads to the generation of oxide traps in the dielectric oxide layer and interface traps at the dielectric oxide/semiconductor interface [72-76].

1.3.3 Total dose effects in MOS system

Figure 1-8 demonstrates the schematic energy band diagram of a MOS structure under positive gate bias [77]. The gate oxide is the most sensitive part of a MOS system; when radiation passes through a gate oxide, EHPs are generated. Electrons are much more mobile than holes and are swept out of the oxide in a picosecond or less. It is noticeable that some fraction of radiation-induced EHPs begin to recombine even before the electron escaping [77]. The fraction of EHPs that escape recombination is called the electron-hole yield or charge yield. The holes, which escape initial recombination, are relatively immobile. Under the positive applied electrical field, they will transport towards the oxide/semiconductor interface by hopping through the localized states in the oxide, which causes the short-term recovery of the V_{TH}. As the

holes approach the interface, some fraction will be trapped, forming a positive oxide trapped charge [71]. Meanwhile, the hopping transport could release protons; these protons can also drift to the oxide/semiconductor interface and form interface traps under the applied positive electrical field. The hole and proton transportations are very sensitive to the applied field, temperature, oxide thickness, and oxide processing history [78].

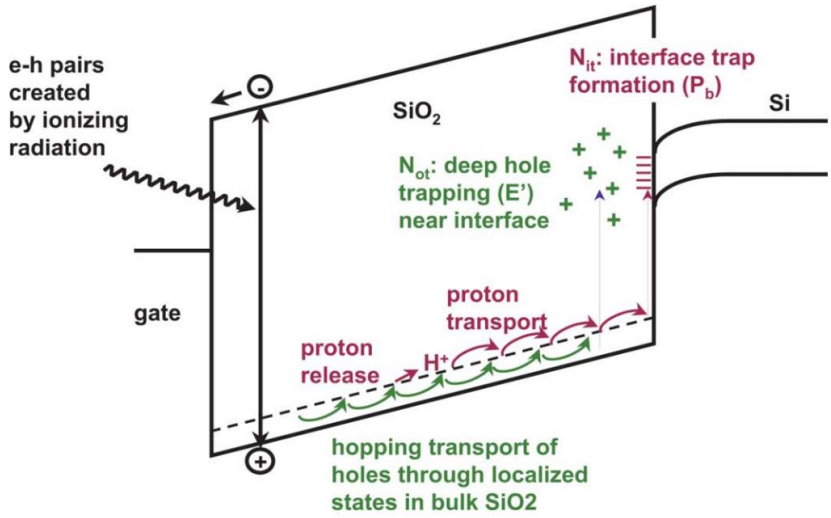

Figure 1-8. Schematic band diagram of a metal-oxide-semiconductor (MOS) capacitor with positive gate bias. Illustrated are the main processes for radiation-induced charge generation [77].

Specifically, total dose effects in MOS devices are mainly caused by the generation of oxide traps among gate oxide and interface traps at the oxide/semiconductor interface.

Oxide traps

Oxide traps are essential for short-time degradation, high dose rate, and thin oxide situation. Oxide traps are generated by holes and protons trapping; they are positive in most situations. The holes come from the radiation-induced EHPs, while protons are

generated during the hopping transport of those radiation-induced holes under the applied electrical field. When the holes and protons approach the oxide/semiconductor interface, some fraction of them will become trapped by the trapping centers, such as oxygen vacancies and lattice mismatch at the surface [79]. The percentage of trapping charges is related to the applied electric field and device fabrication process. Immediately after a hole is trapped in oxides, it begins to be annealed, which means the hole density begins to decrease. Generally, hole annealing is caused by electron tunneling or thermal excitation [80]. At room temperature, electron tunneling dominates the hole annealing process. Electrons tunnel from the substrate into either oxide traps or electron traps associated with trapped holes. The former process removes the tapped charges, and the later process results in a charge-neutral state without removing the tapped holes. Tunnel annealing is strongly dependent on the polarity of the applied electrical field. By reversing the polarity of the voltage bias, electrons can tunnel back into the substrate, and some fraction of the original oxide trapped charges can be restored. Under high temperatures, thermal excitation dominates the hole annealing and causes electrons to be emitted from the oxide valence band into oxide traps. It is noticeable that the hole annealing rate is determined by the device fabrication process, regardless of the radiation source and dose rate.

Interface traps

Interface traps are amphoteric, which is different from oxide traps. They can be positive (below mid-gap), neutral (near mid-gap), or negative (above mid-gap). For

MOS devices based on Si substrate, the generation of radiation-induced interface trap is related to the Si-H bonds at the oxide/semiconductor interface. These Si-H bonds can be broke by radiation-induced proton or suboxide. Furthermore, impure high-*k* atoms of high-*k* oxide-based MOS devices can be the candidate to break the Si-H bonds [74]. When a Si-H bond is broken, a Si is left with an unpassivated dangling bonds as an electrically active defect. Meanwhile, a proton is released and could be trapped in oxide to act as an oxide trap. The breaking of Si-H bonds is called de-passivation of the oxide/semiconductor interface and strongly depends on the bias polarity and the bias environment [81]. The generation rate of interface traps is much slower than that of oxide traps and does not depend on the dose rate [82]. Interface traps annealing requires high temperature and cannot take place at room temperature.

Device properties

Regarding the radiation effects on the MOS capacitor, the shift of C-V curves can be observed. Generally, the shift of flat-band voltage (ΔV_{FB}) is calculated to determine the degradation of the devices. The overall radiation response of a MOS device is separated into the oxide trap response and interface trap response for sensible testing and analysis. Therefore, it is common practice to write as (1.3) [62]:

$$\Delta V_{FB} = \Delta V_{OT} + \Delta V_{IT} \tag{1-3}$$

where ΔV_{OT} and ΔV_{IT} are the C-V shift due to oxide traps and interface traps, respectively. In this situation, it is assumed that the interface traps are net neutral at mid-gap so that the mid-gap voltage shift (ΔV_{mg}) is only related to the generation of

oxide traps [83]. Then the shift due to oxide traps and interface traps can be represented as (1.4) and (1.5) [83]:

$$\Delta V_{OT} = \Delta V_{MG} \tag{1-4}$$

$$\Delta V_{IT} = \Delta V_{FB} - \Delta V_{MG} \tag{1-5}$$

Generally, for a positive charge, ΔV_{FB} is negative; conversely, for a negative charge, ΔV_{FB} is positive. Oxide traps generation induces the parallel shift of both mid-gap and flat band voltages of the C-V curves, while interface traps generation influences the slope of the C-V curve. It is reported that the effects of trapped charges are more significant when they are near the oxide/semiconductor interface [84]. As a result, the investigation of the oxide traps near the oxide/semiconductor interface and interface traps is a focus of this work.

As the thickness of the gate oxide decrease, the radiation-induced leakage current (RILC) becomes serious. RILC is an increase in leakage current that is observed at low-electric fields. It occurs after exposing an ultra-thin gate oxide to relatively high total doses of ionizing radiation [85]. During exposure to ionizing irradiation, neutral electron traps are created in the bulk of the oxide. With a positively applied gate bias, electrons in the silicon conduction band can tunnel first into these neutral electron traps and then escape through the gate electrode. However, in this work, the thickness of gate oxide is relatively large (~ 20 nm), and the dose rate is relatively low (~1×10^{-3} Gy/s (SiO_2)), the effect of RILC is negligible.

1.3.4 In-situ measurement

To characterize the radiation response of a MOS device, conventional off-site methods are widely used. In those methods, the device properties (e.g. C-V, I-V) are measured before radiation to determine the device pristine state [86]. Then the device is exposed to radiation with or without bias-stress at a given dose rate. When the total dose absorbed meets the requirement, the radiation exposure and bias-stress are interrupted, the device is removed from the radiation environment. Finally, the device properties after radiation exposure are measured and analyzed compared to the per-radiation measured results. The disadvantage of these conventional off-site methods is that the ineluctable interruption of irradiation can cause a rapid recovery of ΔV_{FB}, which leads to an underestimation of the degradation caused by radiation-induced charge trapping/de-trapping. Consequently, a real-time on-site technique has been introduced to fully characterize radiation-induced degradation [87]. There are two advantages of this real-time on-site technique. One is the bias-stress gate voltage that exists during the radiation exposure. Another one is that radiation exposure and bias-stress are not interrupted during the whole characterization process. In this work, the real-time on-site measure technique is employed to characterize the radiation response of MOS capacitor devices.

1.4 Objectives of the thesis

To investigate the fabrication and reliability of solution-processed high-*k* dielectrics, this work contains three main chapters.

In Chapter 3, an eco-friendly low-temperature solution process route to fabricate high-*k* thin films with high quality and stability was explored firstly. By using water as precursor solution and nitrate salt as the precursor, water-induced (WI) AlO_x dielectric with satisfied thin film quality and BS stability were successfully fabricated at 300 ºC. Then the total ionizing dose response of Metal-oxide-semiconductor capacitors (MOSCAPs) based on 300 ºC annealed AlO_x gate dielectrics were analyzed through in-situ measurements. During the in-situ measurements, the bias-stress and radiation existed at the same time. Furthermore, the irradiation was not interrupted during the measurements.

In Chapter 4, to explore a practicable and effective method to improve the bias-stress and biased-radiation stress stability of solution-processed high-*k* dielectrics. H_2O_2 was employed in the precursor solution as a strong oxidizer. To verify the radiation effect on the charge transportation and bond-breaking behaviors of solution-processed MOSCAPs investigate in Chapter 3, the γ-ray radiation was substituted by LED light illumination to reduce the incident particle energy. Through the precise characterization of in-situ measurements, the degradation induced by high-energy γ-ray radiation could be further analyzed.

In Chapter 5, The effect of La concentration in the ZrO_2 dielectric on the thin film

stability, such as bias-stress stability, ambient air stability and radiation hardness, were explored. Furthermore, the applications of WI ZrLaO thin films in TFT devices and inverter were explored. At last, the radiation hardness of ZrLaO based WI InO_x/ZrLaO TFT were investigated.

1.5 Appendix

Alkoxide precursors

In 2010, Sirringhaus et al. employed organic-inorganic hybrid metal alkoxide as precursors, which enabled the in-situ hydrolysis at the film surface to achieve an oxide framework at low temperature. The indium-zinc-oxide (IZO) TFT fabricated at 230 ºC through this method demonstrated high mobility up to 8 $cm^2 V^{-1} s^{-1}$, along with ~10^6 I_{on}/I_{off} ratio, small hysteresis, small SS and good BS stability [38]. However, metal alkoxide precursors are unstable and require a complicated synthesis process.

Chemical combustion methods

Another approach to reduce processing temperature is exothermic combustion reaction inside the as-deposited films. The combustion concept for fabricating solution-processed oxide TFTs was first proposed by Marks et al [25]. By incorporating nitrate as an oxidizer and acetylacetone/urea as fuel, the localized exothermic reactions provided sufficient internal thermal energy to decompose the residual impurities and form a metal oxide framework at low temperature (<200 ºC). Subsequently, the same group reported a low-temperature processing named spray combustion synthesis to

fabricate oxide films [88]. The internal combustion heat and spray successfully suppressed gaseous byproducts. However, the violent reactions of combustion synthesis lead to the generation of pinholes in the film, which could act as defects and increase the leakage current.

Charged particles

Charged particles include proton, helium, positron, and electron, they interact with the outer electrons of atoms in the materials through coulomb force and seldom interact with the nucleus. The damage caused by charged particles can be described by linear energy transfer (LET), which represents the energy deposited by an incident particle along the unit length of its incident track. This value is related to the incident particle type and energy, as well as material properties. The greater the energy deposited by the particles per unit length, the greater the damage dealt with the material. However, it should be pointed out that the radiation damage effect of semiconductor devices is very complicated. At present, it has been reported that for similar LET values, the damage caused by different particles to semiconductor devices may be quite different [89].

Neutrons

Neutrons are uncharged particles and they have strong penetrability. They can even penetrate the material for a few centimeters without interacting with atoms in the material. In general, the interaction between the neutrons and electrons of the target atom is negligible, while the interaction between the neutrons and the nuclei is dominating [90]. The interaction can be divided into two types, one is the elastic

collision and another one is the nuclear reaction. During an elastic collision, the neutron can completely knock the target nucleus away from its location, resulting in a recoil ion. This recoil ion continues to deposit energy to the material. For nuclear reaction, neutrons are absorbed by the target nucleus and become an unstable isotope. This characteristic of neutron radiation can be applied to dope semiconductors.

Displacement damage

Displacement damage refers to that the radiation particles destroy the material lattice structure and cause the atoms to leave their local positions, which could form atom vacancies and interstitial atoms. These micro-damage reactions generate one or more energy levels in the energy band. At the same time, the recoil ions formed by the incident particles may continue to generate new recoil ions in the material. As recoil ions continue to transfer their energy to the material, their speed decreases accordingly. When the speed of recoil ions is reduced to a certain degree, they could cause cluster damage and result in local decrystallizatoin among the materials [91]. The degradation of semiconductor material properties caused by displacement damage includes reduced carrier density, increased resistivity, reduced carrier lifetime, and mobility. For a MOS device, displacement damage causes a reduction in minority carrier lifetime in the substrate. Since the properties of most MOS devices are not significantly affected by minority carrier lifetime, they are relatively insensitive to displacement damage [91].

Single event effect

Single event effect is a physical phenomenon proposed during the research of satellite failure in the 1970s. It is caused by the energy deposited by a single incident particle, regardless of the total dose absorbed or dose rate. When a particle with relatively high energy bombards the device circuit, it causes a strong ionization and forms a small region of plasma inside the device, then the logic state of the device is inverted, resulting in single-particle inversion. On the other hand, the generation of EHPs causes the parasitic transistor to be turned on, which leads to a single-particle latch-up. If the current through the device is large enough when a single particle latch is generated, the device can be even burned. It is reported that single event effects could only pose significant problems to CMOS devices at a high dose rate [92]. In consequence, total dose effects on the oxide layer are of the major concern for MOS devices under low dose rate irradiation exposure.

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Chapter 2:Experimental Details

2.1 Physical characterization

2.1.1 Atomic force microscope (AFM)

AFM is the technique mainly used to observe the surface morphology of the sample. It can measure the properties of elasticity, plasticity, hardness, adhesion, and friction of the surface. This method utilizes the interaction force between the tip atom and surface atom. During the scanning, the Van der Waals' force between the tip and the sample is fixed and the morphology change of the sample could be recorded and analyzed.

In this work, the AlO_x thin film morphologies were characterized by AFM in tapping mode. The surface roughness of the samples was quantitatively determined by the root-mean-squared roughness (RMS), defined as equation (2-1):

$$R_{rms} = \sqrt{\frac{\sum_{n=1}^{N}(z_n - \bar{z})^2}{N-1}} \quad (2\text{-}1)$$

where z_n is the measured height, $\bar{z}$ is the average height of the sample and N is the number of measurements.

2.1.2 X-ray diffraction (XRD)

XRD is an important technique for the determination of crystal structure. Besides, it is an effective method for analyzing phase, grain size, and stress state. During the

measurement, a beam of electrons is accelerated at high pressure to bombard the metal target. The inner shell electrons of the target atom are excited by the high-energy electrons. Meanwhile, the electron transition occurs at the outer orbit, and X-rays are emitted. The structural and crystal properties of the sample are obtained by analyzing the emitted X-rays.

To carry out XRD in this work, a nickel-filtered Cu Kα radiation source and a diffractometer with a Cu Kα radiation source were used. The measuring range of 2θ is 20-60 degrees.

2.1.3 X-ray photoelectron spectroscopy (XPS)

XPS is mainly used to analyze the element composition, chemical state, valence state, electron cloud, and energy level structure of the sample. XPS technology has negligible damage to the samples and is basically nondestructive. Future more, it can detect almost all elements with high sensitivity, except H and He. This technique applies X-ray as the incident source to irradiate the sample, excite and ionize the inner shell electrons of the atom. The variation of the photoelectron is monitored to obtain the element composition and structure information of the sample.

In this work, XPS is employed to analyze the concentration of M-O, M-OH, and V_o exist in the solution-processed dielectric thin films. Due to an impurity in the carbon of the samples, the C 1s peak in the spectra at 284.5 eV was used to calibrate charging effects during measurements [1]. All spectra deconvolution was performed by Shirley

background subtraction using a Voigt function convoluting Gaussian and Lorentzian functions.

2.1.4 Thermogravimetric analysis - differential scanning calorimetry (TGA-DSC)

TGA is a kind of method to investigate the relationship between the weight of the sample powder/solution and the temperature. With a program-controlled increasing temperature, the weight loss of the sample powder/solution is recorded to analyze the variation of the characteristic at a certain temperature. In solution-process, the dissolution, hydrolysis, and thermal decomposition of precursor powder have a great influence on the formation of oxide thin films. TGA could be helpful to understand the phase transition during the transformation from precursor materials to metal oxides.

In this work, to investigate the thermal behavior of the precursor powder, the precursor solution was dried at 100 ºC for 1 h to acquire precursor powder. Then the precursor was heated from 20 ºC to 500 ºC with a heating rate of 10 ºC/min, monitored by TGA-DSC.

2.1.5 Fourier transform infrared spectroscopy (FT-IR)

FT-IR is a sensitive method to investigate the chemical composition of the sample. The molecules in the sample absorb a certain spectrum when they vibrate and an absorption spectrum is generated. The chemical bonds and groups in the film can be determined by analyzing the absorption spectrum.

In this work, the chemical characteristics of AlO_x thin films were investigated by FT-IR, where the wave numbers were in the range of 400-4000 cm^{-2}.

2.1.6 Ellipsometry

Ellipsometry is an efficient method for determining optical constants, roughness, and thickness of dielectrics. Briefly, Fourier-modulated radiation is emitted from an interferometer and linearly polarized by a polarizer. When the radiation falls onto the sample with a specific incidence-angle, two reflection-lights will be generated at the surface of dielectrics and dielectric/substrate interface. These two reflection-lights are then transmitted and passed to the second polarizer, then fall into the detector. The thickness of the dielectrics can be calculated from the phase shift of the two reflection-lights [2, 3].

The spectroscopic ellipsometry measurements in this study were carried out by an ellipsometer with an incident angle of 65 ° to measure the physical thickness of the deposited thin films. The wavelength was from 300 nm to 800 nm with a step of 25 nm.

2.2 Electrical characterization

All electrical measurements were carried out in the dark at room temperature.

2.2.1 MOS and MIM devices

Current-Voltage (I-V)

At present, the decreasing thickness of the dielectric layer leads to the increasing of leak current, which could degrade the device performances severely. High-*k* materials are applied to prevent tunnel behavior and suppress the leakage current. Consequently, I-V measurement is an important method to characterize the dielectric layer of MOS and MIM device, since devices with various gate dielectrics are expected to exhibited different leakage behaviors. In this study, I-V measurements were performed by an Agilent B1500A semiconductor device analyzer before the biased radiation exposure to evaluate the gate leakage behavior of AlO_x MOSCAPs and ZrLaO MIM devices.

Capacitance-frequency (C-*f*)

To characterize the frequency dependence of the deposited high-*k* dielectric thin film. C-f measurements were carried out using a HP 4284 precision LCR meter, where the frequency varied from 1 k-1 MHz.

Capacitance-voltage (C-V)

C-V measurement is an important method to investigate the properties of the MOS device, especially the oxide/semiconductor interface. When carrying out C-V measurement, a small signal voltage is applied on the device gate, and the small-signal current flowed through the capacitor is monitored. Then the measured capacitance (C_m) of the MOS device is calculated by equation (2-2):

$$C_m = \frac{i_{ac}}{dV_{ac}/dt} \tag{2-2}$$

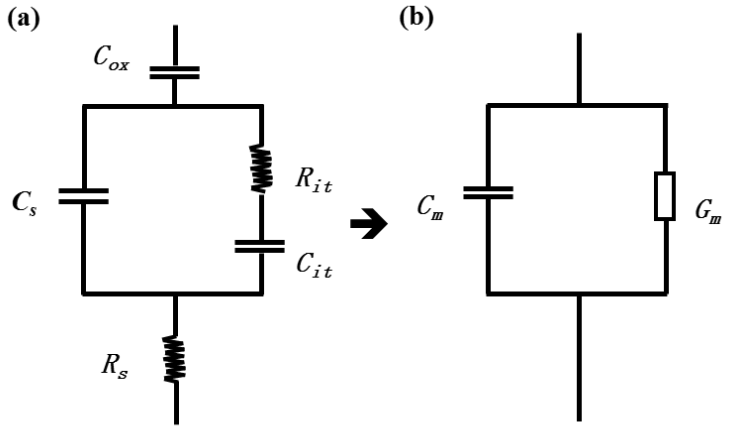

Figure 2-1. Equivalent circuits of MOSCAPs measured in parallel mode with **(a)** actual measurement components and **(b)** equivalent circuit components [4].

where i_{ac} is small-signal current, dV_{ac} is the variation of the small gate signal voltage, and dt is the variation of measuring time.

In this work, a HP 4284A precision LCR meter was used to carry out C-V measurements at 1MHz. Two measurement models can be used, parallel model and series model. As the MOSCAPs fabricated have relatively high resistance (>1 MΩ), and the parallel mode was selected accordingly. The equivalent circuits of the MOSCAP under C-V measurements in parallel mode are shown in Figure 2-1. Figure 2-1 (a) illustrates the actual existing components, while Figure 2-1 (b) exhibits the equivalent circuit contains the measured capacitance (C_m) and conductance (G_m) [5, 6]. C_{ox} is the capacitance of the oxide layer; C_s is the space charge capacitance or depletion capacitance of Si semiconductor substrate, R_s is the series resistance, R_{it} and C_{it} are the resistance and the capacitance related to the interface traps at oxide/substrate interface, respectively. Therefore, the measured capacitance C_m is not only ideally determined by

C_{ox} and C_s but also affected by the interface traps. Meanwhile, the maximum capacitance (accumulation region) in measured C-V curves cannot fully represent C_{ox}. However, as the other components have very limited effects on the C-V curves of MOSCAPs at the accumulation region, the measured maximum capacitance has been served as C_{ox} in most studies [7-9].

Bias-stress (BS)

When MOS devices are operated with continuous applied electrical biases over a prolonged time, the bias stresses can affect the overall device performances. This phenomenon is known as the bias-stress driven instability of MOS devices. Prolonged device operation can cause severe performance degradation, which commonly manifests as a shift in the V_{FB}, a distortion in the shape of the C-V curve, and/or the increased C-V hysteresis. As a result, the BS stability investigation of the MOS devices is a crucial issue for their application of modern electronics.

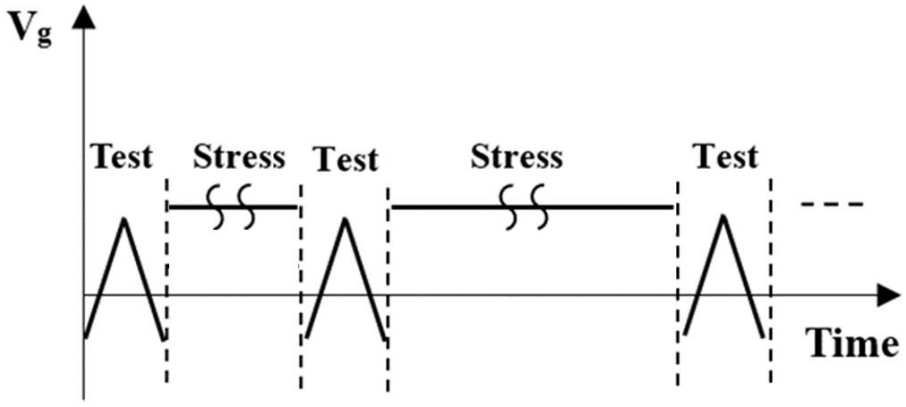

Figure 2-2. Gate sweeping voltage waveform for bias-stress (BS) stability measurement.

BS stability of the AlO_x MOSCAPs was investigated by a HP 4284A precision LCR meter controlled by a computer via the GPIB module. The gate sweeping voltage waveform of the BS measurement is shown in Figure 2-2. During the measurement, a constant voltage bias was applied on the gate of the device. In order to determine the degradation caused by voltage bias-stress, C-V curves were measured at regular points in time of $10^{1/3}$ s, $10^{2/3}$ s, $10^{3/3}$ s, $10^{4/3}$ s, $10^{5/3}$ s, etc. during the voltage bias-stress to allow extraction of the V_{FB} and mid-gap voltage (V_{mg}) .

V_{FB} is the voltage applied on the gate of MOS capacitors when the energy bands of the semiconductor are not bended. V_{FB} is determined from the C-V curves according to the C_{FB}, C_{FB} is calculated according to formula (2-3) in this work:

$$C_{FB} = \frac{C_i}{\frac{C_i}{\sqrt{\frac{\varepsilon_s \varepsilon_0 q^2}{kT} N_D}} + 1} \tag{2-3}$$

where C_i is the oxide areal capacitance, ε_s is the dielectric constant of Si substrate, ε_0 is vacuum permittivity, q is electronic charge, k is Boltzmann constant, T is the absolute temperature and N_D is the doping concentration of Si substrate. It is known that the metal semiconductor work function difference, oxide, and interface traps/charges would not affect the value C_{FB}. As a result, for a given C_{FB}, V_{FB} can be determined from the measured C-V curves. The calculated ideal C_{FB} are listed in Table 2-1.

Table 2-1: The calculated C_{FB} of different AlO_x devices.

Devices	**C_{FB} (pF)**
150-AlO_x	40
200-AlO_x	38
250-AlO_x	36
300-AlO_x	33
0 M H_2O_2-AlO_x	47
2.5 M H_2O_2-AlO_x	48
5.0 M H_2O_2-AlO_x	49
7.5 M H_2O_2-AlO_x	50
10 M H_2O_2-AlO_x	49.5

V_{mg} is the voltage applied on the gate of on the MOS capacitor when the E_i of the semiconductor is equal to its E_F at the dielectric/semiconductor interface. To determine the actual V_{mg}, ideal V_{mg} and ideal high-frequency C-V curve of MOS capacitor need to be calculated first. Then the mid-gap capacitance (C_{mg}) can be determined from the ideal C-V curve for a given ideal V_{mg}. At last, actual V_{mg} can be determined from the measured C-V curves according to ideal C_{mg}.

To determine the ideal V_{mg}, the gate voltage applied on the MOS capacitor can be defined as:

$$V_G = V_{ox} + V_s + V_{ms} \tag{2-4}$$

where V_{ox} is the voltage across on the oxide layer, V_s is the surface potential of the semiconductor and V_{ms} is the metal-semiconductor work function difference. When

V_G=V_{mg}, for the ideal situation (ignore the gate oxide trapped charges), the surface charge area of semiconductor is depleted, and the charge quantity on the metal gate (Q_G) is equal to the charge quantity of depletion layer (Q_{depl}), then V_{ox} can be calculated through:

$$V_{ox} = \frac{Q_G}{C_{ox}} = \frac{Q_{depl}}{C_{ox}} \tag{2-5}$$

Where C_{ox} is the areal capacitance of the dielectric layer. Q_{depl} is calculated by:

$$Q_{depl} = qN_D x_d \tag{2-6}$$

where q is electronic charge, N_D=1.53×10^{15} cm^{-3} is the doping concentration of lightly doped Si substrate with resistance of 2-4 Ω/cm, x_d is the thickness of the depletion layer and can be calculated from:

$$x_d = \sqrt{\frac{2\varepsilon_s\varepsilon_0 V_s}{qN_D}} \tag{2-7}$$

ε_s is the dielectric constant of Si substrate, ε_0 is the vacuum permittivity. When the semiconductor is under mid-gap situation, the surface potential V_s of the semiconductor can be calculated by:

$$V_s = E_i - E_F = \frac{kT}{q} In(\frac{N_D}{n_i}) \tag{2-8}$$

Afterwards, the x_d and Q_{depl} can be determined, and equation) can be written as:

$$V_{ox} = \frac{Q_{depl}}{C_{ox}} = \frac{\sqrt{2\varepsilon_s\varepsilon_0 V_s qN_D}}{C_{ox}} \tag{2-9}$$

V_{ms} is calculated through equation:

$$V_{ms} = \frac{W_m - W_s}{q} \tag{2-10}$$

where W_m and W_s are the work function of the metal Al and semiconductor Si, respectively. Then the ideal V_{mg} can be calculated according to equations)-(2-10), in this work, the value of ideal V_{mg} is -0.42 V and -0.43 V for the 7.5 M H_2O_2-AlO_x and 0 M H_2O_2-AlO_x MOS devices, respectively.

After determining the ideal V_{mg}, the ideal high frequency C-V curves needs to be calculated. As the mid-gap situation occurs between the depletion and inversion state of semiconductor, only the C-V curves of depletion and inversion region under high frequency needs to be determined, which can be calculated through equation:

$$\mathrm{C} = \frac{C_i A}{\sqrt{1 + \frac{2\varepsilon_{ox}^2 \varepsilon_0 V_G}{\varepsilon_s q N_D t_{ox}^2}}} \tag{2-11}$$

where A is the electrode area, ε_{ox} is the dielectric constant of gate oxide, ε_s is the dielectric constant of Si substrate, N_D is the doping concentration of Si substrate, V_G is the gate voltage and t_{ox} is the thickness of gate oxide. It is known that for the real situation, the metal semiconductor work function difference, oxide, and interface traps/charges would not affect the value C_{mg}. Taking H_2O_2 AlO_x MOSCAPs as an example, the calculated ideal high-frequency C-V curves of AlO_x MOSCAPs working in depletion and inversion region is demonstrated in Figure 2-3, and the ideal C_{mg} can be determined to be around 12.2 pF. At last, the real V_{mg} can be read from the measured C-V curves of all MOS devices according to the ideal C_{mg}. The calculated ideal V_{mg} for different devices are listed in Table 2-2.

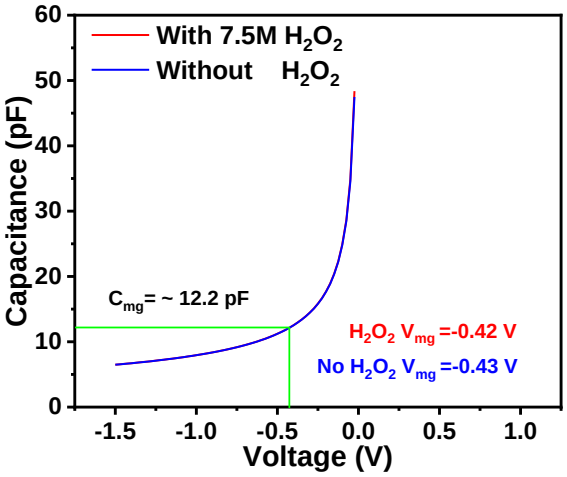

Figure 2-3. The calculated ideal C-V curves in depletion and inversion region of AlO_x MOSCAPs.

Table 2-2. The calculated V_{mg} of different AlO_x devices.

Devices	**V_{mg} (V)**
150-AlO_x	-0.46
200-AlO_x	-0.47
250-AlO_x	-0.48
300-AlO_x	-0.50
0 M H_2O_2-AlO_x	-0.43
2.5 M H_2O_2-AlO_x	-0.42
5.0 M H_2O_2-AlO_x	-0.42
7.5 M H_2O_2-AlO_x	-0.42
10 M H_2O_2-AlO_x	-0.42

Biased radiation stress (BRS)

To investigate the BRS stability of the AlO_x MOSCAPs, a novel real-time and on-site radiation response testing system was applied [10]. As shown in Figure 2-4, the

probe station platform consists of a platform with an x-y adjustable stage, an optical microscope equipped with a digital camera, an on-wafer probe mounted on a precision positioner, a testing sample loading chuck mounted on a rail, and a lead container to keep the γ-ray radiation source at the center of the platform [10]. Both the optical microscope and the probe positioner are mounted on robotic arms with the program-control PC placed outside the probe station. The robotic arms can move vertically along the z-axis and horizontally along the y-axis while the lead container mounted on a stage can move in a horizontal plane along the x-axis and the y-axis [10]. When carrying out the BRS stability measurement, constant voltage bias stress was applied on the gate under radiation exposure. A 662-keV Cs^{137} γ-ray radiation source was used, the stress time was up to 10^5 s and the total dose was up to 92 Gy (SiO_2). During the BRS measurement, the MOS devices suffered from γ-ray radiation and gate voltage bias-stress at the same time. To observe the degradation of the devices' properties, C-V curves were measured at regular points in time of $10^{1/3}$ s, $10^{2/3}$ s, $10^{3/3}$ s, $10^{4/3}$ s, $10^{5/3}$ s, etc. to allow extraction of the V_{FB}. The radiation exposure was not interrupted during the C-V measurements. It is noticeable that the voltage waveform during BRS is the same as that used in BS stability measurement, as shown in Figure 2-2. The same interval of the C-V measurement during the BS and BRS enables the comparison of the BS degradation with BRS degradation.

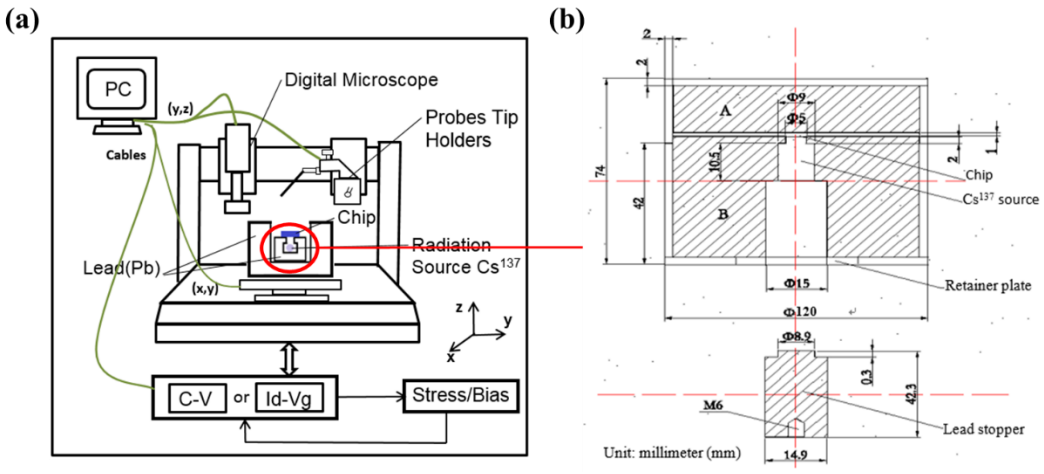

Figure 2-4. **(a)** Real-time and on-site measurement system of γ-ray radiation. **(b)** Schematic diagram of the lead container with a Cs^{137} γ-ray radiation source in the ionizing radiation probe station system [10].

Biased illumination stress (BIS)

Similar to BRS measurement, to investigate the BIS of AlOx MOSCAPs, all devices were measured under a white light source with an illuminance of ~1000 LUX at room temperature, while different bias-voltages were applied on the gate. The stress time was up to 46000 s. During BIS measurement, the MOS devices suffered from white light exposure and gate voltage bias-stress at the same time. To observe the degradation of the devices' properties, C-V curves were measured at regular points in time of $10^{1/3}$ s, $10^{2/3}$ s, $10^{3/3}$ s, $10^{4/3}$ s, $10^{5/3}$ s, etc. to allow extraction of the V_{FB}. The interval of the C-V measurement during the BS and BIS is the same as well to compare the BS degradation with BIS degradation.

2.2.2 TFT devices

Field-effect mobility (μ_{FE})

μ represents the average drifting speed of carriers under the unit electric field, which can be expressed as (2-12):

$$\mu = \frac{V_d}{E} \tag{2-12}$$

where E is the electrical field, V_d is the average drifting speed of carriers under the electrical field. For a semiconductor, the relationship of its conductivity (σ) and mobility is:

$$\sigma = nq\mu \tag{2-13}$$

where n is the carrier concentration and q is the electron charge. For a TFT device, the high μ_{FE} leads to large on current and fast switching speed.

If $V_{GS}>V_{TH}$ and $V_{DS} \leq V_{GS}-V_{TH}$, the device is working in a linear region, I_{DS} increases linearly with increasing V_{DS}, the linear mobility (μ_{lin}) can be calculated by (2-14):

$$\mu_{lin} = \frac{L}{WC_iV_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} \tag{2-14}$$

If $V_{GS}>V_{TH}$ and $V_{DS} \geq V_{GS}-V_{TH}$, the device is working in a saturation region, I_{DS} is saturated and remains constant with increasing V_{DS}, the saturation mobility (μ_{sat}) can be calculated by (2-15):

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \tag{2-15}$$

In this work, the μ_{sat} is calculated to estimate the device properties.

Threshold voltage (V_{TH}) and turn-on voltage (V_{on})

V_{TH} of a TFT is the voltage at the intersection of the linear part of the $I_{DS}^{1/2}$-V_{GS} curve and the V_{GS} axis; V_{on} is the V_{GS} voltage when I_{DS} in the I_{DS}-V_{GS} curve starts to increase rapidly. V_{TH} and V_{on} both represent the voltage node when the device transitions from an off state to an on state. In general, the measured $I_{DS}^{1/2}$-V_{GS} curve of a TFT is not completely linear, and the fitted V_{TH} is mainly used to calculate the μ_{FE}. In oxide TFT, V_{on} accurately describes the transition voltage when a device transforms from an off state to an on state, and can be used to determine the type of a TFT device. If V_{on}>0 V, the TFT is enhanced. The carrier concentration of the channel layer is low without applying voltage, and a positive gate voltage is necessary to induce more carriers to form a conductive channel; if V_{on}<0 V, the TFT is depleted, and the carrier concentration in the channel without V_{GS} is high enough to enable the current between the source and drain when a V_{DS} is applied. To turn off the device, a negative V_{GS} is required to deplete the carrier concentration in the channel. The value of V_{on} is sensitive to the inherent properties of materials, the higher the carrier concentration is, the more negative V_{on} is acquired. In addition, the material type, layer thickness, dielectric oxide trap density, semiconductor/dielectric interface quality, and electrode work function could affect the value of V_{on}.

On current (I_{on})/ off current (I_{off}) ratio

The ratio of on current (I_{on}) and off current (I_{off}) is called I_{on}/I_{off}. The value of I_{off} determines the turn off ability and the minimum power consumption of a TFT. I_{off} is

related to the device dimension, channel material, and dielectric material. The value of I_{on} determines the driving ability of a TFT, large I_{on} correspond to strong driving ability. Generally, the commercial application of TFT in flat panel display requires $I_{on}/I_{off} > 10^5$, $I_{off} < 10^{-12}$ A. The optimized oxide TFT can meet these requirements, which is one of the reasons that TFT can be applied to flat panel display.

Subthreshold swing (SS)

SS can be ascertained by the V_{GS} required to increase the I_{DS} by 1 decade when the device is turned on under certain V_{GS} and V_{DS}. The unit of SS is V/decade and the value of SS determines the ability of the gate voltage to control the carriers in the semiconductor. Large SS leads to weak ability to control the carriers and vice versa. The value of SS is related to the areal capacitance of the dielectric layer, the dielectric oxide trap density, and the semiconductor/dielectric interface trap density. In addition, SS can be utilized to estimate the interface trap density (D_{it}) at the semiconductor/dielectric interface through (2-16):

$$SS = \frac{kTIn(10)}{q}\left(1 + \frac{q}{C_i}D_{it}\right) \tag{2-16}$$

where q represents electron charge, k represents the Boltzmann constant, and C_i represents the areal capacitance of the dielectric layer.

Hysteresis

During the bidirectional sweep of TFT transfer characteristic measurement, due to the mobile ions, structural defects, and oxide traps (e.g. oxygen vacancy) and dielectric/semiconductor interface traps (e.g. dangling bonds) among the device, the

I_{DS}-V_{GS} curves measured from forward sweep and revere sweep could be different [11]. The difference between two I_{DS}-V_{GS} curves is called the hysteresis of a TFT and the hysteresis is calculated by the difference of V_{GS} took from two transfer curves under the same I_{DS}. If there exists electron trapping in the dielectric layer of the device channel, the loop of transfer curves is clockwise. On the other hand, the mobile ions among oxide bulk could lead to a counterclockwise loop of transfer curves. Hysteresis is undesired because it indicates that the TFT device has defects or water/oxygen adsorption.

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Chapter 3: Aqueous solution-processed AlO_x dielectrics and their biased radiation response investigated by an on-site technique

3.1 Introduction

To date, metal-oxide TFTs have attracted considerable attention for next-generation display technology due to their high optical transparency, excellent charge transport characteristics, good chemical stability, and high mechanical tolerance [1-7]. Compared to traditional vacuum thin film deposition methods, solution-processes enable the fabrication of larger area flexible metal-oxide TFTs due to advantages of simplicity, low-cost, and high throughput. Over the past decade, solution-processed thin film deposition techniques for oxide materials have been well developed, including dip-coating, spin-coating, and inkjet-printing [8-15]. In addition, solution-processed high-*k* dielectrics such as Al_2O_3, ZrO_2, La_2O_3, and HfO_2 in TFTs have been utilized to achieve low operation voltage and gate leakage current [2, 9-11, 15-24]. Among the various high-*k* dielectrics, Al_2O_3 is considered to be an excellent candidate due to its high breakdown field, good thermal and chemical stability, relatively high dielectric constant, smooth surface, and amorphous structure under typical processing conditions [1, 11, 20, 22, 25, 26]. Most of the solution-processed AlO_x thin films are currently fabricated by toxic organic precursor solvents such as 2-methoxyethanol and acetonitrile. These precursor solvents could induce potential

environmental damage within the processing procedures. Since water can be implemented as a suitable precursor solution, aqueous solution-processed AlO_x dielectric could be a promising alternative candidate for the application in eco-friendly, low-cost, and low power consumption TFT devices [1, 11, 18, 25].

Furthermore, solution-processed oxide TFTs are crucial to enable large-area electronics in radiation harsh environments, such as whole-body-scanning X-ray detectors and large-area antenna arrays [27]. Only a few studies have addressed radiation damage in solution-processed high-*k* dielectrics for TFT applications [27]. Typically, ionizing radiation can generate bulk oxide traps and interface traps near the oxide/semiconductor interface, which cause device degradation [28]. Besides, the applied voltage bias-stress on TFT devices will enhance the motion, reaction, and trapping of charges at or near the oxide/semiconductor interface [29]. Therefore, the long-term reliability of solution-processed devices under BRS needs to be investigated. The electrical characteristics of devices have been evaluated before and after irradiation via the conventional off-site radiation response method. The ineluctable interruption of irradiation can cause a rapid recovery of the V_{FB} shift, which leads to an underestimation of the degradation caused by charge trapping/de-trapping. Consequently, on-site measurements have been introduced to fully characterize radiation-induced degradation. There has been limited research reported on the γ-ray radiation response of solution-processed high-*k* dielectrics by on-site techniques.

In this chapter, the effect of annealing temperature in the range 150-300 ºC on the physical and chemical properties of solution-processed AlO_x thin films was investigated by spectroscopic ellipsometry, TGA-DSC, AFM, XRD, and FT-IR. In order to investigate the electrical properties comprehensively, AlO_x thin films were integrated

into MOS capacitors. C-*f*, C-V, J_{leak}-V, and ΔV_{FB} measurements were carried out. Furthermore, BS and BRS stabilities of 300 ^{o}C fabricated AlO_x were systemically investigated by an on-site technique with stress time up to 100000s and total dose up to 92 Gy (SiO_2).

3.2 Experimental details

The fabrication process of the AlO_x MOSCAP is shown in Figure 3-1. To prepare the precursor solution, aluminum nitrate hydrate ($Al(NO_3)_3 \cdot xH_2O$) was dissolved in water to produce a colorless and clear solution with 2.5 M molar concentration. The solution was stirred in an ultrasonic bath for 2 h to ensure the precursor was fully dissolved since the nitrate salts have excellent water solubility. Then the solution was filtered by a 0.45 μm polyethersulfone (PES) syringe filter before spin coating.

To prepare the substrates for solution-processed AlO_x, single-crystal lightly doped N-type silicon wafers (orientation: 100, doping concentration: ~10^{15} cm^{-3}, resistivity: 2-4 Ω·cm) were dipped in 2 % HF aqueous solution for 60 s to remove the native oxide and then dried by N_2. Subsequently, the Si substrates were exposed under air plasma for 15 mins to increase their hydrophilia. After the preparation of Si substrates, the precursor solution was spin-coated on the processed substrate at 4500 rpm for 40 s and then annealed on the hot plate at temperatures in the range of 150-300 ^{o}C for 1 h. Finally, 300 nm thick Al top and bottom electrodes were deposited through

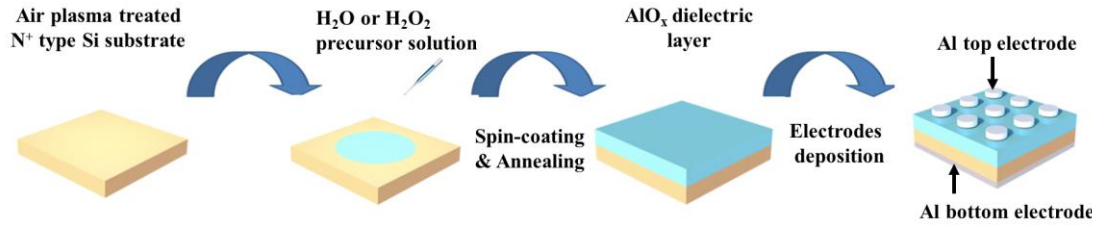

Figure 3-1. The fabrication process of solution-processed AlO_x MOSCAPs.

shadow masks by e-beam evaporation. The circular top electrode had a diameter of 0.3 mm.

To fabricate Al_2O_3 MOSCAPs through ALD, single crystal lightly doped N-type silicon wafers (orientation: 100, doping concentration: ~10^{15} cm^{-3}, resistivity: 2-4 Ω·cm) were selected as the substrate. Before depositing Al_2O_3 thin films on the substrate, the Si wafers were firstly subjected to the standard Radio Corporation of America (RCA) cleaning procedures to remove the native oxide, organic and metallic contamination, as shown in Figure 3-2 [30, 31]. Afterward, the wafers were dipped in diluted hydrofluoric acid solution (2% HF) for 60 s to remove native oxides and oxides created during the RCA clean procedure and then dried by nitrogen gas (N_2). After the cleaning of Si wafers, Al_2O_3 thin films were deposited by ALD. TMA ($Al(CH_3)_3$) was chosen as the precursor and H_2O was selected as oxidant. During the fabrication process, the temperature of the Al_2O_3 precursor and ALD chamber was 100 °C. The total cycle number was 500 ALD cycles with the following sequence: water / purge / precursor / purge (30 ms / 25 s / 150 ms / 25 s). After the deposition of Al_2O_3 thin film, 300 nm

thick Al top and bottom electrodes were deposited by e-beam evaporation, where the circular top electrodes had a diameter of 0.3 mm.

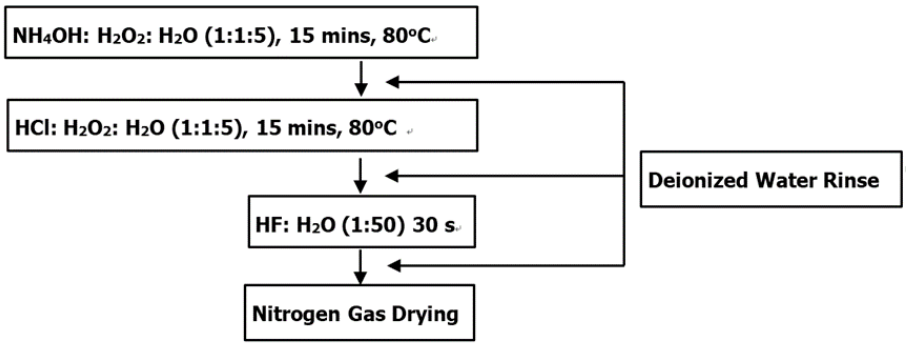

Figure 3-2. Flow chart of Radio Corporation of America (RCA) clean procedures and post-HF treatment for Si wafers. Deionized (DI) water rinse was performed after each procedure to remove the remained solutions on the Si surface.

3.3 The annealing temperature effects on the AlO_x thin film properties

Figure 3-3 displays the thermal behavior of AlO_x precursor powder. The measurement temperature increased from 20 °C to 500 °C with a heating rate of 10 ^oC/min. It can be seen that the weight of precursor powder decreases abruptly from 100 ^oC to 280 ^oC, which is likely to be due to the evaporation of the solvent, decomposition of the impurities, and hydrolysis of the metal precursors of $Al(NO_3)_3$ precursor powder. After 280 ^oC, the gradual weight loss of precursor powder indicates that the residual of the solvent and impurities of the precursor powder (such as nitrate) have been almost eliminated. The TGA-DSC results prove that the 300 ^oC annealing temperature is high enough to form the metal-oxygen metal frame, densify the films, and eliminate precursor impurities in the AlO_x layer. Table 3-1 summarizes the microstructural and

dielectric properties of solution-processed AlO_x dielectrics under various annealing temperatures, including thickness, roughness, leakage current at 6 V, areal capacitance, and dielectric constant at 1 kHz.

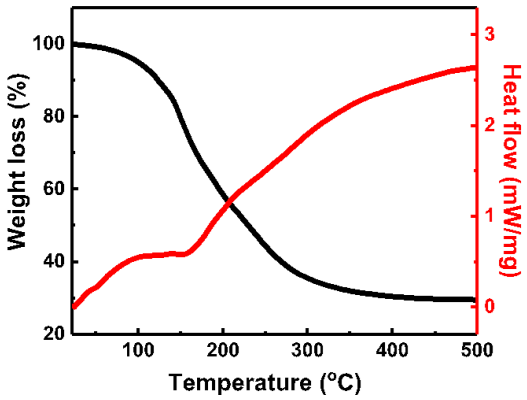

Figure 3-3. Thermogravimetric analysis-differential scanning calorimetry (TGA-DSC) curves of $Al(NO_3)_3$ precursor powder heated from 20 °C to 500 °C with a heating rate of 10 °C/min.

3D AFM images of solution-processed AlO_x thin films annealed at different temperatures are shown in Figure 3-4. It is noticeable that big bright spots can be observed in Figure 3-4 (a) and (d). The specified big bright spot is also observed in other literature to report solution-processed high-*k* dielectric thin films annealed at different temperatures (130-500 °C) [10, 20, 32, 33]. These bright spots are considered to be related to surface peaks generated during the formation of the thin film, which could be a type of defect associated with solution-processing. One plausible explanation is that these surface peaks are formed by the tiny particles (diameters <0.1 μm) present in precursor solutions, as the concentration (2.5 M) of the precursor solution is relatively high. These tiny particles can thus pass through the mesh holes of the PES

syringe filter (0.45 μm diameter). More detailed investigation and discussion can be found in [34].

Table 3-1. Microstructural and dielectric properties of solution-processed AlO_x thin films.

Annealing Temperature (°C)	**Thickness (nm)**	**Roughness (nm)**	**Leakage Current at 8 V (μA/cm²)**	**Areal Capacitance (nF/cm²) at 1 kHz**	**Dielectric Constant at 1 kHz**
150	60.2 ± 4.1	0.14	24 ± 3.8	99.1 ± 6.9	7.0 ± 0.5
200	54.2 ± 3.3	0.11	8.8 ± 1.1	127.8 ± 5.5	7.8 ± 0.2
250	50.8 ± 2.4	0.19	6.1 ± 0.7	135.4 ± 3.1	8.2 ± 0.1
300	44.1 ± 0.9	0.2	0.97 ± 0.05	171.6 ± 1.4	8.6 ± 0.1

Table 3-2. Comparison of solution-processed high-*k* dielectrics parameters with other works.

Dielectric	Temperature [°C]	d [nm]	C_i [nF cm^{-2}]	*k*	J_{leak} (A cm^{-2}) (Voltage)	E_b [MV cm^{-1}]	Year	Ref.
0 M H_2O_2 AlO_x	300	~45	171	8.7	2.6×10^{-6} (6 V)	-	2019	This work Chapter 3
7.5 M H_2O_2 AlO_x	260	~20	300	6.78	9.40×10^{-6} (4 V)	-	2020	This work Chapter 4
ZrLaO	350	61.3	267.5	18.5	3.7×10^{-6} (2.5 MV/cm)	>5	2020	This work Chapter 5
Al_2O_3	350	44	625	7.1	1.0×10^{-3} (2 MV/cm)	-	2014	[19]
HfO_2	450	104	151	18.8	4.0×10^{-5} (2 MV/cm)	2.7	2015	[35]
ZrGdO	460	13	380	5.39	5.7×10^{-4} (1 MV/cm)	4	2019	[36]
HfLaO	500	60	178	22	3.0×10^{-6} (2 MV/cm)	4.7	2014	[37]
La_2O_3	500	137	75	11.6	2.0×10^{-6} (1 MV/cm)	1.7	2014	[37]
ZrO_2	500	20	398.8	9	2.8×10^{-6} (1.5 MV/cm)	-	2018	[38]
YScO	500	64	133	9.6	5.0×10^{-6} (2 MV/cm)	3.8	2016	[39]

Despite the existence of the observed surface peaks, the RMS roughness values of all AlO_x thin films are found to be in the range of 0.1-0.2 nm, indicating that AlO_x thin films have an ultra-smooth surface when annealed at temperature up to 300 °C, which is in consistent with their amorphous structure. The smooth surface of the dielectric is suitable for suppressing the surface-roughness-induced leakage current and achieving

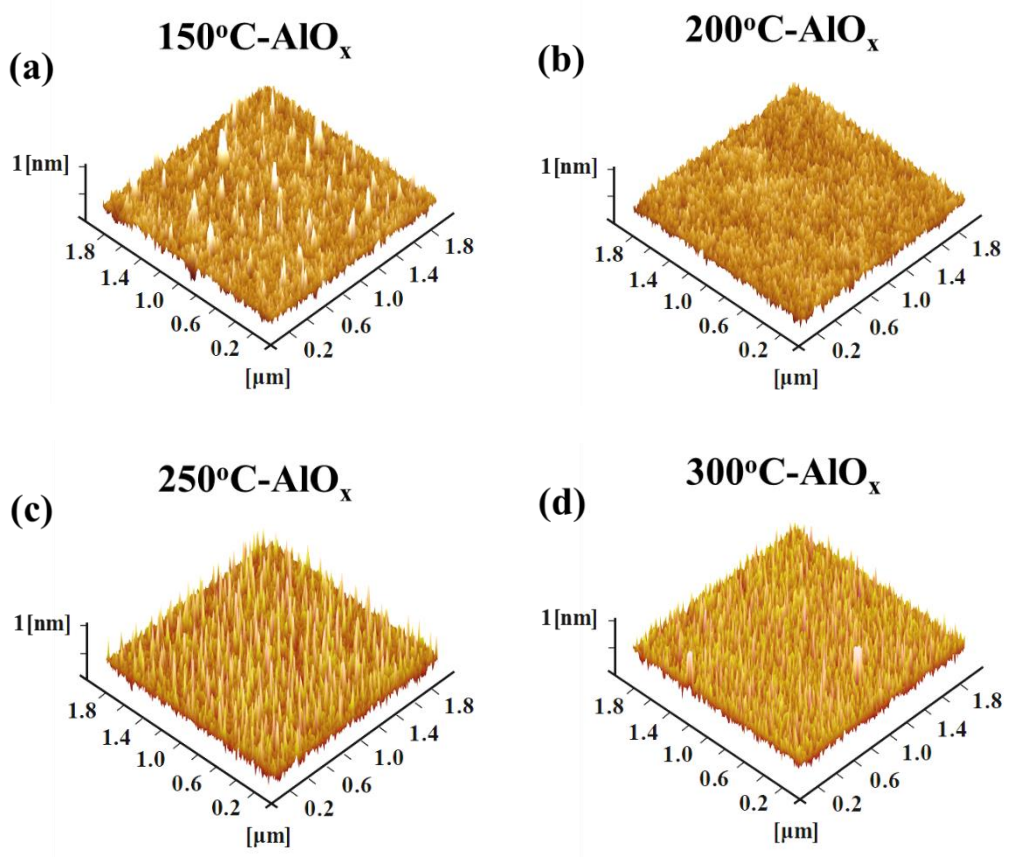

Figure 3-4. 3D AFM images of solution-processed AlO_x thin films annealed at **(a)** 150 °C, **(b)** 200 °C, **(c)** 250 °C and **(d)** 300 °C. The image dimensions are 1.8 µm × 1.8 µm.

expeditious charge carrier mobility within the interface between gate dielectric layer and semiconductor layer for potential TFT application [40].

Figure 3-5 (a) shows the XRD spectra of AlO_x thin films annealed at different temperatures. No peaks corresponding to the crystalline AlO_x are observed, which confirms that AlO_x films remain amorphous up to 300 °C. The amorphous structure allows for low leakage current and higher breakdown voltage. Conversely, poly-crystalline films allow enhanced leakage current and impurity diffusion via grain boundaries [14, 41, 42].

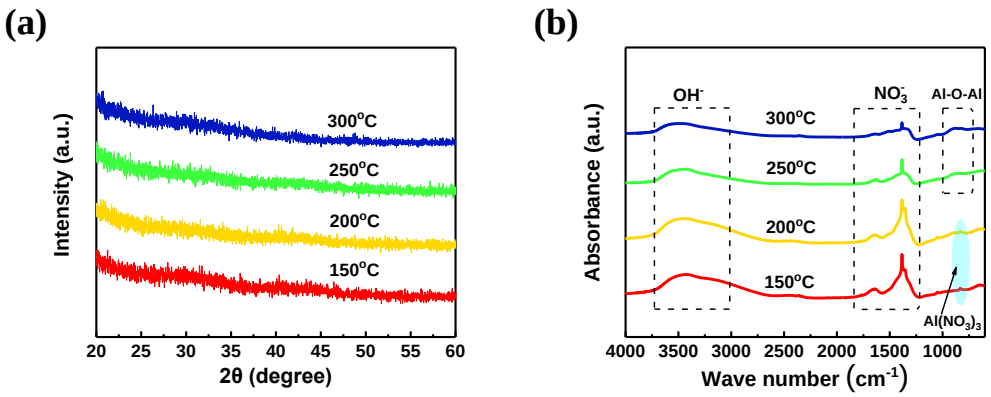

Figure 3-5. (a) XRD patterns and **(b)** FT-IR spectra of solution-processed AlO_x thin films annealed at different temperatures.

FT-IR spectra of the solution-processed AlO_x thin films are shown in Figure 3-5 (b). The broad peaks in the range of 3000-3600 cm^{-1} are likely to be related to hydroxyl (O-H) group stretching vibrations [43]. The peaks in the 1300-1500 cm^{-1} range represent nitrate (NO^{3-}) group deformation vibrations [22, 43, 44]. As the annealing temperature increases, these two peaks diminish, which is ascribed to the evaporation of the solvent and the gradual decomposition of O-H and NO^{3-} groups in thin films. The bands in the range of 750-900 cm^{-1} are due to vibrations of the Al-O bond. In low temperature (<200 °C) annealed conditions, the Al-O bond is not formed and only weak absorptions of hydrated metal nitrate species are observed [45]. At annealing temperature >250 °C, the Al-O bond is configured.

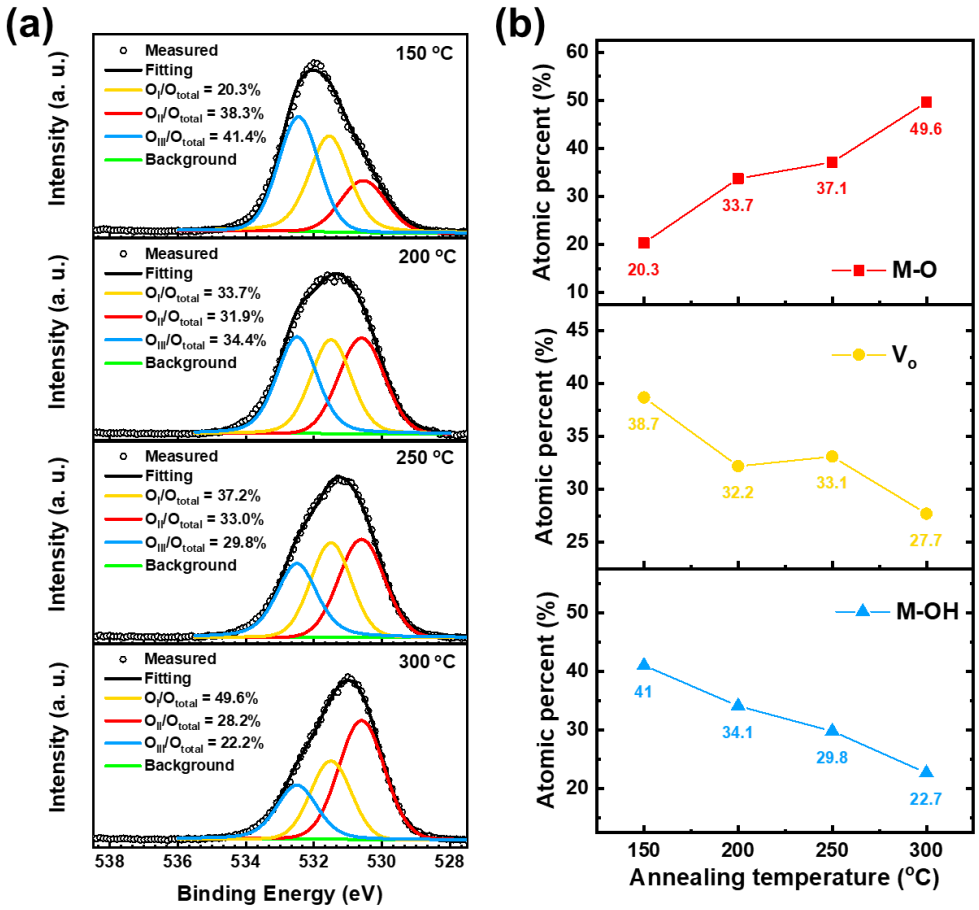

Figure 3-6. (a) O 1s peaks and their deconvolution results of AlO_x thin films annealed at 150 - 300 °C. **(b)** Semiquantitative analyses of the oxygen component for the corresponding AlO_x thin films.

To further determine the chemical compositions of AlO_x thin films annealed at various temperatures, XPS measurements were carried out. Figure 3-6. (a) divide O 1s peaks into three peaks centered 529.5 (O_I), 531.1(O_{II}), and 532.1 eV (O_{III}), respectively. The peak with low binding energy (O_I) represents O^{2-} ions combined with Al ions, the peak with the medium binding energy (O_{II}) is assigned to O^{2-} ions in the oxygen-deficient regions, and the peak with high binding energy (O_{III}) is related to loosely bound oxygen, such as chemisorbed surface hydroxyl, $-CO^3$, absorbed H_2O, or

absorbed O_2. Figure 3-6. (b) summarizes the calculated atomic percentages based on the area integration of O 1s peaks in Figure 3-6. (a), it is found that, with increasing annealing temperature, the area ratio of O_I peak to the total oxygen region (O_I/O_{total}) increases from 20.3 % to 49.6 % and the area ratio of O_{II} peak to the total oxygen region (O_{II}/O_{total}) decreases from 38.7 % to 27.7 %. This phenomenon indicates that an increased annealing temperature contributes to the enhanced dehydroxylation, converting metal hydroxides into metal oxides. According to previous reports, the existence of M-OH groups can serve as trap sites for charge-carriers, leading to the increased leakage current, reduces breakdown electric field and degraded sub-threshold characteristics at the gate insulator/semiconductor interface [46]. Consequently, 300 ^oC is considered to be high enough to remove the solvent residue and impurities, and facilitate the formation of the metal-oxide framework, which is in agreement with the TGA-DSC and XPS results shown in Figure 3-3 and Figure 3-6, respectively.

Figure 3-7 (a) shows the areal C-*f* plots of AlO_x MOSCAPs. All devices have demonstrated satisfied small frequency dispersion with measurement frequency from 1 k-1 M Hz. The areal capacitance increases with the rise in annealing temperature. This can be attributed to the formation of the metal-oxide framework and its densification at high annealing temperatures [11, 14]. The dielectric constants of AlO_x thin films were calculated using the capacitance values measured at 1 kHz (see Table 1) and are consistent with values reported for solution-processed AlO_x (~8) [19, 25].

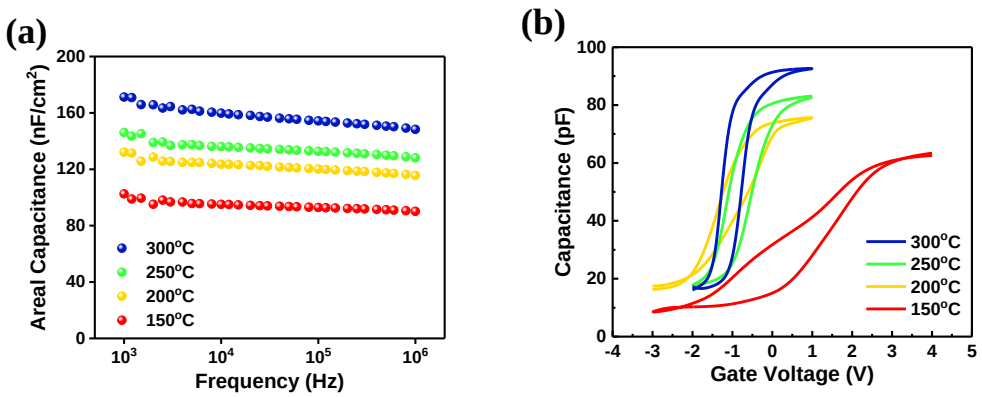

Figure 3-7. (a) Capacitance-frequency (C-*f*) and **(b)** capacitance-voltage (C-V) characteristics of solution-processed AlO_x MOSCAPs annealed at 150, 200, 250 and 300 °C.

The C-V characteristics of AlO_x MOSCAPs measured at 1 MHz are shown in Figure 3-7 (b). Since the slope of the C-V curves in the depletion region reflects the interface trap density, the slope increases with increasing annealing temperature, indicating a decrease in interface trap density. This could be due to the evaporation of hydroxyl groups and residual nitrate, the decomposition of the metal precursor, and the formation of the metal-oxide framework under high annealing temperature [2, 10, 20, 44]. In addition, the increased capacitance at the accumulation region is related to the increased AlO_x concentration at the high annealing temperature.

The leakage current density-gate voltage (J_{leak}-V) measurements were performed to evaluate the leakage behavior of AlO_x thin films, as shown in Figure 3-8 (a). It can be seen that J_{leak} decreases with increasing anneal temperature. The 150 °C - AlO_x thin film has a J_{leak} of 2.6 $\times 10^{-5}$ A/cm^2 at 6 V, which is relatively high compared to the thin films annealed at 200, 250, and 300 °C. This indicates that the AlO_x annealed at 150 °C suffers from an incomplete decomposition of precursor solution and therefore contain

O-H and NO^{3-} groups, as shown in Figure 3-5 (b). The O-H and NO^{3-} groups provide leakage current paths and result in a high J_{leak} [11] [47]. The 200 °C - AlO_x, 250 °C - AlO_x, and 300 °C - AlO_x thin films all show quite low J_{leak} at 6 V; namely 5.0 × 10^{-6} A/cm^2, 3.5 ×10^{-6} A/cm^2 and 2.6 × 10^{-6} A/cm^2, as shown in Table 3-1 [19]. This low leakage current could be attributed to the decomposition of the metal precursor as well as the formation of the metal-oxide framework [2, 10, 20]. The comparison of solution-processed high-*k* dielectrics parameters of this thesis with other works are shown in Table 3-2.

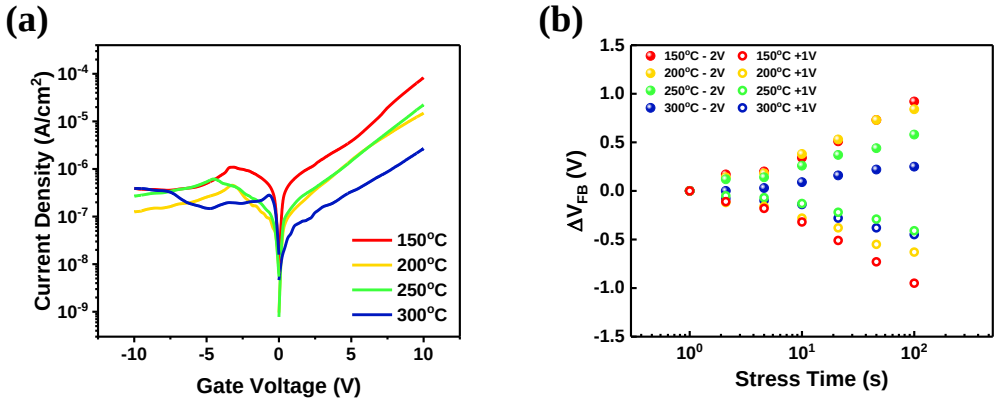

Figure 3-8. (a) Leakage current density-gate voltage (J_{leak}-V) and **(b)** ΔV_{FB} vs stress time of solution-processed AlO_x MOSCAPs annealed at different temperatures.

The BS stability of AlO_x MOSCAPs annealed at different temperatures is assessed from V_{FB} shifts under 100 s BS, as shown in Figure 3-8 (b). It is found that 300 °C - AlO_x MOSCAP has the minimum ΔV_{FB} under positive bias-stress (PBS) and negative bias-stress (NBS), and hence shows the best BS stability. This is likely to be due to its low defect density and high metallic oxide concentration, which are in agreement with

the results of TGA-DSC (Figure 3-3), AFM (Figure 3-4), FT-IR (Figure 3-5 (b)) and J_{leak}-V_g (Figure 3-8 (a)) shown earlier.

3.4 The total dose effects of 300 ºC annealed AlO_x thin film

It can be concluded from the results above, that the 300 ºC - AlO_x thin films have the best film quality, as indicated by their low defect density, high metallic oxide concentration, low leakage current, and BS stability. Further radiation investigation of the BS and BRS stabilities of 300 ºC - AlO_x MOSCAPs are now investigated in detail. Figure 3-9 (a) and (b) show the C-V curves of 300 ºC - AlO_x MOSCAPs under PBS and NBS with stress time up to 10^5 s, respectively. For comparison, the C-V curves under positive biased radiation stress (PBRS) and negative biased radiation stress (NBRS) with a total dose of around 92 Gy (SiO_2) are shown in Figure 3-9 (c) and (d). The shift of the C-V curves, positive or negative, was determined by the gate bias stress polarity. PB and NB produced negative and positive ΔV_{FB}, respectively. Positive ΔV_{FB} could be ascribed to the electron trapping in the AlO_x bulk and the passivation of the AlO_x/Si interface, while negative ΔV_{FB} was believed to be caused by proton trapping in the AlO_x bulk as well as the generation of Si dangling bonds at the AlO_x/Si interface. It is also observed that radiation exposure had effects on the shifts of the C-V curves under BRS, which was likely to be due to radiation-induced EHPs generation facilitating the charge trapping/de-trapping behavior in the AlO_x bulk, as well as the passivation/de-passivation at the AlO_x/Si interface.

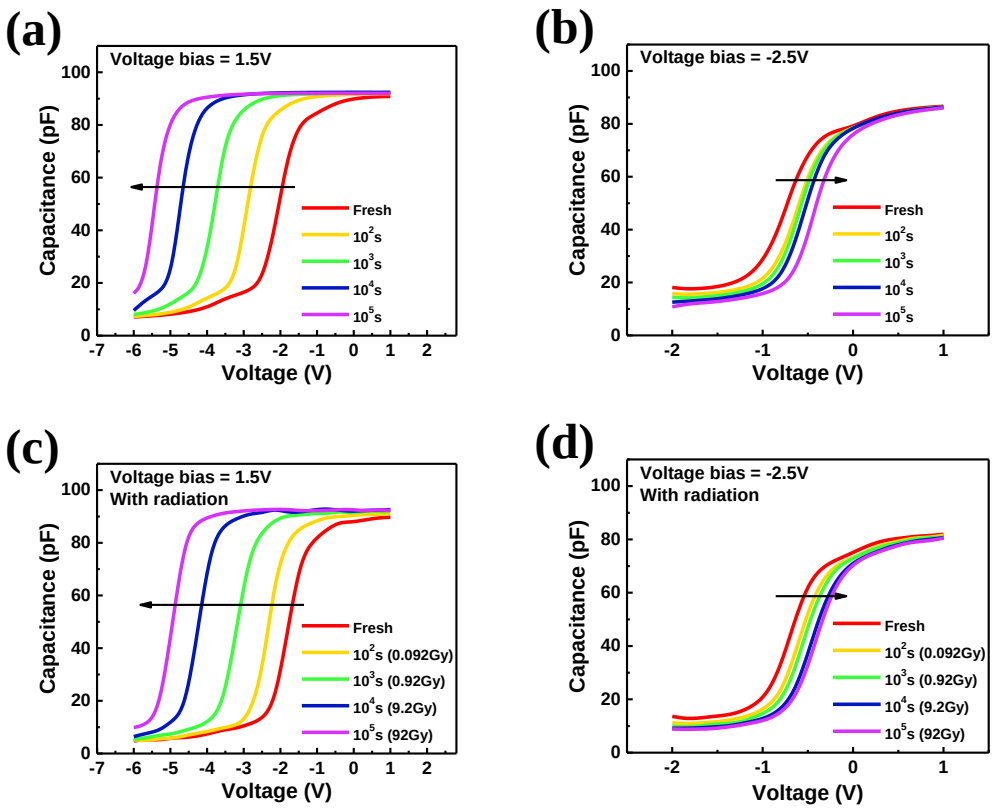

Figure 3-9. C-V curves of solution-processed 300 ºC - AlO_x MOSCAPs under gate voltage of **(a)** +1.5 V, **(b)** -2.5 V, **(c)** irradiated +1.5 V and **(d)** irradiated -2.5 V with 10^5 s bias-stress time. The total dose is around 92 Gy (SiO_2).

Figure 3-10 (a) and (b) summarize the ΔV_{FB} of 300 ºC - AlO_x MOSCAPs under 10^5 s BS and BRS, respectively. The device exhibited less ΔV_{FB} under NBS than under PBS with/without radiation, indicating better NBS stability than PBS stability. As shown in Figure 3-10 (b), the radiation is observed to cause a positive ΔV_{FB} under both PBRS and NBRS, which is likely to be induced by the formation of negatively charged states and/or the build-up of interface traps with the assistance of radiation. The comprehensive mechanism will be discussed below. Furthermore, radiation-induced EHPs would having no significant effect on device properties without an applied electric field [48]. ΔN_{ot} causes a parallel shift of both mid-gap and flat band voltages,

while ΔN_{it} only causes ΔV_{FB} due to the stretch-out of the C-V curve. Consequently, ΔV_{FB} is attributed to the combined effect of the generation of oxide traps in AlO_x and interface traps near the AlO_x/Si interface.

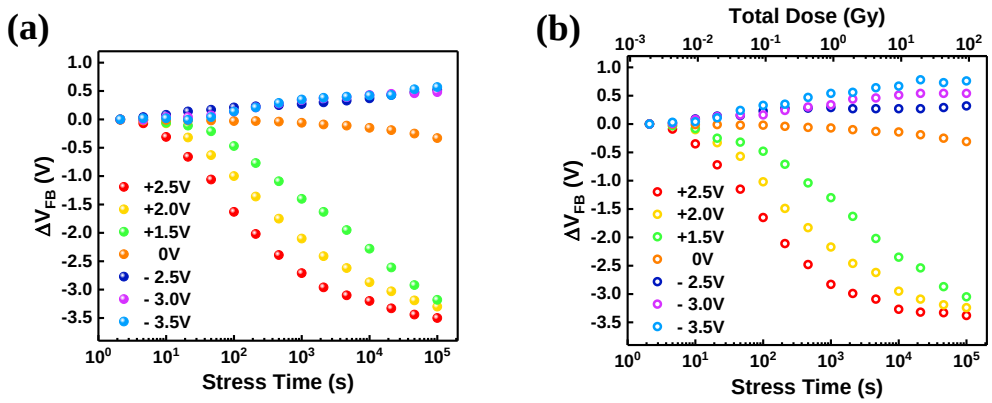

Figure 3-10. Flat-band voltage shift (ΔV_{FB}) of solution-processed 300 °C - AlO_x MOSCAPs induced by different bias-stresses as a function of **(a)** stress time, **(b)** stress time & total dose.

As shown in Figure 3-11, ΔN_{ot} can be estimated by equation (3-1) [49]:

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \tag{3-1}$$

where ΔV_{mg} is the mid-gap voltage shift obtained from C-V curves, C_{ox} is the gate capacitance, q is the electronic charge, and A is the electrode area. It is notable that, under NBRS, ΔN_{ot} increased with increasing radiation dose and there was a net negative oxide trapped charges induced by BRS.

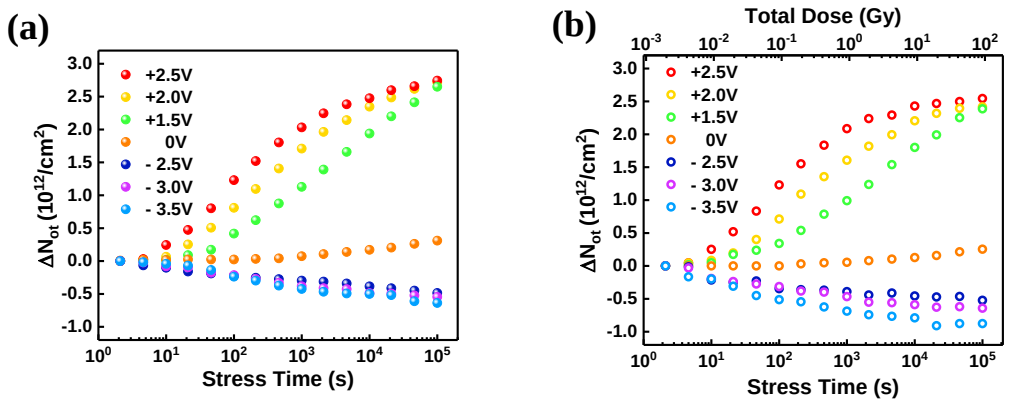

Figure 3-11. Variation of oxide traps (ΔN_{ot}) of solution-processed 300 °C - AlO_x MOSCAPs induced by different bias-stresses as a function of **(a)** stress time, **(b)** stress time & total dose.

As shown in Figure 3-12, ΔN_{it} can be estimated by equation (3-2) [49]:

$$\Delta N_{it} = \frac{C_{ox}(\Delta V_{FB} - \Delta V_{mg})}{qA}. \quad (3\text{-}2)$$

radiation generated negative interface traps under all measurement conditions. Furthermore, for all total doses, ΔN_{ot} and ΔN_{it} were in the order of 10^{12} and 10^{11} $cm^{-2,}$ and no significant variation of N_{it} was observed compared to N_{ot}, indicating that oxide traps dominate the shift of V_{FB}. Such a high level of N_{ot} was likely to be due to hydrogen reactions. Similar results have been reported on high-*k* dielectric based MOSCAPs. Kahraman et al. have reported Gd_2O_3 MOSCAPs with $\Delta N_{ot} = 2.3\times10^{12}$ cm^{-2} and ΔN_{it} $=2.5\times10^{11}$ cm^{-2} after circa 50 Gy γ-ray exposure in [50] and Er_2O_3 MOSCAPs with ΔN_{ot} (1.3×10^{12} cm^{-2}) and ΔN_{it} (9.4×10^{10} cm^{-2}) after circa 78 Gy γ-ray exposure in [51].

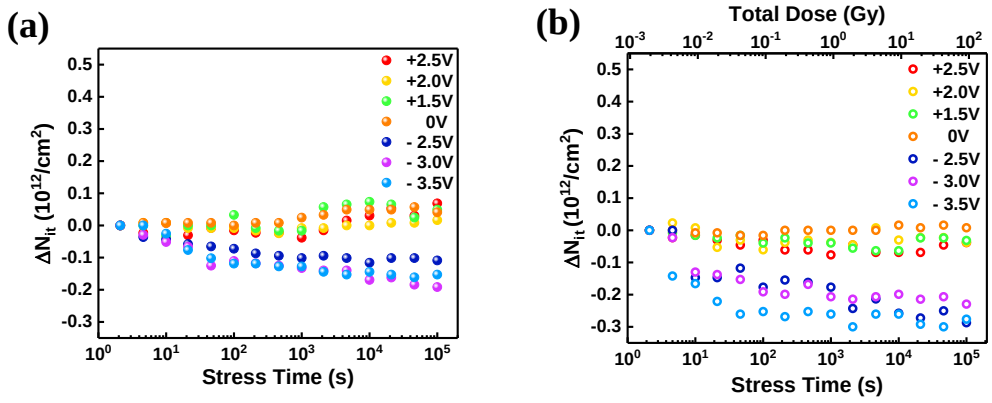

Figure 3-12. Variation of interface traps (ΔN_{it}) of solution-processed 300 °C - AlO_x MOSCAPs induced by different bias-stresses as a function of **(a)** stress time, **(b)** stress time & total dose.

As shown in Figure 3-11 and Figure 3-12, compared to BS, ΔN_{ot} and ΔN_{it} were found to decrease slightly under PBRS, while they increased in magnitude under NBRS. Under PBRS, the reduced ΔN_{ot} was ascribed to the combined effect of bias-stress and radiation exposure with increasing stress time. To compare the BRS stability of solution-processed AlO_x with Al_2O_3 thin films fabricated by ALD. 40 nm thick ALD Al_2O_3 thin films with *k* value ~ 8.0 were fabricated at 100 °C. Afterwards, their BS and BRS stability were investigated with stress time up to 46000 s and total dose ~ 92 Gy. The calculated ΔN_{ot} of ALD AlO_x capacitors with and without radiation are shown in Figure 3-13 (a) and (b), respectively. These devices reveal small radiation induced oxide traps and interface traps, indicating better radiation hardness relative to solution-process 300 °C-AlO_x. It is reported that solution-processed, low temperature AlO_x contains a large concentration of bonded oxygen, which could provide defect states in the bandgap of AlO_x [11].

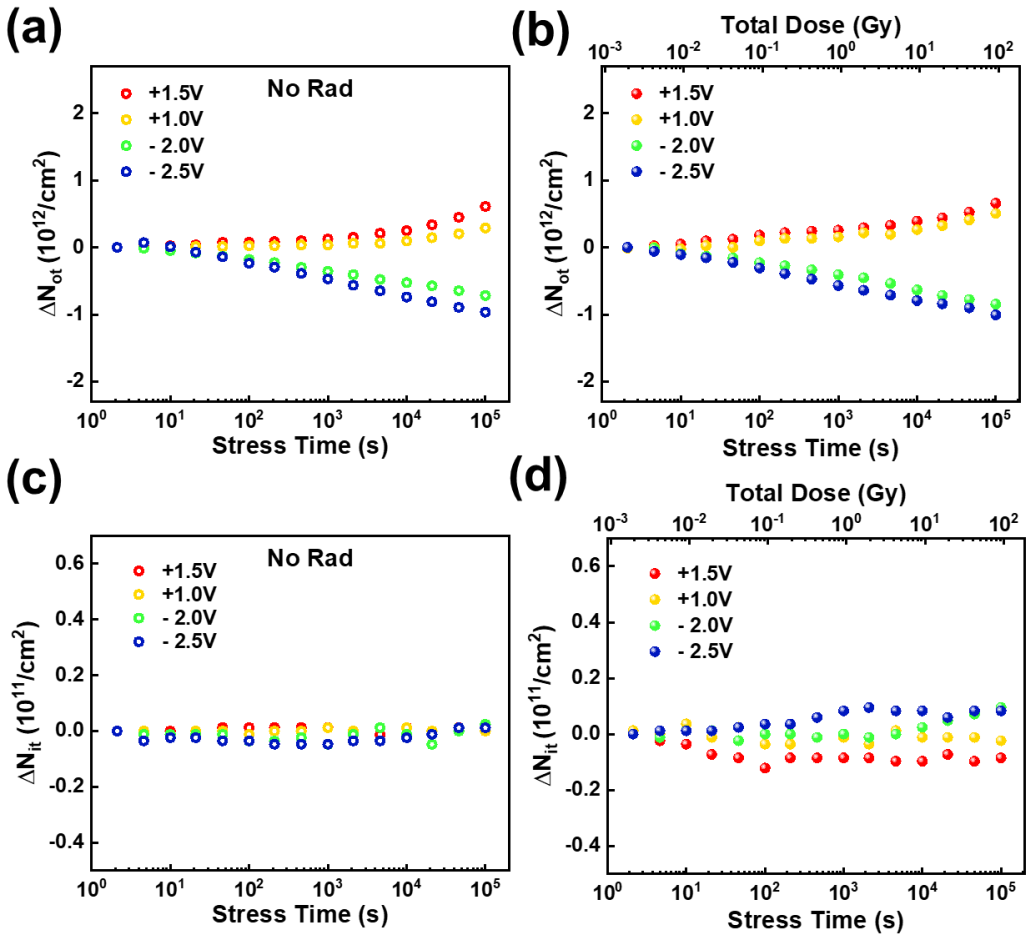

Figure 3-13. Variation of oxide traps (ΔN_{ot}) induced under **(a)** BS and **(b)** BRS. Variation of interface traps (ΔN_{it}) induced under **(c)** BS and **(d)** BRS.

As shown in Figure 3-14 (a), neutral oxide traps were created in the bulk of the AlO_x during exposure to ionizing irradiation [52]. With a positively applied gate voltage, electrons in the accumulation region at the AlO_x/Si interface could tunnel from the Si substrate into those radiation-induced neutral oxide traps (process (2) in Figure 3-14 (a)). The effects of radiation exposure and gate voltage added up and negatively charged traps were formed accordingly as the BRS time increased, which thus partially

compensated the positive oxide trapped charges near the AlO_x/Si interface, thus reduced positive ΔN_{ot} [53, 54].

The decreased ΔN_{it} under PBRS could be explained by the conventional two-stage process theory originally described by McLean [55]. As depicted in Figure 3-14 (a), in the first stage, as the radiation passes through a gate oxide, EHPs were created within the gate dielectric (process (1) in Figure 3-14 (a)) [56]. The radiation-induced electrons escaped from the oxide within several picoseconds due to their higher mobility compared to the holes. Meanwhile, the radiation-induced holes moved towards the AlO_x/Si interface under PBRS. Thereafter, in the second stage, hydrogen was liberated during the transport of holes, in the form of protons (H^+) [29], and reached the interface via a hopping transport. The H^+ could then passivate the existing Si dangling bonds (Si^-) via reaction (3-3) listed below (process (3) in Figure 3-14 (a)). Once a defect is passivated by hydrogen, it no longer functions as an interface trap, therefore ΔN_{it} was reduced accordingly. Meanwhile, the Si-H bonds at the AlO_x/Si were also de-passivated by protons through reaction (3-4):

$$Si^- + H^+ \rightarrow Si - H \quad (3\text{-}3)$$

$$Si - H + H^+ \rightarrow Si^+ + H_2 \quad (3\text{-}4)$$

$$Si - H \rightarrow Si^- + H^+ \quad (3\text{-}5)$$

Nevertheless, the high concentration of protons and Si dangling bonds near the AlO_x/Si interface could cause a higher probability for protons to passivate Si dangling bonds

via reaction (3-3), rather than to de-passivate a Si-H bond and form an interface trap via reaction (3-4) [57-59].

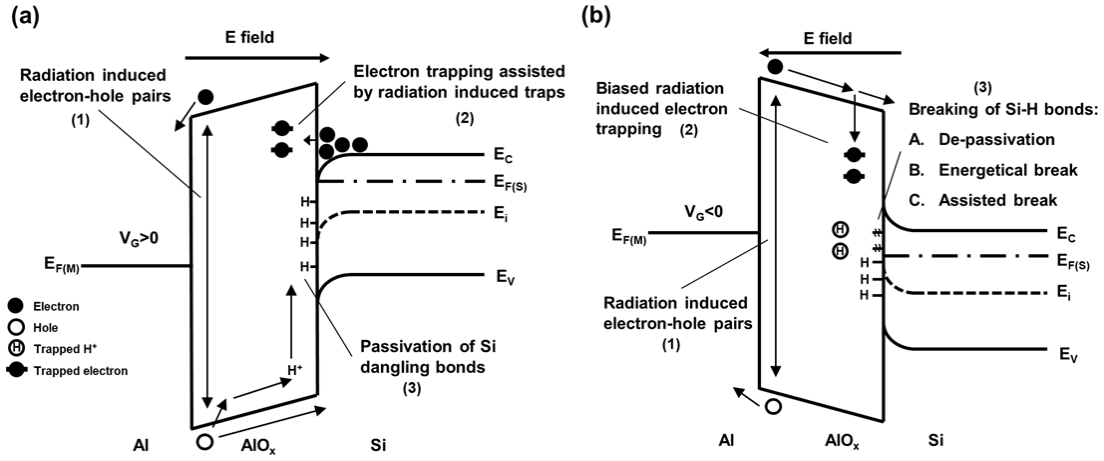

Figure 3-14. Energy band diagrams of solution-processed 300 °C - AlO_x MOSCAPs under **(a)** positive biased radiation stress (PBRS) and **(b)** negative biased radiation stress (NBRS).

The mechanism for the increase of ΔN_{ot} and ΔN_{it} in magnitude under NBRS is more complicated. As shown in Figure 3-14 (b), radiation-induced electrons transported towards Si substrate under the applied negative electric field. Some of them fell into traps to form negative trapped oxide charges and cause an increase of ΔN_{ot} magnitude. In the meantime, the applied negative electric field inhibited the motion of the radiation-induced H^+ to the AlO_x/Si interface, and hence the passivation (reaction (3-3)) at the interface was suppressed. Nevertheless, the de-passivation (reaction (3-4)) could still occur and lead to an increase of ΔN_{it} if there is a source of hydrogen at the interface or in the Si substrate. For an n-type Si substrate, P-H complexes, or oxygen protrusions could be the possible source of hydrogen for de-passivation [60]. Furthermore, the

energetic breaking of Si-H bonds through reaction (3-5) under BRS (process (3) in Figure 3-14 (b)) could contribute to the increase of both ΔN_{ot} and ΔN_{it}. When a Si-H bond is broken, it will release H^+ which could be trapped in AlO_x to form an oxide trap under NBRS. Meanwhile, a Si dangling bond is formed and acts as an interface trap. The BRS could significantly reduce the binding energy of a H atom, indicating that the Si-H bond is relatively easy to break [29]. In addition, the defects or impurities, such as impurity Al atoms near the AlO_x/Si interface and suboxide bonds, could assist in the breaking of Si-H bonds and cause trapping of the H^+ released from the Si-H bonds under NBRS. Consequently, under NBRS, the biased radiation-induced electron trapping among AlO_x bulk resulted in a negative ΔN_{ot}. While the de-passivation, energetic break, and assisted break of Si-H bonds by impurity Al atoms near the AlO_x/Si interface and suboxide bonds were the three main factors that contribute a negative ΔN_{it}.

3.5 Summary

The method to form high-quality aqueous solution-processed AlO_x thin films with reduced impurities and defects was investigated. It has been found that an annealing temperature of 300 ºC could result in AlO_x thin films with low defect density, high metallic concentration, weak frequency dispersion, low interface trap density, low leakage current, and good BS stability. In addition, the BRS stability of 300 ºC-AlO_x based MOS capacitors was studied. The results suggest that ΔN_{ot} can be attributed to trapping/de-trapping behavior of radiation-induced protons in AlO_x bulk, whilst ΔN_{it} is

mainly caused by the passivation/de-passivation of Si dangling bonds at AlO_x/Si interface. Furthermore, oxide trap charges were more effective than the interface trap charges in shifting V_{FB} for 300 ºC-AlO_x MOS capacitors. Both ΔN_{ot} and ΔN_{it} were observed to decrease slightly under PBRS and increase under NBRS. When the device was under PBRS, the radiation-induced electron dominated the decrease of ΔN_{ot} and the passivation of Si dangling bonds at the AlO_x/Si interface dominated the decrease of ΔN_{it}. Under NBRS, the de-passivation, energetic break, and assisted break of Si-H bonds by impurity Al atoms near the AlO_x/Si interface and suboxide bonds were most likely to contribute to the increase in the magnitude of ΔN_{ot} and ΔN_{it}. The finds of this chapter offer a clear inspiration for achieving highly stable solution-processed high-*k* dielectrics working in radiation harsh environment.

3.6 References

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Chapter 4: Improved bias stress and biased radiation stress stability of aqueous solution-processed AlO_x thin films using hydrogen peroxide

4.1 Introduction

Nowadays, solution-processes have been developed due to the possibility of low-cost and large-area fabrication without using vacuum deposition techniques. Furthermore, solution-processed high-*k* oxide dielectrics enable the low leakage current, low operation voltage, and ease process integration with solution-processed TFTs [1-3]. However, high-temperature annealing of solution-process limits the potential application of solution-processed materials on flexible substrates. Therefore, it is necessary to develop low-temperature solution-processed techniques for the full realization of flexible and large-area oxide electronics. H_2O_2 is a suitable oxidizer for solution-processing to lower the annealing temperature. Through strong oxidation, H_2O_2 could decompose the chemicals and impurities at low temperature and combine with oxygen-related defects within oxide layers, which helps to reduce the V_o in AlO_x bulk and interface traps at AlO_x/Si interface. Comparing to other methods reported to reduce V_o (e.g. high-pressure oxygen annealing, ozone-plasma treatment), adding H_2O_2 in solution-process is simple, effective, and low-cost.

It is reported that solution-processed AlO_x thin films suffer from inferior BS and BRS stabilities compared to those fabricated by traditional vacuum methods, which severely limits their practical applications [4-6]. Some literature has improved the BS stability of solution-processed devices through high-pressure annealing [7], doping with carrier suppressor [8, 9], UV treatment [7, 10] and diffusion between different materials [11]. In those works, the BS stability of solution-processed devices has been examined and discussed together with the mechanism in detail. However, a few studies have been conducted on stability under various bias stress state, especially the stabilities of solution-processed materials under BRS [4, 6, 12, 13]. As solution-process is crucial to large-area electronics in harsh radiation environments, such as whole-body-scanning X-ray detectors and large-area antenna arrays [12]. Notably, the methods to improve the BRS stability of solution-processed devices have been seldomly reported and need to be systemically investigated [12].

In this chapter, H_2O_2 was employed to lower the annealing temperature of solution-processed aqueous AlO_x thin films. It was found that thin films with high quality, low oxide trap and semiconductor/oxide interface trap density have been successfully fabricated at low temperature (~260 ^oC). Besides, the BS and BRS stabilities of aqueous solution-processed AlO_x MOS capacitors with 7.5 M H_2O_2 are significantly improved with stress time up to 46000 s and total dose up to 42 Gy.

4.2 Experimental details

The fabrication process of H_2O_2-AlO_x is similar to the fabrication process shown in Figure 3-1. 0.6 M ($Al(NO_3)_3 \cdot xH_2O$) was dissolved in DI water with 0 - 10 M H_2O_2 to produce a colorless and clear solution. The solution was stirred for 6 h to ensure the precursor was fully dissolved since the nitrate salts have excellent water solubility. Then the solution was filtered by a 0.22 μm Polytetrafluoroethylene (PTFE) syringe filter before spin coating.

To prepare the substrates, single-crystal lightly doped N-type silicon wafers (orientation: 100, doping concentration: ~10^{15} cm^{-3}, resistivity: 2-4 Ω·cm) were dipped in 2 % HF aqueous solution for 30 s to remove the native oxide and then dried by N_2. Subsequently, the Si substrates were exposed under air plasma for 30 mins to increase their hydrophilia. After the preparation of Si substrates, the precursor solution was spin-coated on the processed substrate at 4000 rpm for 40 s. Then the samples were directly transferred to a hot plate set to 125 °C and ramped to a final annealing temperature of 260 ºC at a rate of 25 ºC min^{-1} and held for 1 h. Finally, 300 nm thick Al top and bottom electrodes were deposited through shadow masks by e-beam evaporation. The circular top electrode had a diameter of 0.3 mm.

4.3 Improved device properties and stability through employing H_2O_2

Leakage behavior (J_{leak}-V_g) of the AlO_x thin films was investigated and shown in Figure 4-1 (a). The thickness of all AlO_x thin films is around 23-25 nm. It can be observed that adding H_2O_2 effectively reduced J_{leak}. It was attributed to the improved film quality with reduced structure defects, precursor impurities, and V_o. In this situation, the leakage paths were suppressed and the leakage current was reduced accordingly. The mechanism of the leakage current may be attributed to the Poole-Frenkel (PF) emission, since it is usually assigned as the dominating leakage mechanism in metal-insulator-metal thin film stacks [14]. Similar to Schottky emission, PF emission describes how thermal excitation of electrons may overcome the trap barrier and emit them into the dielectric conduction band. Thus, PF emission is sometimes called internal Schottky emission. The electron Coulomb potential energy in a trap center decreases under the applied electric field, hence the probability of an electron being thermally excited out of the trap increases. PF emission can be expressed as (4-1) [15]:

$$J \propto E \exp\left[\frac{-q(\emptyset_B - \sqrt{qE/\pi k_d \varepsilon_0})}{k_B T}\right] \quad (4\text{-}1)$$

where J is the current density, E is the electric field across the gate oxide layer, q is the elementary charge, $\emptyset_B$ is the voltage barrier that an electron (or a hole) escapes from its trap level into the conduction band (or valence band), k_d is the self-consistent

dynamic dielectric constant, ε_0 is the permittivity of vacuum, k_B is Boltzmann's constant, and T is the temperature. The leakage current is dependent on the T and E. Since the leakage behavior was investigated under room temperature, if the leakage current was caused by PF emission, the ln(J/E) versus $E^{1/2}$ should be linear. The oxide field (E) was calculated according to equation (4-2):

$$E = \frac{V_{ox}}{t} \tag{4-2}$$

where V_{ox} is the voltage drop across the oxide, t is the thickness of the AlO_x thin films. V_{ox} can be calculated from equation (4-3):

$$V_{ox} = V_g - V_{FB} - \emptyset_s \tag{4-3}$$

where V_g is the gate voltage, V_{FB} is the flat-band voltage, $\emptyset_s$ is the voltage drop across Si substrate (surface potential). For a lightly doped n-type Si substrate, if the substrate is accumulated, there will be about $\emptyset_s = 0.2$ V across the accumulation layer. While under negative bias-stress voltage, if the substrate is inverted, there could be about $\emptyset_s = 0.8$ - 0.9 V across the depletion region. This all assumes no pinning of the Fermi-level. As shown in Figure 4-1 (b), the leakage behavior of the AlO_x capacitors in the accumulation region was investigated, good linear fits for the leakage of the J-V characteristics were obtained. This implies that the PF effect may be the main leakage mechanism of the solution-processed AlO_x oxide when the Si substrate was accumulated.

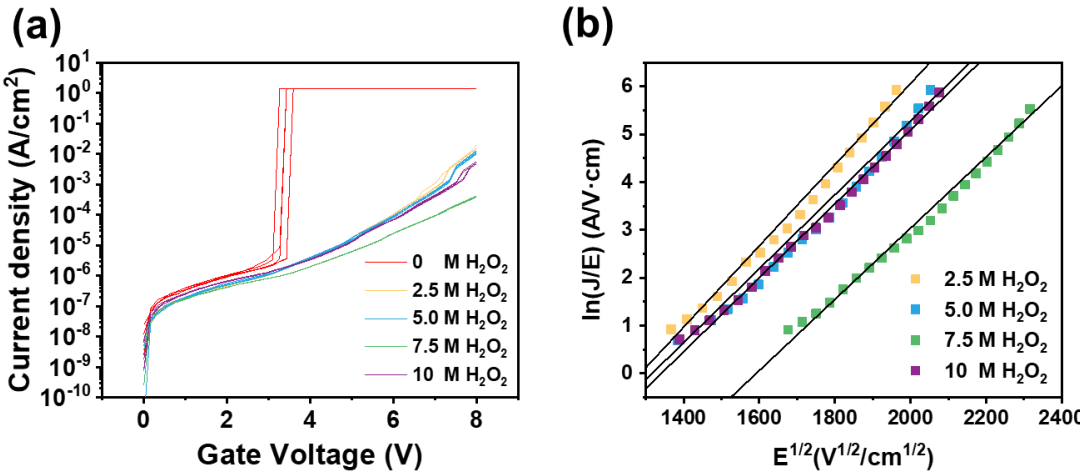

Figure 4-1. (a) Leakage behavior (J_{leak}-V) and **(b)** the Poole-Frenkel (PF) fitting between the leakage current and the electric field in the accumulation region of AlO_x MOSCAPs with different H_2O_2 concentration.

Table 4-1 summarizes the properties of H_2O_2 AlO_x thin films and MOSCAPs with different H_2O_2 concentration. The C-V curves measured at 1 MHz of AlO_x MOSCAPs are displayed in Figure 4-2 (a). To verify the uniformity of the H_2O_2 AlO_x thin films and ensure the authenticity of the measurement results, at least 5 devices of each H_2O_2 concentration were measured as shown in Figure 4-17 in Appendix. It is found that the C-V curves of 7.5 M H_2O_2 MOSCAPs had larger C_{max}, larger slope in the depletion region compared to others. The larger C_{max} corresponding to higher AlO_x metal oxide framework concentration. The slope of the C-V curves in the depletion region is related to the AlO_x/Si interface quality. The larger slope represents the enhanced interface quality with fewer interface traps.

Table 4-1. The properties of H_2O_2 AlO_x thin films and MOSCAPs with different H_2O_2 concentration

H_2O_2 concentration (M)	**Thickness (nm)**	**Leakage Current at 4 V (A/cm^2)**	**Areal Capacitance (nF/cm^2) at 1 kHz**	**Dielectric Constant at 1 kHz**
0	25.3	3.00×10^{-5}	207	6.29
2.5	24.7	1.24×10^{-5}	215	6.42
5.0	23.2	1.11×10^{-5}	234	6.56
7.5	22.5	3.16×10^{-6}	248	6.72
10	21.5	6.08×10^{-6}	237	6.23

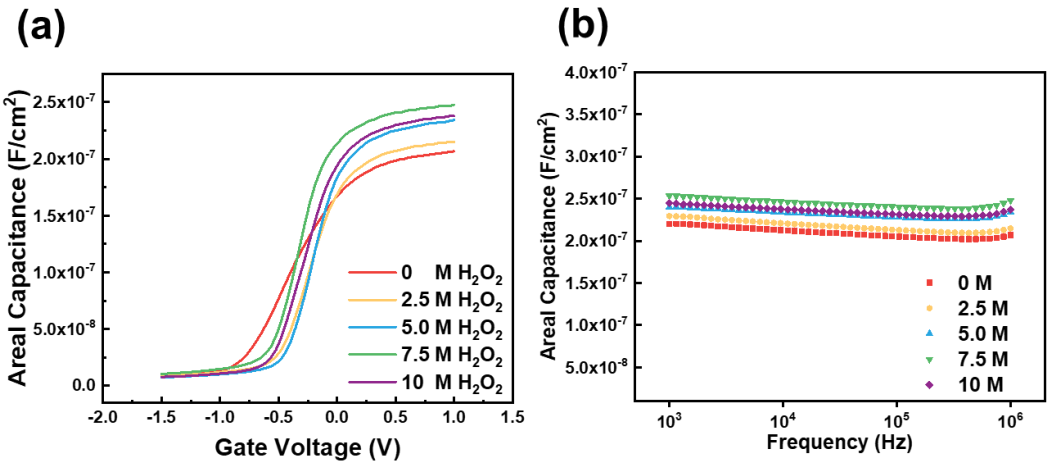

Figure 4-2. (a) C-V and **(b)** C-*f* plots curves of solution-processed AlO_x MOSCAPs with different H_2O_2 concentration (0 M, 2.5 M, 5.0 M, 7.5 M, 10 M).

The C-*f* characteristic of AlO_x MOSCAPs are demonstrated in Figure 4-2 (b). Corresponding to the C-V curves in Figure 4-2 (a), employing H_2O_2 increased the accumulation capacitance of AlO_x capacitors as well as the dielectric constant. The increased accumulation capacitance is mainly ascribed to the high percentage of AlO_x metal oxide framework and reduced precursor impurities. Furthermore, the devices showed a high value of capacitance at low-frequency operation and a low value of capacitance at high-frequency operation. In general, the capacitance of conventional dielectric films shows a constant value regardless of frequency. However, the solution-processed amorphous AlO_x dielectrics demonstrated frequency-dependent dielectric behaviors, like ion gel dielectric layers, which could be caused by the residual precursor impurities and defects among the thin film [16].

To determine the effect of H_2O_2 in reducing interface trap density of AlO_x MOSCAPs, C-V curves were carried out under measurement frequency (f_m) from 1 k-1 MHz, because higher f_m can only detect shallower interface states with higher characteristic interface trap frequency (f_{it}), thus higher V_G is required to pull down the conduction band at the interface. In other words, higher f_m results in larger flatband voltage (V_{FB}). The detectable energy of the interface traps (E_T) under different f_m can be determined by

$$E_T(f_m) = E_C - E_T = kTln(\frac{v_{th}\sigma_n N_c}{2\pi f_m}) \quad (4\text{-}4)$$

were k is the Boltzmann's constant, T is the measurement temperature, N_C = $2.8\times10^{19}cm^{-3}$ is the effective density of states in the conduction band of Si, σ_n =$1\times10^{-}$

^{14} cm^2 is the electron capture cross section, and v_{th}=2×10^7 $cm \cdot s^{-1}$ is the thermal velocity of electrons. The equivalent average energy level of the interface states (E_{AVG}) in the energy from $E_T(f_1)$ to $E_T(f_2)$ can be represented by:

$$E_{AVG} = \frac{E_T(f_1) + E_T(f_2)}{2} \tag{4-5}$$

In this way, D_{it}-E_t mapping can be realized from the *f*-dependence of voltage frequency dependent flatband voltage shift (ΔV_{FB}), according to (4-6) [17].

$$D_{it}(E = E_{AVG}) = \frac{C_{ox} \cdot \Delta V_{FB}}{q \Delta E_T} \tag{4-6}$$

Where C_{ox} is the areal capacitance of H_2O_2-AlO_x thin films and was extracted from the C-V curves measured at 1kHz to avoid the low frequency limit effect [18], ΔE_T is the interface trap frequency dependent energy difference, which can be calculated by:

$$\Delta E_T = E_T(f_1) - E_T(f_2) \tag{4-7}$$

As mentioned before, V_{FB} is obtained through measured C-V curves for a given ideal C_{FB}. C_{FB} is calculated through equation (2-2). Afterwards, the normalized C-V curves are shown in Figure 4-3, normalization is helpful to determine the flatband voltage shift (ΔV_{FB}) under different measurement frequency (f_m), ΔV_{FB} can be determined through:

$$\Delta V_{FB} = V_{FB}(f_1) - V_{FB}(f_2) \tag{4-8}$$

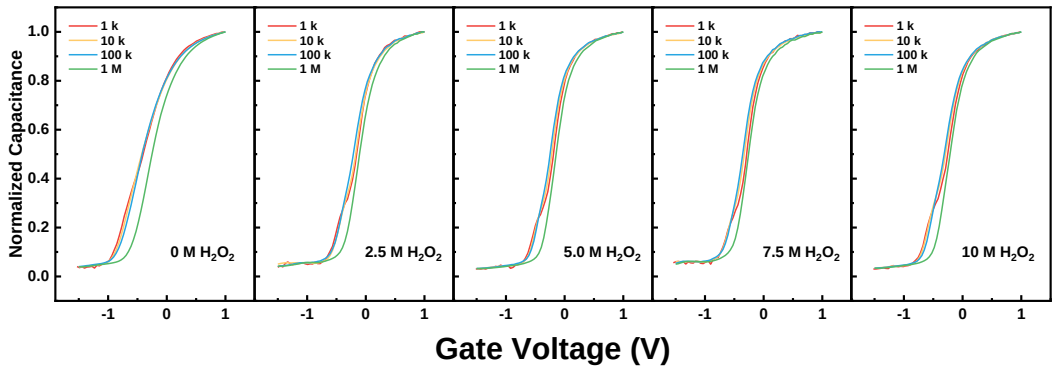

Figure 4-3. The normalized C-V curves measured under different frequency of H_2O_2 AlO_x MOSCAPs with different H_2O_2 concentration.

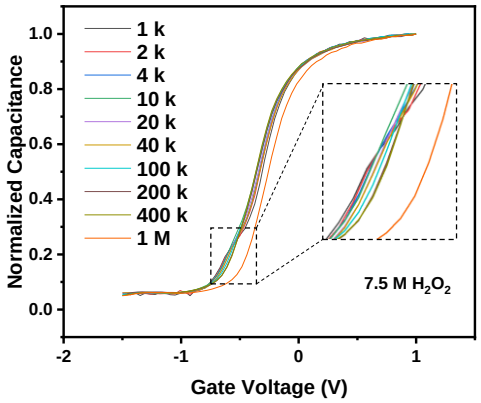

Figure 4-4. The C-V curves of H_2O_2 AlO_x MOSCAP with 7.5 M H_2O_2 concentration. The inset enlarged figure displays the C-V hump is low frequency measurement.

It is notable that there exist a C-V hump at low frequency (f_m < 10 k), which is a capacitance footprint of carrier interaction between interface states and semiconductor conduction band [19]. The C-V hump can serve as a qualitative interface quality indication for the devices with a similar dielectric capacitance. According to equations (4-6) to (4-8), the calculated D_{it} and the standard deviation of the D_{it} distribution of each sample is demonstrated in Figure 4-5 (a). As E_c-E_t increases, the energy level of

D_{it} is getting away from the bottom of conductance band, the D_{it} continuously decreasing. According to the disorder-induced gap state model, the acceptor-like and donor-like interface states having a U-shaped distribution between E_c and E_v of a semiconductor [20].

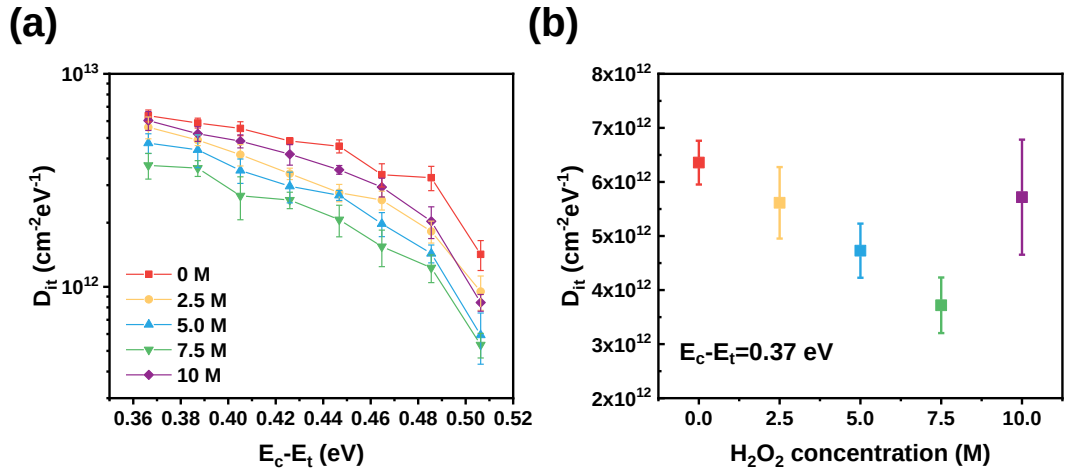

Figure 4-5. The calculated D_{it} and the standard deviation of the D_{it} distribution **(a)** in the E_c-E_t range of 0.37 eV to 0.534 eV, and **(b)** at the E_c-E_t= 0.37eV of H_2O_2 AlO_x MOSCAPs with different H_2O_2 concentration (0 M, 2.5 M, 5.0 M, 7.5 M, 10 M).

It is reported that the capture cross section of the interface traps varies from 1.4×10^{-15} cm^2 to 1.4×10^{-14} cm^2 when the traps energy level located from E_c-E_t = 0.24 V to 0.73 eV. In order to avoid underestimating the interface trap density, it is assumed that the electron capture cross section at the interface σ_n was1×10^{-14} cm^2 in this work, which gives the value of D_{it} in the energy level range from 0.37 eV to 0.51 eV from the conduction band edge. Figure 4-5. (b) displays the comparison of D_{it} at E_c-E_t=0.37 eV, with H_2O_2 concentration increasing from 0 M to 7.5 M, the D_{it} reduced from 6.35×10^{12} $cm^{-2}eV^{-1}$ to 3.72×10^{12} $cm^{-2}eV^{-1}$, the results are comparable to the value (2.2×10^{13} $cm^{-2}eV^{-1}$) calculated from high-*k* oxide MOSCAPs reported in [21]. However, as the H_2O_2

concentration increased to around 10 M, there is an increase of D_{it} from 3.72×10^{12} $cm^{-2}eV^{-1}$ to 5.72×10^{12} $cm^{-2}eV^{-1}$ compared to those calculated from devices with 7.5 M concentration. This phenomenon could be probably ascribed to the quickly condensation of precursor accompanied with O_2 releasing, caused by strong oxidation of H_2O_2 and lead to a rough semiconductor/oxide interface with increasing interface trap density [22].

The BS stability of AlO_x MOSCAPs were investigated under gate voltage stress (V_{GS_Stress}) = + 2 V and V_{GS_Stress}= - 2 V with stress time up to 1000 s. During the bias-stress reliability measurement, the C-V sweep voltage should not cause the degradation of the devices reliability and ensure the reliability degradation resulted by single bias-stress is extracted through the regularly C-V measurements. To single out the effects of C-V sweep measurement voltage on the device reliability degradation, multiple C-V sweeps up to 15 times were carried out in 46000 s, as shown in Figure 4-18 in Appendix. To ensure the authenticity of the measurement results, at least 3 devices of each H_2O_2 concentration were measured. The C-V results demonstrate that, for all samples, no obvious C-V curve shift or stretch out caused by C-V sweeping voltage are detected, representing the C-V sweeping voltage during the bias-stress measurement can barely cause the reliability degradation. Afterwards, the measured C-V curves during the PBS and NBS are shown in Figure 4-19 and Figure 4-20 in Appendix. The extracted ΔV_{FB} are demonstrated in Figure 4-6. As the H_2O_2 concentration increased, the BS stability is gradually improved.

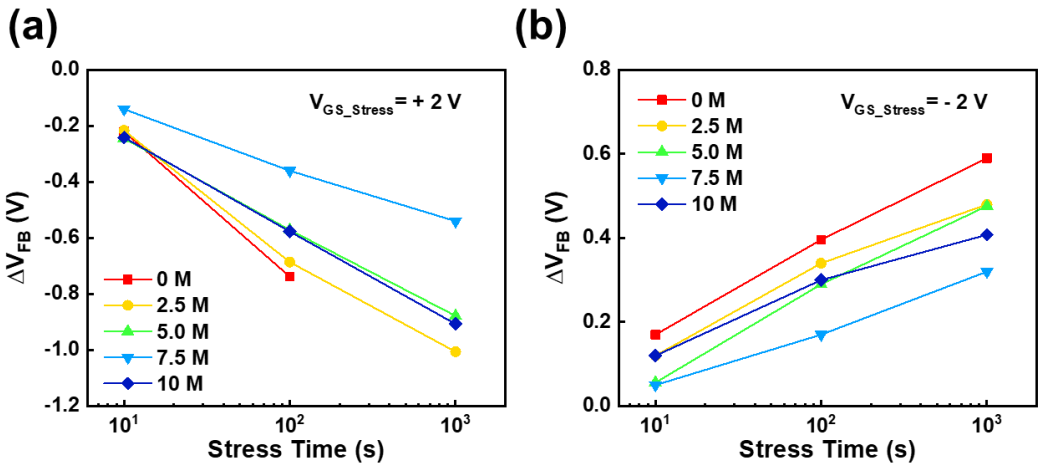

Figure 4-6. The ΔV_{FB} of AlO_x MOSCAPs extracted under **(a)** gate voltage stress (V_{GS_Stress}) = + 2 V and **(b)** V_{GS_Stress}= - 2 V with stress time up to 1000 s.

4.4 Mechanism of employing H_2O_2 in solution-process

H_2O_2 is a strong oxidant, which can oxidize a broad variety of inorganic and organic substrates in liquid-phase reactions under very mild reaction [23]. For solution-process, H_2O_2 is a suitable oxidizer, it is environmentally friendly since it decomposes to give only water and oxygen as the reaction products, which makes it one of the cleanest, most versatile chemical oxidants available. Owing to its low molecular weight, hydrogen peroxide is a more efficient oxidizing agent than other oxidants, as shown in **Table 4-2** [23].

Table 4-2. Common industrially oxidants available [23].

Oxidant	Active oxygen (% w/w)	By-product
H_2O_2	47.1	H_2O
*t*BuOOH	17.8	*t*BuOH
HNO_3	25.0	NO_x, N_2O, N_2
N_2O	36.4	N_2
NaClO	21.6	NaCl
$NaClO_2$	35.6	NaCl
NaBrO	13.4	NaBr
"$KHSO_5$"[a]	10.5	$KHSO_4$
$NaIO_4$	29.9[b]	NaI
PhIO	7.3	PhI

[a] Stabilized and marketed as the "triple salt" $2KHSO_5 \cdot KHSO_4 \cdot K_2SO_4$ (oxone).

[b] Assuming that all four oxygen atoms are used.

TGA-DSC curves of AlO_x precursor powder with 0 M and 7.5 M H_2O_2 are shown in Figure 4-7 (a) and (b), respectively. AlO_x thin films with 0 M and 7.5 M H_2O_2 concentration were selected for comparison, as AlO_x MOCAPs with 7.5 M H_2O_2 concentration have demonstrated the best device properties and BS stability in section 4.3. The formation of the thin film can be divided into three stages. The first stage was the decomposition of the precursor. At this stage, most of the chemicals were vaporized, precursors were decomposed and then hydrolyzed metals (M-OH, M, metal; O, oxygen; and H, hydrogen) were formed. The second stage was called the formation of the film. This stage began with a large exothermic reaction peak, as seen in the red lines in Figure 4-7. M-OH were converted to metal oxide (M-O) gradually to form film during this stage. The third stage followed the exothermic reaction peak and was called the densification of film. It can be found in Figure 4-7 (b) that the exothermic reaction peak

of precursor powder with H_2O_2 occurs at 120 °C, which was lower than the temperature (180 °C) of precursor powder without H_2O_2 in Figure 4-7 (a). This indicated the decomposition of impurities was accelerated, which could start at lower temperature: huge molecules broke down into tiny volatile molecules, such as oxygen, water, and carbon dioxide during the strong oxidizing reaction of H_2O_2 [24]. During this process, H_2O_2 was decomposed by pyrolysis, and hydroxyl radicals (OH•) were released through the stepwise reactions below.

$$H_2O_2 \rightarrow 2OH \quad (4\text{-}9)$$

$$OH + H_2O_2 \rightarrow HO_2 + H_2O \quad (4\text{-}10)$$

$$OH + HO_2 \rightarrow H_2O + O_2 \quad (4\text{-}11)$$

All reaction equations are based on related papers [22, 25]. Although hydroxyl radicals lived a very short time during reactions, they acted as a powerful oxidizer and could accelerate the decomposition of solvent residues because of a higher oxidation potential than H_2O_2. Besides, at 300 °C, the precursor powder 7.5 M H_2O_2 had around 30 % weight left, which was less than that (40 %) of precursor powder without H_2O_2, indicating more impurities were vaporized and decomposed during the annealing process. Consequently, adding H_2O_2 could form dense films with an increased percentage of AlO_x metal oxide and reduced defect sites at the specified annealing temperature.

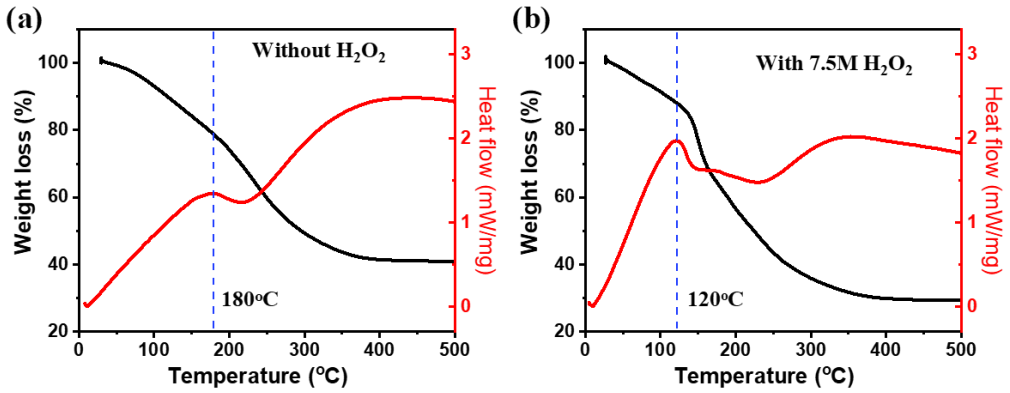

Figure 4-7. TGA curves of $Al(NO_3)_3$ precursor powder **(a)** with 0 M H_2O_2 and **(b)** with 7.5 M H_2O_2 heated from 20 to 500 °C with a heating rate of 10 °C/min.

In order to further explore the effects of employing H_2O_2 on the M-O lattice formation and impurity contents of AlO_x thin films, XPS spectra are performed in Figure 4-8 and all measured peaks were adjusted by C1s peaks of 284.5 eV. Figure 4-8 (a) shows the XPS survey scan of the AlO_x thin films and they reveal all the chemical elements it contains, namely Al, C, O, and Si. No peaks corresponding to impurities elements can be found, indicating that the solution-processed AlO_x thin films were fabricated as expected. The corresponding O 1s narrow scans are shown in Figure 4-8 (b), by applying Gaussian-Lorenz fitting method, the O1s peaks were deconvoluted into two peaks represent low bind energy (O_I, 530.9 eV) and high binding energy (O_{II}, 532.3 eV). The peak of O_I is connected to O^{2-} ions combined with Al ions. On the other hand, the peak of O_{II} is assigned to bonded oxygen, such as oxygen vacancy, hydroxyl groups, or absorbed H_2O on the film surface [22, 25]. The fraction of $[O_I/ (O_I + O_{II})]$ increased from 56.4 % to 68.1 % after adding H_2O_2, while the ratio of $[O_{II}/ (O_I + O_{II})]$ decreased

from 43.6% to 31.9 %. Obviously, the strong oxidizing reactions of H_2O_2 could form a metal oxide framework at a low temperature, and suppress the number of oxygen vacancies as well as other defects. The increased AlO_x metal oxide concentration, reduced oxygen vacancies, and M-OH content could diminish the trap state density, which improved the stability of integrated MOS devices accordingly.

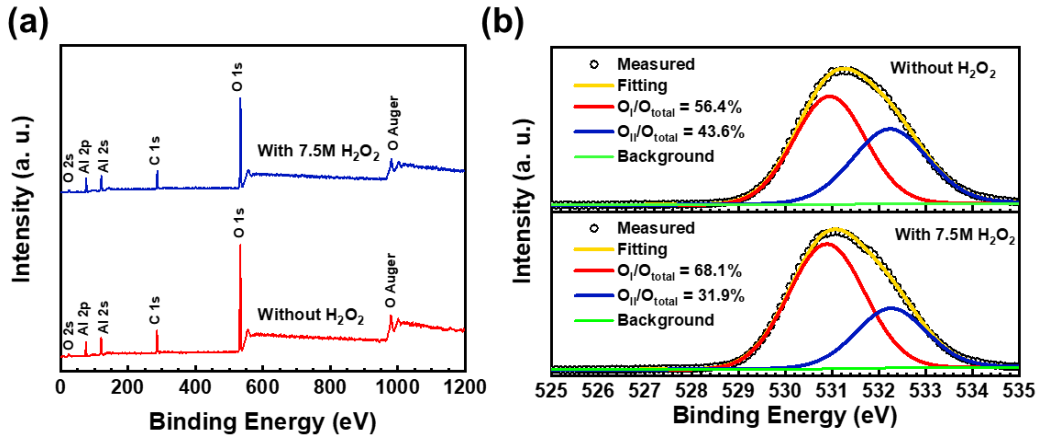

Figure 4-8. XPS spectra of **(a)** survey scans and **(b)** O 1s narrow scans of solution-processed AlO_x films.

4.5 Improved BRS stabilities of AlO_x devices by employing H_2O_2

To investigate the improved BRS stability of 7.5M H_2O_2-AlO_x thin films compared to 0 M H_2O_2 AlO_x thin films, the device response under radiation exposure with different bias stress voltage was investigated and analyzed systemically. Voltage bias was applied on the gate of devices during radiation exposure, as the applied electric field during radiation exposure is essential to investigate the radiation effect on devices

[21]. The BS stability is provided for comparison, in order to separate the biased radiation effect and bias-stress effect. Figure 4-9 display the original C-V curves of 7.5 M H_2O_2-AlO_x devices and 0 M H_2O_2 AlO_x devices under BS and BRS. Note, the radiation exposure was not interrupted when carrying out the C-V measurement during the BRS investigation. For radiation-exposure-only and NBRS, the stress time was 46000 s and the total dose was up to 42 Gy (SiO_2). However, under PBRS, the stress time was only 100 s and the total dose was up to 0.1 Gy. The reason is that the devices exhibited severe property degradation under PBRS corresponded to a large C-V shift and the stress time was shortened. It can be found in Figure 4-9 that BRS could barely lead to an additional C-V shift in the 7.5 M H_2O_2-AlO_x device compared to BS. However, 0 M H_2O_2 AlO_x exhibited BRS induced device degradation corresponding to a larger C-V shift, especially under NBRS. The C-V shifts in Figure 4-9 demonstrate that 7.5 M H_2O_2-AlO_x capacitors not only had improved BS stability, but also had satisfied BRS stability compared to 0 M H_2O_2 AlO_x capacitors.

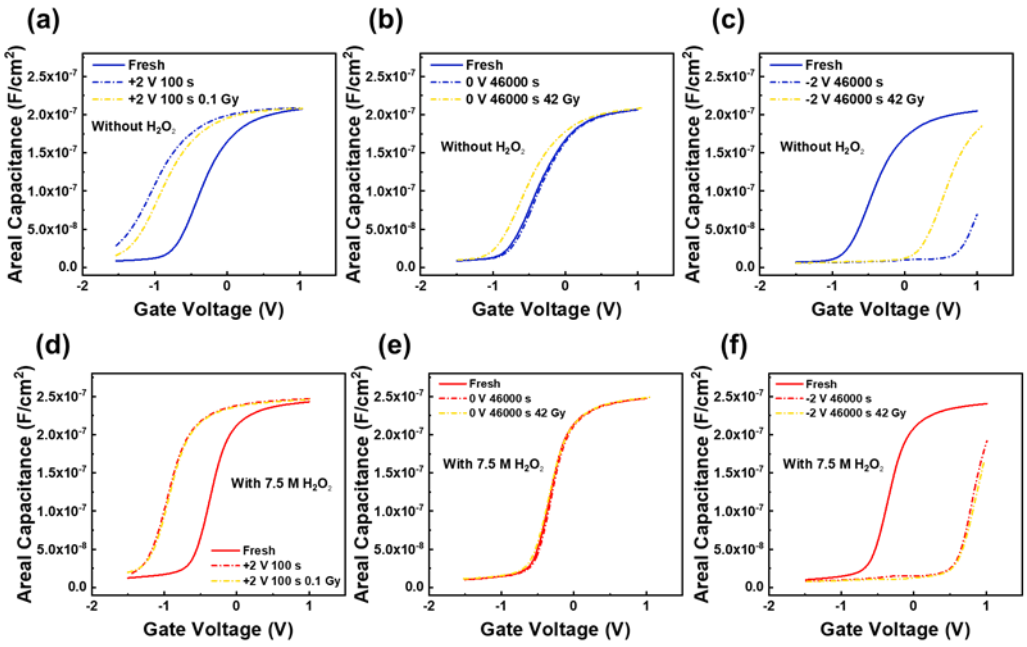

Figure 4-9. C-V curves of solution-processed AlO_x MOSCAPs under BRS conditions of **(a)** 0 V, 42 Gy (SiO_2), without H_2O_2, **(b)** +2.0 V, 0.1 Gy (SiO_2), without H_2O_2, **(c)** -2.5V, 42 Gy (SiO_2), without H_2O_2, **(d)** 0 V, 42 Gy (SiO_2), with 7.5 M H_2O_2, **(e)** +2.0 V, 0.1 Gy (SiO_2), with 7.5 M H_2O_2 and **(f)** -2.5V, 42 Gy (SiO_2), with 7.5 M H_2O_2.

To further investigate the BRS stability of 7.5 M H_2O_2-AlO_x and 0 M H_2O_2 AlO_x capacitors, the device degradation caused by radiation-exposure-only needs to be determined first. Consequently, ΔV_{FB} under No-Bias and radiation-exposure-only was calculated and summarized in Figure 4-10 (a). ΔV_{FB} of 7.5 M H_2O_2-AlO_x devices are represented in circular symbols and ΔV_{FB} of 0 M H_2O_2 AlO_x devices are represented in triangle symbols. The No-Bias results are represented by solid symbols, while the radiation-exposure-only results are represented by hollow symbols. It is observed in Figure 4-10 (a) that radiation could barely affect the ΔV_{FB} of 7.5 M H_2O_2-AlO_x

capacitors, while the 0 M H_2O_2 AlO_x capacitors suffered from the radiation caused degradation under radiation-exposure-only.

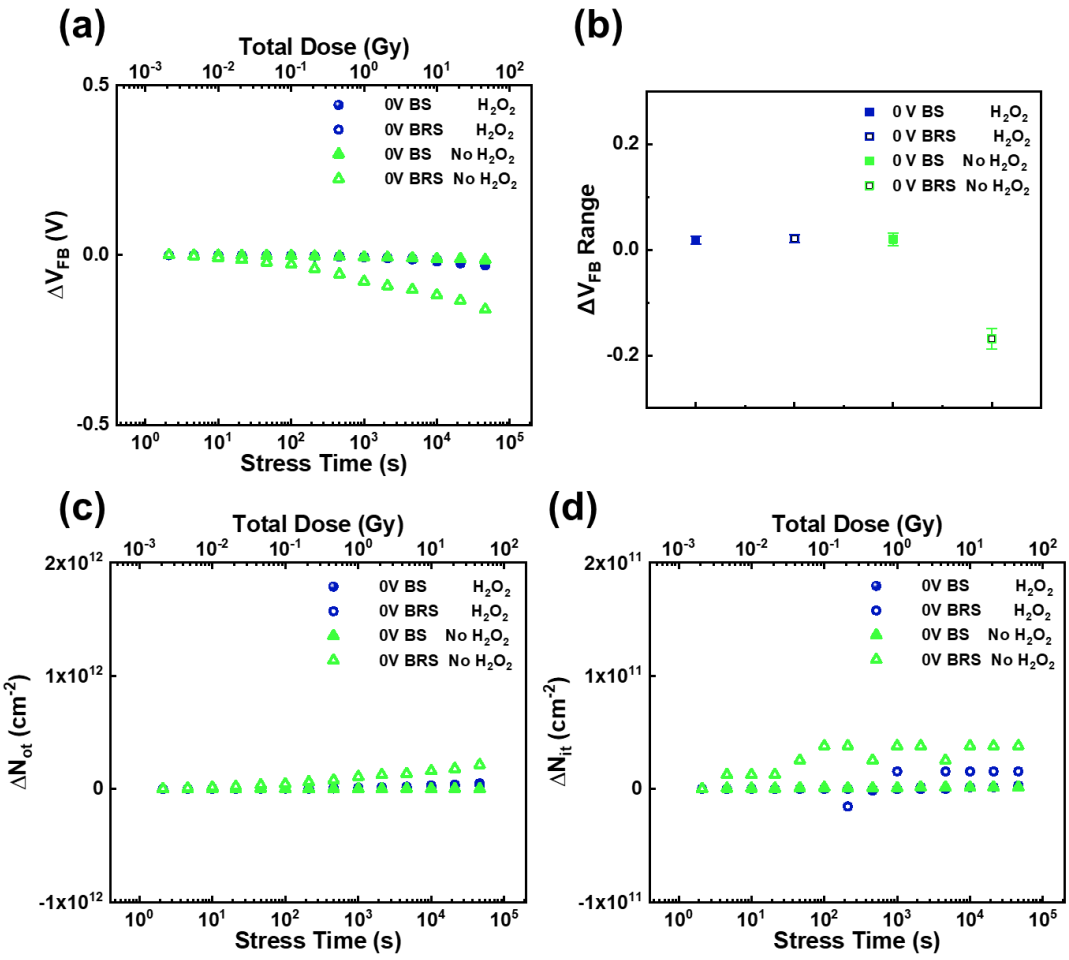

Figure 4-10. (a) ΔV_{FB}, **(b)** ΔV_{FB} distribution, **(c)** ΔN_{ot} and **(d)** ΔN_{it} of AlO_x MOSCAPs under No-Bias and under radiation-exposure-only .

Figure 4-10 (b) shows the distribution of ΔV_{FB} under No-Bias and under radiation-exposure-only, where ΔV_{FB} was calculated from C-V curves measured from at least 3 devices. It is known that ΔV_{FB} is the combined effect of ΔN_{ot} in AlO_x bulk and ΔN_{it} at

the AlO_x/Si interface. ΔN_{ot} causes the parallel shift of C-V curves, while ΔN_{it} influences the stretch-out of C-V curves. ΔN_{ot} can be estimated by equation (4-12) [26]:

$$\Delta N_{ot} = -\frac{C_{ox}\Delta V_{mg}}{qA} \tag{4-12}$$

where ΔV_{mg} is the mid-gap voltage shift obtained from C-V curves, C_{ox} is the gate capacitance, q is the electronic charge and A is the electrode area. ΔN_{it} was estimated by equation (4-13) [26]:

$$\Delta N_{it} = \frac{C_{ox}(\Delta V_{FB} - \Delta V_{mg})}{qA}. \tag{4-13}$$

The results in Figure 4-10 (c) indicate that radiation-exposure-only could barely generate additional oxide traps in 7.5 M H_2O_2-AlO_x capacitors compared to No-Bias. However, for 0 M H_2O_2 AlO_x devices, it is observed that radiation-exposure-only induced net positive oxide trapped charges. 0 M H_2O_2 AlO_x contained enormous numbers of V_o, which could act as defects and trap the radiation-induced holes or hydrogen among AlO_x bulk, leading to the increased positive ΔN_{ot}. As shown in Figure 4-10 (d), radiation-exposure-only generated ignorable additional interface traps compared to No-Bias for all devices.

Radiation could generate EHPs when passing through oxide [27]. It is reported that the EHPs would have no significant effect on devices without an applied electric field [28]. Therefore, the device response under PBRS and NBRS should be the focus when investigating the radiation hardness. Figure 4-11 (a) shows the ΔV_{FB} of all devices under PBS and PBRS. The time dependence of ΔV_{FB} under BS and BRS is in agreement with a stretched exponential equation, which can be expressed as [29]:

$$\Delta V_{FB} = \Delta V_{FB0}(1 - \exp(-\left(\frac{t}{\tau}\right)^{\beta}) \quad (4\text{-}14)$$

where ΔV_{FB0} is the ΔV_{FB} at infinite time, τ is the characteristic trapping time of carriers, and β is the stretched exponential exponent. The stretched-exponential time dependence model hypothesized the emission of trapped charges toward deep states in the bulk dielectric for long stress time ($t > \tau$) and large stress field. It is plausible that the amorphous structure of the gate dielectric will lend itself to an appreciable number of band-tail states which can act as transport states for the emitted lower energy trapped state charge [30], but the extent can be different depending on the materials or deposition condition of dielectric layers. The fitted lines are shown in Figure 4-11 and the fitted values are listed in Table 4-3 and Table 4-4, the time dependences of ΔV_{FB} are well fitted with a stretched exponential equation in all stress conditions. τ and β hardly depend on the bias-stress amplitude, but ΔV_{FB0} showed a strong dependence on bias stress voltages. This result is consistent with those from the literature [30, 31], where the value of ΔV_{FB0} is mainly determined by the bias stress amplitudes and interface qualities. It can be found that 7.5M H_2O_2 devices have larger τ than 0 M H_2O_2 devices, indicating the slower degradation under BS and BRS measurements.

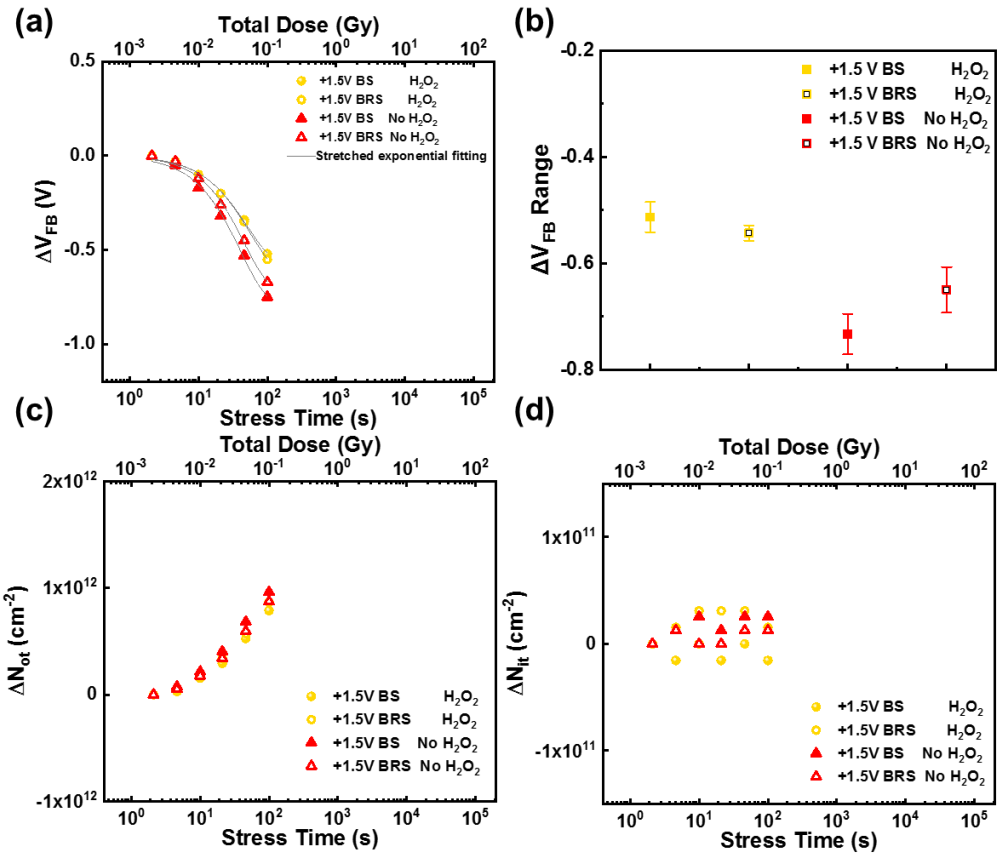

Figure 4-11. (a) ΔV_{FB} and stretched exponential fitting results, **(b)** ΔV_{FB} distribution, **(c)** ΔN_{ot} and **(d)** ΔN_{it} of AlO_x MOSCAPs under PBS and PBRS.

The distribution of ΔV_{FB} measured from at least 3 devices under PBS and PBRS is demonstrated in Figure 4-11 (b). After 100 s PBRS with a total dose of 0.1 Gy, the uniformity of all devices was not significantly affected. Figure 4-11 (c) and (d) display the ΔN_{ot} and ΔN_{it} of AlO_x MOSCAPs, respectively. It can be found in Figure 4-11 (a) that 7.5 M H_2O_2-AlO_x have no radiation-induced oxide traps or interface traps under PBRS. While PBRS could cause a more negative ΔV_{FB} of 0 M H_2O_2 AlO_x, corresponding to radiation-induced electron trapping in AlO_x bulk. The generation of radiation-induced interface traps was negligible for all devices. The reason is that the

generation of radiation-induced interface traps is related to the transport of radiation-induced holes and H^+. Interface trap buildup occurs on time frames much slower than oxide-trap charge buildup, it takes place over many decades in time [32]. As a result, the PBRS time (100 s) was too short to have a significant effect on interface trap density.

Table 4-3. Stretched exponential fitted values of AlO_x MOSCAPs under different BS conditions.

	Bias-stress (BS)			
	H_2O_2		**No H_2O_2**	
	+1.5 V	**-2 V**	**+1.5 V**	**-2 V**
ΔV_{FB0} (V)	-0.59 ± 0.16	1.47 ± 0.1	-0.73 ± 0.09	1.58 ± 0.07
τ (s)	51.4 ± 26.9	$(1.9 \pm 0.5) \times 10^4$	45.8 ± 11	$(3.1 \pm 0.8) \times 10^3$
β	1.08 ± 0.29	0.54 ± 0.02	1.08 ± 0.19	0.44 ± 0.03

As analyzed during the PBRS section, for 0 M H_2O_2 AlO_x, radiation could form negative oxide traps under PBRS, which was probably ascribed to the radiation-induced electron trapping in AlO_x bulk. This trapping behavior is highly sensitive to the electric field across the oxide during the radiation exposure and switching the polarity of the bias-stress voltage should prevent the radiation-induced electron trapping. As a result, the device degradation under NBRS was then investigated. ΔV_{FB} and distribution of ΔV_{FB} measured from at least 3 devices under NBS and NBRS is demonstrated in Figure 4-12 (a) and (b), respectively. For 7.5 M H_2O_2-AlO_x, neither radiation-induced

additional ΔV_{FB} nor uniformity degradation were observed under NBRS compared to NBS. It is observed in Figure 4-12 (a) that NBRS could not cause additional positive ΔV_{FB} compared to NBS, indicating electron trapping in AlO_x bulk dominate the device property degradation under PBRS, and this trapping behavior was suppressed under NBRS in a short time. However, as the NBRS time increased, it resulted in a negative ΔV_{FB} of 0 M H_2O_2 AlO_x, declaring that switching bias not only suppressed the radiation-induced electron trapping, but also lead to radiation-induced positive charges. However, NBRS did not deteriorate the uniformity of all devices. The time dependence of ΔV_{FB} under BRS was in agreement with a stretched exponential equation, the fitted lines are shown in Figure 4-12 (a) and the fitted values are listed in Table 4-3 and Table 4-4. 7.5 M H_2O_2 devices have longer τ than 0 M H_2O_2 devices, corresponding to good stability under NBRS. For further investigation, ΔN_{ot} and ΔN_{it} of AlO_x MOSCAPs were calculated in Figure 4-12 (c) and (d), respectively. No significant radiation-induced oxide traps or interface traps can be found in 7.5 M H_2O_2-AlO_x. While positive oxide traps and negative interface traps were generated under NBRS in 0 M H_2O_2 AlO_x. This could be ascribed to the breaking of Si-H bonds and AlO_x/Si interface, which contributes to an oxide trap (H^+) and an interface trap (Si^-) under NBRS, the detailed mechanism will be discussed with the assistance of energy band diagram later.

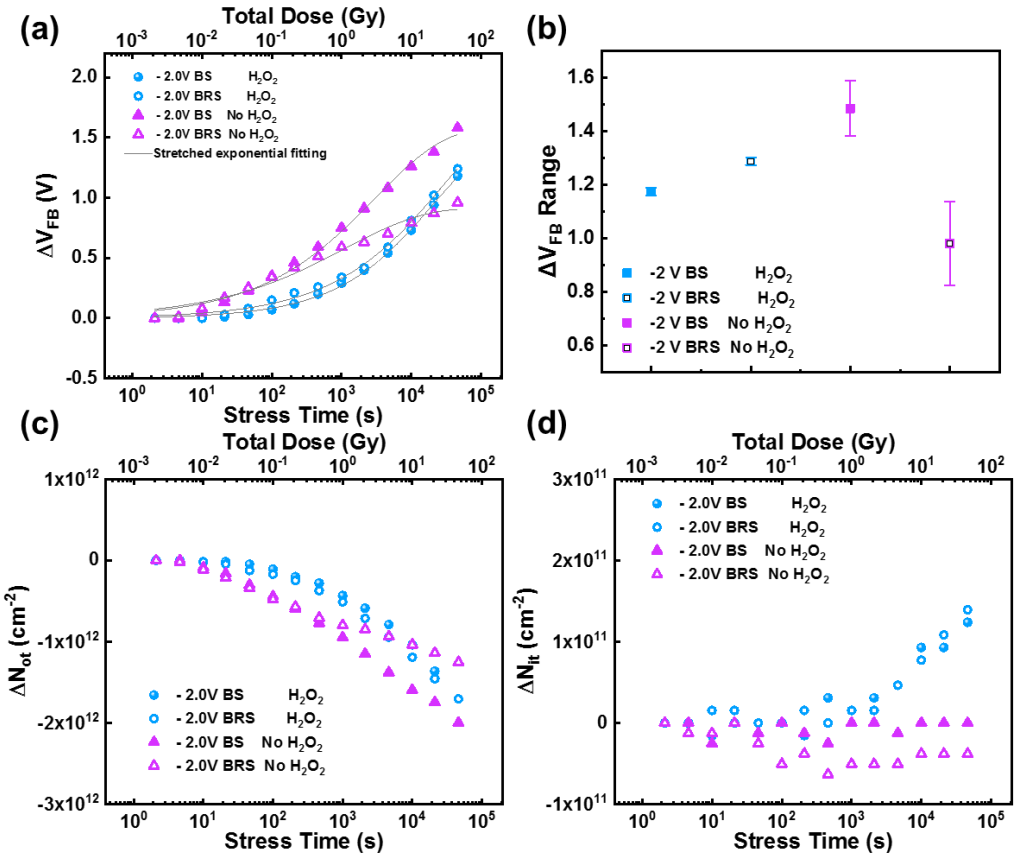

Figure 4-12. (a) ΔV_{FB} and stretched exponential fitting results, **(b)** ΔV_{FB} distribution, **(c)** ΔN_{ot} and **(d)** ΔN_{it} of AlO_x MOSCAPs under NBS and NBRS.

TGA and XPS results displayed in Figure 4-7 and Figure 4-8 indicate that adding H_2O_2 in solution-process could transfer M-OH into the M-O framework at low temperature and result in higher AlO_x metal oxide concentration in 7.5 M H_2O_2-AlO_x thin films than in 0 M H_2O_2 AlO_x thin films. In addition, H_2O_2 also suppressed the oxygen vacancy density, removed the precursor impurities, and enhanced the AlO_x/Si interface through its strong oxidation. The J-V and C-V results displayed in Figure 4-1 and Figure 4-2 further prove the improvement of employing H_2O_2. As a result, the BS and BRS stabilities of the devices were improved through adding H_2O_2.

Table 4-4. Stretched exponential fitted values of AlO_x MOSCAPs under different BRS conditions.

	Biased radiation stress (BRS)			
		H_2O_2		**No H_2O_2**
	+1.5 V	**-2 V**	**+1.5 V**	**-2 V**
ΔV_{FB0} (V)	-0.65 ± 0.14	1.74 ± 0.24	-0.81 ± 0.16	0.92 ± 0.06
τ (s)	56.3 ± 24.2	$(2.8 \pm 0.2) \times 10^4$	41 ± 17.5	$(1.1 \pm 0.5) \times 10^3$
β	1.08 ± 0.22	0.47 ± 0.03	1.1 ± 0.31	0.39 ± 0.05

According to these characterization results, the energy band diagrams of solution-processed AlO_x MOSCAPs under PBRS and NBRS can be displayed in Figure 4-13 (a) and (b), respectively. For 0 M H_2O_2 AlO_x capacitors, reduced positive ΔN_{ot} was observed under PBRS compared to PBS. The decreased positive ΔN_{ot} was probably ascribed to radiation-induced electron trapping (process (3) in Figure 4-13 (a)). Radiation exposure as well as electric bias could form neutral traps among the AlO_x bulk near the AlO_x/Si interface [33]. Meanwhile, electrons in the Si substrate accumulated near the AlO_x/Si interface under a positive applied electric field. Thereafter, those accumulated electrons could tunnel into the radiation generated traps and form negatively charged oxide traps, resulting in a reduced positive ΔN_{ot} [34, 35]. Besides, it is reported that V_o in oxide could significantly degrade the device hardness through acting as trapping sites [36]. From the XPS results and leakage behavior shown in Figure 4-8 (b) and Figure 4-1 (a), respectively, 0 M H_2O_2 AlO_x capacitors exhibited

higher defect density and larger leakage current compared to 7.5 M H_2O_2 AlO_x capacitors, which further verified that radiation-induced electron trapping dominated the generation of negative ΔN_{ot} observed in Figure 4-11 (c). Notably, as the radiation-induced electron trapping is sensitive to the polarity of the applied electric field, switching the bias polarity should significantly suppress this electron trapping behavior. As expected in Figure 4-12 (c), applying a negative bias-stress during radiation exposure leads to no radiation-induced negative oxide traps under the same stress with PBRS.

Unlike oxide traps, radiation had a negligible effect on the interface trap density under PBRS. The interface-trap buildup occurs on time frames much slower than the oxide-trap buildup because it is a two-stage process [32, 37], which is related to the transport of radiation-induced holes and H^+. During the first stage, EHPs are generated in AlO_x under radiation exposure (process (1) in Figure 4-13 (a)). With a positive applied electrical field, the electrons are sweep out of AlO_x thin film in picoseconds, while the holes are transported through AlO_x and trapped near the AlO_x/Si interface to form an oxide trap. The transportation is accompanied by the release of hydrogen, in the form of H^+ (process (2) in Figure 4-13 (a)). In the second stage, the released H^+ move towards the AlO_x/Si interface and passivate the Si^- (reaction (4-15)). Once a defect is passivated by hydrogen, it no longer functions as an interface trap.

$$Si^- + H^+ \rightarrow Si - H \tag{4-15}$$

The generation of radiation-induced interface traps are negligible for all devices. Interface trap buildup occurs on time frames much slower than oxide-trap charge buildup, it takes place over many decades in time [32]. The PBRS time was too short (100 s) to generate significant radiation-induced interface traps.

7.5 M H_2O_2 AlO_x capacitors have demonstrated improved radiation hardness under PBRS with ignorable radiation-induced ΔN_{ot} and ΔN_{it} compared to 0 M H_2O_2 AlO_x capacitors, which is likely due to the dense film with low defect density (V_o) and leakage current, as proved in XPS and J-V results shown in Figure 4-8 (b) and Figure 4-1 (a), respectively. The reduced number of V_o and high AlO_x concentration could suppress the radiation-induced electron trapping behavior. Thereby, the radiation hardness of AlO_x devices under PBRS was improved by employing H_2O_2.

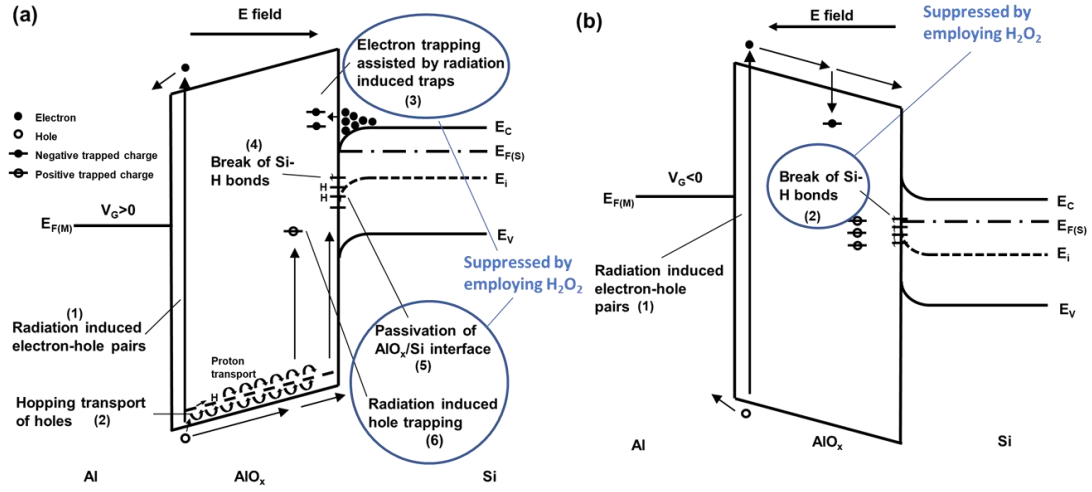

Figure 4-13. Energy band diagrams of solution-processed AlO_x MOSCAPs under **(a)** PBRS and **(b)** NBRS.

Under NBRS, for 0 M H_2O_2 AlO_x devices, negative ΔN_{ot} was found to be decreased in magnitude, while negative ΔN_{it} was produced. As shown in Figure 4-13 (b), under negative applied gate voltage, the radiation-induced electron tunneling from substrate and trapping among AlO_x bulk were suppressed. Instead, the breaking of Si-H bonds at the AlO_x/Si interface dominated the device radiation response, which could contribute to an interface trap (Si^-) and an available H^+ that can be trapped in AlO_x to serve as an oxide trap (reaction (4-16)) [38]. It has been demonstrated by density-functional-theory calculations that the simple thermally assisted Si-H bond breaking is highly improbable for a passivated interface dangling bond under normal device operating conditions, such as simply voltage bias-stress at room temperature [39]. However, the applied electric field combined with radiation exposure can reduce the binding energy of a Si-H bond [38]. There are some candidates that can facilitate the breaking of Si-H bonds, including the impurity Al atoms and suboxide bonds near the AlO_x/Si interface [40]. It has been proved that 0 M H_2O_2 AlO_x thin films contain a high concentration of metal hydroxide and a large density of oxygen vacancy. As a result, as the NBRS time increased, the breaking of Si-H bonds at the AlO_x/Si interface lead to the variations of ΔN_{ot} and ΔN_{it}.

$$Si - H \rightarrow Si^- + H^+ \tag{4-16}$$

On the other hand, 7.5 M H_2O_2 AlO_x capacitors had satisfied radiation hardness under NBRS, no additional radiation-induced ΔN_{ot} or ΔN_{it} could be found. The previous characterization results reveal that 7.5 M H_2O_2 AlO_x thin film contained

enhanced metal-oxygen lattice, reduced $V_{o,}$ and hydroxide species, indicating the amount of impurity Al atoms and suboxide bonds were reduced. The first-principle Hartree-Fock calculation [41] shows that the hydrogen bonding energy increases when the Si–O–Si angle reduces. For thinner and denser oxides, the Si–O–Si bond can be less stretched, which leads to a stronger hydrogen bond. Similarly, for thinner and denser AlO_x thin films, the breaking of Si-H bonds could be suppressed. Besides, the improved film quality with reduced defect density limited the radiation-induced trapping/de-trapping behaviors in 7.5 M H_2O_2 AlO_x devices. Consequently, the radiation hardness of 7.5 M H_2O_2 AlO_x capacitors under NBRS was improved accordingly.

To further verify the radiation induced damage under NBRS, negative biased-illumination stress (NBIS) was performed. As the photon emitted by the LED has very low photon energy (~2.73 eV with $\lambda \approx 455$ nm) compared to the energy (662 keV) of photon emitted by Cs^{137} γ-ray radiation source used in this work. The Si-H bonds at Si/AlO_x interface should not be broke by the incident light and lead to the formation of positive oxide traps. ΔV_{FB} and the distribution of ΔV_{FB} measured from at least 3 devices under NBS and NBRS is demonstrated in Figure 4-14 (a) and (b), respectively. As expected, both of 7.5 M H_2O_2 AlO_x and 0 M H_2O_2 AlO_x exhibited NBIS induced positive shift.

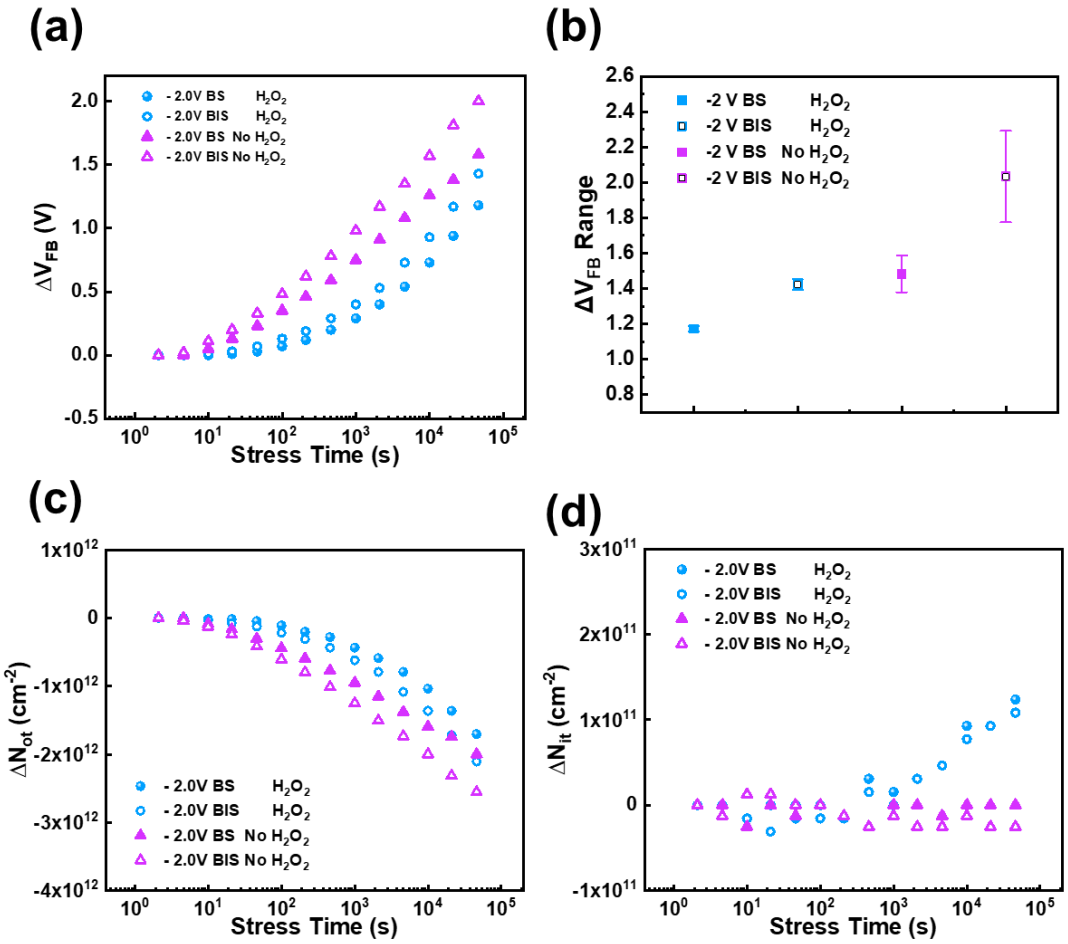

Figure 4-14. (a) ΔV_{FB} and stretched exponential fitting results, **(b)** ΔV_{FB} distribution, **(c)** ΔN_{ot} and **(d)** ΔN_{it} of AlO_x MOSCAPs under NBS and negative biased-illumination stress (NBIS).

For further investigation, ΔN_{ot} and ΔN_{it} of AlO_x MOSCAPs are shown in Figure 4-14 (c) and (d), respectively. The results are different from those measured under NBRS, the NBIS couldn't lead to the formation of positive oxide traps. In opposite, more negative oxide traps were induced. Besides, BIS had a negligible effect on the interface trap density.

The generation of negative oxide traps was related to the enhanced electron trapping under NBIS. It is known that illumination causes the transition of neutral V_o to V_o^{1+} or V_o^{2+} through reaction (4-17) and (4-18), respectively.

$$V_o \rightarrow V_o^{1+} + e^- \quad (4\text{-}17)$$

$$V_o \rightarrow V_o^{2+} + 2e^- \quad (4\text{-}18)$$

V_o is a non-conducting deep state and the excited V_o^{2+} state donates two delocalized free electrons [42]. The electrons transported towards the AlO_x/Si interface under a negative applied electrical field and some fraction of them tunneled into Si substrate. The applied electrical field could decrease this thermal barrier [43, 44] and let V_o^{2+} trap the electrons injected from the gate under the negative applied electrical field, leading to an increase in trapped electron density.

As the voltage bias during the radiation exposure facilitated the motion of radiation-induced EHPs and thus degraded the device properties severely. The recovery behavior of the device under radiation exposure after the bias-stress was removed is a crucial issue to be investigated. Figure 4-15 display the recover behavior of the devices under BS and BRS. The BS and BRS induced degradation involved two components, a permanent (fixed) component, which was not decreased after stress removal, and reversible component, which followed dynamically the applied stress bias. The devices recovered quickly when the bias-stress voltage was interrupted, demonstrating a self-healing ability. However, compared to the recover behavior under BS, BRS still induced permanent damage to all devices.

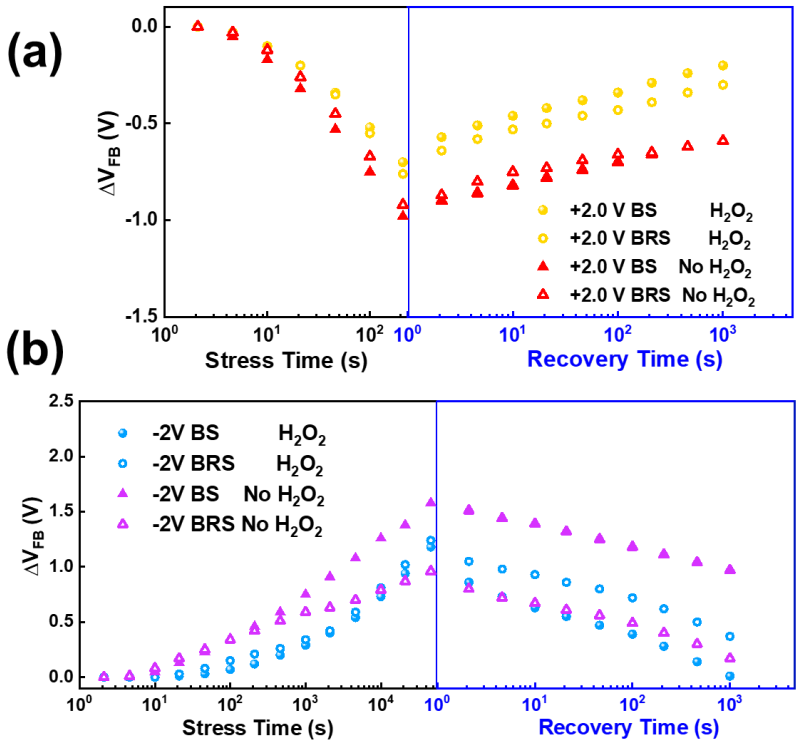

Figure 4-15. ΔV_{FB} recovery characteristics of solution-processed AlO_x MOSCAPs after **(a)** PBS & PBRS and **(b)** NBS & NBRS.

To better estimate the spontaneous recovery behavior of the MOSCAPs at room temperature, the fading characteristic is important [45]. The percent fading value can be calculated from [46]:

$$f = \frac{V_{FB}(0) - V_{FB}(t)}{V_{FB}(0) - V_{FB}} \times 100\% \quad (4\text{-}19)$$

where V_{FB} is the fresh flat band voltage, $V_{FB}(0)$ is the flat band voltage immediately after bias, and $V_{FB}(t)$ is the flat band voltage after annealing time t. The fading values of 7.5 M H_2O_2 AlO_x and 0 M H_2O_2 AlO_x thin films after BS and BRS are shown in Figure 4-16. It can be found that fading values were decreased under BRS compared to BS, except for the 0 M H_2O_2 AlO_x device under NBRS, it even increased after NBRS.

The recovery of the device was related to the annealing of radiation-induced oxide traps, which was probably ascribed to that interface traps annealing requires high temperature [47]. The decreased fading values suggested that BRS induced oxide traps that cannot be annealed and lead to permanent damage to AlO_x thin films. The abnormal high fading value of the 0 M H_2O_2 AlO_x device under NBRS was probably ascribed to the radiation-induced numerous oxide traps (H^+), as investigated in Figure 4-13 (b). Generally, the neutralization of oxide trapped charge occurs primarily by one of two mechanisms: 1) the tunneling of electrons from the silicon into either oxide traps [48] or electron traps associated with trapped holes [49], and/or 2) the thermal emission of electrons from the oxide valence band into oxide traps [50]. The increased oxide traps density leads to increased oxide trap neutralization possibility, increased recovery rate, and increased fading values. For the 0 M H_2O_2 AlO_x device under NBRS, it should be noted that there existed compensation between the bias-stress effect and radiation effect. The radiation-induced positive oxide traps that cannot be annealed could neutralize those bias-induced trapped electrons and lead to the abnormal large fading value 0 M H_2O_2 AlO_x device under NBRS.

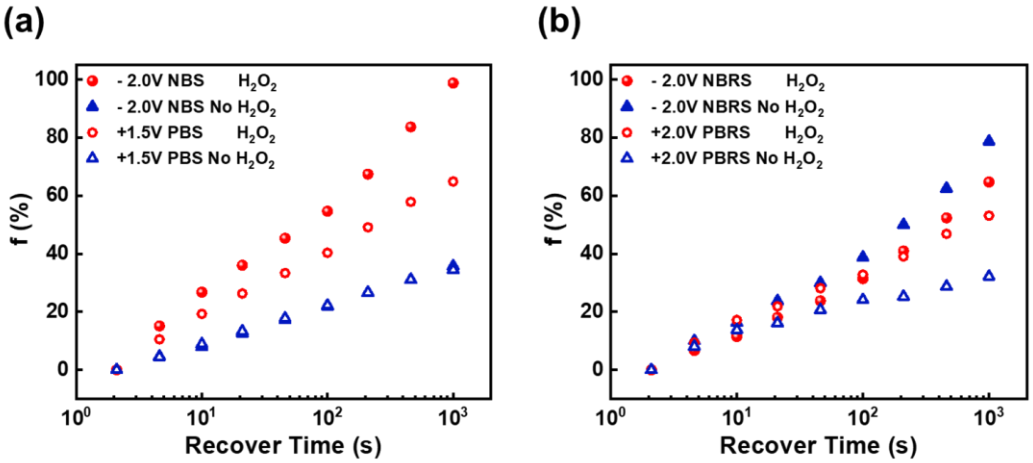

Figure 4-16. Percent fading values of solution-processed AlO_x MOSCAPs after different **(a)** BS and **(b)** BRS conditions.

4.6 Summary

The method to lower the annealing temperature and improve the BS and BRS stabilities of solution-processed AlO_x was explored. H_2O_2 was employed in the precursor solution as a strong oxidizer. In addition, H_2O_2 suppressed the oxygen vacancy density, removed the precursor impurities, and enhanced the AlO_x/Si interface through its strong oxidation at low temperature. The J-V and C-V results further proved the enhancement of employing H_2O_2. In addition, the reliabilities of the devices were improved by adding H_2O_2. 7.5 M H_2O_2 AlO_x devices had demonstrated enhanced BS and BRS stabilities with stress time up to 46000 s and total dose up to 42 Gy (SiO_2). When the devices were under BRS, H_2O_2 could suppressed the transportation & reaction of hydrogen (e.g. breaking of Si-H bond), the electron trapping into radiation generated neutral traps and the V_o among AlO_x bulk. ΔN_{it} was insignificant compared

to ΔN_{ot}, which was ascribed to that interface trap buildup occurs on time frames much slower than oxide-trap charge buildup. The degradation involved a permanent (fixed) component and reversible component. It is found that BRS could result in permanent damage to all devices, 7.5 M H_2O_2-AlO_x devices exhibited stronger recoverability than those without H_2O_2. The results in this chapter indicated that employing H_2O_2 in solution-process had significant potential to improve the BS and BRS stabilities of large area electronics applied for the nuclear environment and display area.

4.7 Appendix

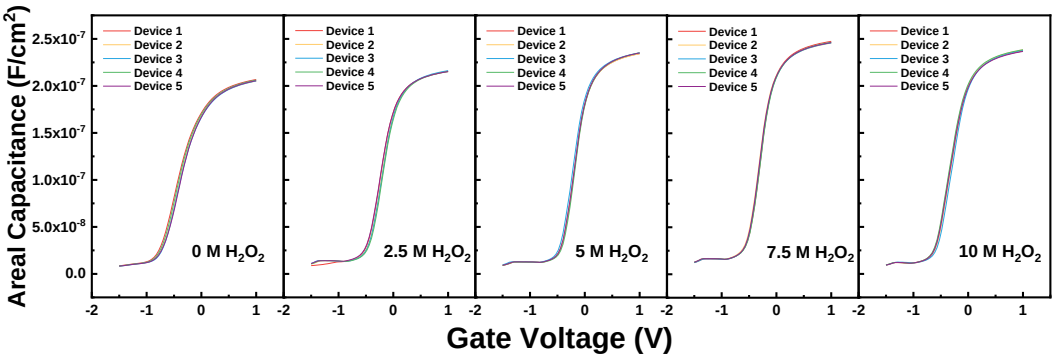

Figure 4-17. The distributions of C-V curves measured from at least 5 AlO_x MOSCAPs with different H_2O_2 concentration (0 M, 2.5 M, 5.0 M, 7.5 M, 10 M).

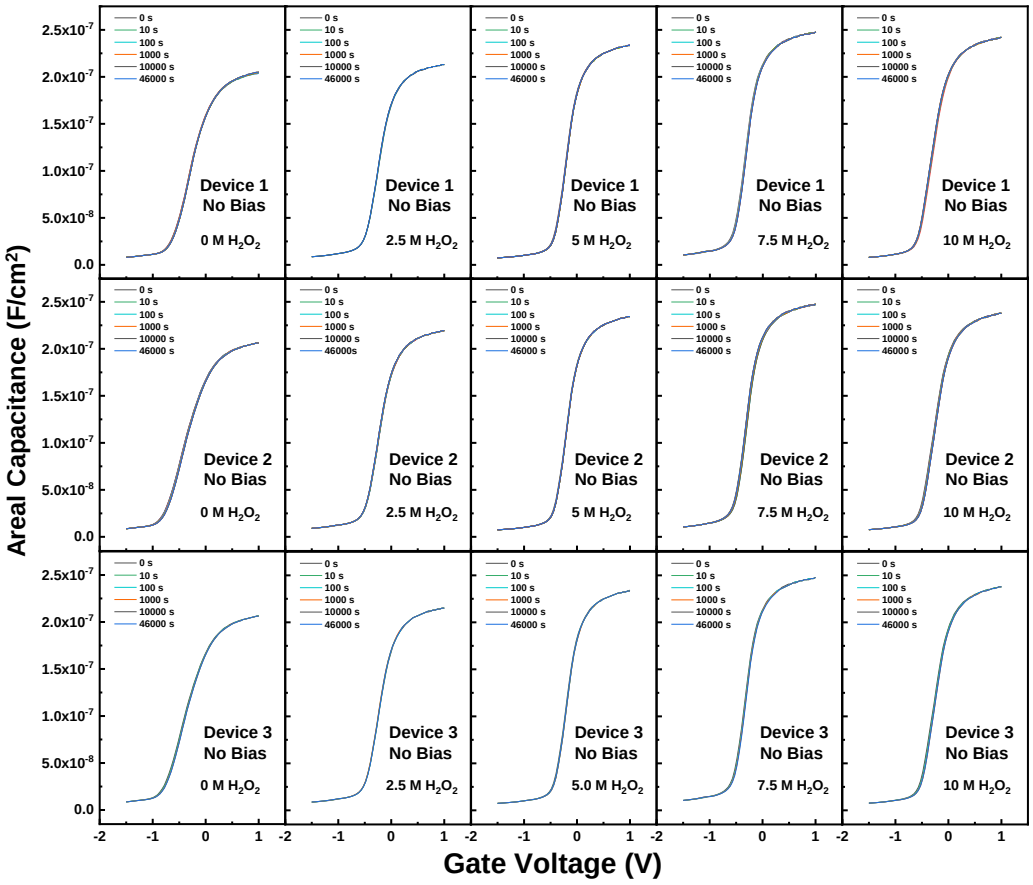

Figure 4-18. The C-V curves measured in 46000 s with no voltage bias applied on the gate of H_2O_2 AlO_x MOSCAPs with different H_2O_2 concentration (0 M, 2.5 M, 5.0 M, 7.5 M, 10 M).

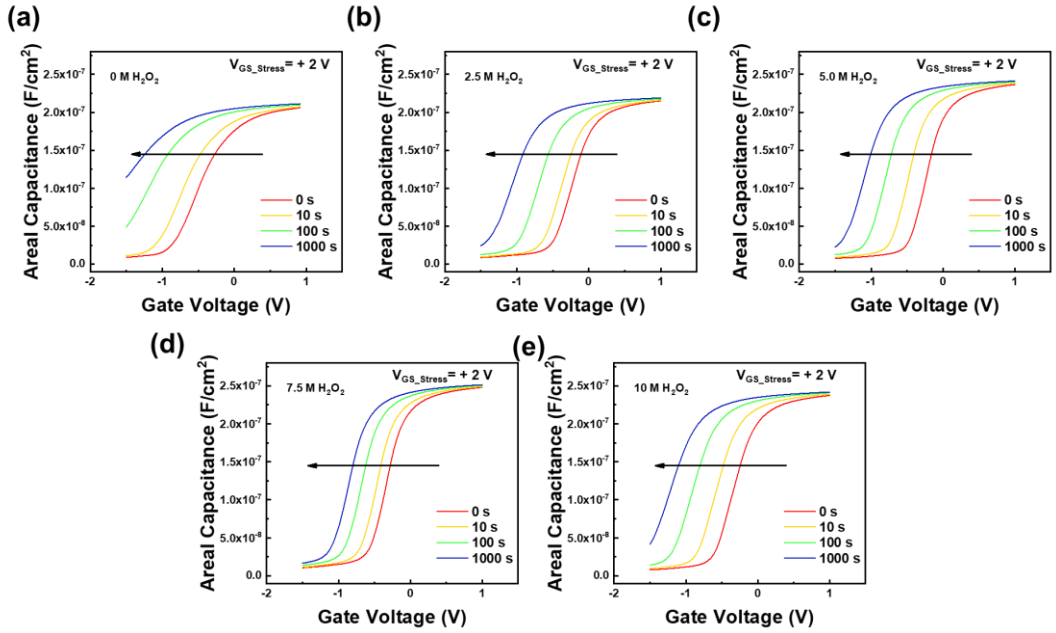

Figure 4-19. The C-V curves measured with bias stress time up to 1000 s under V_{GS_Stress}= + 2 V.

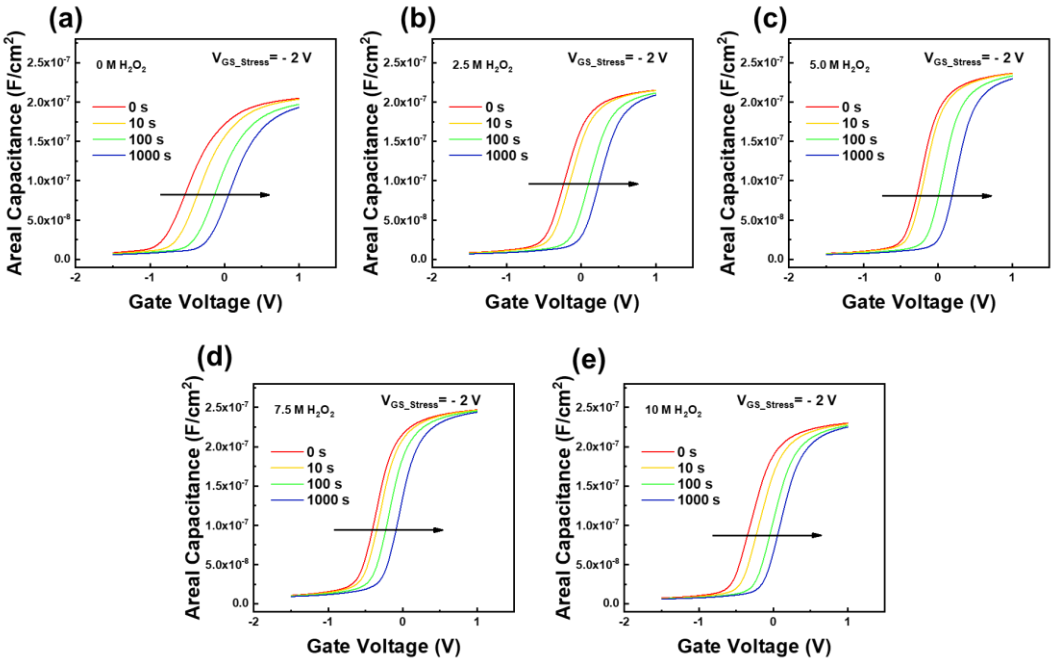

Figure 4-20. The C-V curves measured with bias stress time up to 1000 s under V_{GS_Stress}= - 2 V.

4.8 References

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Chapter 5: Nontoxic, eco-friendly fully water-induced ternary ZrLaO dielectric for high-performance transistors and unipolar inverters

5.1 Introduction

For portable and battery-powered applications, there has been an increasing interest in incorporating high-*k* dielectrics into devices to reduce the power consumption of the TFT devices [1] [2]. ZrO_2 has been regarded as a potential candidate for oxide-based TFTs due to its relatively low interface trap density, high dielectric constants (~ 22), and suitable band alignment [3-6]. Besides, La_2O_3 has attracted much attention in recent years due to its high-*k* value (~ 27), large band gap (5.8~6.0 eV), high breakdown field, good thermodynamic stability, and good high-field reliability on Si [7-10]. Nevertheless, ZrO_2 crystallizes at relatively low annealing temperatures (~500 °C), which results in undesirable grain boundary formation, and La_2O_3 suffers from water and carbonate absorption [11-13], both of which result in increased leakage currents and poor device properties [14].

Fortunately, it has been reported that rare earth (RE)-based ternary oxide as gate dielectric can improve the TFT performance by suppressing the moisture absorption of the RE binary oxide [15, 16]. By combining the Zr and La components into ternary zirconium lanthanum oxides (ZrLaO), it may be possible to take advantage of the

inherent properties of Zr and La while suppressing crystallization and eliminating carbonate and water absorption. Previous research showed that an ideal dopant requires a low standard electrode potential (SEP), low electronegativity, and strong dopant–oxygen bond [17, 18]. Zr has a SEP of -1.45 V, electronegativity of 1.3, and bond dissociation energy of 766 kJ mol^{-1} [17]. Compared to Zr, La is an ideal dopant due to its lower SEP (−2.37 V), lower electronegativity (1.1), higher bond dissociation energy (798 kJ mol^{-1}) with O [19], and La can effectively combine with O and reduce the V_o in ZrO_2 thin films. Consequently, modification of Zr-based oxide dielectric via a small amount of La has been proven to increase permittivity, reduce the defect states, and suppress oxygen vacancies [20, 21].

Radiation damage to the dielectric materials has been regarded as a major device degradation issue for conventional devices fabricated by vacuum methods. Nevertheless, to the best of our knowledge, there have been only a few studies addressing radiation damage to solution-processed high-*k* metal oxides and devices [22]. Considering solution-process is a promising method for large-area applications, it is critical to attaining an understanding of solution-processed device failures in a harsh space environment and the development of rad-hard devices, such as large-area antenna arrays, whole-body-scanning X-ray detectors, and artificial skin on robots designed to operate in space. Generally, oxygen vacancies are the key and responsible reason for the radiation-induced degradation in high-*k* oxides, which could lead to increased electron concentration [22]. Investigation on Al_2O_3 deposited by ALD has shown that

the gamma irradiation on thin-film resulted in significant oxygen vacancy generation and the barrier height reduction [23].

In this chapter, an in-depth investigation was performed to reveal the effects of La composition on the electrical properties of the solution-processed ZrLaO thin films and WI InO_x/ZrLaO TFTs fabricated at 350 ºC. To verify the potential of ZrLaO thin film as the gate dielectric in CMOS logic circuits, their BS stability was investigated and their applications in resistor-loaded inverters were also demonstrated. In addition, the ambient air stability and the radiation hardness of ZrLaO thin films were investigated.

5.2 Experimental details

As shown in Figure 5-1, a 2.00 M (total metal, Zr: La=10:0, 9:1 and 8:2) ZrLaO precursor solution was prepared by dissolving zirconium oxynitrate hydrate ($ZrO(NO_3)_2 \cdot xH_2O$, 99.5 %) in DI H_2O by gentle heating (~70 °C) and vigorous stirring of the solution. After complete dissolution, lanthanum nitrate hexahydrate ($LaN_3O_9 \cdot 6H_2O$, 99.9 %) was added in small portions to the still stirring solution. The InO precursor solution was prepared by dissolving 0.1 M indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$, Aladdin) in DI water and vigorous stirred at room temperature for 8 h. All precursor solution was then filtered through a 0.2 μm PTFE syringe filter before spinning coating.

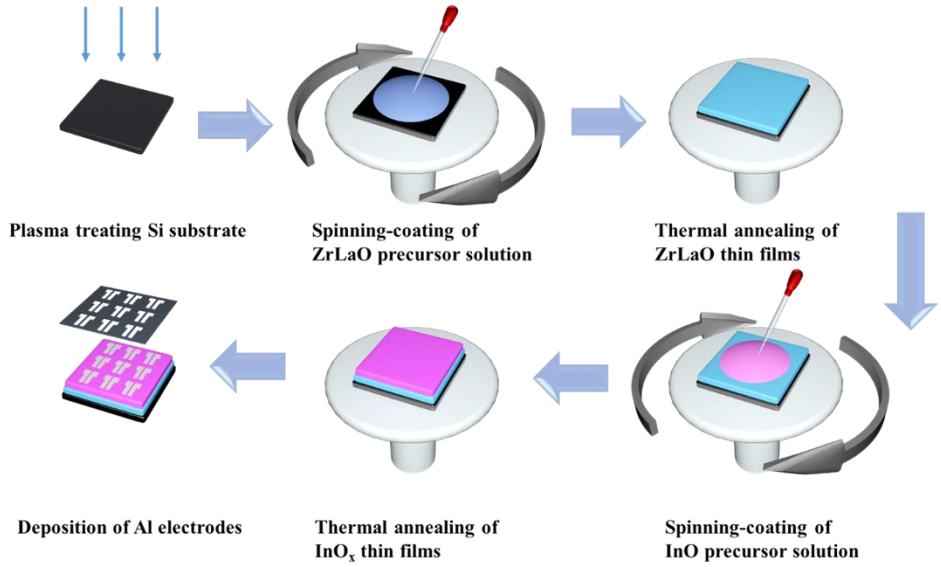


Figure 5-1. Schematic fabrication process of solution-processed water-induced (WI) thin film transistors (TFT).

Heavily doped n type Si substrates were selected for MIM and TFT devices. For MOS devices, lightly doped n type Si substrates (doping concentration: ~10^{15} cm^{-3}, resistivity: 2-4 Ω·cm) were utilized. All Si substrates were dipped in 2% HF aqueous solution for 60 s to remove the native oxide and then dried by N_2. Ten drops of ZrLaO precursor solution were deposited onto cleaned Si substrates and then immediately spun at 3000 rpm for 30 s. Samples were directly transferred to a hot plate set to 125 °C and ramped to a final annealing temperature of 350 °C at a rate of 25 °C min^{-1} and held for 1 h. Then ten drops of $In(NO)_3$ precursor solution were deposited onto the deposited ZrLaO thin films and immediately spun at 3000 rpm for 20 s. After that, the samples were heated on a hot plate at 250 °C for 1h. Finally, 300 nm thick Al top and bottom electrodes were deposited through shadow masks by e-beam evaporation. The ratio of channel width (W = 150 μm) and length (L = 10 μm) was defined as 15 to avoid the

overestimation of the field-effect mobility of the TFTs. If W/L is less than 10, it could lead to the underestimation of the effective channel width and lead to a factor of 10 overestimation of the mobility [24].Precursor and thin film properties

5.3 Precursor and thin film properties

TGA-DSC was used to examine the decomposition pathways of dried precursors powders to their corresponding oxides, as shown in Figure 5-2. The formation of the thin film can be divided into three stages [25]. The first stage was the decomposition of the precursor. At this stage, most of the chemicals were vaporized, precursors were decomposed and then hydrolyzed metals (M-OH, M, metal; O, oxygen; and H, hydrogen) were formed. The second stage is called the formation of the film. This stage began with a large exothermic reaction peak, as seen in Figure 5-2 (b). M-OH were converted to metal oxide (M-O) gradually to form film during this stage. The third stage followed the exothermic reaction peak and was called the densification of film. It can be found in Figure 5-2 (a) that Zr-only and $Zr_{0.9}La_{0.1}O_y$ precursor powders lose more weight at 350 ^oC compared to $Zr_{0.8}La_{0.2}O_y$ precursor powder, indicating more precursor were decomposed and more solvent was vaporized. In Figure 5-2 (b), it is observed that the large exothermic reaction peak temperature of the precursor powders increased with increasing La concentration. The lower decomposition temperatures for $ZrO(NO_3)_2$ were related to the higher charge density of Zr^{4+} relative to La^{3+}, which polarizes nitrate ions and weakens the strength of the N-O bond [26]. As a result, to fabricate high-

quality solution-processed ZrLaO thin films, the La concentration should be appropriate (< 20 %) to enable the transformation of precursor to metal oxide at low temperature. The $Zr_{0.9}La_{0.1}O_y$ precursor has demonstrated decomposition, transformation, and condensation processes similar to Zr-only precursor, which improved the thin film properties through La doping, ensured the oxide condensation and densification at low temperature at the same time.

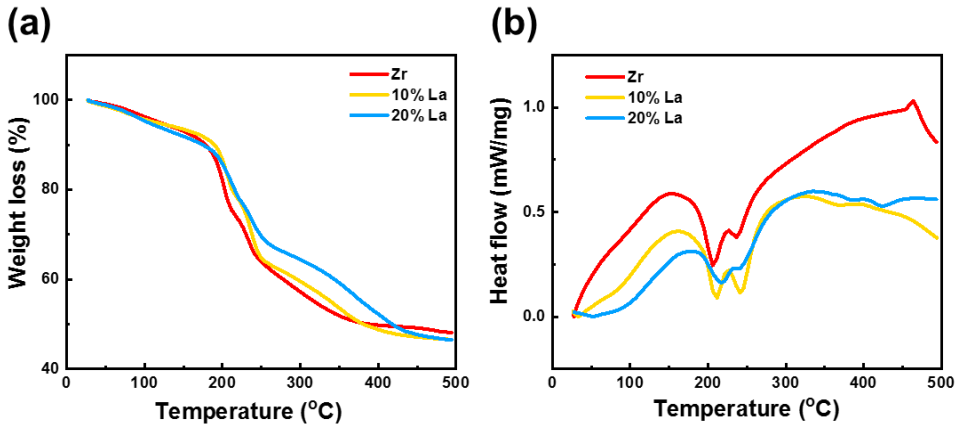


Figure 5-2. (a) TGA and **(b)** DSC curves of ZrLaO precursor powders with different La concentrations (0%, 10%, and 20% La).

Figure 5-3 demonstrates the atomic force microscopy (AFM) images of WI ZrLaO thin films with different La incorporation. The calculated root-mean-square (RMS) surface roughness of Zr-only, $Zr_{0.1}La_{0.9}O_y$, and $Zr_{0.2}La_{0.8}O_y$ thin films are 0.195, 0.133, and 0.141 nm, respectively. The small RMS value is not only related to the amorphous structure of ZrLaO thin films, but also to the utilization of organic free DI water as precursor solvent [27]. For organic-solvent-processed gate dielectrics reported, annealing induces the release of a large amount of volatile gases from the existed

organic ligands and generates nanopores in the dielectric thin films, which leads to the increased surface roughness and the degraded TFTs performance. A smooth surface is beneficial for charge-carrier transportation in semiconductors because a rough interface could induce physical traps or disturb the growth of channel layers. Besides, the leakage current could be effectively suppressed through smooth surface morphology and amorphous structure of the ZrLaO thin films. Consequently, the high-performance TFTs with higher mobility and smaller subthreshold swing (SS) value could be obtained.

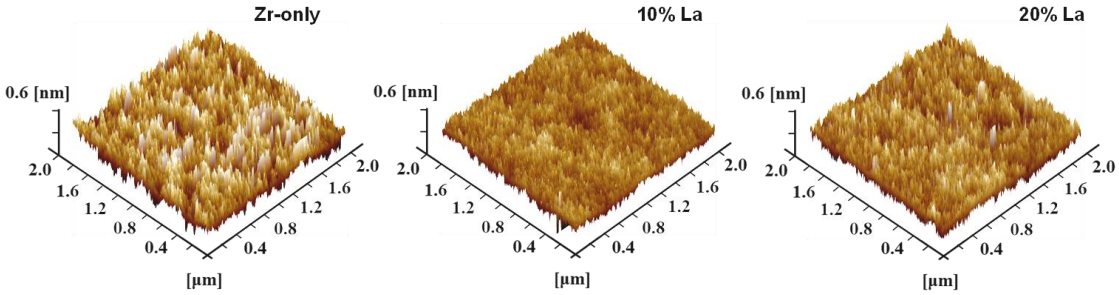


Figure 5-3. 3D Atomic force microscopy (AFM) images of **(a)** Zr-only, **(b)** $Zr_{0.9}La_{0.1}O_y$, **(c)** $Zr_{0.8}La_{0.2}O_y$ thin films.

To understand the mechanism of the film improvement as a function of La content, the survey spectra and the chemical bonding states of the WI ZrLaO thin films were explored by XPS, as shown in Figure 5-4 (a). Only element Zr, La, O, and C were introduced from the thin-film disposition process or air contamination during measurement have been observed, indicating that the films were escaped from contamination and the element La had been successfully incorporated into ZrO_2 gate dielectric. All the XPS peaks were calibrated by C 1s reference at 284.6 eV to

compensate for any charge-induced shift. The atomic ratio of La in ZrLaO thin films is calculated to be 9.4% for 10% La sample, and 18.4% for 20% La sample. CasaXPS software was used to calculated the atomic ratio at the thin films surface, as shown in Figure 5-24 in appendix. The the atomic ratio could be calculated through the atomic ratio of elements through equation (5-1):

$$Atomic\ ratio\ (\frac{La}{Zr}) = \frac{Peak\ area\ (La)}{Peak\ area\ (Zr)} \times \frac{Relative\ sensitivity\ factor\ (Zr)}{Relative\ sensitivity\ factor\ (La)} \quad (5\text{-}1)$$

The peak of La 3d and Zr 3d has the largest peak area and were selected to represent La and Zr elements, respectively. The relative sensitivity factor (RSF) of an element is a consistent for a selected element. For La and Zr, the RSF value is 47.62 and 7.04, respectively, the CasaXPS software has built-in database of RSF based on [28], and the atomic ratio is calculated by the software automatically after determining the peaks of elements.

All spectra deconvolution was performed by Shirley background subtraction using a Voigt function convoluting Gaussian and Lorentzian functions. Figure 5-4 (b) displays the XPS spectra of Zr 3d core-levels for the WI ZrLaO thin films as a function of La concentration. For all samples, two peaks located at 181.6 and 184 eV had been detected, corresponding to Zr $3d_{5/2}$ and Zr $3d_{3/2}$, respectively. Compared with the undoped ZrO_2, the corresponding binding energies of the Zr 3d peaks for WI ZrLaO shifted to lower energies with La incorporation. This phenomenon has also been observed in other lanthanides oxide based on ZrO_2 [29, 30], the reason is probably due to the donation of

electrons from La to Zr-O bonds, in agreement with the electronegativities of Zr, La and O (1.3, 1.1 and 3.4 on the Pauling scale) [31].

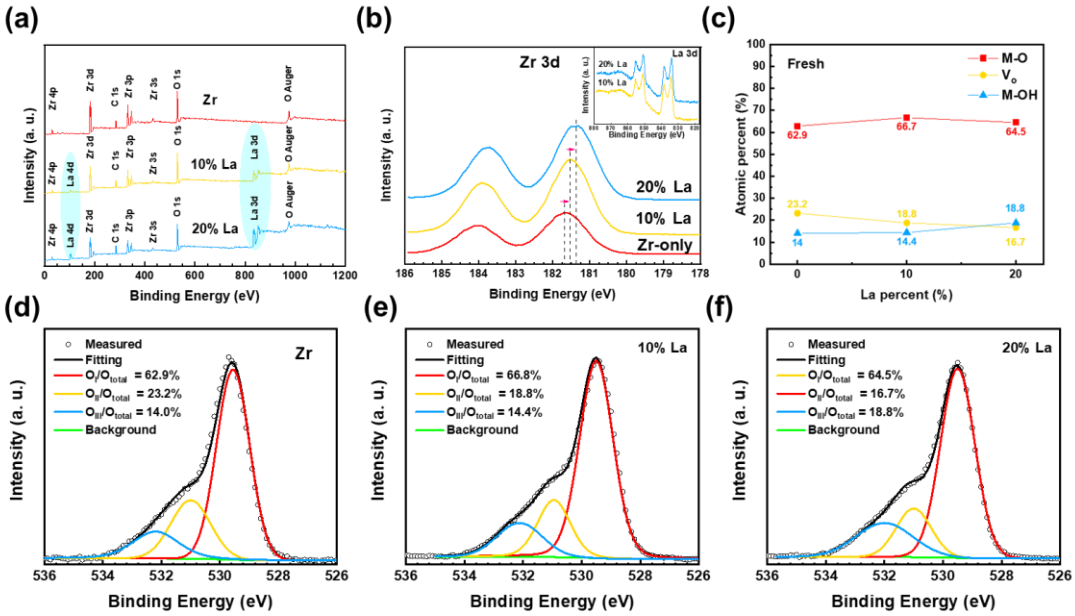


Figure 5-4. (a) Core level XPS survey spectra and **(b)** Zr 3d peaks (inset: La 3d peaks) of ZrLaO thin films as a function of La concentration. **(c)** Semiquantitative analyses of the oxygen component for the corresponding ZrLaO thin films. O 1s peaks and their deconvolution results of ZrLaO thin films with different La concentration **(d)** 0% La, **(e)** 10% La, and **(f)** 20% La.

Figure 5-4 (d)-(e) divide O 1s peaks into three peaks centered 529.5 (O_I), 531.1(O_{II}), and 532.1 eV (O_{III}), respectively. The peak with low binding energy (O_I) represents O^{2-} ions combined with Zr and La ions, the peak with the medium binding energy (O_{II}) is assigned to O^{2-} ions in the oxygen-deficient regions, and the peak with high binding energy (O_{III}) is related to loosely bound oxygen, such as chemisorbed surface hydroxyl, $-CO^3$, absorbed H_2O, or absorbed O_2 [32] [33]. Figure 5-4 (c) summarizes the calculated atomic percentages based on the area integration of O 1s

peaks in Figure 2 (d-e). It is found that, with increasing La content from 0 to 10 %, the area ratio of O_I peak to the total oxygen region (O_I/O_{total}) increases from 62.9 % to 67.3 % and the area ratio of O_{II} peak to the total oxygen region (O_{II}/O_{total}) decreases from 23.2 % to 17.2 %. The results suggest that appropriate La doping (10 %) could suppress the formation of bonded oxygen, especially the V_o, and maximize the metal lattice formation. As La has higher oxygen bond dissociation energy (798 kJ mol^{-1}) with O than Zr (766 kJ mol^{-1}), which may be easier to lower down and control the total V_o amount. However, when the La content increased to 20%, the O_I/O_{total} decreased from 67.3 % to 64.5%, O_{III}/O_{total} increased from 15.5 % to 18.8 %, which was probably attributed to the poor densification and incomplete dehydration of the high-La samples at low temperature [34]. For a good dielectric layer, the amount of bonded oxygen in the dielectric thin films should be kept at a relatively low level because the bonded oxygen generally creates defect states in the forbidden band of the dielectric film, induces the increased leakage current and the reduces breakdown electric field [35, 36].

To investigate the dielectric properties and leakage behavior of WI ZrLaO dielectric layers with various La concentration, Al/ZrLaO/Si gate stack MIM capacitors were prepared. Figure 5-5 (a) demonstrates the frequency-dependent areal capacitance of at least 5 devices for each La concentration, the inset figure shows the structure of MIM devices. The areal capacitance (C_i) of Zr-only, $Zr_{0.9}La_{0.1}O_y$, and $Zr_{0.8}La_{0.2}O_y$ samples was calculated to be 219, 267.5 and 249.6 nF/cm^2 at 1 kHz, respectively, as shown in Figure 5-5 (a). The thicknesses of Zr-only, $Zr_{0.9}La_{0.1}O_y$, and $Zr_{0.8}La_{0.2}O_y$

samples were measured as 50.2, 61.3, and 73.3 nm, respectively. The corresponding *k* values `as a function of La content had been calculated to be 12.4, 18.5, and 20.6. The increased *k* could be ascribed to the higher *k* value of La_2O_3 (~ 27) than ZrO_2 (~ 22). In the all frequency region. Besides, the $Zr_{0.9}La_{0.1}O_y$ samples exhibited the weakest frequency dispersion of capacitance, which indicated the gradual decomposition of defect traps in $Zr_{0.9}La_{0.1}O_y$ and the formation of a dense metal-oxide network [37].

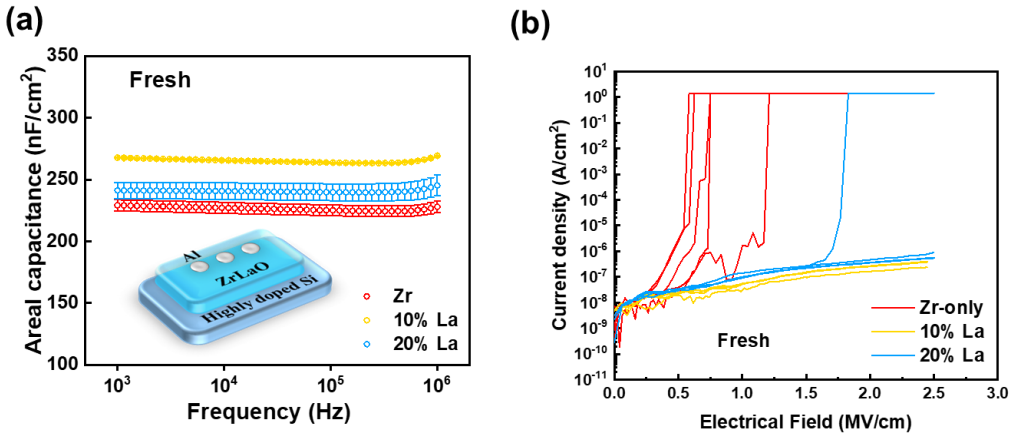


Figure 5-5. (a) C_i-*f* and **(b)** J_{leak}-E of the WI ZrLaO thin films with different La concentrations (0%, 10%, and 20% La). The inset figure is the structure of MIM devices.

The leakage current density (J_{leak})-electric field (E) of the ZrLaO MIM capacitors were investigated to explore the leakage behavior, which is shown in Figure 5-5 (b). It can be found that the La incorporation effectively suppressed the leakage current. Furthermore, the large leakage current density of Zr-only samples can be related to its relative high V_o concentration and low oxygen bond dissociation energy (766 kJ mol^{-1}) with O than La (798 kJ mol^{-1}). The incorporation of La changed the size and shape of

the oxygen ion migration channel in the substitution process, which was beneficial in reducing the lattice defects and improving the electronic transmission, in this situation, the leakage paths were reduced and the leakage current was suppressed accordingly [38]. The increased leakage current of 20 % La sample could probably be ascribed to the incomplete dehydration of residual metal hydroxide, which is related to the high La concentration. Hence, the leakage current was easily formed with high La concentration. Based on the electrical performances of the WI $Zr_{0.9}La_{0.1}O_y$ thin films with different La content, such a low level of leakage current guarantees the achievement of $Zr_{0.9}La_{0.1}O_y$ based TFTs with low voltage and high performance [39].

5.4 InO_x/ZrLaO TFT properties and application

5.4.1 TFT parameters

To verify the potential application of WI ZrLaO thin film as gate dielectric, the full solution-processed aqueous InO_x TFTs based on ZrLaO dielectrics with 0%, 10% and 20% La were constructed. The typical transfer characteristics (I_{DS}-V_{GS}) with a double-sweep gate voltage model, at a drain voltage (V_{DS}) of 4 V, are shown in Figure 5-6 (a). With La concentration varied from 0 % to 10%, I_{off} (1×10^{-11} A) was significantly decreased and the interface between InO_x and ZrLaO is improved. On the other hand, excessive La concentration (20 %) could lead to a decrease in I_{on}, and poor InO_x/ZrLaO interface. It is reported that V_o among oxide could act as trap defects and degrade the properties of the device [40]. According to the above XPS results, the decrease in V_O is

responsible for the reduced current of the device after 20% La doping, while the increase of metal hydroxide related groups resulted in the increased InO_x/ZrLaO interface trap densities.

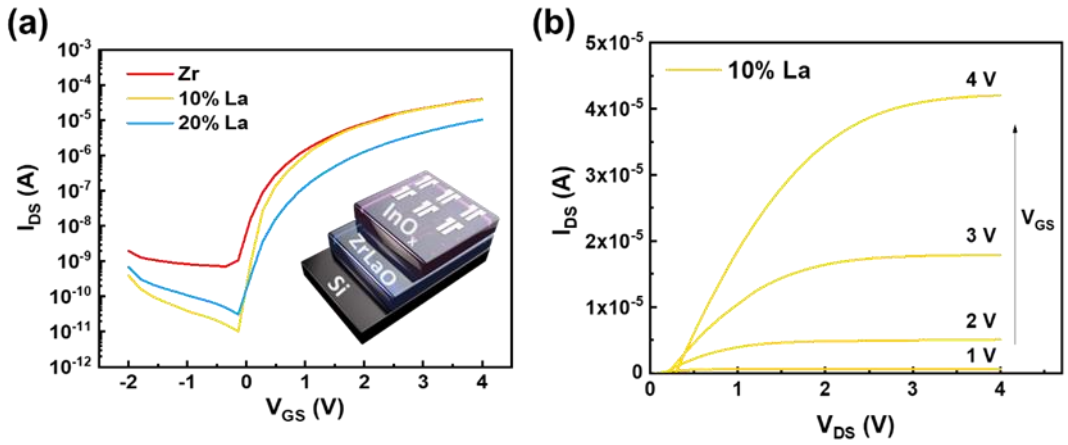


Figure 5-6. (a) Representative transfer characteristics (I_{DS}-V_{GS}), inset is the structure of TFT devices and **(b)** output curves (I_{DS}-V_{DS}) of WI InO_x/ZrLaO TFTs with different La concentration (0%, 10% and 20%).

The output curves (I_{DS}-V_{DS}) of the optimized InO_x/ZrLaO TFTs, shown in Figure 5-6 (b), exhibited the typical n-channel transistor behavior with the clear pinchoff voltage and current saturation. No current-crowding behavior was observed in the low V_{DS} region, indicating good ohmic contact between Al electrodes and the WI InO_x channel layer. At the same time, an ultralow operating voltage of 4 V had been observed in WI InO_x/ZrLaO TFTs. Compared to the reported SiO_2-based TFTs [41, 42], the as-fabricated TFTs expend lower consumption and demonstrate the potential application in low-consumption electronics.

To further investigate the evolution of the electrical properties of the InO_x TFTs as a function of La concentration. The key device parameters of the TFTs and their distributions are summarized in Figure 5-7 and Table 5-1, at least 5 devices were measured for each La concentration to ensure the authenticity of the data. The threshold voltage (V_{TH}) was determined by linear fitting to the dependence of $I_{DS}^{1/2}$ on V_{GS}. The saturation carrier mobility (μ_{sat}) was extracted by the following formula [16]:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \quad (5\text{-}2)$$

where V_{GS} represents the voltage addition between the source and gate electrodes, I_{DS} represents measured saturation current and C_i represents the measured areal capacitance of MIM capacitors. L and W represent the channel length (150 μm) and the width (10 μm), respectively. As analyzed from XPS results, $Zr_{0.9}La_{0.1}O_y$ thin films contained a low density of V_o, which contributed fewer defects in both bulk and interface of the InO_x/ZrLaO TFT device.

Table 5-1. Electrical parameters of WI InO_X/ZrLaO TFTs with different La concentrations (0%, 10%, and 20% La).

La content	μ_{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{TH} (V)	SS (V/ dec)	D_{it} ($\times 10^{12}$ cm^{-2})
Zr-only	1.7 ± 0.27	~ 1×10^5	0.42 ± 0.17	0.27 ± 0.12	5.5 ± 3.0
10% La	2.2 ± 0.06	~ 2×10^6	0.59 ± 0.16	0.11 ± 0.01	1.0 ± 0.3
20% La	0.9 ± 0.28	~ 3×10^5	0.77 ± 0.18	0.26 ± 0.09	4.8 ± 2.1

Table 5-2. Parameters of solution-processed TFTs based on different gate dielectrics.

Dielectric	Temperature [°C]	d [nm]	C_i [nF cm^{-2}]	*k*	E_b [MV cm^{-1}]	Channel	μ_{FE} [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	Year	Ref.
ZrLaO	350	61.3	267.5	18.5	>3	In_2O_3	2.2	2×10^6	2020	This work
GaO	250	52	172	10.1	>2.5	In_2O_3	4.1	1×10^5	2015	[43]
ZrO_2	350	139	138.2	21.7	-	IGZO	0.6	1×10^5	2016	[44]
AlO/Zr/AlO	350	61	95.6	-	2.42	IZO	4.51	5×10^5	2017	[45]
SrO	500	28.3	352.8	11.3	-	In_2O_3	4.98	1×10^6	2017	[46]
ZrGdO	460	13	380	5.39	4	ZTO	3.4	5×10^3	2019	[16]

For the bottom-gate TFTs, the carrier transport is limited in a narrow region at channel/dielectric interface. In this regard, the decreased amounts of defects at the $InO_x/Zr_{0.9}La_{0.1}O_y$ interface could achieve the rapid transport of the induced carriers and thus enhanced μ_{sat}. Besides, the increase in gate capacitance of $Zr_{0.9}La_{0.1}O_y$ causes electrons to rapidly fill the lower localized states between the energy gap, allowing additional induced electrons to occupy the upper localized states. As a result, electrons can easily jump into the nearby localized states along the percolating-conduction path, leading to the enhanced electron mobility [47].

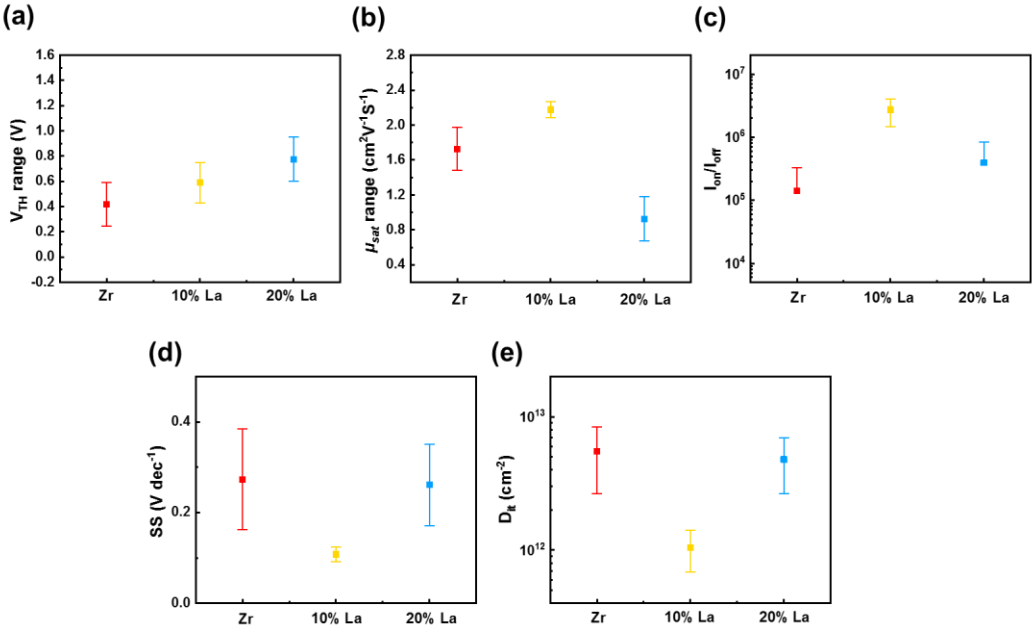


Figure 5-7. Distribution of **(a)** threshold voltage (V_{TH}), **(b)** saturation mobility (μ_{sat}) **(c)** I_{on}/I_{off} **(d)** subthreshold swing (SS) and **(e)** interface trap density (N_{it}) of WI InO_x/ZrLaO TFT with different La concentration (0%, 10% and 20% La).

The SS, defined as V_{GS} required to increase I_{DS} by a factor of 10, generally reflects the switching speed of the TFT, and a small SS is required to achieve the quick switch

behavior [14]. The SS values of Zr-only, $Zr_{0.9}La_{0.1}O_{y,}$ and $Zr_{0.8}La_{0.2}O_y$ TFTs were around 0.27, 0.11, and 0.26 V/dec, respectively. According to the SS value, the interfacial trap density (N_{it}) was calculated to be 5.5×10^{12}, 1.0×10^{12}, and 4.8×10^{12} cm^{-2} using the following equation [48]:

$$SS = \frac{kTIn(10)}{e}\left(1 + \frac{q}{C_i}N_{it}\right) \quad (5\text{-}3)$$

where SS represents the subthreshold swing. q represents electron charge, k represents the Boltzmann constant. The N_{it} value for the $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT is comparable to the TFTs based on other solution-processed high-k dielectrics, e.g., AlO_x (2.6×10^{12} cm^{-2}) [49], YO_x (2.7×10^{12} cm^{-2}) [50], MgO_x (9×10^{12} cm^{-2}) [48], and ScO_x (3×10^{12} cm^{-2}) [27]. The small SS values for $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs may be attributed to the large areal capacitance of the $Zr_{0.9}La_{0.1}O_y$ dielectric layer and the electronic-clean interface between InO_x and $Zr_{0.9}La_{0.1}O_y$. Furthermore, $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT exhibited a negligible hysteresis, indicating suppressed interface traps, which was corresponded to its low N_{it} value. The deceased μ_{sat} and increased N_{it} of $InO_x/Zr_{0.8}La_{0.2}O_y$ TFT was attributed to the poor densification in the high-La samples and poor packing of La in the amorphous state relative to the crystalline state [51]. The large I_{on}/I_{off} ratio, small SS, small N_{it} values, and small hysteresis voltages indicated the formation of a high-quality interface, and demonstrated the feasibility of $Zr_{0.9}La_{0.1}O_y$ thin film as the gate dielectric for InO_x TFTs.

5.4.2 InO_x/ZrLaO TFT based inverter

In previous reports, several high-*k* oxide dielectric films are fabricated via the solution process, and their applications in TFTs are achieved [5, 36, 52, 53]. However, much attention has been paid to the investigation of the electrical properties of the individual TFT device, and the potential applications in more complex logic circuits were ignored. Encouraged by the excellent performance of WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs, their applications in inverter were further explored because the inverter is the basic component in fabricating integrated circuits (ICs) [46, 54, 55]. A simple unipolar resistor-loaded inverter was demonstrated by connecting the WI InO_x/ZrLaO TFTs in series with a 13 MΩ resistor, as shown in the inset of Figure 5-8 (a). Figure 5-8 (a)-(c) exhibit the typical voltage transfer characteristic (VTC) curves of 13 MΩ resistor-loaded inverter with WI InO_x/ZrLaO TFTs at certain voltages (V_{DD}) from 1 to 4 V with 1 V step. It can be found that the output voltage (V_{out}) signal was switched when the input voltage (V_{in}) was swept from 0 to 4 V. It is noticeable that the output high voltage (V_{OH}) was almost same as V_d, while the output low voltage (V_{OL}) was close to 0 V, indicating the good inverter action with ideal swing characteristics.

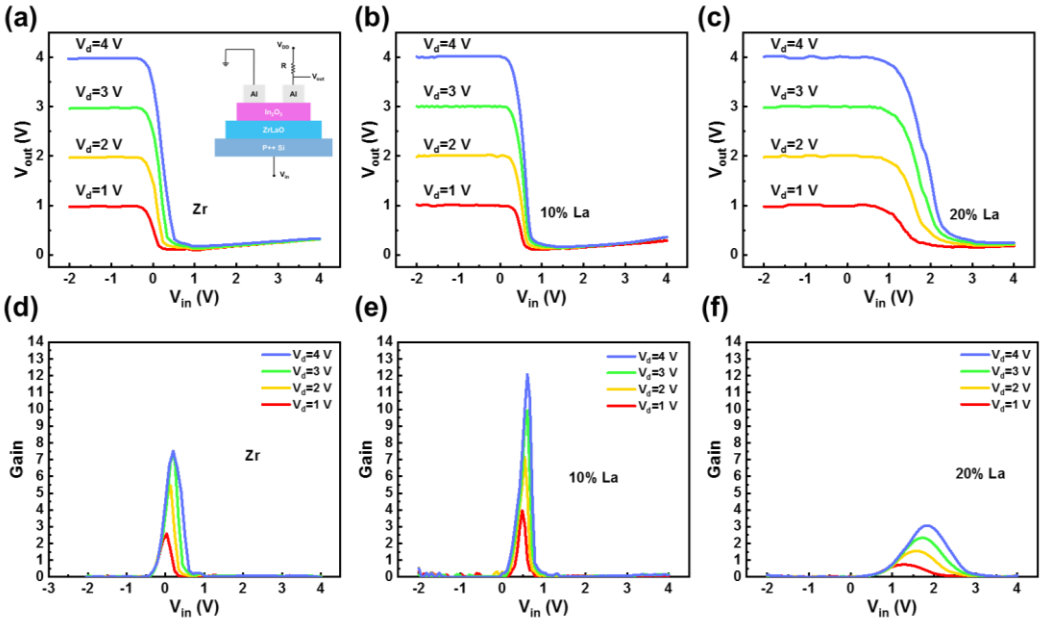


Figure 5-8. Typical voltage transfer characteristic (VTC) of 13 MΩ resistor-loaded inverters with WI InO_x/ZrLaO TFTs with **(a)** 0% La, **(b)**10% La and **(c)** 20% La concentration. The voltage gain of WI InO_x/ZrLaO TFTs based inverters with **(d)** 0% La, **(f)**10% La, and **(g)** 20% La concentration.

Figure 5-8 (d)-(e) show the voltage gain ($-\partial V_{out}/\partial V_{in}$) of the inverter with different V_d. It has been observed that the voltage gain increased with the increase of V_{DD}. The inverters based on WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT exhibits the highest voltage gain. For V_{DD} at 1 V, the voltage gain of about 3.9 had been observed, while for V_{DD} at 4 V, the voltage gain increased to around 12.1. For the continuous signal propagation in ICs which contain a large number of logic gates/stages, the gain value of the inverter is enough large for TFTs to be applied in a logic circuit compared with other works [16, 46, 56, 57]. The high voltage gain was attributed to the balanced field-effect mobility, the

normally-off features, and the small SS of WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT. The high voltage gain and narrow transition width improved the switching characteristics of the inverter.

To estimate the noise margin (NM) of the inverter, the butterfly VTC plot of inverters based on WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT under 1V V_{DD} is shown in Figure 5-9, where another VTC is plotted in a mirror, with output and input axes reversed. The maximum equal criterion (MEC) method was used, a cross-hatched rectangle had been drawn inside the loop of the inverter characteristic, with one corner of the rectangle touching each solid curve [58]. The fitting of a rectangular area within the loop allows one to define a whole range of valid noise margins, and the maximized NM can be estimated by nesting the largest possible rectangular area inside the butterfly plot. The input high voltage (V_{IH}) and the input low voltage (V_{IL}) are the input voltage where the rectangle touches the output curve. The values of output high voltage (V_{OH}) and output low voltage (V_{OL}) are the output voltages for $V_{in} = V_{IL}$ and V_{IH}, respectively, as shown in Figure 5-9. For V_{DD} = 1 V, the high noise margin ($NM_H = V_{OH} - V_{IH}$) and low noise margin ($N_{ML} = V_{IL} - V_{OL}$) were 0.3 and 0.17 V, respectively, which was 60% and 34% of the ideal value ($V_{DD}/2$=0.5V), and was enough for most of the static logic applications [55].

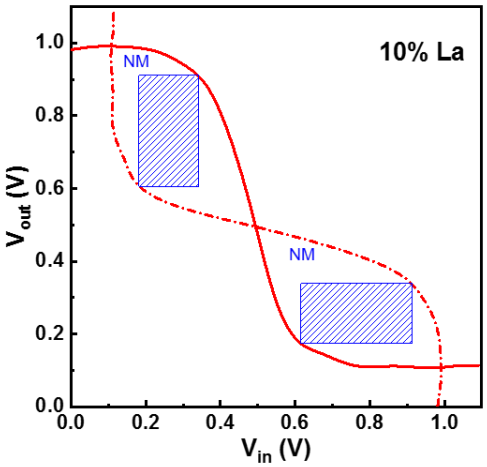


Figure 5-9. Noise margin (NM) extraction of inverters based on WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT using the maximum equal criterion (MEC) method from the butterfly plot.

Moreover, a linear dependence between the voltage gain and V_{DD} of inverters based on WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT has been detected in Figure 5-10 (a), while Zr-only and $Zr_{0.8}La_{0.2}O_y$ based inverter exhibited degradation and could not follow the linear fitting when V_{DD} was increased to 4 V. The transition width, defined as V_{IH}-V_{IL}, was also extracted, as shown in Figure 5-10 (b). Transition width defines the borders of the transition region, a linear dependence between the transition width and V_{DD} had been observed for inverter based on WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT. It is noted that the as-calculated maximum transition width of 0.61 V was lower than those previously reported resistor-loaded inverters based on InO_x (2 V) [59], and IGZO (3.8 V) [60] transistors. Besides, the 0.61 V transition width was the lowest of three kinds of ZrLaO based inverters, the narrow transition width is expected to improve the response characteristics of logic circuits.

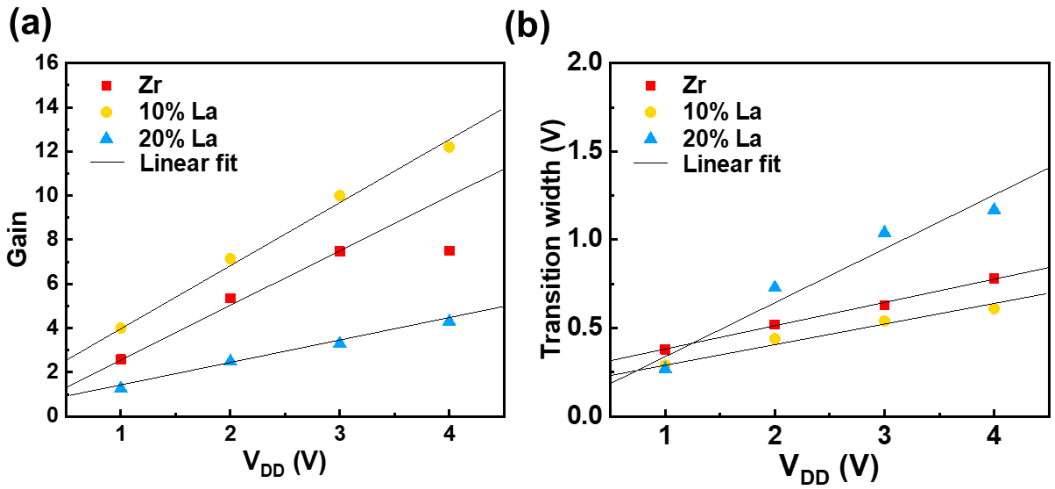


Figure 5-10. Linear fitting of **(a)** voltage gain and **(b)** transition width of the inverter based on WI InO_x/ZrLaO TFT with various V_{DD} values.

To investigate the alternative current (AC) characteristic of the inverter, the dynamic behavior under AC square wave signal was measured and the result is shown in Figure 5-11, where square waveforms with 50-300 Hz frequency were used as input and V_{DD} was 2 V. Under 50 Hz, the calculated propagation delay of from V_{OH} to V_{OL} is represented as t_{phl} (310 μs), while the calculated propagation delay from V_{OL} to V_{OH} is represented as t_{plh} (380 μs). The minimum output voltage is not approaching 0 V, which is related to the measurement system. The detailed discussion about this phenomenon can be found in the appendix. The device exhibited good inversion properties and responded well to the input square-wave signal with frequency up to 300 Hz, implying that the as-constructed inverter had potential applications in complex logic circuits, such as ring oscillators. Based on previous analysis, it can be noted that WI InO_x/ZrLaO TFTs and inverters process an ultralow operation voltage of 4 V, which is much smaller

than those based on SiO_2 gate dielectric. The low operating voltage and low power consumption have turned out to be an inevitable issue for mobile, battery-powered applications. It is believed that better CMOS inverter performance could be achieved with further optimization, including optimizing the channel length, parasitic capacitance, and the mobility of channels. However, in these WI $InO_x/Zr_{0.9}La_{0.1}O$ TFTs inverters, the low operating voltage, large gain value, satisfied noise margin, and 300 Hz dynamic operation demonstrated the potential for ZrLaO dielectric in electronic applications.

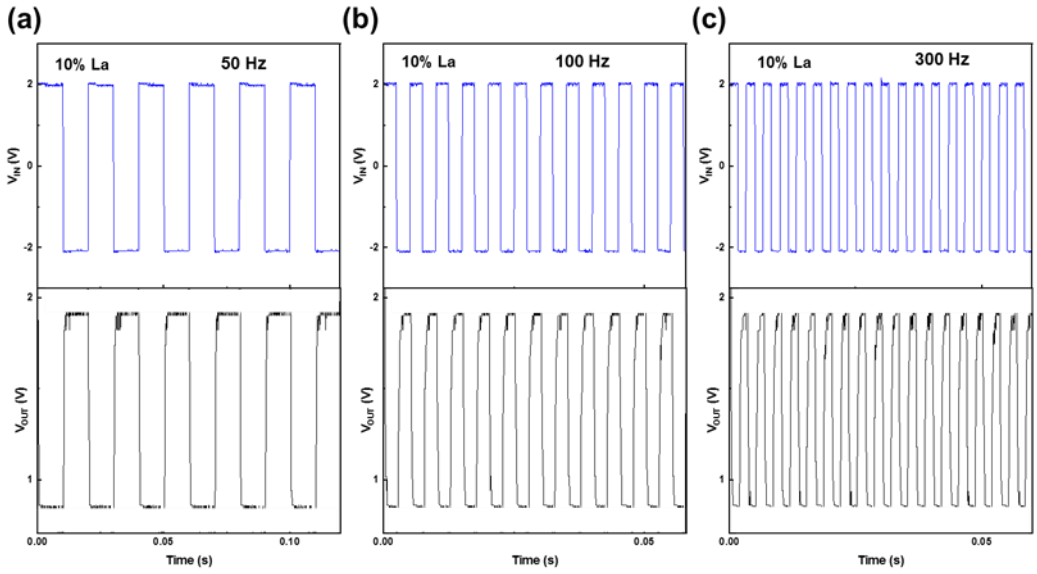


Figure 5-11. Dynamic switching behavior of the inverter based on WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFT under AC square waves at **(a)** 50 Hz, **(b)** 100 Hz and **(c)** 300 Hz.

5.5 Stability of ZrLaO thin films and TFT

5.5.1 Bias stress (BS) stability of InO_x/ZrLaO TFTs

Since the TFT is the basic unit of the integrated circuit, the operational stability of the TFT is a key electrical parameter when considering display applications such as the backplane of AMLCDs and AMOLEDs. To investigate the bias stability of the InO_x/ZrLaO TFTs, bias-stress tests were performed by applying a constant gate bias while maintaining source and drain electrodes grounded. The transfer characteristics of the ZrLaO TFTs under PBS (V_g= + 2 V) and NBS (V_g= - 2 V) conditions are shown in Figure 5-12 (a)-(c) and (d)-(e), respectively. The devices were measured in the dark environment and the stress time was up to 500 s.

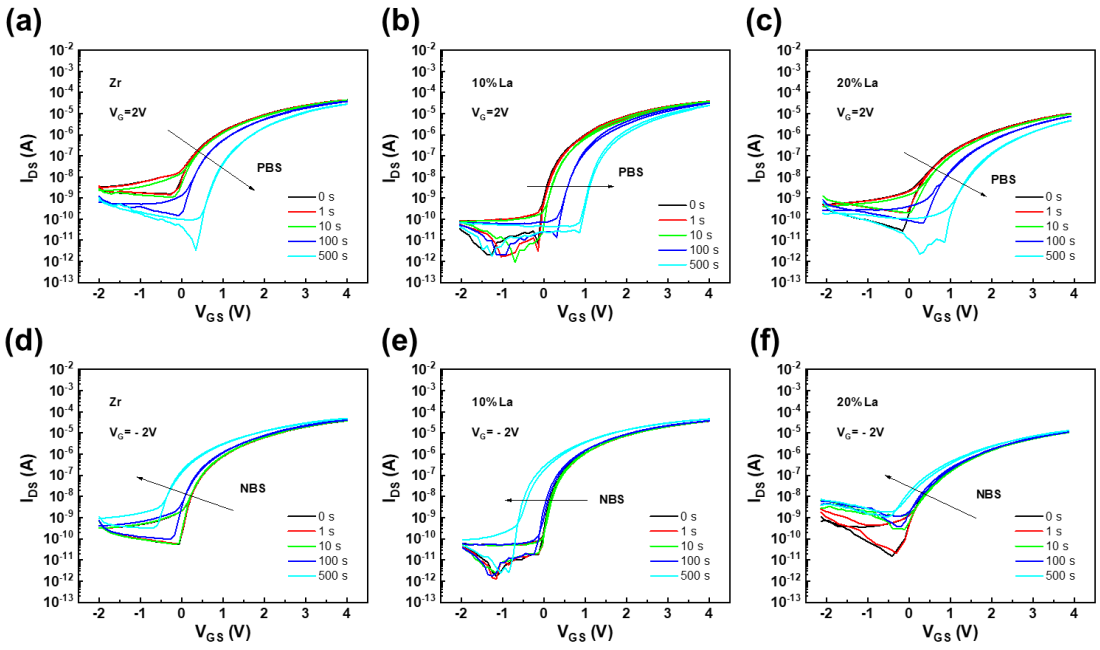


Figure 5-12. Transfer curves of WI InO_x/ZrLaO TFTs under **(a)-(c)** PBS and **(d)-(e)** NBS.

The transfer curves of InO_x/ZrLaO TFTs shifted towards the positive and negative direction with the increase of PBS and NBS time, respectively. All InO_x/$ZrLaO_x$ TFT devices have demonstrated poor BS stability, which could be ascribed to the degradation of InO_x semiconductor layer instead of the ZrLaO dielectric layer. In general, the adsorption of gas molecules at the back-channel surface is known as one of the instability factors of oxide TFTs, which could explain the poor bias-stress stability of InO_x/ZrLaO TFTs. At a positive bias voltage, the oxygen molecules are actively adsorbed on the back-channel surface followed by chemical equilibrium. The equilibrium constant K is given by the following equation [61]:

$$K = \frac{O^-_{solid}}{P_{O_2} \cdot n} \tag{5-4}$$

O^-_{solid}, P_{O_2}, and n represent the adsorbed oxygen concentration on the back-channel surface, the oxygen partial pressure, and the electron density in the InO_x semiconductor film, respectively. The value of K, which is the equilibrium constant, is a constant at a fixed temperature. Therefore, when the accumulated n in the InO_x film increases due to the positive bias voltage, the O^-_{solid} increases, resulting in the acceleration of O_2 adsorption. The adsorbed oxygen molecules react to form oxygen radicals by attracting electrons in the InO_x film due to the extremely high electronegativity of oxygen (3.44), as described in the equation (5-5) [61].

$$O_2(gas) + 2e^- = 2O^-(solid) \tag{5-5}$$

As this reaction continued, a depletion layer is created below the surface of InO_x, contributing to the decreased electron density. The V_{TH} can be affected by the effective electron concentration, according to equation (5-6),

$$n = \frac{C_i(V_{GS} - V_{TH})}{q} \tag{5-6}$$

where C_i is the areal capacitance of dielectric layer and V_{GS} is the gate voltage. The decreased electron concentration could lead to the V_{TH} of the InO_x/ZrLaO TFTs shift to a positive direction.

In contrast, with the consideration of water molecules, the negative gate bias stress -2 V increased the number of holes in the InO_x channel region and caused the adsorbed moisture ($H_2O_{(g)}$) from the atmosphere to form positively charged species ($H_2O^+_{(s)}$). The reaction process is proposed as follows [62]:

$$H_2O_{(g)} + h^+ \rightarrow H_2O^+_{(s)} \tag{5-7}$$

where h+ is a hole. ($H_2O_{(g)}$) and ($H_2O^+_{(s)}$) represent the neutral and positively charged water molecules, respectively. The proposed equation (5-7) indicates that the stated water molecule from the atmosphere typically acts as an electron donor and undergoes a charge exchange process different from $O_{2(g)}$ on the amorphous transparent conducting oxides based film [63]. As the stress duration is increased, the increase in the hole concentration moved the reaction direction toward the right-hand side of the reaction equation. The resultant buildup of positive space charges $H_2O^+_{(s)}$ easily induce conduction electrons in the InO_x/ZrLaO TFT channel, negatively shifting of V_{TH} and

increasing of the ΔV_{TH} magnitude. In addition, the supply of sufficient ($H_2O_{(g)}$) in the air further enhanced the reaction toward the right side of the equation (5-7).

To investigated the BS stability of the single ZrLaO thin films and rule out the biased induced InO_x thin films degradation, the MOSCAPs with the structure of Si/ZrLaO/Al were fabricated. The C-V curves measured from ZrLaO MOSCAPs with 0%, 10% and 20% La are shown in **Figure 5-13**. Similar to the MIM devices based on ZrLaO thin films, the 10% La MOSCAPs have the highest areal capacitance, which is related to the high dielectric constant of La (~27). When the La concentration continuous increasing, the precursor higher La concentration requires higher temperature (~ 400 °C) to form metal oxide framework and eliminate nitrates [34].

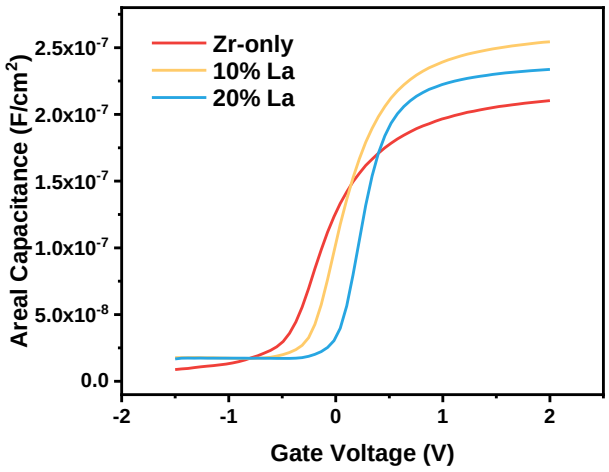


Figure 5-13. The C-V curves of ZrLaO MOSCAPs with different La concentration (0 %, 10 % and 20 % La).

The identify the uniformity of the ZrLaO MOSCAPs, the C-V curves were measured from 5 devices from each sample and are shown in shown in **Figure 5-25** in

Appendix. All devices have demonstrated satisfied device-to-device variation. To investigate the BS stability, the degradation caused by the C-V sweep measurement voltage should be identified. As shown in Figure 5-26 in Appendix, the simply voltage sweep could not lead to the stability degradation of the ZrLaO MOSCAPs with 0 % and 10 % La concentration. On the other side, the samples with 20% La have exhibited the C-V curves shift caused by the measurement voltage. It is reported that La_2O_3 has the highest moisture absorption speed among high-*k* oxides, which is ascribed to its low Gibbs free energy change(ΔG).The moisture absorption phenomenon in high-*k* oxides is the reaction between the solid oxide (M_mO_n) film and the gaseous state water (H_2O) in the air, as represented by (5-8) [64].

$$M_mO_n + H_2O(g) \rightleftharpoons M(OH)_n \tag{5-8}$$

The existence of $M(OH)_m$ in the oxide could severely degrades the reliability and stability of the thin films. However, doping with other high-*k* oxide with appropriating La concentration could suppress the moisture adsorption of La_2O_3 [15]. That is the reason why the La concentration is less than 20% in this work.

After determining that the C-V sweeping voltage could not lead to the stability degradation of ZrLaO MOSCAPs with 0 % and 10 % La concentration. The BS stabilities of ZrLaO MOSCAPs were investigated. As shown in Figure 5-14, ZrLaO MOSCAPs with 0 % and 10 % La concentration have small C-V shift under PBS and NBS, while those with 20% La exhibits poor PBS and NBS stabilities. To further determine the reliability, the extracted ΔV_{FB} are shown in Table 5-3. The ZrLaO

MOSCAPs with 10 % La concentration have the smallest ΔV_{FB}, ΔN_{ot} and ΔN_{it} values under both 1000 s PBS and NBS, demonstrating the best BS stability.

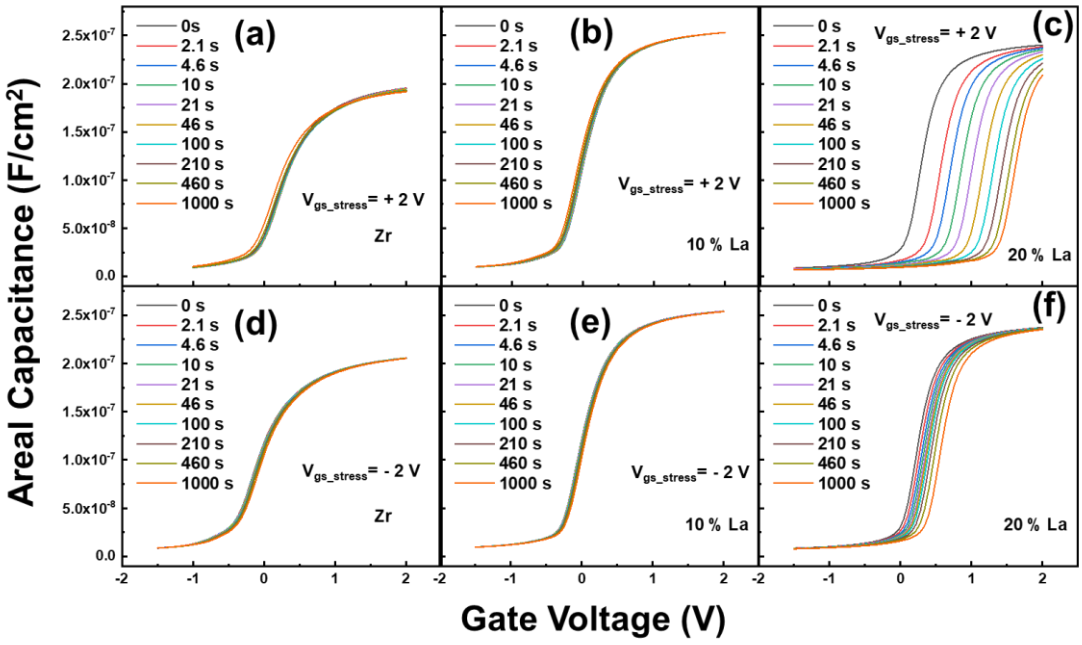


Figure 5-14. The C-V curves of ZrLaO MOSCAPs measured under **(a), (b), (c)** 1000 s PBS and **(d), (e), (f)** 1000 s NBS.

Table 5-3. The extracted ΔV_{FB}, ΔN_{ot} and ΔN_{it} values after 1000 s PBS and NBS.

	1000 s PBS			**1000 s NBS**		
	ΔV_{FB} (V)	**ΔN_{ot} (10^{11}/cm^2)**	**ΔN_{it} (10^{10}/cm^2)**	**ΔV_{FB} (V)**	**ΔN_{ot} (10^{11}/cm^2)**	**ΔN_{it} (10^{10}/cm^2)**
Zr-only	-0.10	3.00	1.18	0.07	-1.60	-4.23
10% La	-0.09	1.67	1.16	0.02	-0.40	-0.66
20% La	1.33	-24.7	-7.04	0.33	-6.10	-0.90

To enhance the BS stability of ZrLaO TFTs, the devices underwent a 30-days ambient air oxidation. The relative humidity and temperature were in the ranges of 50-60 % and 20-25 °C, respectively. Figure 5-15 displays the enhanced BS stability of ZrLaO TFT with 10% La concentration and the exponential fitting results. It can be seen that the ΔV_{TH} is around 0.16 V and the SS has negligible variation after 3600 s +2 V PBS, indicating improved BS stability compared to the device without ambient air oxidation (seen in Figure 5-12). The small ΔV_{TH0} values of fresh devices could be ascribed to the saturation of oxygen of H_2O adsorption on the back-channel surface from ambient [65]. While the large ΔV_{TH0} value of ambient air oxidized devices is probably due to the weak charge trapping effect in the ZrLaO gate insulator, because of the long period, 3600s, of the applied stress, and the ambient air effect on the back channel is negligible [62]. Further investigation on the ambient air effect on the back channel and semiconductor could explain the mechanism of this phenomenon.

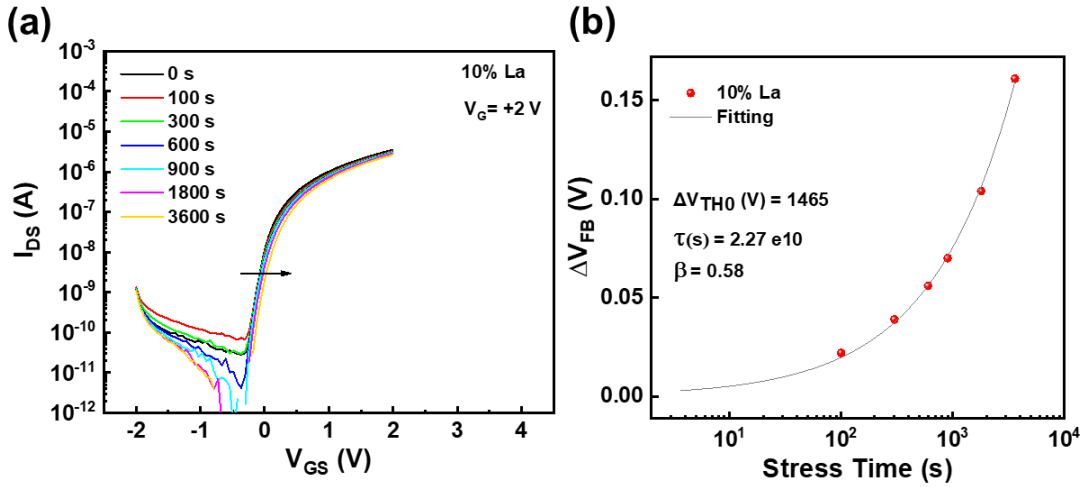


Figure 5-15. (a) The enhanced BS stability of ZrLaO TFT with 10% La concentration after 30-days ambient air oxidation. **(b)** the ΔV_{TH} as a function of stress time. The gate voltage was +2 V and the stress time was up to 3600 s.

5.5.2 Ambient air stability of ZrLaO thin films

To investigate the ambient stability of ZrLaO thin films with different La content, the ZrLaO thin films were exposed to ambient air for 5 weeks. The surface morphology was then characterized by AFM. The calculated RMS values of Zr-only, $Zr_{0.1}La_{0.9}O_y$, and $Zr_{0.2}La_{0.8}O_y$ thin films after 5-week air exposure are 0.209, 0.129, and 0.131 nm, respectively. It is reported that moisture adsorption could lead to the raised RMS value. Compared to the fresh thin films, there is no significant variation of surface roughness of all thin films, demonstrating good moisture resistance [42].

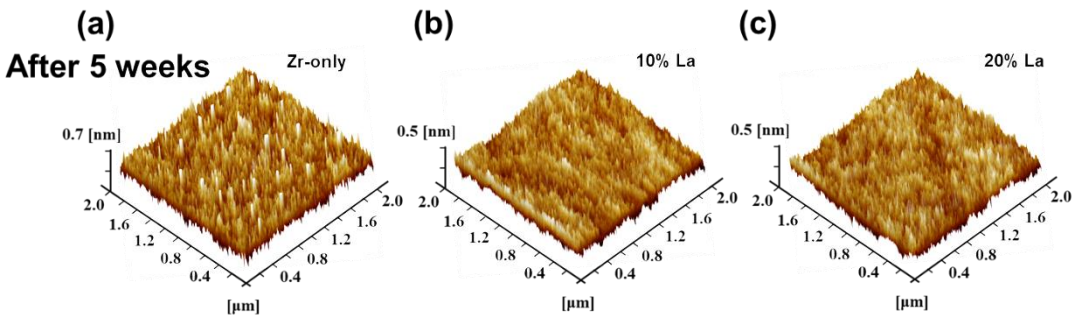


Figure 5-16. 3D AFM images of **(a)** Zr-only, **(b)** $Zr_{0.9}La_{0.1}O_y$, **(c)** $Zr_{0.8}La_{0.2}O_y$ thin films after 5-weeks air exposure.

To further determine the moisture resistance of ZrLaO thin films with different La concentration. The XPS characterization was carried out to analyze the variation of film composition caused by ambient air exposure. As shown in Figure 5-17, compared to the XPS results of fresh ZrLaO thin film in Figure 5-4, the concentrations of M-O of all films show no significant variation after 5-weeks air exposure. Thin films with La incorporation have smaller V_o concentration and are easier to desorb oxygen compared to Zr-only thin films, leading to an increasing V_o concentration after 5-weeks ambient air exposure. This phenomenon is related to the oxygen desorption. The oxygen atoms in ZrLaO may diffuse into the ambience and then an oxygen vacancy is formed. On the other side, the oxygen atoms in ambience may adsorb into films and even recombine with oxygen vacancies. A balance eventually reaches between these two processes if the ambient conditions are stable. Since the formation of O_2 adsorption requires trapping electrons from the conduction band of ZrLaO at the surface, the adsorption rate is controlled by the concentration of electrons in the conduction band on the surface [66]. It is known that small V_o concentration leads to small electron concentration. As

a result, the lack of electrons in the conduction band on the thin film surface could lead to a slow O_2 adsorption rate or even oxygen desorption. Besides, the M-OH concentration of all films has no significant variation after 5-weeks air exposure. Though it is reported that the moisture absorption could occur in most high-*k* oxides and La_2O_3 has the largest moisture-absorption-reaction speed among main high-*k* oxide candidates. Doping an appropriate amount of La_2O_3 into ZrO_2 is an applicable solution to enhance the moisture resistance and inhibit degradation due to stronger moisture resistance of ZrO_2 than La_2O_3.

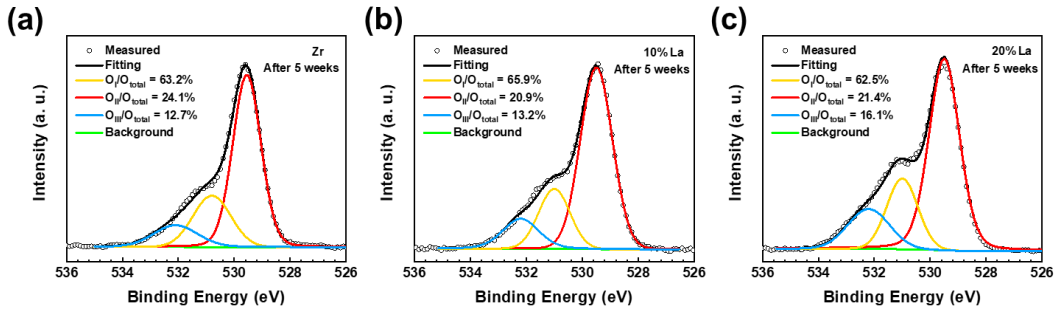


Figure 5-17. O 1s peaks and their deconvolution results of ZrLaO thin films with different La concentration **(a)** 0% La, **(b)** 10% La, and **(c)** 20% La, after 5-weeks air exposure.

To further determine the ambient stability of ZrLaO thin films, the properties of MIM devices are characterized after 5-weeks air exposure. As shown in Figure 5-18 (a), the C_i of Zr-only, $Zr_{0.9}La_{0.1}O_y$, and $Zr_{0.8}La_{0.2}O_y$ samples were calculated to be 231.1, 267.5 and 249.9 nF/m^2 at 1 kHz, respectively, which remained almost the same as those measured from fresh devices. Furthermore, no significant frequency dispersion could be found in all films after 5-weeks air exposure. The degradation of

leakage behavior is also analyzed, as shown in Figure 5-18 (b). As expected, no additional leakage paths were formed due to air exposure. The results indicate that the compositions of ZrLaO thin films are not affected severely by the ambient air, doping the appropriate amount (10%) of La_2O_3 into ZrO_2 ensured the outstanding ambient air stability.

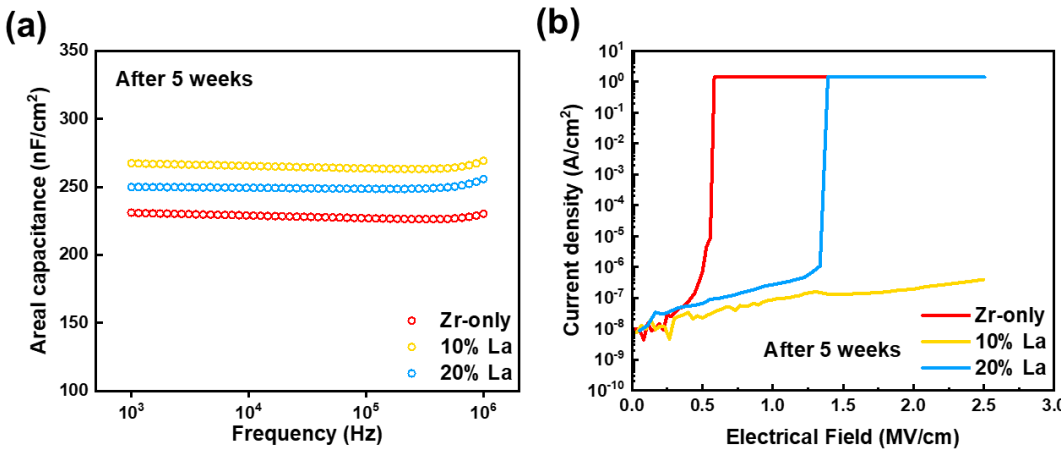


Figure 5-18. (a) C_i-*f* and **(b)** J_{leak}-E of the WI ZrLaO thin films with different La concentrations (0%, 10%, and 20% La), after 5-weeks air exposure.

5.5.3 Radiation hardness of ZrLaO thin films and TFTs

The AFM images of ZrLaO thin films after 1.44 kGy γ-ray irradiation are shown in Figure 5-19. They demonstrated the smooth surface morphology of the Zr-only, $Zr_{0.1}La_{0.9}O_y$, and $Zr_{0.2}La_{0.8}O_y$ thin films with an RMS roughness of 0.282, 0.117 and 0.143 nm, respectively, after photo irradiation with a dose of 1.44 kGy. Compared to the RMS values of 0.209, 0.129, and 0.131 nm, prior to γ-ray irradiation, the Zr-only thin films exhibited an increased RMS value, corresponding to some small peaks

generated by the high-energy photon colliding with the metal-oxide lattice and the change of thin film physical structures [67]. On the other hand, the RMS values of thin films with La incorporation are almost the same before and after irradiation, which could probably be related to the dense film and relative high La-O bond dissociation energy. Nevertheless, the similarly nanosized grains in all the oxide films pointed to the lack of any significant γ-ray irradiation induced degradation, with no induction of grain growth.

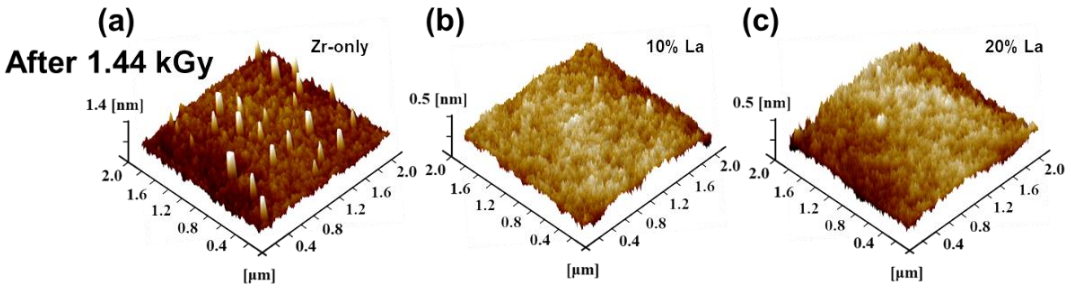


Figure 5-19. 3D AFM images of **(a)** Zr-only, **(b)** $Zr_{0.9}La_{0.1}O_y$, **(c)** $Zr_{0.8}La_{0.2}O_y$ thin films after 1.44 kGy γ-ray irradiation.

XPS was used to investigate the local chemical environment of metal-oxide semiconductors, such as the hydroxide functional group and oxygen vacancies in the oxide lattice. From the results of the detailed analysis of the O1s spectra shown in Figure 5-20, the Zr-only thin films revealed a significant change in the peak shape and constituent ratio. During the photo irradiation, there was a clear decrease in the M-O-M lattice peak (≈529.5 eV) and significant increases in the V_o (≈531.1 eV) and M-O-H (≈531.2 eV) peaks. As mentioned above, the high-energy photon collision with the metal-oxide lattice could induce the formation of oxygen vacancies, which remain as

deep traps or shallow donor states, or which could subsequently generate hydroxides as a result of adsorbing water into the vacancies.

The $Zr_{0.9}La_{0.1}O_y$ thin films showed a less increase of V_o concentration compared to Zr-only films after irradiation, the improved radiation hardness is due to the large oxygen vacancy generation energy of the La_2O_3 could suppress the vacancy generation. It is reported that doping is an effective way to suppress the radiation-induced damage [68]. However, when La incorporation continues to increase to 20 %, the radiation hardness degraded. The M-OH concentration increased slightly after 1.44 kGy radiation exposure, which is possibly ascribed to the irradiation enhanced moisture absorption of La_2O_3, the detailed mechanism requires further investigation. Notably, radiation hardness can be controlled by optimizing the La_2O_3 content (~10 %) doped in ZrO_2.

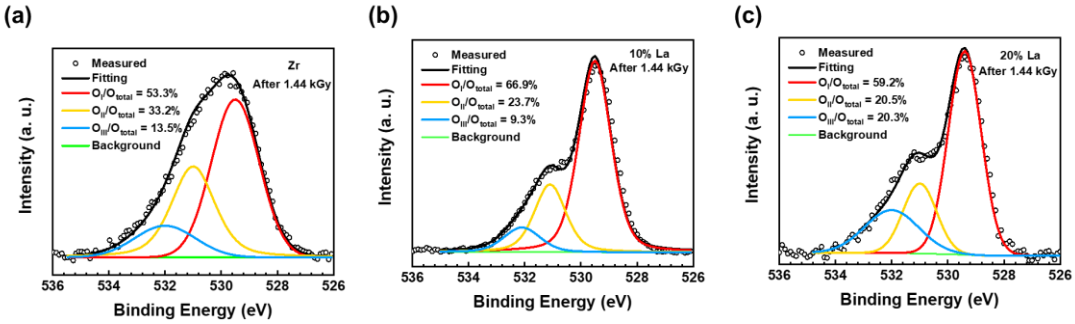


Figure 5-20. O 1s peaks and their deconvolution results of ZrLaO thin films with different La concentration **(a)** 0% La, **(b)** 10% La, and **(c)** 20% La after 1.44 kGy γ-ray irradiation.

As the $Zr_{0.9}La_{0.1}O_y$ thin films have the best air stability and radiation hardness, to further determine the effect of γ-ray irradiation on the electrical performance of ZrLaO based oxide-semiconductor TFTs, the $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs were measured before

and after irradiation exposure. To minimize the effect of moisture effect, the TFTs were exposed to ambient air for 7 weeks to stabilize and reach the balance of oxygen adsorption and desorption, where the mobility decreased from ~2.2 to ~1.2 $cm^2 V^{-1} s^{-1}$, V_{TH} decreased from ~ 0.6 to ~ 0.1 V, and I_{on}/I_{off} decreased from ~ 2.0×10^6 to ~ 2.7×10^5. Afterward, TFTs were put under γ-ray irradiation to investigate radiation-induced degradation. As shown in Figure 5-21. (a), the I_{on} exhibited a decrease after 1 kGy radiation. The calculated TFT parameters are listed in Table 5-4. The transfer curves of the TFT devices exhibited a ΔV_{TH} of 0.06 V and 0.12 V after irradiation with a dose of 0.4 kGy and 1 kGy, respectively. The mobility values of the TFT exhibited a decrease from 1.24 to 0.94 $cm^2 V^{-1} s^{-1}$ with an increase in the irradiation dose. Commonly, radiation results in a higher carrier concentration and channel conductivity [68]. The abnormal decrease of mobility and positive V_{TH} shift is possibly ascribed to the oxygen adsorption at the back-channel. It is reported that oxygen adsorption at the back-channel could form a depletion region at the back-channel and reduce the electron concentration in the semiconductor, which lead to the positive V_{TH} shift and decreased carrier mobility.

To determine the radiation hardness of the TFTs, 10-days air exposure was carried out at the same time to determine the ambient air induced degradation, as shown in Figure 5-21. (b). However, due to the relative humidity around radiation source is high (> 70 %), the ambient air stability ZrLaO thin film still underwent degradation under such a condition. The calculated parameters are listed in Table 5-5. A decrease in I_{on} is observed as well. Correspondingly, the mobility decreases from 1.23 to 0.77 $cm^2 V^{-1}$

s^{-1}, and V_{TH} shifts from 0.07 to 0.12 V. It can be found that the TFT devices exposed to irradiation have higher mobility and larger V_{TH} shift compared to those exposed to ambient air. As reported, radiation could lead to the formation of shallow donors in oxide, which induces the passivation of the band tail stated, a negative shift in the V_{TH} value, and an increase in the mobility [67]. As the dose rate is quite low in this work, the ambient air effect dominated the device degradation, leading to decreased mobility and V_{TH} shift. Meanwhile, the results indicate that the radiation effect and the ambient air effect have a competition, which could explain the less mobility decrease and the less V_{TH} shift of irradiated TFT devices.

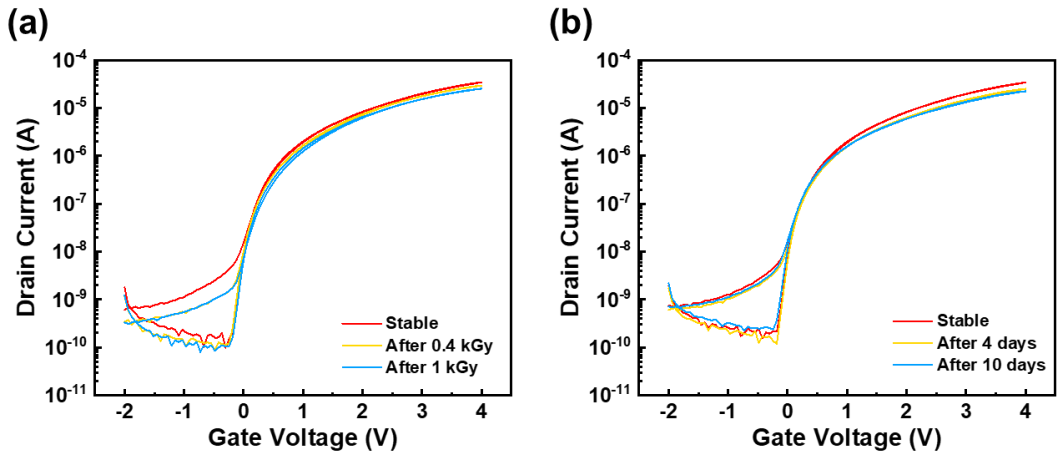


Figure 5-21. Transfer curves of $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs after **(a)** 1 kGy irradiation and **(b)** 10 days air exposure.

Table 5-4. Electrical parameters of WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs after 1 kGy irradiation.

	μ_{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{TH} (V)	SS (V/ dec)
Stable	1.24	2.76×10^5	0.07	0.10
After 40 krad	1.11	2.52×10^5	0.13	0.12
After 100 krad	0.97	2.34×10^5	0.19	0.12

Table 5-5. Electrical parameters of WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs after 10-days air exposure.

	μ_{sat} ($cm^2 V^{-1} s^{-1}$)	I_{on}/I_{off}	V_{TH} (V)	SS (V/ dec)
Stable	1.23	1.61×10^5	0.07	0.11
After 4 days	0.88	1.59×10^5	0.12	0.13
After 10 days	0.77	8.78×10^4	0.12	0.14

To testify the radiation stability of $Zr_{0.9}La_{0.1}O_y$, the BS stability before and after irradiation were investigated, +1 V gate bias was applied to the gate of TFTs with their source and drain grounded. The bias time was up to 500 s. As shown in Figure 5-22. (a), the stable devices exhibited a positive V_{TH} shift under +1 V gate bias, which is possibly due to the enhanced oxygen adsorption during the bias. In Figure 5-22. (b),

after the device was exposed to 1 kGy γ-ray irradiation, no distinct degradation of bias-stress stability is observed. The radiation may have induced oxygen vacancies to increase the electron concentration, which is reflected by the increased V_{TH} shift, compared to the V_{TH} shift of air-exposed devices in Figure 5-22. (c). The ΔV_{TH} as a function of stress time are summarized in Figure 5-23, the time dependence of the ΔV_{TH} followed the stretched exponential model, confirmed the assumption that the charge trapping is the dominant mechanism of ΔV_{TH} in the InO_x/ZrLaO channel and the fitting values are listed in Table 5-6.

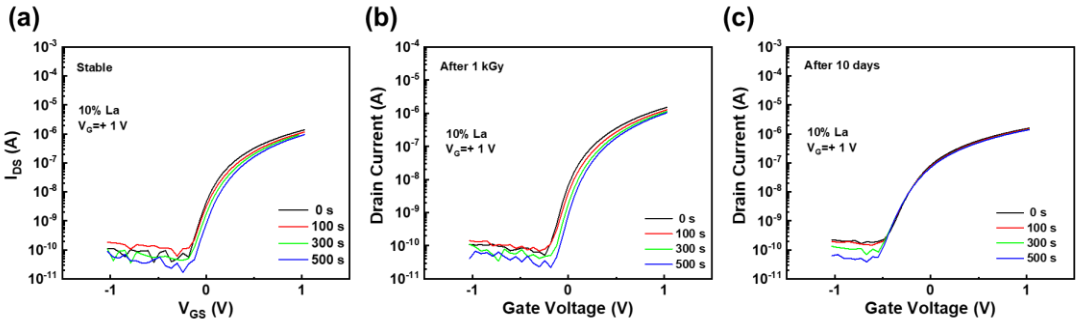


Figure 5-22. Transfer curves of WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs under PBS with conditions of **(a)** stable, **(b)** after 1 kGy irradiation, and **(c)** after 10-days air exposure.

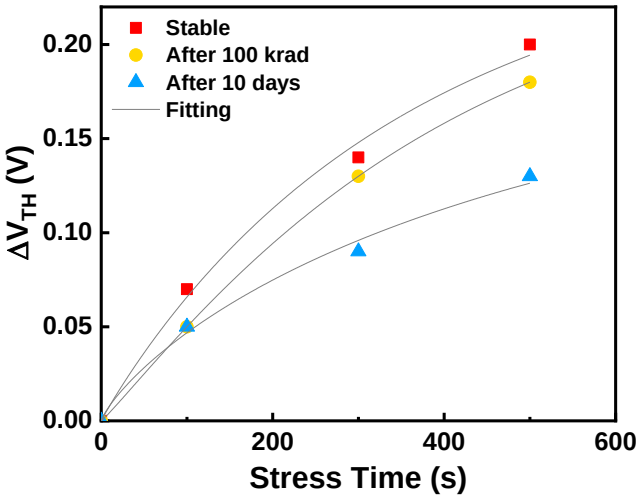


Figure 5-23. ΔV_{TH} of $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs as a function of stress time under the bias stress of +1 V under different conditions. The lines show the exponential fitting of ΔV_{TH}.

Table 5-6. Stretched exponential fitted values of WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs as a function of La concentration under different conditions.

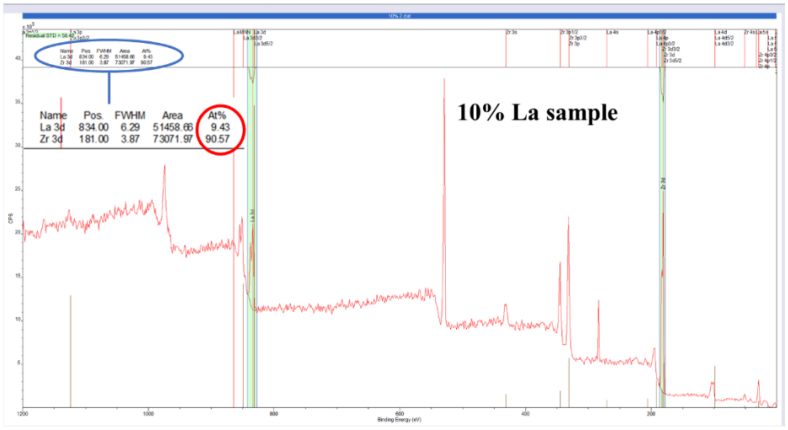
	$InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs		
	Stable	**After 100 krad**	**After 10 days**
ΔV_{TH0} (V)	0.26	0.25	0.21
τ (s)	358	394	554
β	0.96	1.1	0.8

The AFM, XPS and electrical results of ZrLaO thin films as well as ZrLaO based TFT devices indicate that the $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs have satisfied radiation hardness and the 1 kGy irradiation exposure could barely degrade the TFT properties. For further

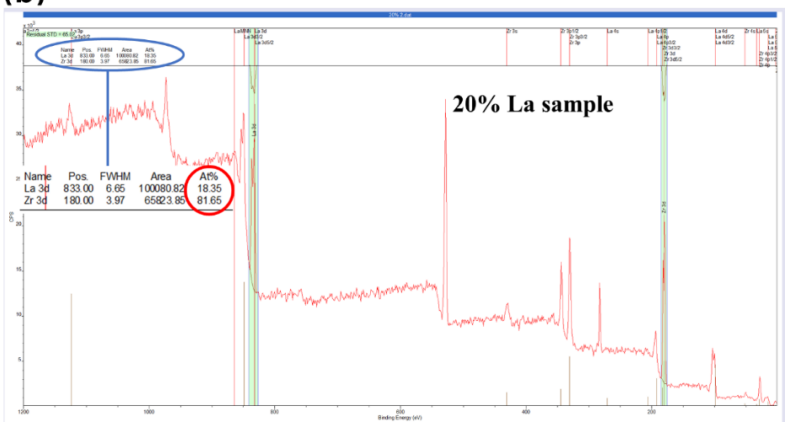
investigation, the device mobility and SS degradation caused by ambient air exposure could be efficiently suppressed by passivation of the back-channel. The organic semiconductor passivation layer over the back-channel thin film could effectively block the moisture and oxygen from the ambient air. Besides, it could further stabilize the device performance when subjected to irradiation. An organic semiconductor, such as [6,6]-phenyl-C61-butyric acid methyl ester (PCBM), could act as a charge transfer and remote dopant layer to control the Fermi level of the films. Moreover, the saturation of the unfilled coordination at the back-channel with an organic semiconductor may suppress the oxygen vacancy generation and help with the regeneration of broken bonds [67].

5.6 Appendix

(a)



(b)



(c)

Regions	A	B
Name	La 3d	Zr 3d
R.S.F.	47.62	7.04
Start	842.5	187.348
End	827.5	177.672
BG Type	U 2 Toug...	U 2 Tougaard
Av. Width	1	1
St. Offset	0	0
End Offset	0	0
Cross Secti...	1397.12 , ...	577.958 , -450 , 0...
Tag	La 3d	Zr 3d
Area	51458.7	73072.0
Std Dev Ar...	0	0
fwhm	6.29346	3.86552
Position	834.0000	181.0000
% Concentr.	9.43	90.57
Max Height	9811.5	23132.2
Min Height	-13.3	-143.3
Peak to Pe...	5.87	94.13

(d)

Regions	A	B
Name	La 3d	Zr 3d
R.S.F.	47.62	7.04
Start	841.5	185.449
End	826.5	175.556
BG Type	U 2 Toug...	U 2 Tougaard
Av. Width	1	1
St. Offset	0	0
End Offset	0	0
Cross Secti...	1143.92 , ...	571.689 , -450 , 0...
Tag	La 3d	Zr 3d
Area	100080.8	65823.9
Std Dev Ar...	0	0
fwhm	6.65239	3.97299
Position	833.0000	180.0000
% Concentr.	18.35	81.65
Max Height	16818.1	18598.3
Min Height	-240.2	-130.0
Peak to Pe...	11.87	88.13

Figure 5-24. Atomic ratio calculation of Zr and La at the surface. The survey spectra of **(a)** 10 % La and **(b)** 20 % La thin films. Element information of **(c)** 10 % La and **(d)** 20 % La thin films.

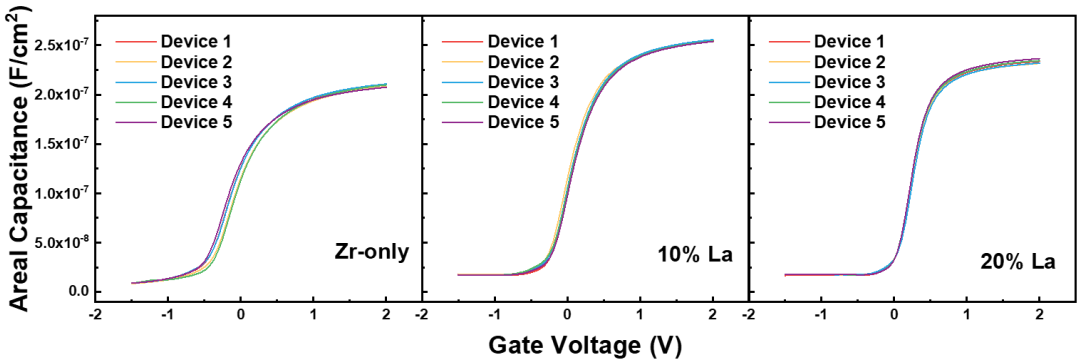


Figure 5-25. The distribution of C-V curves measured from 5 devices of ZrLaO MOSCAPs with different La concentration (0 %, 10 % and 20 % La).

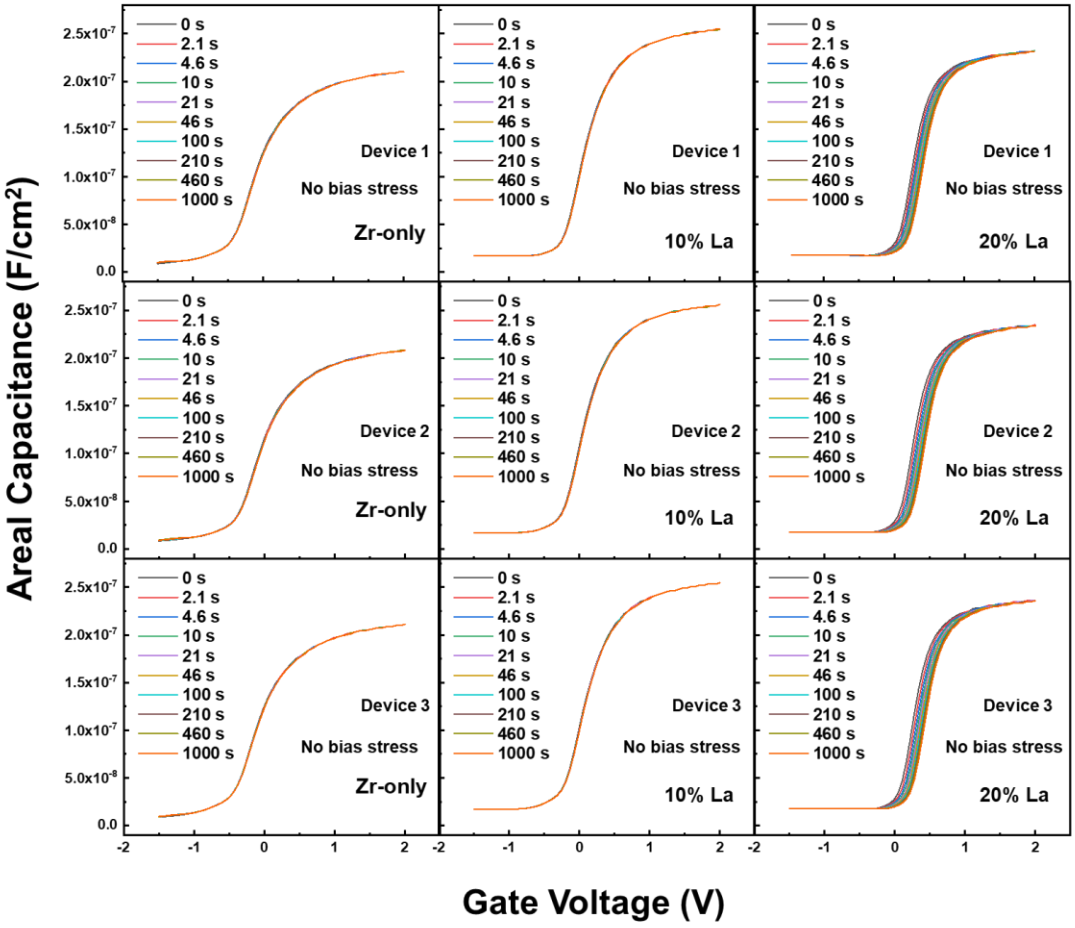


Figure 5-26. The C-V curves of ZrLaO MOSCAPs measured under no bias voltage with time up to 1000 s. For each sample, at least 3 devices were measured.

The load resistors during the static and dynamic measurements of the inverter circuit are different. 13 MΩ resistor is utilized in static inverter circuit and 370 kΩ resistor is utilized in dynamic inverter circuit. As shown in Figure 5-27, because Keysight B1500A was used to apply V_{in} and measure the V_{out} for the static inverter measurement. B1500A has very large internal resistance ($R=R_{B1500A} \approx 1$ GΩ), when TFT is off, the R_{off} is around 10 GΩ ($I_{off} \sim 10^{-11}$ A) and the parallel resistance $R_{\text{static parallel off}}$ of R_{off} and R_{B1500A} is close to R_{B1500A} (1 GΩ), which is >> R_{load} = 13 MΩ, and the measured maximum static V_{out} can be calculated through:

$$V_{out\ maximim\ static} = V_{DD} \times \frac{R_{static\ parallel\ off}}{R_{static\ parallel\ off} + R_{load}} \approx V_{DD}$$

On the other side, when the TFT is on, the internal resistance R_{on} is around 200 kΩ according to the I_{DS}-V_{DS} curve and the parallel resistance ($R_{\text{static parallel on}}$) of R_{on} and R_{B1500A} is close to R_{on} (200 kΩ), which is << R_{load} = 13 MΩ, and the measured minimum static V_{out} can be calculated through:

$$V_{out\ minimum\ static} = V_{DD} \times \frac{R_{static\ parallel\ on}}{R_{static\ parallel\ on} + R_{load}} \approx 0\ V$$

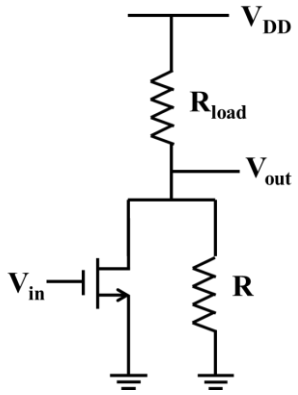


Figure 5-27. The actual inverter circuit, R is the internal resistance of voltage monitor equipment.

However, for the dynamic inverter measurement, a waveform function generator was used to send square wave and a oscilloscope was used to measure the V_{out}. The oscilloscope (Rigol DS1302CA) has the maximum internal resistance of $R=R_{oscil}=1$ MΩ, and the parallel resistance ($R_{dynamic\ parallel\ off}$) of R_{off} and R_{oscil} is close to R_{oscil} (1 MΩ), if 13 MΩ resistor is still selected to be the load resistor, the measured maximum V_{out} could be very small ($V_{DD}/14$), according to equation:

$$V_{out\ maximim\ dynamic} = V_{DD} \times \frac{R_{dynamic\ parallel\ off}}{R_{dynamic\ parallel\ off} + R_{load}} \approx \frac{1M\Omega}{1M\Omega + 13M\Omega} = \frac{V_{DD}}{14} \quad (9)$$

To solve this problem, smaller R_{load} needs to be selected to increase the maximum V_{out}, R_{load} = 370 kΩ resistor was selected. Then the V_{out} maximum can be calculated through:

$$V_{out\ maximim\ dynamic} = V_{DD} \times \frac{R_{dynamic\ parallel\ off}}{R_{dynamic\ parallel\ off} + R_{load}} = 2.5 \times \frac{1 \times 10^{10} \times 1000/(1 \times 10^{10} + 1000)}{1 \times 10^{10} \times 1000(1 \times 10^{10} + 1000) + 370} \approx 1.82\ V \quad (10)$$

Which is close to the measured maximum V_{out}. The measured minimum V_{out} is around 0.85 V, according to I_{DS}-V_{DS} curve, when V_{DS}=0.85 V, the R_{on} was around 240 kΩ.

Equation (11) can be used to verify the inverter circuit,

$$V_{out\ minimum\ dynamic} = V_{DD} \times \frac{R_{dynamic\ parallel\ on}}{R_{dynamic\ parallel\ on} + R_{load}} = 2.5 \times \frac{240 \times 1000/(240 + 1000)}{240 \times 1000(240 + 1000) + 370} \approx 0.86V \quad (11)$$

which is close to the measured minimum V_{out}. To conclude, for the dynamic inverter circuit, because the small internal resistance of the oscilloscope (1 MΩ), a smaller load resistor (370 kΩ) was selected, which leads to the smaller $V_{out\ maximim\ dynamic}$ and larger $V_{out\ minimum\ dynamic}$ compared to the static V_{out}. To solve this problem, an oscilloscope with large internal resistance should be used in the future dynamic measurements.

The use of -2 V as the input voltage is to ensure that the TFT is in the off state when the V_{out} is high. Besides, start from -2V input voltage can also match the measurement voltage range (-2 ~ 4V) of the transfer and output characteristics of the TFT.

5.7 Summary

In summary, novel ZrLaO thin films were fabricated via a non-toxic and fully water-inducement route, and their applications as gate dielectrics in TFTs were investigated. Results have indicated that WI $Zr_{0.9}La_{0.1}O_y$ films annealed at 350 °C have high M-O concentration, low V_o density, small frequency dispersion, and large breakdown electrical field. The $Zr_{0.9}La_{0.1}O_y$ thin films without passivation have demonstrated satisfied radiation hardness (1.44 kGy) as well as ambient air stability (5-weeks). The $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs exhibited satisfied ambient air stability (10-days

ambient air exposure) and radiation hardness (1 kGy irradiation), no obvious electrical property degradation was found. Doping La into ZrO_2 has demonstrated better radiation hardness, due to the higher La-O bond dissociation energy than Zr-O bond and the suppressed oxygen vacancy generation at the bulk oxide. It is found that radiation could generate oxygen vacancies and increase the mobility of the TFT devices. Compared to the irradiation effect, the oxygen adsorption at the back-channel caused by ambient air exposure dominated the degradation of the TFT devices, which should be suppressed by back-channel passivation. Fully WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs have a μ_{sat} of 2.2 $cm^2 V^{-1} s^{-1}$, a large I_{on}/I_{off} of 2×10^6, a small SS of 0.11 V dec^{-1}, a small N_{it} of 1×10^{12} cm^{-2}. $Zr_{0.9}La_{0.1}O_y$ based inverters exhibited full swing characteristics with a high gain of 12.1 at $V_{DD} = 4$ V. These optimized parameters were obtained at a low operating voltage < 4 V. The results represent a great step toward the achievement of low-cost, low-power consumption and large area flexible electronics working in radiation harsh environment.

5.8 References

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Chapter 6:Conclusion and Perspectives

6.1 Conclusion

This thesis investigates the fabrication and reliability of solution-processed high-*k* gate dielectrics. In chapter 3, the method to form high-quality aqueous solution-processed AlO_x thin films with reduced impurities and defects was investigated. It has been found that an annealing temperature of 300 ºC could result in AlO_x thin films with low defect density, high metallic concentration, weak frequency dispersion, low interface trap density, low leakage current, and good BS stability. In addition, the BRS stability of 300 ºC-AlO_x based MOS capacitors was studied. The results suggest that ΔN_{ot} can be attributed to trapping/de-trapping behavior of radiation-induced protons in AlO_x bulk, whilst ΔN_{it} is mainly caused by the passivation/de-passivation of Si dangling bonds at AlO_x/Si interface.Furthermore, oxide trap charges were more effective than the interface trap charges in shifting V_{FB} for 300 ºC-AlO_x MOS capacitors. Both ΔN_{ot} and ΔN_{it} were observed to decrease slightly under PBRS and increase under NBRS. When the device was under PBRS, the radiation-induced electron dominated the decrease of ΔN_{ot} and the passivation of Si dangling bonds at the AlO_x/Si interface dominated the decrease of ΔN_{it}. Under NBRS, the de-passivation, energetic break, and assisted break of Si-H bonds by impurity Al atoms near the AlO_x/Si interface and suboxide bonds were most likely to increase the magnitude of ΔN_{ot} and ΔN_{it}. The

findings of this chapter offer clear inspiration for achieving highly stable solution-processed high-*k* dielectrics working in harsh radiation environments.

In chapter 4, the method to lower the annealing temperature and improve the BS and BRS stabilities of solution-processed AlO_x was explored. H_2O_2 was employed in the precursor solution as a strong oxidizer. In addition, H_2O_2 suppressed the oxygen vacancy density, removed the precursor impurities, and enhanced the AlO_x/Si interface through its strong oxidation at low temperature. The J-V and C-V results further proved the enhancement of employing H_2O_2. In addition, the reliabilities of the devices were improved by adding H_2O_2. 7.5 M H_2O_2-AlO_x devices had demonstrated enhanced BS and BRS stabilities with stress time up to 46000 s and total dose up to 42 Gy (SiO_2). When the devices were under BRS, H_2O_2 could suppress the transportation & reaction of hydrogen (e.g. breaking of Si-H bond), the electron trapping into radiation generated neutral traps and the V_o among AlO_x bulk. ΔN_{it} was insignificant compared to ΔN_{ot}, which was ascribed to that interface trap buildup occurs on time frames much slower than oxide-trap charge buildup. The degradation involved a permanent (fixed) component and a reversible component. It is found that BRS could result in permanent damage to all devices; 7.5 M H_2O_2-AlO_x devices exhibited stronger recoverability than those without H_2O_2. The results in this chapter indicated that employing H_2O_2 in the solution-process had significant potential to improve the BS and BRS stabilities of large-area electronics applied for the nuclear environment and display area.

In chapter 5, novel ZrLaO thin films were fabricated via a non-toxic and fully water-inducement (WI) route, and their applications as gate dielectrics in TFTs were investigated. Results have indicated that WI $Zr_{0.9}La_{0.1}O_y$ films annealed at 350 °C have high M-O concentration, low V_o density, small frequency dispersion, and large breakdown electrical field. The $Zr_{0.9}La_{0.1}O_y$ thin films without passivation have demonstrated satisfied radiation hardness (1.44 kGy) and ambient air stability (5-weeks). The $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs exhibited satisfied ambient air stability (10-days ambient air exposure) and radiation hardness (1 kGy irradiation); no obvious electrical property degradation was found. Doping La into ZrO_2 has demonstrated better radiation hardness due to the higher La-O bond dissociation energy than the Zr-O bond and the suppressed oxygen vacancy generation at the bulk oxide. It is found that radiation could generate oxygen vacancies and increase the mobility of the TFT devices. Compared to the irradiation effect, the oxygen adsorption at the back-channel caused by ambient air exposure dominated the degradation of the TFT devices, which should be suppressed by back-channel passivation. Fully WI $InO_x/Zr_{0.9}La_{0.1}O_y$ TFTs have a μ_{sat} of 2.2 $cm^2 V^{-1} s^{-1}$, a large I_{on}/I_{off} of 2×10^6, a small SS of 0.11 V dec^{-1}, a small N_{it} of 1×10^{12} cm^{-2}. $Zr_{0.9}La_{0.1}O_y$ based inverters exhibited full swing characteristics with a high gain of 12.1 at $V_{DD} = 4$ V. These optimized parameters were obtained at a low operating voltage < 4 V. The results represent a significant step toward the achievement of low-cost, low-power consumption and large-area flexible electronics working in harsh radiation environments.

6.2 Perspectives

Replacement of conventional vacuum deposition methods by solution-based techniques has recently been vigorously pursued, particularly toward cost-effective industrial applications for printed electronics. However, fabrication of solution-processed high-*k* oxide dielectrics in earlier works generally required high-temperature annealing, which limited applications in flexible electronics. Several approaches have been developed to address this issue, including WI, combustion reaction, plasma/UV-assisted post-annealing treatments, and solution-processed self-assembled nanodielectrics (SANDs), reducing overall processing temperatures while retaining or even improving electrical and dielectric performance. Another challenge of solution-based oxide TFTs is the reliability and stability issues. Although so many contributions on solution-based oxide TFTs have been published to date, the application is still pending. The reason is the relatively more insufficient reliability and stability of the solution-processed devices than the vacuum-based counterparts. In-depth studies of the reliability and stability issues of the solution-processed oxide TFTs are essential for future practical applications. Furthermore, considering solution-process is a promising method for large-area applications, it is critical to understand solution-processed device failures in a harsh space environment and the development of radiation-hard devices. Further research into radiation-hard TFT devices with an optimized oxide semiconductor and dielectric with in situ measurements will reveal the detailed damage mechanism and realise large-area sensor arrays, high-performance radar, and radiation

dose monitoring over a large area for nuclear and aerospace applications.