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Field-effect silicon-plasmonic photodetector for coherent T-wave reception

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Abstract: Plasmonic internal photoemission detectors (PIPED) have recently been shown to combine compact footprint and high bandwidth with monolithic co-integration into silicon photonic circuits, thereby opening an attractive route towards optoelectronic generation and detection of waveforms in the sub-THz and THz frequency range, so-called T-waves. In this paper, we further expand the PIPED concept by introducing a metal-oxide-semiconductor (MOS) interface with an additional gate electrode that allows to control the carrier dynamics in the device and the degree of internal photoemission at the metal-semiconductor interfaces. We experimentally study the behavior of dedicated field-effect (FE-)PIPED test structures and develop a physical understanding of the underlying principles. We find that the THz down-conversion efficiency of FE-PIPED can be significantly increased when applying a gate potential. Building upon the improved understanding of the device physics, we further perform simulations and show that the gate field increases the carrier density in the conductive channel below the gate oxide to the extent that the device dynamics are determined by ultra-fast dielectric relaxation rather than by the carrier transit time. In this regime, the bandwidth can be increased to more than 1 THz. We believe that our experiments open a new path towards understanding the principles of internal photoemission in plasmonic structures, leading to PIPED-based optoelectronic signal processing systems with unprecedented bandwidth and efficiency.

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1. Introduction

Optoelectronic signal processing techniques offer great potential for generation and detection of waveforms in the sub-THz and THz frequency range, so-called T-waves [1–4], which may be key to ultra-broadband wireless communications in future sixth-generation (6G) networks [5,6]. In this context, ultra-fast plasmonic photodetectors and electro-optic modulators have been shown to open a path towards generation, detection, and conversion of T-wave signals on the silicon photonic platform [3,4]. Among the various approaches to plasmonic photodetectors [7–12], devices based on internal photoemission can combine high bandwidth with a strongly voltage-dependent sensitivity and are thus not only suited for T-wave generation by photomixing, but also for coherent detection of T-waves by optoelectronic down-conversion with optical local oscillator (LO) signals [3]. However, while the fundamental advantages of plasmonic internal photoemission detectors (PIPED) have been experimentally shown [3,7], the underlying operating principles are still subject to discussion. One of these questions concerns the relative contributions of photo-emitted electrons and holes to the overall current, which is a key aspect to improve the device performance and to quantify the associated fundamental physical limitations for conversion efficiency and bandwidth.

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In this paper, we expand the PIPED concept by introducing a third electrode, which, in analogy to field-effect transistors, we refer to as the gate contact. Varying the gate potential of these field-effect (FE)-PIPED allows to systematically manipulate the contributions of electrons and holes to the overall photocurrent, and thus opens a new experimental access to understanding the device physics. We experimentally demonstrate the concept and verify the underlying principles using dedicated test devices with core widths of 175 nm, and we find that the sensitivity of these devices can be effectively tuned through the gate potential. We further show that the gate voltage increases the sensitivity slope, which determines the down-conversion efficiency for coherent T-wave detection. Specifically, our best performing device shows a two-fold increase in down-conversion efficiency by applying a gate voltage, reaching three times the previously reported efficiency [3]. Based on these findings, we develop a detailed electronic model of the photoemission at the metal-semiconductor interfaces, considering the specific density of states (DOS) on the metal sides. Building upon the improved understanding of the device physics, we further perform simulations showing that the carrier density in a thin channel below the gate can be increased to the extent that the dynamic device response is determined by ultra-fast dielectric relaxation rather than by the carrier transit time. These simulations predict that the bandwidth of the device can be increased beyond 1 THz by applying a gate voltage.

The paper is organized as follows: Section 2 describes the device structure and the fundamental operating principles of the FE-PIPED. In Section 3, we develop a numerical device model and show how the gate potential influences the carrier density and the device bandwidth. Section 4 summarizes the fabrication steps of the devices used in our experiments. In Section 5, we describe the measurement of the devices using DC and T-wave signals, and in Section 6 we summarize our findings and formulate design guidelines for PIPED with significantly improved performance for T-wave signal processing.

2. FE-PIPED structure and operating principle

The FE-PIPED device structure and the operating principle is shown in Fig. 1. Figure 1(a) and its inset display false-colored scanning electron microscope (SEM) images of the FE-PIPED structure, comprising a plasmonic detector core and a silicon photonic waveguide (WG), which are connected by a photonic-to-plasmonic mode converter. The WG feeds light with optical power P_{opt} to the device. The mode converter transforms the photonic mode in the Si WG to a surface plasmon polariton (SPP) mode inside the detector core. Light is absorbed by the Au drain electrode and by the Ti source electrode, generating hot carriers, which can cross the Si core [7]. This leads to an external photocurrent. A bias voltage U_{DS} is applied via two electrodes adjacent to the Si WG core, which are referred to as drain and source. The drain-source bias increases the efficiency of the crossing of the potential barrier [7]. With a so-called gate electrode on top of the oxide covering the Si core, a second control voltage U_{GS} can be applied between gate and source. We define the source electrode to be at the reference potential, and the drain-source voltage U_{DS} as well as the gate-source voltage U_{GS} are counted positive with respect to the source electrode. The cross-section of the detector core represents a metal-semiconductor-metal (MSM) junction and resembles a MOS-FET phototransistor, which motivates the naming of the electrodes.

Figure 1(b) shows the schematic cross-section of the PIPED core along with the normalized color-coded electric field profile of the associated SPP mode that is excited by a quasi-TE mode in the silicon feed waveguide. For this type of mode, the dominant electric field component is oriented parallel to the substrate plane. The vacuum wavelength of the incident light is $\lambda = 1550\,\text{nm}$.

The complex refractive indices $\bar{n} = n - \text{j}n_{\text{i}}$ of the Au and Ti electrodes differ significantly both in the real parts, $n_{\text{Au}} = 0.32$, $n_{\text{Ti}} = 4.0$ [13], and in the (negative) imaginary parts, $n_{\text{i,Au}} = 10.6$, $n_{\text{i,Ti}} = 3.8$ [14]. Therefore, the SPP mode has an asymmetric shape, and the field tends to localize at the Au-Si interface. Still, the Si-Ti interface dominates the overall absorption in the device,

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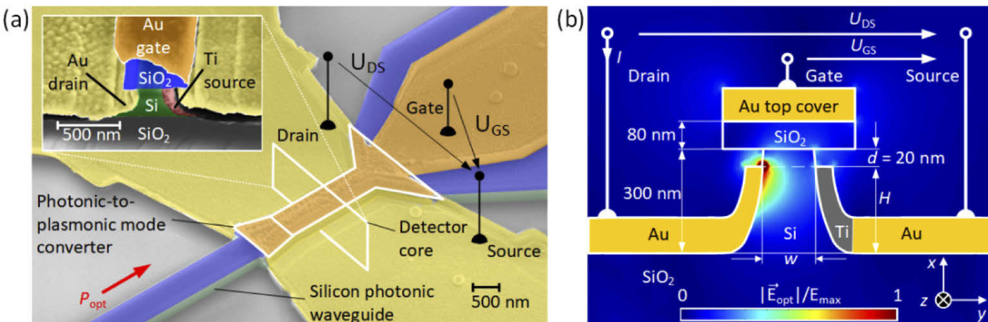

Fig. 1. Field-effect PIPED device structure and operating principle. (a) False-colored scanning electron microscope (SEM) image of field-effect PIPED. Light with optical input power P_{opt} is coupled to the plasmonic detector core via a silicon photonic strip waveguide (WG) (green) having a thermal oxide on top (blue). A photonic-to-plasmonic mode converter transforms the photonic mode to a surface plasmon polariton (SPP) mode in the core. The inset shows the core cross-section. It consists of a Si core clad with an Au electrode at one sidewall (drain) and a Ti electrode at the other sidewall (source) [7]. The bias voltage U_{DS} is applied via the drain and source electrodes, and the gate voltage U_{GS} is applied via the gate contact (orange). The widening of the gate contact outside the core region facilitates the fabrication process and has no influence on the functionality. (b) Schematic cross-section of the photodetector under illumination. The incoming light is coupled to SPP at the interfaces of the Si detector core and the metal layer, and is then absorbed, thereby generating hot carriers. The device core consists of Au and Ti electrodes adjacent to the silicon detector core (metal-semiconductor-metal junction, MSM). The Si core width is chosen to be in the range $w = 75 \ldots 175$ nm. On top of the silicon core, there is a metal-oxide-semiconductor (MOS) junction. The insulating gate oxide has a thickness of 80 nm and an Au top cover. The source potential is chosen as the reference for the drain-source voltage U_{DS} and for the gate-source voltage U_{GS}. The band diagrams in subsequent figures are taken along a horizontal line indicated by the height H. The vertical separation between the upper edge of the drain and source electrodes and the oxide layer is denoted as d. The magnitude of the computed normalized total optical electric field as excited by a quasi-TE mode in the feeding Si strip WG is color-coded. Note that even though the field in the Si detector core is mainly localized at the Au contact, most of the photons are absorbed in the Ti, which features a larger real part of the complex refractive index than the Au.

due to the larger real part of the Ti refractive index. The smaller the core width w becomes, the more the absorption length of the lossy SPP mode decreases. For technically relevant widths of 50 nm $\leq w \leq$ 250 nm, the absorption length $1/\alpha$ is below 1 µm, where α denotes the power attenuation coefficient of the SPP mode. A fully vectorial numerical simulation considering the field distribution excited by a quasi-TE mode in a FE-PIPED of core width $w = 100$ nm indicates that six times more power is absorbed in the Ti electrode than in the Au electrode. Accordingly, the bias voltage U_{DS} is chosen such that photo-emitted electrons from the Ti electrode are drawn towards the Au contact, thus forming the main component of the photocurrent in the external circuit. The FE-PIPED can also be operated in a quasi-TM mode where the dominant electric field component is along the normal to the substrate plane. The mode profile and the associated absorption characteristics can be found in the supplementary information of [7].

If a photon with energy hf is absorbed in a metal, it creates an electron-hole pair separated by an energy difference hf, where the actual energy of the carriers depends on their initial energy before the absorption process. As an example, an electron (or hole) which happens to be at the Fermi energy W_{F} will end up after the absorption process as a "hot" electron (or as a "hot"

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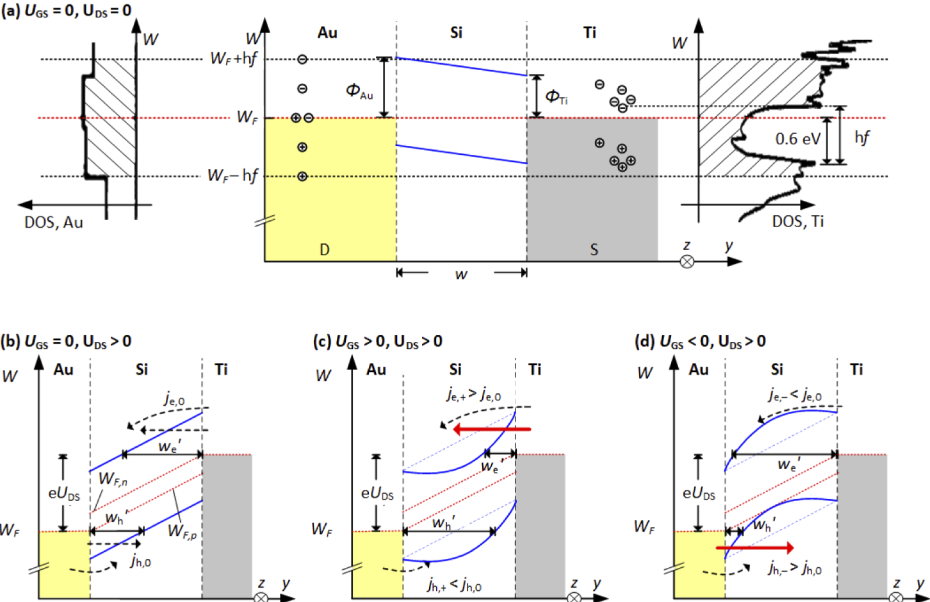

Fig. 2. Band diagram of Au-Si-Ti junction for various gate voltages. The Ti electrode (source) is at the reference potential. The band edges (blue) are schematically drawn along a cut line near height H at the upper edge of the metal drain and source electrodes in Fig. 1(b). The difference in the barrier heights Si-Au and Si-Ti leads to a built-in potential $\varphi_{\mathrm{bi}} = (\Phi_{\mathrm{Au}} - \Phi_{\mathrm{Ti}}) / \mathrm{e} = 0.2\,\mathrm{V}$ in absence of an external bias. The Fermi energy (red dotted line) is denoted by W_{F}. Surface plasmon polaritons (SPP) with energy $hf = 0.8\,\mathrm{eV}$ are absorbed in both metals and create electron-hole pairs. (a) Thermal equilibrium, $U_{\mathrm{GS}} = 0$, $U_{\mathrm{DS}} = 0$, with the respective densities of states (DOS) [18,19]: The electron DOS in Ti peaks at $W_{\mathrm{F}} - 0.6\,\mathrm{eV}$. Most of the hot electrons will be found at $W_{\mathrm{F}} + 0.2\,\mathrm{eV}$, below the barrier energy $W_{\mathrm{B,Ti}} = W_{\mathrm{F}} + \Phi_{\mathrm{Ti}}$. In contrast, the DOS in Au does not strongly depend on energy. Photoemission is therefore governed by hot holes with an essentially uniform energetic distribution. (b) Non-equilibrium, $U_{\mathrm{GS}} = 0$, $U_{\mathrm{DS}} > 0$: Conduction and valence band edges in silicon tilt for a positive voltage U_{DS}, applied between drain (D, Au) and source (S, Ti). Hot electrons from both metals overcome the barriers or tunnel through, leading to particle current densities $j_{\mathrm{h},0}$ (hole emission from Au at $U_{\mathrm{GS}} = 0$) and $j_{\mathrm{e},0}$ (electron emission from Ti at $U_{\mathrm{GS}} = 0$) and resulting in an external photocurrent. The effective barrier widths w_{h}' and w_{e}' limit the carrier emission. The quasi-Fermi levels for electrons $W_{\mathrm{F,n}}$ and for holes $W_{\mathrm{F,p}}$ are oriented parallel to the band edges. (c) Non-equilibrium, $U_{\mathrm{GS}} > 0$, $U_{\mathrm{DS}} > 0$: Band edges with positive curvature, electrons accumulate under the gate contact. The effective barrier width w_{e}' at the Si-Ti interface reduces (increased electron emission, $j_{\mathrm{e},+} > j_{\mathrm{e},0}$), while w_{h}' increases at the Au-Si interface (reduced hole emission, $j_{\mathrm{h},+} < j_{\mathrm{h},0}$). (d) Non-equilibrium, $U_{\mathrm{GS}} < 0$, $U_{\mathrm{DS}} > 0$: Holes accumulate under the gate contact, and the effective barrier width w_{e}' at the Si-Ti interface increases (electron emission reduced, $j_{\mathrm{e},-} < j_{\mathrm{e},0}$), while the barrier width at the Au-Si interface w_{h}' reduces (hole emission increases, $j_{\mathrm{h},-} > j_{\mathrm{h},0}$).

hole) with an electron (or hole) energy $W_{\mathrm{F}} + hf$ (or $W_{\mathrm{F}} - hf$) [15], using the energy counting convention as indicated in Fig. 2.

The Schottky barrier at the MS interface influences how high-energy carriers enter the silicon core. If hot carriers have an energy larger than the Schottky barrier height, they overcome the barrier with a probability that is significantly greater than if the carriers have to tunnel through it [16]. The crossing of the potential barrier is known as internal photoemission (IPE) [17].

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The energetic distribution of hot carriers before and after absorption depends on the material-dependent density of states (DOS) for Ti and Au [18,19], respectively, and on the Fermi function. Because at room temperature the Fermi function features a transition from high (0.88) to low (0.12) occupation probabilities within an energetic width of $4kT_0 \approx 100$ meV (Boltzmann constant k, room temperature T_0), the Fermi function can be approximated by a unit step for the photon energies under consideration, $hf = 0.8$ eV.

In the following, we qualitatively explain the influence of the external bias voltages on the band diagram and on the associated photocurrents. A bias voltage $U_{\mathrm{DS}} \neq 0$ leads to a splitting of the quasi Fermi levels for electrons $W_{\mathrm{F,n}}$ and for holes $W_{\mathrm{F,p}}$ in the silicon core. Independently of the biasing condition, the number of carriers available for photocurrents is generally larger in Ti than in Au as the light absorption is stronger in Ti. The Si band-gap energy amounts to $W_{\mathrm{G}} = 1.11$ eV, and for the barrier height we assume $\Phi_{\mathrm{Au}} = 0.82$ eV. Note that this barrier height is much larger than the values of approximately 0.3 eV [20] that are typically found for interfaces of Au and neat Si surfaces. The increased barrier height in our device is due to the fact that the PIPED relies on interfaces between Au and chemically treated Si surfaces prepared by reactive ion etching (RIE). This significantly affects the actual barrier height, for example by gold diffusion or surface states created by the Si processing [21]. Following [21,22], we estimate a barrier height $\Phi_{\mathrm{Au}} = 0.82$ eV, and we experimentally verify this estimate by evaluating the photoemission current [15] of our PIPED devices over a wavelength range between 1270 nm and 1325 nm. To this end, the device was cleaved, and light emitted by a wavelength-tunable laser was coupled directly to the cleaved facet using an optical fiber. By fitting the wavelength-dependent photocurrent to a Fowler's model for photoemission [15], we find a barrier height at the Au-Si interface of $\Phi_{\mathrm{Ti}} = 0.82$ eV, which is in good agreement with [22]. We further confirm our result with the physical device simulator SILVACO ATLAS by modeling the PIPED dark current for this barrier height, leading to good agreement with our measurements.

Due to this large Schottky barrier height, photoemission is most efficient for positive drain-source voltages $U_{\mathrm{DS}} > 0$, leading to hole emission at the Au-Si interface, Fig. 2(b), (c) and (d). We start with a gate-source voltage $U_{\mathrm{GS}} = 0$ which essentially corresponds to a floating gate and therefore to the behavior of a conventional PIPED structure [3,7]. We then discuss the influence of a changing gate voltage. At the Si-Ti interface, where most of the light is absorbed, the Schottky barrier height amounts to $\Phi_{\mathrm{Ti}} = 0.62$ eV [23], leading to electron emission. Because the electron DOS in Ti peaks at $W_{\mathrm{F}} - 0.6$ eV, Fig. 2(a), and because the electron occupation probability below $W_{\mathrm{F,n}}$ is close to 1, most of the hot electrons will be found at $W_{\mathrm{F,n}}$+0.2 eV, indicated by the dashed black line in Fig. 2(a). Since this energy is still below the barrier energy $W_{\mathrm{B,Ti}} = W_{\mathrm{F,n}} + \Phi_{\mathrm{Ti}}$, internal photoemission predominantly relies on tunneling, and the barrier width at the Si-Ti interface has a significant influence on the electron part of the photocurrent, see Fig. 2(b). Note that from this simplified model illustrated in Fig. 2, one may expect that reverting the sign of U_{DS} could lead to a device with similar functionality based on hole rather than electron emission on the Si-Ti interface. However, this effect is not observed experimentally, i.e., the photocurrent for $U_{\mathrm{DS}} < 0$ is orders of magnitudes smaller than its counterpart for $U_{\mathrm{DS}} > 0$.

In contrast to that, the DOS in Au is rather energy-independent. Photoemission at the Au-Si interface is governed by hot holes that uniformly fill the energy range ($W_{\mathrm{F,p}} - 0.8$ eV)... $W_{\mathrm{F,p}}$. For a Schottky barrier height $\Phi_{\mathrm{Au}} = 0.82$ eV and a Si band-gap energy of $W_{\mathrm{G}} = 1.11$ eV, the hole barrier is energetically located at $W_{\mathrm{F,p}} - 0.29$ eV. For a photon energy of $hf = 0.8$ eV, approximately half of the hot holes are hence to be found at hole energies above $W_{\mathrm{F,p}}$, i.e., at electron energies below $W_{\mathrm{F,p}}$. As a consequence, a significant fraction of the hot holes which are optically excited in the Au electrode can energetically overcome the barrier irrespective of the exact barrier width or shape. This is distinctively different from internal photoemission of hot electrons from Ti to Si, which largely relies on tunneling, and hence strongly depends on the shape and particularly

on the width of the potential barrier. Note that the hot carriers relax and thermalize with the surrounding uniform electron or hole gas if the internal photoemission does not occur within the typical hot-carrier lifetime of a few 10 fs inside the metals [24]. Note also that the contribution of holes from the Au to the overall photocurrent is smaller than that of electrons from the Ti, since the major part of the light is absorbed at the Si-Ti-interface.

In absence of any incident light, the dark current is determined by the emission of cold carriers. The energetic distribution of cold carriers that are in equilibrium with the crystal lattice follows the Fermi-Dirac statistics. Only a small fraction of cold carriers with sufficiently high energy can directly overcome or tunnel through the barriers, a process which is called thermionic emission [16]. Due to tunneling of carriers, thermionic emission also depends on the shape of the respective potential barrier. This leads to a voltage-dependent dark current through the FE-PIPED.

For the band diagram in Fig. 2(b), a positive bias U_{DS} is chosen that overcompensates the built-in potential $\varphi_{\mathrm{bi}} = (\Phi_{\mathrm{Au}} - \Phi_{\mathrm{Ti}}) / \mathrm{e} = 0.2\,\mathrm{V}$. This potential φ_{bi} arises from the different barrier heights for electrons on the gold side (Φ_{Au}) and on the titanium side (Φ_{Ti}). The gate contact is at the same potential as the source contact, $U_{\mathrm{GS}} = 0\,\mathrm{V}$. In this case, the core width w is much shorter than the depletion region that is generated by the applied drain-source voltage $U_{\mathrm{DS}} > 0$ inside the weakly doped Si WG core (acceptor density $n_{\mathrm{A}} \approx 5{\times}10^{15}\ \mathrm{cm}^{-3}$), such that the space-dependent potential can be described by a linear function. Hence, the applied voltage drops quasi-linearly across the Si core, leading to approximately linear conduction and valence band edges. A non-zero gate-source voltage U_{GS}, Fig. 2(c), (d), influences the potential in the Si WG core only in the immediate vicinity of the gate oxide, similar to the situation for a MOS field-effect transistor. Specifically, an applied gate voltage bends the linear bands such that the effective barrier widths at the Si-metal interfaces are changed, which influences photoemission and hence the device current I. With a fixed drain-source voltage $U_{\mathrm{DS}} > \varphi_{\mathrm{bi}}$ and for $U_{\mathrm{GS}} > 0$, the Si-Ti effective barrier width is reduced to w_{e}', and electron injection from the Ti side is increased, Fig. 2(c). Conversely, for $U_{\mathrm{GS}} < 0$, the effective Au-Si barrier width is reduced to w_{h}', leading to a stronger hole injection from the Au, Fig. 2(d). Moreover, the band bending has a strong impact on the carrier dynamics in the Si core: The electron concentration below the gate oxide is increased for $U_{\mathrm{GS}} > 0$, Fig. 2(c), while for $U_{\mathrm{GS}} < 0$, the hole concentration increases. If the carrier concentration in the thin channel below the oxide is large enough, signal propagation is dominated by ultra-fast dielectric relaxation rather than by the drift of individual carriers. This leads to a significant increase of the device bandwidth. We explore this feature in more detail in Section 3.

The spatial separation d of the gate oxide and the electrodes, as seen in Fig. 1(b), is an important design parameter that strongly influences the device behavior. On the one hand, the distance d must not be chosen to be too large, since this would reduce the influence of U_{GS} on the barrier shapes, and the gate functionality would disappear. Moreover, the photoemitted carriers would be injected far away from the thin conductive channel below the oxide, and the benefits of ultra-fast dielectric relaxation would be lost. On the other hand, choosing d too small would lead to a very small effective barrier width w_{e}' and would hence have a detrimental impact on the dark current, especially at high gate fields. These considerations lead to a deeper understanding of the measured I-U_{GS} characteristic. We come back to this aspect in Section 5.1.

3. Optoelectronic bandwidth

The FE-PIPED has the potential to reach an unprecedentedly high light detection speed. To prove this point we use a 2D time-domain simulation of an appropriate device model. We use the simulation tool SILVACO ATLAS for the FE-PIPED model Fig. 1(b) with core width of $w = 100\,\mathrm{nm}$. ATLAS is a physical device simulator that relies on the drift-diffusion model and solves the continuity equations. The influence of the metal-semiconductor interfaces on the

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device currents are taken into account. Our simulation domain is defined in the x-y plane, i. e., in a cut-plane whose normal vector is perpendicular to the direction of the photocurrent and parallel to the direction of light propagation. With this setting, we simulate the potential $\varphi(x,y)$ and the spatial carrier concentration for various biasing conditions.

Figure 3(a) shows the electron and hole concentration in the silicon core, directly at the interface of gate oxide and silicon, in the middle between the drain and the source contact where the carrier concentration due to the gate potential is highest. For a drain-source voltage of $U_{DS} = +1.5$ V and a gate-source voltage of $U_{GS} = 0$ V, without an applied gate, the hole concentration is in the order of 10^{15} cm^{-3}. When applying a gate voltage as small as $U_{GS} = -5$ V, holes accumulate, and their concentration increases to 5×10^{18} cm^{-3}. For creating a similar electron accumulation under the gate oxide, the silicon conduction type must be inverted. The inversion threshold is near $U_{GS} = 3$ V. The electron concentration reaches 10^{19} cm^{-3} for $U_{GS} = 10$ V.

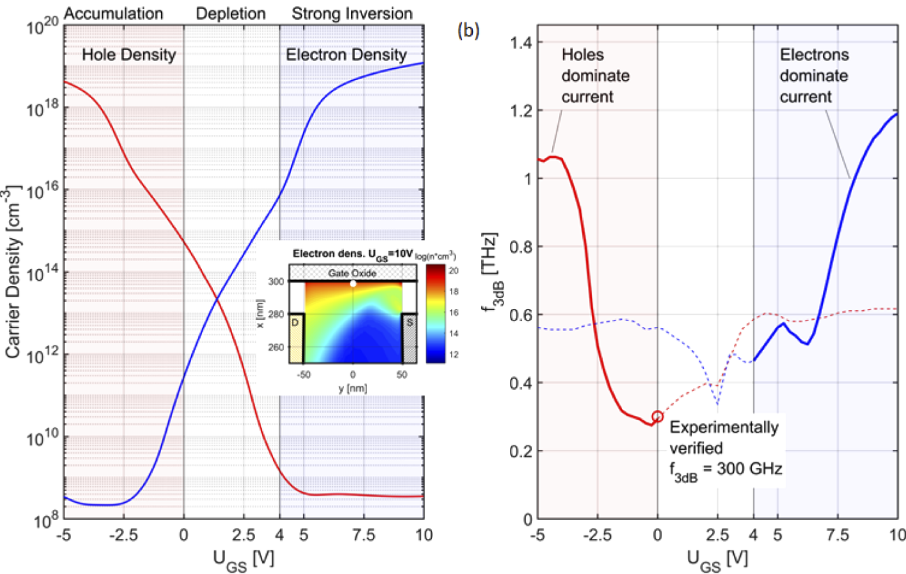

Fig. 3. Simulated carrier densities and optoelectronic bandwidth of FE-PIPED at a drain-source voltage $U_{DS} = 1.5$ V. (a) The carrier densities are displayed at the interface between the silicon and the gate oxide, in the middle between the source and the drain contact (white circle in the inset). The hole density (red curve) increases with negative gate voltages. The silicon is strongly inverted for gate voltages $U_{GS} > 4$ V, and a significant electron density is created (blue curve) in a channel below the oxide. When increasing the modulus of U_{GS}, the electron and hole densities increase up to 10^{19} cm^{-3}. The inset shows the shape of the electron channel for a strong bias $U_{GS} = 10$ V, which is asymmetric due to the drain-source bias voltage. (b) 3 dB limiting frequency for the case of a dominating hole current (solid red curve, $U_{GS} < 0$ V), and for a dominating electron current (solid blue curve, $U_{GS} > 4$ V). The bandwith of the FE-PIPED is predicted to increase beyond 1 THz at a gate voltage of $U_{GS} < -4$ V, and up to 1.2 THz at $U_{GS} > 10$ V. The dashed curves indicate the respective 3 dB limiting frequencies when hot minority carriers propagate through the majority-type channel. The red circle at $U_{GS} = 0$ V marks the measured 3 dB frequency of our PIPED in a previous publication [3], where the device has the same structure as in our present simulation. Simulation and measurement differ in this point by only 0.3%. However, there are kinks in the curves which stem from the fact that the transfer functions cannot be accurately approximated by simple RC lowpasses with well-defined limiting frequencies, which is especially true for frequencies below 0.5 THz.

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We explore the optoelectronic bandwidth as a function of the gate voltage. To this end, we define a time and space dependent electron-hole pair generation rate $g(t,x,y)$ in the silicon next to the apex of the Au electrode (drain) or, alternatively, next to the Ti source contact. We leave the generation rate $g(t,x,y)$ independent of U_{GS} and thus exclude the influence of the gate voltage on the tunneling and therefore on the injection rate. With forward bias $U_{DS} = 1.5$ V, the electron-hole pairs created close to the Au contact separate. The electrons will immediately vanish into the metal, and the remaining holes move under the influence of the electric field and create a current between the device terminals. This simulates the dynamic behavior of a light-induced hot-hole injection from the Au electrode into the silicon. An electron-hole pair created at the Ti contact approximates a light-induced hot-electron injection. The creation of an electron-hole pair instead of a single charge is a constraint imposed by the ATLAS simulation environment.

The generation rate g is defined as a Gaussian function both in time and space. The temporal and spatial widths are $2\sigma_t = 100$ fs and $2\sigma_{x,y} = 5$ nm, respectively. The spatial extension is small compared to the core width w, and the temporal impulse provides sufficiently high frequency components well above 10 THz. The magnitude of the generation rate g is adjusted such that the resulting current in a 1 µm long device corresponds to typically measured PIPED current in the µA region. The current response to the generation impulse can be Fourier transformed and results in a transfer function $H(f, U_{GS}, U_{DS})$, relating the frequency-dependent photocurrent $I_P(f)$ to a (hypothetical) modulated optical input power $P(f)$,

$$H(f, U_{GS}, U_{DS}) = \frac{I_P(f, U_{GS}, U_{DS})}{P(f)}. \quad (1)$$

We then extract the 3 dB limiting frequency, which we name (optoelectronic) bandwidth. Figure 3(b) shows the dependency of the FE-PIPED bandwidth on the gate voltage. The solid red curve indicates the bandwidth for a hole current which dominates for $U_{GS} < 0$ according to Section 2. The solid blue curve stands for the bandwidth if an electron current dominates. This happens after strong inversion and when the band bending favors hot electron tunnel injection from the Ti for $U_{GS} > 4$ V. Our measurements confirm that this condition is actually met, Sect. 5, Fig. 5(b).

Our simulations predict a PIPED bandwidth of 290 GHz for gate-source voltage $U_{GS} = 0$, red circle in Fig. 3(b). This is in good agreement with the measured bandwidth evaluated from a similar device described in a previous publication [3], where we found a bandwidth of 300 GHz. Applying a gate voltage increases the bandwidth gradually, because the bandwidth is determined first by the carrier transit time, but is gradually superseded for larger carrier concentrations by the much faster dielectric relaxation time. For large gate voltages $U_{GS} > 10$ V (which is tolerated without dielectric breakdown) the bandwidth increases to 1.2 THz.

Note that the reported increase in bandwidth from 0.3 THz to 1.2 THz of the FE-PIPED could in principle be also achieved by reducing the core width of a standard (without gate and transit-time limited) PIPED from $w = 100$ nm to 25 nm. However, the fabrication of a PIPED with such small dimension would be impractical: The optical coupling efficiency to such a small plasmonic waveguide would be very low, so that the sensitivity decreases significantly. Furthermore, the fabrication would become extremely challenging.

Our results indicate that the FE-PIPED has indeed the potential to outperform conventional Si-Ge photodetectors if T-waves are involved.

4. Device layout and fabrication

We fabricate and characterize FE-PIPED with gate contacts. The devices are prepared using a similar technique as described previously [7]. We repeat the essential fabrication steps for the convenience of the reader. We start with a silicon-on-insulator (SOI) substrate with 340 nm-thick device layer on top of a 2 µm-thick buried oxide (BOX). As a first step, the gate dielectric is

created by thermally oxidizing the top surface of the silicon device layer. The thickness of the oxide amounts to 80 nm, consuming 40 nm and leaving 300 nm of the Si device layer. This approach ensures excellent homogeneity of the oxide layer along with high resilience to dielectric breakdown. In future devices, the oxide could be replaced by a high-κ dielectric layer for further reducing the gate voltage. After oxidation, we coat the substrate with a negative-tone resist and structure the oxide layer with electron-beam lithography and dry etching to obtain a hard mask to fabricate the silicon optical waveguides. We use a CHF_3 etch, which is highly selective and consumes the oxide only, leaving the silicon unharmed. The second step comprises an undercut of the oxide hard mask in the region of the FE-PIPED device core and the adjacent mode converters using isotropic reactive ion etching (RIE) technology. In this step, we use an SF_6 etch at room temperature, which provides a high selectivity of etching silicon and leaving the oxide unharmed. This undercut creates a silicon strip with a wider oxide cap, see inset of Fig. 1(a). In the third step, we use a PMMA mask and angled evaporation to cover the sidewalls of the silicon strip with Au or Ti. During this step, the oxide cap in combination with the evaporation angle defines the spatial separation d of the gate oxide and the electrodes, see Fig. 1(b).

By design, the PIPED provides two independent optical inputs from opposite sides, but only one of them is required for a photodetector. The remaining one is hence abandoned and covered with a larger gold strip, which connects the gold cap with a remote contact gate pad, see Fig. 1(a) and Fig. 4(b). This electrode is created by Au evaporation normal to the substrate plane, which finally completes the metallization steps. A final anisotropic etch step with SF_6 at −110°C defines the optical waveguides.

Note that the devices used for the experimental exploration of underlying operating principles were purposefully designed to have rather large core widths of $w = 175$ nm, thereby allowing for a clear distinction between electron and hole currents. This, however, leads to a reduced sensitivity as compared to previously demonstrated PIPED with core widths of $w = 75$ nm [7]. The decrease of sensitivity for wider cores can be understood by considering the contributions of the two distinct metal-semiconductor interfaces to the overall photocurrent: For an essentially fixed penetration depth of the optical field in the metal electrodes, the proportion of power propagating in the metals becomes the larger, the smaller the core width w is. However, the Au electrode essentially guides the light, while the Ti electrode absorbs the light. If the electrodes are far apart, the light guidance effect at the Au-Si interface dominates and is essentially not affected by the Ti. If the electrodes are narrowly spaced, absorption is prevalent because the photons guided by the Au-Si interface are drawn towards the strongly absorbing Ti electrode. Specifically, for a core width of 100 nm, the Ti absorbs six times more power than the Au. In addition, the barrier height at the Ti-Si interface is smaller than its Au-Si counterpart, thereby leading to more efficient electron emission at the Ti electrode. At the same time, the reduction of the effective barrier width by applying a drain-source voltage is the larger, the smaller the core width is, i.e., the impact of the drain-source voltage on the carrier emission efficiency is stronger for smaller w. Hence, small core widths w lead to higher sensitivity.

5. Experimental setup and results

To experimentally verify the expected device behavior, we simultaneously measure the DC and the T-wave characteristics of the PIPED using the setup shown in Fig. 4(a). Two continuous-wave optical tones at frequencies f_1 and f_2 emitted by a pair of tunable distributed-feedback lasers (DFB1, DFB2) are superimposed using a 3 dB coupler and produce a power beat $P_{\mathrm{opt}}(t)$ at the difference frequency $f_{\mathrm{THz}} = |f_1 - f_2| = \omega_{\mathrm{THz}}/(2\pi)$,

$$P_{\mathrm{opt}}(t) = P_0 + \widehat{P_1}\cos(\omega_{\mathrm{THz}}t). \tag{2}$$

At the transmitter, this power beat feeds a reverse-biased InGaAs high-speed p-i-n-photomixer (Tx-p-i-n), the photocurrent of which drives a transmitter antenna. At the receiver, the T-wave is

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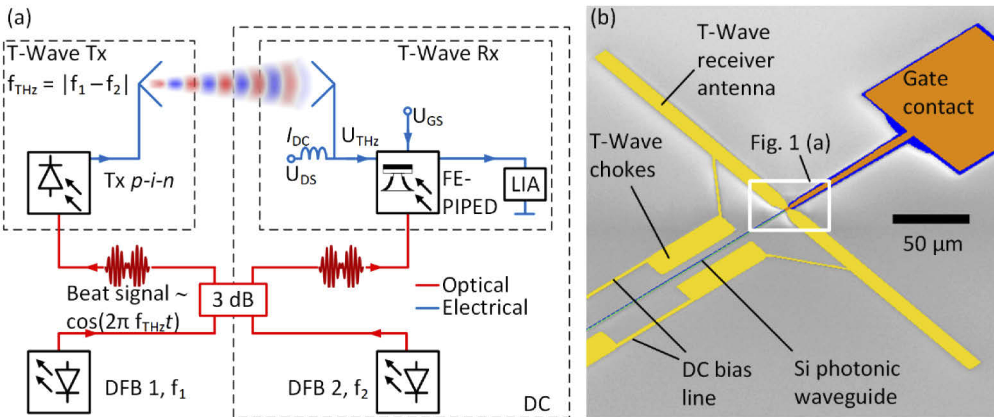

Fig. 4. Characterization scheme for FE-PIPED. (a) Two DFB lasers emitting near a vacuum wavelength of $\lambda_0 = 1535$ nm are tuned to slightly different optical frequencies f_1 and f_2. These emissions are superimposed to generate a power beat at the desired THz frequency, $f_{\text{THz}} = |f_1 - f_2|$. This power beat leads to a photocurrent $i(\text{t}) \sim P(t)$ in the Tx *p-i-n*-photodiode, which drives an antenna emitting the resulting T-wave (T-Wave Tx). At the T-wave Rx, the T-wave is coupled to the drain-source contact of the FE-PIPED, which is additionally biased by a DC voltage U_{DS} via on-chip T-wave chokes. The incoming T-wave voltage leads to a time-dependent modulation of the FE-PIPED sensitivity S with a modulation amplitude that is essentially proportional to the amplitude $\hat{U}_{\text{THz}}$ of the T-wave signal. The FE-PIPED is fed with the same power beat that is used to generate the T-wave signal, and the PIPED-photocurrent is coupled to a transimpedance pre-amplifier (TIA) via a bias-T. The TIA is not drawn for simplicity. This photocurrent partly results from the product of the time-dependent sensitivity and the time-dependent incident optical power, both of which oscillate at the same frequency f_{THz}, thereby enabling homodyne down-conversion of the T-wave signal. A lock-in amplifier (LIA) in combination with an amplitude modulation of the THz signal is used to distinguish the down-converted signal from the other components of the photocurrent. The experiment is repeated at various biasing conditions for the drain and the source of the FE-PIPED. (b) Scanning-electron microscope image of the PIPED T-wave receiver. The receiver antenna couples the incoming T-waves to the PIPED, which is optically fed via silicon photonic WG. Electrical contacts (DC bias line) are used to supply the DC bias voltages. T-wave chokes decouple the T-waves from the DC bias.

captured by a second antenna and coupled to the drain-source contact of the FE-PIPED, where it is superimposed with a static drain-source bias voltage U_{DS} using T-wave chokes, see Fig. 4(b). This leads to a modulation of the voltage-dependent FE-PIPED sensitivity S, the amplitude of which, within a small-signal approximation, can be assumed to be proportional to the amplitude $\hat{U}_{\text{THz}}$ of the received T-wave signal.

The FE-PIPED is fed with the same power beat as the *p-i-n*-photomixer. The photocurrent is then given by the product of the time-dependent sensitivity and the time-dependent incident optical power, both of which oscillate at the same frequency f_{THz}, thus leading to a homodyne down-conversion of the incoming T-wave signal using the optical power beat as a local oscillator, see Section 5.1 for a more detailed description. To distinguish the down-converted signal from the other components of the FE-PIPED photocurrent, we use a lock-in technique. To this end, we superimpose an amplitude modulation onto the T-wave signal by varying the reverse bias at the Tx *p-i-n* photodiode at a frequency of 12 kHz. A lock-in-amplifier (LIA) is then used to extract the corresponding signal component from the output of the transimpedance amplifier (TIA). The FE-PIPED is electrically connected with standard DC probes (GGB Picoprobe MCW-23-2820-1)

to a two-channel precision source measure unit (SMU, Keysight B2900A), which supplies the drain-source voltage U_{DS} and the gate-source voltage U_{GS}. In addition, the SMU records the DC part I_{DC} of the FE-PIPED current I through a bias-T. Parts of this setup (transmitter, antennas and LIA) belong to a commercially available THz spectroscopy system (Toptica Photonics, TeraScan 1550). For measuring the static FE-PIPED characteristic, we employ only the components enclosed in the dashed rectangle marked “DC” in Fig. 4(a). The optical power beat is coupled to the active part of the FE-PIPED through a grating coupler (GC), a silicon photonic waveguide (WG), and a photonic-to-plasmonic mode converter, see Fig. 1(a) and Fig. 4(b). The T-wave signal is so weak that it has no influence on the DC part of the photocurrent. The SMU measures this average DC produced by the optical power beat.

5.1. DC Characterization of FE-PIPED

The total FE-PIPED output current $I(U_{DS}(t),U_{GS})$ consists of the dark current $I_D(U_{DS}(t),U_{GS})$ and the photocurrent $I_P(P_{opt}(t),U_{DS}(t),U_{GS})$. The sensitivity $S(U_{DS}(t),U_{GS})$ depends on the applied voltages and describes the dependence of the photocurrent on the optical power (in the following we drop the time-argument for better readability),

$$I_P(P_{opt}, U_{DS}, U_{GS}) = S(U_{DS}, U_{GS})P_{opt}. \tag{3}$$

The total average current can be written as

$$I_{DC} = \langle I_P \rangle + I_D = S \left\langle P_{opt} \right\rangle + I_D, \tag{4}$$

where $\langle x(t) \rangle$ denotes a time average of the harmonic quantity $x(t)$ over one period of the T-wave oscillation. The DC sensitivity S is measured by recording the average current with and without illumination, and by relating the difference to the optical input power,

$$S = \frac{\langle I_P \rangle}{\left\langle P_{opt} \right\rangle} = \frac{I_{DC} - I_D}{\left\langle P_{opt} \right\rangle}. \tag{5}$$

Figure 5 shows the DC sensitivity of a FE-PIPED having a core width of $w = 175\,\text{nm}$ as illustrated in Fig. 2, with drain-source and gate-source voltages U_{DS} and U_{GS} as measurement parameters. Figure 5(a) visualizes the data as a color-coded plot with equidistant contour lines. For a drain-source voltage difference smaller than the built-in potential, $U_{DS} \leq \varphi_{bi} = 0.2\,\text{V}$, hot carriers entering the silicon core are dragged back to the respective metal electrodes, and the sensitivity is close to zero. For bias voltages $U_{DS} > \varphi_{bi}$, carriers emitted into the silicon core are pulled towards the opposite metal electrode, and the photocurrent increases with U_{DS}. Two distinct areas with a large sensitivity can be identified. In the upper left region of Fig. 5(a) with $U_{GS} < 0\,\text{V}$ and $U_{DS} > 1\,\text{V}$, hole emission from the gold electrode is favored by the band bending, which decreases the width of the Schottky barrier as depicted in Fig. 2(d). The upper right area with $U_{GS} > 6\,\text{V}$ and $U_{DS} > 1\,\text{V}$ is associated with strong electron emission from the titanium electrode as illustrated in Fig. 2(c). These areas are separated by a trench near $U_{GS} = 4\,\text{V}$ where the sensitivity is small. Figure 5(b) depicts the sensitivity along horizontal cut lines in Fig. 5(a), the color-coding corresponds to the coding of the horizontal lines in Fig. 5(b).

The dependence of the sensitivity on the gate voltage is not symmetric and reflects the interplay of different barrier heights and widths for the Au-Si (hole injection) and the Si-Ti interfaces (electron injection), of the influence of the different DOS, and of the photon absorption differences of titanium and gold, see Section 2 and Fig. 2(a). This is the reason why the minimum sensitivity is not found for $U_{GS} = 0\,\text{V}$. In summary, we see that the sensitivity is greatly increased by a gate voltage $U_{GS} \neq 0\,\text{V}$. The largest sensitivities are to be seen for $U_{GS} > 0\,\text{V}$ due to the stronger impact of a gate voltage on the electron emission at the Ti electrode. The maximum measured sensitivity of $60\,\text{mA/W}$ is obtained for $U_{DS} = 1.5\,\text{V}$ and $U_{GS} = 9\,\text{V}$, and it exceeds the value for

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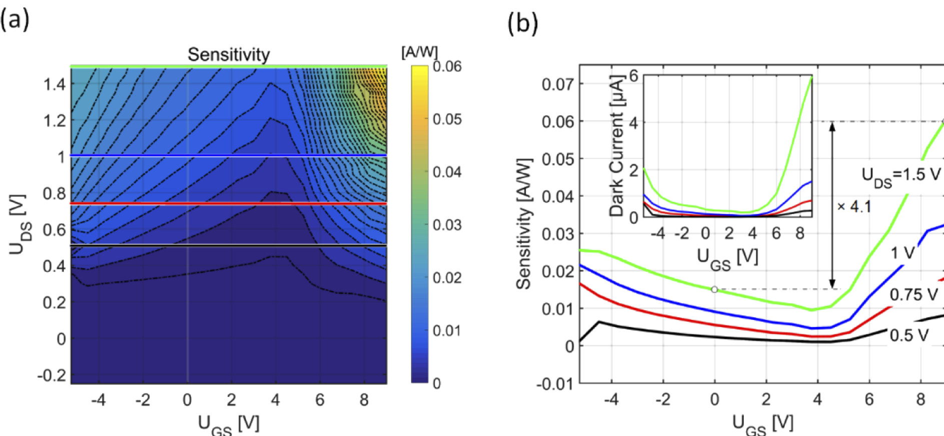

Fig. 5. Measured DC sensitivity for a FE-PIPED with core width $w = 175$ nm, operated at an average optical power of $P = 0.21$ mW in the silicon photonic feed WG. (a) Color-coded contour plot of sensitivity S as a function of drain-source voltage $U_{\rm DS}$ and gate-source voltage $U_{\rm GS}$. For $U_{\rm DS} < 0.5$ V, no significant sensitivity can be measured for any gate voltage. For $U_{\rm DS} > 0.5$ V, two distinct areas of large sensitivity can be identified. The left area corresponds to hole emission from the Au electrode for $U_{\rm GS} < 0$, Fig. 2(d), whereas the right area corresponds to electron emission from the Ti electrode for $U_{\rm GS} > 0$, Fig. 2(c). In between, near a gate voltage of $U_{\rm GS} = 4$ V, the photocurrent is minimum. (b) FE-PIPED sensitivity as a function of $U_{\rm GS}$ for constant drain-source bias voltages $U_{\rm DS}$ of 0.5 V, 0.75 V, 1 V, and 1.5 V, corresponding to the horizontal lines in (a). The maximum measured sensitivity of 60 mA/W is obtained for $U_{\rm DS} = 1.5$ V and $U_{\rm GS} = 9$ V and exceeds the value for $U_{\rm GS} = 0$ V by more than a factor of four ($\times$ 4.1). The minimum sensitivity is found near $U_{\rm GS} = 4$ V. The inset displays the dark current with the same color coding as the main graph.

$U_{\rm GS} = 0$ V by more than a factor of four. The minimum sensitivity is found near $U_{\rm GS} = 4$ V. Note that the FE-PIPED discussed here was intentionally designed to have a large width $w = 175$ nm of the Si core, see Section 4 for details. The wide core also reduces the dark current and allows for a wider range of gate voltages, which was instrumental to analyzing the full characteristics of the device. This, however, comes at the price of a reduced photoelectric sensitivity of only 15 mA/W without gate voltage, and 60 mA/W with an applied gate voltage. Both values are smaller than the sensitivity 120 mA/W previously obtained for a PIPED without a gate contact [7], but with a core width of only $w = 75$ nm.

We also tested FE-PIPED with a gate contact and smaller core widths, leading to sensitivities in the same range as reported before [7]. In particular, we have characterized an FE-PIPED with a core width of $w = 75$ nm, reaching a sensitivity of $S = 120$ mA/W with an applied gate voltage of $U_{\rm GS} = -3$ V and at a drain-source voltage $U_{\rm DS} = 2.5$ V. In our previous publication [7] for a similar device without a gate, we had to apply a higher drain-source voltage of $U_{\rm DS} = 3.25$ V to reach the same performance. We find that a gate voltage does not significantly increase the sensitivity for narrow-core devices. We attribute this result to the fact that the narrow core allows for an efficient tunneling injection already at moderate drain-source biases, and the further band bending due to the gate voltage does not significantly improve the tunneling efficiency as is the case for larger core widths. Note, however, that the gate voltage can improve the sensitivity slope $dS/dU_{\rm DS}$ of the FE-PIPED, which is key for an efficient T-wave down-conversion. This aspect is discussed in more detail in Section 5.2.

The measured dark current of the FE-PIPED is illustrated in the inset of Fig. 5(b). It follows the same general behavior as the photocurrent, with a minimum at $U_{GS} = 4$ V, followed by a steep rise for large negative or positive gate voltages. For $U_{DS} = 1.5$ V, the dark current is 320 nA without an applied gate voltage and it increases under the influence of the gate voltage to 2 µA at $U_{GS} = -5$ V and to 6 µA at $U_{GS} = 9$ V. While both the photocurrent and the dark current show a rise for larger gate voltages, the photocurrent increases significantly stronger.

For a noise estimate, we concentrate on $U_{GS} = 9$ V with a dark current $I_D = 6$ µA and a sensitivity $S = 60$ mA/W. To obtain a lower limit for the noise-equivalent power (NEP), we assume shot noise of the dark current to be the dominant noise source. Note the restrictions implied in our assumption: The two metal-semiconductor junctions are both subject to a random transition of carriers, which may be correlated – we neither account for this effect nor for any resulting frequency-dependence of the noise power spectral density. With these assumptions, we find a current power spectral density for the shot noise of the dark current of $2eI_D = 1.9 \times 10^{-24} A^2/Hz$, leading to an $NEP_{\text{shot, dark}} = \sqrt{2eI_D}/S = 23pW/\sqrt{Hz}$. We compare this result with the noise of an external impedance-matching resistor $R = 50\ \Omega$, having a noise current power spectral density of $4kT_0/R = 3.2 \times 10^{-22} A^2/Hz$ at room temperature $T_0 = 290K$, which leads to an $NEP_{\text{Nyquist}} = \sqrt{4kT_0/R}/S = 300pW/\sqrt{Hz}$. Because $NEP_{50\,\Omega} \gg NEP_{\text{shot}}$, we conclude that the dark current of the FE-PIPED does not significantly contribute to the overall noise as soon as the device is embedded into a 50 Ω-terminated T-wave circuit.

5.2. T-Wave characterization of FE-PIPED

If the drain-source voltage $U_{DS}(t)$ is modulated by a T-wave signal, the sensitivity $S(U_{DS}(t), U_{GS})$ will be time-dependent as well. Exploiting the fact that the photocurrent according to Eq. (3) is given by the product of the time-dependent sensitivity and the optical power, we may then use a time-dependent power beat $P_{opt}(t)$ according to Eq. (2) as a local oscillator (LO) for homodyne down-conversion of the T-wave signal to the baseband. In our experiment, the drain-source voltage consists of a strong DC bias $U_{DS,0}$ and a weak sinusoidal T-wave voltage $U_{THz}(t)$, which originates from the receiver antenna and which is superimposed onto the DC bias $U_{DS,0}$ by T-wave chokes, see Fig. 4(b). The drain-source voltage then reads

$$U_{DS}(t) = U_{DS,0} + U_{THz}(t), \qquad U_{THz}(t) = \widehat{U}_1 \cos(\omega_{THz} t + \varphi). \tag{6}$$

For a sufficiently small T-wave amplitude $\widehat{U}_1$, we may linearize the function $S(U_{DS}(t), U_{GS})$ in a small-signal approximation in the vicinity of the operating point $U_{DS,0}$,

$$S(U_{DS}(t), U_{GS}) = S_0(U_{DS,0}, U_{GS}) + \left.\frac{dS}{dU_{DS}}\right|_{U_{GS}} U_{THz}(t). \tag{7}$$

By combining Eq. (2), (3), (6) and (7), the baseband part of the photocurrent can be written as

$$I_{BB} = I_{BB,0} + I_{BB,1}, \qquad I_{BB,1} = \frac{1}{2} \left.\frac{dS}{dU_{DS}}\right|_{U_{GS}} \widehat{U}_1 \widehat{P}_1 \cos(\varphi(\omega_{THz})). \tag{8}$$

The phase $\varphi(\omega_{THz})$ describes the phase difference between the received T-wave, Eq. (6), and the phase of the power beat Eq. (2), and is adjusted for maximum $I_{BB,1}$ by slightly varying the THz frequency. Note that in Eq. (8) the direct current $I_{BB,0}$ can be separated from the mixing product $I_{BB,1} \propto \hat{P}_1(t)$ by modulating the transmitted THz power and using a LIA, see Fig. 4(a) and [3].

According to Eq. (8), the detected baseband current amplitude $I_{BB,1}$ is in proportion to the sensitivity slope dS/dU_{DS} for a given gate-source voltage U_{GS}. Evaluating the measured DC characteristic $S_0(U_{DS,0}, U_{GS})$ of Fig. 5(a), we compute this derivative and display the result

in Fig. 6(a). Two peaks of dS/dU_{DS} with a normalized value close to one can be seen, and we find a trench with a dS/dU_{DS} close to zero for $U_{GS} = 4$ V. Applying a gate voltage hence improves the efficiency of T-wave down-conversion and thus increases the mixing product $I_{BB,1}$. This is experimentally confirmed by directly measuring the baseband current amplitude $I_{BB,1} \propto dS/dU_{DS}$ as a function of U_{GS} and U_{DS}, see Fig. 6(b). The similarity to Fig. 6(a) is evident: There is a distinct maximum at $U_{GS} > 6$ V and $U_{DS} > 1$ V, a trench at $U_{GS} = 4$ V,

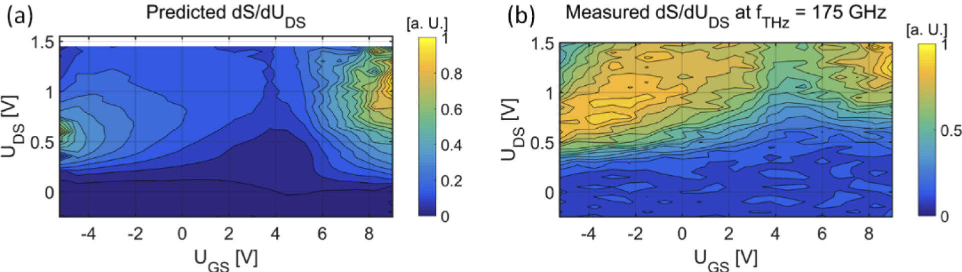

Fig. 6. Color-coded normalized derivative $dS/dU_{\mathrm{DS}} \propto I_{\mathrm{BB,1}}$ as a function of U_{DS} und U_{GS}. (a) Evaluation of the DC data from Fig. 5(a). Two plateaus with a normalized value close to 1 are to be seen, and a trench with a normalized value close to 0 for $U_{\mathrm{GS}} = 4$ V. (b) Measured normalized values from recording the baseband current amplitude $\hat{I}_{\mathrm{BB}}$. The general similarity of (a) and (b) is obvious. The influence of the field effect on the sensitivity is maintained even at T-wave frequencies.

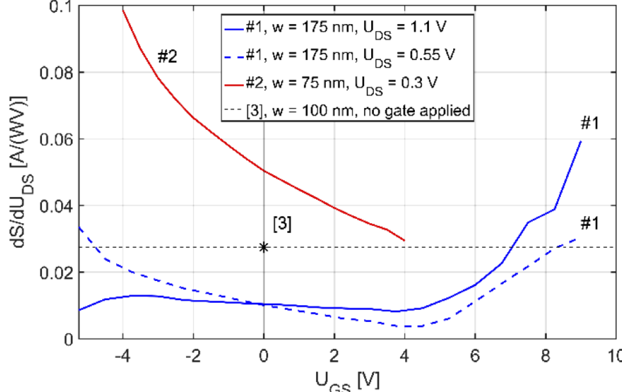

Fig. 7. Gate-source-voltage dependent sensitivity slope $dS/dU_{\mathrm{DS}} \propto I_{\mathrm{BB,1}}$ as measured for FE-PIPED with widths w of 75 nm and 175 nm. The sensitivity slope is evaluated from the measured DC characteristics $S(U_{\mathrm{DS}}, U_{\mathrm{GS}})$ according to Eq. (6). The solid and dashed curves denoted with #1 belong to the same device which also forms the basis of the analysis in Fig. 4 and Fig. 5. The two curves represent horizontal cut lines through the two pronounced maxima of Fig. 5(a) at $U_{\mathrm{DS}} = 0.55$ V (dashed) and $U_{\mathrm{DS}} = 1.1$ V (solid). The slope is largest for bias voltages of $U_{\mathrm{DS}} = 1.1$ V and $U_{\mathrm{GS}} = 9$ V and reaches $S_1 = 59$ mA/(WV). This value is six times larger than the one obtained for the same drain-source voltage and $U_{\mathrm{GS}} = 0$ V. It is also more than two times larger than the standard PIPED design used in [3], which is indicated with *. This device featured a width of 100 nm, but lacked a gate electrode and was hence operated without any gate-source voltage. The curve labeled #2 belongs to another FE-PIPED with a core width of $w = 75$ nm. For this device, the maximum sensitivity slope $dS/dU_{\mathrm{DS}} = 98mA/(WV)$ at $U_{\mathrm{GS}} = -4$ V is two times larger than the sensitivity slope at $U_{\mathrm{GS}} = 0$ V and three times larger when compared to the standard PIPED design used in [3].

and another plateau-like maximum towards smaller values of U_{GS}. Note that, for both of these maxima, the measured improvement of the down-conversion efficiency relative to the case $U_{GS} = 0$ V is not as pronounced as predicted by the evaluation of the DC characteristics. This aspect is subject to further investigations.

Figure 7 compares the gate-voltage-dependent sensitivity slope dS/dU_{DS} for FE-PIPED with core widths in the range 75 nm $\leq w \leq$175 nm. Without any gate voltage, $U_{GS} = 0$ V, the sensitivity slope dS/dU_{DS} becomes larger with decreasing width w. An applied gate-source voltage can strongly increase dS/dU_{DS} for each width considered. The sensitivity slope increases S with decreasing core width w. However, the dark current also grows with U_{DS} and could even destroy the device when a DC voltage is applied. This affects especially the devices with a small core width w. Hence, the explored range of gate-source voltages was limited. The largest dS/dU_{DS} in our experiments is measured for a width of $w = 75$ nm and reaches dS/dU_{DS} = 98 $mA/(\mathrm{W\,V})$ for bias voltages of $U_{DS} = 0.3$ V and $U_{GS} = -4$ V. This is two times the sensitivity slope without a gate voltage and a value more than three times larger when compared to our previously highest reported sensitivity slope dS/dU_{DS} = 27 $mA/(\mathrm{W\,V})$ for a device without gate and a core width of $w = 100$ nm [3]. Note that the device #2 in Fig. 7 was only measured up to a gate-source voltage of 4 V so that the increase of the sensitivity towards larger positive gate voltages is not visible. We believe that a systematic optimization of mode converter, core width, oxide thickness and choice of metals will allow to further increase the sensitivity slope and thus the efficiency of optoelectronic down-conversion of T-wave signals in FE-PIPED.

6. Design considerations

Based on our investigations, we believe that the performance of PIPED can be greatly improved both in bandwidth and in sensitivity by the addition of a gate contact. The key design parameters of the resulting FE-PIPED are the width w of the Si waveguide core and the vertical separation d between the upper edge of the drain and source electrodes and the oxide layer. Specifically, the photodetector sensitivity is the larger, the smaller the core width w becomes. We find that FE-PIPED with a width of $w = 75$ nm provide the highest sensitivity slope $\mathrm{d}S/\mathrm{d}U_{DS}$. However, in this case also the dark current increases so that a compromise has to be found. The feasibility of FE-PIPED with even smaller widths $w < 75$ nm is under investigation.

For the spatial separation d between the gate dielectric and the upper edge of the metal drain and source contacts an optimum value has to be found that avoids a practical short while still maintaining the effectiveness of the gate.

The T-wave down-conversion efficiency is significantly increased by a positive (large w) or a negative gate voltage (small w), which then leads to a more efficient hole injection for $U_{GS} < 0$ on the Au side, or to a more efficient injection of electrons for $U_{GS} > 0$ on the Ti side.

So far, the T-wave input circuit to the FE-PIPED feeds the T-wave to the drain-source contact leading to a sensitivity slope > 0.1 A/(WV). One could also think of coupling the T-wave signal to the gate-source contact. This, however, would reduce the sensitivity slope to a much lower value. The magnitude of the sensitivity slope for the case of a modulated gate-source voltage can be derived from the slopes of the family of curves in Fig. 5(b). For a device with a width of $w = 175$ nm, we expect a sensitivity slope below 0.01 A/(WV) throughout the complete range of gate-source bias voltage and for the maximum drain-source bias of $U_{DS} = 1.5$ V. However, this finding is constrained to FE-PIPED with a thermal oxide cap, as used in our experiments. The usage of a high-κ dielectric layer between the silicon and the gate contact might lead to a more favorable potential distribution in the silicon, thereby leading to a stronger effect of the gate voltage.

We expect that future work in these directions leads to improved systems for generation and detection of sub-THz and THz waveforms on the silicon photonic platform.

7. Conclusion

We introduce an extended concept for a field-effect-(FE-)controlled plasmonic internal photoemission detector (FE-PIPED). The field effect opens a new experimental access to the understanding of internal photoemission in plasmonic structures and of the associated carrier dynamics. Based on an improved understanding of the device physics, we perform simulations and show that the gate voltage can enhance the bandwidth of FE-PIPED to beyond 1 THz. We show experimentally that the gate field also increases the sensitivity slope, which is a key figure of merit for T-wave coherent reception.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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