Karlsruhe Institute of Technology

Elektrotechnisches Institut (ETI)
Prof. Dr.-Ing. Michael Braun
Prof. Dr.-Ing. Martin Doppelbauer
Prof. Dr.-Ing. Marc Hiller
Kaiserstr.12. 76131 Karlsruhe

Elektrotechnisches Institut

Title:	A Highly Integrated 25-Level Cascaded H-Bridge Active Filter for the Mitigation of High Order Current Harmonics
Authors:	Daniel Bernet, Marc Hiller
Institute:	Karlsruhe Institute of Technology (KIT) Institute of Electrical Engineering (ETI) Power Electronic Systems (PES)
Type:	Conference Proceedings
Published at:	PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management
Hyperlinks:	https://pcim.mesago.com/

A Highly Integrated 25-Level Cascaded H-Bridge Active Filter for the Mitigation of High Order Current Harmonics

Daniel Bernet, Rüdiger Schwendemann, Lukas Stefanski, Marc Hiller

Karlsruhe Institute of Technology, Institute of Electrical Engineering (ETI), Germany

Corresponding author: Daniel Bernet, daniel.bernet@kit.edu

Abstract

The increasing share of power electronics in the conversion and distribution of electrical energy represents a novel challenge for energy quality and supply stability. It is to be expected that high-frequency current harmonics will increase significantly with the number of grid-connected power converters. To reduce the associated disadvantages, this paper presents a 25-Level Cascaded H-Bridge Active Filter for mitigating converter-induced current harmonics in the kilohertz range. Compared to conventional active filters, the proposed use of a voltage-source active filter does not require high control bandwidth, tuning to specific frequencies or measurement and tracking of high frequency currents. The highly integrated design on printed circuit boards allows a high number of voltage levels and a high power density at small additional effort and costs. A 12 kVA-demonstrator is used to mitigate the switching frequency current harmonics of a grid-connected two-level converter, verifying the effectiveness of the active filter configuration.

1. Introduction

The current development trends of an increasing importance of regenerative energy sources, energy storage and electric mobility are likely to increase the share of power electronics in the conversion and distribution of electrical energy. These applications use power converters that have a modulated, non-sinusoidal output voltage and operate with control loops of different bandwiths, causing current harmonics over a wide frequency range. As a result, a significant increase in the use of grid-connected power converters can lead to harmonic instability and possibly to an interruption of the power supply through interaction with other grid equipment [1]. To ensure stable grid operation and high voltage quality even under these conditions, more demanding harmonic limits are discussed [2] and likely to be introduced in future grid standards.

Grid-connected power converters in the low voltage range up to 1 kV typically operate at switching frequencies between 2 kHz and 20 kHz. Due to their limited harmonic performance, conventional passive [3] or active filters [4] are commonly used to meet the harmonic limits defined by applicable grid standards such as DIN EN 61000 [5] or IEEE 519 [6].

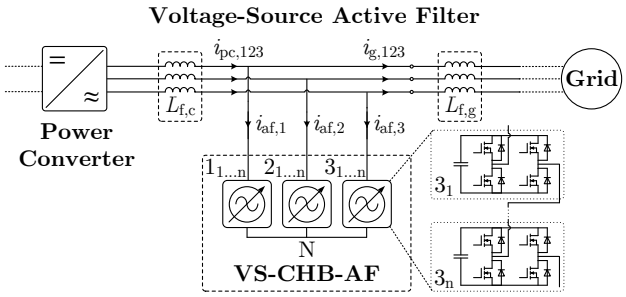


Fig. 1: Voltage-Source Cascaded H-Bridge Active Filter for the mitigation of converter-induced harmonics

These filters allow the mitigation of voltage and current harmonics, however the filter performance is often subject to a limited frequency range or a frequency dependent attenuation. The frequencies of converter-induced current harmonics, which occur at integer multiples of the carrier frequency, are typically higher than the frequencies that can be mitigated by commercially available active filters. For example, the GRIDCON ACF by MASCHINENFABRIK REINHAUSEN [7] allows the reduction of current harmonics with frequencies up to 2550 Hz. Considering more demanding harmonic limits of future grid standards, power converters would therefore require a high passive filtering effort to ensure compliance with the grid standards.

In order to overcome the aforementioned limited frequency range of conventional active filters, this work addresses the design and implementation of a Voltage-Source Cascaded H-Bridge Active Filter (VS-CHB-AF) according to Fig. 1. Unlike previous works on voltage-source active filters (VS-AFs) for passive loads [8–12], we introduced the integration of a low-power VS-AF into high-power grid converters in [13, 14]. Thus, the implementation of a coupled control scheme allows the active filter to mitigate the switching frequency current harmonics of the power converter. In this contribution, the layout and design of the VS-CHB-AF is carried out with the aim of achieving a high power density and voltage quality. Experimental results using the designed prototype show the mitigation of converter-induced current harmonics and thus demonstrate the significant potential as an alternative to conventional active and passive filter configurations.

2. Converter Design

This section presents the design process of the VS-CHB-AF. In a first step, the design requirements resulting from the application as VS-AF are derived in section 2.1. Based on these considerations, the determination of the number of cells and the DC-link capacitance is described in sections 2.2 and 2.3, respectively. The resulting PCB-design is presented in section 2.4, including a thermal analysis and the structure of the signal processing system.

2.1. Design requirements

The configuration of the proposed VS-CHB-AF is shown in Fig. 1. In comparison to widely used conventional shunt active filters [15–19], the VS-CHB-AF is connected to the power line without a coupling impedance. As a result, the voltage drop across the grid-side filter inductance and thus the grid current $\boldsymbol{i_g} = [i_{g,1}\ i_{g,2}\ i_{g,3}]^T$ is determined by the active filter output line-to-neutral voltage $\boldsymbol{v_{af}} = [v_{af,1}\ v_{af,2}\ v_{af,3}]^T$, the grid line-to-neutral voltage $\boldsymbol{v_g} = [v_{g,1}\ v_{g,2}\ v_{g,3}]^T$ and the filter inductance $L_{f,g}$:

$$L_{f,g}\frac{d}{dt}\begin{bmatrix} i_{g,1} \\ i_{g,2} \\ i_{g,3} \end{bmatrix} = \begin{bmatrix} v_{af,1n} \\ v_{af,2n} \\ v_{af,3n} \end{bmatrix} - \begin{bmatrix} v_{g,1n} \\ v_{g,2n} \\ v_{g,3n} \end{bmatrix} \tag{1}$$

Assuming an undistorted fundamental grid voltage $\boldsymbol{v_g} = {}^1\boldsymbol{v_g} = [{}^1v_{g,1}\ {}^1v_{g,2}\ {}^1v_{g,3}]^T$, the grid current contains only current harmonics caused by the active filter voltage. According to Kirchhoff's Current Law (KCL)

$$\boldsymbol{i_{af}} = \boldsymbol{i_{pc}} - \boldsymbol{i_g} \quad , \tag{2}$$

the active filter current $\boldsymbol{i_{af}} = [i_{af,1}\ i_{af,2}\ i_{af,3}]^T$ includes all harmonic components of the power converter current $\boldsymbol{i_{pc}} = [i_{pc,1}\ i_{pc,2}\ i_{pc,3}]^T$ which are not contained in the grid current, even without identifying individual harmonics. To achieve the mitigation of the converter-induced current harmonics and a sinusoidal grid current, the harmonic content of the active filter output voltage should therefore be as small as possible. A further analysis of the operation principle is not in the scope of this contribution and can be found in [13] and [20].

At the same time, in order to achieve a high power density and to allow the application in highly integrated utilities, the VS-CHB-AF should be designed with small dimensions. Therefore, the active filter design is carried out using a single printed circuit board (PCB) per phase-leg. The limited dimensions of a PCB in turn result in limitations of the maximum number of cells and DC-link capacitance, requiring a reasonable trade-off between voltage quality and power density.

2.2. Number of Cells

The ability of voltage-source active filters to mitigate high-frequency harmonics is determinded by the quality of their output voltage, as described in the previous section. According to Fig. 2, the weighted

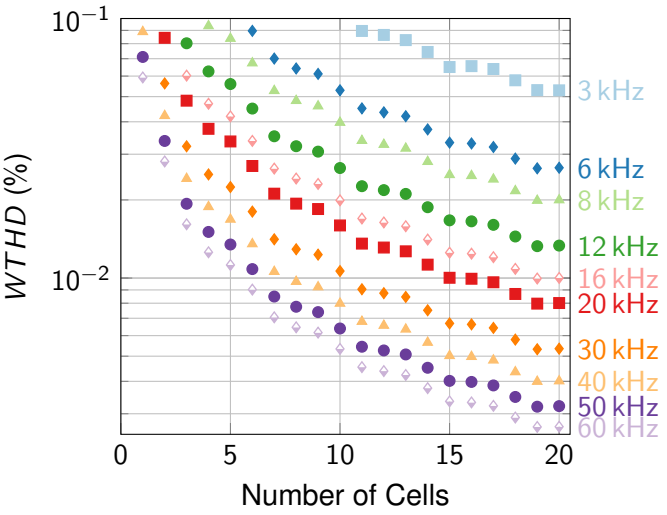


Fig. 2: VS-CHB-AF output voltage $WTHD$ as a function of the number of cells for switching frequencies in the range of $f_{sw,af} = 3\,\text{kHz} \ldots 60\,\text{kHz}$

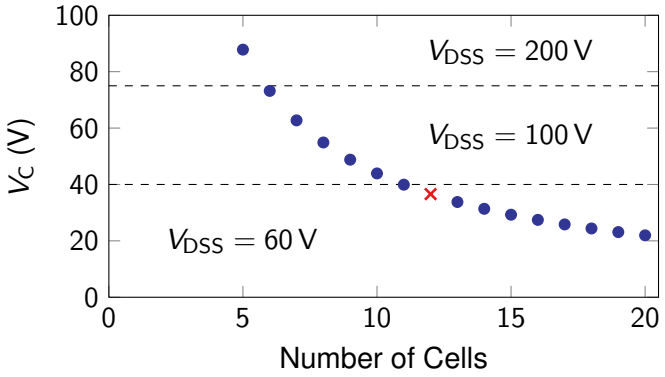


Fig. 3: Required cell voltage V_C as a function of the number of cells for use in the 400 V grid

total harmonic distortion (WTHD) and thus the harmonic content of the VS-CHB-AF output voltage decreases with increasing number of cells n at the same switching frequency $f_{sw,af}$. Considering the reduced voltage stress of the power semiconductors, the achievable switching frequency increases with the number of cells and thus allows a further reduction of the voltage WTHD.

The required cell voltage of the VS-CHB-AF depends on the rated grid voltage V_N and is given by

$$V_C = k_c k_g \frac{\sqrt{2}}{\sqrt{3}} \frac{V_N}{n} \quad , \tag{3}$$

where k_c and k_g are the coefficients for control and grid reserve, respectively. In order to ensure high dynamics and considering both the cell voltage deviation as well as the use of common mode voltages for energy control, the control reserve is set to 25 % ($k_c = 1.25$). With respect to applicable grid standards, a grid reserve of 10 % is provided by $k_g = 1.1$. Fig. 3 shows the required cell voltage V_C as a function of the number of cells according to eq. (3). A number of cells of 6 or lower would require metal-oxide-semiconductor-field-effect transistors (MOSFETs) with blocking voltages of at least $V_{DSS} = 200\,V$. A number of cells between 6 and 11 allows the use of MOSFETs with a blocking voltage of $V_{DSS} = 100\,V$, while for 12 or more cells a blocking voltage of $V_{DSS} = 60\,V$ is sufficient. Taking into account the high availability and low costs of 60 V-MOSFETs, the limited dimensions of a PCB layout as well as the impact on the harmonic content of the output voltage, the number of cells is chosen to be $n = 12$.

2.3. DC-link capacitance

In comparison to converter topologies with a common DC-link, the DC-link capacitors of CHB converters carry the full output current containing a fundamental frequency component. This leads to a significant energy pulsation in the phase arms. To allow the compensation of fundamental frequency reactive power in addition to the mitigation of current harmonics, the cell voltage deviation resulting from the fundamental frequency load current of the VS-CHB-AF has to be considered. Since the VS-CHB-AF has no DC-link supplies, a limitation of the cell voltage deviation can only be achieved by the cell capacitances.

Fig. 4 shows the schematic waveforms of the active filter considering the operation connected to a 400 V−grid. Due to the power factor of $\cos(\varphi) = 0$, when neglecting the power losses of the VS-CHB-AF, the voltage $v_{af,1}$ and the current $i_{af,1}$ have a phase shift of 90 degree. It is seen that the resulting phase-leg voltage deviation $\Delta V_{C,\sum}$ is alternating with double the fundamental frequency. The duration between the minimum and maximum cell voltage thus corresponds to a quarter fundamental period. The number of active cells in a phase-leg $x \in \{1, 2, 3\}$ is according to

$$n^*(t) = \frac{v_{af,x}}{nV_C} \tag{4}$$

determined by the output voltage, where the integer part of $n^*(t)$ is the number of static active cells and the real part corresponds to the duty cycle of a single switching cell within one sampling period. The average number of active cells during a quarter

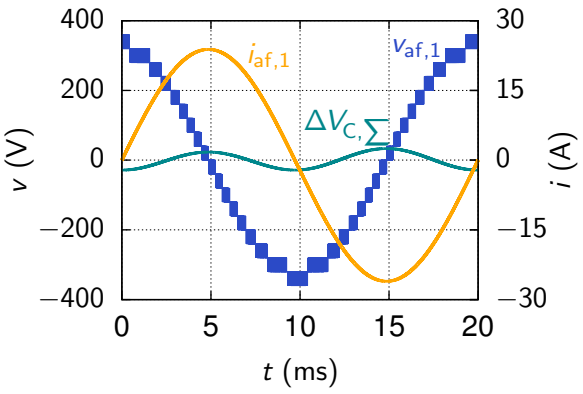


Fig. 4: Schematic waveforms of the voltage $v_{af,1}$, the current $i_{af,1}$ and the voltage deviation $\Delta V_{C,\sum}$

fundamental period can be calculated by

$$\overline{n} = \frac{4}{T} \cdot \frac{\hat{v}_{\mathrm{af},x}}{V_\mathrm{C}} \int_{t}^{t+\frac{T}{4}} \cos(\omega t)\,\mathrm{d}t = \frac{2}{\pi} \cdot \frac{\hat{v}_{\mathrm{af},x}}{V_\mathrm{C}} \tag{5}$$

where $\hat{v}_{\mathrm{af},x}$ is the amplitude of the reference output voltage and T is the fundamental period duration. It has to be noted that the charging current of the cell capacitances is equal to the sinusoidal output current $i_{\mathrm{af},x}$, similarly charging each active cell and thus leading to an effective capacitance of

$$C_\Sigma(t) = \frac{C}{n^*(t)} \quad . \tag{6}$$

The cell capacitance results in

$$C = \frac{1}{n\,\Delta V_\mathrm{C}} \int_{t}^{t+\frac{T}{4}} i_{\mathrm{af},x}(t) \cdot n^*(t)\,\mathrm{d}t \tag{7}$$

$$= \frac{1}{n^2\,V_\mathrm{C}\Delta V_\mathrm{C}} \int_{t}^{t+\frac{T}{4}} i_{\mathrm{af},x}(t) \cdot v_{\mathrm{af},x}(t)\,\mathrm{d}t \tag{8}$$

as a function of the number of cells n, the cell voltage V_C, the cell voltage deviation ΔV_C, the phase-leg output current $i_{\mathrm{af},x}$ and active filter output voltage $v_{\mathrm{af},x}$. A dimensioning according to eq. (8) requires an even distribution of the voltage pulsation within all cells of a phase-leg, which can be ensured with widely used sorting algorithms.

Fig. 5 shows the resulting cell capacitance according to eq. (8) as a function of the relative cell voltage deviation and the output current. It is seen that higher cell voltages allow lower cell capacitances at the same output current and voltage pulsation, since a reduced number of active cells according to (4) requires a lower cell capacitance to achieve the same effective capacitance according to (6). Taking into account the limited PCB size and the optimization of power density and output voltage quality, the cell voltage is set to $V_\mathrm{C} = 40\,\mathrm{V}$, corresponding to the upper limit for the application of $60\,\mathrm{V}-$MOSFETs in Fig. 3. To achieve a high output voltage quality and converter utilization, the maximum relative cell voltage pulsation $\Delta V_\mathrm{C}/V_\mathrm{C}$ is chosen to be $10\,\%$. Due to the high number of cells $n = 12$ that have to be placed on a single PCB, the maximum cell capacitance is limited by the dimension of electrolytic capacitors. Therefore, the cell capacitance is set

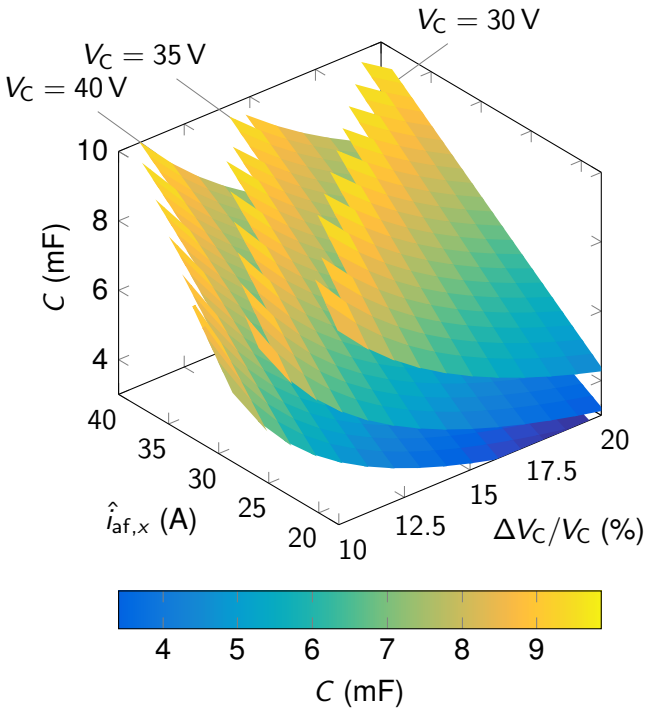


Fig. 5: Cell capacitance C as a function of the relative voltage pulsation $\Delta V_\mathrm{C}/V_\mathrm{C}$ and the current amplitude $\hat{i}_{\mathrm{af},x}$

to $C = 6\,\mathrm{mF}$, leading to a maximum output current of $\hat{i}_{\mathrm{af},x} = 25\,\mathrm{A}$ and a three-phase output power of $S_\mathrm{af} = 12\,\mathrm{kVA}$. According to (5), the average active cells are found by $\overline{n} = 5.2$, corresponding to less than half of the total number of cells. The resulting voltage reserve ensures three-phase energy control and voltage balancing using common mode voltages and sorting algorithms.

2.4. PCB Design

Fig. 6 shows the developed PCB of a 25L-CHB-AF phase-leg, achieving a power density of $4.1\frac{\mathrm{kW}}{\mathrm{l}}$. It is equipped with a Field Programmable Gate Array (FPGA) unit based on the *MAX10*-family of INTEL. To ensure an accurate voltage balancing, the *MAX10* receives the measurement signals of the twelve cell voltages and the phase-leg output current. Since the cells are galvanically isolated, the measurement is carried out with the isolated Delta-Sigma Analogue-Digital Converter (ADC) *AMC1204* by TEXAS INSTRUMENTS. For this reason, only one 1-bit data-stream per cell has to be evaluated by the *MAX10*. The measurement of the output current is performed using the current sensor LAX 100-NP by LEM. To avoid potential interference of the ana-

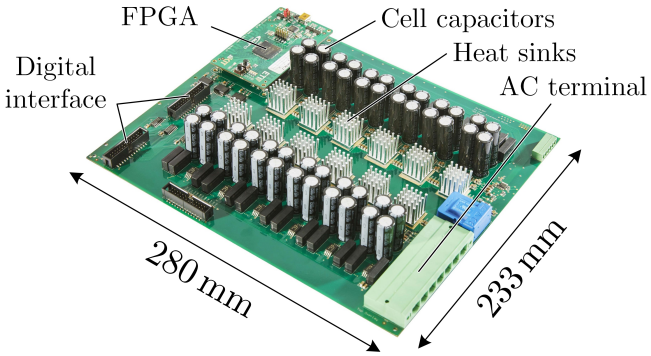


Fig. 6: Designed 25L-CHB-AF phase-leg

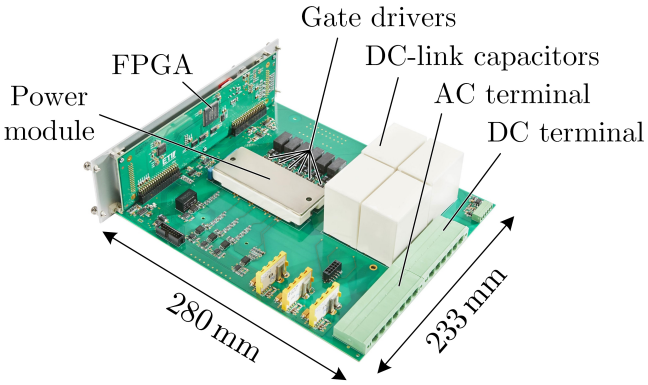


Fig. 7: Two-level converter (2L-VSC)

log signal, the ADC (*ADS8661* by TEXAS INSTRUMENTS) is placed directly next to the current sensor. The communication of the *MAX10* with a superordinate control unit is provided by a digital interface via ribbon cables. Alternatively, this communication can also take place via optical fibers via an external PCB that can be connected to the terminals of the ribbon cables. The galvanic isolation required for the communication with the CHB cells is provided by the ISOW7841FDWER by TEXAS INSTRUMENTS. Since adjacent cells can use a common isolated DC/DC-Converter, a reduction of the required converter volume is achieved.

For the heat sink design, the power losses of the used MOSFETs (*SQJQ960EL* by VISHAY) were calculated according to [21]. Taking the thermal conductivity of the PCB into account – since the MOSFETs are placed on the bottom side of the PCB under the heat sinks – the maximum permissible thermal resistance still allows the use of passively cooled heat sinks.

3. Experimental Results

Experimental results are carried out using the testbench setup according to Fig. 8. The demonstrator uses filter inductors with an inductance of 1 mH (7.9 %) for the converter and grid-side inductances $L_{f,c}$ and $L_{f,g}$, respectively, and a transformer with a voltage ratio of 200 V/400 V for the grid connection.

The active filter uses one 25L-CHB-AF PCB per phase-leg, as shown in Fig. 6, and is operated with a cell voltage of $V_C = 15\,\text{V}$ due to the transformer ratio. Due to a limited computing power of the signal processing unit, the active filter switching frequency is chosen to be $f_{sw,af} = 12\,\text{kHz}$. If required in certain applications, this frequency can be further increased, e.g. by outsourcing control tasks to the FPGA units [22]. The two-level voltage source converter (2L-VSC) used as grid-connected power converter is shown in Fig. 7. It uses the silicon insulated-gate bipolar transistor (Si-IGBT) *FS75R12KT4_B15* from INFINEON with a collector-

Tab. 1: Parameters of the hybrid converter demonstrator

	Parameter	Symbol	Value
System base values	Power	S_r	10 kVA
	Voltage	V_r	200 V
	Current	I_r	28.3 A
Power converter	IGBT voltage rating	V_{CES}	1.2 kV
	IGBT current rating	$I_{C,nom}$	75 A
	DC-link voltage	V_{dc}	350 V
	DC-link capacitance	C_{dc}	200 µF
	Switching frequency	$f_{sw,pc}$	3 kHz
Active filter	MOSFET volt. rat.	V_{DS}	60 V
	MOSFET curr. rat.	I_D	36 A
	Cells per phase-leg	n	12
	Cell voltage	V_C	15 V
	Cell capacitance	C_{af}	6 mF
	Switching frequency	$f_{sw,af}$	12 kHz
Filter Inductors	Inductance	$L_{f,c/g}$	1 mH
	Inductance (p.u.)	$L'_{f,c/g}$	7.9 %
	Resistance	$R_{f,c/g}$	48 mΩ
Transf.	Voltage ratio	v_t	0.5
Grid	Voltage	V_g	400 V
	Frequency	f_g	50 Hz

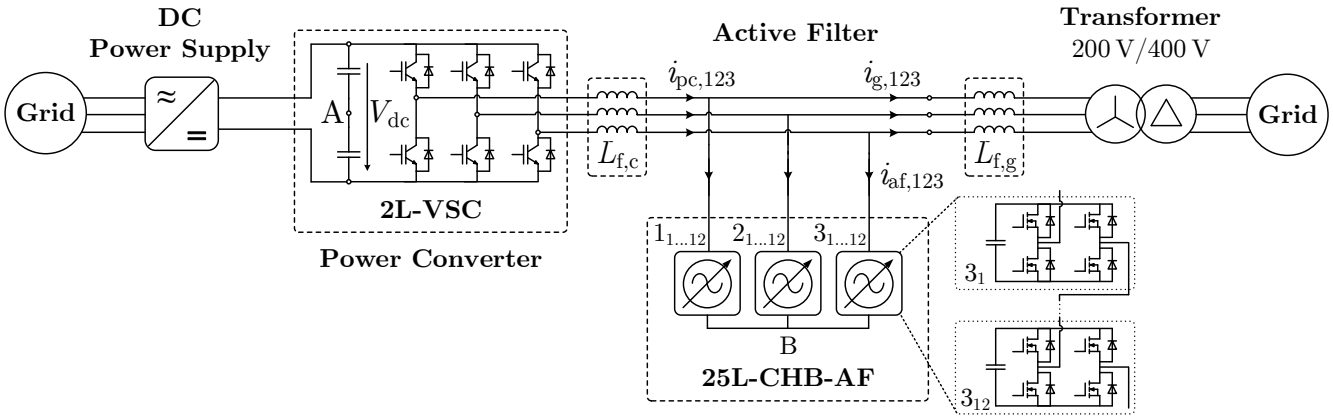
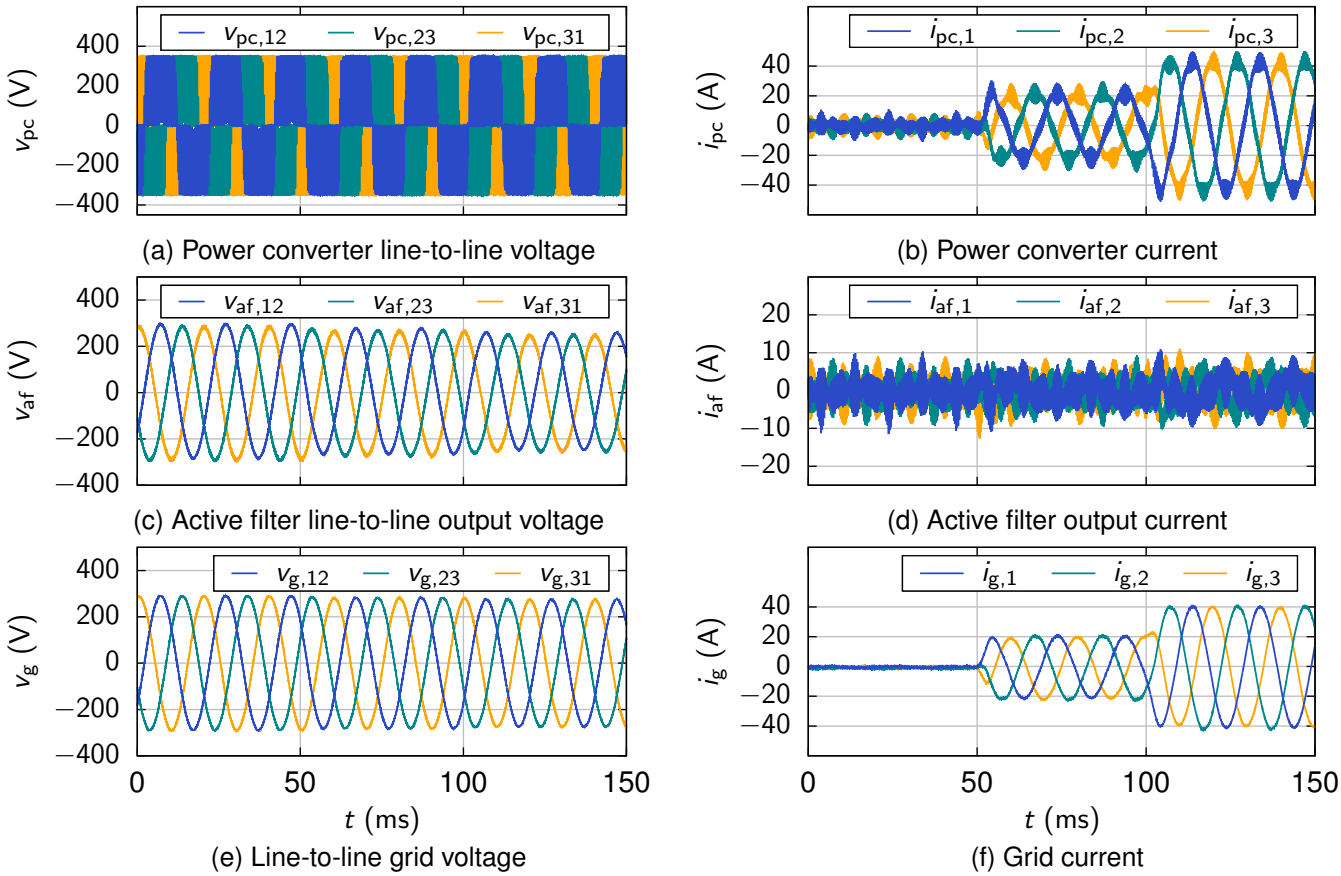


Fig. 8: Configuration of the testbench setup used for experimental verification of the desgined 25L-CHB-AF

emitter voltage of $V_{CES} = 1.2\,kV$ and a continuous DC-current $I_{C,nom} = 75\,A$. In addition, the converter platform includes the DC-link, gate drivers and a *MAX10* based FPGA unit. The 2L-VSC is operated with a DC-link voltage of $V_{dc} = 350\,V$ and a switching frequency of $f_{sw,pc} = 3\,kHz$. All relevant parameters of the testbench setup are summarized in Tab. 1.

Fig. 9 shows the experimental results of the proposed 25L-CHB-AF. Due to the low switching frequency and the two-level voltage shown in Fig. 9(a), the 2L-VSC output current in Fig. 9(b) has considerable switching frequency current harmonics. As a consequence, the total harmonic distortion (THD) of the power converter current results in 21 % at a grid



(a) Power converter line-to-line voltage

(b) Power converter current

(c) Active filter line-to-line output voltage

(d) Active filter output current

(e) Line-to-line grid voltage

(f) Grid current

Fig. 9: Experimental results of the grid-connected hybrid converter demonstrator measured with KEYSIGHT's *MSO 3034T* oscilloscope in high resolution acquisition mode

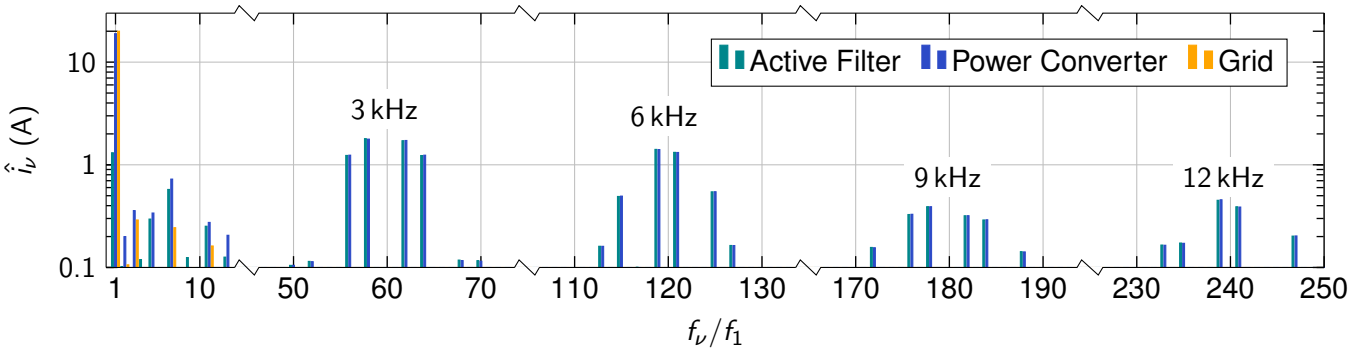


Fig. 10: Harmonic current spectra for $\hat{i}_g = 20\,\text{A}$ with the fundamental frequency $f_1 = f_g = 50\,\text{Hz}$ and the harmonic frequency $f_\nu = \nu \cdot f_1$

current of $\hat{i}_g = 20\,\text{A}$. Since the designed 25L-CHB-AF has a high number of voltage levels, the active filter voltage in Fig. 9(c) is nearly sinusoidal. According to eq. (1), this allows a nearly sinusoidal grid current shown in Fig. 9(f) with a THD of only $2.1\,\%$. Due to KCL in eq. (2), the active filter current in Fig. 9(d) corresponds to the difference between grid- and power converter current, given by the switching frequency current ripple of the 2L-VSC and a small fundamental current for loss compensation of the 25L-CHB-AF. This is illustrated by the harmonic spectra shown in Fig. 10: The active filter mitigates the switching frequency current harmonics of the power converter at the carrier frequency of $3\,\text{kHz}$. It is noteworthy that harmonics with a multiple frequency of the carrier frequency ($6\,\text{kHz}$,$9\,\text{kHz}$,...) are also eliminated by the active filter. Since the 25L-CHB-AF is operated with symmetrical sampling at a sampling frequency of

$$f_{s,af} = f_{sw,af} = 12\,\text{kHz} \quad , \tag{9}$$

the mitigated current harmonics with frequencies greater than or equal to $9\,\text{kHz}$ are above the active filter Nyquist frequency

$$f_{ny,af} = \frac{f_{s,af}}{2} = 6\,\text{kHz} \quad . \tag{10}$$

This can only be achieved by using a voltage-source active filter, since this configuration does not require measurement and control of high-frequency current harmonics. Thus, harmonics with significantly higher frequencies can be mitigated compared to commercially available active filters [7] or the use of multilevel converters in conventional shunt active filter configurations [19]. As a result, the proposed active filter configuration shows promising potential as an alternative to conventional filter systems for grid-connected power converters.

4. Conclusion

This contribution presents a VS-CHB active filter for the mitigation of high-order grid harmonics in the kilohertz range. The PCB-based converter design is carried out considering the trade-off between voltage quality and power density, leading to a 25-Level output voltage and a power density of $4.1\,\frac{\text{kW}}{\text{l}}$. As shown by experimental results, the proposed active filter configuration allows the mitigation of converter-induced current harmonics up to a frequencies larger than its Nyquist frequency of $6\,\text{kHz}$. Compared to conventional active filters, there is a significant increase in the compensated frequency range far into the switching frequency range of grid-connected power converters.

References

[1] X. Wang and F. Blaabjerg. “Harmonic Stability in Power Electronic-Based Power Systems: Concept, Modeling, and Analysis.” *IEEE Transactions on Smart Grid* 10.3, May 2019, pp. 2858–2870.

[2] M. Liserre, F. Blaabjerg, and S. Hansen. “Design and Control of an LCL-Filter-Based Three-Phase Active Rectifier.” *IEEE Transactions on Industry Applications* 41.5, Sept. 2005, pp. 1281–1291.

[3] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak. “A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters.” *IEEE Journal of Emerg-*

ing and Selected Topics in Power Electronics 4.1, Mar. 2016, pp. 54–69.

[4] B. Singh, K. Al-Haddad, and A. Chandra. "A review of active filters for power quality improvement." *IEEE Transactions on Industrial Electronics* 46.5, 1999, pp. 960–971.

[5] *Electromagnetic compatibility (EMC) - Part 2-2: Environment - Compatibility levels for low-frequency conducted disturbances and signalling in public low-voltage power supply systems*. Standard. German Institute for Standardization, May 2020.

[6] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*.

[7] *GRIDCON® ACF ACTIVE FILTERS – For Clean Grids. For any Environment.* Tech. rep. Maschinenfabrik Reinhausen, 2014.

[8] G. Joos, L. Moran, and P. Ziogas. "Performance analysis of a PWM inverter VAr compensator." *IEEE Transactions on Power Electronics* 6.3, July 1991, pp. 380–391.

[9] M. Routimo, M. Salo, and H. Tuusa. "Current sensorless control of a voltage-source active power filter." *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.* IEEE.

[10] M. Routimo, M. Salo, and H. Tuusa. "Control method to improve the transient performance of a current sensorless active power filter." *Nordic Workshop on Power and Industrial Electronics (NORpie), Lund, Sweden*. 2006.

[11] M. Ortuzar, R. Carmi, J. Dixon, and L. Moran. "Voltage-source active power filter based on multilevel converter and ultracapacitor DC link." *IEEE Transactions on Industrial Electronics* 53.2, Apr. 2006, pp. 477–485.

[12] M. Angulo, D. A. Ruiz-Caballero, J. Lago, M. L. Heldwein, and S. A. Mussa. "Active Power Filter Control Strategy With Implicit Closed-Loop Current Control and Resonant Controller." *IEEE Transactions on Industrial Electronics* 60.7, July 2013, pp. 2721–2730.

[13] D. Bernet, L. Stefanski, R. Schwendemann, C. Rollbühler, and M. Hiller. "Grid-Connected Voltage Source Converters with integrated Multilevel-Based Active Filters." *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE Sept. 2018.

[14] D. Bernet and M. Hiller. "Grid-connected medium-voltage converters with parallel voltage-source active filters." *IET Electric Power Applications* May 2019.

[15] P. Mattavelli. "A closed-loop selective harmonic compensation for active filters." *IEEE Transactions on Industry Applications* 37.1, 2001, pp. 81–89.

[16] P. Mattavelli and F. Marafao. "Repetitive-Based Control for Selective Harmonic Compensation in Active Power Filters." *IEEE Transactions on Industrial Electronics* 51.5, Oct. 2004, pp. 1018–1024.

[17] M. Liserre, R. Teodorescu, and F. Blaabjerg. "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame." *IEEE Transactions on Power Electronics* 21.3, May 2006, pp. 836–841.

[18] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg. "Frequency Response Analysis of Current Controllers for Selective Harmonic Compensation in Active Power Filters." *IEEE Transactions on Industrial Electronics* 56.2, Feb. 2009, pp. 337–347.

[19] E. Kontos, G. Tsolaridis, R. Teodorescu, and P. Bauer. "High Order Voltage and Current Harmonic Mitigation Using the Modular Multilevel Converter STATCOM." *IEEE Access* 5 2017, pp. 16684–16692.

[20] L. Stefanski, D. Bernet, M. Schnarrenberger, C. Rollbühler, A. Liske, and M. Hiller. "Cascaded H-Bridge based Parallel Hybrid Converter - A novel topology for perfectly sinusoidal high power voltage sources." *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*. IEEE Oct. 2019.

[21] U. Nicolai, W. Tursky, T. Reimann, and A. Wintrich. *Applikationshandbuch Leistungshalbleiter*. 2010.

[22] L. Stefanski, R. Schwendemann, D. Bernet, M. Widenmeyer, A. Liske, and M. Hiller. "Cascaded H-Bridge based Parallel Hybrid Converter – A new Voltage Source for Power-Hardware-in-the-Loop Emulation Systems." *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE Nov. 2020.