Transceiver ASIC in HVCMOS Technology for 3D Ultrasound Computer Tomography

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Abstract

3D Ultrasound Computer Tomography (3D USCT) is an imaging method for the early detection of breast cancer. It provides three-dimensional multimodal images of the breast. The new 3D USCT device developed currently at Karlsruhe Institute of Technology contains more than two thousand ultrasound transducers placed in a water-filled aperture where the patient submerges one breast. The ultrasound transducers are grouped as transducer array systems (TAS) of 18 receiver (RX) and transmitter (TX) elements. The transducer front-end electronics contain high-voltage (HV) and low-voltage (LV) amplifiers and switches which are implemented as an application-specific integrated circuit (ASIC). This contribution presents a patented mixed signal, multichannel, transceiver ASIC developed in a commercial 350 nm high-voltage CMOS (HV-CMOS) process. The HV-CMOS process provides low-voltage and high-voltage transistors that can be combined on the same substrate. The HV transistors can sustain voltages up to 120 V.

Keywords: application-specific integrated circuit, front-end electronics, medical imaging

1 Introduction

The previous prototype, 3D USCT II is displayed in Figure 1. For our new prototype, 3D USCT III, a larger opening angle and an enlarged aperture with a diameter of 36 cm will increase [3] the region of optimal 3D point spread function [1]. The aperture of ultrasound transducers is hemispherical. The hemispherical aperture can be rotated and translated (for USCT II and III) to increase the number of virtual transducer positions. The measured signals are the so-called A-scans (amplitude scans). Approximately spherical waves in emission and approximately spherical reception are used for full 3D imaging. The center frequency of the ultrasound pulses are approximately 1 to 2.5 MHz. In this work we will present an

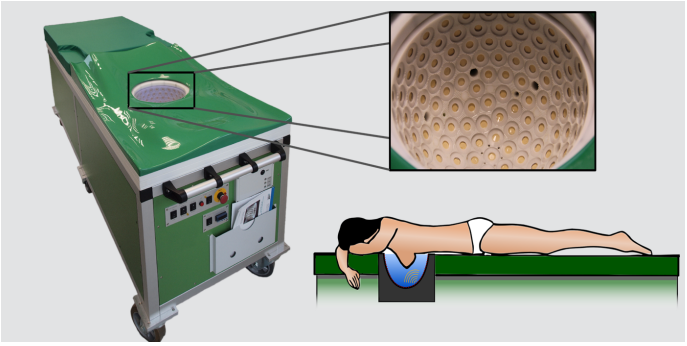

Figure 1: USCT II patient bed (left), transducer aperture (top right) and patient position (bottom right).

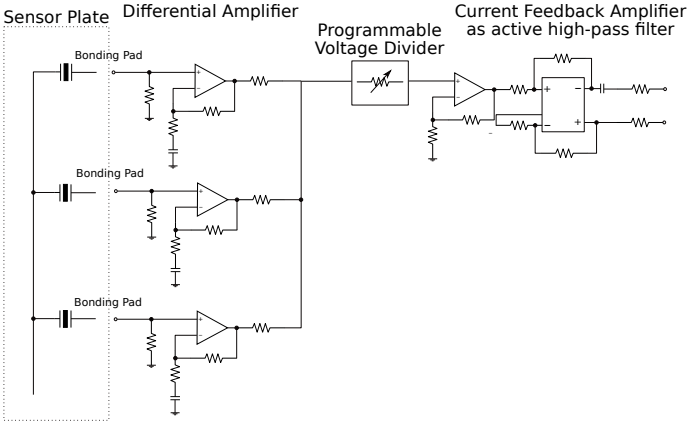

Figure 2: USCT II TAS receiver. Sensor plate, differential amplifier, voltage divider and current feedback amplifier as active high-pass filter [2].

integrated front-end solution. Using the transducer as emitter (TX) and receiver (RX). The TX applies high-voltage to the piezoelectric transducer generating ultrasound pulses. In the other direction, the RX amplifies the low signal amplitudes. An ASIC will be presented to solve these tasks. The development was started with the first generation ASIC consisting of one high-voltage (TX) and low-voltage channel (RX). The channel replaces the discrete step up converter, optocouplers and amplifiers of TAS USCT II emitter and receiver (see Figures 2 and 3). The ASIC features nine channels as required for USCT III and using a 3:1 multiplexer. The ASIC can be programmed with an micro-controller using the serial peripheral interface (SPI). A digital SPI decoder was also implemented in the ASIC.

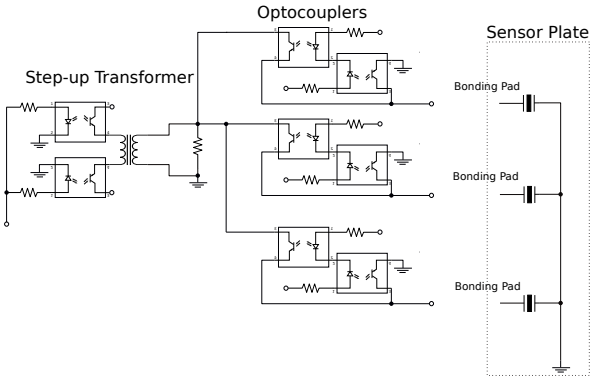

Figure 3: USCT II TAS emitter. Sensor plate, step up transformer, optocouplers [2].

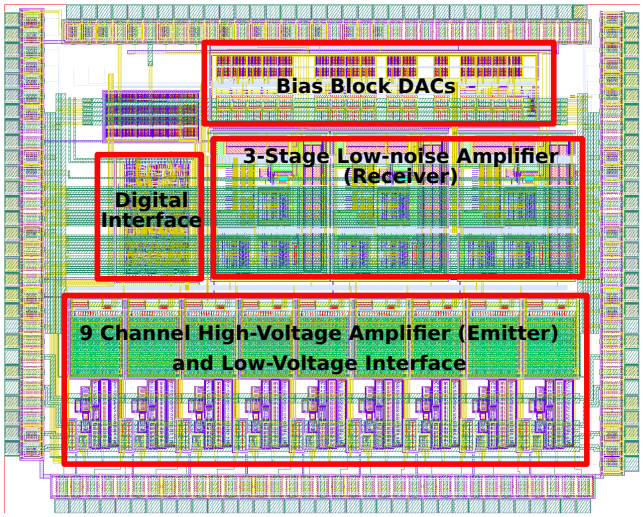

Figure 4: The ASIC consists of 3-stage low-noise amplifiers, noine channel high-voltage amplifier and digital interface and bias block.

2 ASIC Architecture

The ASIC (see Figure 4) consists of nine high-voltage amplifiers as TX elements and three low noise low-voltage amplifiers as RX elements. The high voltage amplifier is designed as an inverting amplifier with a gain of 20. It can generate signals with an amplitude up to 120 V. The 3-stage low noise amplifier is designed for amplification of signals from 10 μV to 10 mV with variable gain from 100 to 10000. In addition, the ASIC contains a digital interface for its configuration. This digital block implements the SPI decoder. The RX signals of 100 μV were amplified by the LV amplifiers up to 300 mV with a gain factor of around 3000.

Technology	AMS 350 nm HV-CMOS
Chip size	3.3 mm x 4.1 mm
High-voltage amplifier	Class AB amplifier (120 V transistors)
Low-noise amplifier	Inverting voltage amplifier, CR-RC shaper (3-stage)
Power consumption (high-voltage channel)	10 mW
Bias current	10 μA
Signal rise time	120 ns
3dB bandwidth	300 kHz - 6 MHz
Gain (high-voltage amplifier)	20
Gain (low-noise amplifier first stage)	40
Output related noise	121 μV
Input related noise	4 μV

Table 1: ASIC main characteristics [4].

The use of the ASIC offers the following advantages for USCT over a discrete component solution:

1 Low power design to avoid heating of the transducers

2 Small size design

3 Crosstalk reduction

4 More RX/TX channels

5 Cost effective solution

Table 1 shows the main characteristics of the ASIC. A simplified overview of the one input channel is depicted in Figure 5. One channel has an emitter stage, tune capacitances, 3-stage low-noise amplifier and switches to enable TX or RX. Figure 6 displays the simplified multichannel architecture with nine input channels and three output channels. The output channels are multiplexed with a 3:1 multiplexer stage.

2.1 High-Voltage Amplifier (TX)

To implement the emitter stage the step-up transformer was replaced by a transconductor and class AB amplifier stage. The transconductor performs a voltage-to-current conversion. The transconductor consists of a cascode differential amplifier (Figure 7) with two input transistors, cascode transistors and current mirror. The difference in their current values is proportional to the difference in the input voltages. Figure 7 shows a simplified schematic of the real implementation. Including the transconductor offset generation. The high-voltage

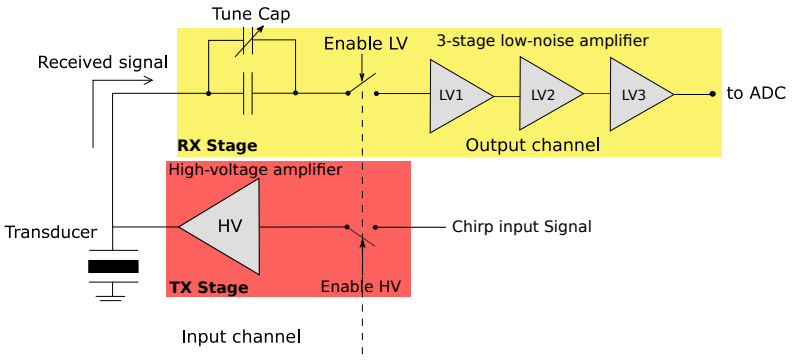

Figure 5: Simplified block schematic of one channel composed of an TX, RX stage, tune capacitances, HV and LV enable switches.

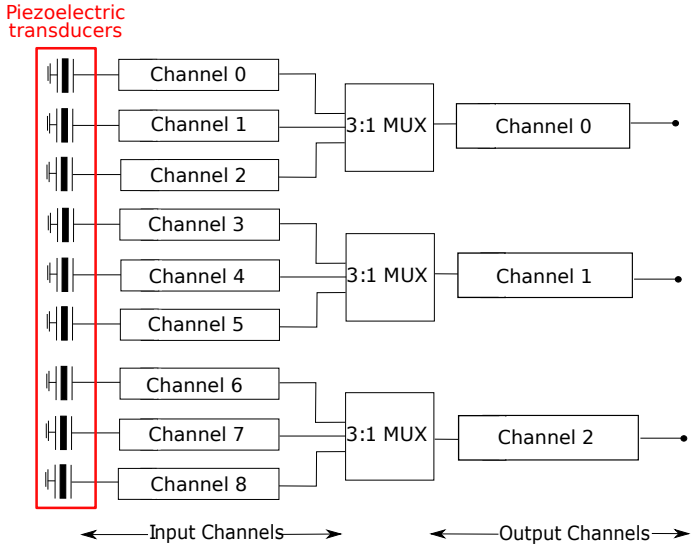

Figure 6: Simplified block diagram of the multichannel architecture [4].

amplifier requires an offset as voltage reference. In a next step the transconductor was connected to a source follower stage. To improve the circuit the current source must be replaced by a transistor. This type can be described as class B output stage. A class B stage has a distortion around the input voltage $V_{in} = 0$. In order to avoid the distortion an improved source follower stage with two diode-connected transistors was introduced. A stable voltage is achieved which shifts the operating points and the class B becomes a low distortion class AB amplifier (see Figure 8) [4]. The class A part of the amplifier has high gain and high linearity. This kind of amplifier has a 2π conduction angle. That means the amplifier remains active for 360-degree signal and the complete input signal is used. The class B amplifier consists of two MOSFET transistors (NMOS and PMOS). Each transistor is biased during

the positive and negative of a sinusoidal input signal. Here the signal gets pushed or pulled. As mentioned before, to overcome the distortion problem the combination of both structures are used [4].

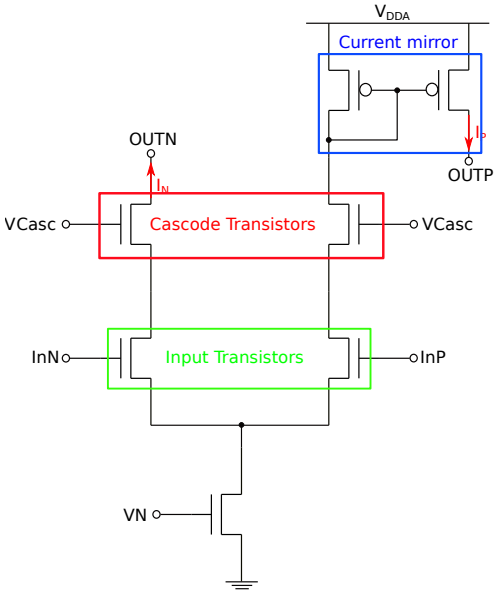

Figure 7: Transconductor circuit based on a cascode differential amplfier circuit (simplified) [4].

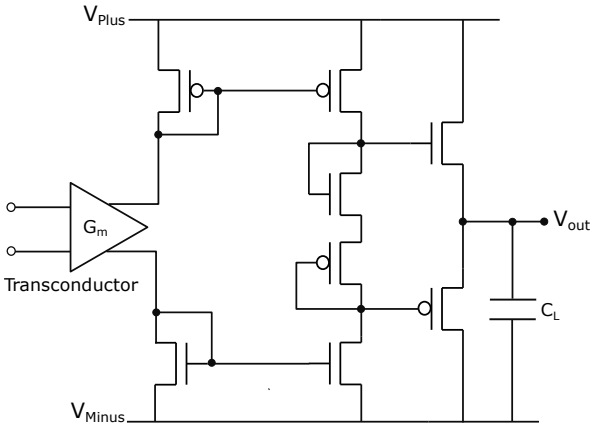

Figure 8: The high-voltage consists a class A and B stage in combination [4].

To verify the functionality of the emitter, various simulations like transient, large signal analysis, small signal analysis and noise were performed. The excitation signal used in

the simulations is the linear chirp signal. Such signal input is set to receive analog high-voltage signals, which can be provided by an external high-voltage transmitter. The chirp frequency increases linearly with time, so the frequency response of this signal has a constant amplitude. In the simulation a high-voltage of $\pm$48 V was used. The amplifier with a closed loop gain of 20 can deliver an output of 96 V peak-to-peak. The closed loop was realized as DC feedback. The TX emitter is implemented as an inverting amplifier (see Figure 9) with three outputs. Two of them are fed to the feedback with a feedback capacitance to increase the stability. To simulate the piezoelectric transducer an equivalent circuit was used as load for the TX emitter. An impedance analyzer was used to determine the LCR parameter. It contains an LCR series network and three parallel capacitances forming the capacitive load. This type of circuit can be handled as series resonant circuit. Note, to guarantee maximum gain and high linearity a parameter sweep of all bias parameters must be performed. Figure 9 shows the simulation circuit of the TX emitter as inverting amplifier topology [4].

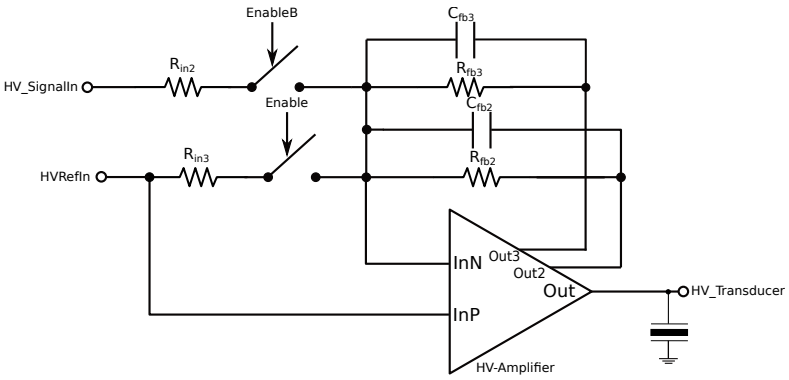

Figure 9: TX emitter amplifier works as an inverting amplifier. The feedback capacitance are used to improve the stability.

2.2 Low-Voltage Amplifier (RX)

The ultrasonic signal received from the piezoelectric transducer has low signals in order of 1 μV to 100 μV. To amplify such small signals a 3-stage low-noise amplifier was designed (see Figure 10). A 3:1 multiplexer selects one of three input receivers. The first stage achieves a gain of 100 where a inverting voltage amplifier with capacitive loads was chosen to achieve low-noise. The second and third stages are composed of CR-RC shaper topology. The simulated gain in the second stage can be chosen between 1-16 and for the third stage between 2-64. The amplifier is stable up to an amplification value of 5000. To set the gain, the tune capacitance can be switched in parallel to increase the gain factor. In the third stage the input capacitance can also be tuned. The outputs from stages 2 and 3 are fed into the a output selection logic. This logic is realized as a multiplexer [4].

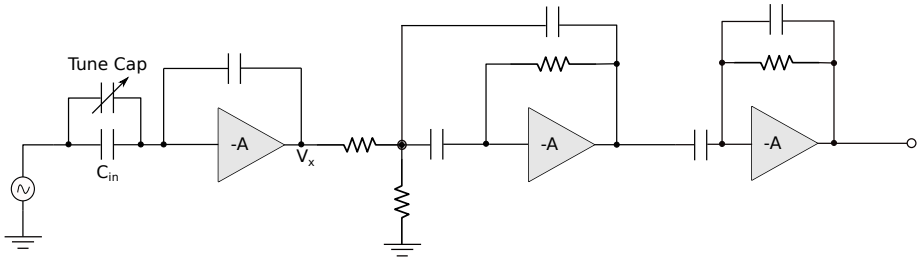

Figure 10: Simplified schematic of the 3-stage low-noise amplifier.

As core amplifier for the inverting voltage amplifier and CR-RC shaper a folded cascode topology (Figure 11) was implemented. This folded cascode is a single-ended amplifier with a PMOS as input transistor. The cascode transistors form an NMOS-PMOS structure. In addition, a load resistance is used to increase the voltage gain. Two outputs can be distinguished: one output refers directly to the cascode output and the second output is a source follower output. Generally, the idea of a cascode structure is to convert the input voltage to a current and feed the result to a common-gate stage [4]. The low-voltage path is activated through a select signal using the selection logic. The amplifier stages are designed to amplify signals starting from 100 kHz to 48 MHz at gain of 70 dB. A required frequency bandwidth between 500 kHz and 6 MHz is achieved [4].

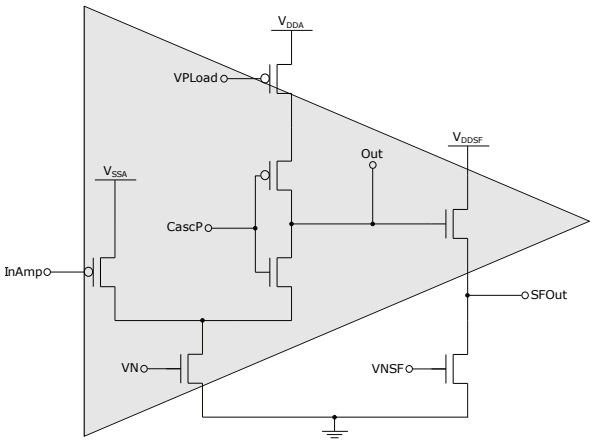

Figure 11: Folded cascode amplifier with PMOS as input transistor.

2.3 Digital Interface

To configure the ASIC an SPI (synchronous serial communication interface) was implemented as digital interface. A micro-controller is used to drive the SPI protocol. Further the micro-controller has a select line and a clock (SCLK) generated by the micro-controller. Generally, SPI devices communicate using a master-slave architecture. The SPI can select the ASIC using the select signal and acts as chip select. While data is being sent, the data written to the ASIC and is also read back. The clock is only enabled whilst these write/read operations to spare power consumption. To implement the digital interface it includes processes such as register transfer level (RTL) design, functional verification and synthesis. The backend process consists of floor planning, place and route, clock three synthesis, layout versus schematic (LVS) and GDS file generation.

3 Measurement Results

Recent measurements with prototype transducers are promising and fulfill the requirements of 3D USCT. The TX excitation, a linear chirp between 200 kHz to 4.7 MHz, was generated off-chip and amplified by the high voltage amplifier.

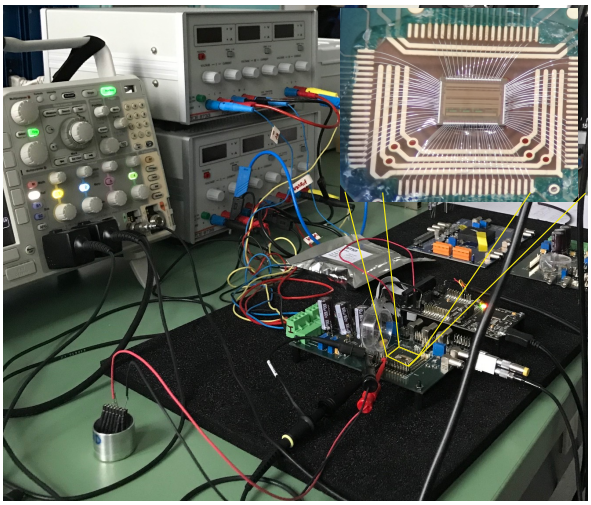

Figure 12: Measurement setup consisting of micro-controller and test board (yellow lines show the location of the ASIC bonded on the test board).

The test setup (see Figure 12) consisting of a micro-controller, test board where the ASIC is bonded and Qt test environment. The test board has several features to test all nine high-voltage and low-voltage outputs. For the measurement of the high-voltage amplifier an input

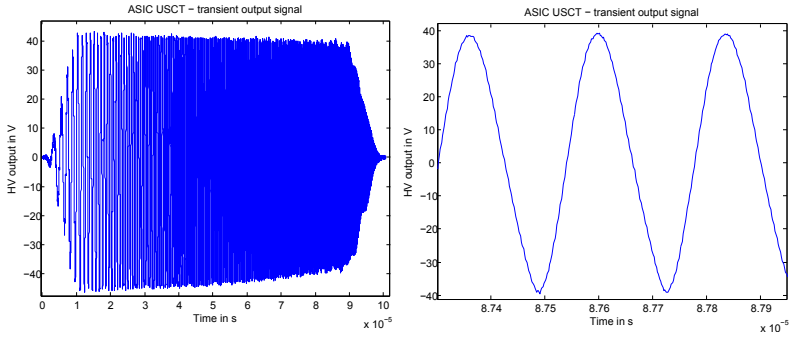

Figure 13: High-voltage output chirp signal (left). The output amplitude is 90.4 V (lower frequencies) and the measured gain is 18.4. Zoomed high-voltage amplitude (right) shows high linearity without distortions.

chirp signal (produced with a signal generator) with a sample rate of 40 MSa/s, amplitude of 4.9 V (peak-to-peak), offset of 1.4 V and an applied high-voltage of $\pm$48 V.

The measured high-voltage output is 90.4 V (Figure 13 left) at lower frequencies and the gain is 18.4. As expected high linearity (Figure 13 right) is given for low and high frequencies. The bandwidth between 200 kHz and 4.7 MHz is maintained. The Fast Fourier Transform (FFT) in Figure 14 shows the behavior of the output signal with respect to the input reference signal. The amplification is relatively constant with 18% drop in frequency range.

For the 3-stage low-noise amplifier measurements all low-voltage channels were activated. As explained in chapter 2.2 to obtain high linearity and a amplification of 3000 without oscillations of stage 3 a parameter set for tune capacitances and resistances was established. An input signal with the following parameters was used: rectangular waveform, frequency of 1 MHz, input amplitude of 1 V. The injection capacitance per channel on-chip was 1 fF. With the injection scheme the input signal of the amplifier input corresponds to 100 μV. The stage 3 produced an output amplitude up to 300 mV (peak-to-peak) leading to an amplification of 3000. Stage 3 shows the expected behavior. With the rising edge of the rectangular input the output of stage 3 rises and with the falling edge the output of stage falls accordingly. To measure the crosstalk of the channels between channels 0, 1, 2 one of the three channels is active while all others are off. Table 2 shows the results.

Channel (active)	Crosstalk (V/dB)
0 (560 mV)	2.9 mV / 45.7 dB (Channel 1)
0 (560 mV)	2.7 mV / 46.3 dB (Channel 2)
1 (545 mV)	3 mV / 45.2 dB (Channel 0)
1 (545 mV)	2.8 mV / 45.8 dB (Channel 2)

Table 2: Crosstalk measurement of the low-voltage channels.

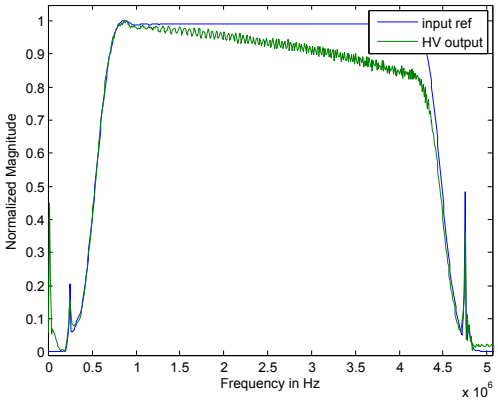

Figure 14: FFT of reference input chirp signal (blue line) and high-voltage chirp signal output (green line).

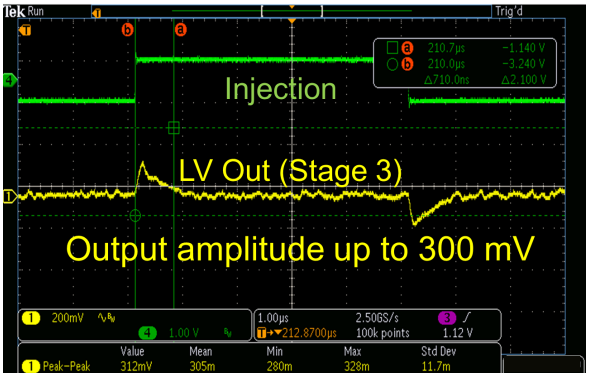

Figure 15: Injection input corresponds to 100 μV input signal. The calculated gain is 3000.

4 Conclusion

A new front-end electronic for USCT has been designed as an ASIC in 350 nm high-voltage CMOS technology. This ASIC is especially used for 3D USCT. The ASIC has nine channels consisting of high-voltage and low-noise amplifiers and a digital interface. The high-voltage transistors can sustain voltages up to 120 V. Simulations, design and measurements were presented in this paper. The ASIC enables with 18 combined receiver (RX) and transmitter (TX) elements. The performance of the high-voltage amplifier stage fulfills the USCT requirements. An output amplitude of 90.4 V and a bandwidth of 200 kHz to 4.7 MHz was achieved. Concerning the low-noise amplifier, a stable amplification up to 5000 was usable. A new version of this ASIC in 180 nm high-voltage CMOS technology is planned. This technology provides 200 V transistors. The same high-voltage circuit topology can be used. The number of channels in the new ASIC will be increased to augment the number of piezoelectric transducers.

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