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Specification, Control, and Applications of Z-Source Circuit Breakers for the Protection of DC Power Networks

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SPECIFICATION, CONTROL, AND APPLICATIONS OF Z-SOURCE CIRCUIT BREAKERS FOR THE PROTECTION OF DC POWER NETWORKS

by

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ABSTRACT

SPECIFICATION, CONTROL, AND APPLICATIONS OF Z-SOURCE CIRCUIT BREAKERS FOR THE PROTECTION OF DC POWER NETWORKS

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There is a highly-increasing demand for the DC power transmission and distribution in modern power systems for the integration of newly-installed renewable energy resources and storage systems to the existing utilities. Application of DC power systems in electric ships, battery energy devices, high-voltage DC networks, smart grids, electric vehicles, microgrids, and wind farms is a recent trend that is being highly investigated. The fault protection of DC systems is an essential but challenging issue that needs careful attention to maintain system operation reliability and device safety. In this research, the specification, control, and application of Z-source breakers (ZCBs) are investigated for DC network protection. Initially, the power loss associated with the topology of ZCBs is a key consideration in the design, and thus, the most efficient ZCB topology is identified. In this study, the topology of inter-cross-connected bi-directional ZCB (ICC-BZCB) was selected due to its least power loss when operating in a steady-state condition. Based on ICC-BZCB, a new approach of parameter specification is proposed by considering the reverse-recovery time of thyristors. The proposed approach ensures the turnoff action of ZCB in practical application. Its effectiveness was verified by experimental tests on a hardware testbed in the laboratory. Secondly, a new method of specifying the Z-source capacitances is proposed to identify the high-impedance faults in DC power networks. The method defines the principle of HIF detection and interruption by monitoring the status of Z-source capacitances. Finally, the assessment of cable length limit for ZCB application is analyzed for the DC system applications.

It has been found that the cable length limit decreases along with the decreasing fault current level, as well as the increasing power delivery level. The cutoff performance of the ZCBs is significantly impacted by the line parameters of the power cables. The outcomes of this research benefit the component design and application design of ZCB devices, which would promote the technology readiness level of ZCB's practice in the DC system protection.

To my loving parents

Yagya Raj Bhatta

&

Sharada Bhatta

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NOMENCLATURE

AC	Alternating Current
ACB	Arc-based Circuit Breaker
ACCB	AC Circuit Breaker
BZCB	Bi-directional Z-source Circuit Breaker
CB	Circuit Breaker
CLL	Cable Length Limit
DC	Direct Current
DCCB	DC Circuit Breaker
DFM	Digital Feeder Monitor
DG	Distributed Generator
ESR	Equivalent Series Resistance
GTO	Gate Turn-off Thyristor
HD-Mode	High Impedance Fault Detection Mode
HI-Mode	High Impedance Fault Interruption Mode
HIF	High Impedance Fault
HIFAS	High Impedance Fault Analysis System
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
ICC-BZCB	Inter-Cross-Connected Bi-directional Z-source Circuit Breaker
IEEE	Institute of Electrical and Electronics Engineer
IGBT	Insulated-Gate Bipolar Transistor

IGBT-CB	Insulated-Gate Bipolar Transistor based Circuit Breaker
IGCT	Integrated Gate-Commutated Thyristor
LCS	Load Commutation Switch
LVDC	Low-Voltage Direct Current
MOSFET	Metal Oxide Field-Effect Transistor
MTDC	Multi-Terminal Direct Current
MVDC	Medium Voltage Direct Current
PECB	Power Electronic Circuit Breaker
PV	Photovoltaic
RMS	Root Mean Square
SC-BZCB	Series-Connected Bi-directional Z-source Circuit Breaker
SCR	Silicon-Controlled Rectifier
SSCB	Solid-state Circuit Breaker
UFD	Ultrafast Disconnector
URB-BZCB	Uncontrolled-Rectifier-Based Bi-directional Z-source Circuit Breaker
UZCB	Unidirectional Z-source Circuit Breaker
VSC	Voltage Source Converters
ZCB	Z-source Circuit Breaker

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CHAPTER 1

INTRODUCTION

1.1 Direct Current Systems

The interconnection of microgrids with wind, solar, and plugin electric vehicles that leads to the formation of smart grids is the future of power systems. A DC network integrating DC-nature renewable energy sources and distributed generators can be a viable solution for renewable energy harvesting, local power reliability, and smart grid automation. Environmental and economic concerns led to the development of renewable energy sources and distributed generations in the past decades. Distributed energy resources such as solar and fuel cells are emerging in electric power systems as a part of DC microgrids/nanogrids, MVDC, and HVDC transmission and distribution networks. The electric grid is one of the largest infrastructure networks ever developed. The existing unidirectional electric grid originated in the late nineteenth century, where the electricity is delivered to the consumers through a complex electrical network involving the process of generation → transmission → distribution. The concept of microgrid as seen in Fig. 1.1 transforms the existing unidirectional electric grid to an active bidirectional network (i.e., generation → transmission → distribution → distributed generations) [1, 2].

DC microgrid with the advantages of lower line losses, high power quality, easy and flexible control is an effective solution to meet the growing demand for power utilization. It acts as an energy collection base for various renewable energy resources and distributed generators in modern power systems. It can provide a long-term sustainable solution for future energy demands. The DC microgrid systems' reliability and efficiency are higher than those of the AC systems [3]. Traditionally, AC systems were generally preferred for high-voltage, high-power transmission for

long-distance power delivery due to the affordability of power transformers. However, the advancement in power electronics technology, and the development of highly efficient AC/DC and DC/DC converters, have exceedingly increased the attraction of using DC systems. Also, applications such as DC or hybrid AC/DC grid networks with distributed energy resources [4, 5] and the MVDC power architecture of future naval vessels [6, 7] examines the implementation of DC power distribution system. The preliminary dissertation focuses on the application, advantages of DC loads/distribution systems along with the challenges, and possible solutions associated with the existing problem of DC network protection.

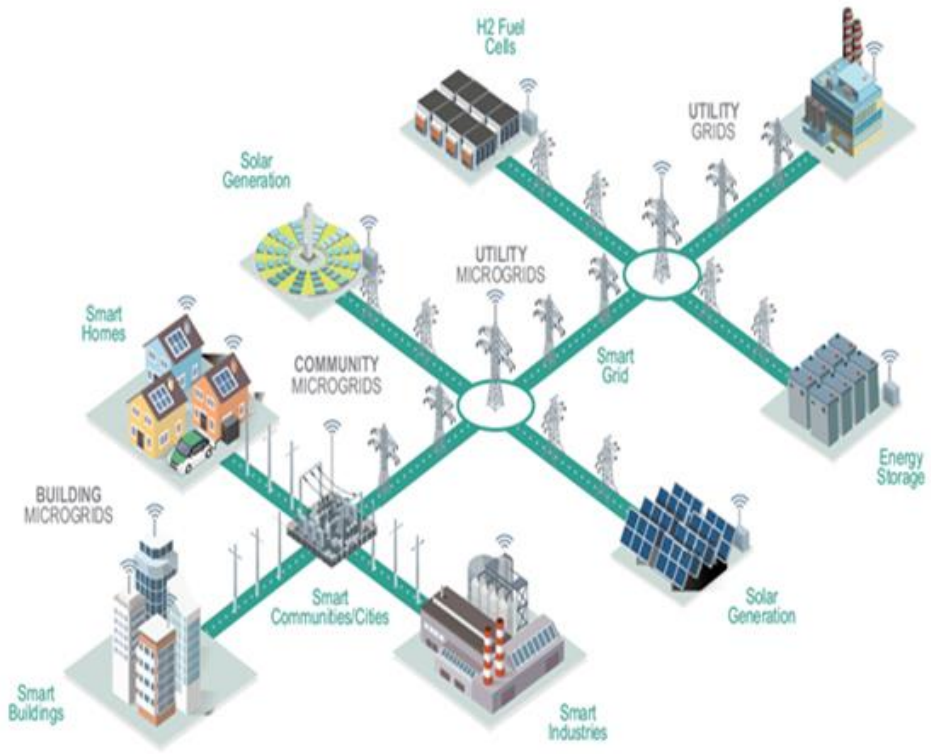


Figure 1.1 Microgrid Energy Systems [8]
(See Appendix A1 for copyright information)

1.2 Applications of DC System

Direct current devices operating from low to high voltage levels are widely implemented in modern society due to the advantages of reduction in the use of copper, higher controllability, lower cost, and easier interconnections. DC power supply is considered as a substitute electric power carrier for the increasing demand of energy utilization. The increasing interest in the DC distribution system is due to the rapid increase in DC type load and expansion of DC type distributed generation technology such as photo voltaic (PV) generation [9]. Low voltage applications utilizing DC power include charging batteries, automotive applications, consumer electronics, aircraft applications, electric vehicles, *etc*. A DC supply generated *via* solar cells, thermocouples, and batteries can be the power source to a portable solar system power in the photovoltaic industry.

Figure 1.2 Example of DC Loads

Fig. 1.2 shows some appliances employing DC power that we use in our day-to-day life. Nearly all commercial and residential energy is consumed in direct current. A high-voltage power transmission utilizes DC for the bulk transmission of current as high-voltage direct current (HVDC) systems are less expensive and more efficient. Lower emission levels and higher operating efficiencies have greatly enhanced the application of small distributed generation (DG) systems, typically around 100 kW, amongst industries and utilities [10]. Advancements in semiconductor technology have led to the exponential growth in DC systems. Voltage levels can be easily stepped up or stepped down using these semiconductor devices, which makes the DC system feasible, leading us towards the digital ages.

1.3 Advantages of DC over Traditional AC Systems

Implementation of various AC to DC converters can be avoided if a DC distribution network is employed as the primary electric grid for the power supply. Compared to a traditional AC grid, the DC distribution grid has proven to offer more efficient and reliable energy transfer [11]. Thus, the advantages of DC distribution over the traditional AC distribution include:

- Since DC has no frequency component, only real power is developed and delivered, whereas AC has both real (delivered) and reactive (absorbed) power. Thus, there is no need for reactive power compensation in DC power transfer.
- There is no skin effect for DC transmission; thus, the DC cable's entire diameter can be used for power transmission, whereas in AC distribution for 60 Hz system, only the outer 8.5 mm of the cable can be used for power transmission, which reduces the efficiency significantly.
- The problems with harmonics, unbalances, synchronization, and reactive power flows are eliminated for DC distribution systems.

- For a similar power transfer, corona loss is less in HVDC transmission lines than the HVAC transmission lines.
- Voltage source converters (VSCs) designed using the semiconductor devices are used to control the DC system, which acts to load changes in a fraction of nanoseconds. In contrast, the traditional AC system uses mechanical governors to correct any load changes requiring a longer time period.
- A fewer number of lines is needed for power transmission in a DC network, which reduces the overall power loss. The flow of power through a DC link is highly accurate and lossless.
- HVDC overhead lines have lesser interference with the nearby communication lines compared to an HVAC line.
- Over a specific distance, which is also known as the break-even distance, as seen in Fig. 1.3, the transmission of power in an HVDC line becomes cheaper than the HVAC lines.

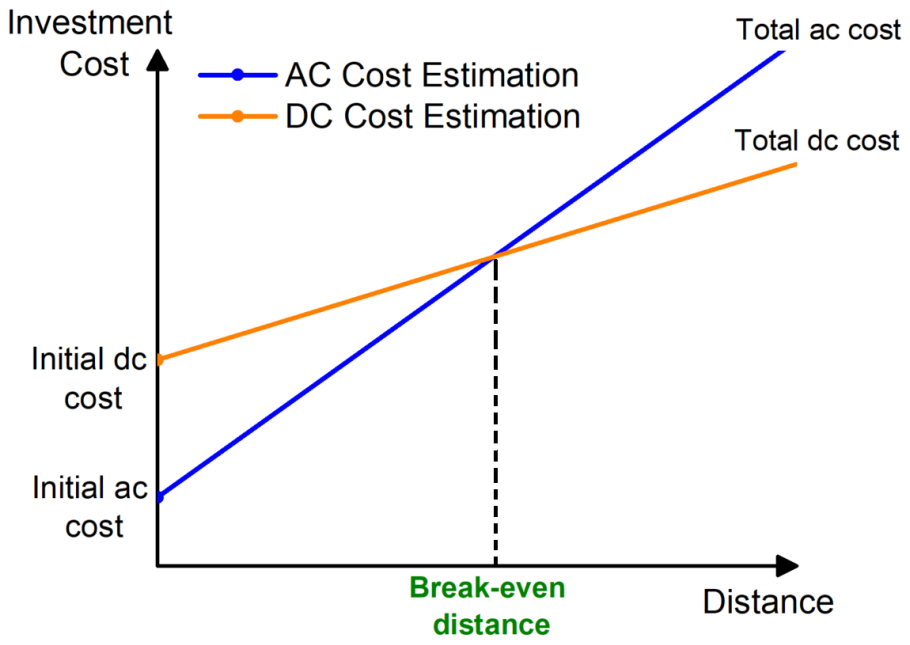


Figure 1.3 Transmission line distance vs. Investment cost for AC and DC systems

- Based on the neutral reference point arrangement, a DC system requires only two to three conductors. In contrast, the AC system requires a minimum of four conductors for three-phase operations, increasing the overall system's cost.
- HVDC line offers better voltage regulations due to the absence of inductance in DC, thus, offering greater controllability than HVAC.

1.4 Protection of DC Systems

The protection of DC systems by interrupting the fault current in the event of a fault is an important issue that needs to be addressed carefully. Protection is one of the important aspects that should be considered from the beginning of system design to achieve cost-effective operation and high system reliability. For a DC power system, the maximum available short-circuit current is the sum of that delivered by the charging system, battery, and loads (if applicable). The interrupting capacity or short-circuit current withstanding capability of a distribution system, or the overcurrent protection devices should be higher than the maximum short-circuit current available for the system voltage and ambient temperature [12]. The technology using DC power is not matured or developed and also lacks enough standards compared to AC, which makes the protection of the DC network more complex. Event-based protection is needed to ensure the protection of a DC distribution system under various circumstances since the DC system is more dynamic than the AC system [13]. The primary challenges associated with the protection of a DC system are lack of current zero-crossing point, cases of severe overvoltage while interrupting the large direct current, and the requirement of fast interruption speed. Due to the small system inductance, the fault current develops promptly in the DC distribution systems, which requires fast protection to improve the system reliability [14]. Thus, it is challenging to design a protective device that can detect, locate,

and interrupt the fault fast enough in a DC network to protect it from the impacts of the fast-rising speed of fault currents.

1.4.1 Lack of Zero-Crossing Point

Unlike the traditional AC systems, the DC system lacks a natural zero-crossing point. The zero-crossing in AC helps to extinguish the arc faster as arc energy reduces significantly near the current zero instant. The AC and DC breakers' requirements vary vastly due to the absence of a natural current zero-crossing point in the DC systems. The short-circuit currents in a DC system need rapid interruption and energy dissipation stored in the system's inductors [15]. A natural zero-crossing point occurs once every 10 milliseconds for a 50 Hz AC system and every 8.3 milliseconds for a 60 Hz AC system. Fig. 1.4 shows a repetitive current-zero crossing [16], which helps for the fault isolation in case of an AC fault by opening any mechanical switch that opens the contact far enough to overcome the voltage differential between the two switch contacts.

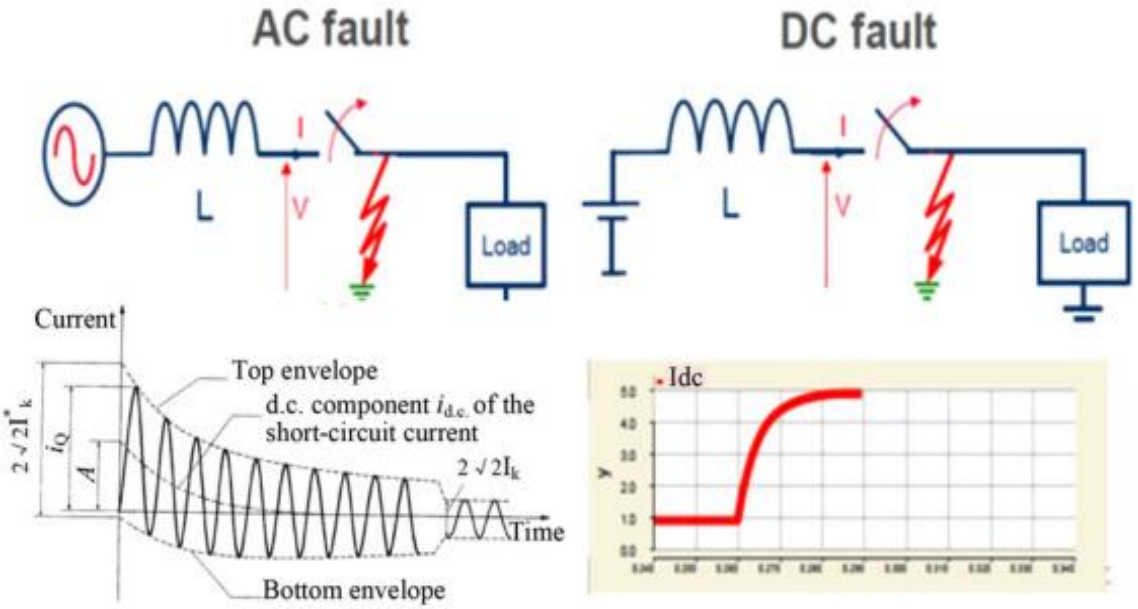


Figure 1.4 AC fault vs. DC fault
(See Appendix A2 for copyright information)

In case of a fault occurring in an AC system, the breaker arcs through the high current period and only attempt to clear the fault upon reaching a current zero point. A similar fault current isolation mechanism creating a zero-crossing point is needed for a DC circuit. The existing method uses an active or passive commutation circuit for creating a zero current level in the DC systems. Precharged capacitors are inserted across the main interrupter element through some switching devices in the active commutation method. The direct current in the interrupter is driven to zero when a surge current is encountered due to the capacitor's insertion. Likewise, a series LC circuit in parallel to the interrupter element forms a passive commutation circuit. A current oscillation in the LC circuit is achieved when the interrupter opens and creates an arc voltage. The capacitor used for the passive commutation circuit is not precharged. Now, using the negative resistance characteristics of the arc and with proper selection of the natural frequency of the commutating circuit, the current zero points are created when the current oscillations grow in the circuit. The resistive energy absorbers are connected in parallel to the interrupter in both active and passive commutation schemes in order to dissipate the additional energy remaining in the system. The passive commutation method is simple and more reliable compared to the active commutation method.

1.4.2 Interruption Speed

A DC circuit breaker (DCCB) can be broadly classified into mechanical and solid-state categories. A mechanical DCCB consists of a conventional AC circuit breaker (ACCB) parallel with the resonant circuit. The fault interruption time, *i.e.*, time from the fault inception to the instance of current interruption is typically 30 to 70 milliseconds for an AC system as standardized by *IEEE*. This time period is too long for DC networks' protection because a short-circuit fault occurring in a DC system can penetrate faster and deeper into the system since the DC system has

low impedance compared to the AC system. Likewise, the VSCs used in a DC system can supply the fault current greater than two to three times the nominal current for a few milliseconds. After this period, a voltage collapse is experienced in the system as the VSC converters cannot take fault current for such a long interval. Thus, a DC fault needs to be cleared in a fraction of milliseconds, which cannot be accomplished using a mechanical DCCB.

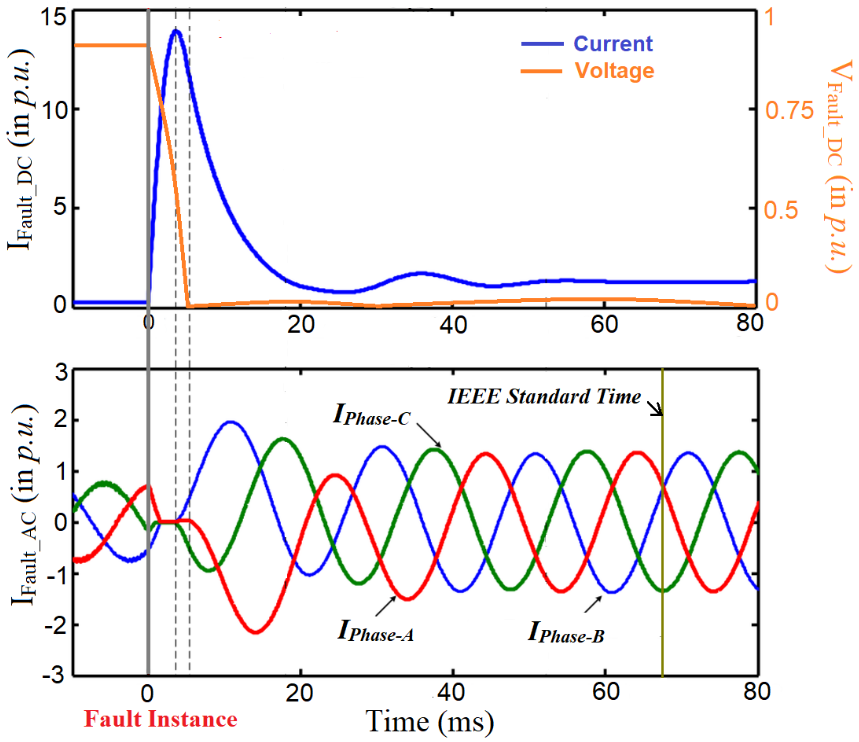


Figure 1.5 Fault clearance time in case of AC and DC faults

In the past decades, the superconducting fault current limiter has also been studied extensively to interrupt a DC fault [17]. A fault current level close to the rated values is easily interrupted using a superconducting fault current limiter at a sufficiently quick time. However, it lacks the ability to isolate the fault completely. When a superconducting fault current limiter is used in series with a mechanical DCCB, it can interrupt a fault current approximately 2 *p.u.* the

nominal current [18]. A major drawback of using this method is the high cost of superconducting components. Thus, solid-state breakers that can interrupt the fault current in a few milliseconds are studied to protect the DC network. Fig. 1.5 shows the fault clearance time required in the case of AC and DC faults [19, 20]. The ongoing research focuses on protecting a DC distribution system within a time frame as fast as 0.5 milliseconds.

1.5 Existing Solutions and its Associated Challenges

Several methods have been proposed to protect the multi-terminal DC (MTDC) systems [21, 22]. The methods studied for extinguishing the DC fault current include applying AC circuit breakers (ACCBs) on the AC side of the VSCs, IGBT circuit breakers (IGBT-CBs) at each end of the DC branch line, and IGBT-CBs placed between the DC network and each VSC. The handshaking method using an AC circuit breaker and DC switchgear was introduced in [23] to protect the VSC based MTDC system. However, due to slow system recovery, this method poses a significant threat to the protection of large scale MTDC systems. Thus, there are several ways that can be implemented for the protection of a DC system, as explained below.

1.5.1 Entire System Shutdown

DC faults can be eliminated from a system by de-energizing it. In this approach, the DC supply is switched off when a fault is encountered in the network. After the generation sources are off, the additional energy developed in the system is discharged through the fault. This method is suitable in the case of a two-terminal system or the HVDC system, where shutting down the whole system has the same effect as isolating the fault. However, in systems with multiple generations involved, shutdown to the entire system causes significant power loss. Also, a coordinated

shutdown is needed to secure all sources from the fault at the same time, especially, to protect any converter that supplies the fault current standalone in case of fault encountered in the system.

1.5.2 Fuses

Fuses are commonly used in low-voltage DC (LVDC) applications, ranging up to several hundred volts depending upon the system dynamics. A fuse characteristic depends on the current-time and voltage rates calculated in root-mean-square (RMS) values. It has the advantage of low cost and is commonly used for DC traction, mining, and battery protection. In case of fault encountered in a network, a fuse melts the metallic element present in it, creating an open contact for isolating the fault. However, a fuse cannot be used in HVDC applications since, for large current surges, the air between the two contacts of a fuse ionizes, forming a path for the fault current to flow. This causes the fault to remain uncleared. The other drawback of using a fuse is its malfunction in case of a slight overcurrent. A fuse should be quickly melted in case of a short time constant. However, for a larger time constant, a fuse's melting time becomes relatively long, which resists the arc from cooling in a quick time interval [24]. Also, predicting the voltage transient state and the rise-time constant of the current transient in case of fuse opening is difficult [25]. Thus, fuses cannot be considered as a viable solution for the protection of DC systems.

1.5.3 Circuit Breakers

A circuit breaker is a device that locally determines the fault and stops the current flow using a switch. It operates based on the current and voltage ratings given in the RMS value. The switch in a circuit breaker can be mechanical or solid-state. A circuit breaker responds to a fault faster than a fuse, is more reliable, and more sensitive. Unlike fuses, which only operate once, a circuit breaker can be used multiple times by simply resetting it after the breaker opens. It protects various fault conditions that include over-current, under-voltage, overpower, and rate of current

change. They are the most flexible and dependable circuit protection devices that work for all voltage levels. However, the fault isolation using a circuit breaker requires a careful inspection in highly inductive DC systems. There are several DC circuit breakers (DCCBs) that can be implemented for DC network protection.

1.5.3.1 Mechanical DC Circuit Breaker

The mechanical DCCB was initially studied in the 1980s [26, 27]. They utilize the technology of an AC circuit breaker. A mechanical DCCB creates a gap between the contacts whenever a fault is encountered in the system. The medium used for arc extinction between the two contacts can be air, vacuum, oil, or SF_6 gas. An arc is formed between the contacts due to the opening of the breaker which is counteracted and discharged through the parallel capacitor (C_c). The combination of C_c with an inductor (L_c) superimposes the oscillating current on the main fault current and thus, creating a zero-crossing point in the main fault current path as seen in Fig. 1.6 [28]. The excess energy generated from the transient surge is dissipated from the circuit as heat in the surge arrestor.

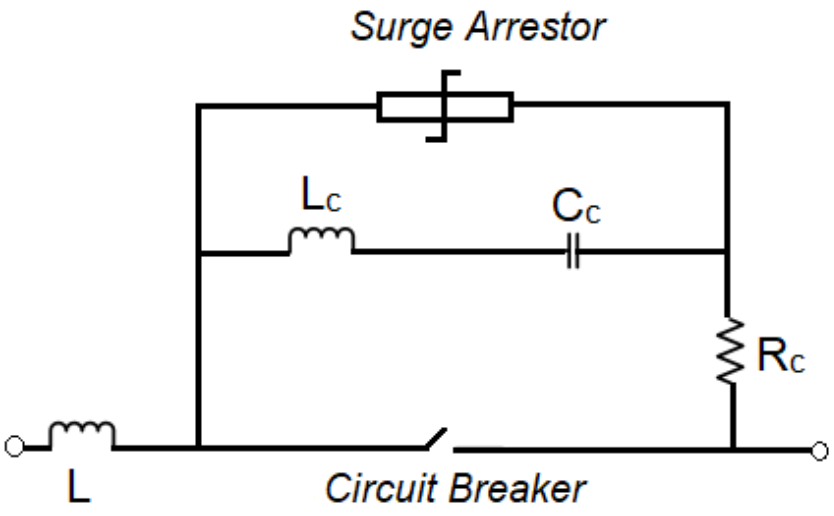


Figure 1.6 Mechanical DC circuit breaker

A mechanical DCCB with the ratings of 250 kV, 8 kA, and 80 kV, 10 kA has been studied in [27] and [29], respectively. For commercial use, smaller rated versions are available in the market. An accurate model of mechanical DCCB composed of a DC reactor, the main breaker, LC resonant circuit, an injecting switch, an arrester MOV, a residual switch, and a charging circuit involving a DC voltage source which is suitable for the grid level study of a DC grid is introduced in [30]. The advantage of using such circuit breakers is its higher efficiency and robustness. Since a mechanical DCCB does not involve any semiconductor devices, the on-state power losses are negligible. However, it has a slow response to faults which can cause major damage to the DC systems in an event of fault occurrence.

1.5.3.2 Solid-State Circuit Breakers

The solid-state circuit breakers (SSCBs) are like the mechanical circuit breakers but do not draw an arc when the breaker opens. It is also known as a power electronic protection device which can solve the limitations of fuses and traditional circuit breakers [31]. It opens a doped channel within the semiconductor device that stops the electron flow as the devices open. High voltage blocking capability, fast switching speed, and effective direct current interruption are notable features of an SSCB [32, 33]. It consists of a snubber circuit, as seen in Fig. 1.7 that absorbs the additional energy developed in the system during faults. The design considerations for a snubber circuit includes high reliability in low-voltage medium-capacity applications, low insertion impacts on fault current clearing, minimum cost and size, and less overvoltage stress on SSCB during the SSCB turn off process [34]. Various solid-state devices can be used for creating an SSCB, which includes silicon-controlled rectifier (SCR), insulated-gate bipolar transistor (IGBT), gate turn-off thyristor (GTO), integrated gate-commutated thyristors (IGCT), metal oxide field-effect transistor (MOSFET), and so on. The GTO application in an SSCB has an advantage of low

on-state voltage and high-voltage blocking capability [35]. Likewise, using IGBTs, an SSCB has a fast interruption time of microseconds along with an ability to withstand high short-circuit current [36]. IGCTs have the features of both IGBTs (high voltage and current ratings) and GTOs (low conduction losses). An SSCB is fast in operation and fully controllable. However, with IGBTs, a significant amount of power is lost during on-state operations, which reduces the overall efficiency of the breaker. Also, the drawback of using a GTO is its low switching speed.

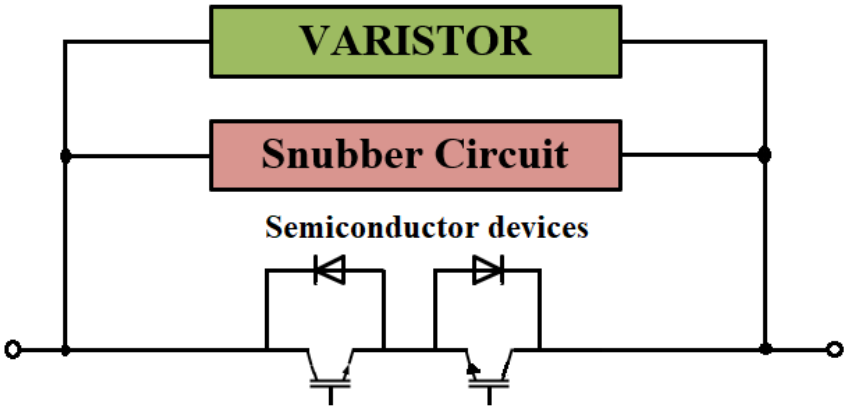


Figure 1.7 Solid-state circuit breaker

1.5.3.3 Hybrid Circuit Breakers

A hybrid DCCB is composed of an ultrafast disconnector (UFD), the main breaker comprising hundreds of IGBTs, a load commutation switch (LCS), and surge arresters [37]. It is a combination of arc-based circuit breaker (ACB) and power electronic circuit breaker (PECB) in parallel. Several configurations of hybrid DCCBs have been proposed that operate in medium and high voltage DC systems to break the direct current faster with more efficiency [38-40]. During normal operation, current flows through the LCS and the UFD. It combines the feature of the high efficiency of a mechanical breaker and the fast turn-off speed of the power electronic circuit

breakers. Since the LCS consists of a few IGBTs, the losses in a hybrid DCCB are small. When a fault occurs, the commutating switch turns off, thereby directing the fault current through the main breaker. The voltage rating of LCS must be higher than the on-state voltage of the main breaker [37]. The rate at which the fault current flows through the main breaker keeps rising continuously at a very high rate. Thus, a current limiting reactor is used to lower this rise in the DC fault current. The arc drawn across the contacts of the mechanical switch is removed by opening the switch under no-current condition. During this period, the main breaker turns off, and the flow of fault current is ceased, thereby clearing the system's fault. The power levels achieved by a hybrid DCCB is relatively high compared to the other breakers as its on-state power loss through the commutating switch is minimal. Also, its efficiency is similar to ACBs. However, they have an increased response time and are more expensive compared to the PECBs. Thus, managing fault currents in the semiconductor switch using a hybrid DCCB is difficult. Also, there are complexities involved in controlling the current commutation in hybrid configurations.

1.6 Problem Statement

The preliminary dissertation focuses on the challenges associated with the protection of DC systems and presents a solution to overcome those problems. The on-state power loss is an important factor that requires careful attention to design any solid-state DC circuit breaker topology. Thus, the most efficient breaker topology is identified and analyzed for various short-circuit faults in theory, analytical review, computer simulation, and finally, in test prototype experimentation. A new method for detecting DC circuit breaker parameters is detailed, which overcomes the problems of the already existing methods. The breaker is tested for a short-circuit case under both low-impedance and high-impedance cases. The study shows a further specification

is needed to the breaker parameters that enable the breaker to freely detect and interrupt both low and high impedance faults occurring in the network. Finally, the practical application of the selected breaker is studied by implementing it in the DC transmission/distribution lines.

1.7 Dissertation Outline

The dissertation is organized as follows: In Chapter 2, an overview of the existing Z-source circuit breaker (ZCB) topologies are presented. These breakers are studied and analyzed, considering the power loss and efficiency aspects. The best breaker topology in terms of efficiency is selected for further investigation. Chapter 3 proposes a new method using the relation of thyristor tripping time to detect the parameter of a ZCB topology. Furthermore, after the parameter detection, the breaker is designed for laboratory experiments, which is then tested for different short-circuit current. In Chapter 4, a new method specifying the parameters of the ZCB topology is proposed to successfully operate a ZCB when a high impedance fault is encountered in the DC systems. This chapter also derives a relation between the minimum fault resistance and the maximum Z-source capacitance required in order to trip the breaker for interrupting the high impedance faults. Chapter 5 covers the practical application of a ZCB when implemented in a DC transmission/distribution line. The effective cable length limit for the protection of DC power networks using a ZCB is assessed, and the relation between maximum cable length and load power requirements is established. Finally, Chapter 6 draws the overall conclusion of this dissertation report. The results in Chapter 2 have been reported in the conference proceedings in reference [41]. Likewise, the findings in Chapter 3 are published in [42, 43]. The outcomes of Chapter 4 are reported in the journal [44] and the conference proceedings in reference [45] and finally, the results of Chapter 5 are published in [46].

CHAPTER 2

Z-SOURCE CIRCUIT BREAKER: A REVIEW OF EXISTING TOPOLOGIES

2.1 Z-source Circuit Breaker

To overcome the problems associated with various DCCBs and facilitate the coordination of cascaded breakers, a resonant style DC circuit breaker named the Z-source breaker (ZCB) is proposed. A ZCB, as seen in Fig. 2.1 is a thyristor (SCR) based DC circuit breaker which uses a Z-source impedance network that automatically interrupts the load-carrying currents at an extremely high speed [47]. An improved version of the first proposed topology of the ZCB, which has a capability to handle load change conditions and limitations of the capacitor current, is introduced in [48]. Due to the feature of automatic fault isolation with zero detection delay, the ZCB is very favorable for short-circuit protection. It operates based on the interaction between LC elements and the SCR in a resonant circuit. A fraction of the transient fault current is supplied through the Z-source capacitors in an event of a fault that forces a current zero-crossing in the SCR. The fault current path does not incorporate the source and the SCR.

The concept of a Z-source circuit was initially proposed by F.Z Peng in [49], introducing a Z-source inverter that could interface to a voltage or a current source and utilize the short-circuit state to achieve a voltage boost. The LC connection in a Z-source circuit could operate in both boost and buck mode. This concept of "Z-source" was later adopted into ZCB for the protection of the DC network. Based on the application, a ZCB is classified into two categories: unidirectional ZCB (UZCB) and bidirectional ZCB (BZCB). As per the title, a UZCB can interrupt fault current in only one direction (*i.e.*, fault introduced at the output of the ZCB), whereas a BZCB can interrupt power exchanges between DC microgrids in both directions (*i.e.*, either at the input or output terminal of

the ZCB). The BZCB is advantageous compared to the UZCB in applications such as DC microgrids as they realize the bi-directional flow of energy.

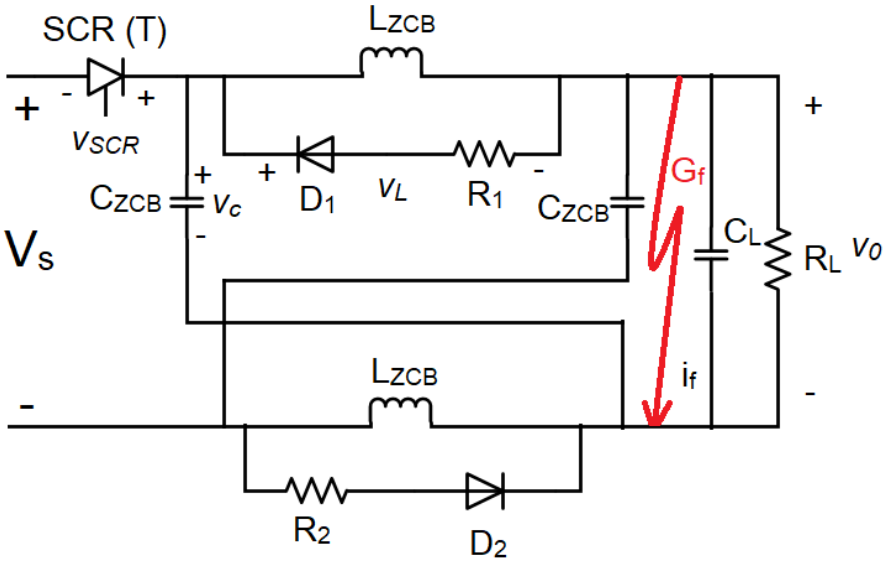


Figure 2.1 Classical Z-source circuit breaker

A ZCB is a unique form of solid-state circuit breaker that typically consists of inductors, SCR/diodes, and auxiliary capacitors to realize the SCR's commutation. SCRs with an ability to handle high voltage/large current are robust and inexpensive, which justifies its application in a ZCB circuit. During fault conditions, the inductor current cannot change instantaneously. Thus, the high-frequency fault current passes through the Z-source capacitors and the SCR. This eventually drops the SCR current to zero and turns it off. After the SCR commutates off, the LC branches create a resonance circuit that dissipates the remaining energy from the ZCB circuit, which is a common principle that every ZCB topologies follow. The natural commutation of a Z-source configuration clears the fault in the system. Once the fault is cleared, control signals can be used to disable sending the gate pulses to the SCR. The control circuit is simplified, only to detect the level

of the SCR current and its operating state, *i.e.*, whether the SCR has commutated off or the SCR current has fallen off to a particular value. The combination of a Z-source breaker and the power electronic converters can be used to handle the fault in a DC converter system. A notable feature of ZCB is its cascaded breaker coordination. In an instance of fault occurrence, only the breaker closest to the fault switches OFF, allowing the rest of the system to operate normally. The path followed by the fault current in the event of fault forms a Z-shaped structure, as seen in Fig. 2.2, where the fault current is supplied by the Z-source capacitor (C_{ZCB}).

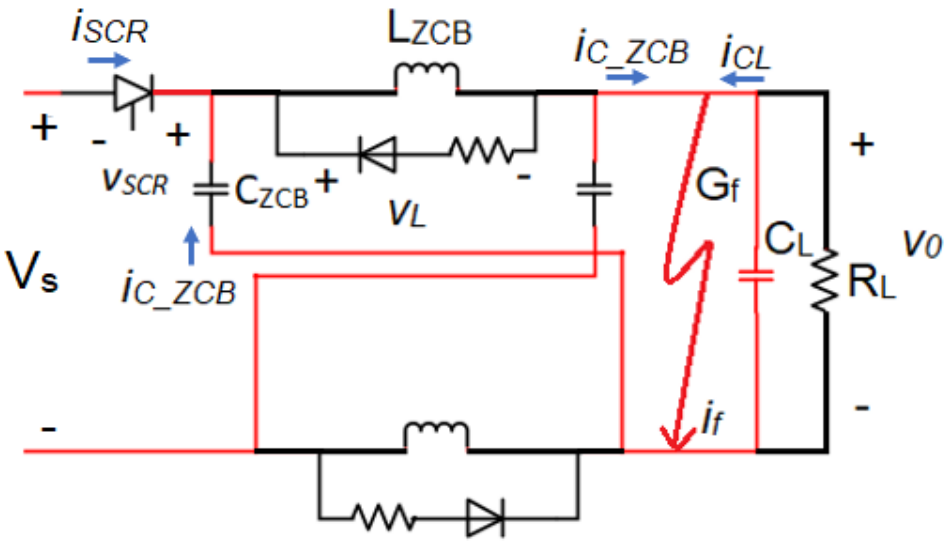


Figure 2.2 Conduction path of transient fault current

2.2 Application of SCRs in ZCB Circuit

Thyristors are the power semiconductor devices that are extensively used in power electronic circuits due to their higher efficiency and robust nature [50-52]. They can be implemented in an advanced gate driver module with input-output isolation and gate drive circuits, microprocessor control, protection, diagnostic circuits, and a controlled power supply. Initially, a

gate signal is required to turn the SCR on, which can be removed once it turns on and achieves a steady-state operation [3, 47, 49]. The gate trigger circuit for an SCR can be realized by simple R or RC networks. A positive voltage applied between the gate, and the cathode of the SCR increases its anode current, which eventually turns on the SCR. Conversely, to turn off the SCR, its forward current is reduced to a value lower than the holding current for a sufficiently long time such that enough reverse recovery charges are accumulated during the commutation. An SCR is bi-stable in operation, *i.e.*, it operates from nonconducting to conducting state and vice versa. Fig. 2.3 shows the driver circuit of an SCR with a 5-VDC power supply that provides driving current to its gate to turn it on. The value of resistors (R_1 & R_2) in Fig. 2.3 are selected such that the maximum gate current does not exceed the threshold current value, which is 15 mA for the SCR used for our laboratory experiments. The value of resistors is calculated as: R_1 = 1100 Ω and R_2 = 430 Ω, respectively. Once the SCR turns on, the gate signal can be removed. Thus, gate drivers are only used for turning on the SCR during the operation of a ZCB, whereas it is turned off *via* the post fault commutation in the Z-source circuit.

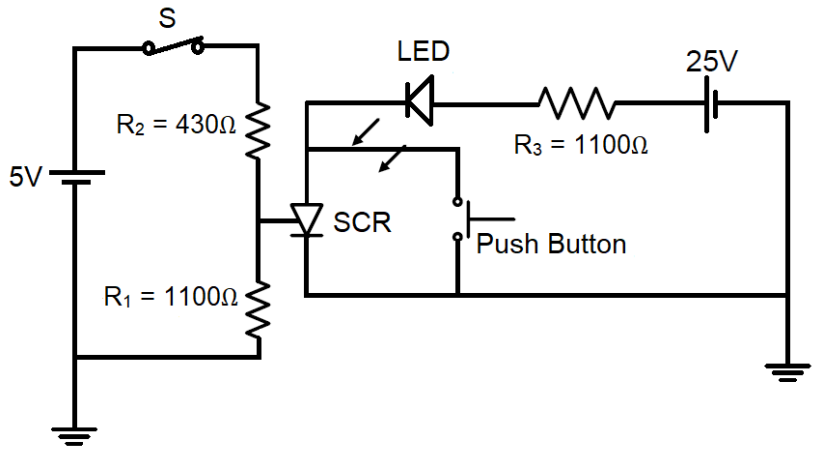


Figure 2.3 Driver circuit for thyristor (SCR)

2.3 Existing Topologies of ZCB

In this section, some of the existing topologies of ZCB are studied. Several ZCB topologies (cross and parallel), including the UZCB and BZCB, have been proposed and discussed in [47, 53, 54]. The main limitation of a UZCB is its unidirectional power flow, which is not suitable for a microgrid system that depends on the power flow in both directions. Thus, the initially introduced topology of UZCB is modified to obtain the BZCB topology. The number of components associated with a BZCB topology is twice as many as the UZCB. For example, a UZCB topology can operate with a single semiconductor device during normal operation, whereas at least two semiconductor devices are required by any BZCB topology. Modifications to an existing ZCB topology to allow step load changes were performed in [48] and [55]. The ZCB circuits are simplified and analyzed during steady-state operation, which helps in the power loss assessment. A study of three different existing BZCB topologies is performed. These topologies vary in LC configuration, however, follow the same operating principle.

2.3.1 Uncontrolled-Rectifier-Based Bi-directional ZCB

The topology of uncontrolled-rectifier-based bi-directional ZCB (URB-BZCB) introduced in [56] has only one SCR and two inductors in the middle of a rectifier bridge, as shown in Fig 2.4. The diode rectifier's full-bridge structure enables the ZCB to interrupt fault current in both directions, thus making the topology bidirectional. The circuit breaker responds to the fault on both input and output terminals. The main feature of a URB-BZCB topology is its ability to maintain the advantages of other series UZCB topologies yet, allowing a bi-directional current flow. The parameters of the URB-BZCB are determined using the minimum detectable fault ramp rate (F_{rr}), the minimum fault conductance, step load change, and maximum allowable load current slew rate [56]. In the event of fault occurrence, like every other ZCB topology, the fault current flows through

the Z-source capacitors (C_1 and C_2) as the current in Z-source inductors (L_1 and L_2) cannot change instantaneously.

The ZCB parameters responsible for the steady-state current flow during normal operation of the circuit consists of line inductance (L_L), diodes (D_1 and D_4), Z-source inductors (L_1 and L_2), SCR (T_1), and Z-source capacitors (C_1 and C_2), respectively. The diodes D_1 and D_4 are conducting the steady-state current, whereas D_2 and D_3 are in the reverse-blocking state. Therefore, the path that the current flows can be either "$L_L - D_1 - L_1 - T_1 - L_2 - D_4 -$ *load*," or "$L_L - D_1 - L_1 - T_1 - C_2$ – *load*", or "$L_L - D_1 - L_1 - C_1 - D_4 -$ *load*," depending on current-flow direction. Fig. 2.5 shows the equivalent circuit of current flow from the ideal DC voltage source (Vs) to the RC load. The inductors L_L, L_1, and L_2 carry load current. This equivalent circuit is used to analyze the power loss of URB-BZCB during normal operation. Since the breaker follows the convention of a BZCB, it would operate in the same manner even if the load and source connections are swapped.

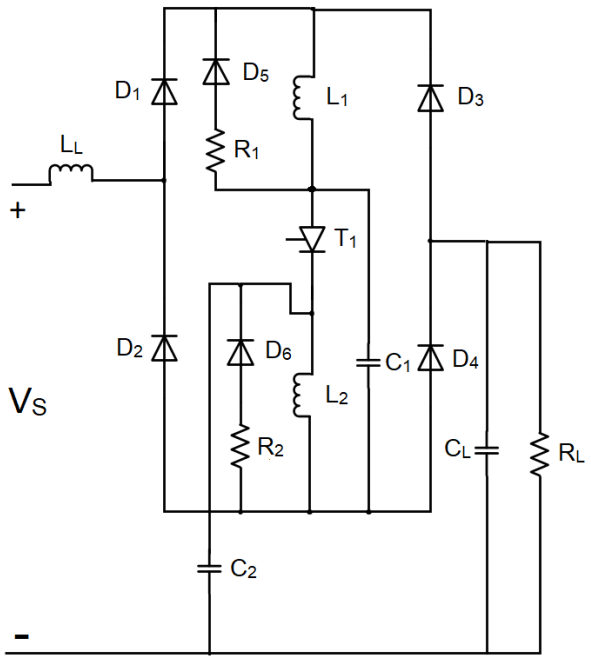


Figure 2.4 Topology of uncontrolled-rectifier-based bi-directional ZCB (URB-BZCB)

For the steady-state power loss analysis, the power loss across the ZCB components (L_L, L_1, L_2, D_1, D_4, T_1, C_1, and C_2), as seen in Fig. 2.5 is evaluated. The ZCB is used to protect an RC load consisting of R_L and C_L. Initially, to turn the circuit breaker from off-state to on-state, a pulse signal is injected into the gate of the SCR (T_1). As the circuit breaker reaches the steady-state, the pulse gating signal can be released to avoid turning off by transients at power on.

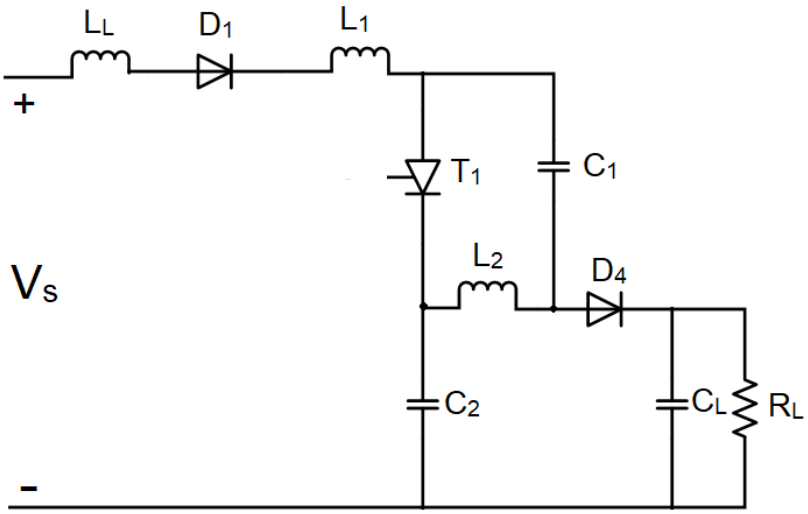


Figure 2.5 Equivalent circuit of URB-BZCB for power loss calculation

2.3.2 Inter-Cross-Connected Bi-directional ZCB

The second ZCB taken into consideration is the inter-cross-connected bi-directional ZCB (ICC-BZCB) from [57], as shown in Fig. 2.6. This is also a bidirectional circuit breaker with an ability to limit and interrupt fault current in both directions. An ICC-ZCB consists of two SCRs, two inductors, three capacitors, and two diodes that follows the same operating principle as other ZCB topologies with the high-frequency currents passing through the auxiliary Z-source capacitors in the event of fault occurrence, which is responsible for the commutation of SCR.

Two pairs of SCR and diode forming a parallel connection are inter-connected with each other. An RC load that consists of R_L and C_L represents a parallel connection of the RC circuit, as seen in Fig. 2.6. A notable feature of this topology is the presence of common ground between the load and the power source. Also, unlike other topologies, the transient fault current drawn from the generation source is minimal in an ICC-BZCB design. It is a multifunction device. Apart from its circuit-breaking feature, an ICC-BZCB can also be used for power flow direction control along with the fault current limiting and interrupting applications.

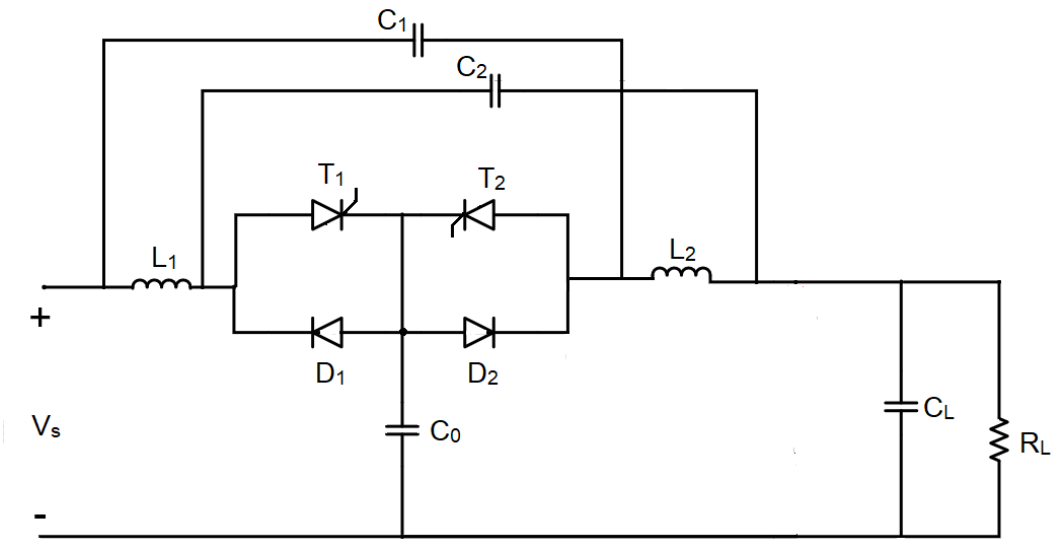


Figure 2.6 Topology of inter-cross-connected bi-directional ZCB (ICC-BZCB)

During normal operating conditions, the SCR (T_2) and the diode (D_1) are reverse biased in the ICC-BZCB. The breaker makes a connection between the DC power source and the load *via* the Z-source parameters L_1, L_2, T_1, D_2, C_1, and C_2. Thus, the power loss across these six ZCB components are considered for overall efficiency evaluation. The voltage across the capacitor C_0

prior to the fault is charged up to the source voltage (V_s). Fig. 2.7 is the equivalent circuit of ICC-BZCB for power loss calculation.

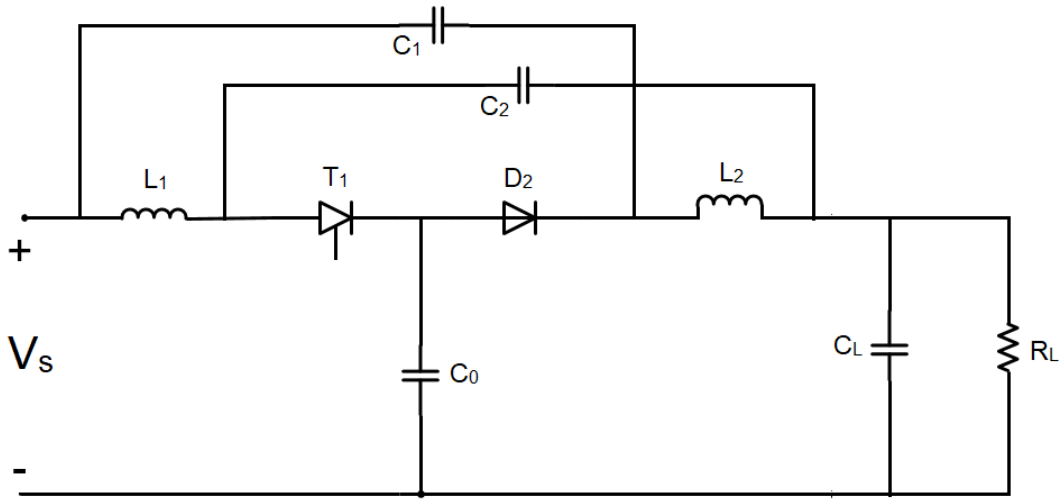


Figure 2.7 Equivalent circuit of ICC-BZCB for power loss calculation

2.3.3 Traditional Series-Connected Bi-directional ZCB

The third candidate is the traditional series-connected bi-directional ZCB (SC-BZCB) from [58], as shown in Fig. 2.8. The topology of SC-BZCB has an antiparallel-connected SCR pair connecting in series with LC resonant circuits, which makes it unique from the other two topologies. Each inductor has a freewheeling diode in parallel. Thus, the number of passive components involved in the traditional SC-BZCB circuit is higher in comparison to the ICC-BZCB and URB-BZCB topologies. Some notable drawbacks of this design are absence of common neutral and low-pass frequency response characteristics. Also, the SC-BZCB is not suitable for the input filtering of power converters and has a high spike in input current due to the reverse recovery of SCRs [56].

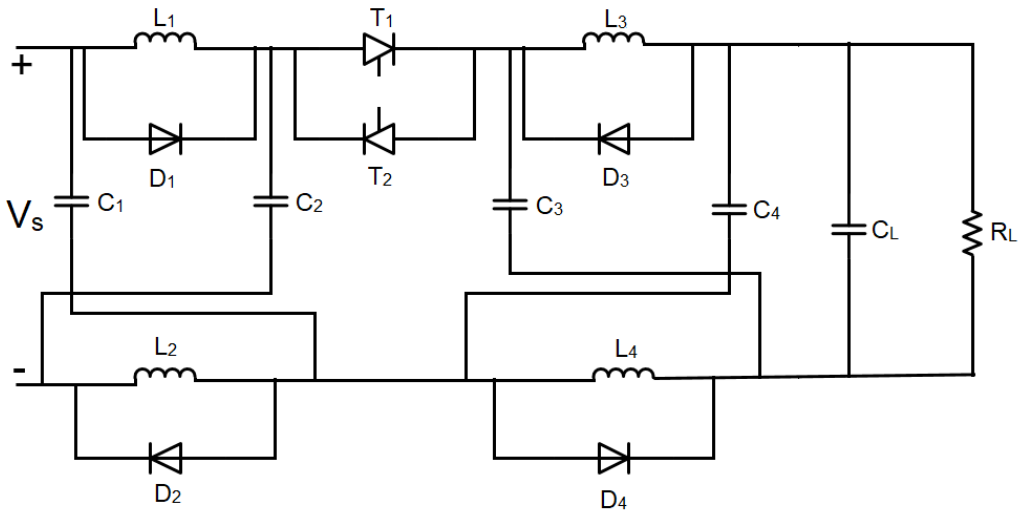


Figure 2.8 Topology of traditional series-connected bi-directional ZCB (SC-BZCB)

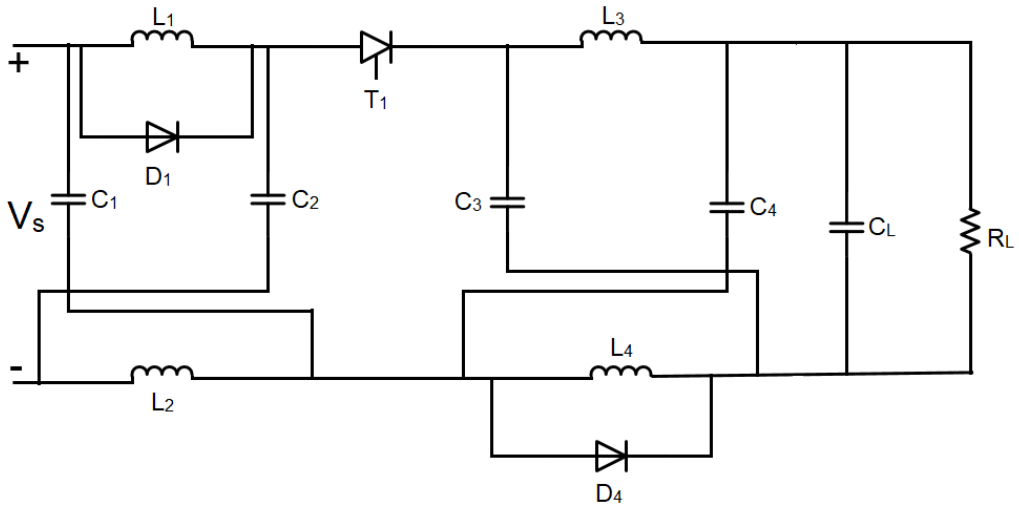


Figure 2.9 Equivalent circuit of SC-BZCB for power loss calculation

During normal operation, depending on the current-flow direction from source to the load, the SCR (T_1) and diodes (D_1 and D_4) operates in conduction mode. In contrast, the SCR (T_2) and diodes (D_2 and D_3) are reversely biased. The current flows through all four inductors (L_1-L_4), capacitors (C_1-C_4), and the SCR (T_1). Thus, there are eleven ZCB components considered for the

efficiency analysis, which includes D_1, D_4, L_1, L_2, L_3, L_4, C_1, C_2, C_3, C_4, and T_1, respectively. Fig. 2.9 is the equivalent circuit of SC-BZCB for power loss calculation.

2.4 Efficiency/Power Loss Analysis

The power loss and efficiency evaluation of the three BZCB topologies presented in Section 2.3 during normal operation is performed. Power loss analysis is a major consideration in breaker selection. Due to the presence of semiconductor devices, the conduction loss associated with them must be considered while designing a ZCB model. Every single power electronic component associated with the ZCB topology that participates in its equivalent circuit for power loss calculation contributes to the overall power loss of ZCB during steady-state normal operation. The maximum efficiency depends on the selection of power components. The power loss equations for inductors, capacitors, diodes, and SCRs are considered for overall efficiency evaluation.

2.4.1 Inductor Loss

The power loss in an inductor includes winding/copper loss and core loss. Core loss depends on the type of core used. Typically, an iron alloy core, a good conductor of electricity, is considered for designing an inductor. Due to short fault time in DC systems, the core loss of the inductor can be ignored. Thus, only the copper loss due to the winding's DC resistance and the RMS current through the inductor is considered for overall power loss calculation, which can be calculated using (1-4). The winding resistance (R_{DC}) can be obtained from the inductor datasheet.

$$P_{loss,inductor} = P_{loss,core} + P_{loss,copper} \tag{1}$$

For the DC supply,

$$P_{loss,core} \approx 0 \tag{2}$$

Thus,

$$P_{loss,inductor} = P_{loss,winding} = {I_{rms}}^2 \cdot R_{DC} \quad (3)$$

$$R_{DC} = \rho \frac{N l_m}{A_w} \quad (4)$$

where,

R_{DC} is the DC resistance of the inductor, in Ω.

N is the number of winding turns.

l_m is the mean length per turn, in cm.

A_w is the area of the wire, in cm^2.

$\rho = 1.762 * 10^{-6} (\Omega - \text{cm})$.

2.4.2 Thyristor (SCR) Loss

The thyristor is a half-controlled, unidirectional power semiconductor device that conducts current only in one direction. It can be controlled only for turning on but not for the turn off process. There are three different kinds of power loss that occurs in a thyristor. These losses are off-state loss, switching loss, and conduction loss. Leakage current in the device results in the off-state loss, which typically is a minimal value and thus can be neglected in this study. The switching loss is transient loss during the turn-on and the reverse recovery processes of the thyristor. The conduction loss depends on the on-state resistance in SCR and the current level during conduction mode. It can also be calculated using the forward voltage drop of the thyristor given in equation (7), determined by its PN junction characteristics. In practice, a thyristor with a low on-state voltage drop should be selected in order to improve efficiency significantly. In general,

$$P_{loss,SCR} = P_{off-state} + P_{switching} + P_{Conduction} \quad (5)$$

For the ZCB application, the switching loss is almost equal to zero. Thus, only the conduction loss of the SCR is considered in this study, which can be calculated using equation (6).

$$P_{loss,SCR} = I^2 \cdot R \quad (6)$$

Also,

$$P_{Loss,SCR} = V_F . I \quad (7)$$

where,

I is the current through SCR, in amps.

R is the on-state resistance of SCR, in ohms.

V_F is the forward voltage drop of SCR, in volts.

2.4.3 Diode Loss

A diode is a power electronic device that allows current to flow through it only in a forward-biased condition, whereas it blocks the current flow when it is reversely biased. The power loss in a diode is determined based on its forward voltage. Thus, to minimize the power loss, diodes with a low forward voltage drop should be considered for practical applications. The forward voltage drop in a diode under similar working conditions is generally lower than that of the thyristor. Hence, the power loss is also low. The energy lost on a power diode is dissipated as heat, considered the power loss. This power loss of diode can be calculated by using equation (8):

$$P_{Diode} = V_F . I_d \quad (8)$$

where,

V_F is the forward voltage across the diode, in volts.

I_d is the current flowing through the diode, in amps.

2.4.4 Capacitor Loss

A capacitor is a device consisting of two conductive metallic plates separated by an insulating dielectric. The dielectric medium between the two plates can be made of glass, ceramic, air, *etc*. The capacitor loss includes the leakage current loss and the equivalent-series-resistance (ESR) loss. ESR of a capacitor is a sum of its in-phase AC resistance, including dielectric

resistance, terminal leads, and plate material at a particular frequency. The ESR loss can be calculated using (9) and (10). The higher the value of ESR, the more is the loss in the capacitor and vice versa. Since we are working with a DC system, the ESR losses are neglected for this study. The only capacitor loss taken into consideration is due to the parallel internal (insulation/leakage) resistance of a capacitor, calculated with (11). The value of this parallel insulation/leakage resistance is extremely high (in Mega Ohms) as obtained from the capacitor's datasheet. Thus, the overall loss in a capacitor is negligible in this study.

$$P_{ESR} = {V_{RMS}}^2 . \omega . C . \tan(\delta) \tag{9}$$

$$\tan(\delta) = \frac{1}{Q} = \frac{ESR}{X_C} \tag{10}$$

where,

V_{RMS} is the voltage across the resonant capacitor, in volts.

Q is the quality factor.

X_C is the reactance of the capacitor, in ohms.

$$P_{IR} = \frac{{V_s}^2}{IR} \tag{11}$$

where,

V_s is the supply voltage, in volts.

IR is the insulation/leakage resistance of the capacitor, in ohms.

2.5 Comparison of the Power Loss and Efficiency Analysis

The power loss and efficiency of the three ZCB topologies presented in Section 2.3 are compared under the same working conditions. The source voltage (V_s = 400 V), load capacitance

(C_L = 500 μF), and the load power (P_L = 16 kW) are all set at the same value for the three case studies. The on-resistance of SCR is set to 0.1 Ω. The specification of ZCB parameters is identified for the total power loss analysis. Each topology's total power loss is the sum of individual losses associated with the ZCB components during the steady-state condition. The voltage drop across the components and the current information is used for the overall power loss evaluation. It can be calculated using equation (12).

$$P_{loss\_total} = \sum (P_{loss,inductor} + P_{loss,diode} + P_{loss,SCR} + P_{IR}) \tag{12}$$

The parameter identification method using the minimum detectable fault ramp rate and fault conductance, as presented in [56], is used for specifying the values of the components of the URB-BZCB topology as listed in Table 1. In order to maintain uniformity, these parameters are also applicable to the study case of SC-BZCB. The insulation resistance of the capacitor is obtained as: IR ≥ 10000 Ω-F at 20 °C, 500 V-DC, 60 seconds, and the ESR value is selected as 0.4 Ω.

Table 1. ZCB component specification for the topology of URB-BZCB and SC-BZCB

Parameter	**Value**	**Remarks**
$C_1 = C_2 = C_{ZCB}$	33 μF	Z-source capacitors
$L_1 = L_2 = L_{ZCB}$	1 mH	Z-source inductors
L_L	5 mH	Line inductance
V_F	1.1 V	Diode forward voltage
IR	303 MΩ	Leakage/Insulation resistance
ESR	0.4	Equivalent Series Resistance
F	500 Hz	Resonance frequency
V_s	400 V	Source voltage
Load power	16 kW	Overall load

Likewise, the parameter values of an ICC-BZCB are also derived using the relations of minimum detectable fault conductance and the minimum required fault conductance ramp rate as given in [57] and listed in Table 2.

Table 2. Parameters used for the design of an ICC-BZCB topology

Parameter	**Value**	**Remarks**
$C_1 = C_2 = C_0 = C_{ZCB}$	45 µF	Z-source capacitors
$L_1 = L_2 = L_{ZCB}$	1 mH	Z-source inductors
V_F	1.1 V	Diode forward voltage
IR	222 MΩ	Leakage/Insulation resistance
ESR	0.4	Equivalent Series Resistance
F	1000 Hz	Resonance frequency
V_s	400 V	Source voltage
Load power	16 kW	Overall load

Equivalent circuits for the three ZCB topologies given in Fig. 2.5, 2.7, and 2.9 are used for the total power losses calculation under a common load condition. The ZCB parameters used for designing the three topologies are obtained from Tables 1 & 2, respectively. Equation 12 is used for calculating the total power loss. Finally, efficiency is evaluated, as presented in Table 3.

Table 3. Overall power loss and efficiency evaluation

Topology	**Total Power Loss**		**Overall Efficiency (%)**
	in watts	in %	
URB-BZCB	260.588	1.6286	98.3714
ICC-BZCB	211.132	1.32	98.68
SC-BZCB	262.176	1.6386	98.3614

The difference in power loss and the efficiencies in these three topologies is due to the difference in the number of power electronic components present in the ZCB topology for steady-state power loss evaluation. Table 4 shows the number of components associated with the power loss assessment for the three topologies considered.

Table 4. Number of components associated with the ZCB topology for power loss evaluation

Category	**URB-BZCB**	**ICC-BZCB**	**SC-BZCB**
Number of Inductors	3	2	4
Number of Capacitors	2	3	4
Number of Diodes	2	1	2
Number of Thyristors	1	1	1

2.6 Summary

In this chapter, a brief review of three existing bi-directional Z-source circuit breaker topologies that include the topology of URB-BZCB, ICC-BZCB, and SC-BZCB, is performed. The three ZCB models are analyzed concerning the power loss and efficiency aspects. Based on the calculations, with a requirement of energizing the same load, it is found that the ICC-BZCB has the least power loss during the normal steady-state operation. The calculations show that the most significant power loss evaluation parameters are the switching devices, *i.e.,* diode and thyristor. Since the topologies of URB-BZCB and SC-BZCB have two diodes in their circuits compared to the ICC-BZCB topology with one diode, they have slightly higher power loss than the ICC-BZCB during normal operating conditions. This analysis has been later studied in [59-61] which also shows that power loss in their respective proposed ZCB topologies is significantly reduced with the presence of fewer number of semiconductor devices.

CHAPTER 3

PARAMETER IDENTIFICATION OF ZCB TO ENSURE SUCCESSFUL TURNOFF OF SCR IN PRACTICAL APPLICATIONS

3.1 Introduction

Recently, the application of DC power systems has become a leading developer of real-time data management software solutions and smart grid automation for power generators, large energy consumers, and utility industries. This is due to the integration of DC-nature renewable energy sources with the distributed generators. Direct current systems are growing as a primary source of power supply due to the development of several DC renewable energy resources like solar and fuel cells and its application in high-power, low-loss power electronics, and power semiconductor devices in the past decades. Moreover, reduction in copper use, higher controllability, lower cost, and easier interconnections are some notable advantages of DC over AC systems. DC power supply is considered as a substitute electric power carrier for the increasing demand of energy utilization. The demand is ever-raising due to its higher overall efficiency for DC loads, easier integration of renewable and distributed energy sources, and uninterruptible power supply with readily available energy storage elements [62-64]. Applications such as electric ships, wind farms, data centers, microgrids, and smart homes can benefit from using DC electric power.

For further research, the topology of ICC-BZCB is considered as it is found to be the most efficient among the other existing ZCB topologies. Analysis of power losses associated with its individual components at various tripping times (SCR turn-off time) is performed to protect a DC load. The auxiliary Z-source capacitors C_1, and C_2 are used to realize SCRs' commutation [57]. Statistical values of the ZCB parameters (Z-source inductors, Z-source capacitors, load capacitor, load resistor) are evaluated for various tripping times. Hence the overall power loss in the circuit is

determined. An appropriate core selection method for designing a Z-source inductor is proposed by comparing the tripping time and inductive permeability.

3.2 Component Sizing Criteria for ICC-BZCB

The previously proposed method for detecting the ICC-BZCB parameters used the minimum detectable fault ramp rate and the minimum detectable conductance relations [57]. In this study, a new method is introduced for detecting the ZCB parameters using the relation of SCR tripping time [42]. The tripping time of ZCB is the time period between the initial fault occurrence and the SCR regaining its forward blocking capability. In an ICC-BZCB, during normal operating conditions, the thyristor (T_2) and the diode (D_1) are reverse biased. The breaker makes a connection between the load and the power source via thyristor (T_1) and diode (D_2), as seen in Fig. 2.7. The tripping time for the thyristor is set to different values, and the corresponding values of Z-source inductors (L_1 and L_2), Z-source capacitors (C_0, C_1, C_2), load capacitor (C_L) is evaluated. A comparison is made between the overall power loss in the circuit for different sets of Z-source parameter values. The numerical values for ICC-BZCB parameters are calculated using the thyristor current equation, and the minimum detectable fault ramp rate equation derived in [57]. The thyristor current is given as follows:

$$i_{SCR}(t) = I_{load} - \frac{2CV_s k}{2C + 3C_L} t + \frac{kV_s}{2C + 3C_L}\left(\frac{1}{4L} + \frac{3Ck}{2C + 3C_L}\right) t^3 \tag{13}$$

where,

i_{scr} is thyristor current in Amps.

I_{load} is load current in Amps.

C is Z-source capacitance in Farads.

C_L is load capacitance in Farads.

V_s is source voltage in Volts.

k is the minimum detectable fault ramp rate in $\Omega^{-1}.s^{-1}$

L is Z-source inductance in Henry.

t is tripping time of SCR in secs.

The relation for calculating the minimum detectable fault ramp is given in equation (14).

$$k = \frac{1}{R_f} * \frac{1}{t} \tag{14}$$

where,

tripping time (t in secs) is the varying parameter.

The numerical values of the ZCB components for various tripping times are calculated by substituting the value of k obtained from equation (14) in equation (13 & 15) and solving them.

$$k = \frac{81}{32C^2{R_f}^2}(2C + 3C_L) \tag{15}$$

The value of Z-source inductors can be determined using the relation in (16).

$$L \gg \frac{1}{30} C{R_f}^2 \tag{16}$$

Since equation (13) is a third-order equation in tripping time (t), three different sets of values for Z-source parameters are obtained. The value of 't' is varied, and ZCB parameters are evaluated for different cases. Out of the three possible sets of values obtained using (13), one pair consisted of negative values, which is neglected. The remaining two sets of values are considered for overall power loss calculation and ZCB design considerations. The value of Z-source inductor (L) calculated using (16) is amplified by 10 times the actual calculated value in order to prevent

any possible spike in the source current that may arise while tripping the ZCB when a fault is encountered in the system. Also, with a high inductance value, the current flowing through the inductor can be preserved constantly during fault conditions. The inductor value should not have any effects on the thyristor current. Tables 5 and 6 represent two sets of Z-source parameter values for varying tripping times. The tripping times for the ZCB are varied within an interval of (5 μs - 1000 μs), and the corresponding ZCB parameters for the respective tripping times are evaluated.

Table 5. ICC-BZCB parameters (set-1) for various tripping times

Tripping time (t in μs)	**Z-Source Inductance (L_1, L_2 in mH)**	**Z-source Capacitance (C_0, C_1, C_2 in μF)**	**Load Capacitance (C_L in μF)**
5	0.615	1.15	0.63
10	1.23	2.3	1.26
20	2.5	4.6	2.5
100	12.3	23.07	12.6
500	61.5	115.35	63.25
1000	123	230.7	126

Table 6. Second set of Z-source parameters specified for ICC-BZCB

Tripping time (t in μs)	**Z-Source Inductance (L_1, L_2 in mH)**	**Z-source Capacitance (C_0, C_1, C_2 in μF)**	**Load Capacitance (C_L in μF)**
5	0.22	0.42	0.3
10	0.45	0.84	0.61
20	0.9	1.7	1.25
100	4.5	8.4	6.1
500	22.4	42	30.5
1000	45	84	61

3.3 Inductor Design Principle

An inductor is selected based on two key factors: inductance required with DC bias (L) and the DC current (I). For inductor design, magnetic powder cores are selected as they have outstanding magnetic characteristics, including high resistivity, low power losses, and stability under high DC bias conditions. In order to determine the core size and the required number of turns for an inductor design, the LI^2 chart for the magnetic powder cores in [65] is used to locate the permeability of the core. For our design, the SCR tripping time (t) is set as 10 μs, source voltage (V_s) is 240 V, and the load resistance (R_L) is 80 Ω. Using equations (13-16), the Z-source inductor is calculated as 1.23 mH.

$$N = \sqrt{\frac{L10^3}{A_L}} \tag{17}$$

$$H = \frac{NI}{l_e} \tag{18}$$

where,

L is the required inductance, in μH.

A_L is the inductance factor, in nH/T^2.

l_e is the path length, in mm.

The core selected for this inductor design is a toroid with a part number C055076A2 [65]. Using the inductance factor (A_L) obtained from the datasheet of the core, the number of turns required for the inductor design (N) is calculated using (17). Then, the DC bias (H) is evaluated using (18), which is compared with the permeability curve to determine any roll off in the per-unit value of initially determined permeability. The ratio between the surface area of inductor windings (S_{wire}) to total surface area (S_{total}) of the core is considered less than 0.4 to ensure that the inductor does not saturate under normal and fault conditions. Fig. 3.1 shows the inductor designed with (L = 1.23 mH) for the laboratory experiment.

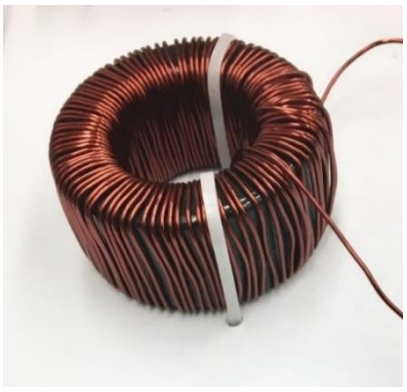


Figure 3.1 Inductor Designed for Lab Test (L = 1.23 mH)

Table 7. Specifications of the inductor designed in lab

Inductor Specifications	**Value**
Inductance (L)	1.23 mH
DC current (I)	3 A
LI^2	11.07 mH-A^2
Material	Magnetic Powder Core
Shape	Toroid
Permeability	60 μ
Inductance factor (A_L)	56 nH/T^2
Outer Diameter (OD)	36.7 mm
Inner Diameter (ID)	21.54 mm
Core Height (HT)	11.35 mm
Path length (l_e)	89 mm
Area of Cross Section	67 mm^2
Number of turns (N)	149
AWG Wire	18
Diameter of Wire	1.024 mm
Area of wire (A)	0.824 mm^2
S_{wire}	122.71 mm^2
S_{total}	364.4 mm^2
Ratio between S_{wire} / S_{total} (R)	0.337 < 0.4

Table 7 above shows the specifications used for the inductor design in the laboratory for making the ZCB circuit. The number of turns required for the inductor was calculated as 149 turns using (17). The loss in an inductor designed using the magnetic powder cores with varying permeability for three different cases of tripping times is studied. The inductance value for each case is calculated using equation (13-16). The inductance value is kept unchanged while varying the permeability of the core. The variation in the permeability value realized using the LI^2 chart changes the core's effective inductance (A_L) accordingly. Any alterations in the A_L value also change the required number of turns (windings) for an inductor design, which directly impacts on the overall power loss evaluation. Table 8 illustrates these details.

Table 8. Inductor loss (winding loss) evaluation for (t = 100, 500, 1000 μs)

Parameter	**Permeability (μ)**	**Inductance (A_L)**	**Inductor winding loss (in watts)**	**Remarks**
t = 100 μs L = 4.5 mH	14	44	10.78	$\boldsymbol{\mu \geq 125}$ (inductor saturates)
	26	82	7.89	
	60	189	5.2	
	125	394	N/A	
t = 500 μs L = 22.4 mH	14	26	15.99	$\boldsymbol{\mu \geq 60}$; (inductor saturates)
	26	48	11.76	
	60	111	N/A	
t = 1000 μs L = 45 mH	14	37	17.2	$\boldsymbol{\mu \geq 26}$; (inductor saturates)
	26	68	N/A	

The winding loss in an inductor is calculated using equation (3 & 4). Using the findings of Table 8, a relation between the available inductor core permeability and the ZCB tripping time is established. It is observed that as the value of tripping time increases, the inductor design cannot account for a higher permeability value as the inductor goes into saturation mode. The permeability versus DC bias curve is a primary parameter to determine the saturation point. Likewise, the relation between the permeability of the core and the number of windings required for the inductor design is also studied, as seen in Fig. 3.2. The relation is inversely proportional, *i.e.*, for an inductor design, as the permeability of the core increases, the number of turns required reduces accordingly. Similarly, keeping the permeability of a material constant, the number of windings required is directly proportional to the SCR tripping times (Fig. 3.3).

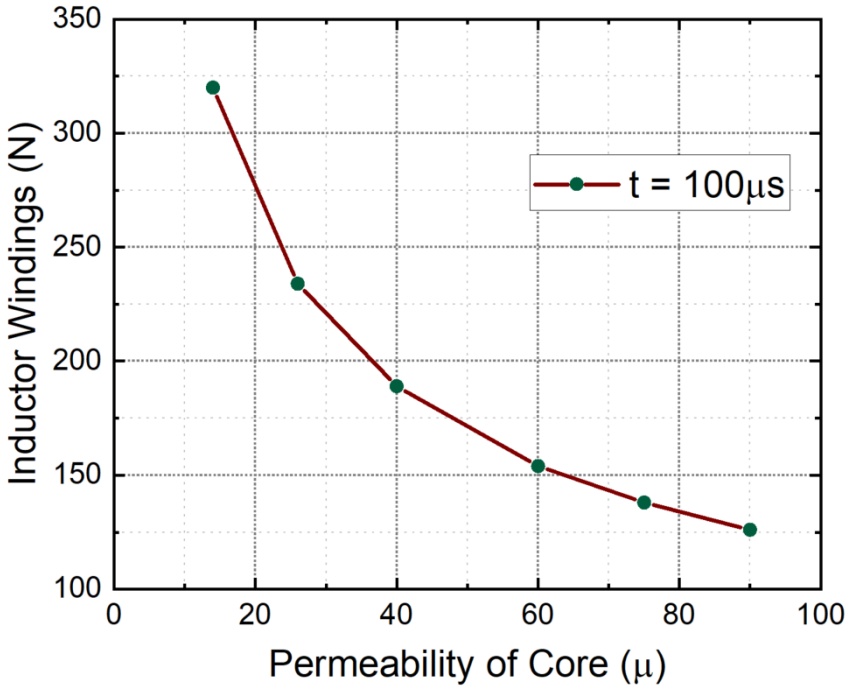


Figure 3.2 Relation between the permeability of the core and the number of inductor windings

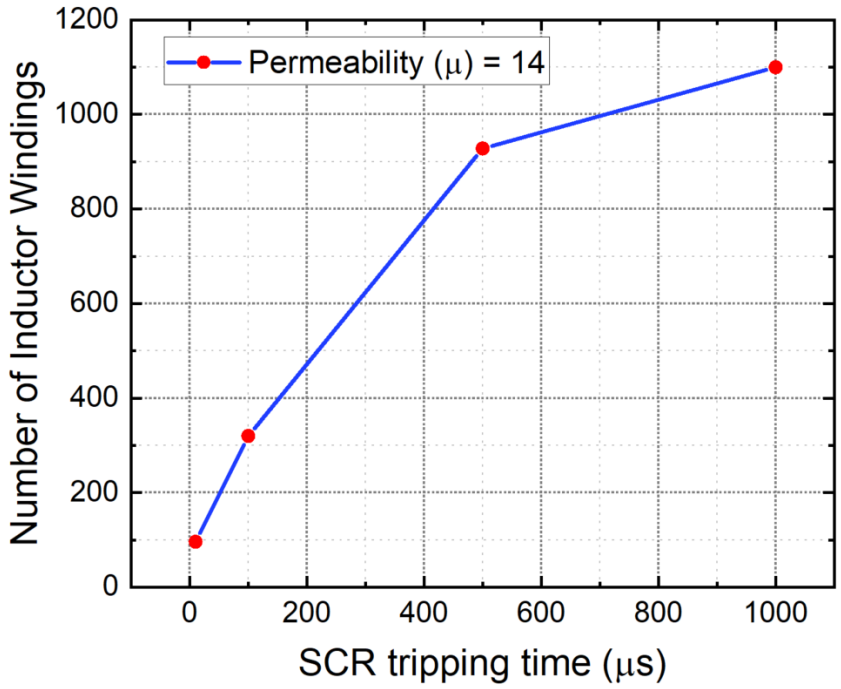


Figure 3.3 Graph showing a relation between SCR tripping time vs. Number of inductor windings

In totality, a general relation is established between inductor windings, tripping time of SCR, and permeability of inductor core. Initially, the inductance value is calculated using the SCR trip time, which is then is used to determine the number of turns required for the inductor design. A relation between the selected inductor core's permeability to the number of inductor windings, SCR tripping time, and inductor loss is established. The key conclusions drawn from this study are:

(a) the higher the value of permeability, the lower the number of turns (inductor windings) required

(b) for a constant permeability, the number of inductor windings is directly proportional to the SCR tripping times

(c) the overall power loss is directly influenced by the core's permeability and the SCR tripping times (Fig. 3.4) [43].

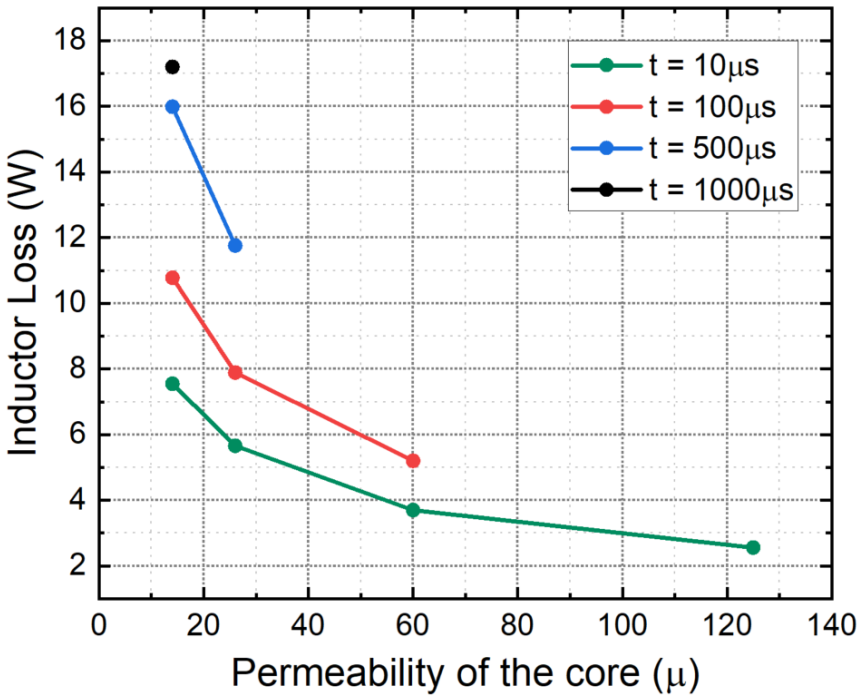


Figure 3.4 Inductor power loss vs. permeability of core at various tripping times
(See Appendix A3 for copyright information)

The increase in the SCR's tripping time limits the selection of the inductor core with different permeability values. As seen in Fig. 3.4, the inductor core selection options for t = 10 μs is wide with different available core permeabilities. However, as t increases, the available core for an inductor design gets limited with the permeability. Thus, when t = 1000 μs, only one option of inductor core is available for the design. Also, the inductor loss is directly related to the SCR tripping time, *i.e.*, for a constant permeability of a core, the inductor loss is higher for a higher tripping time and vice versa. This can be observed for the case with μ = 14 in Fig. 3.4.

3.4 Assessment of Steady-State Power Loss of ICC-BZCB at Various Tripping Times

The overall power loss in an ICC-BZCB during the steady-state normal operation is the sum of individual loss associated with every single component that participates in its equivalent circuit. The equations and considerations of power losses are presented for inductors, capacitors, diodes, and SCRs in [41]. For the total power loss analysis, the respective specification of ZCB components is identified and evaluated for various tripping times. The total power loss is the sum of individual losses in (12). The load-power requirements are set uniform for all the cases with the source voltage (V_s = 240 V), load current (I_L = 3 A), and fault resistance (R_L = 40 Ω). The on-resistance of SCR is set to 0.1 Ω.

All the components associated with the ICC-BZCB topology are chosen carefully, reducing the overall power loss. The inductor with the best applicable permeability (highest possible) is selected. Table 9 presents the required set of data to evaluate the loss in each ZCB components. The Z-source parameter values for an ICC-BZCB with various tripping times are calculated using equations (13-16). Table 5 specifies the ZCB parameters that are chosen for overall power loss analysis. The total power losses of ICC-BZCB topology under a common load condition for various tripping times are calculated. It can be seen in Table 10 that the SCR tripping time has a direct relationship with the overall power loss. As the value of tripping time increases, overall power loss in the circuit also increases, thus reducing the DC network's overall efficiency. The efficiency of a breaker is maximum when the tripping time is short. From this analysis, it can be concluded that the tripping time of ZCB is a primary factor that needs to be considered while designing a Z-source breaker.

Table 9. Specification of required set of data for component power loss calculation

Parameter	Value	Remarks
ID	Varies	Internal diameter of magnetic powdered core (inductor)
OD	Varies	External diameter of magnetic powdered core (inductor)
A_L	Based on permeability	Inductance of core (inductor)
V_F	1.1V	Diode forward voltage
IR	300 MΩ	Leakage/Insulation Resistance of capacitor
ESR	0.4	Equivalent Series Resistance of capacitor
V_s	240 V	Source Voltage
I_L	3A	Load Current
F	Variable	Resonance Frequency
P_L	720W	Load Power

Table 10. ICC-BZCB parameters for overall power loss calculation using values from Table 8

Input Parameters		**Overall Power Loss**		**Overall Efficiency (%)**
Tripping time (t in μs)	Inductor Permeability (μ)	in watts	in %	
10	125	9.314	1.29	98.71
20	60	12.46	1.73	98.27
100	60	14.6	2.03	97.97
500	26	27.74	3.85	96.15
1000	14	38.60	5.36	94.64

3.5 Experimental Validation

3.5.1 Steady-state Power Loss Assessment

A testbed is devised in the lab, as shown in Fig. 3.5. The Z-source capacitors, SCR, and diodes are selected such that it meets the load current requirements of our testbed designed using

the parameters specified in Table 11. The datasheet of SCR [66], diodes [67], Z-source capacitors [68], and the load capacitor [69] are used for the selection of the given components such that they are able to handle the desired load current requirements of 3 A. A thermal metallic AC circuit breaker with the 6 A AC 360 V DC ratings [70] along with the 10 A cartridge fuses [71] are placed in series between the main DC power supply and Z-source inductor to provide double-layer protection to the DC source. The "Fault Emulation Board" represents a parallel combination of six 240 Ω resistors offering a 40 Ω fault resistance.

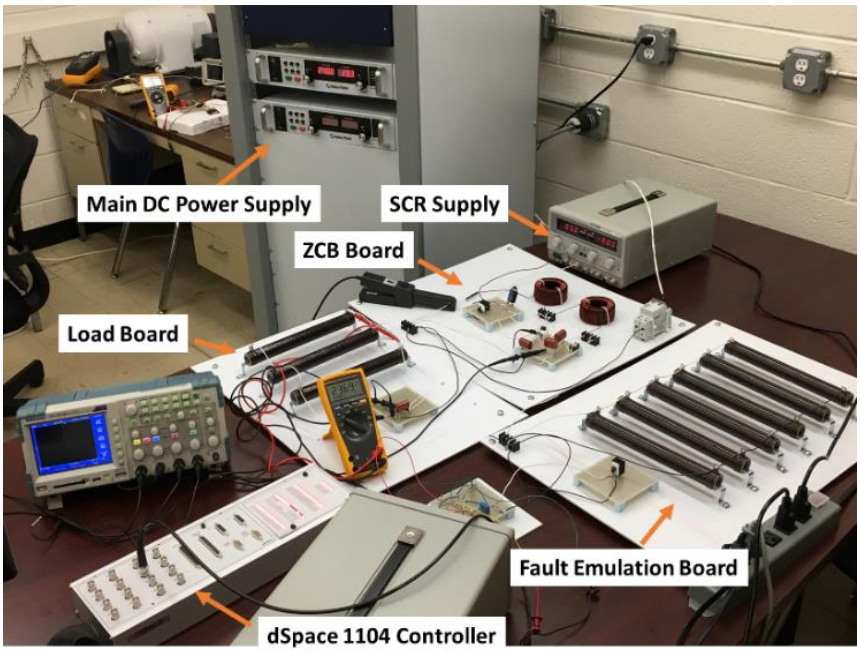


Figure 3.5 Testbed of ICC-BZCB designed in lab

During the experiment, a fault is emulated by sending a control signal to the IGBT [72] on the fault emulation board through the dSpace controller. The gate driver circuit of the IGBT is energized with a 12-VDC voltage supply. Once the IGBT turns on, the additional resistive branches on board are brought into operation, and then the LC resonant branch of ZCB is triggered

to turn off the SCR. A detailed observation is made on the voltage across all components of ZCB for variable supply, as seen in Fig. 3.6. The source voltage is chosen, ranging between 40 V – 240 V with an increment of 40 V in each interval.

Table 11. Laboratory testbed design parameters for ICC-BZCB

Testbed design parameters	**Value**
Desired tripping time (t)	10 μs
Source voltage (V_s)	240 V
Load current (I_L)	3 A
Load power (P_L)	720 W
Z-source inductance (L_1, L_2)	1.23 mH
Z-source capacitance (C_0, C_1, C_2)	2.2 μF
Load capacitance (C_L)	1.26 μF

The Z-source inductors are designed and manufactured using the method illustrated in Section 3.3. The core is carefully selected which meets the desired inductance requirement of DC bias and the DC current. The SCR is initially turned on with a 5 V supply that is connected to its gate terminal. Once the SCR turns on, the gate signal can be removed as the SCR is now fully equipped to operate in a steady-state condition. Now, the ICC-BZCB is fully equipped to be supplied with the DC source. From the calculations, a safe voltage limit for this particular ICC-BZCB design is up to 240 V. Thus, the source voltage was varied such that the maximum voltage limit is within the safety threshold limit. The voltage drop across each ZCB component (Z-source capacitors, inductors, power diodes, and SCR) is measured during the steady-state operation with the help of a multimeter as represented in Fig. 3.6. These results can be used to assess the power

loss distribution of components in ICC-BZCB when there is a rated load with a configured tripping time of 10 µs.

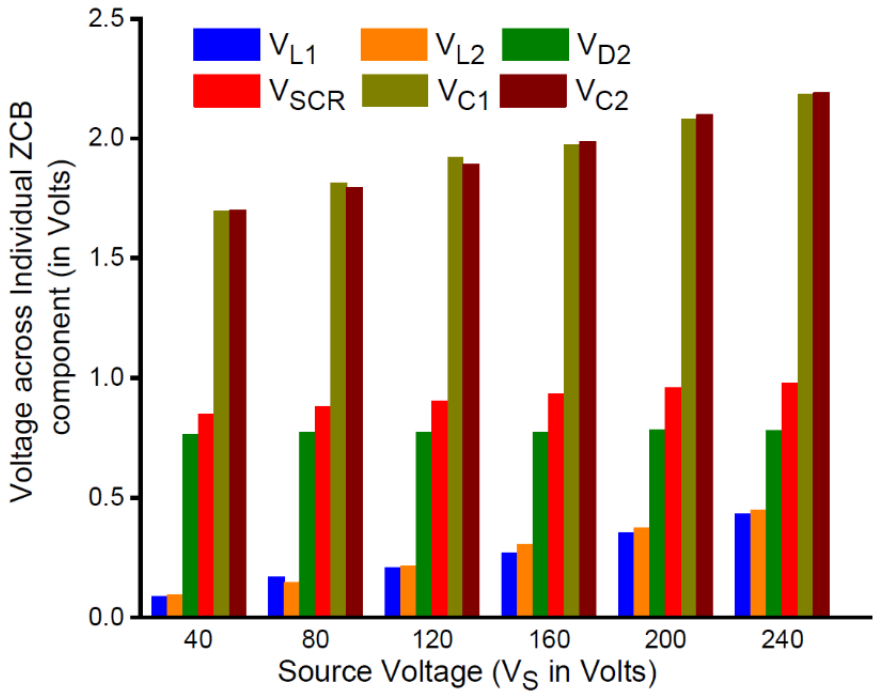


Figure 3.6 Voltage distribution of ICC-BZCB for efficiency evaluation

Table 12. Efficiency evaluation for variable (V_s) during steady-state rated-load (R_L = 80 Ω)

V_S (V)	**I_S (A)**	**V_L (V)**	**I_L (A)**	**Efficiency (%)**
40	0.45	37.91	0.455	95.828
80	0.92	77.72	0.932	98.417
120	1.40	117.41	1.410	98.541
160	1.88	157.70	1.890	99.087
200	2.36	197.66	2.367	99.123
240	2.84	238.04	2.847	99.426

A steady-state power loss analysis is performed (as seen in Table 12) to calculate overall efficiency during the rated-load (R_L = 80 Ω) operation. The source voltage is varied at an interval of 40 V. The corresponding power loss associated with the ICC-BZCB topology is calculated to make an appropriate overall efficiency assessment. It is observed that the ICC-BZCB is most efficient when operated at the voltage level that is initially used for determining the breaker parameters. As the source voltage reduces, the breaker's efficiency reduces accordingly, as seen in Table 12.

Table 13. Steady-state power loss analysis of ICC-BZCB

Test Conditions:	**ZCB Component**	**Power Loss Analysis (in %)**	
		Theoretical	Experimental
Supply Voltage (V_s)= 240 V	L_1	0.13	0.094
Load Resistance (R_L) = 80 Ω	L_2	0.13	0.097
Load Capacitance (C_L) = 1.26 µF	C_1 & C_2	$2.66 \times 10^{-5} \approx 0$ (Negligible)	$1.1 \times 10^{-6} \approx 0$
Inductance (L_1 & L_2) = 1.23 mH	Diode (D_2)	0.042	0.17
Capacitance (C_1, C_2 & C_0) = 2.3µF	SCR (T_1)	0.125	0.213
	Overall Power Loss	0.427	0.574

Now, as the breaker efficiency is recorded maximum at 240 V, the individual loss associated with all the breaker components at V_s = 240 V is identified to detect the parameter contributing the most significant loss. From the observation (as seen in Table 13), it can be concluded that the experimental power loss associated with the Z-source inductors and capacitors is very minimal, and most of the loss in the breaker is noted at the switching devices, *i.e.*, diode

and the SCR. The practical efficiency calculated using the input/output load power in Table 12 matches the efficiency evaluation using the individual loss in the ZCB components in Table 13.

3.5.2 Fault Analysis

After performing the steady-state efficiency analysis, the next step was to inject a fault into the ICC-BZCB design via the fault emulation branch (consisting of 40 Ω fault resistance in series with an IGBT). As the fault was encountered in the system, the breaker was unable to trip the fault current with the specifications that were used for designing the ZCB. The practical observations did not satisfy the simulation results that led to the fault remaining uncleared. Thus, the flaw in the existing parameter identification method was detected. A new method of configuring Z-source capacitors for ICC-BZCB is proposed considering the SCR's reverse recovery time [42].

A. IGBT Gate Driver Circuit

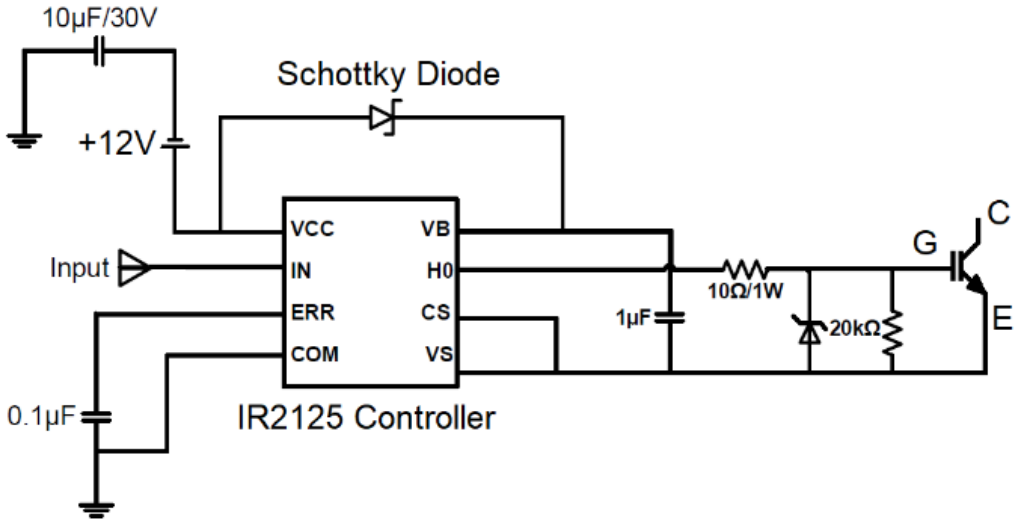


Figure 3.7 Gate driver circuit of IGBT

A fault can be emulated by turning an IGBT "ON" to bring a group of resistors online, which is a branch connected in parallel to R_L. Fig. 3.7 represents the gate driver circuit of an IGBT constructed using an IR2125 controller. A 12-VDC power supply is used to energize the controller, and a step-up signal is injected into the "IN" pin to close the IGBT for the tripping of the ZCB. The step-up signal is conveniently generated in the hardware testbed by using the dSpace-1104 R&D Controller with integrated modules in the MATLAB/Simulink software.

B. Differences in Simulation and Experimental Observations

As stated earlier, *"The tripping time of a ZCB is the time period between the initial fault occurrence and the SCR regaining its forward blocking capability i.e., (0 – t_2) in Fig 3.8."* The existing parameter identification method does not consider the reverse-recovery time (*i.e.*, the turnoff time) of SCR properly and neglects it from the tripping time ($t_{tripping}$). The turnoff time (t_{off}) of the SCR is defined as the time interval between the anode current becoming zero and the SCR regaining a forward blocking capability *i.e.*, $t_1 – t_2$ as seen in Fig 3.8. Thus, the ZCB fails to operate.

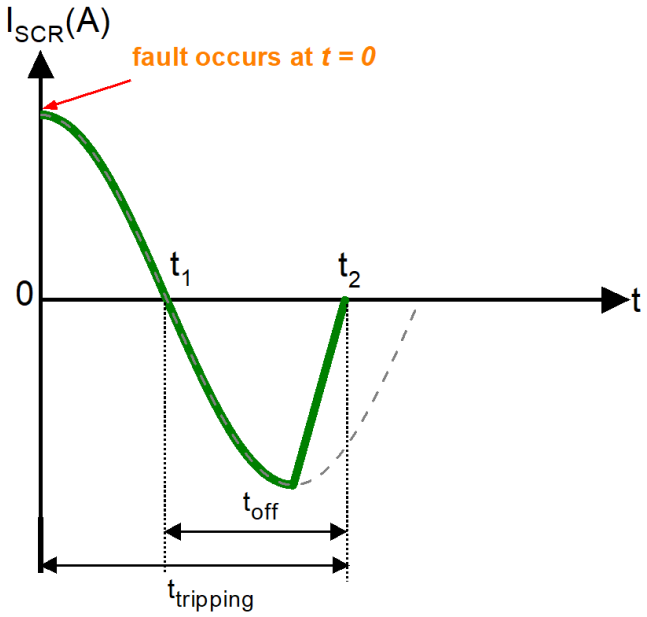


Figure 3.8 SCR current after a fault with consideration of the reverse-recovery time

There are several existing methods for evaluating the ZCB parameters. The ramp rate of fault current and the current magnitude are used to determine ZCB's parameters in [53, 56, 57]; the Z-source parameters are evaluated based on the required resonant time in [3, 47]; and a step-change in fault current is applied to determine the minimum value of Z-source capacitances and inductances in [73], which is extended from the method of [3] and [53]. Each of these methods is based on ZCB topologies theoretically that treats the SCR as an ideal model. For a successful turnoff of the SCR, the turnoff time (t_{off}), which is the period from ($t_1 – t_2$), in Fig. 3.8 should be considered for practical applications.

Table 14. Measured value of components on hardware testbed

Parameter	**Value**	**Remark**
$C_0 = C_1 = C_2$	2.2 μF	V_{Max} = 400 V
$L_1 = L_2$	1.27 mH	Max. DC current = 10 A
C_L	1.3 μF	V_{Max} = 400 V
R_L	80 Ω	Max. DC current = 4.5 A

Thus, an appropriate parameter identification method considering the entire tripping time of the SCR should be considered for designing a ZCB topology. If the parameter values are not specified correctly, then any fault in the system may remain unclear, which poses a significant threat to the DC systems. The neglection of SCR turnoff time in the existing method will result in disastrous consequences in DC circuits if the SCR fails to trip in practical applications. Fig 3.9 shows a comparison between the two SCR current waveforms from simulation and experimental testbed. The configurations for both the simulation and experimental cases are kept uniform with identical parameters of Table 14. The SCR was unable to turnoff for the experimental test due to

the requirement of reverse-recovery even though its current reaches below zero for a small fraction of time after a fault.

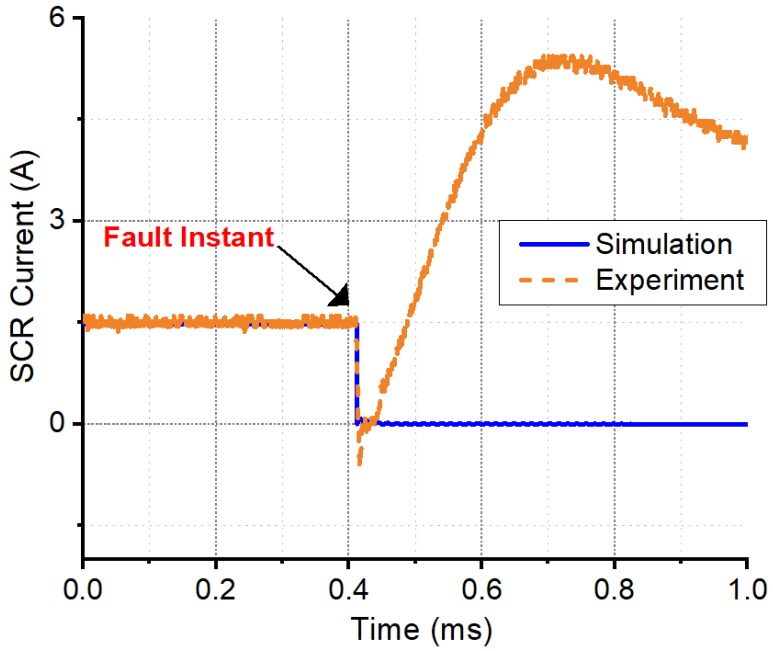


Figure 3.9 SCR current for simulation and practical test

C. Z-source Capacitor Configuration Method

An adequate amount of negative current flowing into the anode of the SCR builds a forward-voltage blocking capability which is a key consideration for achieving a successful reverse-recovery of the SCR. A new method of configuring Z-source capacitances is proposed to supplement the existing parameter identification method and guarantee the turnoff of SCR applied in practice [42]. The new method consists of these two steps:

1) **Identifying ZCB parameters under a boundary condition**: For a successful turnoff of the ZCB, an SCR should have at least two zero-crossing points *i.e.*, t_1 & t_2 as seen in Fig. 3.8. A boundary condition is defined as the instance where the SCR has a single point in time to reach

zero current after a fault is encountered in the system. The SCR current for the case with boundary condition drops below the zero current level for a certain period and then immediately spikes back which causes the fault to remain uncleared in the system as observed from the experimental waveform in Fig. 3.9. A boundary condition differentiates the case of absolute failure from the case of possible failure in SCR's turnoff. The absolute failure in SCR's turnoff refers to the case where the SCR doesn't reach a zero current at all when the ZCB is triggered in an event of a fault. In contrast, a possible failure in SCR's turnoff refers to the case where the SCR current meets the requirement of two zero-crossing points, however, the turnoff of SCR now depends on the negative area that the two points cover. A mathematical relation for the boundary condition is derived in (19) and the calculated Z-source capacitance for this case is used as a base value for C_{ZCB} adjustments in step #2.

$$\begin{cases} i_{SCR}(t_{tripping}) = 0 \\ \dfrac{di_{SCR}(t)}{dt}\Big|_{t=t_{tripping}} = 0 \end{cases} \tag{19}$$

2) **Re-evaluating the ZCB parameters:** The ZCB parameters identified from step #1 were not able to generate sufficient negative current for SCR to internally establish its depletion region. Thus, a correction equation given in (20) is used to further specify the Z-source capacitance. Following the new parameter identification method, a set of Z-source parameters are used as listed in Table 14, when the desired tripping time is set to 10 μs. A correction should be made to these parameters to generate enough negative current and remove excess carriers in the SCR p-n junction internally. The reverse current contribution of the Z-source capacitor for SCR's turnoff increases accordingly by increasing the capacitance value. Therefore, in order to meet the SCR's turnoff requirement, a correction equation is developed to adjust the Z-source

capacitance. Since 'C_0' in an ICC-BZCB topology can contribute to the bidirectional fault protection, it is suggested to adjust C_0 for achieving a successful turnoff of ZCB in the event of a fault occurrence at either terminal (*i.e.*, input or output side). The coefficient of "*a*" is defined in (20) as the ratio of the actual capacitance (as "$C_{o\_adjusted}$"), which is required to turn the SCR off in practical applications, to the boundary capacitance of $C_{o\_boundary}$ (calculated using the relations in 13-16).

$$a = \frac{C_{0\_adjusted}}{C_{0\_boundary}} \tag{20}$$

Considering the accumulation of enough negative electrons to build up the depletion region in an SCR, a correction equation is developed for Z-source capacitance adjustment using Fig. 3.10 [42]. A relationship between the SCR current, the required tripping time ($t_{tripping}$), and the SCR turnoff time (t_{off}) are developed for the boundary condition and the case with adjusted Z-source capacitance. As seen in Fig 3.10, the SCR current curve in red has only one zero-touching point at $t = t_{tripping}$ for the boundary condition. Thus, to turn off the SCR for this case, the SCR current should remain in the negative region for an additional time of t_{off}. According to the SCR's turnoff features, the enclosed area of "Area-A" can provide sufficient negative electron for turning it off. In contrast, to turn off the SCR for a given tripping time, the attenuation in SCR current can be intensified by increasing the Z-source capacitance by the ratio 'a'. This forced turnoff region is the enclosed area of "Area-B" in Fig 3.10.

A correction equation of (21) for the Z-source capacitors is finally derived by using the relation based on "Area-A = Area-B." The ZCB design using the boundary condition from step #1 is adjusted by adding additional capacitance to C (*i.e.*, C_0, C_1, and C_2).

$$\frac{4}{(a^2+a+2)} = \frac{t_{tripping}}{t_{tripping}+t_{off}} \tag{21}$$

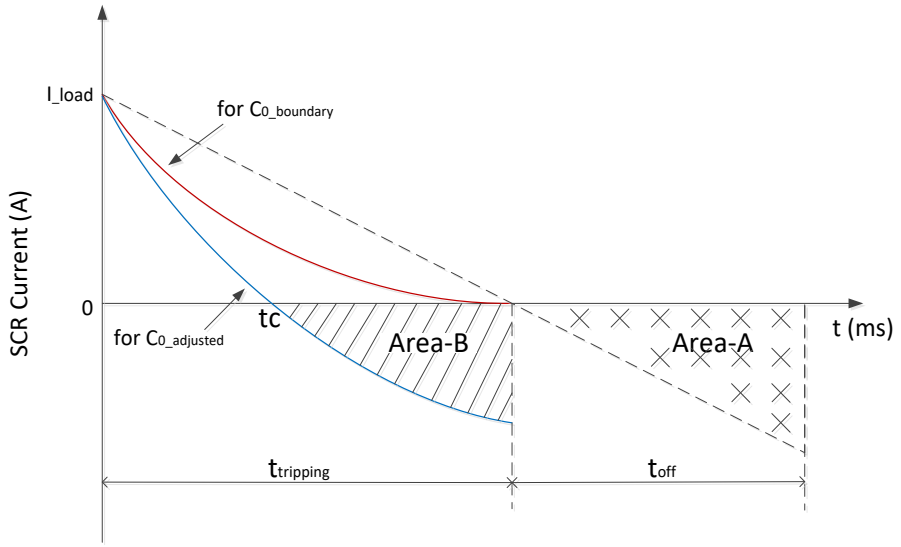


Figure 3.10 Relationship between SCR current, required tripping time ($t_{tripping}$), and the SCR turnoff time (t_{off}).
(See Appendix A4 for copyright information)

D. Test for Validation of Capacitance Correction

The derived correction equation of (21) for capacitance C_0 is justified by this test. The required tripping time ($t_{tripping}$) for the hardware testbed design is 10 μs, and the maximum turnoff time (t_{off}) of the SCR component applied is 45 μs from the manufacturer's datasheet. The threshold of C_0 is calculated as 8.8 μF using equation (21). Therefore, to ensure the turnoff of the SCR, three additional capacitors of 2.2 μF should be added in parallel to the original C_0. Fig. 3.11 shows the anode current in SCR after a fault is triggered. Each film capacitor of capacitance 2.2 μF is added into the C_0 value on the testbed incrementally. In Fig. 3.11, there are five curves representing the SCR current for C_0 = (4.4, 6.6, 8.8, 11.0, 13.2) μF. When C_0 is lower than the threshold of 8.8 μF

calculated using (21), *i.e.*, 4.4 μF and 6.6 μF, the SCR current cannot be interrupted, and thus the DC protection fails. In contrast, the SCR current can be successfully cut off when the C_0 reaches the threshold value or higher, *i.e.*, 8.8 μF, 11.0 μF, and 13.2 μF, to protect the DC circuit. The fault cases' experiments were performed at a lower voltage level of V_s = 120 V, considering the safety constraints of the laboratory DC source which has a maximum supply current limit of 8 A. This resulted in the pre-fault SCR current of 1.5 A and maintained the uncontrolled fault currents under 4.5 A to protect laboratory equipment. The expected fault current was 9 A for the original design with a supply voltage of 240 V. All the other tests are performed under the rated voltage of 240 V. Thus, to successfully trip the breaker, a proper adjustment in the Z-source capacitor (C_0) enables the operation of a ZCB when there is a fault encountered in the system. Hence the test for capacitance correction is validated.

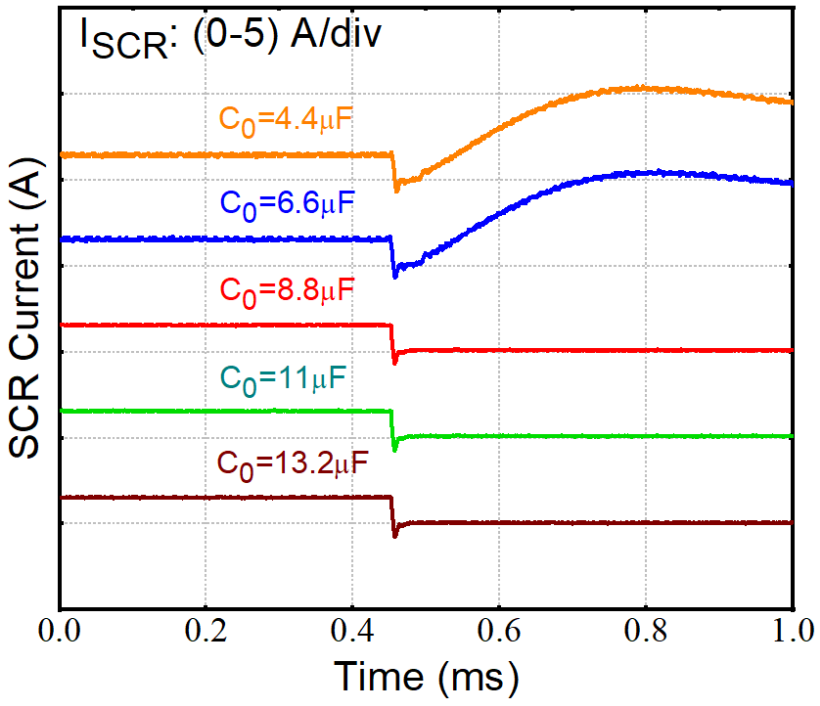


Figure 3.11 SCR current during fault

The post-fault SCR currents (zoomed-in) changing along with the increase of capacitance in C_0 is shown in Fig. 3.12. An increment in the value of C_0 within the unit time increases the accumulated electrons for reverse recovery accordingly, therefore, turning off the ZCB. There are two cases of failed SCR turnoff behaviors as observed in the tests of Fig. 3.11 and Fig. 3.12, respectively. Since the capacitance C_0 = 4.4 μF and 6.6 μF is less than the threshold value of 8.8 μF calculated using the relation in (21), the fault remains uncleared for these values of capacitances. Thus, the general usage of equation 21 is verified using Fig 3.11 and Fig. 3.12. The anode current of the SCR is represented by the curve for C_0 = 8.8 μF in Fig. 3.13 after a fault is triggered. It should be noticed that even after an appropriate adjustment and correction made to the capacitance (C_0) in consideration of the SCR's reverse-recovery time, the fault current through the SCR was cut off within the desired tripping time of 10 μs. Thus, the capacitance adjustment does not alter the turnoff time of the SCR.

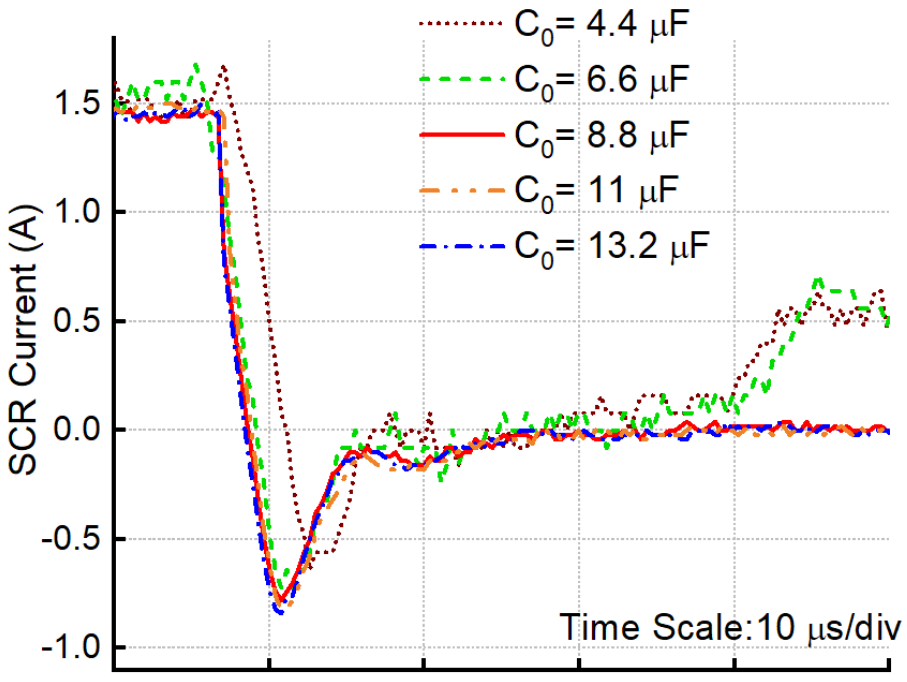


Figure 3.12 SCR current (zoomed-in) during turnoff process

Further, this test was performed on 5 samples of the identical model of SCRs. The same threshold in capacitance correction was demonstrated by the testing results (*i.e.*, all the SCR samples turned off successfully when the C_0 reached a value equal to or higher than 8.8 μF). Also, the reverse was true for all the SCR samples, *i.e.*, the breaker did not turn off for the cases with C_0 = 4.4 μF and 6.6 μF, respectively. The fault current waveforms for the 5 different samples of SCR with C_0 set at 8.8 μF can be observed in Fig. 3.13. The tripping time of these 5 SCR samples noted from the measurement ranges between (10.0 μs, 10.8 μs) which was within the threshold of the tripping time that was chosen initially to determine the ZCB parameters. The uniqueness of each sample causes these minor differences and is in a reasonable range. The effectiveness of the proposed Z-source capacitor configuration is verified by this test which ensures the SCR's turnoff in practical applications.

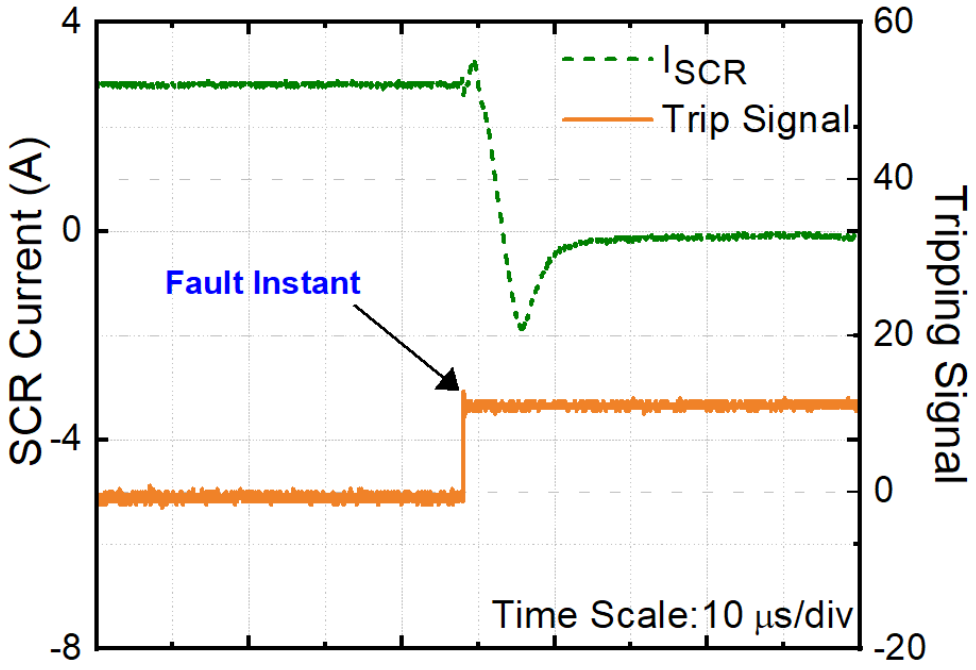


Figure 3.13 SCR current and the trip signal for a configured tripping time of 10 μs (SCR current, in green dashed line; fault tripping signal, in orange solid line)

E. Featured Waveforms During SCR turn off

This section demonstrates the featured waveforms of components on the testbed during the fault current interruption of the ZCB. The Z-source capacitor (C_0) is set to 8.8 μF for this study. A comparison of experiment and simulation waveforms of the SCR's voltage is shown in Fig 3.14. Likewise, Fig. 3.15 and 3.16 represent the current through the SCR (I_{SCR}) and the current from the DC source (I_S), respectively. The measurement data were recorded in an oscilloscope during the hardware experiment and the simulation data was obtained from the MATLAB/Simulink modeling. Both these data were then imported into the OriginLab software to generate Fig. 3.14, 3.15, and 3.16 for comparison. As seen in the three figures, the experiment result matches the simulation analysis well.

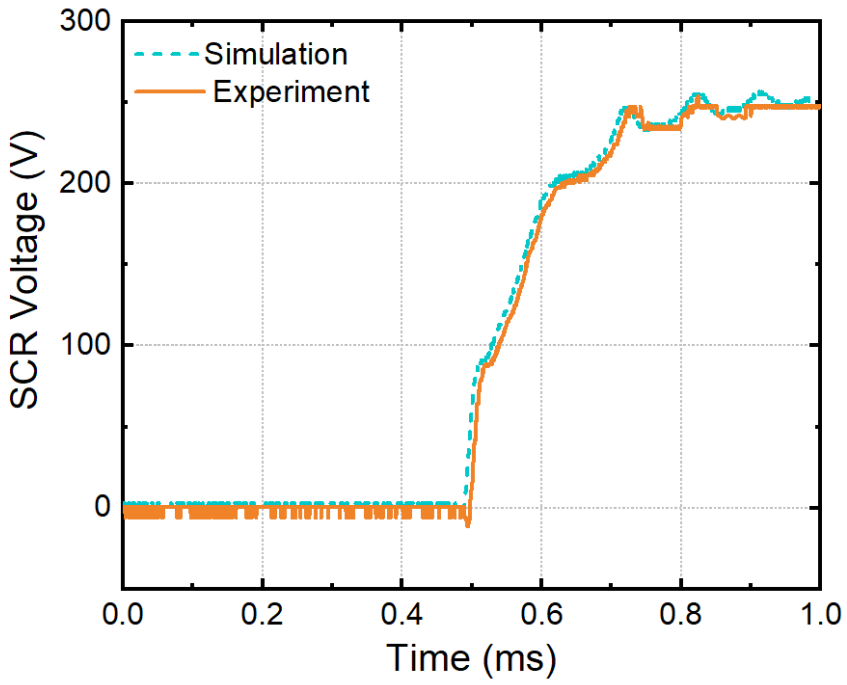


Figure 3.14 Voltage across the SCR (Exp: solid orange line, Sim: dashed blue line)

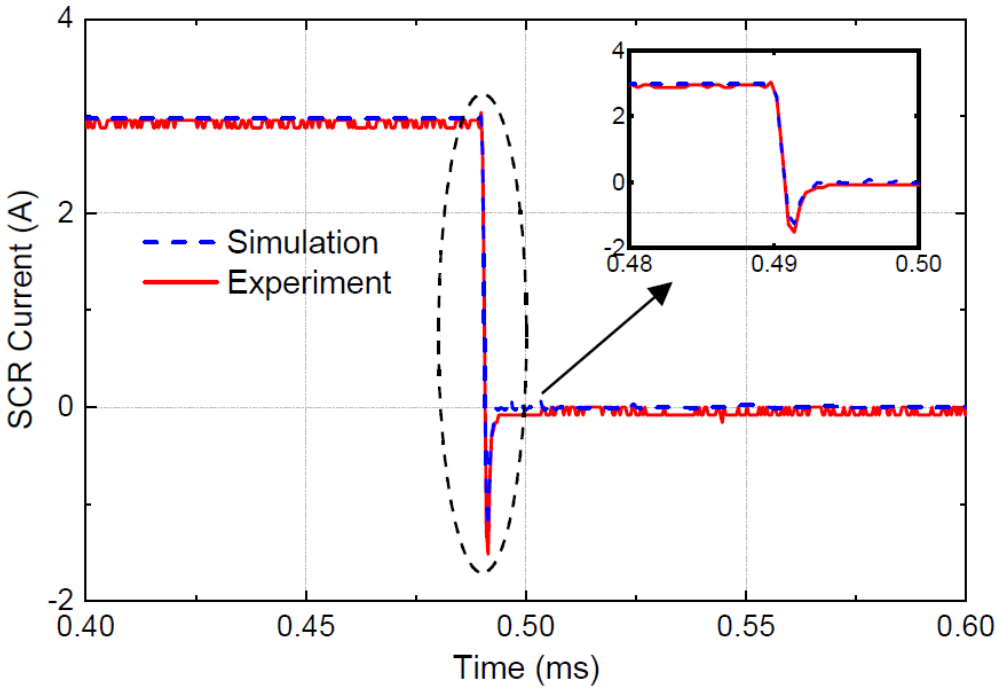


Figure 3.15 Current through the SCR (Exp: solid red line, Sim: dashed blue line)
(See Appendix A4 for copyright information)

As shown in the zoomed-in version of Fig. 3.15, the SCR current was cut off within the desired timeframe of 10 μs. A damped resonant phenomenon was observed for the initial 5 ms from the instance of fault occurrence that reduced the DC source current to zero. During this resonance phenomenon, the source current attains its highest value after the SCR is turned off as shown in Fig. 3.16. The theoretical study of the ZCB topology demonstrates that this peak current will never exceed two times its rated current value and only remains in that peak level for tens of microseconds. The peak current in the source as observed in the simulation and experimental case (Fig. 3.16) when a fault occurs was in the range of 4.5 A, which is less than twice the steady-state current, *i.e.*, 6 A. Thus, it has no influence on the security of switching and other components in the circuit which makes the ICC-BZCB safe & reliable to operate for the protection of DC systems.

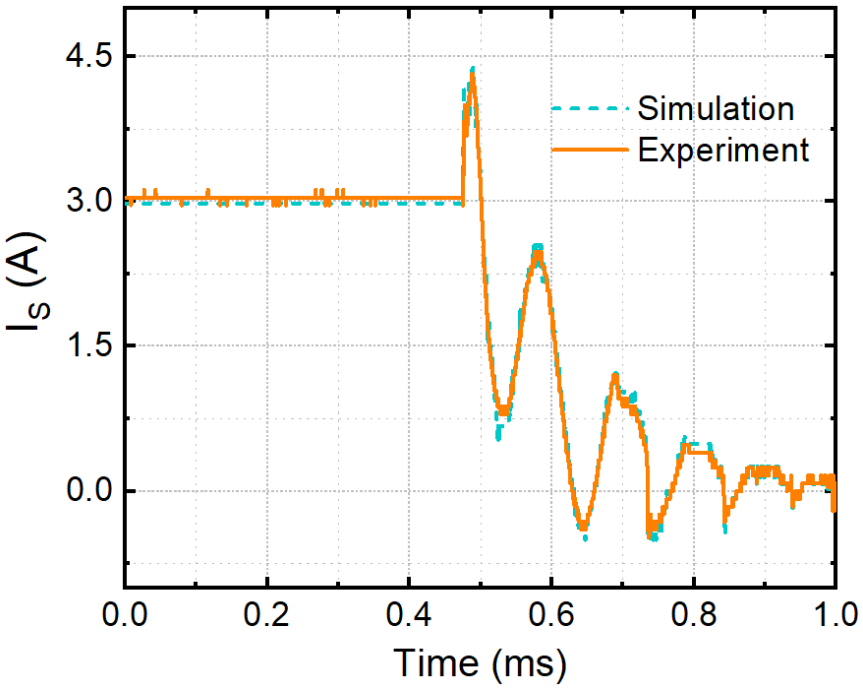
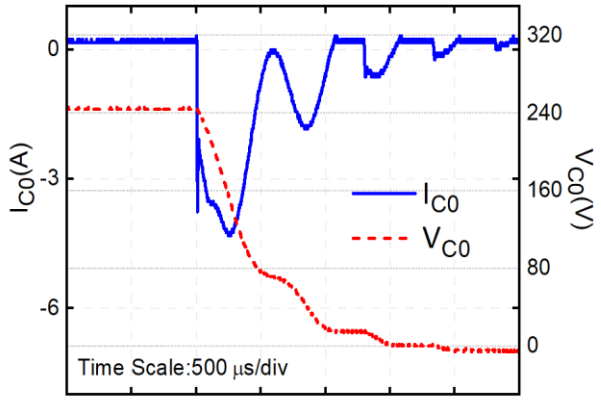
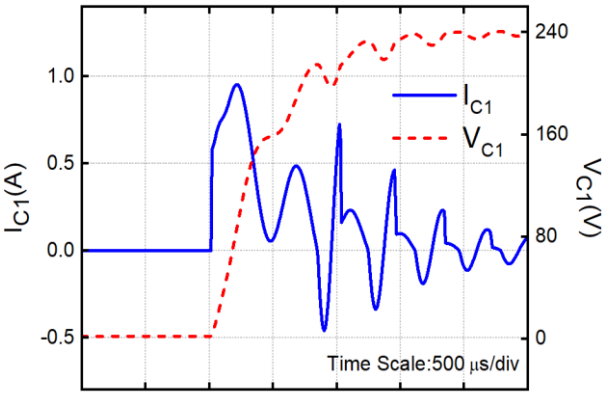


Figure 3.16 Current from the DC source (Exp: solid orange line, Sim: dashed blue line)

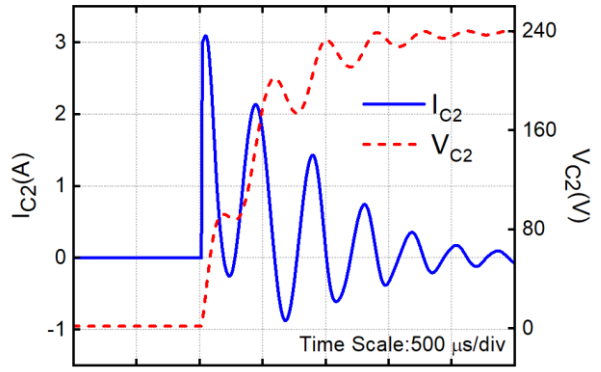
Fig. 3.17 demonstrates the waveforms of featured resonant circuit components (*i.e.*, C_0, C_1, C_2, D_2, L_1, and L_2) and the load during the transient period of SCR turnoff. The energy in LC components is released *via* resonance after the SCR turns off, eventually, turning off the load following its RC feature. As seen in Fig. 3.17 (e) & (f), the current through the inductor does not change instantaneously. Thus, the fault current passes through the Z-source capacitors (C_0, C_1, & C_2) when a fault occurs in the system. Fig. 3.17 (a), (b), & (c) illustrates the current and voltage waveforms of Z-source capacitors (C_0, C_1, & C_2), respectively. The resonance in LC components helps in the commutation of the SCR. Finally, the remaining energy in the system is released before the breaker is reset for the next cycle of operation. The load current goes to zero as the Z-source breaker trips successfully in the event of a fault as seen in Fig. 3.17 (g). The voltage and current waveform of the diode (D_2) is shown in Fig. 3.17 (d).


0
-3
-6
320
240
160
80
0
I_{C0}(A)
V_{C0}(V)
I_{C0}
V_{C0}
Time Scale:500 μs/div

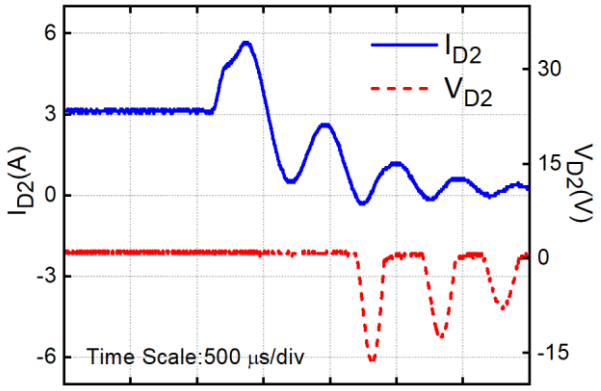
(a)


1.0
0.5
0.0
-0.5
240
160
80
0
I_{C1}(A)
V_{C1}(V)
I_{C1}
V_{C1}
Time Scale:500 μs/div

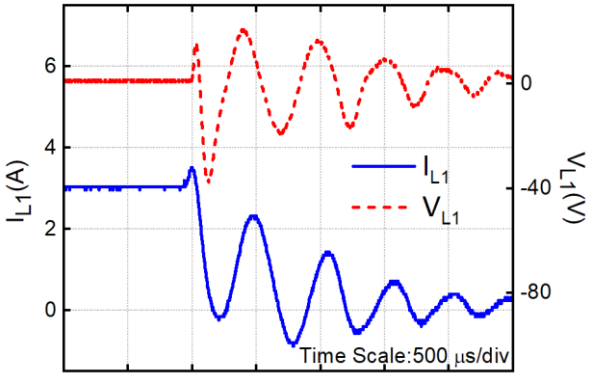
(b)


3
2
1
0
-1
240
160
80
0
I_{C2}(A)
V_{C2}(V)
I_{C2}
V_{C2}
Time Scale:500 μs/div

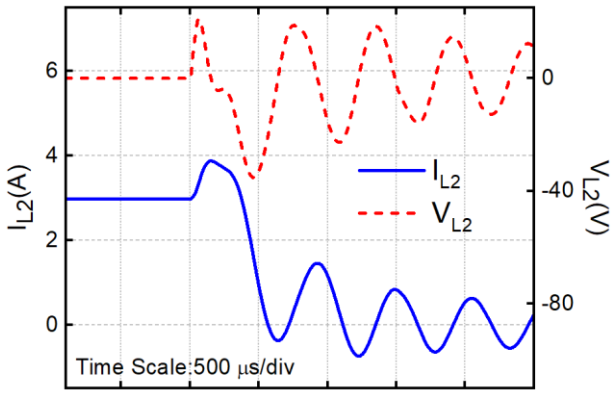
(c)


6
3
0
-3
-6
30
15
0
-15
I_{D2}(A)
V_{D2}(V)
I_{D2}
V_{D2}
Time Scale:500 μs/div

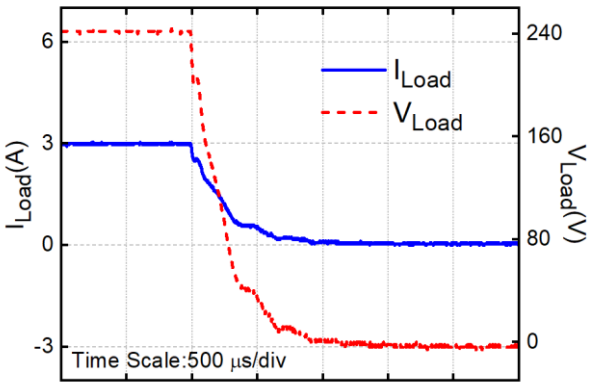
(d)


6
4
2
0
0
-40
-80
I_{L1}(A)
V_{L1}(V)
I_{L1}
V_{L1}
Time Scale:500 μs/div

(e)


6
4
2
0
0
-40
-80
I_{L2}(A)
V_{L2}(V)
I_{L2}
V_{L2}
Time Scale:500 μs/div

(f)



(g)

(a) voltage and current of C_0 (current, solid blue line; voltage, dashed red line)
(b) voltage and current of C_1 (current, solid blue line; voltage, dashed red line)
(c) voltage and current of C_2 (current, solid blue line; voltage, dashed red line)
(d) voltage and current of diode D_2 (current, solid blue line; voltage, dashed red line)
(e) voltage and current of inductor L_1 (current, solid blue line; voltage, dashed red line)
(f) voltage and current of inductor L_2 (current, solid blue line; voltage, dashed red line)
(g) voltage and current at load (current, solid blue line; voltage, dashed red line).

Figure 3.17 Experiment waveforms of featured components in the ZCB circuit

F. Effect of Parameter Revision on ZCB's Power Delivery Efficiency

The Z-source capacitance adjustment is applied, and the power delivery efficiency of the ICC-BZCB with the adjusted C_0 is re-evaluated and compared to the original case in Fig 3.6. The comparison of voltage distribution in the ZCB components between the original and the adjusted cases is demonstrated in Fig. 3.18. A numerical analysis of power loss for the two cases *i.e.*, with and without the Z-source capacitance adjustments can be seen in Table 15. The same value of parameters as listed in Table 13 are used for the ZCB design. Since the only parameter adjusted is the Z-source capacitance (C_0), it is noticed that the efficiency has a minor decrease of only 0.35 % caused by this adjustment. This 0.35 % drop is distributed evenly among all the ZCB parameters as observed in the adjusted case of Table 15. The maximum loss can be seen on the switching devices *i.e.*, the diode and the SCR. The breaker's overall efficiency for both adjusted and preliminary cases is greater than 99 %, which makes the ZCB an efficient candidate for the protection of DC systems.

Table 15. Power loss comparison for preliminary and adjusted case of C_0 in the ICC-BZCB

ZCB Component	**Experimental Power Loss (in %)**	
	Preliminary	*Adjusted*
L_1	0.094	0.138
L_2	0.097	0.16
C_1 & C_2	$1.1 \times 10^{-6} \approx 0$ (NEGL.)	$1.54 \times 10^{-6} \approx 0$ (NEGL.)
Diode (D_2)	0.17	0.28
SCR (T_1)	0.213	0.346
Overall Power Loss	0.574	0.924
Efficiency	99.426	99.076

* NEGL. stands for Negligible.

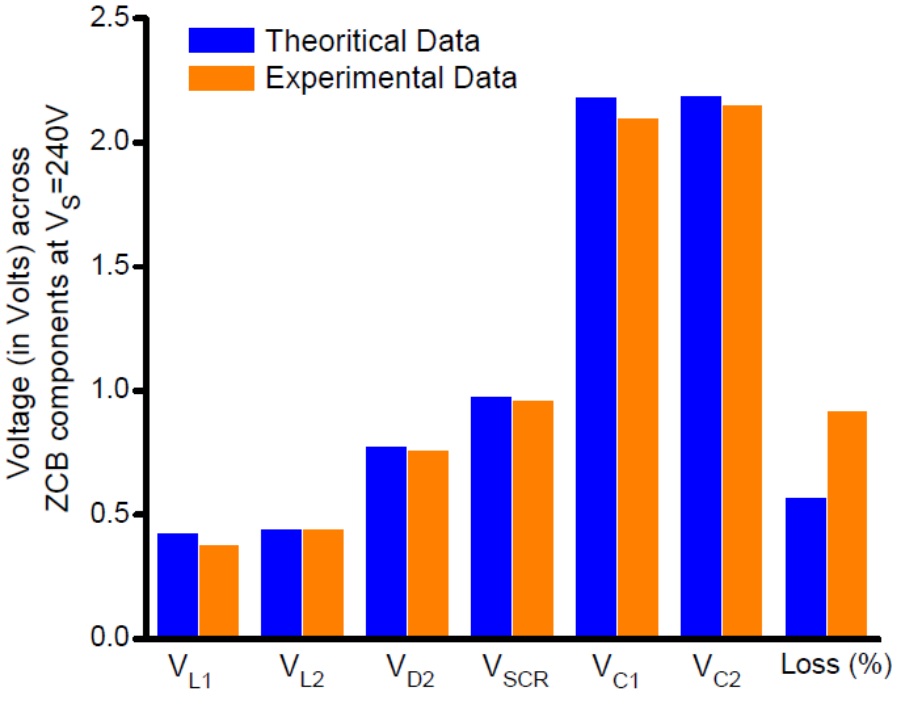


Figure 3.18 Comparison of voltage distribution of ZCB components between the original and adjusted cases

3.6 Summary

A relationship between steady-state power loss and required tripping time for ZCB is studied based on the topology of ICC-BZCB. From the analysis, it is found that the voltages of the capacitors and inductors in ZCB increase along with source voltage, while the voltage of SCR and power diode remains constant. The tripping time of SCR is a major consideration when evaluating the overall power loss in the ZCB during normal steady-state operation when there is a requirement of energizing the same load. In general, for selecting an inductor, it can be concluded that as the permeability of the inductor increases, losses associated with it decreases accordingly. For a constant permeability, the required number of inductor windings increases with an increase in tripping time of SCR, which in turn increases overall power loss in the DC network.

A novel method of configuring Z-source capacitors is proposed to ensure the turnoff of SCR in an ICC-BZCB. The correction equation of Z-source capacitance is developed to accumulate enough negative SCR current for the depletion region buildup and thus guarantee the success rate of ZCB in DC circuit protection. Simultaneously, the new method can preserve the required tripping time to improve the controllability of ZCB. The experiments on a hardware testbed verified the effectiveness of the method. In addition, it was found that the correction and adjustment of the Z-source capacitor has a negligible effect on ZCB's power delivery efficiency.

Therefore, with this novel method of Z-source capacitor configuration, the ZCB can be a good candidate for the protection of the distributed energy resources, HVDC transmission, and MVDC distribution networks as defined in the IEEE Std. 1547-2018. Based on the demonstrated behavior of ZCB in response to faults, the coordination of ZCBs and other switchgear can be maintained efficiently to enhance the reliability of the hierarchical protection scheme for pure DC systems and hybrid AC/DC power networks.

CHAPTER 4

HIGH IMPEDANCE FAULT DETECTION USING ICC-BZCB

4.1 Introduction

Integration of digital communication and sensing technologies has played a major role in the rapid development of modern power systems in the past few decades. It improves the efficiency, reliability, and control flexibility in electric power networks. The previously unnoticeable disturbances are now detected easily due to advancements in technology and automation in the transmission/distribution system. The over-current protection devices easily detect the low-impedance faults caused by the high conductivity elements. However, real-time monitoring and locating the High-Impedance Faults (HIFs) are still challenging tasks that need careful attention. The detection of these low-grade faults has now been a challenge for the distribution engineers for many years.

The HIF occurs in a medium-voltage power system when there is an electrical contact between an energized conductor and a highly resistive surface (such as sand, asphalt, tree branches, *etc.*) They do not draw enough current needed to operate the conventional overcurrent protection devices such as relays, fuses, and reclosers. The most common cause for the occurrence of a HIF is breaking an overhead conductor and falling to the ground, which in most cases results in a fire hazard, as seen in Fig. 4.1. A HIF's characteristics are very similar to that of the noisy, small, and poorly behaved single-phase load [74]. This results in the HIF remaining uncleared and exposes the person to a high risk of electric shock. The possibility of fire hazards can impose a threat to the livestock and can cause significant damages to properties [75].

Figure 4.1 A downed conductor arcs to the wet grass [76, 77]

The utilities for public safety often install expensive and sophisticated commercial or self-developed HIF detection devices. The two most commonly installed products are the High Impedance Fault Analysis System (HIFAS) from Nordon Technologies and the Digital Feeder Monitor (DFM) from General Electric [78]. Integration of renewable energy resources in DC format has led to the fast development of the DC transmission and distribution systems in the past decades. Sometimes, a fault impedance in the low-voltage DC system is comparable to the nominal ratings. This results in the low magnitude short-circuit currents producing the electric arcs with high-frequency contents [79]. Thus, the HIF condition in DC power systems should be detected and subsequently isolated to minimize any significant danger.

The research in the past shows that though most of the HIFs are different from each other, they do have some similar characteristics that one uses to detect the presence of a fault. Thus, the

techniques implementing the manipulation and processing of voltage and current measurements during the HIF conditions are used to overcome the problem of HIFs for the power grids. A HIF is detected by extracting the HIF characteristics using the wavelet transform-based method by decomposing a signal into different frequency bands and locations in time, as introduced in [80, 81]. The study in [82] presents a method of placing multiple smart meters across the power network for HIF detection. Additionally, a short-time Fourier transform approach was proposed in [83], where the phase current's main harmonic components are extracted to identify HIF occurrence. In [84], the waveform distortion analysis with the solid electrical breakdown theory was performed to detect the HIF in a network. Likewise, the HIF condition in [85] was detected using the quasi differential zero sequence protection to analyse the current zero-sequence RMS value on feeders. A study of the change in impedance characteristics by injecting a high-frequency current signal into the grid to impose voltage on its node for detecting the HIF was performed in [86]. Similarly, a decision tree-based methodology for the detection of a HIF was implemented in [78]. Despite the wide variety of existing methods, due to the limitations such as lack of versatility, improper defining of effective variables, and associated limits, detection of HIF in a power system may remain unnoticed [87].

4.2 ZCB and HIF Detection/Interruption Modes

A new method specifying the parameters of the ICC-BZCB to detect and interrupt HIFs is proposed that enables a new function of ICC-BZCB. The system reliability can be vastly improved with the application of the proposed method that can be easily integrated into a power network. The proposed method can identify HIF conditions by monitoring the status of Z-source capacitances. The operation of ZCB in case of a HIF can be classified into two modes: a) HIF

Detection Mode (HD-Mode); b) HIF Interruption Mode (HI-Mode). The HD-Mode is defined as the voltage oscillation on Z-source capacitances that demonstrates the HIF occurrence but no HIF interruption, whereas the HI-Mode is defined as the response of the ZCB to a HIF in order to cut it off. This is an easy and efficient way in practical application to realize the HDM/HIM specification in ZCB.

4.3 Method of HIF Detection/Interruption with Z-source Breaker

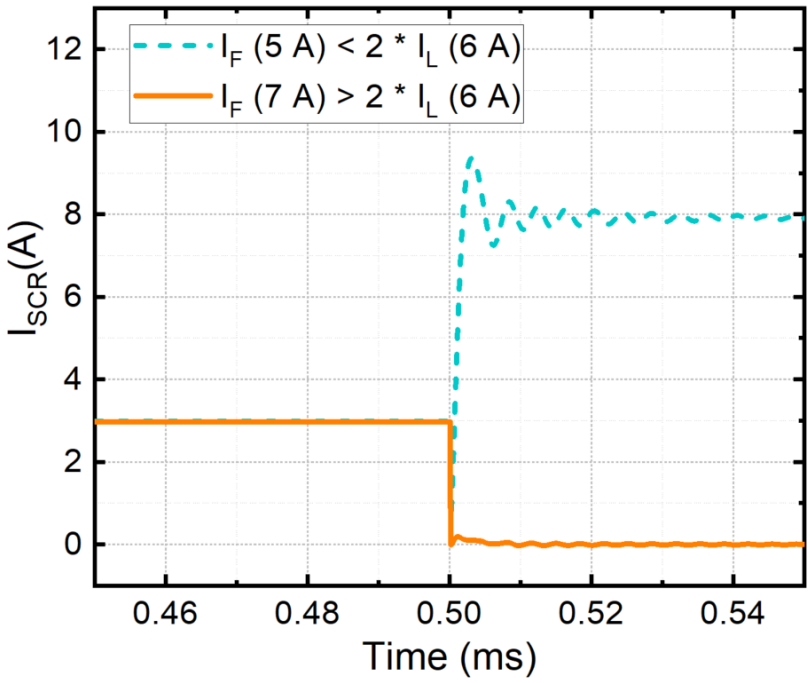


Figure 4.2 SCR currents of ZCB in two different cases of fault current to prove the feasibility of ZCB control

(See Appendix A5 for copyright information)

A new design methodology for detecting and interrupting the HIF specifying the ICC-BZCB parameters is proposed. A proper component sizing enables HIF detection/interruption in the ICC-BZCB. The application of this method is studied and verified in a 240-V, 3-A DC system.

The ZCB parameters for the chosen system are obtained from Table 11. The ICC-BZCB designed in the laboratory can trigger any fault current higher than or equal to the minimum detectable fault current as selected by the operator, which is two times the rated load current, *i.e.*, 2 * I_L = 6 A.

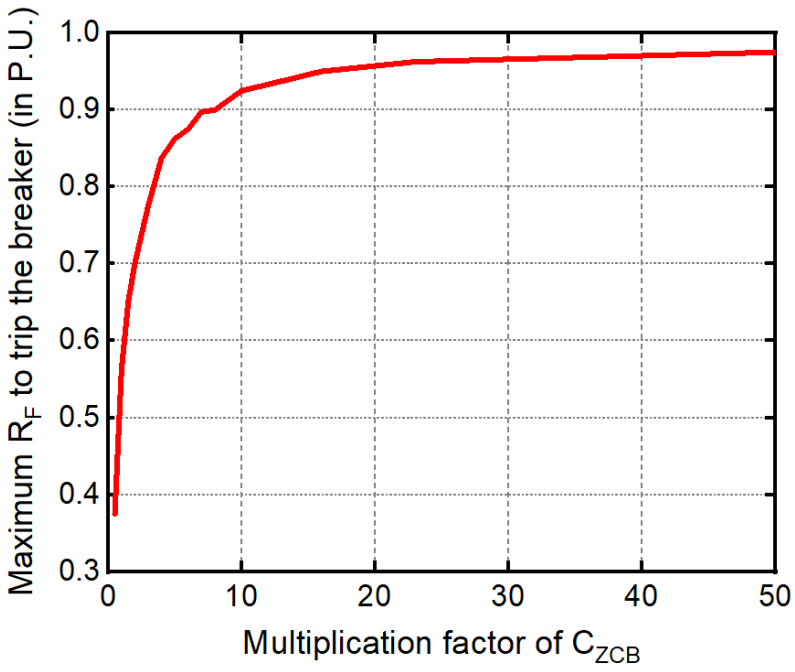


Figure 4.3 Graph showing the relation between R_f and $C_{ZCB\text{-}Mul}$

The preliminary design is studied for two different cases of fault currents: Case I with a fault current I_F = 5 A, which is less than twice the rated load current; and Case II with I_F = 7 A, which is higher than twice the rated load current. Fig. 4.2 shows the operation of a ZCB designed with the specification illustrated in Table 11 for the two different fault current cases. It is observed that the breaker is irresponsive in Case I with I_F = 5 A, whereas the fault current is cut off successfully in Case II, *i.e.*, I_F = 7 A [45]. This test shows that specifying the parameters of ZCB can be a possible solution for the HIF in a DC system.

A new method specifying the Z-source capacitances (C_{ZCB}) is proposed to control ZCB operating into the HD-Mode and HI-Mode freely. In this method, the relative response of an ICC-BZCB is studied by increasing all the Z-source capacitances (*i.e.,* C_0, C_1, and C_2) proportionally. It is found that as the value of C_{ZCB} increases the reverse current contribution of C_{ZCB} in responding to the HIF increases accordingly within the breaker. Fig. 4.3 represents the relationship between the fault resistance (R_f) and the required Z-source capacitance ($C_{ZCB\text{-}Mul}$) to turn the SCR off under HIF conditions. As the value of C_{ZCB} increases, the minimum detectable fault conductance of the breaker becomes even smaller. Thus, the breaker is able to cut-off a relatively smaller fault current with an increase in the value of C_{ZCB}. Table 11 is used as the base values for the multiplication factor of C_{ZCB} in Fig. 4.3 to specify and control HIF detection/interruption modes.

The maximum fault resistance that a breaker can trip under HIFs, as seen in Fig. 4.3, is derived as (22). The equivalent circuit of ICC-BZCB right after a fault is represented in Fig. 4.4, which indicates the currents contributed to the SCR's turnoff supplied by the Z-source capacitors. The ZCB, with the proper adjustments of Z-source capacitors, is now enabled to handle a fault current from a HIF with an even smaller conductance value.

$$R_{F-Max} = \frac{R_{Fault-Base}}{50}.(7\ln(C_{ZCB-Mul}) + 30) \tag{22}$$

where: $R_{F\text{-}Max}$ is the maximum fault resistance that a ZCB can trip independently (in Ω); $R_{Fault\text{-}Base}$ is the base fault resistance (in Ω) that equals 80 Ω; $C_{ZCB\text{-}Mul}$ is the multiplication factor, by which the Z-source capacitors should be amplified on the preliminary design values listed in Table 11.

From theoretical analysis, the current through the Z-source capacitor (C_2) in terms of fault current (i_F) given in [57] can also be restructured for the proposed HIF detection/interruption control, as:

$$i_{C2} = C_{ZCB-Mul}\left(\frac{C_{ZCB}}{C_{ZCB}.C_{ZCB-Mul} + 1.5C_L}\right)i_F \quad (23)$$

Combining (23) with the equations of (24) and (25) (*i.e.* the equation (1) & (5) in [57]), a modified equation for the minimum detectable fault conductance is derived as (26):

$$I_{Load} = \frac{V_s - v_{f,SCR} - v_{f,Diode}}{R_{Load} + R_{on,SCR} + R_{on,Diode} + R_{inductors}} \quad (24)$$

where, V_s is source voltage; $V_{f,\ SCR}$ & $V_{f,\ Diode}$ are forward voltage of the SCR and the diode respectively; R_{Load} = Load resistance, $R_{on,\ SCR}$ = on-state SCR resistance, $R_{on,Diode}$ = on-state diode resistance, $R_{inductors}$ = inductor resistance.

$$i_{fault} = G.V_S \quad (25)$$

$$G_{min} = \frac{C_{ZCB-Mul}.C_{ZCB} + 1.5C_L}{C_{ZCB-Mul}.C_{ZCB}}.\frac{1}{R_L} \quad (26)$$

Using equations (22) and (26), the same curve in Fig. 4.3 can be obtained. However, for practical applications, equation (22) is much more convenient than (26). Thus, (22) is used for any further analysis of HIF detection using an ICC-BZCB. The post-fault behaviour of ICC-BZCB is studied to define the HD-Mode and HI-Mode, respectively. During initial moments of a fault, the total transient current of C_0 and C_1 are in the reverse direction of SCR's pre-fault current [57], as shown in Fig. 4.4. Thus, if the magnitude of the sum of these reversely flowing currents (i_{C0} & i_{C1}) is less than the holding current (i_H) of the SCR, *i.e.* (i_{C0} + i_{C1}) < i_H, the SCR would not turn off and operates in HIF detection mode. In this state, a HIF is detected by the breaker but not successfully interrupted.

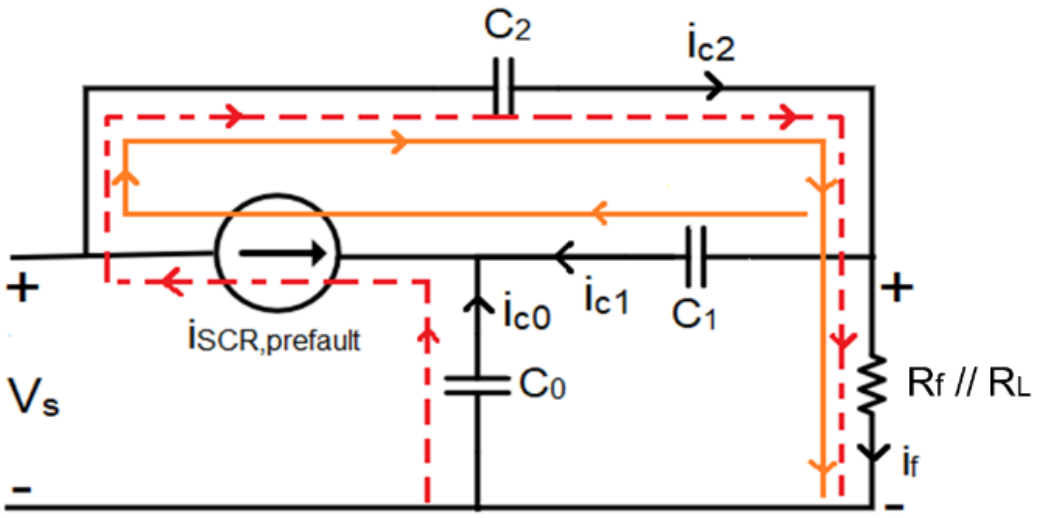


Figure 4.4 Equivalent ZCB circuit for analyzing the current during the initial instance of fault

Likewise, if the magnitude of the sum of the reversely flowing currents (i_{C0} & i_{C1}) is greater than the holding current (i_H) of the SCR, *i.e.* ($i_{C0} + i_{C1}$) > i_H for an adequate period of time, the SCR turns off and operates in HIF interruption mode. The holding current of SCR is the minimum anode current required to turn it off. The discharging status of ZCB capacitance is monitored to detect the HIF. In other words, the SCR does not turn off if a HIF cannot induce sufficient discharging from Z-source capacitors. Thus, the HIF might remain unnoticed and cause significant damages to electric devices in the system. In addition, the discharging amount is also proportional to the capacitance values of the Z-source capacitors. Therefore, by adjusting the Z-source capacitances, the ICC-BZCB can be controlled and specified in either HD-Mode or HI-Mode, for HIF detection/interruptions.

Table 16. Adjusted C_{ZCB} for various $C_{ZCB\text{-}Mul}$

Base C_{ZCB} (μF)		**$C_{ZCB\text{-}New}$ = $C_{ZCB\text{-}Mul}$ * Base C_{ZCB} (μF)**		
	$C_{ZCB\text{-}MUL}$	1.0	2.0	3.0
2.2	$C_{ZCB\text{-}New}$	2.2	4.4	6.6

A simulation study is performed using the MATLAB/Simulink software on the low-power DC system with the adjusted Z-source capacitance values obtained from Table 16 to demonstrate the effect of equation (22) for HIF detection/interruption. In the simulation tests, the Z-source capacitances are adjusted along with a rise in fault resistance. All the breaker parameters applied are initially acquired from Table 11. C_{CZB} value is magnified by 1.0, 2.0, and 3.0 times, respectively. The updated values of C_{ZCB} for different multiplication factors are listed in Table 16. The fault resistance is set to R_F = 40 Ω, 50 Ω, and 60 Ω, respectively, and the performance of the breaker with the various C_{ZCB} values is analyzed.

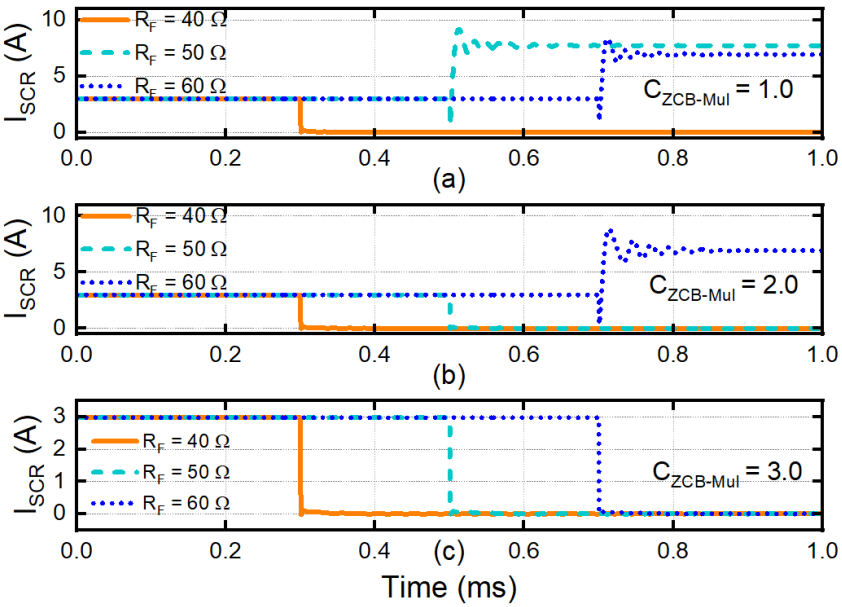


Figure 4.5 Three simulation tests to verify (22): a) $C_{ZCB\text{-}Mul}$ = 1.0; b) $C_{ZCB\text{-}Mul}$ = 2.0; c) $C_{ZCB\text{-}Mul}$ = 3.0 times

The SCR currents for various R_F values along with adjusted C_{ZCB} is seen in Fig. 4.5. The maximum R_F that the breaker can trip for case (a) with $C_{ZCB\text{-}Mul}$ = 1.0 times is 40 Ω. Thus, only the case with R_F = 40 Ω is tripped, whereas the other two cases of fault current remain uncleared. Likewise, the value of $R_{F\text{-}Max}$ calculated using (22) for $C_{ZCB\text{-}MUL}$ = 2.0 is $R_{F-Max} \approx 56\ \Omega$, and $R_{F\text{-}Max}$ for $C_{ZCB\text{-}MUL}$ = 3.0 is $R_{F-Max} \approx 61\ \Omega$. Thus, from Fig. 4.5 (b), it can be observed that for $C_{ZCB\text{-}MUL}$ = 2.0, the breaker successfully turns off for R_F = 40 Ω & 50 Ω but is irresponsive to 60 Ω as this resistance value exceeds the maximum R_F of 56 Ω for this case. However, for $C_{ZCB\text{-}MUL}$ = 3.0, the maximum R_F is 61 Ω, leading to three successful interruptions without failing since it is higher than all the three R_F values, as seen in Fig 4.5 (c). Thus, these tests verify the effectiveness of the proposed method by specifying ZCB's HD-Mode/HI-Mode *via* (22). To prove the general usage of the proposed method in DC power networks, it is further verified *via* experiment tests on a low-power testbed in the lab and simulation tests on a high-power testbed.

4.4 Results

In this section, the effectiveness of the derived curve for HIF detection in Fig. 4.3 is validated with the simulation, and experimental results. To verify the simulation study in Section 4.3 and accuracy of Fig. 4.5, a low-power experimental test is performed on a hardware testbed. Next, a high-power simulation test of 5-kV, 5-MW, which represents a high resistive load is performed in MATLAB/Simulink environment, to prove the general usage of (22) in different systems.

4.4.1 Experimental Verification with 180-W, 120-V Testbed

An ICC-BZCB experimental prototype, as seen in Fig. 3.5 is designed to verify the proposed HIF control of ZCB. The testbed was established according to the parameters listed in

Table 11. When the power supply is 240 V and the ZCB is specified to the "*HI-Mode*", the fault current can be successfully cut off, as shown in Fig. 4.6. However, as the fault impedance increases, the ability of the ICC-BZCB to interrupt the fault current gradually decreases, which causes the fault in the system to remain uncleared. Since the lab experiments were performed in both HI-Mode and HD-Mode, due to the limitations of the current rating of 8 A in the "*Main DC Power Supply*," some cases of "*HD-Mode*" were intentionally performed with a lower input voltage of 120 V. This resulted in the pre-fault SCR current of 1.5 A and maintained the uncontrolled fault currents under 4.5 A to protect the laboratory equipment, as the actual expected fault current is 9 A under 240 V power supply.

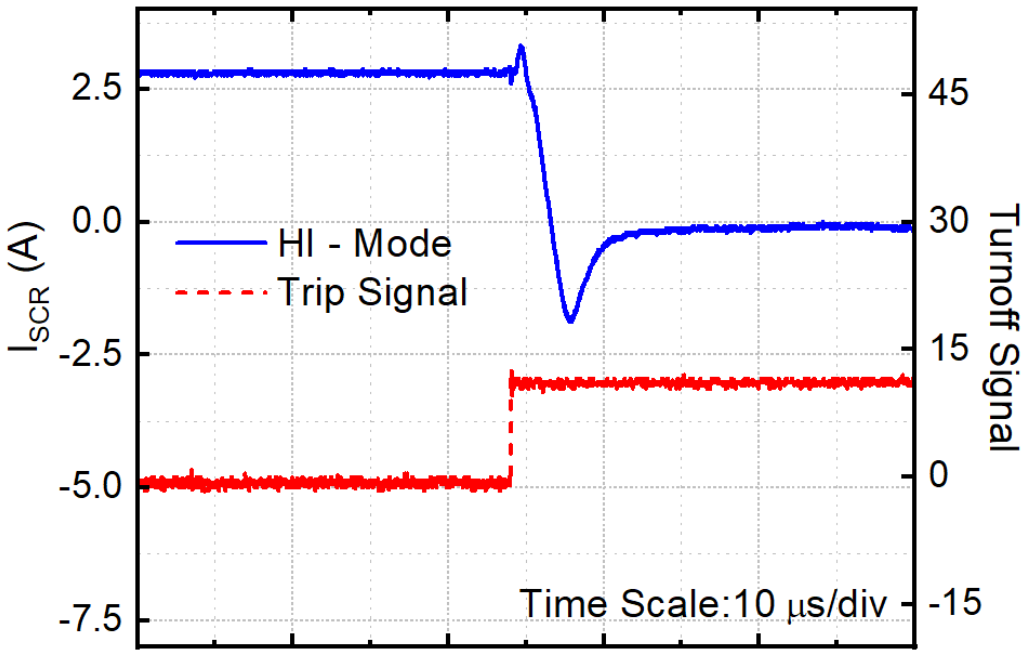


Figure 4.6 Indication of HI-Mode with a fault current of 3 A cutoff under 240 V power supply (SCR current, in blue solid line; fault turnoff signal, in red dashed line)

Three sets of experimental tests are performed on the testbed to verify the proposed method's effectiveness by adjusting the values of Z-source capacitances according to Fig. 4.3 and (22). The C_{ZCB} is adjusted to 1.0, 2.0, and 4.0 times to their initial specified value in Table 11. During the experiments, a fault is emulated by an additional resistive branch connected in series to a controlled IGBT forming the "*Fault Emulation Board*," as shown in Fig. 3.5.

*Test #1 – "C_{ZCB} amplified by 1.0 times, i.e., C_{Adj} = 1.0 * C_{ZCB}":*

In this test, the fault resistance (R_F) is gradually increased, and the ZCB's behavior in response to the fault current is analyzed. The four cases of fault resistance considered for this study are: R_F = 35 Ω, 40 Ω, 50 Ω, and 62.5 Ω, respectively. The multiplication factor of C_{ZCB} for this test is set to 1.0, *i.e.*, the same Z-source capacitance values are used as calculated in Table 11, which is 2.2 μF. All the other parameters remain unchanged except C_{ZCB}.

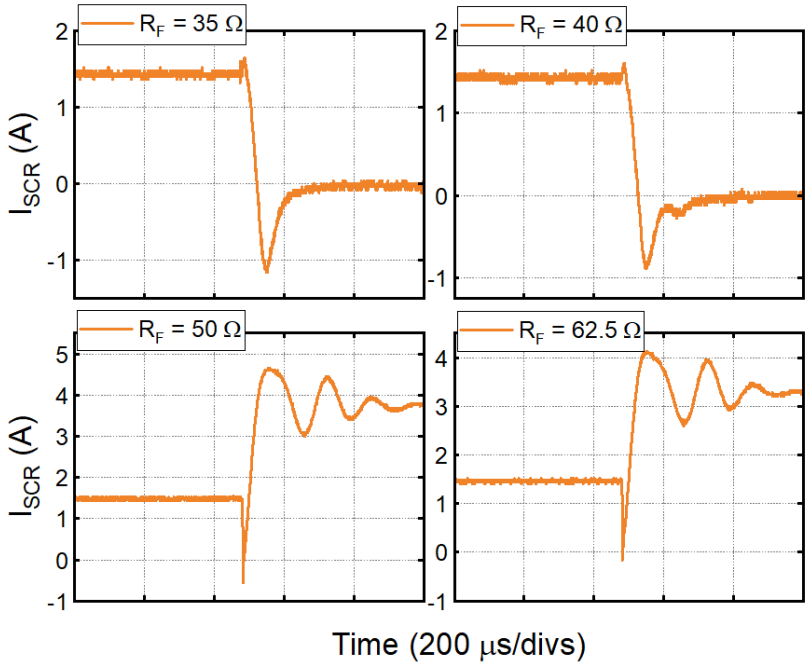


Figure 4.7 The ZCB's cut-off behavior for $C_{ZCB\text{-}Mul}$ = 1.0.

As seen in Fig. 4.7, when the ZCB operates in the HI-Mode, the breaker cuts the circuit off in the HIF cases of lower fault resistances *i.e.*, in the cases of ($0.438 * R_{Fault\_Base} = 35\ \Omega$) and ($0.5 * R_{Fault\_Base} = 40\ \Omega$). However, for higher fault resistances (in the cases of $0.625 * R_{Fault\_Base} = 50\ \Omega$ and $0.78 * R_{Fault\_Base} = 62.5\ \Omega$), the ZCB does not cut off the fault and stays in HD-Mode. A HIF can be detected by monitoring the status of C_{ZCB} and reported to the power system operator. The experimental results match the simulation analysis of Fig. 4.5 (a).

Test #2 – "C_{ZCB} amplified by 2.0 times, i.e., $C_{Adj} = 2.0 * C_{ZCB}$":

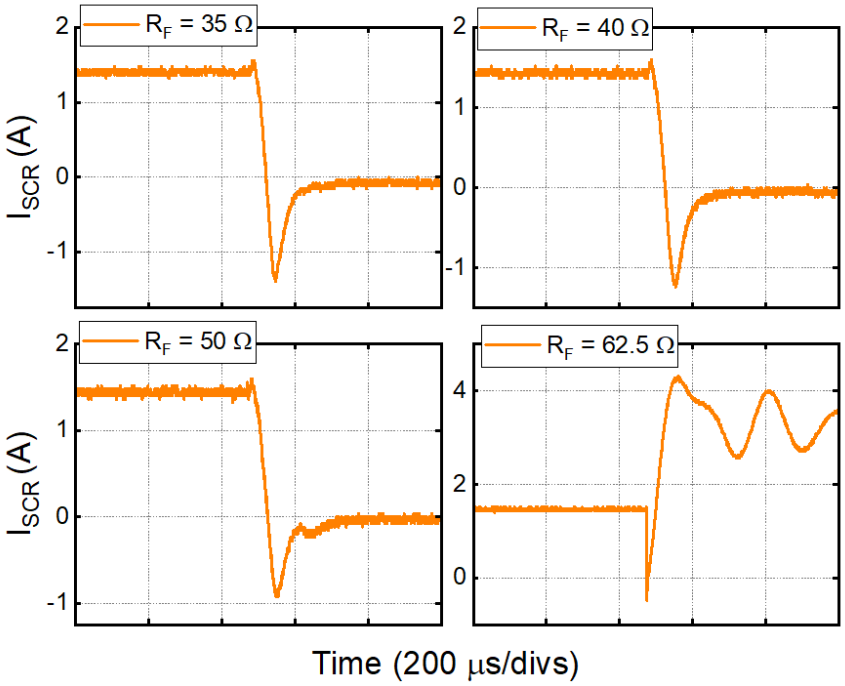


Figure 4.8 The ZCB's cut-off behavior for $C_{ZCB\text{-}Mul} = 2.0$.

In this test, the multiplication factor of C_{ZCB} is increased by 2.0 times. Thus, the boundary resistance of HI-Mode and HD-Mode increases to 56 Ω. This increase in the boundary leads to the breaker's turnoff when the fault resistance is $R_F = 0.625 * R_{Fault\_Base} = 50\ \Omega$, thereby, turning the

breaker off for three cases of fault current with R_F = 35 Ω, 40 Ω, and 50 Ω, respectively, as shown in Fig. 4.8. It matches the result of Fig. 4.5 (b).

*Test #3 – "C_{ZCB} amplified by 4.0 times, i.e., C_{Adj} = 4.0 * C_{ZCB}":*

In this test, the multiplication factor of C_{ZCB} is further increased to 4.0 times which increases the boundary of the HI-Mode and HD-Mode to 63.5 Ω calculated using (22). The increase in boundary of R_F beyond Test #2 leads to the breaker's turnoff when the fault resistance is at the highest selected value of R_F = 0.78 * R_{Fault_Base} = 62.5 Ω, as shown in Fig. 4.9. Thus, the breaker is able to cut-off all the specified fault cases with C_{ZCB} = 4.0 times. The waveform for voltage across the Z-source capacitors (C_0, C_1, and C_2) for the case with C_{ZCB} = 4.0 times and R_F = 62.5 Ω is shown in Fig. 4.10.

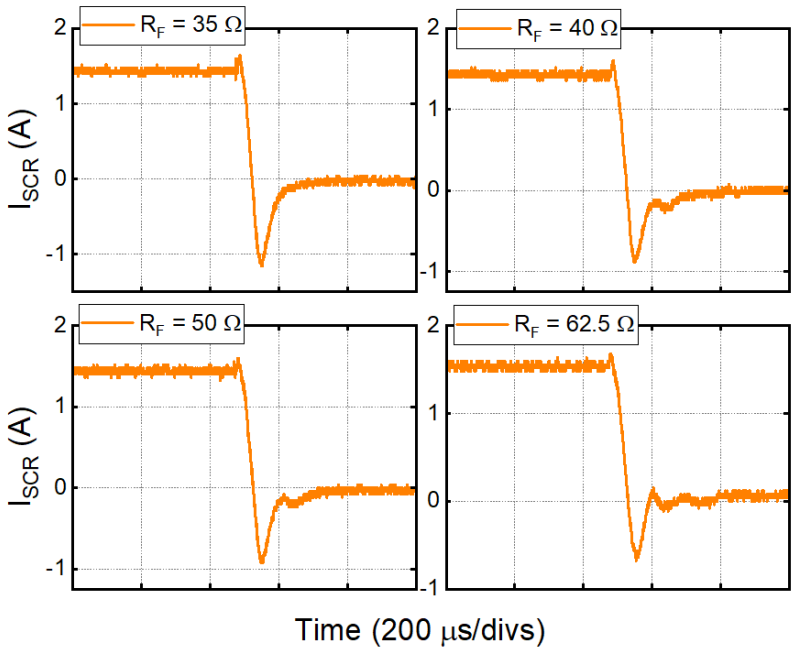


Figure 4.9 The ZCB's cut-off behavior for $C_{ZCB\text{-}Mul}$ = 4.0.

Table 17 summarizes the status of ZCB for different cases of HIFs with adjusted C_{ZCB} values. These results prove the effectiveness of (22) and demonstrate the controllability of ZCB towards HIFs, which is enabled by adjusting C_{ZCB} values properly.

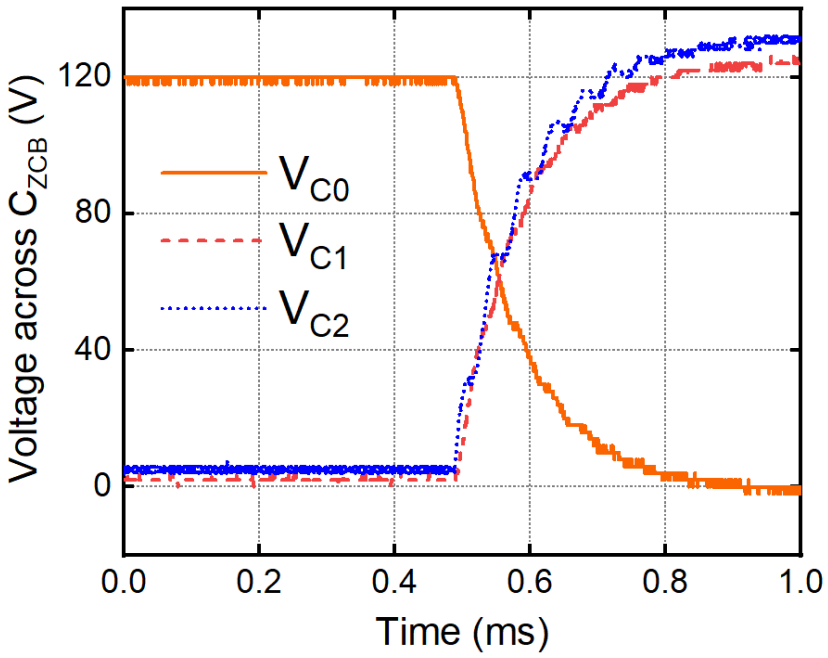


Figure 4.10 Voltage across Z-source capacitors for C_{ZCB} = 4.0 times and R_F = 62.5 Ω

Table 17. Summary of ZCB's status in three experiments

R_F (in Ω)	**ZCB Status**		
	C_{ZCB} = 1.0	C_{ZCB} = 2.0	C_{ZCB} = 4.0
35 Ω & 40 Ω	ON	OFF	OFF
50 Ω	ON	OFF	OFF
62.5 Ω	ON	ON	OFF

4.4.2 Simulation Tests of a 5-MW, 5-kV Case

A 5-MW, 5-kV case representing a high-resistive load is studied in the MATLAB/Simulink environment to prove the general usage of (22). Table 18 lists the parameters used for designing the simulation system. The fault resistance is gradually increased, and the response of the ZCB to this varying fault current is observed.

Table 18. Specified parameters for simulation system

Parameter	**Remark**	**Value**
$C_1 = C_2 = C_0 = C_{ZCB}$	Z-source capacitors	36.92 µF
$L_1 = L_2 = L_{ZCB}$	Z-source inductors	76.9 µH
C_{Load}	Load capacitor	20.25 µF
V_{Source}	Source voltage	5000 V
R_{Load}	Load resistance	5 Ω
R_{Fault_base}	Fault resistance base	5 Ω
P_{Load}	Max. Load Power	5 MW
t_q	SCR tripping time	10 µs

Analysis of the peak currents through the Z-source capacitors is used for numerically validating the effectiveness of the proposed method. As stated earlier, "*During initial moments of a fault, the total transient current of C_0 and C_1 are in the reverse direction of SCR's pre-fault current.*" Thus, the magnitude of the sum of i_{C0} & i_{C1} should be higher than the magnitude of the rated current of SCR at pre-fault in order to ensure the SCR to commutate off naturally. For this test, the holding current of SCR (i_H) is 1 kA. Fig. 4.11 and 4.12 shows the transient currents of the Z-source capacitors (C_0, C_1, and C_2) and the load capacitor (C_L). These currents are measured under different HIF resistances that are used for the performance analysis of ZCB towards HIFs.

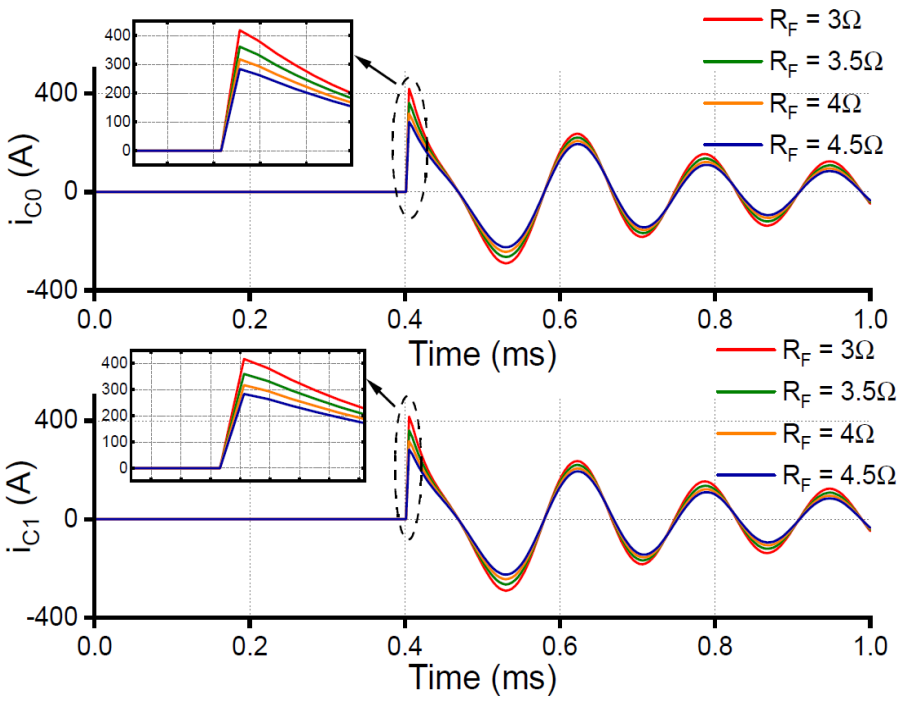


Figure 4.11. Transient currents through C_0 & C_1 for different HIF resistances with $C_{ZCB\text{-}Mul}$ = 1.0

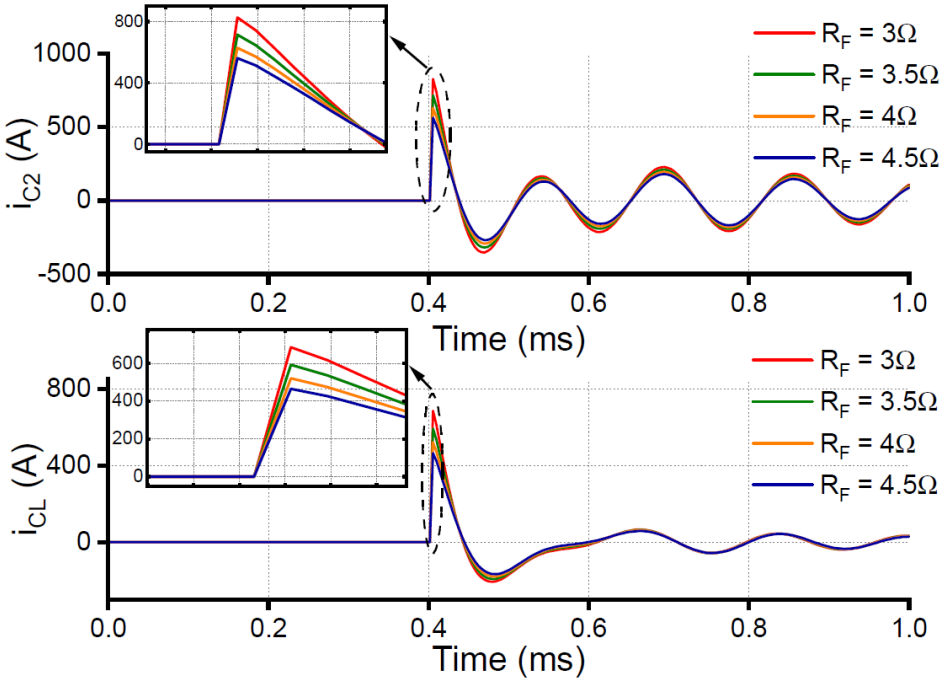


Figure 4.12 Transient currents through C_2 & C_L for different HIF resistances with $C_{ZCB\text{-}Mul}$ = 1.0

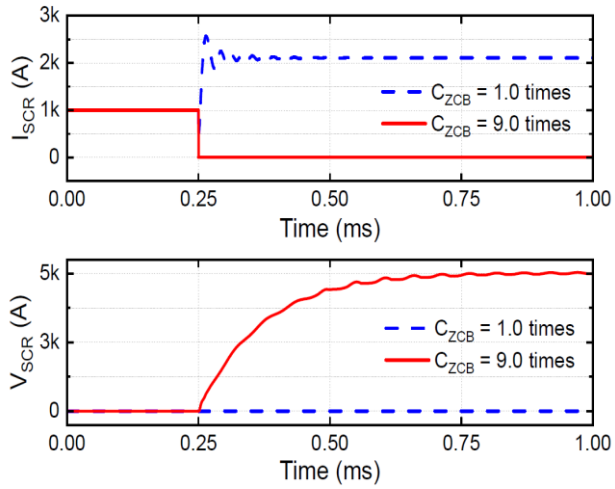
Table 19. Transient current and fault resistance analysis

R_F (Ω)	$C_{ZCB\text{-}MUL}$	i_{C0} (A)	i_{C1} (A)	$i_{C0} + i_{C1}$ (A)
3	1.0	418	417	835
3.5		362	361	723
4		318	318	636
4.5		283	284	567
3	3.0	755	755	1510
3.5		704	704	1408
4		474	472	946
4.5		419	417	836
3	7.0	851	851	1702
3.5		790	790	1580
4		743	743	1486
4.5		492	482	974
3	9.0	875	876	1751
3.5		813	812	1625
4		762	763	1525
4.5		723	722	1445

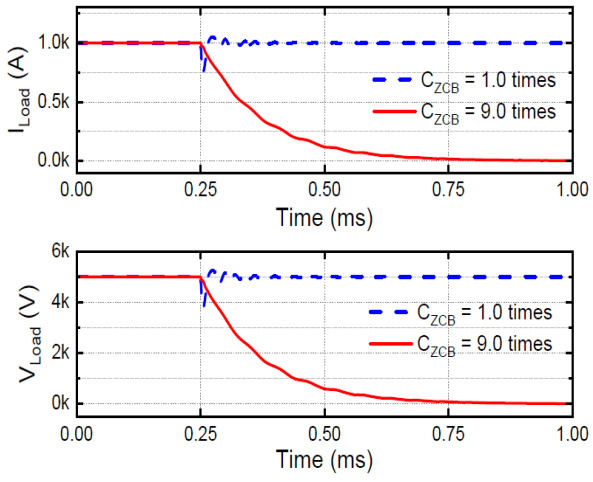
The fault resistance is gradually increased from 3 Ω to 4.5 Ω and the peaks of transient currents in C_{ZCB} are measured in these tests, as listed in Table 19. It is observed that the smaller the fault resistance, the higher is the peak of transient current. The sum of transient Z-source currents is less than the rated SCR current of 1 kA for all the cases with $C_{ZCB\text{-}Mul}$ = 1.0, as highlighted with red in Table 19. Thus, the SCR does not commutate off for any of the cases. With the adjustment in C_{ZCB} (*i.e.*, 3.0, 7.0, and 9.0 times), the sum of transient Z-source currents increases proportionally to $C_{ZCB\text{-}MUL}$, which causes the breaker to turnoff if the current is higher than the 1 kA threshold value. The SCR commutates off naturally for R_F = 3 Ω & 3.5 Ω when

$C_{ZCB\text{-}Mul}$ = 3.0. Likewise, it turns off for R_F = 3 Ω, 3.5 Ω, & 4.0 Ω when $C_{ZCB\text{-}Mul}$ = 7.0, and finally turns off for all the cases of R_F with $C_{ZCB\text{-}Mul}$ = 9.0, as highlighted in green in Table 19. Fig. 4.13 shows the waveform of voltages and currents for different ZCB components when the $C_{ZCB\text{-}MUL}$ equals 1.0 and 9.0 times, respectively.

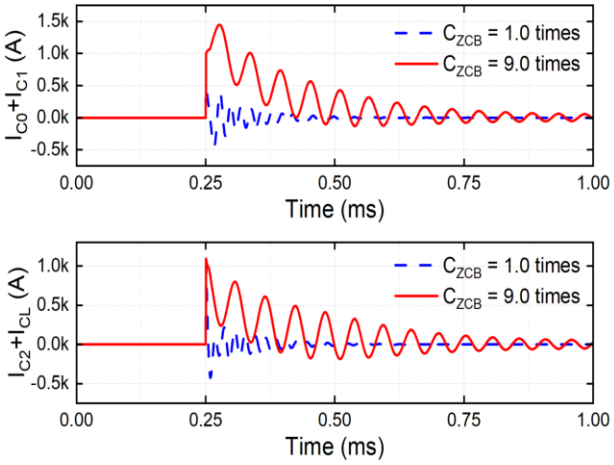
The result from Table 19 proves the effectiveness of using (22) to specify HD-Mode/HI-Mode of ZCB for the high-power case. Fig. 4.3 shows that the curve gradually goes into saturation as the value of R_F increases. Thus, for this method of HIF detection specifying the Z-source capacitance of a ZCB circuit, the effective region is (0, 10) in the multiplication factor of C_{ZCB}. Fortunately, for many power engineering standards and applications, the system operates in an overload condition and does not need a circuit cut-off when the R_F is higher than 1.0 per unit. Therefore, the proposed method can be applied to general HIF conditions.



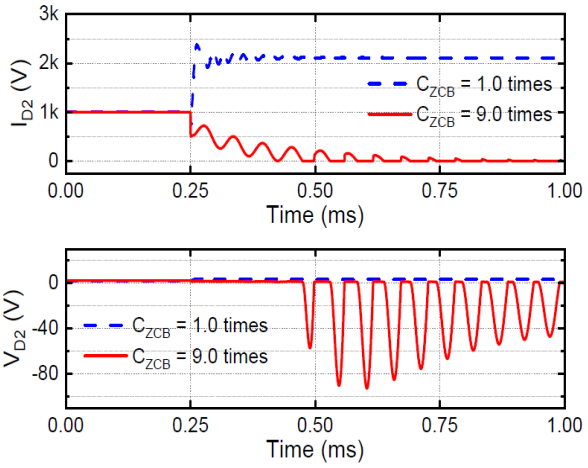
(a) current and voltage of SCR



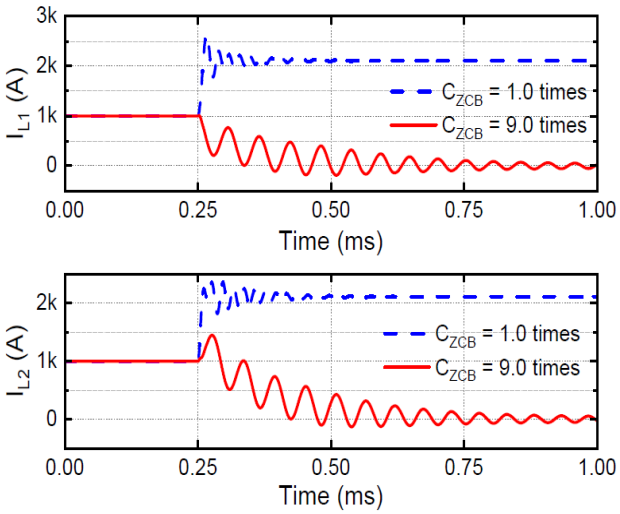
(b) current and voltage of the load



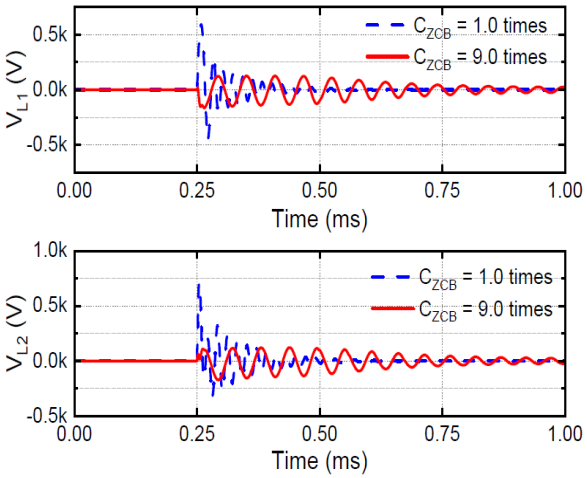
(c) transient currents (i_{C0}+i_{C1}) and (i_{C2}+i_{CL})



(d) current and voltage of diode D_2



(e) current of inductor L_1 and L_2



(f) voltage across inductor L_1 and L_2

Figure 4.13 Simulation waveforms of featured components in the ZCB circuit

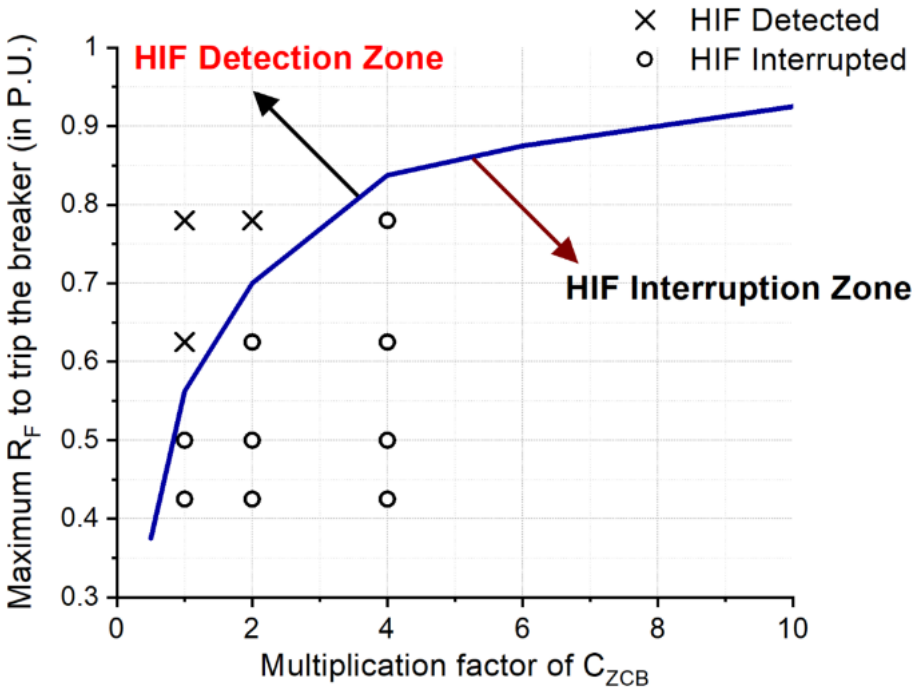


Figure 4.14 A zoomed-in effective region of Fig. 4.3 with specified HIF conditions
(See Appendix A5 for copyright information)

A zoomed-in figure as seen in Fig. 4.14 is generated using the data obtained from the laboratory experiments to show the effectiveness of identifying HIF conditions using the specifications of ICC-BZCB. The mark "X" in the Fig. 4.14 refers to the ZCB operating in HD-Mode, whereas the mark "O" refers to the operation of ZCB in HI-Mode. The "X" marks are separated from the "O" marks by the figure's derived curve. Hence, Fig. 4.14, along with the tests in sections 4.4.1 and 4.4.2, supports the proposed method's effectiveness and accuracy and proves the general usage of (22) in engineering practice.

4.5 Summary

The operation of a ZCB is specified in either the HI-Mode for HIF interruption or the HD-Mode for HIF detection using the new method. The parameter identification method proposed in

Chapter 3 is used to determine the ZCB parameters for both simulation and experimental validation. The Z-source capacitors are adjusted properly to enable the specification of ZCB. A mathematical relationship between the required Z-source capacitance and the maximum HIF resistance is derived. The effectiveness and general usage of the proposed method are validated in two different DC systems: a low-power experimental testbed and a high-power resistive simulation system. The fault current level detected/interrupted using the new method is as small as 2 times its nominal rated current. The method is easy to be implemented in modern power systems to enhance their controllability and reliability in protection. Thus, the presented method can increase the effectiveness of ZCB for any short-circuit fault detection/interruption, which further enhances the application of a ZCB for protecting the DC power network.

CHAPTER 5

CABLE LENGTH LIMIT ASSESSMENT FOR THE PROTECTION OF DC POWER NETWORKS USING Z-SOURCE CIRCUIT BREAKERS

5.1 Introduction

DC transmission lines are widely used in the modern power systems due to the advantages of long distance transmission, high transmission capacity, lower losses, and flexible power control [88-90]. The complexity in the working environment of a transmission line causes a high fault probability. Thus, locating a fault on the HVDC lines that interconnect two AC systems for a large power transfer is a challenging task which needs careful attention. The fault occurring on the HVDC transmission lines may cause instability of the entire power system which eventually results in a large economic loss. It also results in a large fault inrush current that influences the operation of the whole grid causing damage to the electric apparatus and even posing a significant threat to the human life. Thus, an accurate fault location method is beneficial to reduce the fault impact and ensure the safety of the power system in an event of a DC line fault [91, 92].

The application of an ICC-BZCB for detecting the effective cable length when applied on the DC distribution/transmission line is examined. This study introduces an approach of assessing the cable length limit (CLL) to ensure the effective protection of Z-source Circuit Breakers (ZCBs) in DC power networks. The line parameters of power cables have a significant impact on the cutoff performance of ZCBs. The simulation testing system of a 5-MW distribution line feeder is used for specifying the ZCB parameters. The effectiveness of ZCB protection is tested in groups of simulation tests with various cable lengths, fault current levels, and power delivery levels. The effective cable lengths have been assessed and analyzed for the ZCB to detect and successfully

interrupt a faulty branch in the DC network. From the testing results, relationship between CLL, fault current level, and power delivery level has been derived *i.e.,* the CLL decreases along with the decreasing fault current level, as well as the increasing power delivery level. A CLL curve is then developed for a certain load condition with this derived relationship which can be used by the power engineers to design and specify the effective protection ranges for ZCBs. An equation to calculate the effective length of ZCB for DC lines is derived with the help of the data obtained from the simulation analysis that can be used as a framework to generate new CLL curves for various load-power requirements. This study increases the reliability of ZCB's response to a fault in DC transmission and distribution lines. It can also help the power system designer/operator to maintain reliable protection with ZCBs in DC power system networks.

The existing methods for detecting the location of a fault in DC lines can be categorized into two groups: online fault location method and offline fault location method. The location of a fault in the online method is estimated using the voltage and current information after the fault occurrence and before tripping of the breaker [93]. In contrast, an auxiliary device is added after tripping the breaker to calculate fault in the offline method [94]. Some of the other existing techniques for locating faults in the DC lines are current measurement and machine learning method [95], transient measurement approach [96], a combination of least square method & boundary induction-based method [93], and distributed current sensing approach [97]. A travelling wave fault location method based on the wave front information is introduced in [98] that uses the step wave to extract all the frequency components when a DC line fault occurs in the network. The fault distance is located with the help of the known signal that is injected into the DC line in [99, 100]. However, prior information of the signal injection source is required to detect the fault location. Likewise, the study in [90] uses an algorithm based on travelling-wave natural frequency

to predict the location of DC line faults in an HVDC system. The fault distance can also be calculated using the surge travelling time and the wave speed [101, 102]. A fault location method suitable for low-voltage DC lines is presented in [103] where the residual current of DC line is used for locating the fault after tripping. The study in [104], uses the voltage across the DC fault current-limiting reactor to detect the short-circuit fault in the HVDC grids. In summary, most of the existing online and offline fault location methods adopt the RLC model that still requires a further improvement in terms of the error and time required for the fault location. Thus, in this research, a novel method using the topology of an ICC-BZCB is introduced to detect the fault location in the DC power lines using the current information after the occurrence of a fault in a system to attain maximum accuracy.

5.2 ZCB Application With and Without Line Parameter Considerations

A ZCB is a solid-state resonant style DCCB that is placed close to the device to-be-protected in the power network. It has an automatic fault decision-making capability and can quickly pull the main circuit current to zero when a short-circuit fault occurs in a DC microgrid [105]. It protects the electric component at its downstream. In an event of a fault occurrence, when the ZCB is far from the fault location, the additional impedance of DC cable might drag the ZCB's operation out of its detectable range. This causes failure in the fault protection which can damage the electric devices within the power system and even disintegrate the entire power network. Therefore, proper assessment of the Cable Length Limit (CLL) is essential to guarantee the ZCB's response to a fault in the desired ranges and provide an effective protection solution to assist the power engineers for designing the DC power networks. Fig. 5.1 shows the circuit representation of an ICC-BZCB when connected in series to the transmission line.

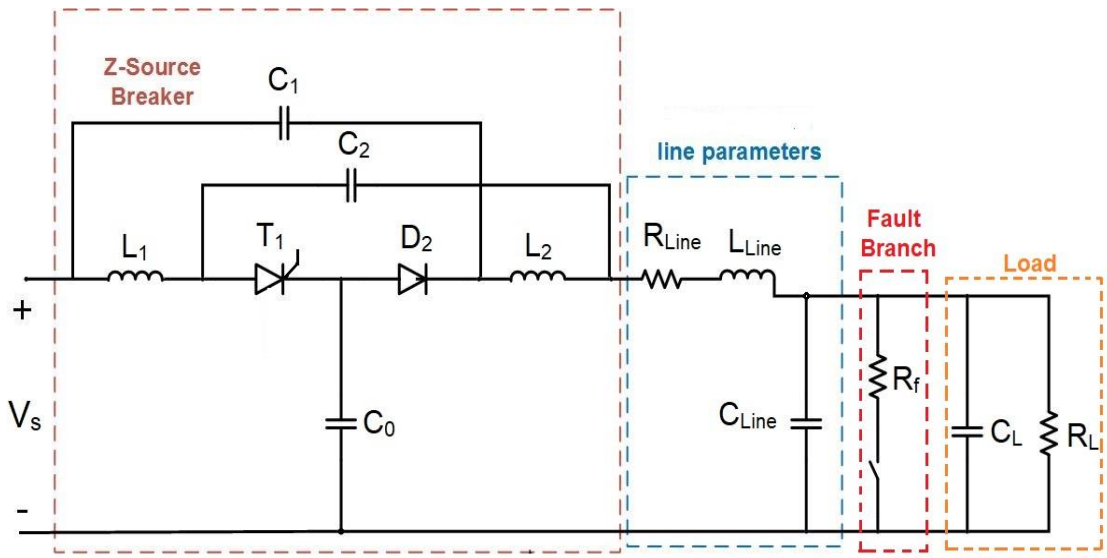


Figure 5.1 Topology of ICC-BZCB with transmission line parameters

Initially, the ZCB parameters are calculated according to the boundary conditions of the tripping time and other restrictions for a 5-MW system using equations (13-16). The testing system is configured with a supply voltage of (V_s = 5 kV) and a DC load which is represented by a parallel combination of C_L and R_L as seen in Fig. 5.1. The fault branch is represented by a switch in series with the fault resistance. The line parameters are obtained from [106, 107] which is based on the calculated realistic value for the MVDC/HVDC lines. Table 20 lists the specified line parameters and the ZCB parameters when the tripping time of ZCB is set to 10 μs with the base fault resistance ($R_{f\text{-}Base}$ = 5 Ω) which is same as the rated load resistance. The effect of cable line parameters to the cut-off performance of the ZCB in response to the faults is studied by designing and analysing the testing system in the MATLAB/Simulink environment.

Table 20. Specifications of ZCB and line parameters

Category	Parameters	Value	Remarks
Z-source breaker components	$C_0 = C_1 = C_2 = C_{ZCB}$	369 µF	Z-source Capacitors
	$L_1 = L_2 = L_{ZCB}$	76.9 µH	Z-source Inductors
Source and load parameters	V_S	5 kV	Source voltage
	P_L	5 MW	Load power
	R_L	5 Ω	Load resistance
	C_L	20.25 µF	Load capacitance
Cable line parameters	r	$3e^{-2}$ Ω km^{-1}	Line series resistance
	l	$1.05e^{-3}$ H km^{-1}	Line series inductance
	c	$11e^{-9}$ F km^{-1}	Line shunt capacitance
Fault branch	R_{f_Base}	5 Ω	Base fault resistance

5.3 Proposed Method for Determining the Cable Length Limit

The cable line consists of three elements (R_{Line}, L_{Line}, & C_{Line}) which has an influence in the ZCB's operation. As the "Γ" model of the power cable is considered, the L_{Line} can be directly combined with the L_2 for analyzing the ZCB's operation. However, since the value of L_2 calculated using [43, 57] is much larger than the value of L_{Line}, the effect of L_{Line} on accessing the CLL can be neglected in this study. Next, the effect of C_{Line} in the CLL assessment is investigated. The C_{Line} in parallel with the C_L value at the load side increases the overall the capacitance which effects the CLL of the line significantly, and thus, needs to be considered. The third element *i.e.,* R_{Line}, is connected in series with the fault circuit which attenuates the resonance of the LC circuit and contributes to the turning off of the SCR by supplying the reverse current. Thus, the effect of R_{Line}

must be included in the assessment of CLL. The method specified in [43] uses a third-order equation to evaluate the boundary values of Z-source parameters (C_0, C_1, & C_2). Now, considering the parameters of the power cable, the order of the equation increases to fourth order making it difficult to perform the CLL assessment mathematically by solving the higher order equations. Therefore, in general, the following steps can be followed to evaluate the CLL of a power cable:

Step 1: Calculate the parameters of ZCB using prior methods without considering the power cable's influence

Step 2: Build and simulate the physical model of the ZCB using a simulation tool (MATLAB/Simulink) and check the impact of cable length, fault resistance, and power delivery levels on the ZCB's turn off behavior

Step 3: Use the simulation results to find the CLL of the power cable.

5.4 ZCB Performance for Various Cable Lengths

A simulation testing system for the circuit connection of Fig. 5.1 is designed in the MATLAB/Simulink environment. The parameters of the ICC-BZCB and the line in the testing system are configured using the specifications acquired from Table 20. The simulated testing system is a "Γ" model power cable that is applied to the cable line as seen in Fig. 5.1. The ZCB's behaviors "With" two different cable lengths (*i.e.,* 65 m and 75 m) are compared to demonstrate the effect of cable line parameters on ZCB's cutoff performance. The ZCB is tested under three fault current levels for each cable length. The value of load current at prefault for the testing design is initially set to (I_L = 1.0 kA). The operation of ZCB for three cases of fault current level is studied as seen in Fig. 5.2 & Fig 5.3, respectively. The fault resistance in Case I is (R_f = 0.1 p.u.). Thus, the short-circuit fault which equals to the sum of fault from load (R_L) and fault resistance (R_f) in this case is equal to 11 p.u. *i.e.,* 10.0 p.u. from R_f and 1.0 p.u. from R_L. Likewise, Case II with a

fault resistance of (R_f = 0.5 p.u.), creates a fault current of 3.0 p.u. Finally, Case III shows a fault condition with (R_f = 1.0 p.u.) that causes a fault current of 2.0 p.u. (Fig. 5.3).

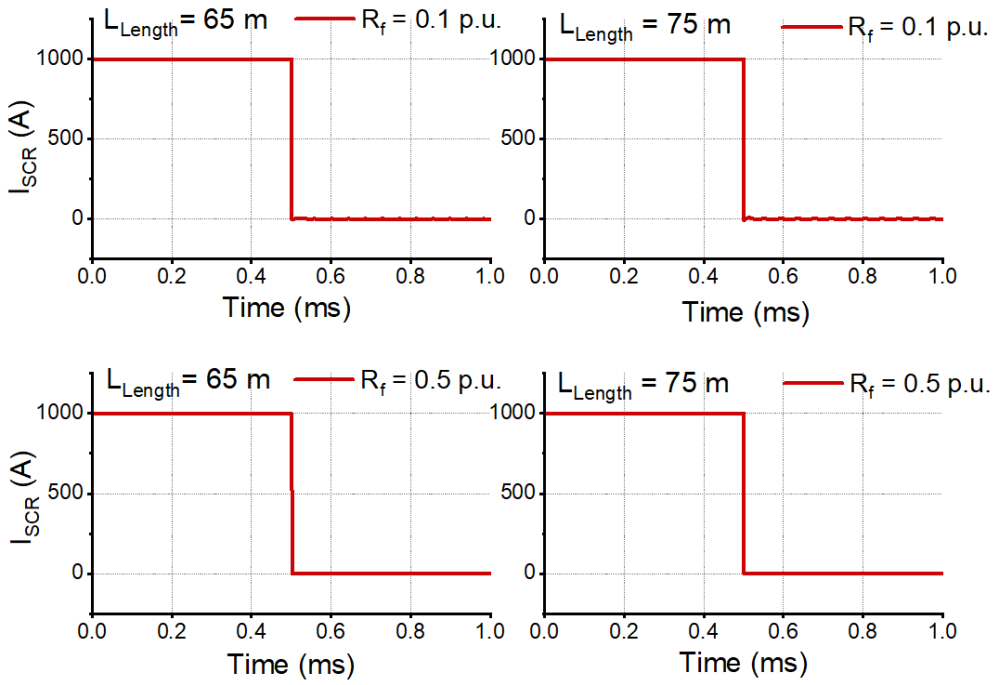


Figure 5.2 ZCB's performance under different fault current levels (R_f = 0.1 p.u. & R_f = 0.5 p.u.) and cable length limits (L_{Length} = 65 m & L_{Length} = 75 m)

The testing results shows that the ZCB independently responds to a high-level fault current in Case I & II and neglects the variance in cable length (no matter it is either 65 m or 75 m), as shown in Fig. 5.2. However, for Case III with R_f = 1.0 p.u., the ZCB only turns off for L_{Length} = 65 m whereas fails to cutoff fault current when the cable length is extended to 75 m as seen in Fig. 5.3. The key conclusions that can be drawn for this test results are:

(a) The performance of a ZCB is significantly impacted by the fault current level *i.e.*, for the same cable length consideration of (L_{Length} = 75m), the ZCB successfully turns off for R_f = 0.1 p.u. and 0.5 p.u. However, the fault current remains uncleared for R_f = 1.0 p.u.

(b) Likewise, the effectiveness of the ZCB in the DC transmission/distribution line is influenced by the length of the cable as observed in Fig. 5.3.

Therefore, to ensure the effective protection of ZCB in DC system protection, the cable length limit must be carefully studied. Sections 5.5 & 5.6 evaluates the cable length limit depending on fault levels and power delivery levels, respectively.

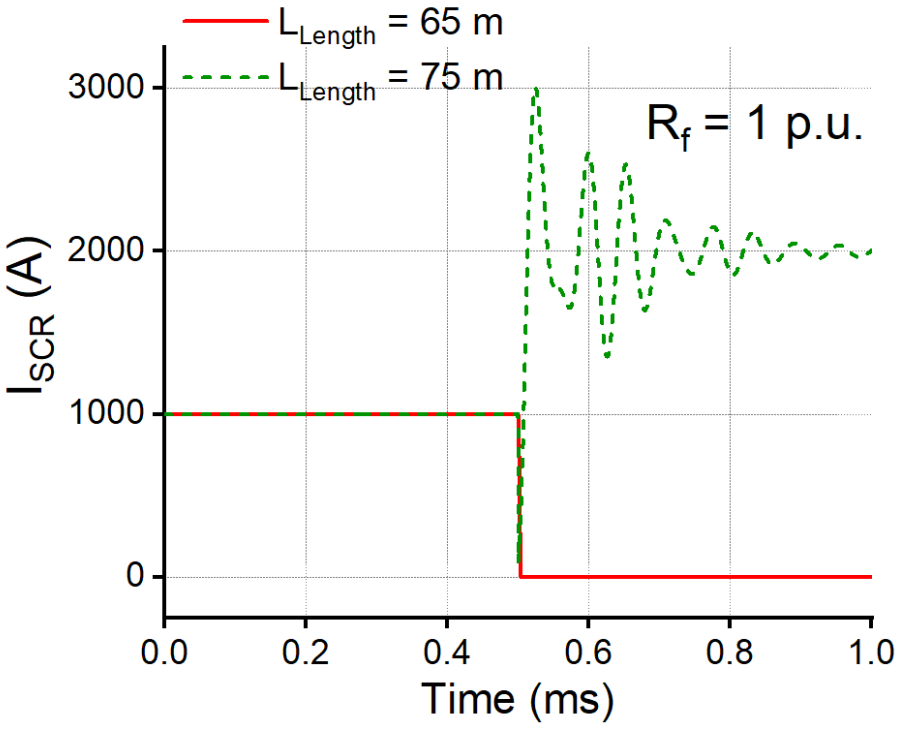


Figure 5.3 ZCB's performance for fault current level at R_f = 1.0 p.u. and cable length limits of L_{Length} = 65m & L_{Length} 75m, respectively

5.5 Cable Length Assessment Depending on Fault Levels

In this section, the Cable Length Limit is assessed under different fault levels. The cutoff behavior of the ZCB is studied with multiple sets of simulation tests for different cable length to detect the CLL under a certain fault level. The performance of ZCB for a fault level from 2.0 p.u. to 11.0 p.u. is analyzed. In this study, the realistic value of DC cable parameters given in Table 20 are used for the simulation analysis. The actual cable values are calculated using (27) as listed in Table 22. Some of the DC cables that are used in practice can be observed in Table 21 [46].

Table 21. Models and ratings of some DC cables

Model	Rated Power	Rated Voltage	Rated Current
Prysmian Group DC Power Cables (XLPE, P-Laser, MI-paper, and MI-PPL paper)	2,400 MW - 4,000 MW	525 kV- 800 kV	4.57 kA - 5.6 kA
Phoenix Contact DC Cables	2 kW - 200 kW	600 V - 1.0 kV	2 A - 200 A
Amphenol SINE Systems DC Power Cords	7.8 kW - 18 kW	600 V	13 A - 30 A
Molex Power Cables	3 kW - 40 kW	600 V - 1.0 kV	5 A - 40 A

The testing parameters of the simulation system and the estimated CLL for each fault level are listed in Table 22. The actual values of fault resistance, line resistance, and line inductance are calculated using (27) and (28), respectively, where R_{f_base}, r, l, & c are obtained from Table 20. For the CLL measurement, the performance of the ZCB is analyzed in simulation by gradually increasing the cable length from 0 until the length of ZCB that fails to cut-off the fault. During these tests, the ZCB parameters are kept unchanged. Fig. 5.4 demonstrates the effective and non-

effective zone for the ZCB under various fault levels. The results show that as the fault resistance increases, the effectiveness of the ZCB in terms of the cable length decreases gradually.

$$R_{f\_Actual} = R_{f\_Base} \times R_{f(p.u.)} \tag{27}$$

$$\begin{cases} R_{Line} = r \times L_L \\ C_{Line} = c \times L_L \\ L_{Line} = l \times L_L \end{cases} \tag{28}$$

Table 22. Summary of identified CLLs versus fault levels

R_f (in p.u.)	R_{f_Actual} (in Ω)	Cable Length Limit (L_L, in m)	Actual Line Parameters		
			R_{Line} (in Ω)	C_{Line} (in F)	L_{Line} (in H)
0.1	0.5	485	$14.55e^{-3}$	$5.335e^{-9}$	$5.1e^{-4}$
0.2	1	375	$11.25e^{-3}$	$4.125e^{-9}$	$3.94e^{-4}$
0.5	2.5	200	$6e^{-3}$	$2.2e^{-9}$	$2.1e^{-4}$
0.8	4	115	$3.45e^{-3}$	$1.265e^{-9}$	$1.21e^{-4}$
1	5	70	$2.1e^{-3}$	$0.77e^{-9}$	$0.735e^{-4}$

Therefore, in case of a high-level fault current (*i.e.*, a low fault resistance), the breaker can provide protection for a long distance whereas the protective distance reduces significantly for a low-level fault current (*i.e.*, a high fault resistance). Thus, the power system designer and operator must plan the cable length limit accordingly if he/she plans to protect the entire line for their expected fault levels. The relationship between CLL and R_{fault} is inversely proportional, *i.e.*, as the value of fault resistance increases, the effective CLL of the power cable reduces accordingly and vice versa as seen in Fig. 5.4. Hence, every high fault current in the cable can be protected if the

specified minimum fault current is secured within that certain cable due to their relatively-higher CLLs.

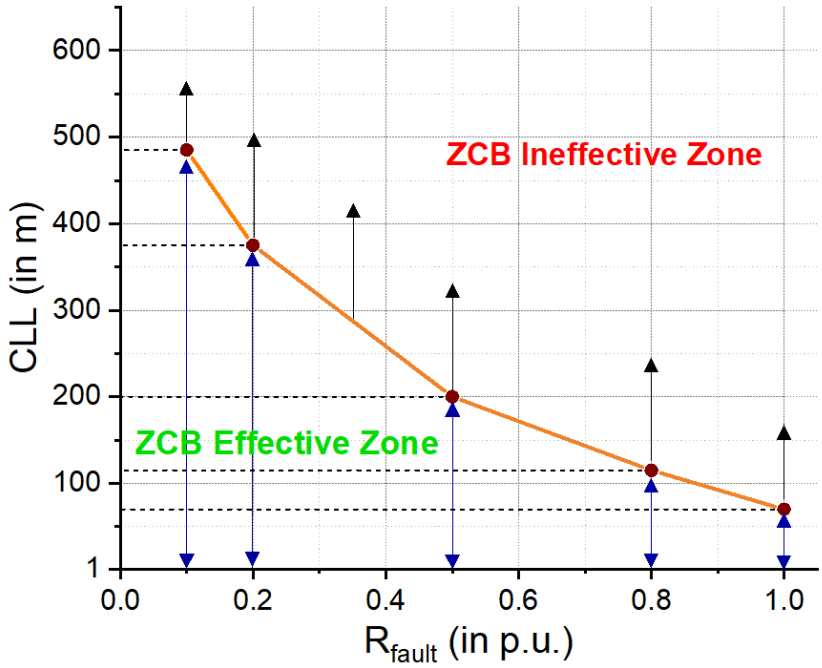


Figure 5.4 Summary of cable length limit related to various fault current levels

5.6 Cable Length Limit Assessment Depending on Power Delivery Levels

The variation in power delivery level in DC cables is used to further study the CLL in this section. The voltage in a DC network is constant which supplies multiple DC feeders with different power delivery level requirements depending on their load connections. The change in the CLL of a power cable with a changing power delivery level is still an open question. This study intends to determine the relationship between the CLL and the power delivery level by showing how the CLL is influenced by its power delivery level and finally, formulating a mathematical relationship between them.

5.6.1 Effective Protection for Various Power Delivery Conditions

In this section, the CLL is assessed by changing the power delivery level at the prefault condition. Two cases of variations in the load-power requirements and its effect on the CLL at prefault are studied. The locations of fault for successful tripping of ICC-BZCB are recorded in the DC lines. For both the cases, the voltage of the DC supply is fixed at V_s = 5.0 kV in the simulation system. Case I: the load-power is set at P_L = 75 kW, 100 kW, 500 kW, and 5.0 MW, respectively. Case II: the load power is varied in the range of 4.50 MW – 5.50 MW with an increment of 0.25 MW for each power delivery level.

A fault is emulated in the system using the fault branch consisting of a switch and a fault resistance (R_f), as seen in Fig. 5.1. The ZCB parameters calculated for both the cases using the parameter identification method given in Chapter 3 are listed in Table 23 & 24. The values of base fault resistances used for this study are also listed in Table 23. The actual value of fault resistance (R_{f_Actual}) is calculated using (27) which is expressed in per unit as R_f (in p.u.) in Fig. 5.5 & 5.6. The ZCB's behaviors are recorded and analyzed under different fault levels for each load-power prefault condition.

Table 23. Specification of ZCB parameters for Case I

Power Delivery Level (P_L)	**Load Current (I_L)**	**$C_0 = C_1 = C_2 = C_{ZCB}$**	**$L_1 = L_2 = L_{ZCB}$**	**R_{F_base}**
75 kW	15 A	5.54 μF	5.126 mH	333.33 Ω
100 kW	20 A	7.38 μF	3.85 mH	250.00 Ω
500 kW	100 A	36.9 μF	0.77 mH	50.00 Ω
5.0 MW	1000 A	369 μF	76.9 μH	5.00 Ω

Table 24. Specification of ZCB parameters for Case II

Load Power (P_L)	**$C_0 = C_1 = C_2 = C_{ZCB}$**	**$L_1 = L_2 = L_{ZCB}$**	**C_L**
4.5 MW	332.2 μF	85.44 μH	18.22 μF
4.75 MW	350.7 μF	80.95 μH	19.23 μF
5 MW	369.1 μF	76.89 μH	20.25 μF
5.25 MW	387.6 μF	73.23 μH	21.26 μF
5.5 MW	406.1 μF	69.91 μH	22.27 μF

The CLL curves are developed for both the cases of power delivery levels using the simulation results as shown in Fig. 5.5 and 5.6, respectively. Both the figures demonstrates a similar pattern in the cable length limit assessment. As the power delivery level increases the effective length of the ZCB reduces gradually. Each CLL curve represents the CLL points under various fault levels at that certain power delivery level. Table 25 and Table 26 lists the data of identified CLL points and related power delivery levels. The following conclusions can be drawn by observing the CLL curves and analyzing the data:

a) For a constant load, the effective protection of the breaker reduces as the value of R_f increases and vice versa. This is the same conclusion as in Section 5.5 which remains unchanged with the power delivery level.

b) For a constant R_f, the breaker is able to respond to the fault for a long distance in case of a lower load-power requirement and vice versa. In other words, lower the power delivery level higher is the CLL. Therefore, to maintain an effective protection of ZCB in DC networks for the long-distance, high-power condition, multi-line power delivery can be a solution to increase the CLL.

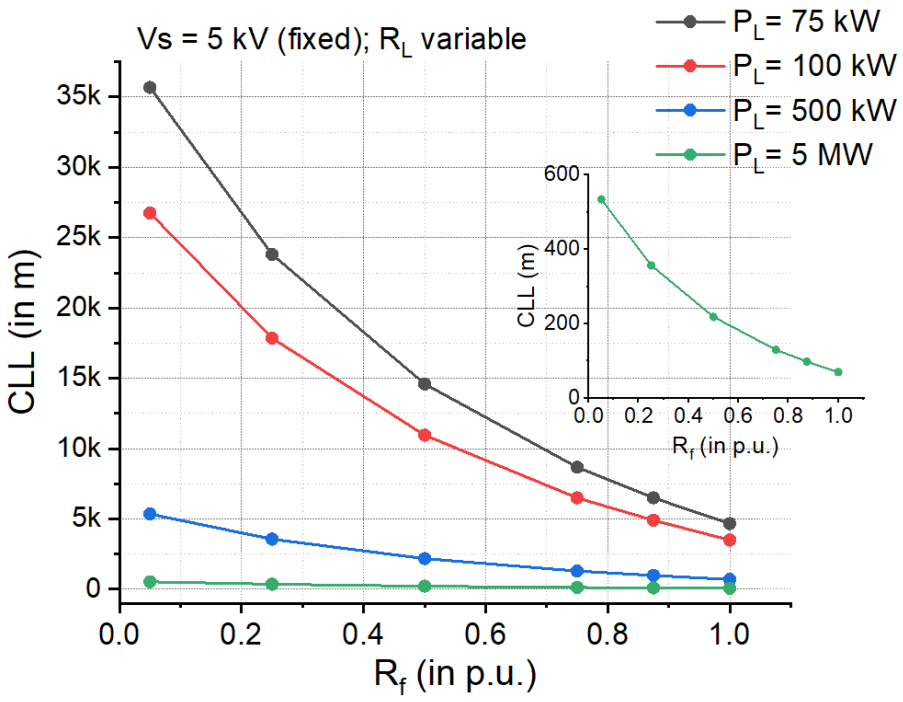


Figure 5.5 CLL curves for various load-power requirements (Case I)

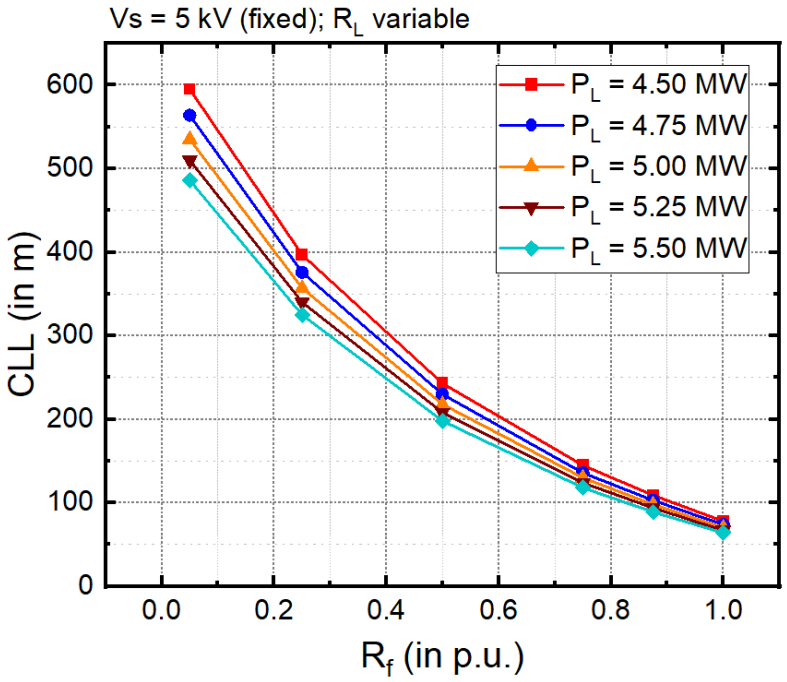


Figure 5.6 CLL curves for various load-power requirements (Case II)

Table 25. Identified CLLs versus power delivery levels (Case I)

R_F (p.u)	R_{F_Actual} (Ω)				Cable Length Limit (L_L in km)			
	75 kW	100 kW	500 kW	5 MW	75 kW	100 kW	500 kW	5 MW
0.05	16.67	12.50	2.50	0.25	35.67	26.75	5.35	0.535
0.25	83.33	62.50	12.50	1.25	23.80	17.85	3.57	0.357
0.5	166.67	125.00	25.00	2.5	14.54	10.90	2.18	0.218
0.75	250.00	187.50	37.50	3.75	8.67	6.50	1.30	0.130
0.875	291.67	218.75	43.75	4.37	6.53	4.90	0.98	0.098
1.0	333.33	250.00	50.00	5.00	4.67	3.50	0.70	0.070

Table 26. Identified CLLs versus power delivery levels (Case II)

R_F (p.u)	R_{F_Actual} (Ω)					Cable Length Limit (L_L in m)				
	4.50 MW	4.75 MW	5 MW	5.25 MW	5.50 MW	4.50 MW	4.75 MW	5 MW	5.25 MW	5.5 MW
0.05	0.28	0.26	0.25	0.24	0.23	595	564	535	510	486
0.25	1.39	1.32	1.25	1.19	1.14	397	376	357	340	325
0.50	2.78	2.63	2.5	2.38	2.27	243	230	218	208	198
0.75	4.16	3.95	3.75	3.57	3.40	145	136	130	124	118
0.87	4.86	4.61	4.37	4.17	3.98	109	103	98	94	89
1.00	5.55	5.26	5.00	4.76	4.55	78	74	70	67	64

5.6.2 CLL Curve Verification with a Case Study

The CLL curve of power delivery level can be derived mathematically by applying the curve-fitting technique to the CLL points in Fig. 5.5 & 5.6. Six simulation tests are performed by adding a short DC line (with a length of 10 km) between the ICC-BZCB model and the load of 75 kW in MATLAB/Simulink to verify the usefulness of CLL curves. The threshold value of a 10 km cable line is obtained using the CLL curve of 75 kW as 0.67* R_f in p.u. The responsiveness of ICC-BZCB to the six different R_f values are simulated.

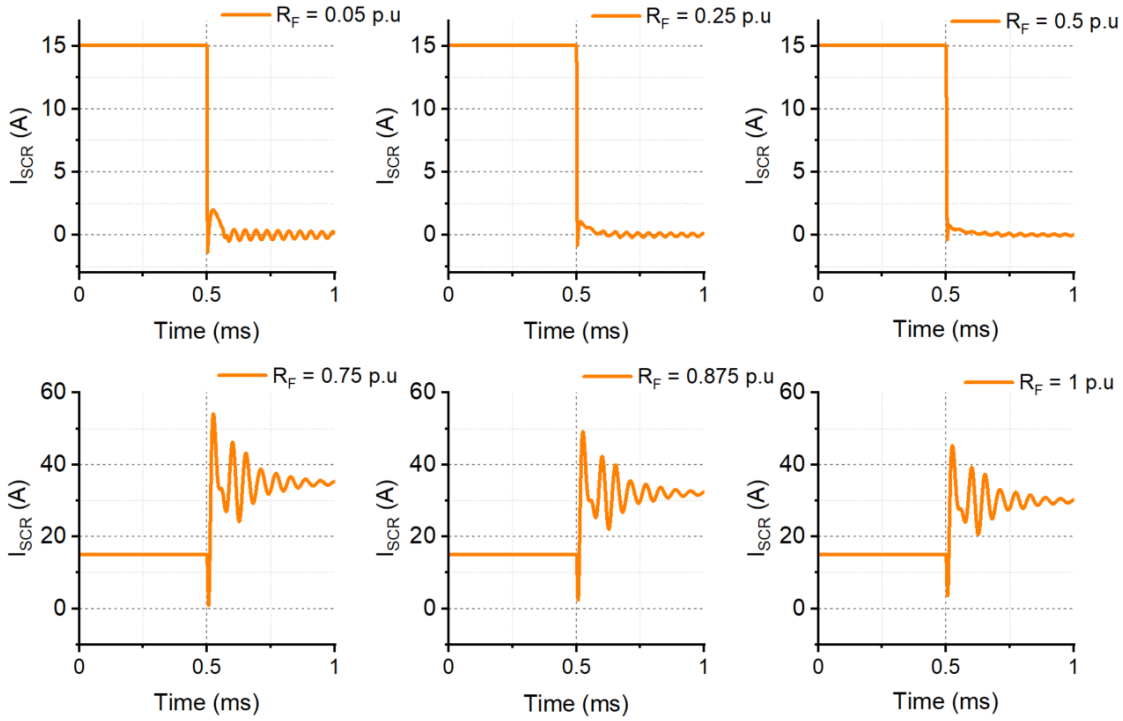


Figure 5.7 Simulation study of ICC-BZCB's effectiveness under various R_f values (10-km line)

The ZCB responds to all faults with fault resistance equal or less than the threshold of 0.67 p.u., *i.e.*, the breaker turns off for R_F = 0.05 * R_f (p.u.), 0.25 * R_f (p.u.), and 0.5 * R_f (p.u.), whereas the breaker losing its responsiveness when the magnitude of R_f increases beyond that threshold, as

seen in Fig. 5.7. Therefore, the derived CLL curves are valid to specify the cable line limits under a certain load condition and a specified minimum fault current to be cut-off. The evaluated and tested CLL curve can act as a base for other conditions and using the relation in (29) the CLL curves for the new conditions can be easily derived.

$$L_{L\_New} = \frac{P_{base}}{P_{New}} \times L_{L\_base} \tag{29}$$

In (29), L_{L_base} and P_{base} are the existing CLL point, and its related power delivery level, respectively; and L_{L_new} and P_{new} are the new CLL point and its related power delivery level, respectively. When the effective length of ZCB is measured and calculated for the base condition, all the other effective length curves can be generated conveniently using (29).

5.7 Summary

In this study, the cable length limit is assessed and determined to guarantee reliable DC-line protection from ZCB. The relationships of CLL to fault level and power delivery level have been derived. The two key conclusions drawn from this study are: a) the cable length limit decreases along with the decreasing fault current level; and b) the cable length limit decreases along with the increasing power delivery level. Therefore, the cable length must be limited within a certain range to ensure ZCB's turnoff behavior to a target fault level. Also, for long-distance protection of cable lines, the effective protection range of ZCBs can be extended by applying the multi-line power delivery approach. An equation of calculating the effective length of ZCB for DC lines is derived based on the relationship of CLL curves which can be used to generate new CLL curves for various load-power requirements. Power system designer/operator can use the derived CLL curves to maintain reliable protection with ZCBs in DC power system networks.

CHAPTER 6

CONCLUSION

Initially, the power loss analyses of three bi-directional Z-source circuit breakers are performed. Based on the calculations, it is found that the topology of ICC-BZCB has the least power loss during normal steady-state operation when there is a requirement of energizing the same load. A relationship between steady-state power loss and required tripping time for ZCB is studied based on the topology of ICC-BZCB. From the analysis, it is found that the voltages of the capacitors and inductors in ZCB increase along with source voltage, while the voltages of SCR and power diode remaining constant. The tripping time of SCR is a major parameter for evaluating overall power loss in the ZCB during normal steady-state operation when there is a requirement of energizing the same load. In general, for selection of an inductor, it can be concluded that as the permeability of the inductor increases, losses associated with it decreases. For a constant permeability, the required number of inductor windings increases with an increase in tripping time of SCR, which in turn increases overall power loss in the DC network.

A novel method of configuring Z-source capacitors is developed to ensure the turnoff of SCR in ICC-BZCB. The correction equation of Z-source capacitance is developed to accumulate enough negative SCR current for the depletion region buildup accurately and thus guarantee the success rate of ZCB in DC circuit protection. At the same time, the new method can preserve the required tripping time to improve the controllability of ZCB. The effectiveness of the method has been verified by the experiments on a hardware testbed. In addition, it has been found that the correction and adjustment of the Z-source capacitor has a negligible effect on ZCB's power delivery efficiency.

A new method is introduced to specify ZCBs to operate in either the HI-Mode for HIF interruption or the HD-Mode for HIF detection and reporting. The specification of ZCB is enabled by adjusting the Z-source capacitors properly. A mathematical relationship between the maximum HIF resistance and required Z-source capacitance has been derived and its effectiveness & general usage has been validated in two different DC systems: a low-power experimental testbed and a high-power resistive simulation system. The new method can detect/interrupt a HIF that is as small as 2 times its nominal rated current. This method is easy to be implemented in the modern power systems to enhance their controllability and reliability in protection.

Finally, an application of ICC-BZCB when implemented in the DC transmission/distribution line is studied. The cable length limit is assessed and determined to guarantee reliable DC-line protection from ZCB. The relationships of CLL to fault level and power delivery level has been derived. The research shows that as the cable length limit decreases, the fault current level decreases accordingly. Also, the cable length limit decreases along with the increasing power delivery level for long-distance protection of cable lines. The effective protection range of ZCBs can be extended by applying the multi-line power delivery approach. Various CLL curves are derived, which can be used by power system designer/operator to maintain reliable protection with ZCBs in DC power system networks.

Future Work

This research can be further extended for the system-level study of a Z-source circuit breaker by studying the coordination between the two ZCBs in a cable line. The study on the effectiveness of the ZCB can be extended for an even longer distance when implemented in the DC transmission/distribution lines. As we know, the power loss which is a key consideration for a ZCB design is mostly due to the presence of switching devices. Thus, further research on a more efficient ZCB topology with reduced number of components that can lower the breaker losses can be investigated. Also, the application of ZCB in hybrid AC-DC power systems can be examined.

REFERENCES

[1] R. H. Lasseter, "Microgrids," in *2002 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No. 02CH37309)*, 2002, vol. 1, pp. 305-308: IEEE.

[2] B. Lasseter, "Microgrids [distributed power generation]," in *2001 IEEE power engineering society winter meeting. Conference proceedings (Cat. No. 01CH37194)*, 2001, vol. 1, pp. 146-149: IEEE.

[3] K. A. Corzine and R. W. Ashton, "Structure and analysis of the Z-source MVDC breaker," in *Electric Ship Technologies Symposium (ESTS), 2011 IEEE*, 2011, pp. 334-338: IEEE.

[4] D. Boroyevich, I. Cvetkovic, R. Burgos, and D. Dong, "Intergrid: A future electronic energy network?," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 1, no. 3, pp. 127-138, 2013.

[5] S. Grillo, V. Musolino, L. Piegari, E. Tironi, and C. Tornelli, "DC islands in AC smart grids," *IEEE Transactions on Power Electronics,* vol. 29, no. 1, pp. 89-98, 2013.

[6] P. Cairoli and R. A. Dougal, "New Horizons in DC Shipboard Power Systems: New fault protection strategies are essential to the adoption of dc power systems," *IEEE Electrification Magazine,* vol. 1, no. 2, pp. 38-45, 2013.

[7] G. F. Reed, B. M. Grainger, A. R. Sparacino, and Z.-H. Mao, "Ship to grid: Medium-voltage DC concepts in theory and practice," *IEEE Power and Energy Magazine,* vol. 10, no. 6, pp. 70-79, 2012.

[8] Solar Power Events. Available: https://events.solar/midwest/smart-energy-microgrid-marketplace/

[9] H. Kim, "DC distribution systems and circuit breaking technology," *The Journal of the Korean Institute of Power Electronics,* vol. 15, no. 5, pp. 40-46, 2010.

[10] Y. Li, D. M. Vilathgamuwa, and P. C. Loh, "Design, analysis, and real-time testing of a controller for multibus microgrid system," *IEEE Transactions on power electronics,* vol. 19, no. 5, pp. 1195-1204, 2004.

[11] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400V DC distribution in telco and data centers to improve energy efficiency," in *INTELEC 07-29th International Telecommunications Energy Conference*, 2007, pp. 32-39: IEEE.

[12] *IEEE Recommended Practice for the Design of DC Power Systems for Stationary Applications," in IEEE Std 946-2020 (Revision of IEEE Std 946-2004) , vol., no., pp.1-74, 23 Sept,* 2020.

[13] M. Farhadi and O. A. Mohammed, "Event-based protection scheme for a multiterminal hybrid DC power system," *IEEE Transactions on Smart Grid,* vol. 6, no. 4, pp. 1658-1669, 2015.

[14] X. Feng, L. Qi, and Z. Wang, "Estimation of short circuit currents in mesh DC networks," in *2014 IEEE PES General Meeting| Conference & Exposition*, 2014, pp. 1-5: IEEE.

[15] B. Pauli, G. Mauthe, E. Ruoss, and G. Ecklin, "Development of a high current HVDC circuit brekaer with fast fault clearing capability," *IEEE Transactions on Power Delivery,* vol. 3, no. 4, 1988.

[16] T. An, G. Tang, and W. Wang, "Research and application on multi-terminal and DC grids based on VSC-HVDC technology in China," *High Voltage,* vol. 2, no. 1, pp. 1-10, 2017.

[17] H.-P. Kraemer *et al.*, "Test of a 1 kA superconducting fault current limiter for DC applications," *IEEE Transactions on applied superconductivity,* vol. 15, no. 2, pp. 1986-1989, 2005.

[18] D. Jovcic and B. Wu, "Fast fault current interruption on high-power DC networks," in *IEEE PES General Meeting*, 2010, pp. 1-6: IEEE.

[19] L. K. Mackey, "Ultrafast Direct Current Protection Systems for Faster Fault Isolation in Multi-terminal LVDC and MVDC Distribution," 2019.

[20] S. Xue, F. Gao, W. Sun, and B. Li, "Protection principle for a DC distribution system with a resistive superconductive fault current limiter," *Energies,* vol. 8, no. 6, pp. 4839-4852, 2015.

[21] L. Tang and B.-T. Ooi, "Protection of VSC-multi-terminal HVDC against DC faults," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No. 02CH37289)*, 2002, vol. 2, pp. 719-724: IEEE.

[22] J. Yang, J. E. Fletcher, and J. O'Reilly, "Multiterminal DC wind farm collection grid internal fault analysis and protection design," *IEEE transactions on power delivery*, vol. 25, no. 4, pp. 2308-2318, 2010.

[23] L. Tang and B.-T. Ooi, "Locating and isolating DC faults in multi-terminal DC systems," *IEEE transactions on power delivery*, vol. 22, no. 3, pp. 1877-1884, 2007.

[24] J.-M. Meyer and A. Rufer, "A DC hybrid circuit breaker with ultra-fast contact opening and integrated gate-commutated thyristors (IGCTs)," *IEEE Transactions on Power Delivery*, vol. 21, no. 2, pp. 646-651, 2006.

[25] D. M. Bui, S.-L. Chen, C.-H. Wu, K.-Y. Lien, C.-H. Huang, and K.-K. Jen, "Review on protection coordination strategies and development of an effective protection coordination system for DC microgrid," in *2014 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2014, pp. 1-10: IEEE.

[26] M. Hajian, L. Zhang, and D. Jovcic, "DC transmission grid with low-speed protection using mechanical DC circuit breakers," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1383-1391, 2014.

[27] S. Tokuyama, K. Arimatsu, Y. Yoshioka, Y. Kato, and K. Hirata, "Development and interrupting tests on 250kV 8kA HVDC circuit breaker," *IEEE Power Engineering Review*, no. 9, pp. 42-43, 1985.

[28] B. Pauli, G. Mauthe, E. Ruoss, and G. Ecklin, "Developmet of a high current HVDC circuit breaker with fast fault clearing capability," *IEEE Transactions on Power Delivery*, vol. 3, no. 4, 1988.

[29] T. Eriksson, M. Backman, and S. Halen, "A low loss mechanical HVDC breaker for HVDC grid applications," *Proc. Cigré Session, Paris, France*, 2014.

[30] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Modelling of high power mechanical DC circuit breaker," in *2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2015, pp. 1-5: IEEE.

[31] J.-D. Park and J. Candelaria, "Fault detection and isolation in low-voltage DC-bus microgrid system," *IEEE transactions on power delivery*, vol. 28, no. 2, pp. 779-787, 2013.

[32] A. Hassanpoor, J. Häfner, and B. Jacobson, "Technical assessment of load commutation switch in hybrid HVDC breaker," *IEEE Transactions on power electronics*, vol. 30, no. 10, pp. 5393-5400, 2014.

[33] K. Sano and M. Takasaki, "A surgeless solid-state DC circuit breaker for voltage-source-converter-based HVDC systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2690-2699, 2013.

[34] F. Liu, W. Liu, X. Zha, H. Yang, and K. Feng, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage DC microgrid," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3007-3021, 2016.

[35] H. Iwamoto, K. Satoh, M. Yamamoto, and A. Kawakami, "High-power semiconductor device: a symmetric gate commutated turn-off thyristor," *IEE Proceedings-Electric Power Applications*, vol. 148, no. 4, pp. 363-368, 2001.

[36] R. F. Schmerda, S. Krstic, E. L. Wellner, and A. R. Bendre, "IGCTs vs. IGBTs for circuit breakers in advanced ship electrical systems," in *2009 IEEE Electric Ship Technologies Symposium*, 2009, pp. 400-405: IEEE.

[37] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker," *ABB Grid Systems Technical Paper*, vol. 361, pp. 143-152, 2012.

[38] D. Döring, D. Ergin, K. Würflinger, J. Dorn, F. Schettler, and E. Spahic, "System integration aspects of DC circuit breakers," *IET Power Electronics*, vol. 9, no. 2, pp. 219-227, 2016.

[39] H. Polman, J. Ferreira, M. Kaanders, B. Evenblij, and P. Van Gelder, "Design of a bi-directional 600 V/6 kA ZVS hybrid DC switch using IGBTs," in *Conference Record of the*

2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No. 01CH37248), 2001, vol. 2, pp. 1052-1059: IEEE.

[40] D. Bösche, E.-D. Wilkening, H. Köpf, and M. Kurrat, "Hybrid DC circuit breaker feasibility study," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 3, pp. 354-362, 2016.

[41] S. Bhatta, Y. Zhang, and R. Fu, "Comparative Analysis of Power Loss Associated with Topology of Bi-Directional Z-Source Circuit Breakers," in *SoutheastCon 2018*, 2018, pp. 1-5: IEEE.

[42] S. Bhatta, R. Fu, and Y. Zhang, "A New Design of Z-source Capacitors to Ensure SCR's Turnoff for the Practical Applications of ZCBs in Realistic DC Network Protection," in *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2021.3063021.

[43] S. Bhatta, Y. Zhang, and R. Fu, "Relationship of Steady-State Power Loss and Configurable Tripping Time in Z-Source Circuit Breakers," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 3483-3489: IEEE.

[44] S. Bhatta, R. Fu, and Y. Zhang, "A New Method of Detecting and Interrupting High Impedance Faults by Specifying the Z-Source Breaker in DC Power Networks," *Electronics*, vol. 9, no. 10, p. 1654, 2020.

[45] S. Bhatta, Y. Zhang, and R. Fu, "Detecting High-Impedance Fault with Z-Source Circuit Breakers in Smart Grids," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1755-1761: IEEE.

[46] R. Fu, S. Bhatta, J. M. Keller, and Y. Zhang, "Assessment of Cable Length Limit for Effective Protection by Z-Source Circuit Breakers in DC Power Networks," *Electronics*, vol. 10, no. 2, p. 183, 2021.

[47] K. A. Corzine and R. W. Ashton, "A new Z-source DC circuit breaker," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2796-2804, 2012.

[48] A. Maqsood, A. Overstreet, and K. A. Corzine, "Modified Z-source DC circuit breaker topologies," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7394-7403, 2015.

[49] F. Z. Peng, "Z-Source Inverters," *Wiley Encyclopedia of Electrical and Electronics Engineering*, pp. 1-11, 1999.

[50] S. Bernet, "Recent developments of high power converters for industry and traction applications," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1102-1117, 2000.

[51] M. H. Rashid, *"Power Electronics: Circuits, Devices & Applications"*, 4th ed. Pearson, 2013.

[52] N. Mohan, *"Power Electronics: Converters, Applications, and Design"*, 3rd ed. Wiley, 2002.

[53] A. H. Chang, B. R. Sennett, A.-T. Avestruz, S. B. Leeb, and J. L. Kirtley, "Analysis and design of DC system protection using Z-source circuit breaker," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1036-1049, 2016.

[54] K. Corzine, "Dc micro grid protection with the z-source breaker," in *IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, pp. 2197-2204: IEEE.

[55] A. Overstreet, A. Maqsood, and K. Corzine, "Modified z-source dc circuit breaker topologies," in *2014 Clemson University Power Systems Conference*, 2014, pp. 1-6: IEEE.

[56] D. J. Ryan, H. D. Torresan, and B. Bahrani, "A Bi-Directional Series Z-Source Circuit Breaker," *IEEE Transactions on Power Electronics*, 2017.

[57] D. Keshavarzi, T. Ghanbari, and E. Farjah, "A Z-Source-Based Bidirectional DC Circuit Breaker With Fault Current Limitation and Interruption Capabilities," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6813-6822, 2017.

[58] A. Maqsood and K. Corzine, "The Z-source breaker for fault protection in ship power systems," in *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2014 International Symposium on*, 2014, pp. 307-312: IEEE.

[59] Y. Yang and C. Huang, "A Low-Loss Z-Source Circuit Breaker for LVDC Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.

[60] S. Savaliya and B. Fernandes, "Performance evaluation of a modified bi-directional z-source breaker," *IEEE Transactions on Industrial Electronics*, 2020.

[61] X. Diao, F. Liu, Y. Song, M. X. Y. Zhuang, W. Zhu, and X. Zha, "A New Efficient Bidirectional T-source Circuit Breaker for Flexible DC Distribution Networks," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.

[62] G. Byeon, T. Yoon, S. Oh, and G. Jang, "Energy management strategy of the DC distribution system in buildings using the EV service model," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1544-1554, 2013.

[63] S.-M. Chen, T.-J. Liang, and K.-R. Hu, "Design, analysis, and implementation of solar power optimizer for DC distribution system," *IEEE transactions on power electronics*, vol. 28, no. 4, pp. 1764-1772, 2013.

[64] M. Kempkes, I. Roth, and M. Gaudreau, "Solid-state circuit breakers for medium voltage DC power," in *Electric Ship Technologies Symposium (ESTS), 2011 IEEE*, 2011, pp. 254-257: IEEE.

[65] Magnetics. *MPP Toroids.* Available: https://www.mag-inc.com/Media/Magnetics/Datasheets/C055076A2.pdf

[66] Littlefuse Inc. *SCR 400V 6A TO220AB-L*. Available: littelfuse.com/~/media/electronics/datasheets/switching_thyristors/littelfuse_thyristor_sxx06xsx_sxx06x_datasheet.pdf.pdf

[67] Comchip Technology. *Diode GEN PURP 400V 6A P600*. Available: https://media.digikey.com/pdf/Data%20Sheets/Comchip%20PDFs/6A05-10-G.pdf

[68] Panasonic Electronic Components. *CAP FILM 2.2UF 5% 400VDC RADIAL*. Available: https://industrial.panasonic.com/ww/products/capacitors/film-capacitors/film-cap-electroequip/models/ECWF4225JL

[69] Panasonic Electronics Components. *CAP FILM 1.3UF 5% 400VDC RADIAL*. Available: https://industrial.panasonic.com/ww/products/capacitors/film-capacitors/film-cap-electroequip/models/ECWF4135JL

[70] Schurter Inc. *CIR BRKR THRM MAG 6A 360 VDC*. Available: https://us.schurter.com/bundles/snceschurter/epim/_ProdPool_/newDS/en/typ_AS168XDC2.pdf

[71] Schurter. *Cartridge Fuses SPT 5X20 10 A FUSE*. Available: https://www.mouser.com/datasheet/2/358/typ_SPT_5x20_Pigtail-1276004.pdf

[72] IXYS. *IGBT 650V 200A 830W TO247*. Available: https://www.littelfuse.com/~/media/electronics/datasheets/discrete_igbts/littelfuse_discrete_igbts_xpt_ixyh100n65c3_datasheet.pdf.pdf

[73] M. W. Aslam and N. A. Zaffar, "A novel bidirectional Z-source DC circuit breaker for DC microgrids," in *Power India International Conference (PIICON), 2016 IEEE 7th*, 2016, pp. 1-5: IEEE.

[74] C. L. Benner and B. D. Russell, "Practical high-impedance fault detection on distribution feeders," *IEEE Transactions on Industry Applications*, vol. 33, no. 3, pp. 635-640, 1997.

[75] H. Laaksonen and P. Hovila, "Method for high-impedance fault detection," *CIRED-Open Access Proceedings Journal*, vol. 2017, no. 1, pp. 1295-1299, 2017.

[76] M. Sedighizadeh, A. Rezazadeh, and N. I. Elkalashy, "Approaches in high impedance fault detection a chronological review," *Advances in Electrical and Computer Engineering*, vol. 10, no. 3, pp. 114-128, 2010.

[77] R. Das and D. Bayoumi, "System for detection of high impedance fault," in *19th International Conference on Electricity Distribution, Vienna, Austria*, 2007, pp. 0876-0880.

[78] Y. Sheng and S. M. Rovnyak, "Decision tree-based methodology for high impedance fault detection," *IEEE Transactions on Power Delivery*, vol. 19, no. 2, pp. 533-536, 2004.

[79] D. P. Gomes, C. Ozansoy, and A. Ulhaq, "High-sensitivity vegetation high-impedance fault detection based on signal's high-frequency contents," *IEEE Transactions on Power Delivery,* vol. 33, no. 3, pp. 1398-1407, 2018.

[80] W. Santos, F. Lopes, N. Brito, and B. Souza, "High-impedance fault identification on distribution networks," *IEEE Transactions on Power Delivery,* vol. 32, no. 1, pp. 23-32, 2016.

[81] J. Chen, T. Phung, T. Blackburn, E. Ambikairajah, and D. Zhang, "Detection of high impedance faults using current transformers for sensing and identification based on features extracted using wavelet transform," *IET generation, transmission & distribution,* vol. 10, no. 12, pp. 2990-2998, 2016.

[82] F. L. Vieira, M. José Filho, P. M. Silveira, C. A. Guerrero, and M. P. Leite, "High impedance fault detection and location in distribution networks using smart meters," in *2018 18th International Conference on Harmonics and Quality of Power (ICHQP)*, 2018, pp. 1-6: IEEE.

[83] É. M. Lima, C. M. dos Santos Junqueira, N. S. D. Brito, B. A. de Souza, R. de Almeida Coelho, and H. G. M. S. de Medeiros, "High impedance fault detection method based on the short-time Fourier transform," *IET Generation, Transmission & Distribution,* vol. 12, no. 11, pp. 2577-2584, 2018.

[84] B. Wang, J. Geng, and X. Dong, "High-Impedance Fault Detection Based on Nonlinear Voltage–Current Characteristic Profile Identification," *IEEE Transactions on Smart Grid,* vol. 9, no. 4, pp. 3783-3791, 2016.

[85] J. T. A. Vianna, L. R. Araujo, and D. R. R. Penido, "High impedance fault area location in distribution systems based on current zero sequence component," *IEEE Latin America Transactions,* vol. 14, no. 2, pp. 759-766, 2016.

[86] A. M. Pasdar, Y. Sozer, and I. Husain, "Detecting and locating faulty nodes in smart grids based on high frequency signal injection," *IEEE transactions on Smart Grid,* vol. 4, no. 2, pp. 1067-1075, 2013.

[87] G. de Alvarenga Ferreira and T. M. L. Assis, "A Novel High Impedance Arcing Fault Detection Based on the Discrete Wavelet Transform for Smart Distribution Grids," in *2019 IEEE PES Innovative Smart Grid Technologies Conference-Latin America (ISGT Latin America)*, 2019, pp. 1-6: IEEE.

[88] F. Kong, Z. Hao, S. Zhang, and B. Zhang, "A novel traveling wave based main protection scheme for bipolar 800 kV UHVDC bipolar transmission lines," *IEEE Trans. Power Delivery,* vol. 29, no. 5, pp. 2270-2278, 2016.

[89] F. D. Marvasti and A. Mirzaei, "A novel method of combined DC and harmonic overcurrent protection for rectifier converters of monopolar HVDC systems," *IEEE Transactions on Power Delivery,* vol. 33, no. 2, pp. 892-900, 2017.

[90] Z.-Y. He, K. Liao, X.-P. Li, S. Lin, J.-W. Yang, and R.-K. Mai, "Natural frequency-based line fault location in HVDC lines," *IEEE transactions on power delivery,* vol. 29, no. 2, pp. 851-859, 2013.

[91] J. Suonan, S. Gao, G. Song, Z. Jiao, and X. Kang, "A novel fault-location method for HVDC transmission lines," *IEEE transactions on power delivery*, vol. 25, no. 2, pp. 1203-1209, 2009.

[92] J. P. Triveno, V. P. Dardengo, and M. C. de Almeida, "An approach to fault location in HVDC lines using mathematical morphology," in *2015 IEEE Power & Energy Society General Meeting*, 2015, pp. 1-5: IEEE.

[93] X. Feng, L. Qi, and J. Pan, "A novel fault location method and algorithm for DC distribution protection," *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 1834-1840, 2017.

[94] K. Liao, Z. He, and X. Li, "A fault location method based on traveling wave natural frequency used on±800kV UHVDC transmission lines," in *2011 International Conference on Electrical and Control Engineering*, 2011, pp. 5652-5655: IEEE.

[95] D. Tzelepis *et al.*, "Advanced fault location in MTDC networks utilising optically-multiplexed current measurements and machine learning approach," *International Journal of Electrical Power & Energy Systems*, vol. 97, pp. 319-333, 2018.

[96] J. He, M. Zhang, G. Luo, B. Yu, and Z. Hong, "A fault location method for flexible DC distribution network based on fault transient process," *Power Syst. Technol.*, vol. 41, no. 3, pp. 985-992, 2017.

[97] D. Tzelepis, G. Fusiek, A. Dyśko, P. Niewczas, C. Booth, and X. Dong, "Novel fault location in MTDC grids with non-homogeneous transmission lines utilizing distributed current sensing technology," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 5432-5443, 2018.

[98] C. Zhang, G. Song, T. Wang, and L. Yang, "Single-ended traveling wave fault location method in DC transmission line based on wave front information," *IEEE Transactions on Power Delivery*, vol. 34, no. 5, pp. 2028-2038, 2019.

[99] Z. He, J. Zhang, W.-h. Li, and X. Lin, "Improved fault-location system for railway distribution system using superimposed signal," *IEEE transactions on power delivery*, vol. 25, no. 3, pp. 1899-1911, 2010.

[100] B. Yong, C. Wei, L. Jiansheng, D. Lei, L. Qingdong, and Y. Ning, "Single phase to earth fault location method in distribution network based on signal injection principle," in *2011 4th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)*, 2011, pp. 204-208: IEEE.

[101] P. Gale, P. Taylor, P. Naidoo, C. Hitchin, and D. Clowes, "Travelling wave fault locator experience on Eskom's transmission network," 2001.

[102] P. K. Kalra, "Fault diagnosis for an HVDC system: A feasibility study of an expert system application," *Electric power systems research*, vol. 14, no. 2, pp. 83-89, 1988.

[103] Y. Yang, C. Huang, and Q. Xu, "A fault location method suitable for low-voltage DC line," *IEEE Transactions on Power Delivery*, vol. 35, no. 1, pp. 194-204, 2019.

[104] C. Li, A. M. Gole, and C. Zhao, "A fast DC fault detection method using DC reactor voltages in HVdc grids," *IEEE Transactions on Power Delivery,* vol. 33, no. 5, pp. 2254-2264, 2018.

[105] Y. Yang, C. Huang, Z. Zhao, Q. Xu, and Y. Jiang, "A New Bidirectional DC Circuit Breaker with Fault Decision-Making Capability for DC Microgrid," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* 2020.

[106] L. Teppoz, "Commande d'un système de conversion de type VSC-HVDC. Stabilité-Contrôle des perturbations," 2005.

[107] J. Sabatier, T. Youssef, and M. Pellet, "An HVDC line parameters estimation method without optimization," *International Journal of Electrical Power & Energy Systems,* vol. 83, pp. 541-546, 2016.

APPENDIX A

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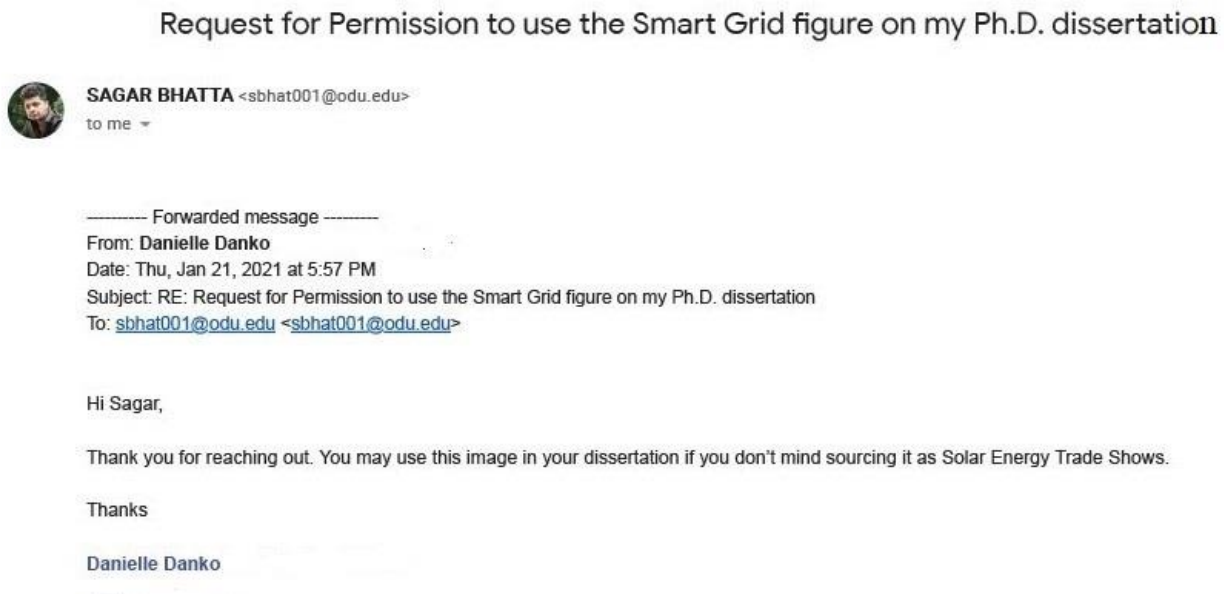

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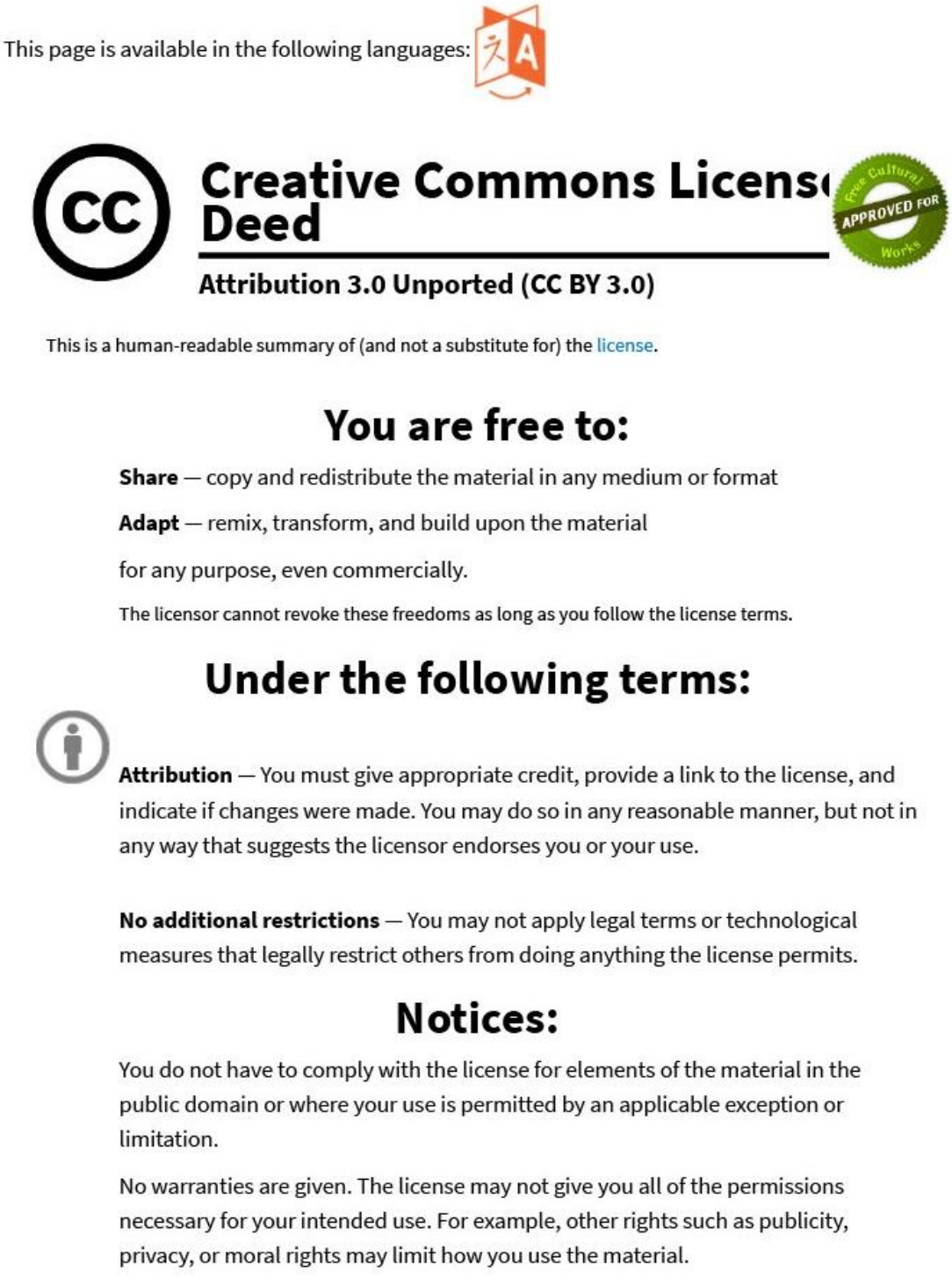

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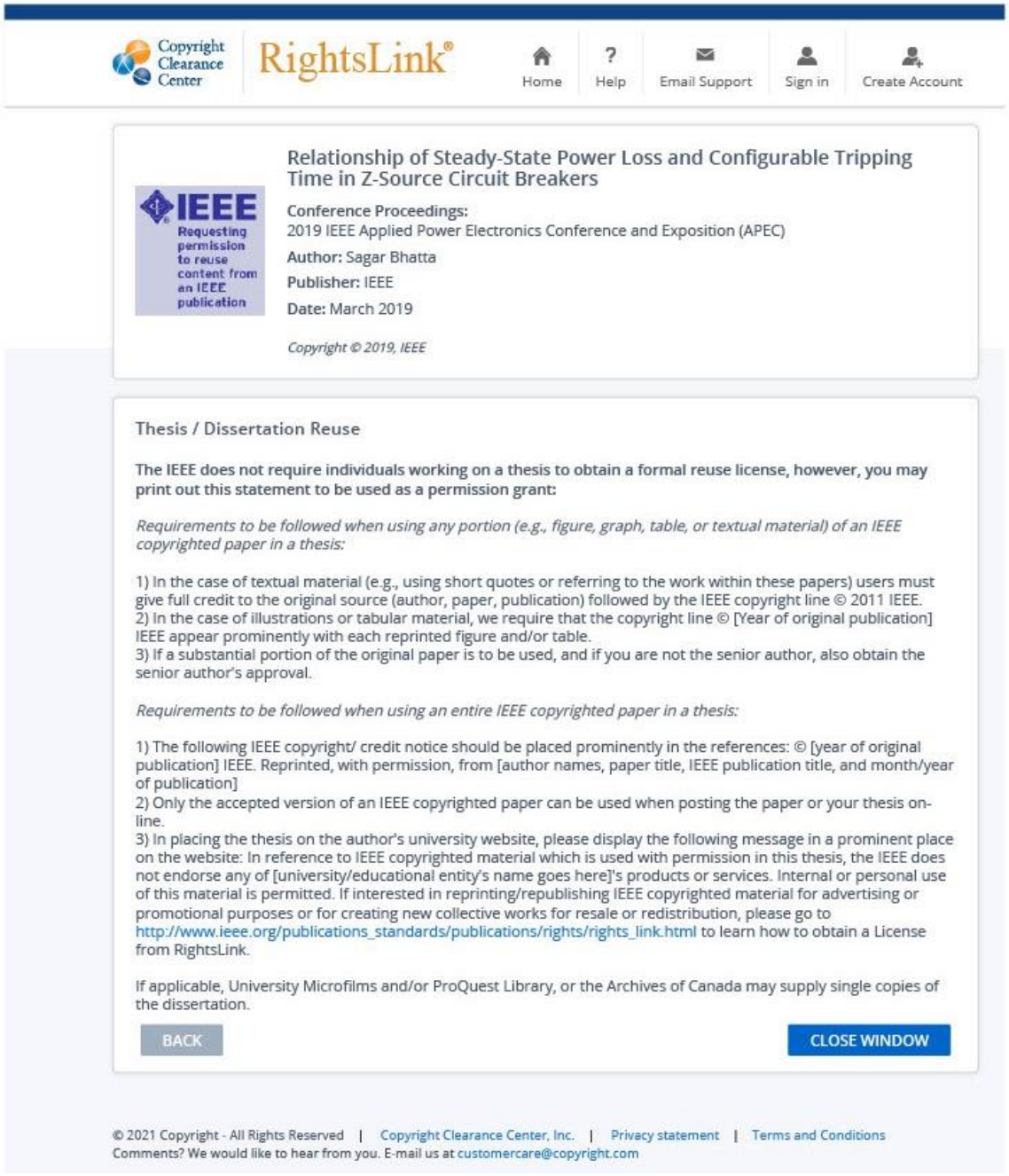

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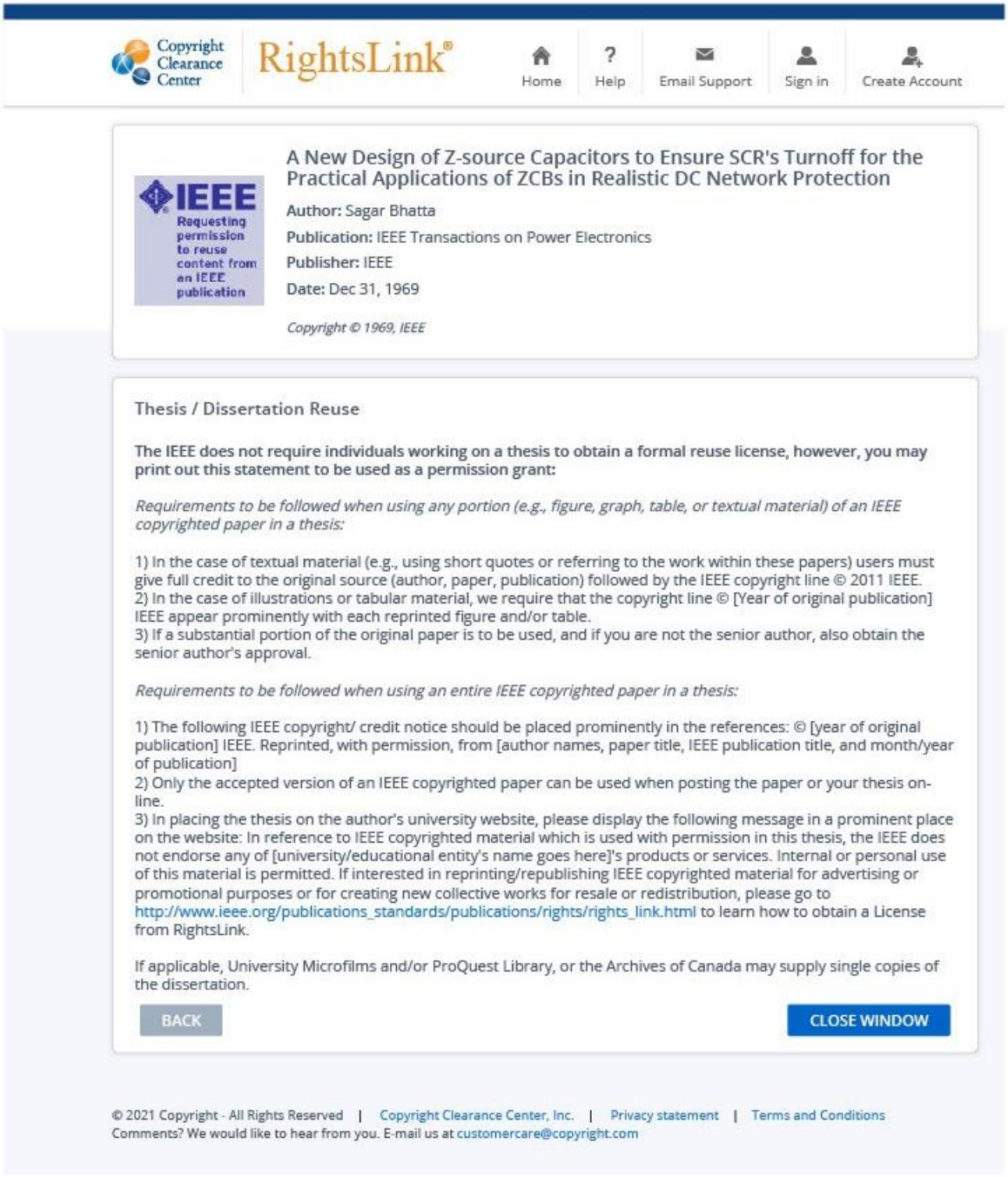

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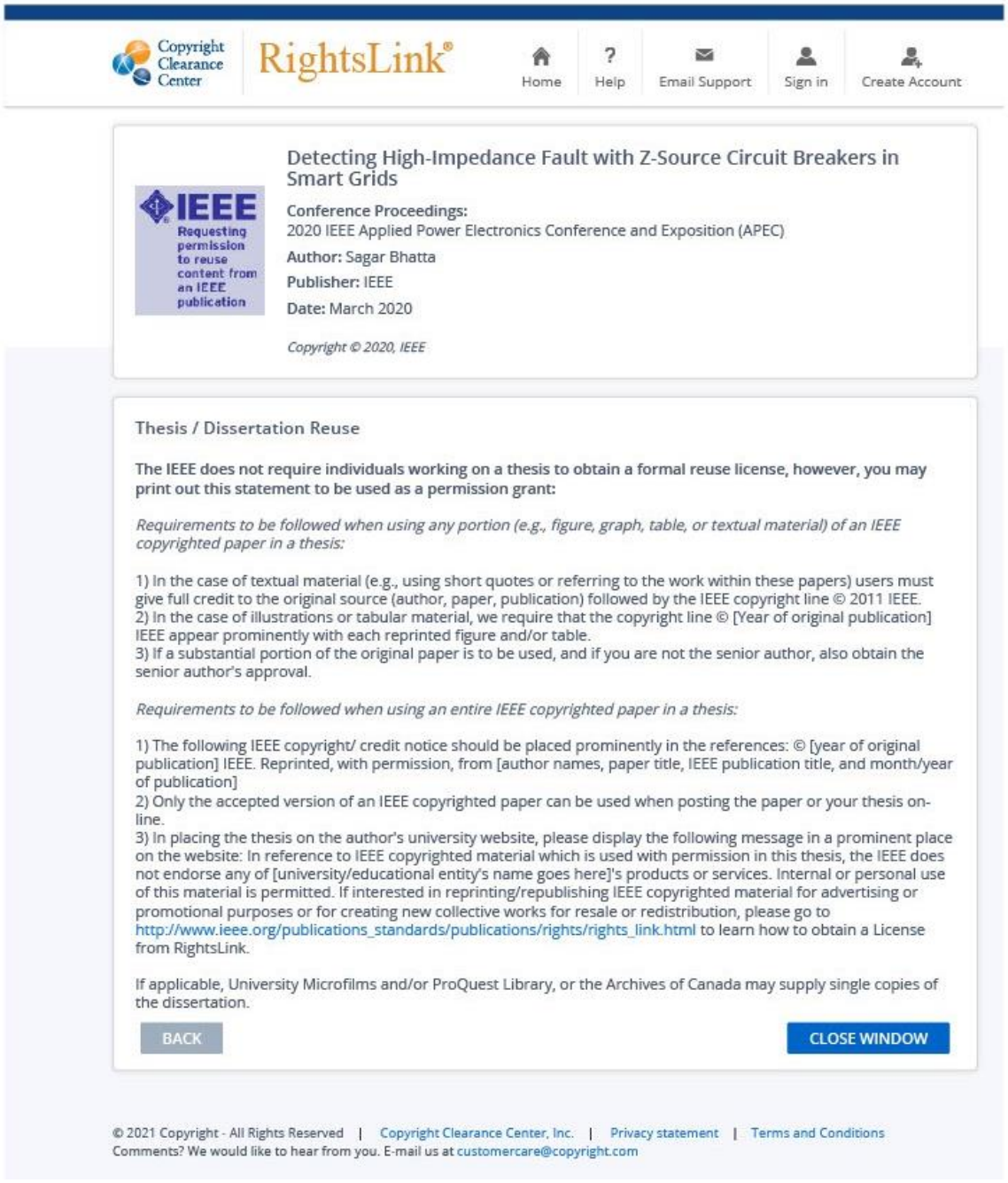

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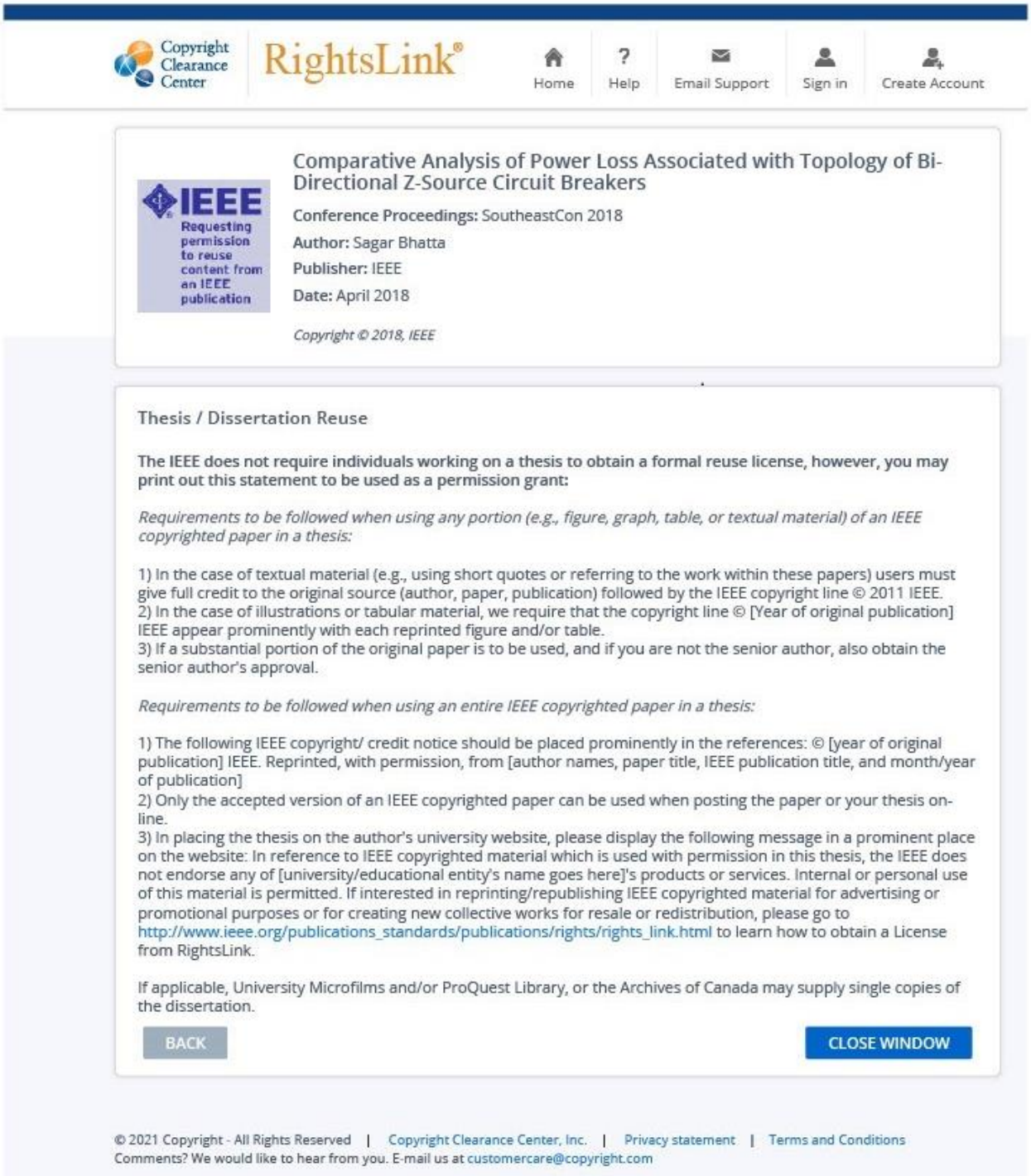

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- S. Bhatta, Y. Zhang, and R. Fu, "Detecting High-Impedance Fault with Z-Source Circuit Breakers in Smart Grids," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1755-1761: IEEE.
- S. Bhatta, Y. Zhang, and R. Fu, "Relationship of Steady-State Power Loss and Configurable Tripping Time in Z-Source Circuit Breakers," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 3483-3489: IEEE.
- S. Bhatta, Y. Zhang, and R. Fu, "Comparative Analysis of Power Loss Associated with Topology of Bi-Directional Z-Source Circuit Breakers," in *SoutheastCon 2018*, 2018, pp. 1-5: IEEE.