Design of a Power Management Circuit for an Opto-Electro Stimulator

***Abstract*—This paper presents the design of an integrated power management circuit for use in an implantable opto-electro stimulator. It features an active rectifier with pulse width modulation (PWM) regulation to generate a 3.3 V regulated output, and a 3-stage high voltage charge pump that generates a 12 V output from a 3.3 V input with a 20 MHz, two-phase non-overlapping clock generator. The circuits were designed in a 0.18-μm CMOS technology requiring a chip area of 0.048 mm^2. Simulation results show that the regulating rectifier has a voltage conversion efficiency of 94.3% and 92.8% with an input of 3.5 V and 3.6 V, respectively. The peak power transfer efficiency for a regulated output voltage of 3.3 V is 70.7% with an output power range of 30.3 mW. The charge pump overall capacitance is 60 pF.**

Keywords*—Active rectifier, charge pump, integrated circuits, optogenetics, power management.

I. Introduction

Deficiencies in the peripheral nervous system can result in various neurological disorders. One example is motor neurone disease (MND), which results in a loss of the motor neurons that control the skeletal muscle activities. There are currently no therapies to delay or reverse MND, making the disease fatal [1]. Current research aims to regenerate the damaged motor nerve using stem cell-derived motor neurons. Before the muscle atrophy occurs, and the paralysis becomes irreversible, the stem cell motor neurons must be engrafted close to the targeted muscles to ensure muscle reinnervation [2]. The nerves grow at a slow rate of around ~ 1 mm/day; therefore, reconnecting the motor neural circuits to the central neural system is challenging. A recent study suggests using optical stimulation to control muscle contraction after the muscles are innervated with the light-sensitive ion channel channelrhodopsin-2 (ChR2) on genetically modified, engrafted stem cell motor neurons [3]. This multidisciplinary research combines electronics, optogenetics and stem cell technologies to treat muscle paralysis caused by MND.

Implantable medical devices (IMDs) require an adequate power source. The use of batteries in implants has limitations, including a limited lifetime, requiring periodic replacement with the complications of surgery. Although rechargeable batteries are quite common in implants, their large size causes a limitation on the device miniaturization. Inductive wireless coupling has been widely used [4]-[6]. In the conventional two-step ac-dc conversion, an active rectifier followed by a dc regulator is used to convert the wirelessly transmitted ac signal to a regulated dc voltage supply. The power conversion efficiency (PCE) and voltage conversion efficiency (VCE) should be maximized to avoid reaching the specified human tissue specific absorption rate (SAR), also obtaining a high overall system efficiency [4]. An active rectifier with high-speed comparators has been proposed to boost the output voltage whenever it is low [5]. The output of such rectifiers tends to peak to the input voltage regardless of the required output voltage supply. Combining rectification and regulation into one stage can improve the overall efficiency, decrease the chip size, and better control the output voltage [6].

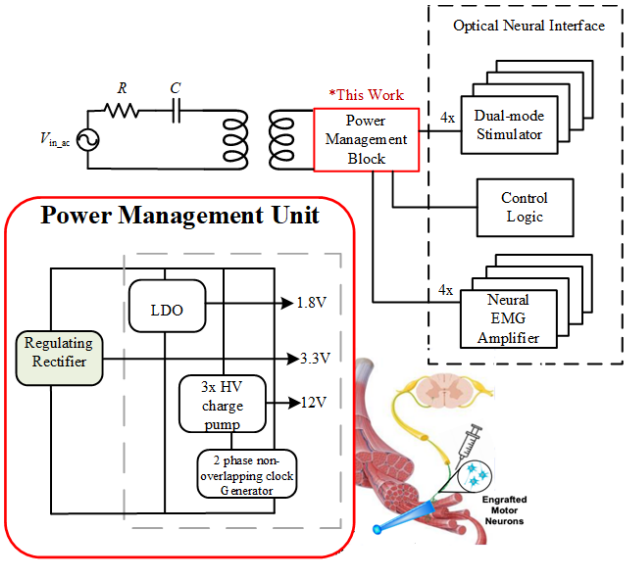

Fig. 1. Power management unit of a multi-channel opto-electro stimulator for treating motor neurone disease.

This paper focuses on the design of an active regulating rectifier, a three-stage high voltage (HV) charge pump, and the two phase non-overlapping clock generator for an opto-electro stimulator. The design also includes a dynamically body biased high speed comparator with a novel configuration of the pulse width modulation (PWM) regulation that is designed for an optical neural interface to improve the overall system efficiency and decrease the total area. The remainder of this paper is organized as follows. Section II describes the active rectifier incorporating a pulse width modulation (PWM) regulating architecture, the high-speed comparator, the design of the three-stage HV charge pump, and the design of a 20 MHz oscillator. Section III presents the simulated performance of the power management circuit. Conclusions are drawn in Section IV.

II. System Overview

The architecture of the power management circuit is shown in Fig.1. It comprises a regulating rectifier, low dropout regulator (LDO) [10], HV charge pump, and a two-phase non-overlapping clock generator to generate outputs of 1.8 V, 3.3 V and 12 V to power the other implant circuits (dual mode stimulator, control logic, and neural electromyography (EMG) amplifier).

A. Regulating Rectifier Architecture

As shown in Fig. 2. the active rectifier has an input voltage of V_{in_ac} which is the difference between V_+ and V_-. The pair of multiplexers are connected to the gates of the two pMOS ($MRP1$ and $MRP2$) selecting to drive either the high-speed comparator ($COM1$ and $COM2$) or the input voltage (V_+ or V_-) depending on the output of the PWM controller. The comparators ($COM1$ and $COM2$) drive the cross-coupled nMOS ($MRN1$ and $MRN2$) via the inverters. A dynamic body

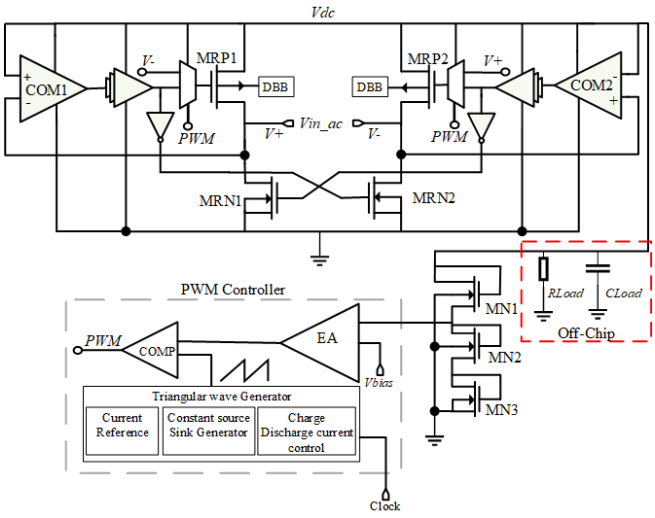

Fig. 2. Regulating rectifier with PWM Controller including the off-chip resistor and capacitor.

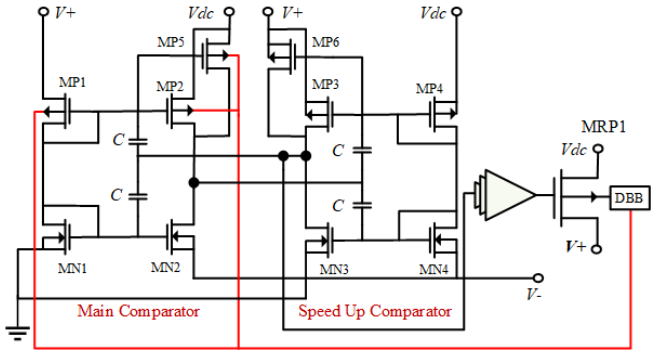

Fig. 3. Proposed high-speed comparator with body biasing technique to the pMOS of the main comparator.

biased (DBB) control technique [11] was implemented on the power transistors of the active rectifier to automatically connect to the highest potential between the input voltages (V_+ and $V\_$), and the output voltage, V_{dc} to avoid latch up.

For regulation, a PWM controller alters the duty cycle based on the error between the set voltage V_{bias} and the measured output Voltage, V_{dc} that is very nearly equal to the desired value. The voltage output is connected to three diode connected transistors ($MN1$, $MN2$, and $MN3$) that are used for the PWM controller and also an off chip resistor load, R_{Load}, is added for simulations. The design also includes a C_{Load} of 3 nF off-chip filter capacitor to reduce the ripple of V_{dc}. Apart from maintaining the regulation, it is desirable to retain the power losses especially in implantable applications which require high efficiency. PWM can offer accurate regulation of the output voltage to keep it in the required range at the desirable range of 3.3 V. The error amplifier (EA), a comparator ($COMP$), and the triangle wave generator are included in the PWM Controller as shown in Fig. 2. The triangle wave generator consists of a current reference, constant source/sink current generator, and a charge discharge current control. The triangle wave generator output can be inputted into comparator ($COMP$) with the output of the error amplifier to generate the PWM signal. In the design, when PWM = Logic 0 the gate of $MRP1$ and $MRP2$ are connected to positive or negative rails (V_+ or $V\_$). When PWM = Logic 1, they are connected to the comparators ($COM1$ and $COM2$).

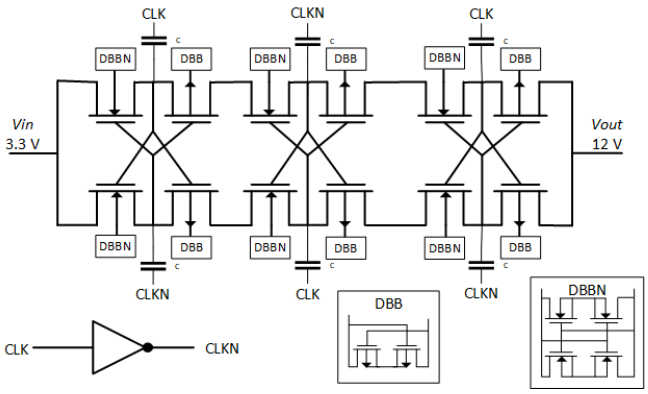

Fig. 4. Proposed latch design of three stage charge pump with body biasing of both nMOS and pMOS transistors.

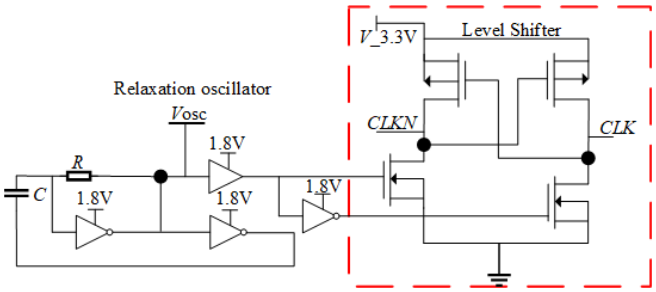

Fig. 5. Oscillator with level shifter to generate 20 MHz CLKN and CLK.

B. *Proposed High Speed Comparator Design*

In Fig. 2. the comparators ($COM1$ and $COM2$) design is shown in Fig. 3. Consisting of both a main comparator and a high-speed comparator. The comparator compares the two inputs V_{dc}, which is the regulated voltage output, and the two rail voltage inputs (V_+ and $V\_$). The cross-coupled comparator arrangement [5] improved the rectifier's efficiency, the conduction time of the active diodes in the rectifier, and decreases the reverse leakage current. The body terminals of transistors $MP1$, $MP2$, and $MP5$ in the main comparator are dynamically biased with the rectifier power transistor to avoid body effect and decrease the reverse current. This technique can enhance the performance of the comparators.

C. *Three Stage Charge Pump Architecture*

A widely used charge pump topology to generate boosted voltage is the Dickson charge pump with diode-connected CMOS transistors [9]. However, it suffers from a voltage drop equal to the threshold voltage in order to operate in the forward biased region. It also suffers from an increase in the threshold voltage that is caused by the body effect, which can degrade the pumping efficiency. The latch charge pump from [10] was adopted to ensure highly efficient pumping operation and to minimize the voltage drop in the charge. Existing stimulators use a large capacitor of 1 μF implemented by off-chip flying capacitors that are switching at a low frequency of 100 kHz, which can take up more silicon area than the stimulator itself [11]. The number of stages in the charge pump can be decided using the current consumption minimization strategy [12]. As a result, a three-stage charge pump as shown in Fig. 4 is used to boost the 3.3 V generated by the active regulating rectifier to produce 12 V output voltage. The respective body terminals of the switches are dynamically biased to make sure the substrate and n-well are

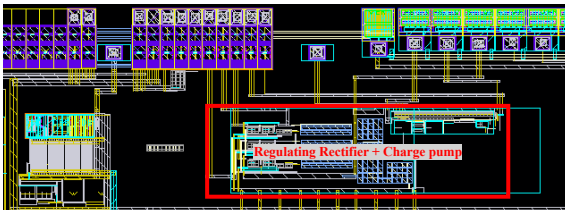

Fig. 6. The chip layout of the regulating rectifier and the charge pump.

always connected to the correct voltage during operation [11]. The implemented switches use deep n-well nMOS transistor and has two pairs of dynamic body bias to make sure that its substrate and n-well are always connected to the correct terminal. In Fig. 5, a 20 MHz oscillator is adopted containing a relaxation oscillator feedback loop that is under 1.8 V [13], and a level shifter at 3.3 V.

III. Simulated Results

The circuit layout is shown in Fig. 6. It includes the regulating rectifier, charge pump, and the LDO within an area of 0.048 mm^2.

A. Regulating Rectifier

The simulated results were carried out with a 13.56 MHz input frequency with an output load of R_{Load}= 0.33 kΩ and C_{Load}= 3 nF capacitor. Fig. 7 shows the rectified dc output V_{dc} = 3.3 V when V_{in_ac} is 3.5 V and 3.6 V. It also shows the output of the error amplifier that helps in creating the PWM controller signal for regulation. The maximum voltage conversion efficiency (VCE) obtained is around 94.3% when the input is 3.5 V and 92.8% when the input is 3.6 V. The VCE is defined as

$$\eta_{Voltage} = \frac{V_{dc}}{\max(|V_{in\_ac}|)} \quad (1)$$

and PCE is defined as

$$\eta_{Power} = \frac{P_{out\_dc}}{P_{in\_ac}} = \frac{P_{Load}}{P_{Load}+P_{Loss,total}} \quad (2)$$

The output power is calculated by taking the average output dc power, P_{out_dc} divide it by the P_{in_ac}, which is the integration of the product of the differential voltage, V_{in_ac}, across the ac source, and the current of the source. Where P_{Load} is the output power, and $P_{Loss,total}$, includes the charging and discharging power consumption, the comparators (COM1, COM2, and COMP), error amplifier, and the PWM controller. The peak measured PCE is 70.7%, and it is achieved at an input dc voltage of 3.5 V. It is crucial to optimize the size of the transistors considering the power consumption. The optimal size ratio of the pMOS and nMOS transistors proven in [14] can be found from

$$\left(\frac{W_p}{W_n}\right)_{opt} = \sqrt{\frac{K_n(V_{dc}-V_{ThN})}{K_p(V_{dc}-|V_{ThP}|)}} \quad (3)$$

The width of both pMOS, W_p, and nMOS, W_n, are optimized. K_p and K_n are the pMOS and nMOS transconductances, respectively. Having larger transistors decreases the R_{on} loss, however, it increases the switching loss and comparator delays. In [15], the input frequency, f_{input}, is minimized to 2 MHz to obtain a high PCE, however, the design still suffers from a low VCE.

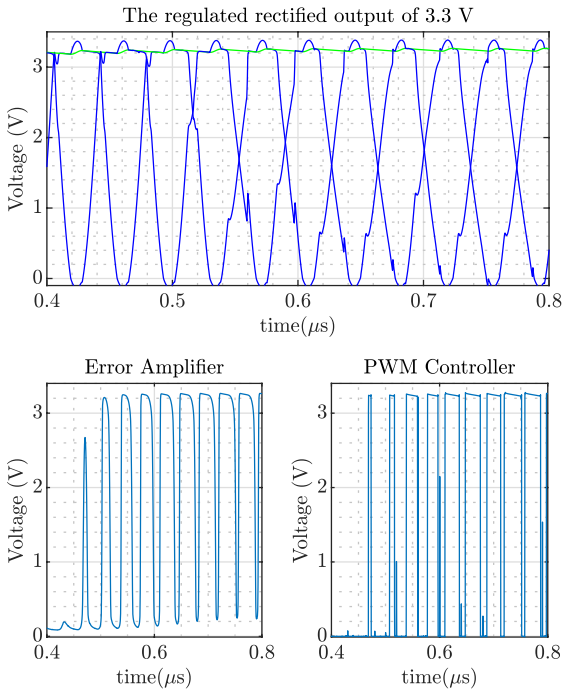

Fig. 7. The simulated results show the output of the active regulating rectifier of 3.3V, the output of the error amplifier, and the output of the PWM Controller.

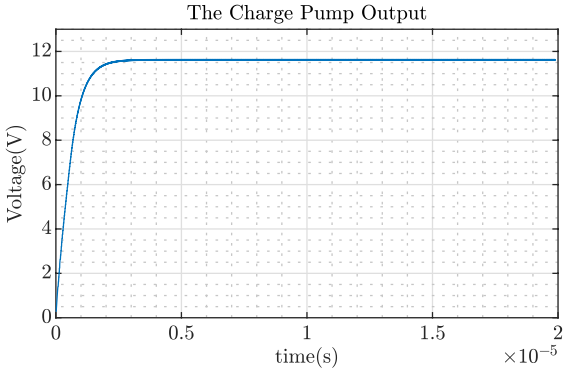

Fig. 8. Shows the output of the charge pump, which is around 11.8 V.

B. Three Stage Charge Pump

In the charge pump design, the charge is pushed from the supply, V_{in}, to the output node, V_{out}, stage by stage. The output voltage of the charge pump circuit can be pumped to a higher voltage than the inputted voltage. The voltage fluctuation of the pumping nodes, ΔV can be expressed as

$$\Delta V = V_{CLK}\left(\frac{C_{pump}}{C_{pump}+C_{parasitic}}\right) - \frac{I_{out}}{f(C_{pump}+C_{parasitic})} \quad (4)$$

where V_{Clock} is the voltage amplitude of the clock signals used, C_{pump} is the pumping capacitance, and $C_{parasitic}$ is the parasitic capacitance of each pumping stage. I_{out} is the current output, and f is the clock frequency. When taking V_{Clock} as the same voltage level as the power supply voltage, V_{in}, the voltage fluctuation can be expressed as

$$\Delta V \approx V_{clock} = V_{in} \quad (5)$$

The output voltage, V_{out}, for the latch charge pump with charge transfer at steady state with the assumption that the vol-

TABLE I. COMPARISON OF REGULATING RECTIFIER WITH PREVIOUS WORKS

	Lee [14] TCAS-I11	Li [16] JSSC15	Kim [6] JSSC17	Erfani [15] TBioCAS20	***This Work***
Process	0.5-µm 3M2P CMOS	0.35-µm CMOS	0.18-μm 1P8M CMOS SOI	0.18-μm TSMC 1P/6M	**0.18-μm CMOS**
Freq. (MHz)	13.56	13.56	144	1-10	**13.56**
V_{in_ac} (V)	3.8	NA	0.98-1.5	1.5-3.3	**3.5**
V_{dc} (V)	3.12	3.6	1	1.5-2.5	**3.3**
R_{load} (kΩ)	0.5	0.2,1	8	0.1	**0.33**
$P_{out,Max}$ (W)	20m	102m	700μ	65m	**30.3m**
VCE (%)	82.2	NA	92	75.8	**94.3**
PCE Peak (%)	87	92.6	54	90.7 (@2 MHz)	**70.7**
Reg.	NA	PWM	Hybrid	**PWM + PFM**	**PWM**
Area (mm^2)	0.4	0.18	0.0078	**NA**	**[a]0.048**

[a.] Including the charge pump

tage drop across the pumping switches is zero and (5) is applicable. A simply reduced equation the three stages charge pump circuit can be expressed as

$$V_{out} = (n+1)V_{in} - V_t - \frac{nI_L}{fC_{pump}} \quad (7)$$

Where n is the number of stages, V_t is the threshold voltage of MOS transistors, and I_L is the load current. Therefore, the larger the C_{pump} is the larger the V_{out} . The P_{out} of the charge pump can be calculated as

$$P_{out} = V_{out}\ I_{out} = \frac{{V_{out}}^2}{R_{Load}} \quad (8)$$

The theoretical maximum power efficiency of the charge pump is

$$\eta_{CP\,Max} = \frac{1}{n+1+\alpha(\frac{V_{out}}{V_{in}})} - \frac{V_{out}}{V_{in}} \quad (9)$$

Where α is multiplier factor assumed to be 0.2 [17]. The simulated results were carried out with 20 MHz clock, 10 pF C_{pump}, and 60 pF output capacitor. The output is around 11.8 V with a resistor of 50 kΩ as shown in Fig. 8. The power conversion efficiency is 92.2%. The output is restricted to be under 12 V to ensure that the deep n-well in the transistors is not damaged when the load is increased.

IV. CONCLUSION

In this paper, an active rectifier operating in 13.56 MHz with a high-speed comparator architecture is implemented. The design is implemented with PWM controller for regulating and having an output of 3.3 V. The proposed design help reduces power dissipation. The results show the proposed active regulating rectifier achieves a peak PCE of 70.7% under a 0.33 kΩ load resistor and a high VCE at 94.3% under the loading resistor. The charge pump is also designed to be a three HV charge pump for the stimulator design requirements. Future work will focus on implementing an adiabatic switch control signals to enhance the performance of the charge pump and improve efficiency.

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