A Power Efficient Time-to-Current Stimulator for Vagal-Cardiac Connection after Heart Transplantation

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***Abstract*—This paper presents a stimulator for a cardiac neuroprosthesis aiming to restore the parasympathetic control after heart transplantation. The stimulator is based on time-to-current conversion, instead of the conventional current mode digital-to-analog converter (DAC) that drives the output current mirrors. It uses a DAC based on capacitor charging to drive a power efficient voltage-to-current converter for output. The stimulator uses 1.8 V for system operation and 10 V for stimulation. The total power consumption is $I_{stim} \times 10\,\mathrm{V} + 18.4\,\mu\mathrm{W}$ during the biphasic current output, with a maximum I_{stim} of 512 µA. The stimulator was designed in CMOS 0.18 µm technology and post-layout simulations are presented.**

Keywords— Heart transplant, implantable devices, neural stimulator, time-to-current, vagus nerve stimulation.

I. INTRODUCTION

Every year, there are over 3000 heart transplantation surgeries conducted worldwide. Such surgery is the last resort of a patient who is at the end-stage of heart failure. Even though heart transplantation can extend the life expectancy of those patients, health-related issues remain. This is mainly due to cardiac denervation leading to chronotropic incompetence. Because of the complexity involved during the surgery, denervation is inevitable and causes the transplanted heart to function without any parasympathetic control. By innervating the sinoatrial and atrioventricular node, the parasympathetic control functions to slow the heart rate and relax the heart [1]. Such control is mastered by the vagus nerve for cardiac activity modulations; denervation means this connection is lost between the patient and donor heart which is only controlled by the circulation catecholamines. This not only affects the exercise capacity and health-related quality of life of the patient but also leads to long-term complications.

To re-bridge this neural link, a cardiac neuroprosthesis is proposed comprising a regenerative electrode structure and with a multi-channel stimulator chip for artificial vagus control. As the concept diagram shows in Fig. 1, the stimulator chip will be coupled to a regenerative neural interface [2], [3] capable of guided nerve regeneration. The remaining nerves between the donor and recipient are to be placed in the main tubing of the regenerative electrode. Between the disconnected nerves, multiple micro-tubings are designed to guide nerve regeneration. Surrounding the micro-tubing, electrodes are embedded and connected to the stimulator implant. Once nerves are regenerated, the implant can aid cardiac-vagal re-connection by providing multi-site stimulation. With both the re-connection of vagus and 'grafting' of the electrode stimulation capability, the parasympathetic control would be reinstated.

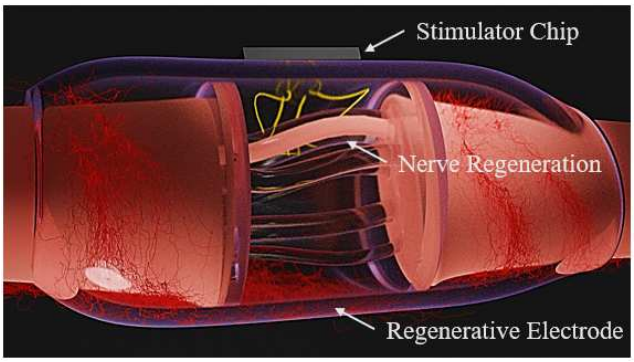

Fig. 1. Concept of cardiac neuroprosthesis with regenerative electrodes for vagal-cardiac re-connection.

This paper concerns the design of the neural stimulator for regenerative electrodes. A neural stimulator normally consists of a current driver that delivers biphasic current pulses between a pair of electrodes. Neural responses could be triggered by a small stimulation current ranging from tens to hundreds of micro-amps [4]. Between the pair of electrodes, due to the unavoidable use of miniature electrodes, the load impedance that the stimulator needs to drive could easily be higher than 10 kΩ [5]. As a result, the stimulator requires a high output impedance, and the use of high voltage compliance is often inevitable. Given the obvious power constraint that is imposed on any implantable device, power efficiency is one of the main stimulator design challenges. In addition, a balanced biphasic current pulse is required with an electrode discharging mechanism to remove any residual charges. Lastly, the stimulator must be fail-safe. To avoid dc-current induced electrolysis, the most common practice is to insert a blocking capacitor. An alternative safety design is reported [6]. It is also essential to have a fuse mechanism that stops the system operation if excessive current is detected.

In this paper a simple time-to-current based stimulator is presented. It can output a maximum current (I_{stim}) of 512 µA from a 10 V high voltage (HV) supplied output branch. Apart from this single HV output branch, other circuits are operated under a 1.8 V supply. The stimulator has a linear time-to-current conversion rate of 1 $\mu A/\mu s$ with a total power consumption of $I_{stim} \times 10\,V + 18.4$ µW during the biphasic current output. The rest of the paper is organized as follows. Section II describes the stimulator architecture and Section III outlines the design concept as well as details of the various system blocks. Section

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IV presents post-layout simulation results and concluding remarks are drawn in and Section V.

II. Stimulator Architecture

As shown in Fig. 2 (a), there are mainly two ways to produce biphasic stimulation [6]: 1) using a high-side and a low-side current driver together [7] to deliver the biphasic pulses under dual high voltage supplies; 2) using one-side driver only with an H-bridge arrangement for biphasic operation. As current is produced by one driver only, the one-side method should have better biphasic current matching and higher power efficiency. For electrode discharging, an additional switch S3 as shown in Fig. 2 (a) can be used. This switch closes during pulse intervals (the gap between two adjacent biphasic pulses) to equalize the electrode potentials.

Over the years, numerous stimulator designs have been reported. Fig. 2 (b) shows a popular current driver topology for one-side drive design [8]–[12]. From a current mode digital-to-analog converter (DAC), the desired current amplitude is generated and then mirrored from transistor M1 to M2 for stimulation. When operated under high voltage compliance, an HV transistor is required under the bias control of opamp A1. This active feedback clamps the drain voltage of M2, and not only offers reliable current mirroring and high output impedance, but also couples the low-voltage (LV) MOS to HV MOS to drive a large impedance load.

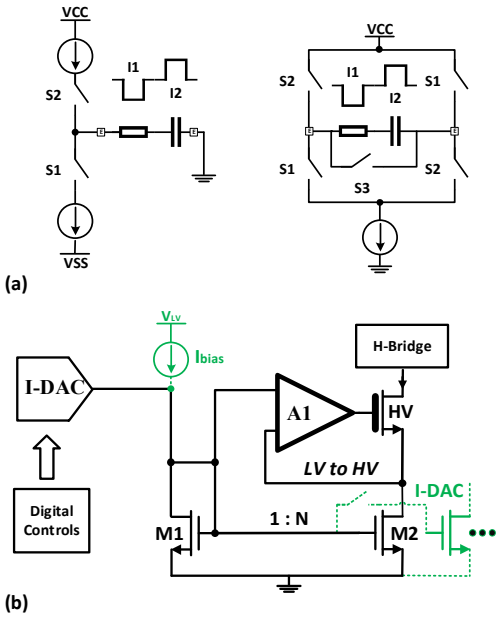

Fig. 2. (a) Top-level stimulator design topologies. (b) Commonly adapted current driver topology for stimulator (the green lines show a possible variant).

There could be current scaling between M1 and M2, but power is still required for the current-mode DAC (I-DAC) operation. An alternative design could be the rearrangement of the I-DAC as shown by the green dotted plots in Fig. 2 (b). The original I-DAC is replaced by a constant dc biasing current, and the DAC operation is moved to the M2 location for better power efficiency. This merges the DAC with the output stage of the stimulator; thus for multi-channel design, DAC sharing is no longer viable [11].

III. Neural Stimulator Design

The proposed design provides a new DAC arrangement that is both power efficient and simple to apply in multi-channel designs. As shown in Fig. 3 (a), instead of using a conventional I-DAC that has multiple current branches, by controlling the charging period of a capacitor, the desired voltage can be generated by simply charging it with a small constant dc current. Directly using the output voltage from such capacitor-charging based DAC (C-DAC) to bias e.g., the gate of M2 offers a more power efficient design. In such C-DAC, the relationship between charging time and voltage developed on the capacitor is linear. Thus, the time-to-current control would be quite simple if the voltage-to-current conversion also has a linear relationship. By biasing M2 in the triode region, the circuit is effectively a voltage-to-current converter with a linear transfer function of $I = V_{ref}/R_{\mathrm{M2}}$, where V_{ref} is a fixed bias voltage and R_{M2} is the equivalent resistance of MOS transistor M2 whose resistance varies according to C-DAC. An issue with such a topology is its non-linearity due to the MOS resistor M2 which requires extra compensation [13].

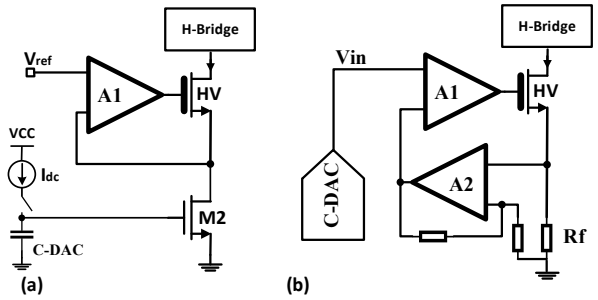

Fig. 3. (a) Stimulator based on voltage-to-current converter with MOS resistor. (b) Proposed time-to-current converter stimulator topology using C-DAC.

A. Voltage-to-Current Converter

A method to implement such a voltage-to-current converter with good linearity is shown in Fig. 3 (b). It uses a fixed-value resistor instead of M2 and applies the C-DAC voltage to the positive input of the active feedback opamp. For better power efficiency, a 1.8V MOS transistor based opamp is used to drive a 10V HV MOS at the output branch. This requires maximizing the overdrive voltage, so a small feedback resistor $R_f = 100\Omega$ is used. However, for the target maximum current of 500 µA, this reduces the maximum C-DAC voltage to 50 mV making its implementation challenging. To overcome this issue, another non-inverting amplifier opamp A2 with a gain of 10 is added. The transfer function of the proposed design shown in Fig. 3 (b) is:

$$I_{out} = V_{in}\frac{gm_{HV}\cdot A_{ol}}{1 + R_f\cdot G\cdot gm_{HV}\cdot A_{ol}} \approx V_{in}\frac{1}{R_f\cdot G} \quad (1)$$

where gm_{HV} is the transconductance of the HV MOS transistor, A_{ol} is the open-loop gain of A1 and $G = 10$ is the gain of non-

inverting amplifier. The transconductance for this current driver is 1 mA/V. Regarding the design of the two opamps, firstly in order to utilize the full LV supply to drive the HV MOS transistor, a rail-to-rail opamp is used for A1 [14]. The design of A2 is based on a two-stage folded-cascode. For A2, a p-type input stage must be employed to ensure the detection of the small voltage developed across R_f.

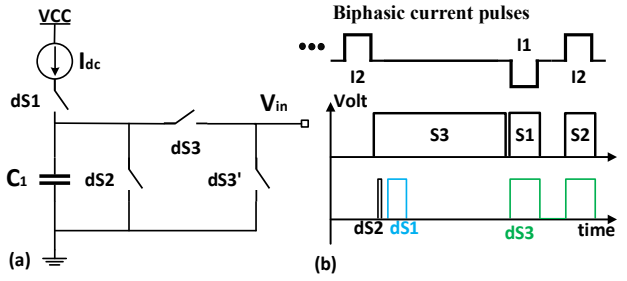

Fig. 4. (a) The circuit implementation of C-DAC. (b) The switch timing diagram of the C-DAC and H-bridge.

B. *Time-to-Voltage Converter*

For the targeted application, the stimulation frequency is mostly < 1 kHz, and the pulse widths are in the range of hundreds of microseconds. Thus, the charging period needs to fit between the pulse intervals. By designing a charging period of up to 512 µs and a LSB charging time of 2 µs, would give an 8-bit DAC equivalent resolution. The C-DAC circuit implementation is shown in Fig. 4 (a) and the digital control timing diagram is shown in Fig. 4 (b). For the H-bridge switches, HV MOS transistors are used and the digital logic control is uplifted to 10 V with level shifters. With the overall digital operation under a 1 MHz master clock, the digital control has a time resolution of 1 µs. S1, S2 and S3 are the control signals for the H-bridge [refer to Fig. 2 (a)]. At the pulse interval, no current is delivered to the load, and S3 is closed for electrode discharge. During this time, dS2 closes for 1 µs to reset capacitor C_1. When dS2 opens dS1 connects the dc current, I_{dc}, to charge the capacitor C_1. The capacitor is set to 25 pF and the charging current I_{dc} is set to 25 nA which is the total biasing current required for this C-DAC. The voltage developed across the capacitor is given by:

$$V_{in} = I_{dc} \times T_{dS1}/C_1. \qquad (2)$$

During the inter-phase delay (the gap between I1 and I2), no current flows through R_f. If A1 still receives an input, its output would be saturated leading to a current spike when the H-bridge turns on again. dS3' is closed to avoid output saturation of A1 when no current flow through the HV branch. The voltage-to-current converter has a transconductance of 1 mA/V. One LSB of charging time corresponds to 2 mV of V_{in} leading to an output current of 2 µA. Effectively, a simple and linear time-to-current conversion relationship is established as 1 µA/µs.

With regard to safety, because the maximum gate voltage that can be applied to the HV MOS transistor is 1.8 V, the maximum possible output current can be limited by design. Also, the output of A2 could be used for real-time current monitoring. Using a comparator, exceeding a reference voltage can generate an overcurrent shutdown for safety operation. This fuse mechanism takes advantage of existing components which otherwise would require added circuitry using conventional designs [e.g., Fig. 2 (b)].

IV. System Simulation Results

The stimulator was designed in HV 0.18 µm CMOS technology as shown in Fig. 5 with a silicon area of 0.16 mm^2.

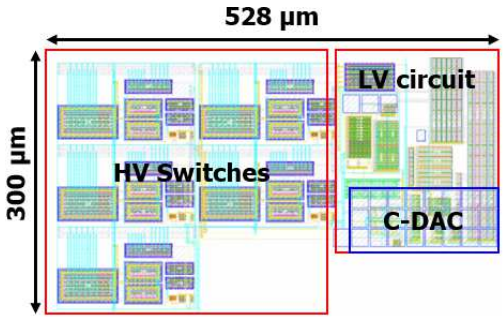

Fig. 5. The stimulator layout view.

Without connecting to the C-DAC or the H-bridge, the ac transconductance response of the proposed voltage-to-current converter is shown in Fig. 6.

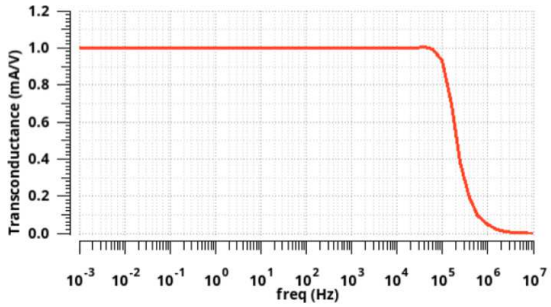

Fig. 6. Transconductance of the proposed voltage-to-current converter.

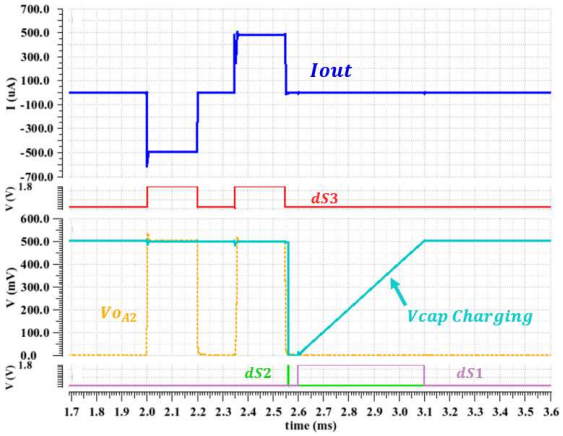

Fig. 7. The stimulator output of 500 µA; $Vcap$ is the voltage on the charged capacitor $C1$, and Vo_{A2} is the output of A2.

Fig. 7 shows the system operation, using a 10 kΩ resistive load. As shown, after dS2 reset, the voltage on the capacitor, $Vcap$, rises, the charging period of dS1 is set to 500 µs. After charging

to 500 mV, $Vcap$ is held and is connected to the H-bridge by dS3. The stimulator can then initiate biphasic operation. Vo_{A2}, the output of opamp A2, during biphasic phase, equalizes to $Vcap$ and indicates the desired current amplitude is being outputted; Vo_{A2} is also used for current monitoring.

Table I. Comparison with other stimulator designs.

	This work	[7]	[8]	[9]
Technology	0.18 µm	0.35 µm	0.6 µm	0.35 µm
Max current amplitude	512 µA	1 mA	< 1 mA	94.5 µA
Voltage compliance	10 V	20 V	18 V	5 V
Operation power[1]	18.4 µW	171 µW	1.1 mW	45 µW
DAC current[2]	25 nA	26 - 102 µA	64 µA	6.4 µA
DAC resolution	8-bit	5-bit	8-bit	6-bit
Stimulator area	0.16 mm^2	0.2 mm^2	2.27 mm^2	0.02 mm^2

[1]Excluding stimulation output; [2]At maximum DAC output.

The stimulator has a total power consumption of $I_{stim} \times 10\ \text{V} + 18.4\ \mu\text{W}$ where I_{stim} is the current delivered to the load and the maximum I_{stim} is $512\ \mu\text{A}$. The quiescent power of the stimulator (e.g., during inter-phase delay where $I_{stim} = 0$) is 13.4 µW.

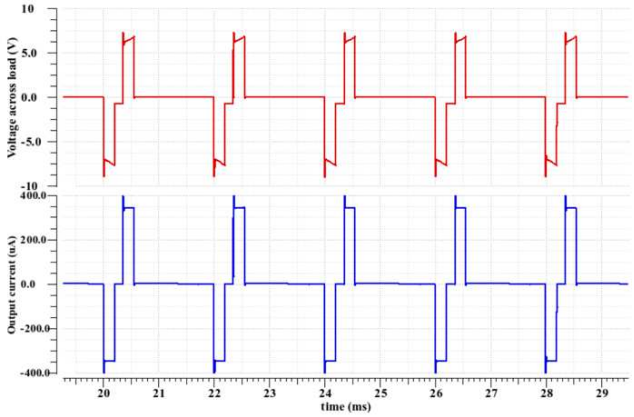

Fig. 8. Simulation results of the stimulator output of 350 µA with a RC load in series (R = 20 kΩ and C = 100 nF). The top plot is the voltage measured across the load and the bottom plot is the current through the 20 kΩ.

Fig. 8 shows the stimulator current when driving a RC load with R = 20 kΩ and C = 100 nF with a C-DAC charging period of 350 µs. The top plot shows the voltage developed across the RC load, and the bottom plot shows the current through the load.

Table I summarizes the design parameters and compares it to other work. As shown, even under a high voltage compliance, the design can output half milliamp of current in a very power efficient manner. The stimulator design may occupy a larger silicon area when using HV CMOS technologies. For high-density electrode applications, as an optimization, the C-DAC capacitor could be placed on top of other analog circuits to obtain a smaller silicon area.

V. Conclusion

A new stimulator architecture design has been presented. By simply charging a capacitor, the desired voltage can be generated and sent to a voltage-to-current converter to achieve a linear and power efficient time-to-current conversion. The stimulator, implemented using CMOS 0.18 µm technology, can output a maximum I_{stim} of 512 µA with a total power of $I_{stim} \times 10\ \text{V} + 18.4\ \mu\text{W}$ during stimulation with a single 10 V HV output branch. The stimulator also features real-time current monitoring for safety operation and can be easily adapted for multi-channel vagal nerve stimulation.

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