An Active Microchannel Neural Interface with Artifact Reduction

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Abstract— **High-density neural electrodes in microchannel interfaces require in-situ amplification of the neural signals and rejection of high-voltage stimulus pulses leaking to the channel in order to adequately detect neural signals in the presence of concurrent stimulation. This paper presents the design of an active microchannel neural interface in 0.18 µm CMOS employing neural recording and stimulation. To reduce stimulus artifacts, a novel method is proposed that disconnects the recording module during concurrent channel stimulation and automatically applies detection and reduction of stimulus artifacts from adjacent channels using a tunable filter. Simulations show that the method provides at least 54 dB artifact attenuation.**

***Index Terms*— Neural interface, biomedical electrodes, neural recording, microchannels, high-voltage stimulation, artifact detection**

I. Introduction

Regenerative neural interfaces selectively interface subpopulations of neurons using separate electrodes, while offering a trade-off between encouraging axonal growth and selectivity [1]. Microchannel neural interfaces (MNI) are regenerative interfaces which maximize the amplitude of recorded action potentials by confining the extracellular space surrounding the axon [1]. As shown in Figure 1a and Figure 1b, MNIs comprise parallel tubes (channels) formed of a biocompatible insulator such as silicone [2] or polyimide [1], containing electrode contacts. Microchannel lengths typically range from 2 mm to 5 mm for nerve regeneration; this allows neural recording independent of the location of the nodes of Ranvier in the MNI [1]. A channel width of 100 μm to 200 μm achieves a selective interface with a large extracellular resistance, while limiting channel blockage by fibrotic tissue [1].

Channel density in passive MNIs is limited by the need for interconnects for each electrode [3]. Furthermore, the use of tripolar electrodes, a method of artifact reduction, requires additional interconnects per channel, increasing design complexity and the risk of device failure. To overcome such challenges, a stimulator-recording system with miniaturized on-chip connections was reported, [3] with electrodes on the surface of an application specific integrated circuit (ASIC) to multiplex all the corresponding connections. As a result, fewer and shorter interconnects are required to access the channels. Further scaling could be achieved by stacking several parallel ASICs to create a 3-dimensional microchannel array, as shown in Figure 1c.

Adequate recording of neural signals requires a sufficiently high input range and signal-to-noise ratio to prevent signal distortion, as well as a large enough common-mode rejection ratio, which is often limited by channel interferences and mismatch in the electrode impedances. In-situ amplifiers have been developed to address this issue by reducing the capacitive coupling of the connective tracks. The resulting active electrodes can convert the electrode sites to low-impedance nodes, limiting their sensitivity to crosstalk and other artifacts [4].

A challenge is imposed, however, for concurrent stimulation and recording with an MNI**.** Due to the large electrode impedances and the required stimulus currents reported on microchannel devices, very high stimulus compliance voltages (40 V) can appear at the inputs of the recording front-end during concurrent channel stimulation. To address this, a method is proposed in this paper that minimizes artifacts during recording. This can be addressed by temporarily disconnecting the recording unit to block the stimulus artifact. Moreover, in-band artifacts can be detected at the recording input from the adjacent channels' stimulus pulses, which can be automatically detected to enable adjustment of the filter characteristics.

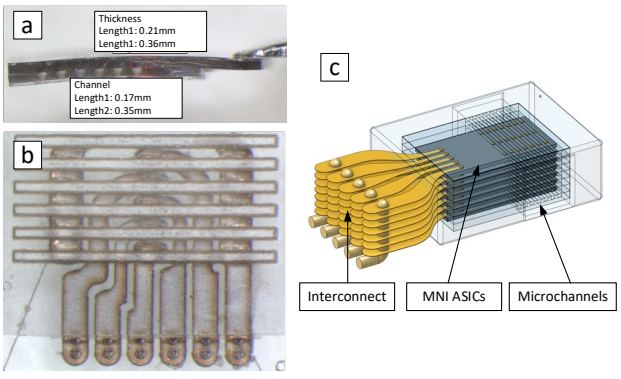

Figure 1. A stacked MNI device showing the (a) layer thickness, (b) channel surface area, and (c) multi-layer *view* [3].

The paper is organized as follows. Section II reviews the conventional methods used for artifact reduction and introduces the proposed novel technique. Section III provides an overview of the active MNI concept and the circuitry for artifact detection and reduction during recording. Section IV presents the simulation results. Comparison with other designs is detailed in Section V, and concluding remarks are presented in Section VI.

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II. Artifact Reduction Methods

A. Conventional Methods

Commonly used techniques that mitigate the effects of stimulus artifacts can be divided into three categories: prevention, front-end immunity, and back-end processing [5]. Preventive methods such as charge balancing ease the requirement on the front-end, though fail to remove artifacts sufficiently, leading to amplifier saturation and slow amplifier recovery. Alternative techniques that improve the front-end immunity aim to prevent saturation to maintain a linear response [6], or achieve rapid recovery for reduced data loss [7]. Back-end cancellation methods are often applied to digitized signals to reconstruct the neural data or subtract artifacts via adaptive filtering [5], achieving reliable artifact removal at the cost of area and complexity [8].

B. Proposed Method

This work proposes an automatic and simple design for artifact reduction, combining two methods to increase front-end resilience to high-voltage artifacts. Namely, signal blanking, which protects the recording amplifier inputs, easing the requirements for a high dynamic range and allowing a low-voltage implementation of the recording front-end, and pole shifting, which reduces the effects of adjacent channel pulses and minimizes data loss by adjusting the low-pass cut-off frequency of the amplifier during adjacent channel stimulation.

An additional means of further reducing the artifacts is via the application of chopped stimulus pulses, which consist of high-frequency current packets within each pulse with small intervals between pulses. Compared to the conventional lumped pulse technique, which applies current pulses hundreds of microseconds wide, the µs-wide current packets of the chopped pulses result in high frequency outputs due to the resistive component of the electrode-electrolyte interface, while the envelope generated by the capacitive components of the interface can appear at much lower amplitudes [9]. Consequently, the artifacts due to chopped pulses can be filtered more effectively. The pixel-based structure of the recording and stimulation circuitry for each channel in the MNI allows for individual and customized control of each electrode.

III. System Design

Figure 2 shows an overall block diagram of the active MNI ASIC, composed of seven tripolar electrode channels, such as those shown in Figure 1b, alongside a global control and biasing unit. All channels include a localized recording module that operates the artifact reduction circuits, and a stimulation module, the parameters of which are directly set by the local digital control unit. A global 2nd-order low-pass filter is included in each chip to provide a sharper roll-off, thus attenuating the artifacts more distinctly.

The primary goal of the system is to apply closed-loop stimulation by recording the neural signals generated via the stimulus pulses. To achieve this, a bandwidth of 300 Hz to 5 kHz [3] is selected for detecting action potentials with amplitudes ranging from 20 µV [1] to 520 µV [10] under nominal recording conditions, during which no stimulus artefacts from adjacent channels are detected.

A pole shifting mechanism is implemented to limit the effects of crosstalk during concurrent stimulation and recording by constricting the recording bandwidth of the amplifier [11]. This function is automatically enabled upon the detection of higher-than-expected input signals via a differential comparator, as discussed in the following sub-sections.

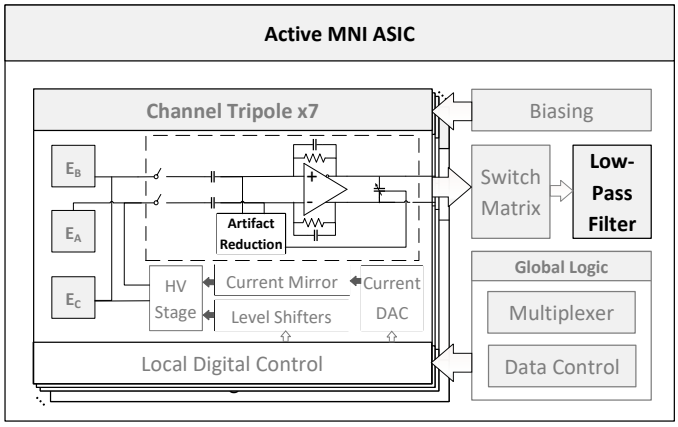

Figure 2. Active MNI system block diagram.

A. Neural Recording

The fully differential low-noise amplifier (LNA) illustrated in Figure 3a was implemented with a capacitive feedback network to remove all DC offsets from the inputs and define a mid-band gain of $C_{in}/C_f = 40$ dB. A feedback resistor R_f is placed in parallel with the capacitor C_f to bias the input terminals and define the high-pass corner. The load capacitor C_L connected across the outputs selects a tunable low-pass corner.

Two high-voltage (HV) switches, M_{H0} and M_{H1}, are included at the amplifier inputs to provide blanking of the stimulus pulses in the same channel, which can exceed the safe limits specified for the low-voltage (LV) transistors. The use of protective HV switches allows the safe operation of the HV stimulator unit alongside the LV recording circuitry, which consumes less power and a smaller chip area.

A telescopic cascode operational transconductance amplifier (OTA) with common-mode feedback was selected to detect neural signals in the specified range as shown in Figure 3b. The dimensions of input transistors M_1 and M_2 were carefully selected to minimize the flicker noise introduced by operating in the weak inversion region. Conversely, the g_m/I_d ratio of the load transistors M_7 and M_8 was minimized to operate in strong inversion for a low thermal noise.

The pseudo-resistor R_f was implemented using a parallel-NMOS architecture. This structure is selected to optimize the control and performance of the feedback resistor under the effects of PVT variations with minimal noise and power consumption.

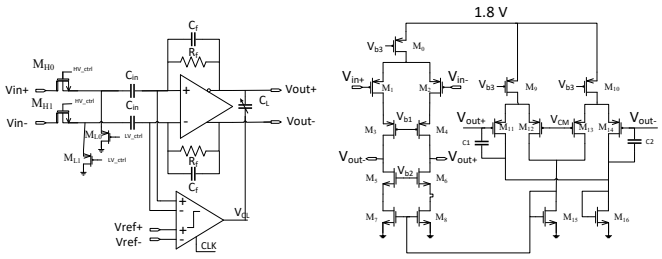

Figure 3. LNA schematics showing (a) amplifier with blanking and artifact detection, and (b) OTA with common-mode feedback.

B. Artifact Detection

In order to accurately record neural activity without saturation by artifacts generated from adjacent channels' stimulus pulses, the recording amplifier provides a variable bandwidth to block the high-amplitude stimulus pulses. The application of pole shifting provides front-end immunity to the amplifier against stimulus artifacts, thus reducing data loss without the need for a high dynamic range [5]. A similar technique more often described as 'soft switching' takes advantage of the adjustability of passive components such as pseudo-resistors and variable capacitors in controlling the bandwidth, limiting the effects of switching artifacts such as leakage and charge injection [11]. This also supports rapid recovery for the front-end and does not require electrode discharge for every event of adjacent channel stimulation, as is the case following amplifier disconnection during blanking, which is necessary to protect the LV recording unit [7].

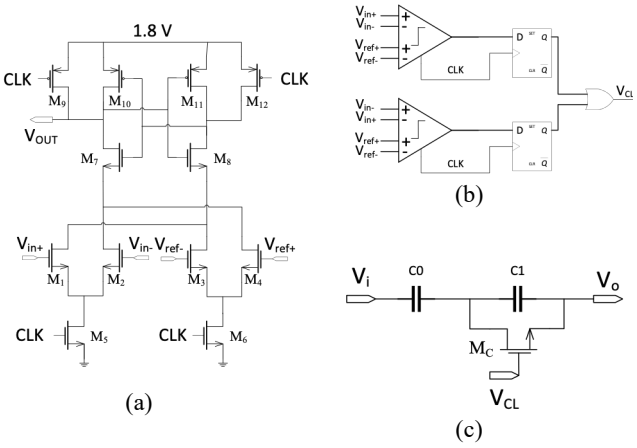

Figure 4. Schematic diagram of (a) fully differential comparator, (b) logic output stage, and (c) variable load capacitor.

Timely detection of artifacts is achieved via the fully differential comparator shown in Figure 3a and Figure 4a. A latched architecture is implemented to achieve a high speed without compromising power or area, while the differential sensing inputs account for the voltage excursions expected in the recorded neural signals. In order to enable pole shifting upon the detection of high input signals at either input, thus accounting for both anodic-first and cathodic-first stimulus pulses, two such comparators are placed in each channel as shown Figure 4b, with a control signal extracted using D flip-flops and an OR gate.

A schematic of the variable load capacitor (C_L) is presented in Figure 4c, where the comparator output determines the state of transistor switch, M_C, via its gate control signal, V_{CL}. During pole shifting, the switch bypasses the capacitor C_1 and provides a load capacitance equal to C_0, while during nominal operation, the switch is off, and the load capacitor is a series combination of C_0 and C_1.

IV. Simulation Results

A microchannel neural interface using the proposed circuits was designed and simulated in a 0.18 µm HV CMOS technology. The performance of the recording unit is presented below.

A. Recording Amplifier

The capacitively-coupled LNA is designed to provide a total gain of 40 dB via the input and feedback capacitors set at 20 pF and 200 fF, respectively. To obtain the nominal bandwidth for action potentials (300 Hz to 5 kHz), the feedback resistor is tuned to 2.5 MΩ, and the series load capacitors to 2.6 fF across the outputs of the amplifier. The OTA has an input-referred noise of 5.2 μV_{rms}. This proves a sufficiently low noise floor, as the recorded action potential signal magnitudes in microchannels range from 20 µV to around 520 µV.

The high-voltage blanking switches at the amplifier inputs block HV signals by providing an off-resistance of 5.5 MΩ during same-channel stimulation and present an on-resistance of up to 500 Ω during recording, which is at least two orders of magnitude smaller than the expected electrode impedance [1]. Monte Carlo analysis was carried out to measure the variation in the value of the pseudo-resistor, R_f. The average resistance was measured within 8.5% of the nominal value, with a standard deviation of 1.8%. This corresponds to a maximum difference of 0.21 GΩ, which results in up to 23 Hz of variation in the frequency domain.

B. Bandwidth Adjustment

Figure 5a shows the frequency response of the recording amplifier over the nominal action potential range and the modified range upon the application of artifact reduction that shifts the low-pass cut-off frequency of the filter to 1 kHz, which is below the typical stimulus pulse frequency range.

Transient analyses of the differential comparator demonstrated the pole shifting functionality over inputs above and below the comparator threshold voltage. A maximum delay of 20 ns was measured on the rising edge of the comparator for a clock period of 10 µs, resulting in a minimum slew rate of 88.6 V/µs. This proves a sufficiently fast response for artifacts with frequencies as high as 20 kHz, which are used to block nerve conduction [12]. The reduction capability of the pole shifting module was tested by measuring the LNA outputs of a composite input signal that consists of stimulation artifacts

generated as 30 mV pulses with the commonly-applied pulse width of 0.2 ms [13], and recording spikes 500 µV in amplitude applied at a 1 kHz frequency, resulting in a -36 dB artifact-to-signal ratio at the inputs. Figure 5b illustrates the effect of pole shifting on the LNA output signals in the time domain. This method achieves an attenuation ratio of 54 dB with chopped stimulus artifacts.

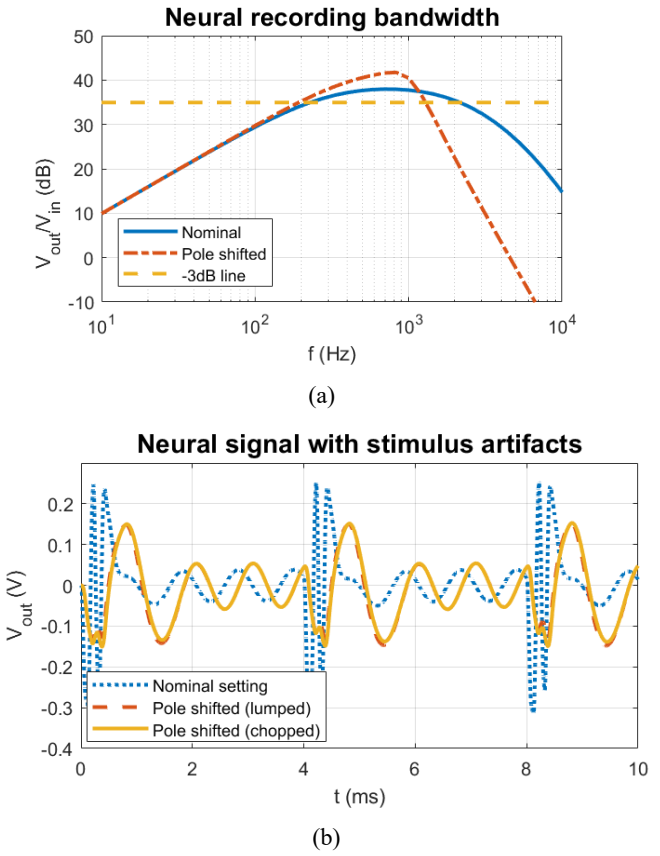

Figure 5. Simulation results of (a) LNA bandwidth adjustment and (b) Artifact attenuation with chopped and lumped pulses.

V. Discussion and Conclusion

This design demonstrates an on-board recording and stimulation system for microchannel applications, capable of detecting artifacts generated due to the high-voltage stimulus pulses that exceed the expected magnitude range of the action potential signals in each channel. The combination of the capacitively-coupled LNA and the comparators occupies an area of 0.23 mm^2 and consumes up to 3.89 µW of power during artifact reduction. The design achieves an acceptable trade-off between the simulated power and noise. It has an input-referred noise of 6.3 μV_{rms} and a noise efficiency factor of 5.13 over the recording frequency range of 300 Hz to 5 kHz. Future work will include improving the signal-to-noise ratio of the LNA by optimizing the low-pass filter that acts to reduce artifacts.

An active MNI system for the stimulation and recording of nerves enclosed in microchannels has been presented and simulated in 0.18 µm CMOS. The concept of artifact detection via the fully differential comparator and its reduction using the pole shifting technique has been explained and verified using Cadence Spectre. An attenuation ratio of at least 54 dB has been demonstrated in reducing stimulus artifacts.

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