Design, Fabrication, and Testing of MicroDSC Sensors

A final report prepared by:

Dr. Lawrence A. Bottomley
School of Chemistry & Biochemistry
Georgia Institute of Technology
Atlanta, GA 30332-0400
Ph: 404-894-4014
Email: Bottomley@gatech.edu

and submitted to:

Mr. Michael Curran
Sensor Tech, Inc.
447 Bull Street
Savannah, GA 31401

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1. Introduction

This report describes research focused on the design, fabrication and testing of a microelectronic differential scanning calorimetry (μDSC) device designed for sensing airborne analytes. Specifically, the fabrication of pairs of sensors comprised of a metal oxide film electrically isolated from a heater on a suspended platform comprised of alumina. The heater required low power and was capable of maintaining the temperature of the metal oxide layer at 600 ºF for extended periods of time. Four electrical connections were made to the serpentine heater intended for a four point probe measurement. Additionally, each sensor possessed a resistive thermal device (RTD) integrated sensing element.

1.1. Thermal Modeling. Thermal modeling was done by Jabulani Barber of the Bottomley research group to identify the optimal design for materials specified by Sensor Tech to use in fabricating the first prototype microDSC device. The modeling goal was to provide rapid and uniform heating of the metal oxide catalyst to the desired temperature. Simulations were conducted using the engineering software package Comsol Multiphysics 3.4 (Burlington, MA) to model the thermal conduction of the device. Component pairs were identified that enabled rapid and uniform heating with low power requirements with minimal thermally-induced stresses. The results of this modeling study were used in selecting the material combinations and subcomponent dimensions. For thermal isolation of the hotplates within the device from one another, a cantilever-based design was employed. Modeling revealed that complete thermal isolation of devices from each other would be achieved; the sapphire base substrate could be thinned beneath the serpentine heating element to reduce the thermal capacitance of the device. The serpentine heating element was positioned further from the top edge of the cantilever to decrease the heat loss to the sapphire substrate and the surrounding gas stream flowing over the cantilever. From modeling studies, the serpentine heater required 50 μm line widths and 10 μm spacing to reduce its resistance in response to the large voltage required to achieve the desired temperature.

1.2. Process and Mask Design. The process flow was designed around the base substrate made of sapphire. A serpentine platinum RTD was incorporated above each heater region. The metal oxide catalyst was designed to have an area identical to that of the RTD sensor, ensuring high uniformity in temperature across the catalyst surface. Mask sets were designed by Kane Barker of the Bottomley research group using AutoCad (Autodesk, Inc., San Rafeal, CA) based on the results obtained from the thermal modeling and the process design. Mast alignment markings and device identifiers were integrated into the mask designs to facilitate identification of chip sets after wafer dicing. Mask sets were fabricated by Photo Sciences, Inc. Torrance, CA). The following section describes in detail the photolithography processing steps designed to fabricate the first and second μDSC prototype devices.

2. Prototype #1 Initial Process Flow

The process design for prototype #1 was built around commercially available sapphire wafers. Ten 2" diameter sapphire wafers (300 μm thick) were purchased to serve as substrates. The following subsections lay out the steps involved in bringing a single wafer to completion. The process flow is presented in bulleted form to emphasize the detailed steps involved in the fabrication of the μDSC device.

2.1. Deposition of Silicon Nitride Mesas for μ-Heater (Figure 1).

Step 1. Plasma-enhanced chemical vapor deposition (PECVD) was employed to deposit a 1 μm layer of silicon nitride (Si_xN_y) over the entire sapphire wafer. PECVD was chosen because it provides a means for depositing a low stress film of desired thickness which is critical to reduce accumulated stresses as the number of layers on the sapphire wafer increases. Uniformity in this layer is critical for isolation of the nickel serpentine heater.

Step 2. Photolithography patterning is the standard tool for producing patterns on a wafer. The intended resist was AZ4260 along with the appropriate dark-field mask #1, and developer AZ400K.

Step 3. An RIE process was used to etch the Si_xN_y over other options because it is capable of producing straight and vertical walls. This etching step resulted in the formation of the Si_xN_y mesas which were used to define the dimensions of the serpentine heater.

Step 4. Post etching, the photoresist was removed using the appropriate solvent.

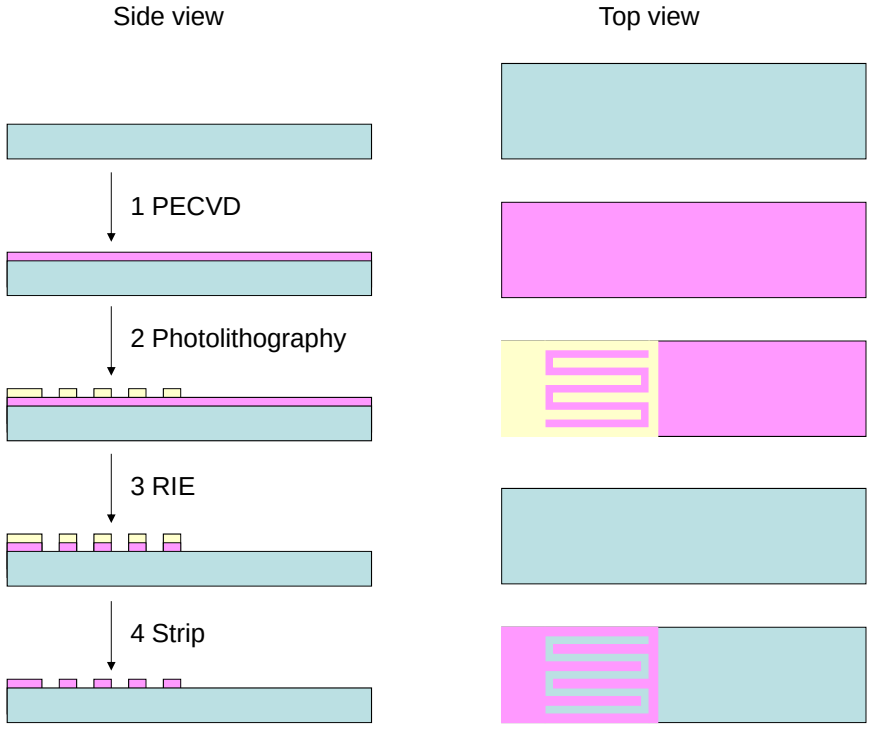

Figure 1. Schematic of the proposed process flow for deposition of silicon nitride mesas onto a clean sapphire wafer substrate. Both side and top views are provided.

2.2. Creation of Wiring for μ-Heater (Figure 2)

Step 5. The pattern for the lead wires was created by openings in the photoresist. The intended resist was SC1827 along with light-field mask #2 and developer Microposit 351.

Step 6. PVD was carried out using an e-beam metallization tool to produce a smooth thin film of titanium to serve as an adhesion layer for the subsequent deposition of gold. The gold leads serve as the connections to the serpentine heater.

Step 7. Excess metal deposited by the PVD process was removed from the wafer surface, leaving behind the metal in the desired location.

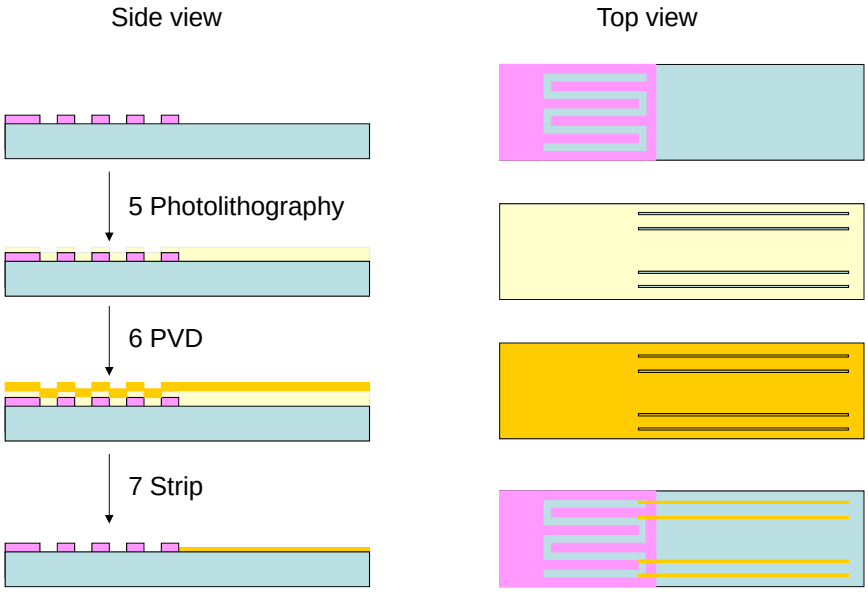

Figure 2. Schematic of the proposed process flow for creation of lead wires for serpentine heater. Both side and top views are provided.

2.3. Deposition of Nickel Serpentine for μ-Heater (Figure 3)

Step 8. The pattern for the serpentine heater was created by the openings in the newly deposited photoresist corresponding to the mesas created in the initial Si_xN_y layer. Photolithographic patterning step #3 was performed using SC1827 resist and clear-field mask #3.

Step 9. PVD was carried out using an e-beam metallization tool to produce a smooth surface of gold. Nickel was an ideal heating element because of its intrinsic resistivity. The thickness of the nickel deposition was adjusted based on the thickness of the Si_xN_y mesas.

Step 10. Excess metal was removed from the surface, leaving nickel in the desired location.

Step 11. Thermal annealing was required to fill gaps or discontinuities that were created during metal deposition. In doing so, electrical contact between the previously deposited gold leads and the nickel heater were made.

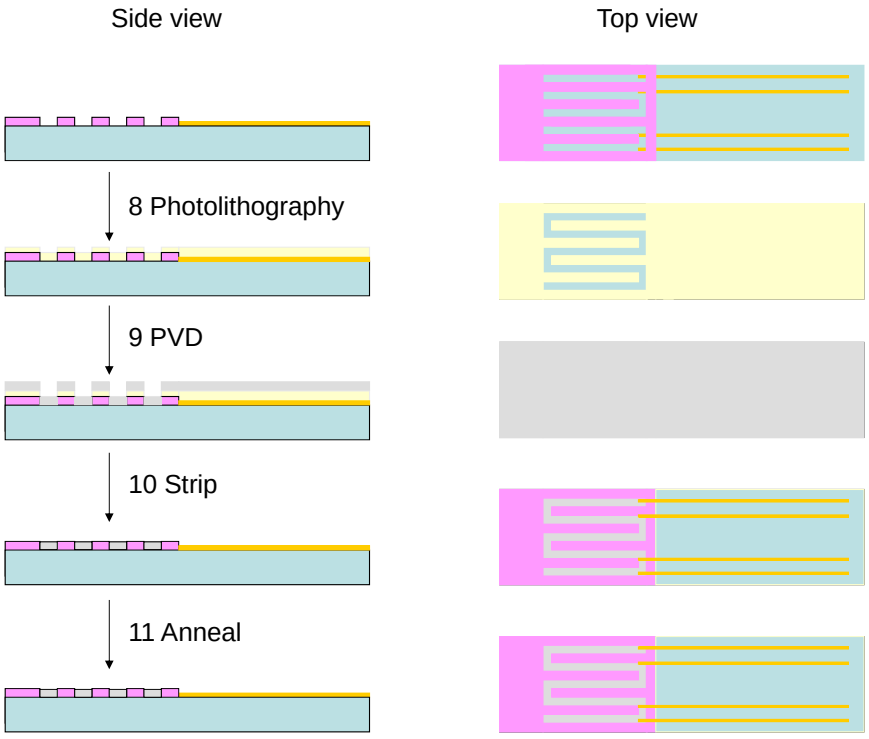

Figure 3. Schematic of the proposed process flow for deposition of serpentine nickel heater. Both side and top views are provided.

2.4 Deposition of Silicon Nitride Barrier Layer (Figure 4)

Step 12. Si_xN_y was deposited using PECVD to produce an isolating layer, both electrically and chemically, between the nickel heater and gold leads and future layers. Again, a low stress deposition method was employed to minimize surface stress.

Step 13. Photolithographic patterning step #4 was performed using SC1827 resist and clear-field mask #4.

Step 14. A wet chemical etch of the Si_xN_y was carried out to remove excess Si_xN_y, decreasing the possibility of thermal loss during testing. A wet chemical etch was required as Georgia Tech Cleanroom policy excludes metals from the RIE tools previously used to etch Si_xN_y.

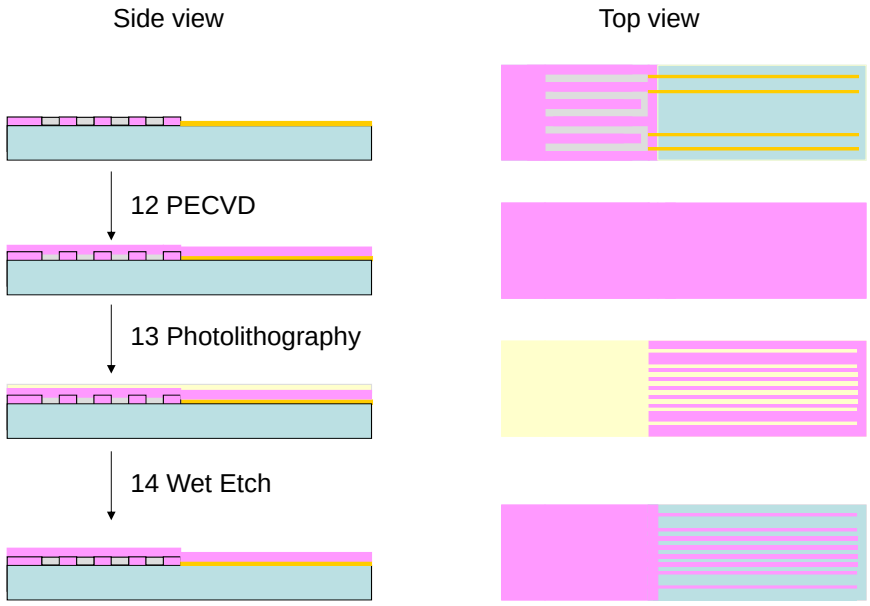

Figure 4. Schematic of the proposed process flow for deposition of the first silicon nitride barrier layer. Both side and top views are provided.

2.5. Creation of Wiring for RTD (Figure 5)

Step 15. The pattern for the wiring for the RTD was created by the openings in photoresist SC1827 and the appropriate clear-field mask #5.

Step 16. PVD was carried out using an e-beam metallization tool to produce a smooth thin film of titanium. Titanium served as an adhesion promoting layer for the subsequent deposition of gold onto the Si_xN_y layer.

Step 17. Excess metal deposited by the PVD process was removed, leaving metal in the desired location.

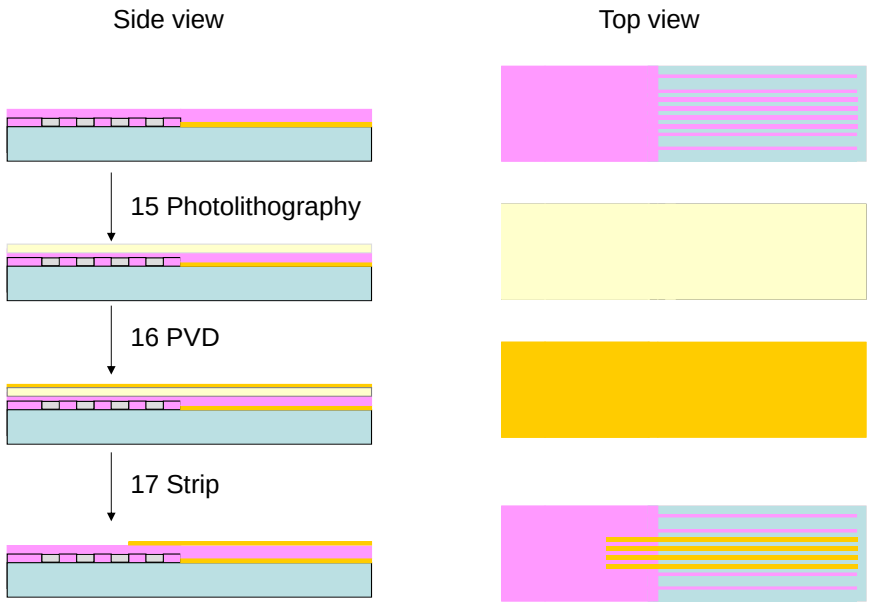

Figure 5. Schematic of the process flow for deposition of RTD connection wires. Both side and top views are provided.

2.6. Deposition of Platinum RTD (Figure 6)

Step 18. The pattern for the RTD was created by the openings in photoresist SC1827 and the appropriate clear-field mask #6.

Step 19. PVD was carried out using an e-beam metallization tool to produce a smooth thin film of platinum, completing the RTD. No adhesion layer was required because platinum is adherent to Si_xN_y. The dimensions of the serpentine RTD were determined from the thermal modeling studies described previously in this Report, section A.1.1.

Step 20. Lift off of the resist removed the excess metal deposited by the PVD process, leaving metal in the desired location.

Step 21. A sintering/anneal step was critical to allow the metals to fill gaps or discontinuities created during PVD of metal layers.

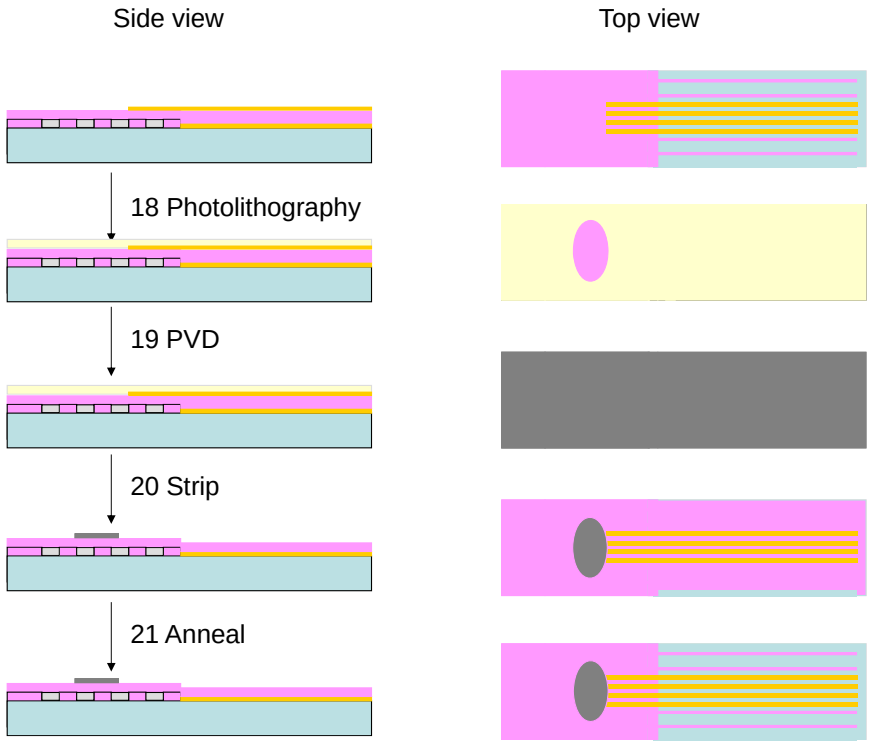

Figure 6. Schematic of the process flow for creation of the temperature sensing element. Both side and top views are provided.

2.7. Deposition of Silicon Nitride Barrier Layer (Figure 7)

Step 22. Si_xN_y was deposited using PECVD to produce an isolating layer, both electrically and chemically, between the nickel heater and gold leads and future layers. Again, a low stress deposition method was employed to minimize surface stress.

Step 23. Photolithographic patterning step #7 was performed using SC1827 resist and clear-field mask #7.

Step 24. A wet chemical etch was used to remove excess Si_xN_y. Similar to the first Si_xN_y barrier layer, any excess Si_xN_y functions as a pathway for thermal loss.

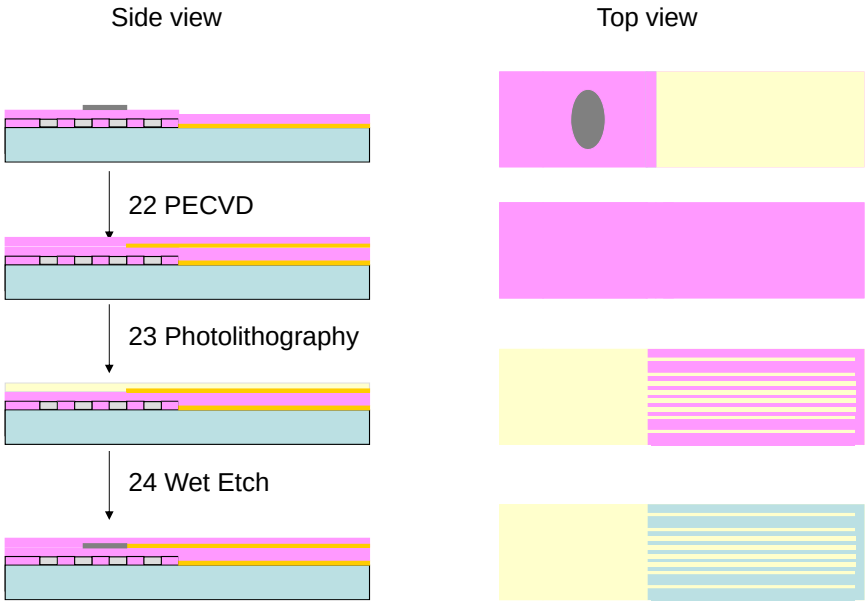

Figure 7. Schematic of the process flow for the deposition of the second silicon nitride barrier layer. Both side and top views are provided.

2.8. Deposition of Gold Bonding Pads (Figure 8)

Step 25. The pattern for the gold bonding pads was created by the openings in photoresist SC1827 and the appropriate clear-field mask #8 onto the Si_xN_y barrier layer.

Step 26. A wet chemical etch was performed to remove Si_xN_y covering the gold bonding pads. The gold deposited in steps photolithography steps #6 and #16 served as the etch stop.

Step 27. Upon etch completion, PVD was carried out using an e-beam metallization tool to produce a smooth film of gold, completing the bonding pads. Gold was the preferred choice for bonding pads because it is easily bonded to other metals and wires.

Step 28. Lift off of the resist removed the excess metal deposited by the PVD process, leaving metal in the desired location.

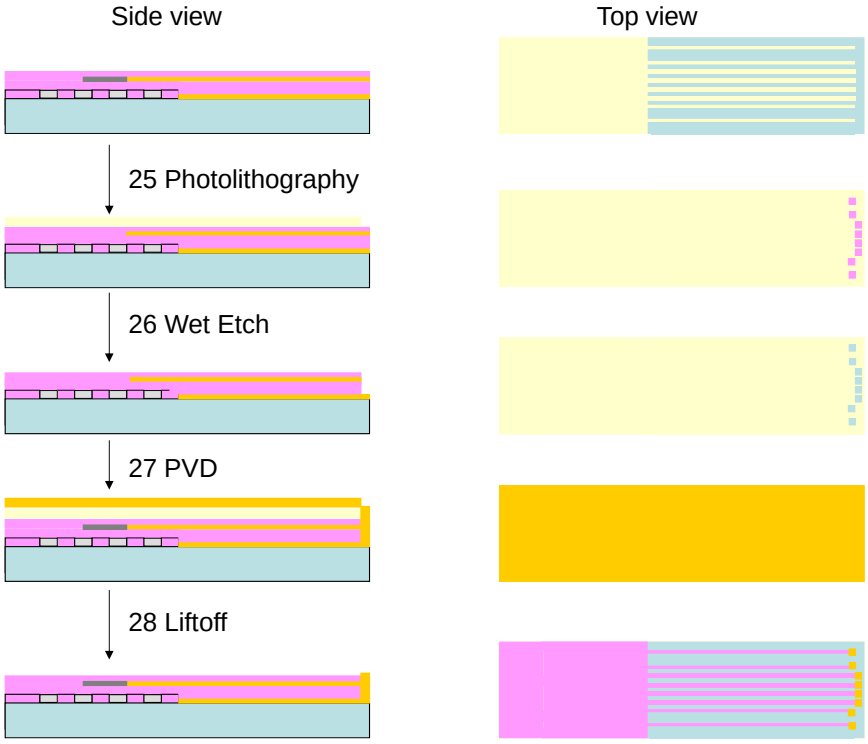

Figure 8. Schematic of the process flow for the deposition of the gold wire bonding pads. Both side and top views are provided.

2.9. Deposition of Metal Oxide Catalyst Layer (Figure 9)

Step 29. The pattern for the metal oxide catalyst was created by the openings in photoresist SC1827 and the appropriate clear-field mask #9.

Step 30. For deposition of the metal oxide catalyst layer an RF sputtering method was employed as opposed to PVD. The area of the metal oxide is identical to the area of the platinum RTD.

Step 31. Lift off of the resist removed the excess metal deposited by the PVD process, leaving metal in the desired location.

Step 32. After deposition of the catalyst layer, a thick layer of photoresist was applied to the topside of the wafer to preserve the devices during shipping, milling, and dicing. The resist layer was easily removed once the diced chips were returned.

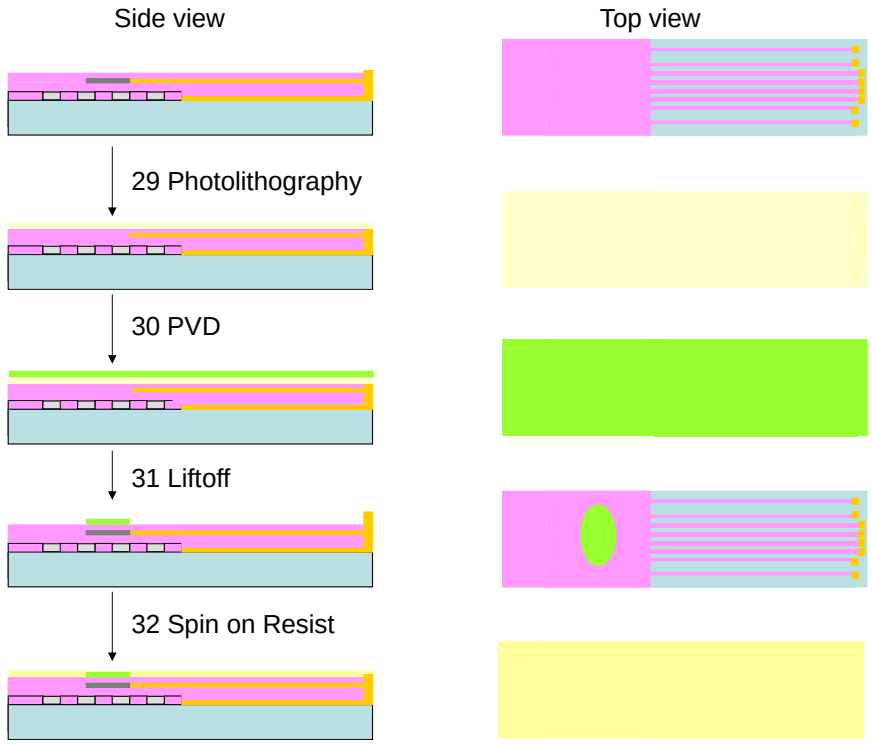

Figure 9. Schematic of the process flow for deposition of the metal oxide catalyst layer by sputtering. Both side and top views are provided.

2.10. Shipping, Dicing, and Wire-bonding (Figure 10)

Step 33. The wafer(s) were shipped to Cidra Technologies, LLC for milling & dicing.

Step 34. Milling was done to thin the device from the end of the serpentine heater out to the end of the cantilever. Thinning results in a significant improvement in device temporal response to analyte gas stream composition.

Step 35. Wire bonding was done in-house onto a specially designed package.

Figure 10. Schematic of process flow for deposition of photoresist protective layer for shipping and dicing. Both a side and top view is provided.

3. Necessary Modifications to the Process Flow for Prototype #1

3.1. Photolithography Processing. Initially photoresist AZ4260 was chosen for the initial Si_xN_y layer patterning. Based on the feature sizes for the Si_xN_y mesas, this resist is not optimal. Instead, photoresist SC1827 was used. This resist was used for all processing steps, including the protective layer prior to shipment after the wafers were completed. In addition, both the developer and stripper were changed accordingly. For the developer, MF-319 and MF-341 were compared and MF-319 was deemed optimal. For the stripper, sonication in acetone proved to be sufficient for removal of excess resist.

Extreme difficulty was encountered during processing for the first metallization step. Multiple steps were taken in an attempt to pinpoint the issue in the process. To verify that there was complete development of the resist, profilometry was employed. An additional process step was added and performed in the RIE. The "Descum" process step aids in the removal of residual resist after developing as well as any other contaminants that may be preventing metal for adhering to the wafer surface. Additionally, a new titanium target was melted to be sure that contamination in the ingot was not responsible for the lack of adhesion. Successful deposition and lift-off was acheived only when pretreatment of the wafer with hexamethylsilazane (HMDS) was intentionally omitted. HMDS is a commonly used covalent linker for photoresist on silicon and gallium arsenide wafers. Based on this discovery, HMDS was not used for any of the metallization process steps.

3.2. Nickel Serpentine Heater Deposition. Upon deposition of nickel using the electron beam evaporator, the wafer was heated to high and the resist baked onto the surface. Excessive cleaning in acetone and numerous Descum runs in the RIE did not remove the residual resist. Because of this, a custom made cooling plate was implemented in order to keep the surface of the wafer cool. Upon deposition of the nickel serpentine using the cooling plate, resist was successfully removed with acetone alone. For all depositions of a high melting temperature metal, the cooling plate was employed to ensure that resist could be removed fully from the surface.

3.3. Etching of the Silicon Nitride Barrier Layers. Originally, the Georgia Tech Cleanroom staff limited the use of the RIE based on metals exposed on the wafer. Potential sputtering of the metal within the chamber would contaminate the tool for the next user. Upon looking into the gases used for the Si_xN_y etch; sputtering of the metals on the surface would not occur. Specifically, fluorine gas is used in the recipe and it will not sputter gold. Therefore, a dry etch could be employed as opposed to the BOE wet etch.

3.4. RTD Deposition. Originally, platinum was to be deposited for the RTD sensing unit based on the thermal properties. The boiling point of platinum is 3825 °C; much higher than the nickel (2732 °C) which previously presented a problem with excessive heating of the wafer. The cooling plate designed for nickel deposition was used to test platinum deposition, but the degree of cooling was not enough to prevent photoresist from baking onto the surface. In addition to the photoresist, platinum was baked onto the wafer. Based on these results, nickel was chosen for the RTD sensing unit instead.

3.5. Annealing. The original protocol called for an annealing step after deposition of wiring to be sure that electrical contacts were made and there weren't any disconnects in the metal layers Annealing was performed in a rapid thermal processor (RTP) which is the tool typically used to heat silicon wafers to a high temperature. Upon performing RTP under nitrogen environment for 2 min at 700 °C, inspection of the wafer post annealing revealed that the Si_xN_y layers were cracked and the surface of the metals were roughened. Figure 11 depicts optical images of the features on the wafer surface. It is clear that an annealing step is not plausible based on the effect the high amount of heat has on the materials on the wafer surface. The purpose of for annealing the materials was to ensure electrical contacts, however resistance measurements obtained without annealing the layers provided good results so this step was removed from the process all together. The substrate heating during the nickel deposition most likely acted as an annealing step and reduced the disconnects within the metal layers.

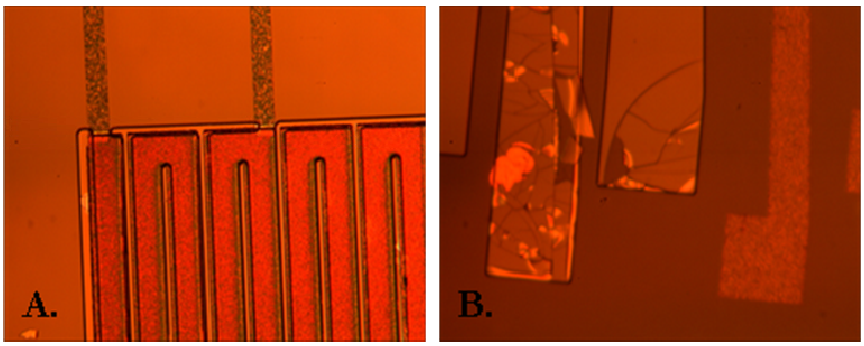

Figure 11. Optical micrographs following RTP annealing. A depicts the heater region where both the gold leads and the nickel serpentine heater. B presents the Si_xN_y mesas following the anneal step. It is clear that all the materials on the wafer surface appear to have been negatively affected by the annealing step.

3.6. Gold Bonding Pads. Wet chemical etching of the Si_xN_y to release the underlying gold for stress relief and to provide regions for the bonding pads was problematic. The etch rate for BOE through Si_xN_y can be as slow as 50 Å/min so the wafer was submerged in the solution and checked periodically to determine if the etch was completed. The BOE would not have affected the underlying gold if the wafer was left in the etchant for too long. Figure 12 shows a wafer following BOE etching for 30 minutes. It is clear in the optical images that the resist partially delaminated during the process exposing regions of the pattern to etchant (see red arrows superimposed on the images). The underlying Ni heater is no longer isolated from the RTD. The fact that the delamination is limited to regions adjacent to patterns suggests that loss of adhesion of the resist is localized and not a result of thermally-induced stress that accompanies the BOE process. If thermal stress or pinhole defects in the resist were the cause of failure during the etch process, we would anticipate more widespread damage. The Georgia Tech Cleanroom staff were consulted on the issue, and permission was granted to perform the etch in the RIE, as the gold would not sputter in the fluorine gas environment.

In addition to a revised etch process for the gold bonding pads, and additional alignment was implemented to be sure gold was deposited precisely in the correct region. Once the Si_xN_y etch was completed, the resist was removed and the wafer was realigned with the same mask. During the etch process, the developed features may have altered slightly in shape and size resulting in gold deposition in unwanted areas. The additional alignment avoids this issue.

3.7. Protective Resist Coating. Originally SU-8 was chosen as the protective coating during shipment and dicing. However, this resist is difficult to remove from a surface without harming the features underneath. Additionally, the resist may put stress on the wafer and possibly cause it to bend. For these

reasons, SC1827 was chosen instead. At a thickness of 2.5 μm, it should provide the necessary protection for shipment and dicing.

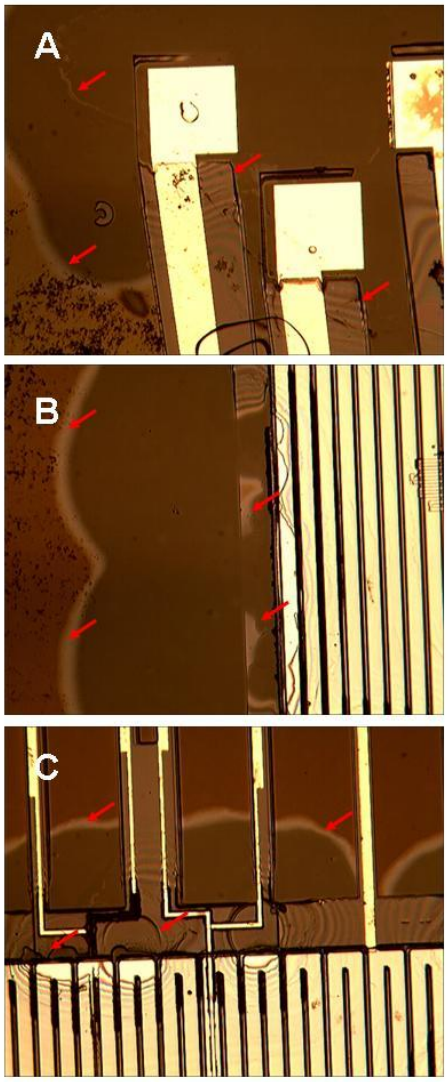

Figure 12. Optical micrographs following BOE. A depicts the area encompassing the wire bonding pads; B depicts area adjacent to Au interconnects; C depicts area adjacent to serpentine heater. Red arrows have been added to emphasize regions where the BOE created defects.

4. Revised Prototype #1 Initial Process Flow

The substrates used were C-axis, 50.8 mm diameter and 300-350 μm thick sapphire wafers purchased from Wafer World, Inc. (West Palm Beach, FL). Wafers were RCA cleaned to remove residual organic and inorganic contaminants from the surface prior to any processing.

For brevity, "photolithography patterning" includes the following process steps: spin-coat photoresist; soft-bake; mask alignment; exposure; hard bake; and develop resist. Photolithography patterning was carried out using a Karl Suss MA-6 Mask Aligner (Suss Microtec, Waterbury Center VT) for all steps. Patterning was completed using Microposit SC 1827 positive resist and Microposit MF®-319 developer (Shipley Company Inc., Marlborough MA). The resist was spun to a thickness of 2.5 μm, followed by a 5 minute soft bake in a 150 °C oven, exposed using a 405 nm UV lamp source on the aligner, developed and hard baked for 10 minutes in 150 °C oven prior to the next step**.**

Table 1. Process parameters used for silicon nitride deposition in the UNAXIS PECVD, silicon nitride etching and O_2 plasma cleaning in the Vision RIE.

Silicon Nitride Deposition Settings	
Heat Exchange	60 °C
Wat Low	250 W
Pressure	1100 Torr
RF Power	60 W
Reflectance	0
DC Bias	7
SiH_4 gas	200 sccm
NH_3 gas	8 sccm
He gas	560 sccm
N_2 gas	150 sccm

Silicon Nitride Etch Settings	
RF Power	350 W
Ar gas	20 sccm
O_2 gas	6 sccm
CHF_3 gas	40 sccm

O2 plasma cleaning Settings	
RF Power	350 W
O_2 gas	50 sccm

4.1. Deposition of Silicon Nitride Mesas for micro-Heater. Initially, 1.05 μm of Si_xN_y was deposited using a Unaxis PECVD (OC Oerlikon Corporation, Pfaffikon, Switzerland). A low-stress recipe was created using the set points and parameters displayed in Table 1. Both helium and nitrogen gases were used to control the level of stress on the sapphire wafer. Since the deposition rate of Si_xN_y in this tool is ~100 nm/min, the deposition was run for 105 minutes to ensure adequate deposition of material (Note: This recipe was used for all Si_xN_y depositions). The thickness and uniformity was verified using a Nanospec 3000 refractometer (Nanometrics, Inc., Milpitas, CA). A total of five measurements were taken for each wafer to evaluate deposit uniformity across the wafer. A plot of the average thicknesses as well as the standard deviation is provided in Figure 13 for a batch of 8 wafers. Patterning step #1 was completed

using the mask pattern presented in Figure 14. Upon completion of

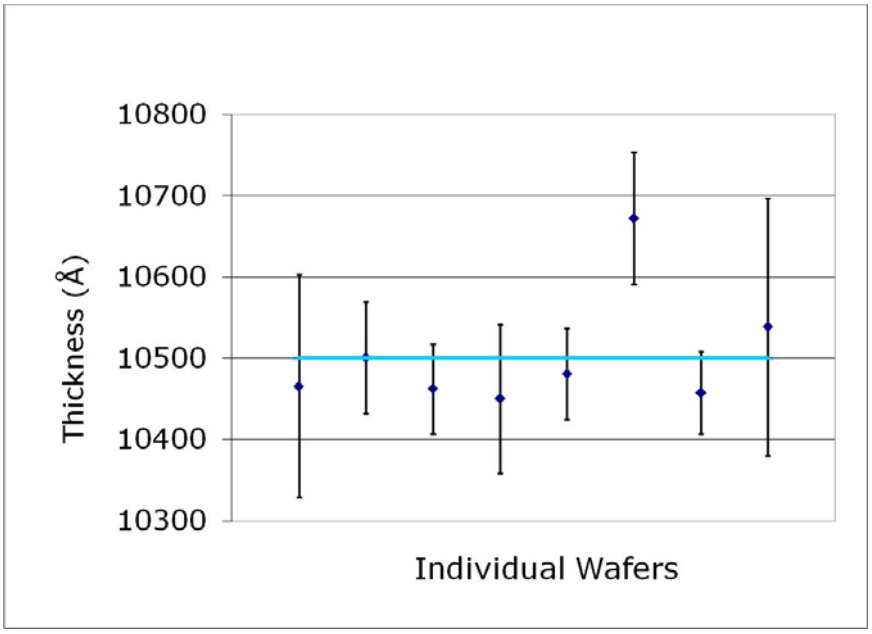

Figure 13. Plot of the average thicknesses after PECVD deposition of silicon nitride using the recipe presented in Table 1. Error bars are included to depict the deviation from the average for a total of 5 measurements. The line represents the thickness expected from the length of deposition.

patterning, Si_xN_y was dry etched in a Vision 320 reactive ion etch (RIE) plasma system (Advanced Vacuum AB, Lomma Sweden) using the parameters presented in Table 1. Since the etch rate in this tool for Si_xN_y is 500 Å/min, a 15 minute etch was required to pattern the SixNy.. This was the tool and recipe used for all Si_xN_y etching. Remaining resist was removed through sonication in acetone for 15 minutes followed by O_2 plasma cleaning in the Vision RIE using the parameters displayed in Table 1. Sonication in acetone followed by O_2 plasma cleaning was used to lift-off remaining resist for all patterning steps unless otherwise noted. The step height of the Si_xN_y was measured using a P15 OF profilometer (KLA Tencor, Milpitas CA) to be 1.05 μm. This profilometer was used to measure all step heights for both deposited and etched layers throughout the process flow. Figure 15 presents optical micrographs of the initial Si_xN_y mesa on the sapphire wafer surface. Images presented include the barriers for the serpentine heater (photolithography step #2), the region for RTD/gold lead connections (photolithography steps #5 and #6), as well as the region where the gold bonding pads was deposited (photolithography step #7).

4.2. Creation of Wiring for micro-Heater. Photolithography patterning step #2 was completed using the process parameters described previously (see Figure 16 for the mask pattern used). After successful patterning, a titanium adhesion layer was deposited at 1 Å/sec (recipe deposition thickness 500 Å) followed by successive deposition of gold at 3 Å/sec (recipe deposition thickness

4000 Å) in a CVC-SC5000 electron beam evaporator (Condensed Vacuum Corp., Rochester NY) at a base deposition pressure of 1 x 10^{-7} Torr

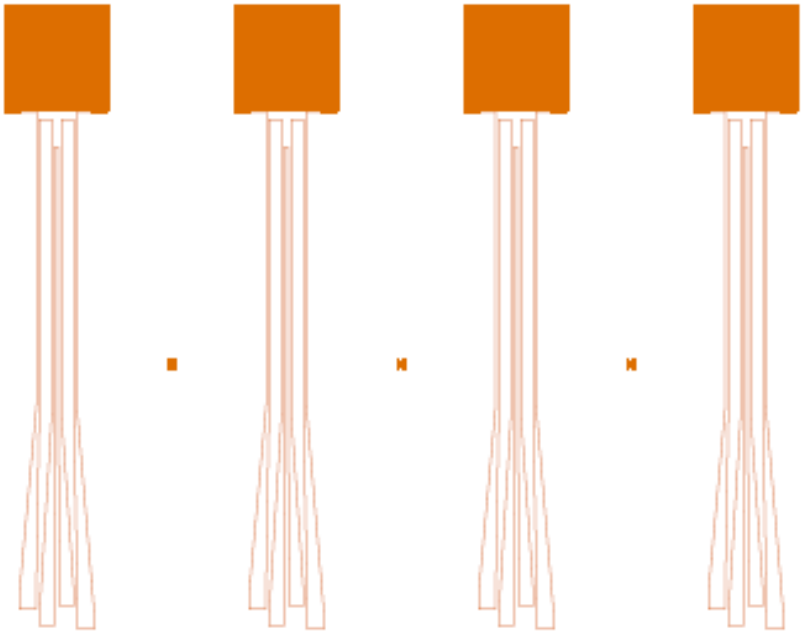

Figure 14. Feature details for a single chip, representative of the mask used during photolithography pattering step #1, deposition of the Si_xN_y mesas.

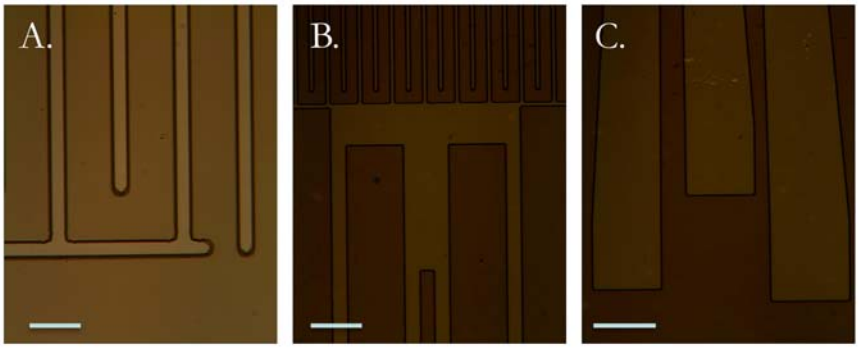

Figure 15. Optical micrographs of the sensor following etching of the silicon nitride to create the heater pattern. A depicts is the heater region barriers, B presnets the region where the RTD connects was deposited in phtolithography step #5, and C depicts where the gold bonding pads was located. The scale bar denotes 50 μm in A and B and 250 μm in C.

(Note: Unless otherwise noted, all metallization steps were carried out in this tool). Excess metal was stripped from the surface using the method previously described. The step heights of each layer were measured to be ~3800 Å. Figure 17 presents optical micrographs of the gold leads following deposition and lift-off.

Both the point of contact with the serpentine heater (photolithography step #3) and the bonding pad regions are included.

Figure 16. Feature details for a single chip, representative of the mask used during photolithography pattering step #2, deposition of the serpentine heater gold leads.

A.4.3. Deposition of Nickel micro-Heater

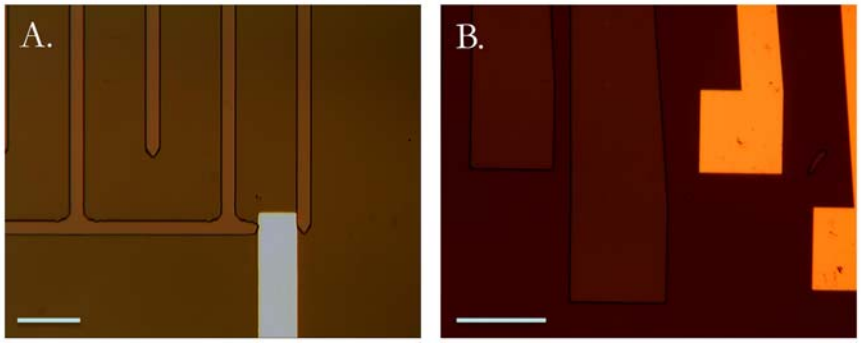

Figure 17. Optical micrographs of the gold serpentine heater leads. A depicts the contact area of one of the leads (white) for the serpentine heater to be deposited between the Si_xN_y (orange). The scale bar depicts 50 μm. B depicts the wire bonding pads at the bottom of the device (orange) as well as the Si_xN_y mesa (brown). The scale bar depicts 250 μm. In both images the dark brown in the base sapphire substrate.

4.3. Deposition of Nickel micro-Heater. Photolithography patterning step #3 was completed using the process parameters described previously (see

Figure 18 for the mask pattern used). After successful patterning, nickel was deposited at 2 Å/sec (recipe deposition thickness 1.1 μm) using a custom fit cooling plate at a base pressure of 1 x 10^{-7} Torr. Excess metal and resist was removed from the surface using the method described previously with an additional 10 minutes of sonication in acetone and

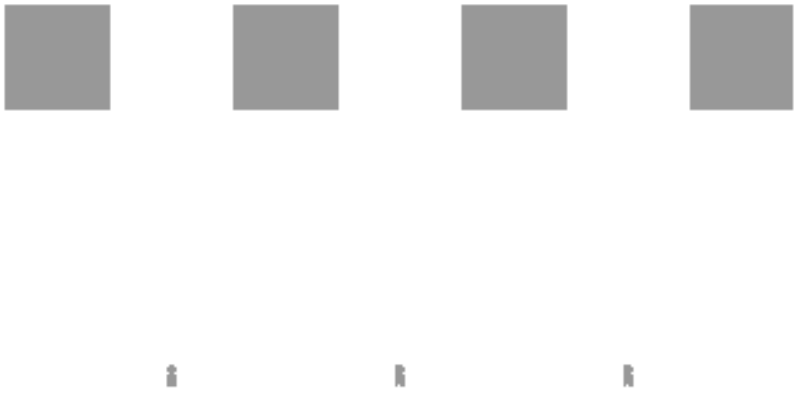

Figure 18. Feature details for a single chip, representative of the mask used during photolithography pattering step #3, deposition of the nickel serpentine heater.

additional 15 minutes of O_2 plasma cleaning. The step height of the nickel serpentine was measured to be 0.928 μm. Resistivity measurements were obtained inside the cleanroon, to verify electrical contact was made between the gold and nickel serpentine. Values ranging from 150 to 200 Ω were measured for both inner and outer gold leads, respectively. Figure 19 presents optical micrographs showing the serpentine heater after deposition of the nickel.

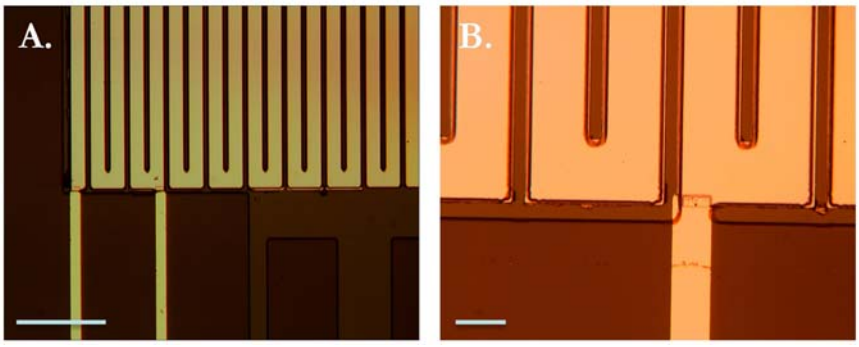

Figure 19. Image A is an optical micrograph depicting a portion of the Ni serpentine heater pattern. Image B is a higher magnification image of the Au/Ni contact made between a gold lead and the serpentine heater. The scale bar in A denotes 250 μm and in B denotes 50 μm.

4.4. Deposition of Silicon Nitride Barrier Layer #1. Using the low stress recipe previously described, 1.05 μm layer of Si_xN_y was deposited over the entire wafer. Photolithography patterning step #4 was completed using the process parameters described previously using the mask pattern presented in Figure 20.

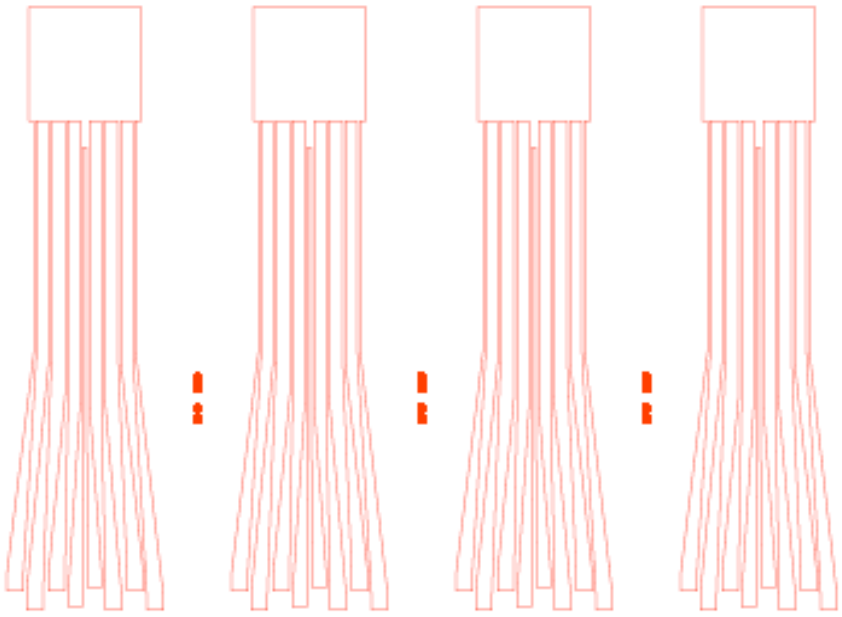

Figure 20. Feature details for a single chip, representative of the mask used during photolithography pattering step #4, deposition of the Si_xN_y barrier layer.

Following patterning, Si_xN_y was etched in the same fashion as the mesas using the Vision RIE. Excess photoresist was stripped from the wafer and the step height was measured to be 1.04 μm. Figure 21 presents optical micrographs of the first Si_xN_y barrier layer. Both the serpentine heater and bonding pad regions are presented.

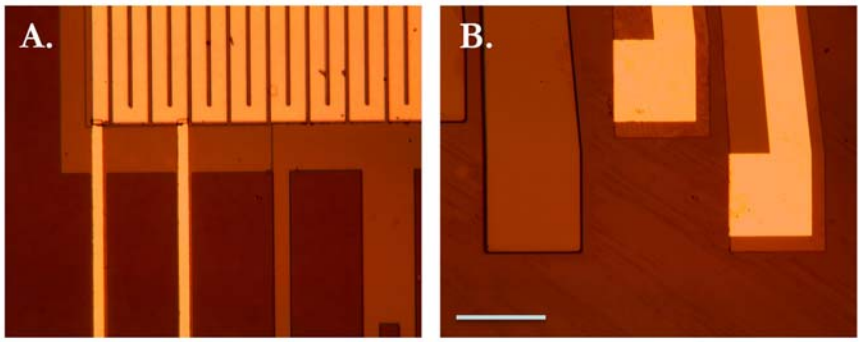

Figure 21. Optical micrographs obtained following deposition of the first silicon nitride barrier layer over the serpentine heater (A) and gold leads (B). In the images, the yellow represents the deposited metals, the orange is the Si_xN_y, and the brown is the sapphire base substrate. The scale bar denotes 250 μm for both images.

4.5. Creation of Wiring for RTD. Photolithography patterning step #5 was carried out using the resist and developer previously described (see Figure 22 for the mask pattern used). Post patterning, a titanium adhesion layer was deposited at 1 Å/sec (recipe deposition thickness 500 Å) followed by successive deposition of gold at 3 Å/sec (recipe deposition thickness 3800 Å) at a base pressure of 1 x 10^6 Torr to create the gold leads required for wiring to the RTD. The excess metal and photoresist were removed from the surface and the step height was measured to be ~3500 Å. Figure 23 presents optical micrographs following deposition of the gold lead connections for the RTD circuit. Both the region where connections with the RTD are to be made and the bonding pads are presented.

4.6. Deposition of Nickel RTD. Photolithography patterning step #6 was carried out using the resist and developer described in previous steps. See Figure 24 for the mask pattern used. After successful patterning, titanium was deposited at 1 Å/sec (recipe deposition thickness 300 Å) followed by successive deposition of nickel at 2 Å/sec (recipe deposition thickness 4000 Å) using a custom made cooling plate at a base pressure of 1 x 10^7 Torr to fabricate the RTD. Excess metal was removed from the surface using the method previously described, with an additional 10 minutes of sonication in acetone. Profilometry results

Figure 22. Feature details for a single chip, representative of the mask used during photolithography pattering step #5, deposition of the wiring for the RTD.

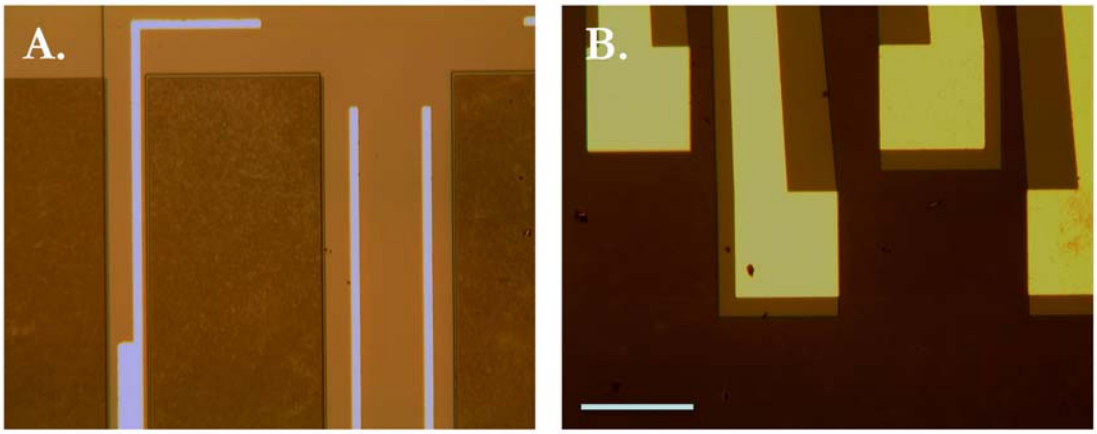

Figure 23. Optical micrograph of the gold leads (A) interconnecting the thermal sensor to the gold bonding pads (B). The scale bar denotes 250 μm for both images.

indicated the RTD thickness was 2500 Å. Figure 25 presents optical micrographs following deposition if the nickel RTD. Two images were overlaid to allow for a high resolution photo of a larger region. Both the RTD as well as the nickel/gold lead connections are presented.

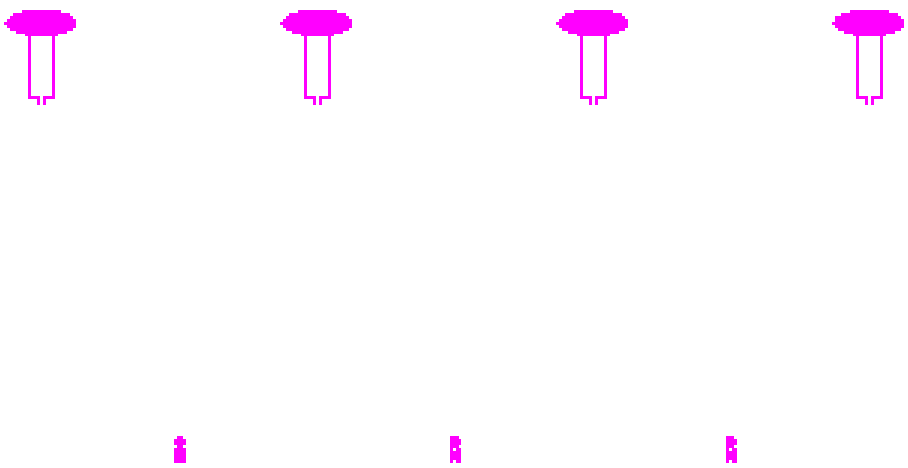

Figure 24. Feature details for a single chip, representative of the mask used during photolithography pattering step #6, deposition of the nickel RTD .

4.7. Deposition of Silicon Nitride Barrier Layer #2. A 1.0 μm thick layer of Si_xN_y was deposited using the same low stress recipe used previously. Upon completion of the deposition, photolithography patterning step #7 was completed (see Figure 20 for the mask pattern used). The Si_xN_y layer was etched in the Vision RIE using the recipe previously described to create the second Si_xN_y barrier layer. Excess photoresist was removed and the step height of this layer was measured to be 1.08 μm. Figure 26 presents optical micrographs of both the serpentine heater and bonding pad regions after deposition of the second Si_xN_y barrier layer.

4.8. Deposition of Gold bonding Pads. Photolithography patterning step #8 was completed using the resist and developer previously described (see Figure 27 for the mask pattern used). Post patterning, Si_xN_y was etched in the Vision RIE. The run was carried out at 15 minute intervals followed by profilometry to monitor the progress of the etch towards the gold leads, for a total of 60 minutes. Upon etch completion the resist was removed using sonication in acetone followed by a 15 minute O_2 plasma clean. The wafer was then re-aligned and patterned for the gold deposition. Gold was deposited at 3 Å/sec (recipe total deposition thickness of 8000 Å) at a base pressure of 1 x 10^{-6} Torr. The excess metal and photoresist were removed from the surface and the thickness of the deposited gold was measured to be 3500 Å, resulting in a total gold bonding pad thickness of 7500 Å for the outer four leads (heater

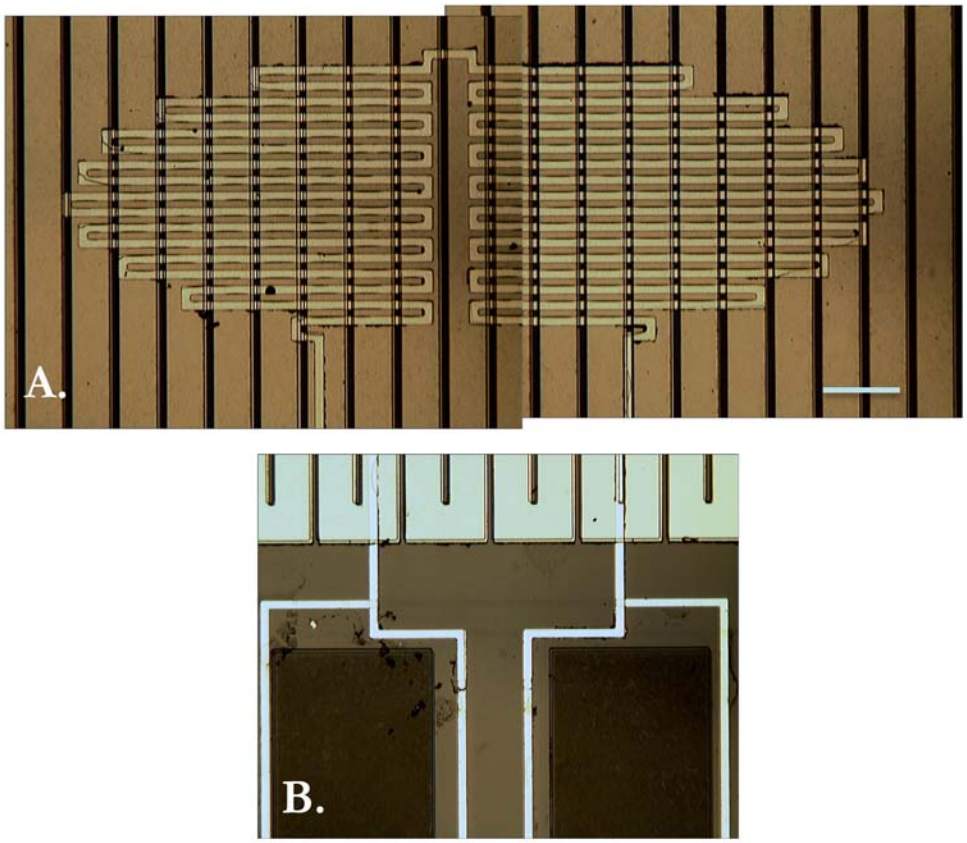

Figure 25. Optical micrograph following deposition of Ni RTD (A). Note that two images are overlaid to provide an image of a wider area of the device. Optical micrograph of the gold and nickel connections for the RTD circuit (B). The scale bare denotes 100 μm for both images.

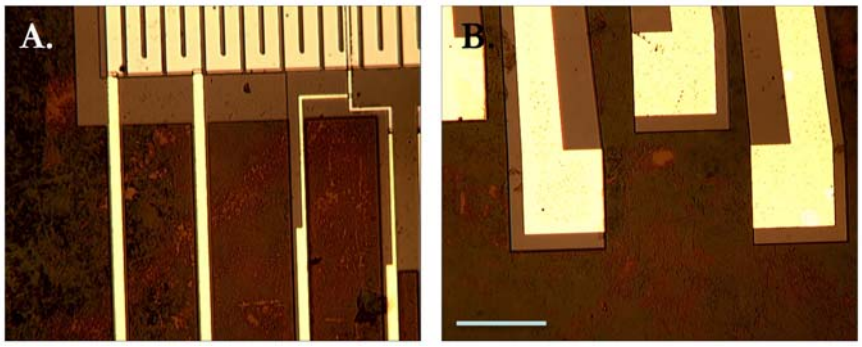

Figure 26. Optical micrograph following deposition of the second silicon nitride barrier layer. A depicts the base of the heater region showing the gold connections leading to the bonding pads shown in The scale bare denotes 250 μm for both images.

connections) and 7000 Å for the inner four leads (RTD sensor connections).

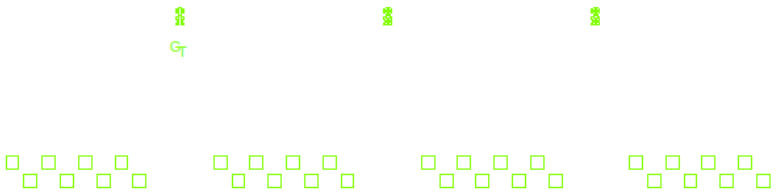

Figure 27. Feature details for a single chip, representative of the mask used during photolithography pattering step #8.

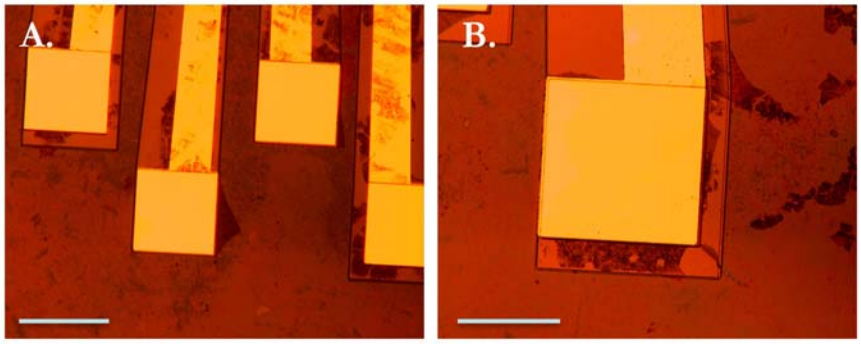

Figure 28. Optical micrographs of the gold bonding pads following dry etch and gold deposition. A depicts the 4 inner pads and B depicts a zoomed in image up of a single bonding pad. The scale bars denote 250 μm in A and 125 μm in

Figure 28 presents optical micrographs of the gold bonding pads after etching away Si_xN_y and depositing gold.

4.9. Deposition of Metal Oxide Active Catalyst – Copper. Photolithography patterning step #9 was completed using the appropriate photoresist and developer previously described (see Figure 29 for the mask pattern used). For the first prototype, a metal oxide catalyst of copper was chosen. Once patterned, the copper catalyst was deposited at 3 Å/sec (final recipe deposition thickness of 4000 Å) at a base deposition pressure of $1x10^{-6}$ Torr. Excess metal and photoresist was stripped from the surface using and the

step height of the catalyst was measured to be 3000 Å. Figure 30 presents an optical micrograph of the copper catalyst post deposition on one of the sensors. Two images were overlaid to allow for a high resolution photo of a larger area.

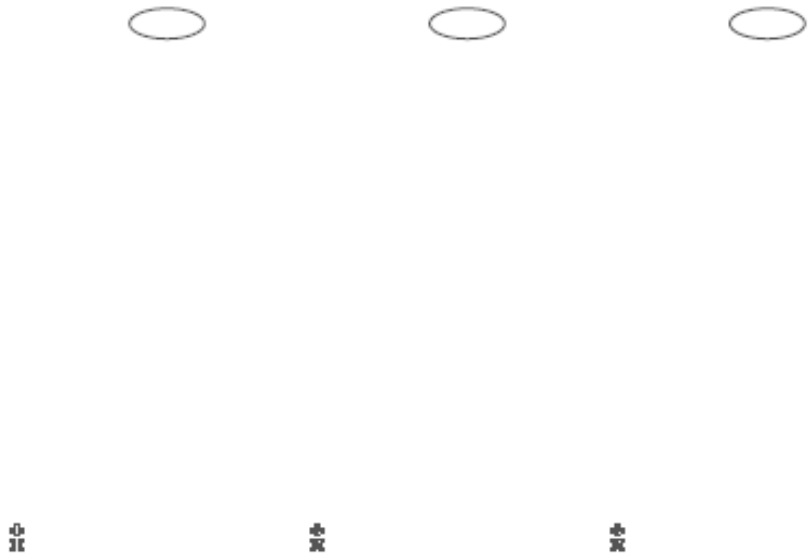

Figure 29. Feature details for a single chip, representative of the mask used during photolithography pattering step #9, deposition of the active metal oxide catalyst (copper).

4.10. Preparation for Shipment. To protect the wafer during shipment and the dicing process, Shipley SC1827 photoresist was spun onto the wafer to a final thickness of ~2.5 μm and hard baked for 20 minutes. A photograph of an entire wafer is presented in Figure 31 prior to shipping the wafer off for dicing. Dicing was carried out to create chips with a single reference sensor and three active catalyst sensors per chip. In addition to cutting the chip out of the wafer, the fingers were thinned.

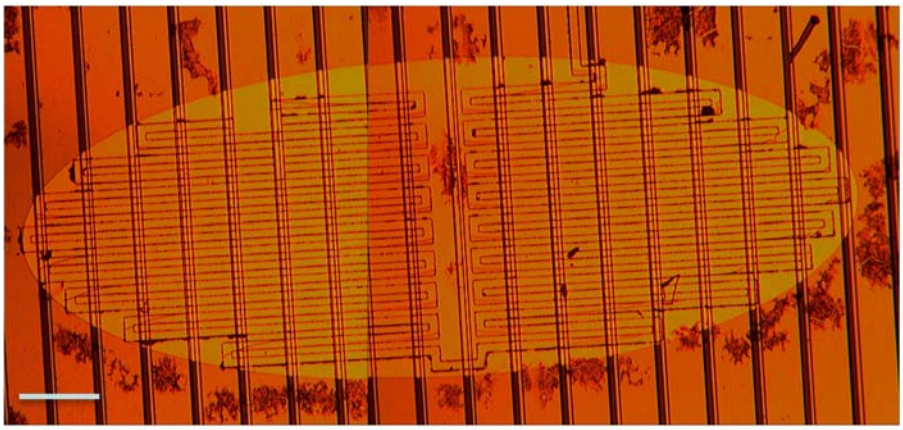

Figure 30. Optical micrograph of the heater RTD following deposition of the metal catalyst. Note that two images are overlaid to provide a photo of a larger region of the device. The copper is the yellow circle and the nickel serpentine RTD can be seen underneath. The scale bar denotes 100 μm.

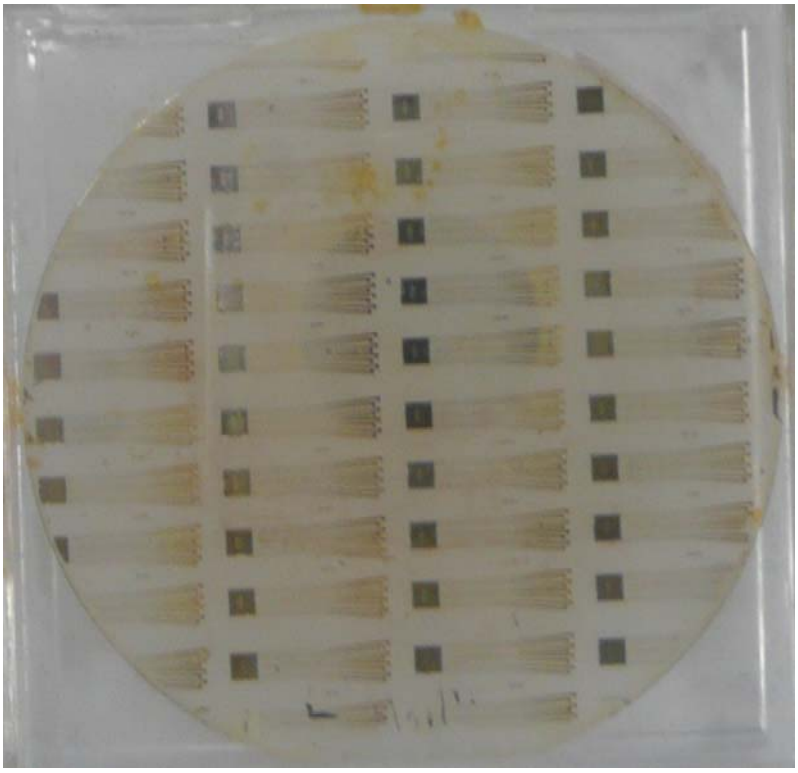

Figure 31. Photograph of a completed wafer. The devices are clearly visible. Since the photograph was taken prior to shipment for dicing, the yellowish color is due to the protective photoresist layer.

5.Prototype #1 Device Testing

Upon examination of the heater units post dicing, the catalyst appears to have been removed during the dicing process. Figure 32 presents optical micrographs of all four heaters on a single chip. Note that the catalyst no longer appears to be present (see Figure 28 for a zoomed in image after successful deposition of the catalyst). The reference heater (a.) unit looks identical to the other 3 sensors (- d.) where catalyst should have been present. Because of this, devices could not be tested for the intended use as a gas sensor. However, to verify that the process provided functional chips in all other aspects, the electrical contacts were examined. Since the lack of catalyst occurred post dicing, part of the dicing process must have removed the catalyst from the surface. Because of this, dicing will not be used for future prototypes.

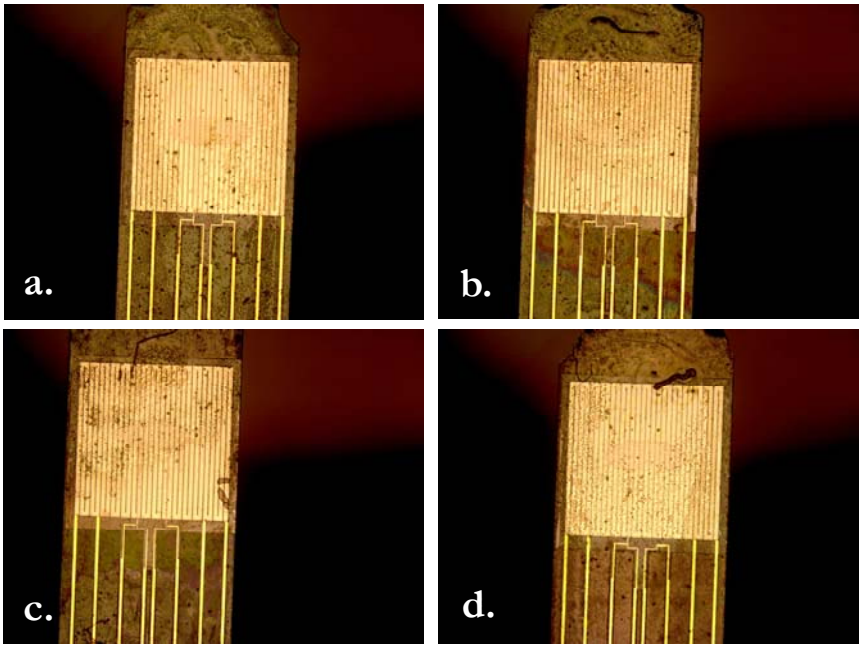

Figure 32. All four heating units on one chip following dicing of the wafer. a.) reference sensor where no catalyst was deposited. No catalyst appears to be present. b, c, d.) Sensors where catalyst was deposited prior to dicing. No catalyst appears to remain (see Figure 9 for an optical micrograph of the catalyst following deposition).

5.1. Resistance Measurements. Once the chips were diced and wire bonded to the package, they were ready to be tested. Prior to carrying out heating experiments, resistance measurements were taken on all circuits to verify that the proper connections were in place after dicing was completed. Table 2 through 4 provides all the measured values for the individual chips. The pin numbers in column 1 correspond to the pin connections outlined in Figure 34. Upon testing, it was noticed that the RTD circuit was not complete. Specifically, the RTD

$Power_{in}$ and RTD $Power_{out}$ addition to RTD $Sense_{in}$ and RTD $Sense_{out}$ were open circuits (see Figure 34).

Table. 2. Resistivity measurements for all Chip 1 after dicing and testing. In the table, the pin number corresponds to the pins outlines in Figure 34 for the wire bonding. An **X** under the resistance reading designates that an open circuit existed.

Chip 1				
Sensor	**Bonding Pad Pin Pairing**		**Resistance Reading (Ω)**	**Circuit**
Reference	61	62	1.1	Heater
Reference	3	4	54.9	Heater
Reference	3	61	107.2	Heater
Reference	4	62	121.1	Heater
Reference	4	61	121	Heater
Reference	3	62	107	Heater
Reference	2	63	**X**	RTD
Reference	1	64	**X**	RTD
Reference	63	64	53.4	RTD
Reference	1	2	66	RTD
Sensor 1	7	15	144.5	Heater
Sensor 1	8	14	117.2	Heater
Sensor 1	7	14	131	Heater
Sensor 1	8	15	131	Heater
Sensor 1	7	8	55.6	Heater
Sensor 1	9	10	48.8	Heater
Sensor 1	12	13	150.4	RTD
Sensor 1	14	15	55.8	RTD
Sensor 1	9	13	**X**	RTD
Sensor 1	10	12	**X**	RTD
Sensor 2	18	25	132	Heater
Sensor 2	19	26	**X**	Heater
Sensor 2	19	25	132	Heater
Sensor 2	18	19	56	Heater
Sensor 2	18	26	**X**	Heater
Sensor 2	20	21	**X**	RTD
Sensor 2	23	24	58.1	RTD
Sensor 2	25	26	**X**	RTD
Sensor 2	20	24	**X**	RTD
Sensor 2	21	23	**X**	RTD
Sensor 3	36	29	149	Heater
Sensor 3	35	30	121	Heater

Table. 2. Continued

Sensor 3	29	30	58.3	Heater
Sensor 3	29	35	135.2	Heater
Sensor 3	30	36	136	Heater
Sensor 3	35	36	59	Heater
Sensor 3	31	32	150.7	RTD
Sensor 3	34	31	**X**	RTD
Sensor 3	33	32	**X**	RTD
Sensor 3	33	34	185	RTD

Based on these results, it was determined that disconnects were present in the RTD serpentine unit. Upon further investigation, it was discovered that the heater region was not flat enough based on the deposition thicknesses for Si_xN_y and the nickel heater; disconnects were occurring at the edges.

Table. 3. Resistivity measurements for all Chip 2 after dicing and testing. In the table, the pin number corresponds to the pins outlines in Figure 34 for the wire bonding. An **X** under the resistance reading designates that an open circuit existed.

Chip 2				
Sensor	**Bonding Pad Pin Pairing**		**Resistance Reading (Ω)**	**Circuit**
Reference	4	61	133	Heater
Reference	3	62	109	Heater
Reference	3	4	49.4	Heater
Reference	61	62	49.6	Heater
Reference	3	61	121	Heater
Reference	4	62	120	Heater
Reference	2	63	**X**	RTD
Reference	1	64	**X**	RTD
Reference	1	2	37.9	RTD
Reference	63	64	**X**	RTD
Sensor 1	7	15	136	Heater
Sensor 1	8	14	111	Heater
Sensor 1	7	8	52.2	Heater
Sensor 1	15	8	124	Heater
Sensor 1	15	14	51	Heater
Sensor 1	7	14	123.3	Heater
Sensor 1	9	13	**X**	RTD
Sensor 1	10	12	**X**	RTD
Sensor 1	9	10	**X**	RTD
Sensor 1	12	13	**X**	RTD
Sensor 2	18	26	138	Heater
Sensor 2	19	25	111	Heater
Sensor 2	18	19	64	Heater
Sensor 2	18	25	125	Heater
Sensor 2	18	19	52	Heater
Sensor 2	19	26	126	Heater
Sensor 2	20	24	**X**	RTD
Sensor 2	21	23	**X**	RTD
Sensor 2	20	21	52	RTD
Sensor 2	23	24	62.1	RTD
Sensor 3	29	36	**X**	Heater
Sensor 3	30	35	**X**	Heater
Sensor 3	30	29	58.6	Heater
Sensor 3	31	32	50	Heater

Table. 3. Continued

Sensor 3	29	35	**X**	Heater
Sensor 3	30	36	**X**	Heater
Sensor 3	31	34	**X**	RTD
Sensor 3	32	33	**X**	RTD
Sensor 3	33	34	**X**	RTD
Sensor 3	35	36	**X**	RTD

Table. 4. Resistivity measurements for all Chip 3 after dicing and testing. In the table, the pin number corresponds to the pins outlines in Figure 34 for the wire bonding. An **X** under the resistance reading designates that an open circuit existed.

Chip 3				
Sensor	**Bonding Pad Pin Pairing**		**Resistance Reading (Ω)**	**Circuit**
Reference	4	61	**X**	Heater
Reference	3	62	**X**	Heater
Reference	3	4	49	Heater
Reference	61	62	**X**	Heater
Reference	3	61	**X**	Heater
Reference	4	62	**X**	Heater
Reference	2	63	**X**	RTD
Reference	1	64	**X**	RTD
Reference	1	2	**X**	RTD
Reference	63	64	**X**	RTD
Sensor 1	7	15	133.2	Heater
Sensor 1	8	14	114.2	Heater
Sensor 1	7	8	50.4	Heater
Sensor 1	15	8	121.3	Heater
Sensor 1	15	14	56	Heater
Sensor 1	7	14	126	Heater
Sensor 1	10	12	**X**	RTD
Sensor 1	9	10	**X**	RTD
Sensor 1	12	13	**X**	RTD
Sensor 2	18	26	**X**	Heater
Sensor 2	19	25	109.4	Heater
Sensor 2	18	19	**X**	Heater
Sensor 2	18	25	**X**	Heater
Sensor 2	18	19	**X**	Heater
Sensor 2	19	26	123.5	Heater
Sensor 2	20	24	**X**	RTD
Sensor 2	21	23	**X**	RTD
Sensor 2	20	21	**X**	RTD
Sensor 2	23	24	**X**	RTD
Sensor 2	25	26	52.4	Heater
Sensor 3	29	36	**X**	Heater
Sensor 3	30	35	**X**	Heater
Sensor 3	30	29	52	Heater
Sensor 3	31	32	73.3	Heater

Table. 4. Continued

Sensor 3	29	35	**X**	Heater
Sensor 3	30	36	**X**	Heater
Sensor 3	31	34	1.3	RTD
Sensor 3	32	33	68	RTD
Sensor 3	33	34	**X**	RTD
Sensor 3	35	36	53.3	RTD

6.Wiring

6.1. Wire Bonding. A total of 3 chips were successfully diced from one wafer. Each diced chip was fixed to a 64 pin side braze package (part # CSB06401) purchased from Spectrum Semiconductor Materials, Inc (San Jose, CA) using a high temperature ceramic epoxy (product # 940HT-1) purchased from Cotronics Corporation (Brooklyn, NY). The epoxy was prepared according to the suppliers instructions. Figure 33 presents photographs of one diced chip attached to the package. The chip was wire bonded to the package using an MEI mode 1204-W hybrid wedge bonder (Marpet Enterprises, Inc) at a temperature of 150 °C using a controlled heat stage purchased from JM Industries (Worcester, MA). Gold wire, with a thickness of 1.5 mil, was used as received from Sigmond Cohn Corporation (Mt Vernon, NY). The heater regions for all sensors were designed to hang over the edge of the package to aid in gas flow during future testing. Figure 34 presents the wiring diagram for a full chip containing a reference sensor and 3 sensors with catalyst. Included on the diagram is also the function of each connection on the device. A more detailed description and schematic is provided in Figure 35 for a single sensor.

After wire bonding was completed, optical images were acquired for all bonding pads. Figure 36 presents an optical micrograph of the eight bonding pads on one of the sensors. It is representative of all four sensors on each chip. Also presented is an optical micrograph of the bonding pads on the package and the gold wire connections.

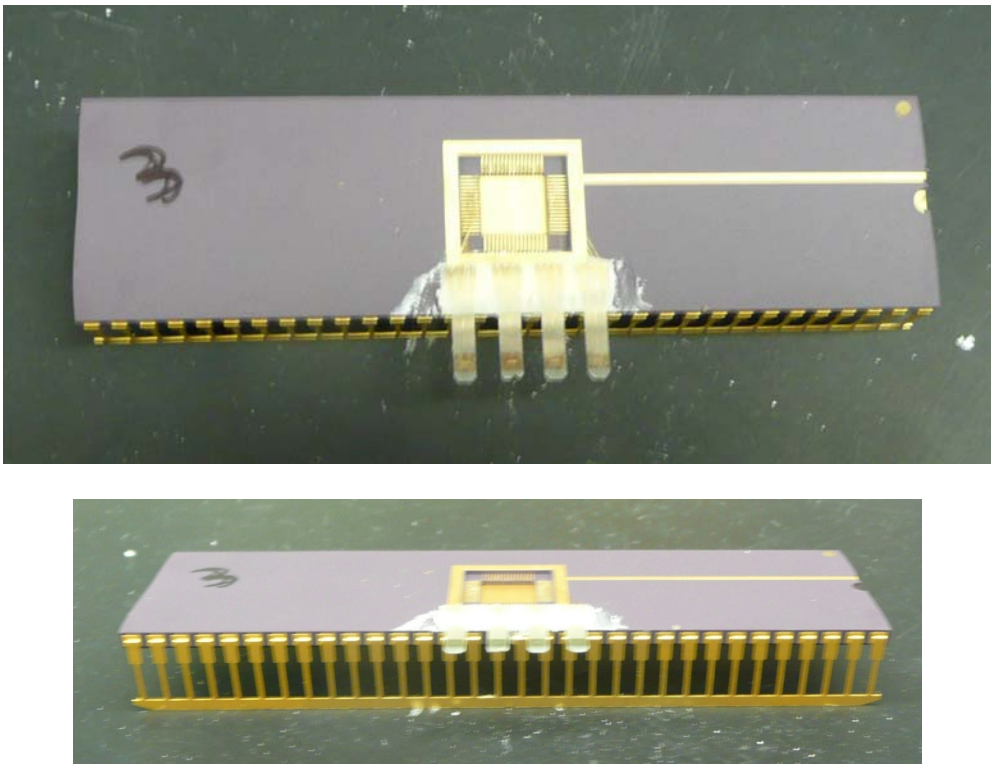

Figure 33. Photographs of a diced chip fixed to the package post wire-bonding. Gold wire was using to bond the pads on the device to the pads on the package. Both a top (upper) and side (lower) view image are provided. The heater regions are hanging off the edge of the package to aid in gas flow during testing. The wiring diagram followed for the bonding is presented in Figure 22.

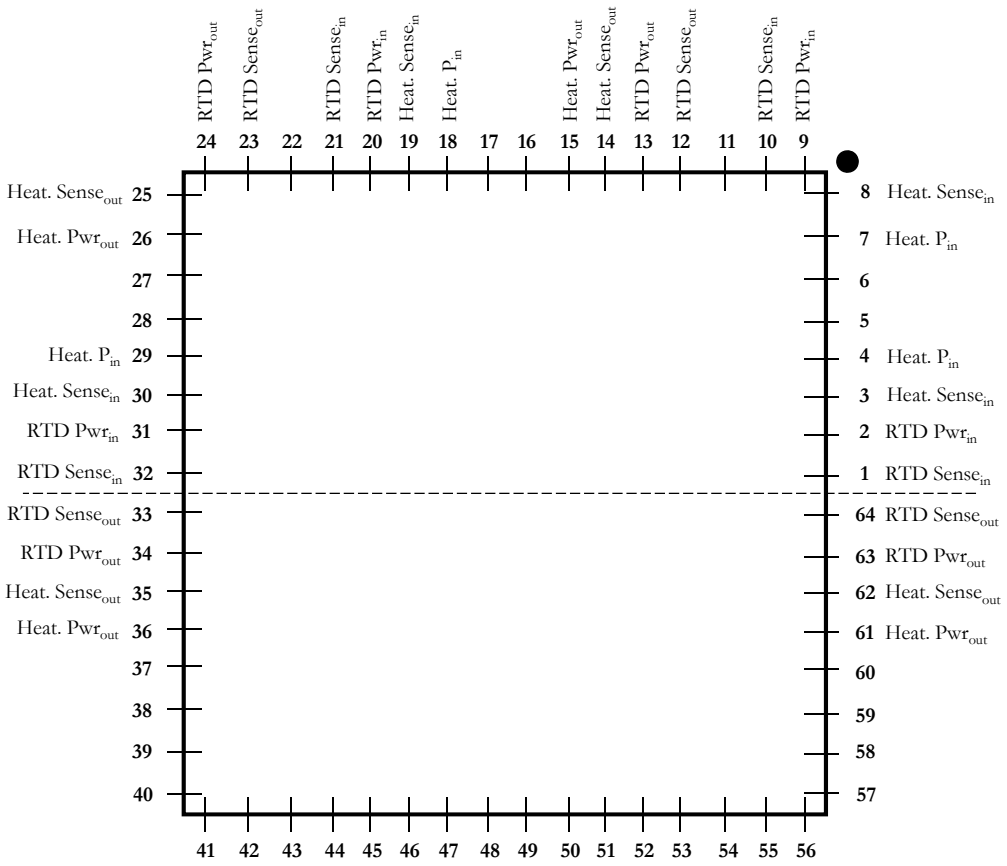

Figure 34. Wiring diagram used for bonding. Bonding pins with a label next to them were used. All others were not connected. Pins 64-4 were connected to the reference sensor, pins 7-10 and 12-15 were connected to sensor #1, pins 18-21 and 23-26 were connected to sensor #2, and pins 29-36 were connected to sensor #3. The labels at the pins are representative of the function of that bonding pin on the device. A more detailed image is presented in Figure 33.

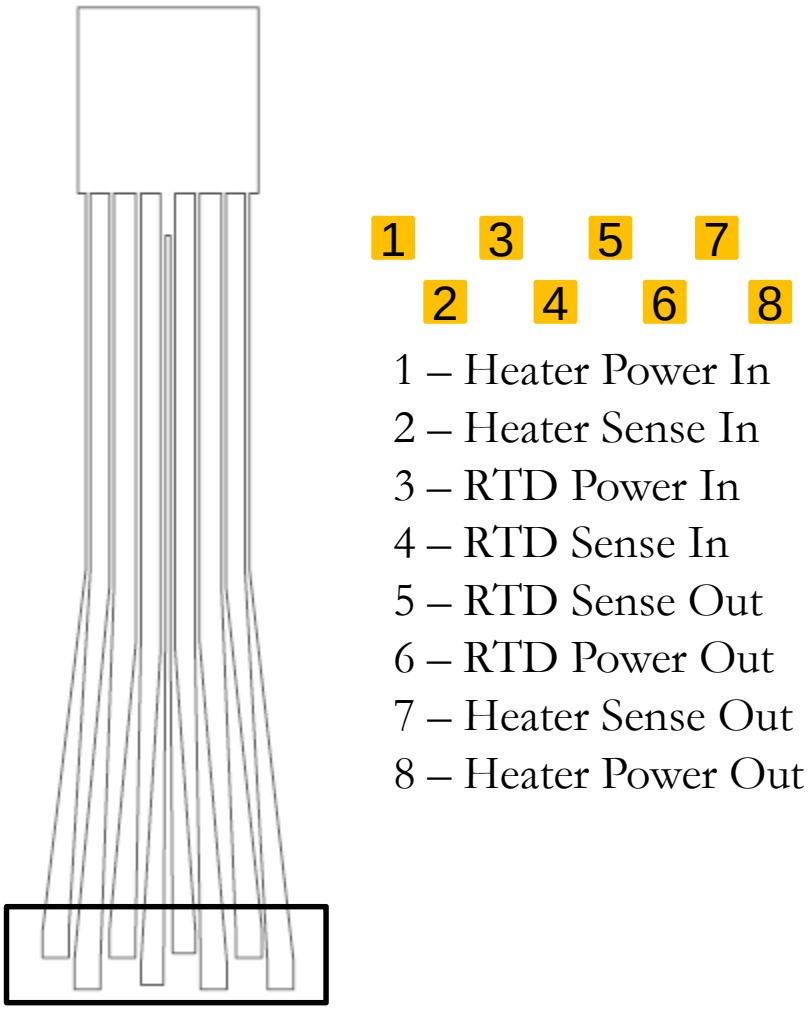

Figure 35. Schematic of one sensor on a chip. Rectangle depicts the region shown in detail on the right. Bonding pads 1-8 are labeled and the corresponding function on the chip is provided. Pads 1, 2, 7, and 8 correspond to the heating unit circuit and pads 3 - 6 correspond to the RTD circuit.

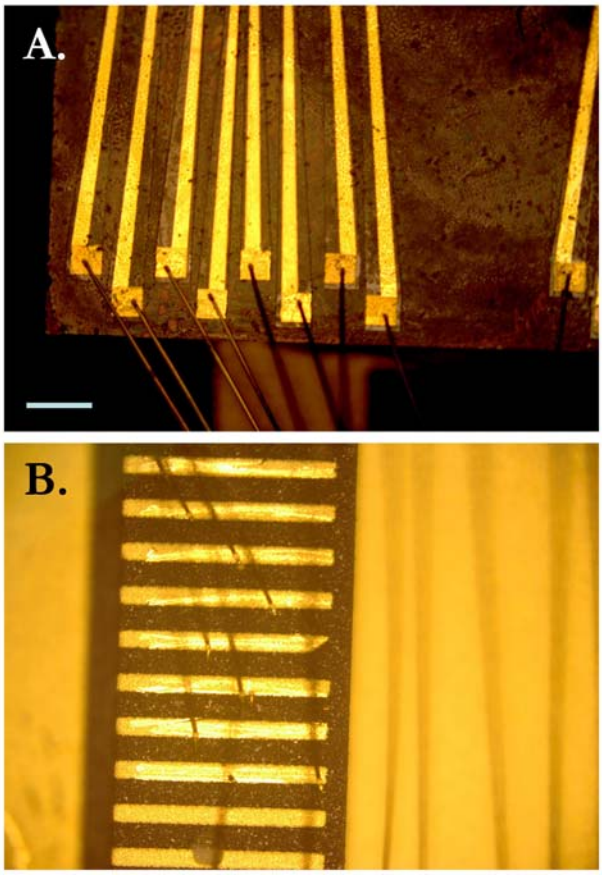

Figure 36. A presents the eight gold bonding pads for the reference sensor on Chip 1. Also presented in B are the bonding pads on the package. Scratches on the bonding pads were to roughen the surface to help make a better wire connection. The scale bar denotes 500 μm for both images.

6.2. Creation of the Wiring Board. Upon completion of functional sensors, the chip was ready for gas testing. In preparation for this, a board was wired to connect 4 RJ-45's (one corresponding to each sensor on the chip) to the 64 pin package. RJ-45's were purchased from Winford Engineering (product #PBC8P8C) and were fixed to breadboard adaptors. Each RJ-45 was then connected to a detector for monitoring the changes in resistance with heating over the heater and RTD units. For ease of use, a ZIF DIP socket was purchased from Linear Sales (part #264-4493-00-0602J) and wired to the board so that the same set-up could be used with multiple devices. Figures A.37 as well as A.38 present photographs of the completed board. Specifically, Figure 37 presents a top view showing the DIP socket and the RJ-45's lined up and Figure 38 presents the bottom view of the twisted pair wiring from the socket pins to the RJ-45's pins.

6.3. Creation of a Test Circuit.

To assess the wiring of the circuit board prior to device testing, a test circuit was created to verify that the correct connections were made. The circuit consisted of a series of resistors (10 Ω) and light bulbs (MB-1829) to test the heating and the RTD units, respectively. These were soldered in pairs, corresponding to the functions outlined in Figure 35. The wiring diagram for the test circuit is provided in Figure 37. Due to space limitations during creation of the test circuit, pins used are not all in a row. Spaces needed to be included between resistor and light bulb pairs. This can be seen in the side view of the test circuit provided in Figure 38. Also presented in Figure 38 are the top and bottom views showing the soldering in more detail.

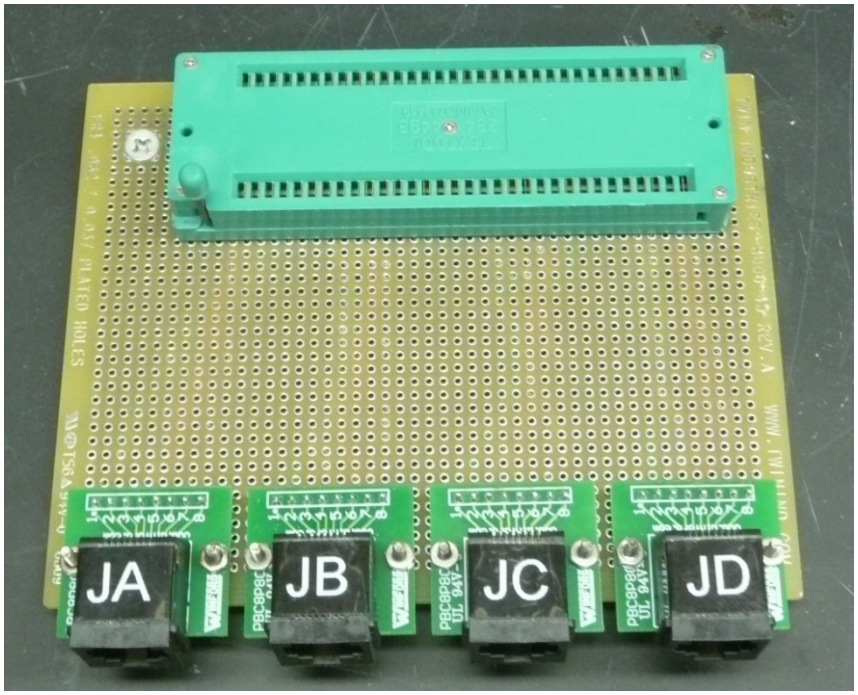

Figure 37. Photograph showing the 4 RJ-45's as well as the 64 pin ZIF DIP socket. Each RJ-45 is connected to a specially designed box changes in resistance are measured. The socket was implemented to allow for multiple chips to be tested without creating a board for each. The wiring from the socket to the RJ-45's is presented in Figure 40.

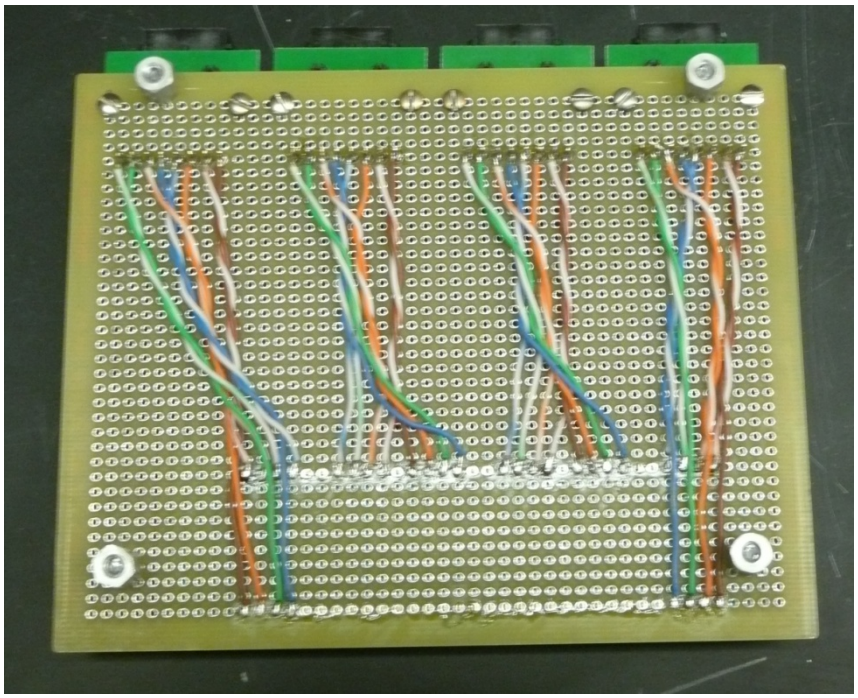

Figure 38. A photograph showing the wiring from the socket (bottom of the image) to the RJ'45's (top of the image). Each RJ-45 corresponds to a different sensor on the fabricated ships. The packages pin assignments by sensor are depicted in Figure 32 and the socket pin assignments are designated in Figure 37.

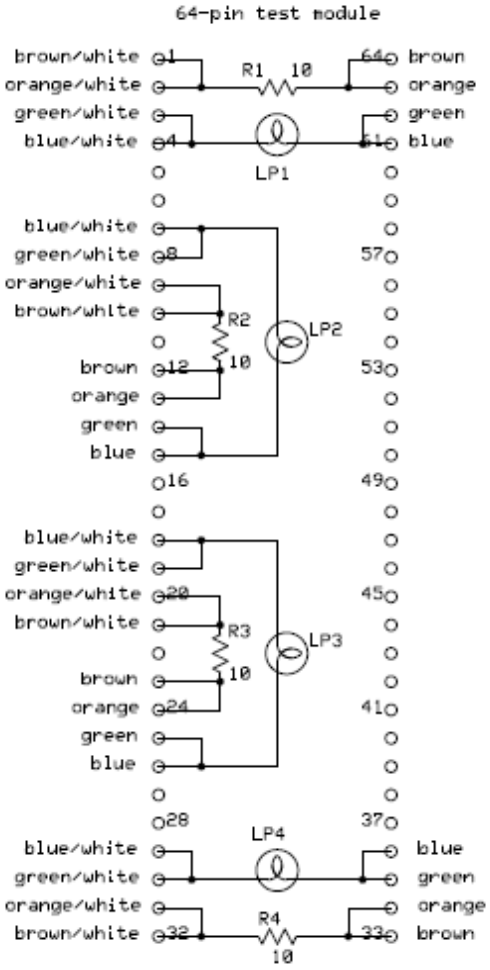

Figure 39. Schematic showing the pin layout for the test circuit and where resistors and light bulbs were positioned. Also shown is the spacing required due to the space limitations of the package. Each pin on this image corresponds to the wiring diagram presented in Figure 34.

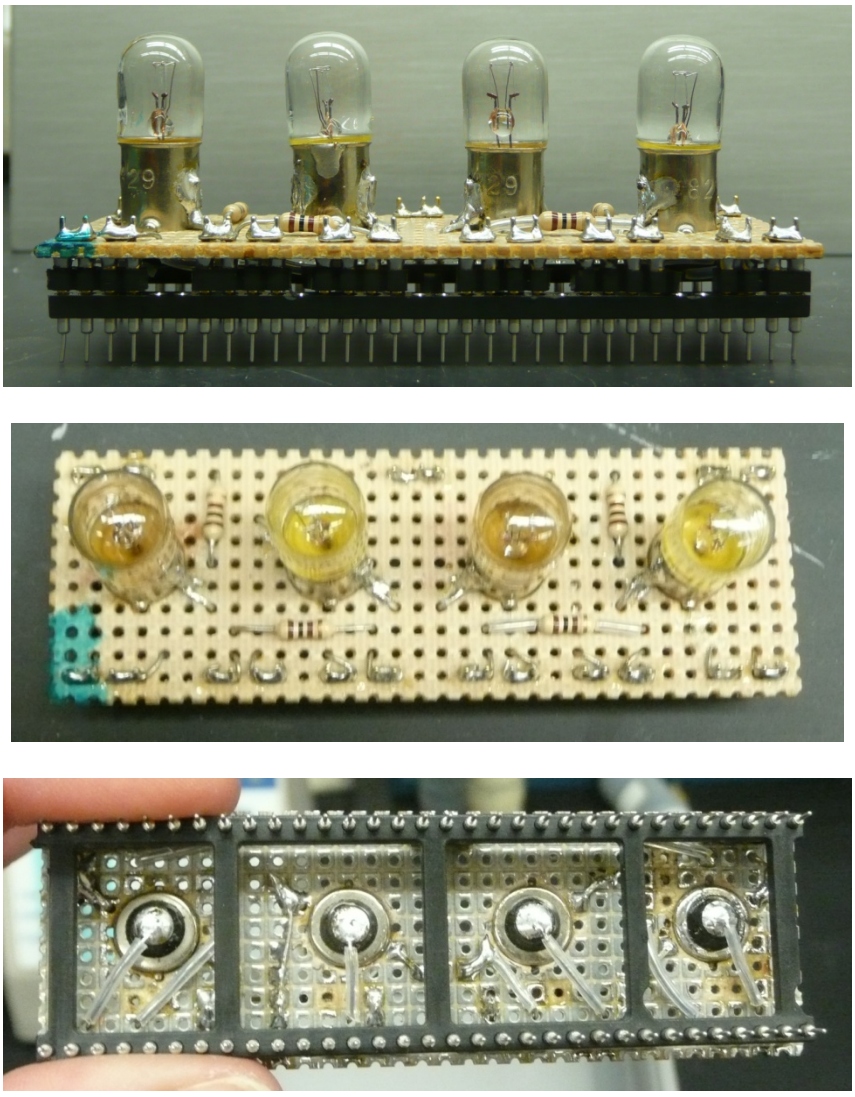

Figure 40. Photographs of the test circuit created to test the connections on the board prior to experimentation with the sensor chips. The side view shows the resistors and light bulbs as well as the spacing created on the 64 pin socket. The middle and bottom image show additional details including the soldered connections (bottom image).

7. Prototype #2 Initial Process Flow

Upon careful consideration of the issues and results obtained using sapphire as the base substrate for the sensor, a decision was made to move to a silicon wafer in hopes of creating a functional sensor. In doing so, a few design changes were made. The process flow for prototype #2 is provided below.

7.1. Deposition of Silicon Nitride Mesas for micro-Heater. Deposition and etching of the Si_xN_y mesa was performed in the same manner as

prototype #1. Photolithography patterning step #1 was completed using the same parameters described in section 4.1 in this report (see Figure 14 for the mask pattern used).

7.2. Creation of Wiring for micro-Heater. Photolithography patterning step #2 was completed using the same process parameters described in section 4.2 of this report (see Figure 16 for the mask pattern used).

7.3. Deposition of Nickel micro-Heater. Photolithography patterning step #3 was completed using the process parameters described in section 4.3 in this report (see Figure 18 for the mask pattern used).

7.4. Deposition of Silicon Nitride Barrier Layer #1. The same low stress recipe previously described in this report was used to deposit Si_xN_y over the entire wafer. The barrier layer mask was altered to add additional alignment marks for the final process step, a silicon wafer etch. Figure 41 presents the new mask pattern for a single chip. The silicon wafer etch is to be carried out using a Bosch process in an ICP where metal may not be exposed during the process. For this reason, the alignment mark had to be created using Si_xN_y. Photolithography patterning step #4 was completed using the process parameters described in the section 4.4.

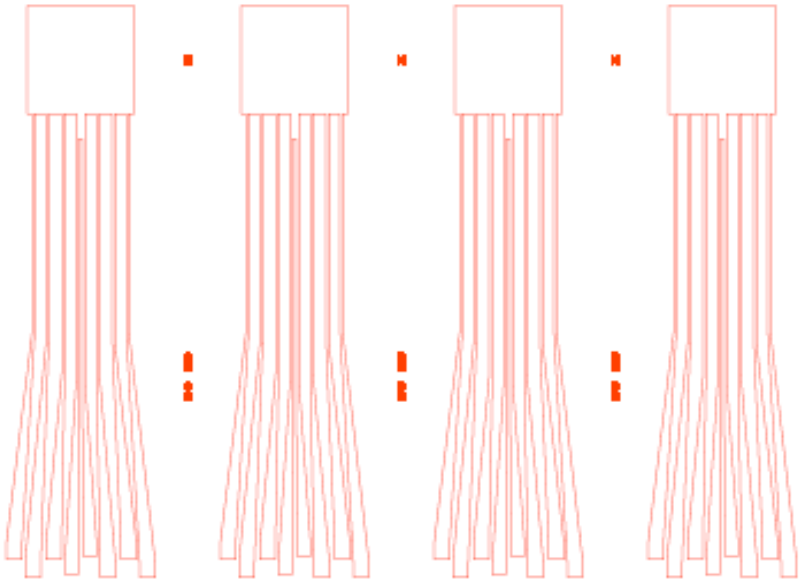

Figure 41. Feature details for a single chip, representative of the new mask made to be used during photolithography patterning step #4 and #7. Alignment marks now exist for the final processing step, a silicon etch.

7.5. Creation of Wiring for RTD. Photolithography patterning step #5 was completed using the process parameters described in section 4.5 of this report (see Figure 22 for the mask pattern used).

7.6. Deposition of Nickel RTD. To correct for the disconnects in the RTD described in section 5.1 of this report, nickel deposition for prototype #2 was sputtered onto the entire wafer surface and etched back using 30% Ferric (III) Chloride. In doing so, the metal will coat all areas of the uneven surface, eliminating disconnects. A new schematic for the RTD deposition process is presented in Figure 42. This was the new photolithography step #6. The same mask presented in Figure 24 was used.

7.7. Deposition of Silicon Nitride Barrier Layer #2. The same low stress recipe previously described in this report was used to deposit Si_xN_y over the entire wafer. Photolithography patterning step #7 was completed using the same process parameters described in section 4.7 of this report. Figure 41 presents the new mask pattern for a single chip. It should be noted that this mask photolithography steps #4 and #7 will still use the same mask.

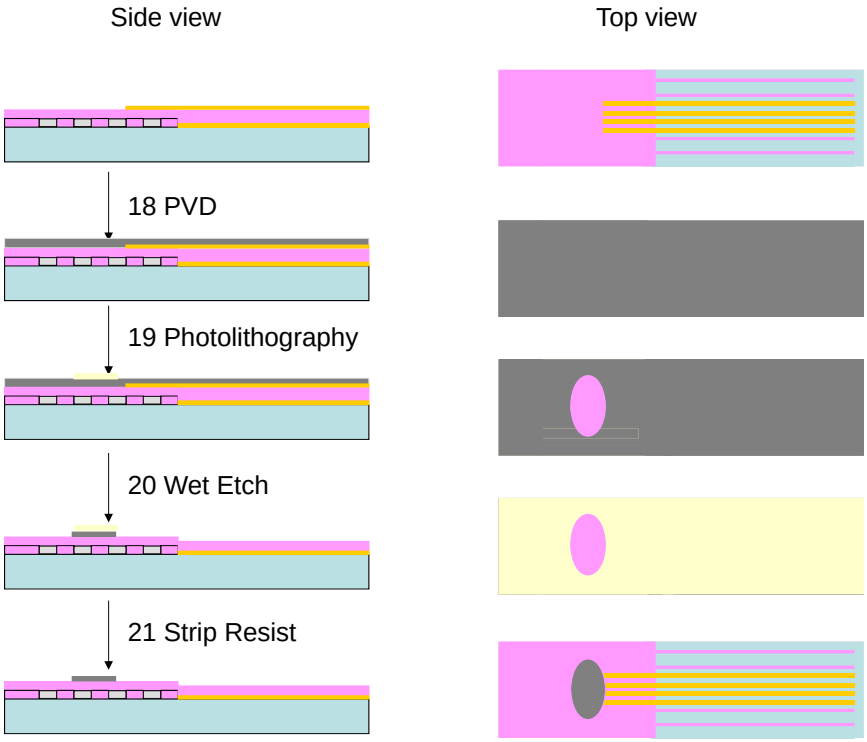

Figure 42. Schematic of the process flow for creation of the RTD sensing element for prototype #2. Both a side and top view is provided.

Figure 43. Feature details for a single chip, representative of the new mask made to be used during photolithography patterning step #9. Two reference and 2 catalyst sensors now exist on each fabricated chip.

7.8. Deposition of Gold bonding Pads. Photolithography patterning step #8 was completed using the process steps described in section 4.8 of this report. See Figure 27 for the mask pattern used.

7.9. Deposition of Metal Oxide Active Catalyst - Cu, Ni and Ti. Photolithography patterning step #9 was completed using a new mask, presented in Figure 43. The metal catalyst deposition was re-designed to account for the possibility that some sensors on a chip may not be fully functional. Instead of a single reference and 3 active catalyst sensors, there was two of each in an alternating pattern. The process steps described in section 4.9 of this report will remain the same for photolithography step #9. For the first prototype, a metal oxide catalyst of copper was chosen. This metal was used again in addition to nickel and titanium, all on separate wafers.

7.10. Silicon Wafer Etch. An additional process step has been added for prototype #2 for release of the parts from the wafer. Due to the issues encountered with dicing the wafer, an etch was employed through the entire silicon wafer. The silicon wafer etch is to be carried out using a Bosch process in the PECVD-ICP. The shape and design of the chip will remain the same as the diced sapphire chip for prototype #1; however the finger region was slightly shorter to account for the inability of the silicon etch to thin the end of the fingers. The mask features for a single chip is presented in Figure 44. All other steps post fabrication such as device testing and wiring will remain the same. Presented in Figure 45 is a schematic for a single chip post etching with the features included. The blue ovals represent the metal oxide atop the heater region

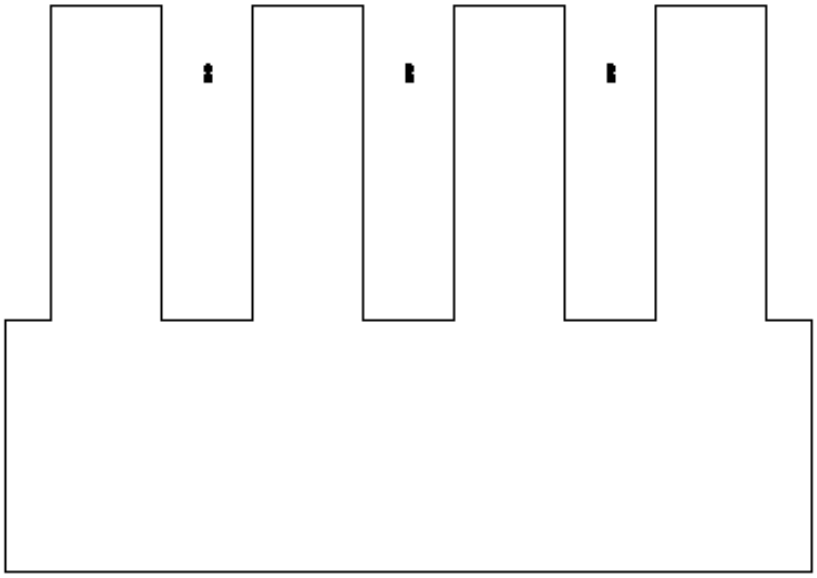

Figure 44. Feature details for a single chip, representative of the new mask made to be used during photolithography patterning step #10. A complete etch of the silicon wafer is to be performed to create the chips instead of having them diced.

represented by a grey square. The black lines represent the gold lead connections for both the heater and RTD sensing unit. It should be noted that the spacing is not drawn to scale. Also included are the gold bonding pads at the base of the gold leads in a staggered patter, represented by the green squares.

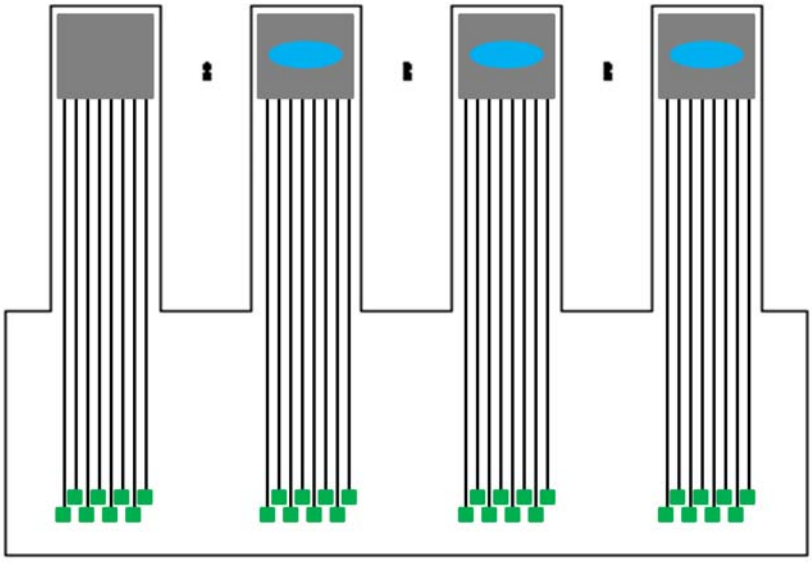

Figure 45. Schematic of a completed chip with three sensing units and one reference. The grey boxes represent the heater nit, the blue ovals represent the metal oxide catalyst atop the RTD sending unit, the black lines represent the gold lead connections for the heater and RTD, and the green squares represent the gold bonding pads.

8. Attempted Fabrication of Prototype #2.

Due to the pending graduation of the student working on this project (Nicole Marotta) and the lack of success in creating functioning devices, the decision was made to hire the process engineers in the Georgia Tech Microelectronics Center to fabricate prototype #2. Mikkel Thomas and Dr. Hang Chen were brought onboard to review the entire process flow and carryout fabrication. Following their review and extensive discussion, fabrication commenced with two notable modifications: 1) each nickel layer was deposited by sputtering rather than e-beam evaporation, in part, because of the backlog on the tool required for the e-beam deposition; 2) over deposition was deliberately performed and a wet etch technique was used to remove excess metal. This approach was used to minimize disconnects along the serpentine temperature sensing lines. It turned out that over-sputtering and etching back technique for the 1 μm thick nickel produced sufficient stress in the gold and nitride patterns that resulted in their lift-off from the wafer. The fabrication process was restarted from the beginning. On this attempt, a Ti adhesion layer was inadvertently omitted from the nickel deposition step. During lift-out, delamination of the nickel heater lines resulted. At this point, the term of the contract had expired. A request by the P.I. to grant a no-

cost extension to continue pursuit of the fabrication was denied by Sensor Tech. Given the repeated failures in manufacture of the devices, this decision was appropriate.