DESIGN OF HIGH-ISOLATION AND WIDEBAND RF SWITCHES IN SIGE BICMOS TECHNOLOGY FOR RADAR APPLICATIONS

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Adilson S. Cardoso

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DESIGN OF HIGH-ISOLATION AND WIDEBAND RF SWITCHES IN SIGE BICMOS TECHNOLOGY FOR RADAR APPLICATIONS

Approved by:

Dr. John D. Cressler
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Ioannis Papapolymerou
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Jeffrey Alan Davis
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Date Approved: April 2nd, 2012

To my Lord and Savior, Jesus Christ

Whose unconditional love,

and blessings has enabled me to complete this work.

"Proverbs 3:5-6"

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SUMMARY

The objective of this thesis is to present the design procedure, simulation, and measurement results for Radio Frequency (RF) switches in 130 nm Silicon Germanium (SiGe) BiCMOS process technology. RF switches are an essential building block in several applications, including tactical radar systems, satellite communications, automotive radars, wireless communications, radio astronomy, and various instrumentation systems. For many of these applications the circuits have to operate reliably under extreme operating conditions, including conditions outside the domain of commercial military specifications. To the best of the author's knowledge, the effects of cryogenic temperature on the performance of RF switches will be investigated for the first time in this work. The novelty of this work lies in the design of new topologies for a ultrahigh-isolation single-pole, single-throw (SPST) and a single pole, four-throw (SP4T) CMOS switch; that was designed primarily for multiband microwave radar systems and to study of the effects of cryogenic temperature on these circuits and devices.

The advantages of a BiCMOS technology process in the context of extreme environment applications are presented in Chapter 1. Chapter 2 provides a brief overview of the operating regimes of a Field Effect Transistors (FETs); followed by the design procedure of a SPST switch as the building block for the SP4T switch. The measured room temperature performance metrics of the switches are discussed, and the chapter concludes with a comparison with other previous works. In Chapter 3, the measured results at cryogenic temperatures are presented and analyzed. Both DC and Scattering parameters (S-parameters) of bulk and Triple-Well FET devices are first presented to aid in the analysis of the observed effects for the SPST and SP4T results.

This is followed by the description of a measurement procedure using an open cycle cryogenic station that provides a more accurate estimate of power handling capability (P_{1dB}) of the switches at cryogenic temperatures. Finally, Chapter 4 summarizes the results attained and the relevance of this work for extreme environment applications, and provides recommendations for future studies on of RF switches in this area.

CHAPTER I

INTRODUCTION

Silicon (Si) based semiconductor devices have fueled the "communication revolution"[4] for the last three decades. However, as the demand for faster, denser, and cheaper integrated systems continues to grow, the physical scaling limits of Si devices is fast approaching [5], warranting new viable and cost effective solutions. A growing concern with the Si based processes is the ability to efficiently support integration and the ever evolving system functionalities (e.g., digital, RF, analog) using the same substrate while meeting all the system design requirements. Generally, communication systems will have different design constraints for the various functional blocks, and these constraints translates to different trade-offs at the device, circuit, and system level. Thus, the need to develop new process technologies that satisfies the "one-technology-fits-all" criterion [5] has become very attractive to the semiconductor industry. Ideally, such process needs to be able to simultaneously support all the trade-offs required in circuit designs ranging from digital, to analog, and RF [5].

Silicon Germanium (SiGe) BiCMOS technology provides a viable and cost effective solution for the aforementioned concerns. BiCMOS technology is a combination of both bipolar and CMOS technologies [6]. Recently, several process technologies are integrating basic microelectromechanical (MEMS) blocks (i.e., capacitive RF switches) into existing BiCMOS processes [7] to improve their capabilities. The underlying concept of BiCMOS technology is to take advantage of maturity of Si processing to manufacture high quality CMOS transistors while leveraging the bandgap-engineered SiGe Heterojunction Bipolar Transistors (HBT) to a platform that is suitable for a

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variety of system-on-chip (SOC) application, including extreme environment opera-tion (i.e., cryogenic temperature, radiation-rich conditions). This work investigates the use of third generation BiCMOS (IBM 8HP) technology to design n-channel Field Effect Transistors (nFET) based wideband high-isolation RF switches. The main ad-vantage of using FET over Heterojunction Bipolar Transistors (HBTs) is to achieve low dc power consumption, high isolation, moderate linearity and insertion loss.

RF switches are an essential building block for applications in several arenas, including tactical radar systems, automotive radar, satellite communications, wireless communications, and various instrumentation systems [8]. Some of these applications are moving towards a multiband architecture as system specifications grow more stringent. A relevant example can be found in the wireless communication industry's adoption of multiband-multimode (MMMB) systems due to increase in application demands [9]. Subsequently, the design requirements for many RF communication sub-blocks are also shifting towards multiband designs. An example of a theoretical multiband system is shown in Figure 1.
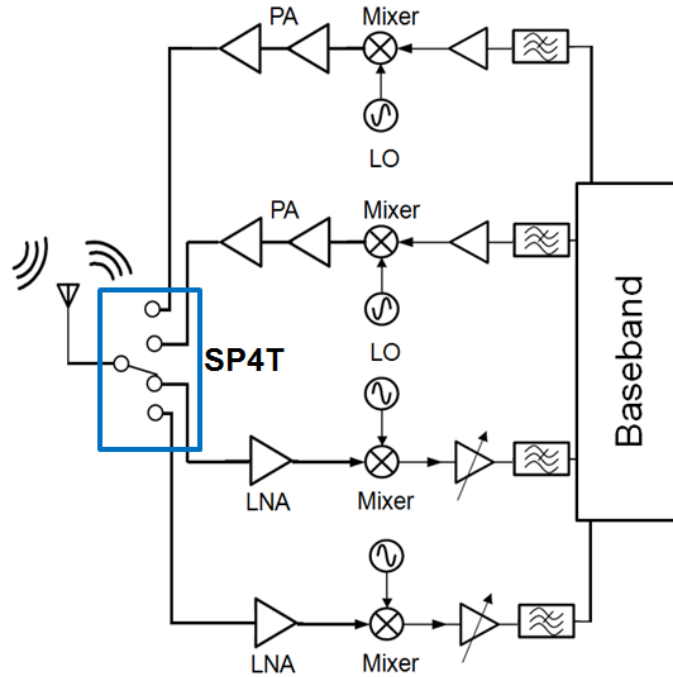
Figure 1: Block diagram of multiband RF transceiver module.

In the context of such multiband RF systems, the multi-throw nFET switches requires close attention to several design specifications. These design requirements will vary according to application needs. Typically, an RF switch design should achieve a low insertion loss, high isolation, and high linearity but, because of the inherent limitations of the underlying nFET transistors, meeting all of the required specifications becomes difficult. By far, the most commonly followed design approach for RF switches is to minimize the insertion loss, while achieving modest isolation and high linearity [8, 10–13]. However, for some applications high isolation is a more important design requirement than low insertion loss and high linearity. This work investigates the implications of using a design approach in which the main constraint is to maximize the pole-to-pole isolation, while achieving a modest insertion loss with good linearity. To the best of our knowledge, the SP4T switches have the highest pole-to-pole and input-to-output isolation at a frequency bandwidth of 1 to 40 GHz.

CHAPTER II

RF SWITCH DESIGN

2.1 nMOS Transistors for RF Switch Circuits

This section provides a brief overview of the regions of operations of FETs, in particular nFET transistors where "n" denotes the type of the induced channel when the device is conducting. p-channel FETs are not used in the designs because of their inherently lower carrier mobility (holes) and thus, higher on-Resistance in comparison to their counter-part, n-channel FETs. Understanding the mode of operations of the transistor will help to explain some of the switch design constraints and the results presented in the subsequent sections, including the cryogenic temperature effects discussed in Chapter 3.

In RF switch design there are two important mode of operations for the nFET. The first mode is the cut-off, also known as the subthreshold or weak-inversion. In the cut-off mode the transistor is biased such that $V_{GS} < V_{TH}$, where V_{GS} is the voltage between the gate and the source and V_{TH} is the threshold voltage of the device. For RF applications, the transistor in this mode is considered to be completely turned-off (e.g., no I_D current) but, in reality, there is a weak-inversion current that varies exponentially with the V_{GS}. However, this current is significantly small in the order of 10^{-12} (pico-Amperes) or lower, for more information see [14], [3]. In this mode of operation, the resistance of the transistors R_{ds} (see Figure 2) is considered to be infinite or very large [3] at low frequencies. This is because under this bias condition the inversion channel is not yet formed, and very little charge carriers (for an nFET the carriers are electrons) cannot travel from the source to the drain. Therefore, manifesting as a high resistance along the drain and source terminals

of the device. Ideally, when the transistor is turned OFF no RF signals should propagate from one terminal to the other (input to output), and this is typically true at low frequencies. But, at high frequencies RF signals will leak from one terminal to another due to the finite substrate resistivity of the silicon substrate in FETs and the parasitic capacitances [2] (as shown in Figure 2 (a)). Figure 2 (a) shows the potential RF leakage paths (highlighted in blue dashed lines) for a bulk nFET as frequency increases, and these can be formed by either individual or a combination of any of these parasitic capacitances, bulk-to-source (C_{bs}), bulk-to-drain (C_{bd}), gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). However, the main factors in determining the device insertion loss (measured as S_{21} when the switch is on) are the bulk-to-source (C_{bs}) and bulk-to-drain (C_{bd}) junction capacitances, and the associated parasitic resistances due to the conductive nature of silicon substrate [15].

An alternative to the bulk nFET device is the nFET Triple-well (TW) transistors. A schematic view of the TW transistor is shown in Figure 2 (b) along with the parasitic capacitances and resistance. The TW is becoming a prevalent option on most CMOS and BiCMOS technologies, and the added cost is not significant in comparison to the bulk only technology processes. A cross-sectional view of the TW device is also shown in Figure 3, and this type of structure provides added substrate isolation and body bias control [2] through the N-Well terminal. Because of this added isolation the effective substrate resistance increases, the parasitic losses of the transistors reduces thus, minimizing the amount of RF leakage through the substrate, which in turn improves the insertion loss of the switch (see Chapter 2.2.1 for further details). The purpose of R_G and R_B shown in Figure 2 (b), is to minimize the fluctuations of V_{GS} and V_{GD} at the source and drain terminals; therefore, increasing the device robustness by minimizing breakdown, improving dc bias isolation, and transistor reliability [1], [2].
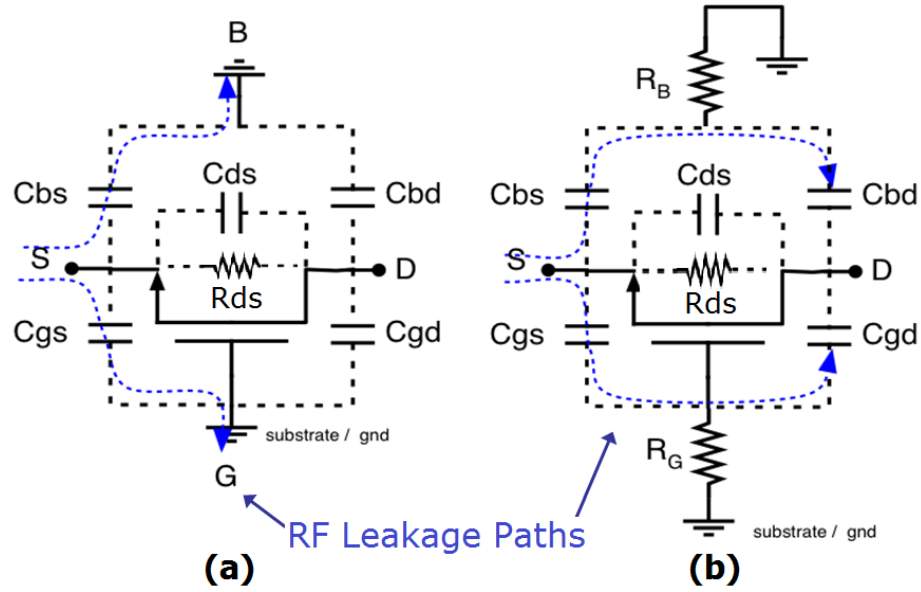
Figure 2: nFET transistors diagrams highlighting the parasitic devices and RF leakage paths for (a) bulk nFET and (b)triple-well isolated nFET with floating body resistors [1].
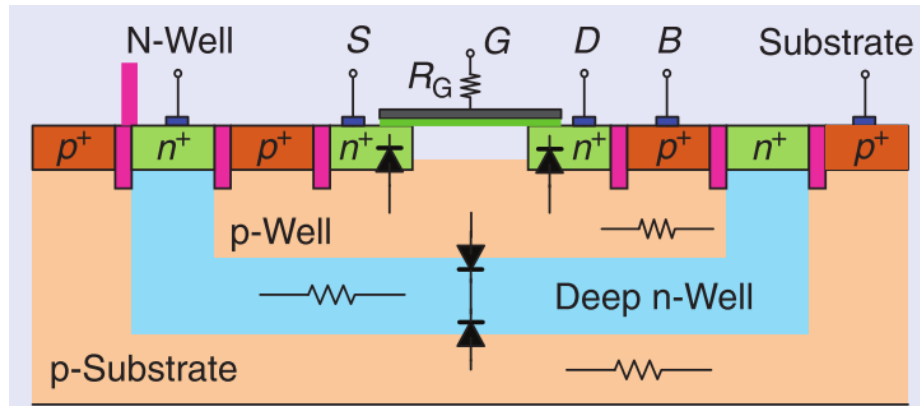
Figure 3: Cross-sectional view of a triple-well nMOS transistor [2].

The second mode of operation is the linear-region, also know as the triode or the ohmic region. In this mode the transistor bias condition is such that $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$, where V_{DS} is the voltage between the drain and the source terminals. Figure 4 shows a cross-sectional view a generic bulk nFET transistor under this bias condition. In this Figure the induced inversion channel is shown below the

oxide and the gate, and it is important to understand how it influences the device operation because it ultimately controls the conductance of the charge carriers in the transistor channel. Assuming a volumetric sample, this conductance can be expressed as shown in Equation 1; it is evident that it is dependent on the carrier mobility, μ and the free carrier density, "n" [16]. The "W", "X_j", and "L" represent the width, depth, and length, of the device respectively.

$$\sigma = (\frac{W X_j}{L})q\mu n \tag{1}$$

As V_{GS} exceeds V_{TH} the charge carriers density in the channel increases, the magnitude of the current, I_D rises and this translates to an improved conductance that is directly equivalent to a reduced device resistance [3]. Therefore, for a set transistor size (W/L) the lowest device resistance is attained by biasing the transistor with the maximum recommended V_{GS}, which increases the channel depth and the inversion layer conductance. This resistance is often referred to as the on-Resistance (R_{on}) or R_{ds} of the transistor (see Figure 2), and it is a dominant factor of the switch design because it is the main contributor of loss (insertion loss, measured as S_{21} when the switch is on) at low frequencies. Therefore, finding the optimal device size (see Chapter 2.2.1) and the proper bias conditions are essential requirements for optimal switch performance results. Equations 2 and 3 shows that I_D is directly proportional to $V_{GS} - V_{TH}$ and V_{DS}, and V_{GS} and V_{DS} are the main bias tuning knobs. A detailed derivation of this equation is found in several microelectronics books, including [3], [14]. As stated previously, at higher frequencies the parasitic capacitances become the main source of insertion loss due to capacitive coupling to the substrate [15].
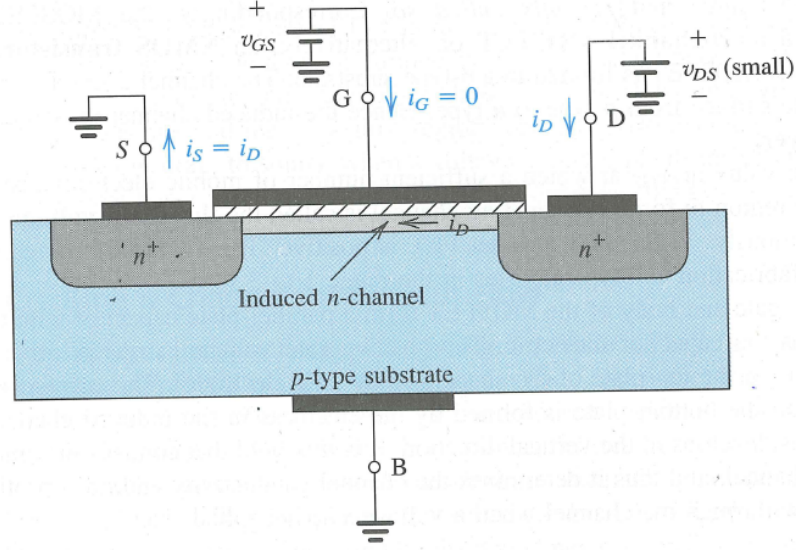
Figure 4: Cross sectional view of generic bulk nFET transistor biased in the linear region showing the induced n-channel layer [3].

$$I_D = k_n' \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] \tag{2}$$

Assuming very small V_{DS} (i.e., 50 mV),

$$I_D \cong k_n' \frac{W}{L}[(V_{GS} - V_{TH})]V_{DS} \tag{3}$$

where,

$$k_n' = \mu_o Cox \tag{4}$$

The term k_n' in Equations 2 and 3, is known as the process transconductance parameter, and it can be express in terms of μ_o, the charge carrier mobility and C_{ox}, the capacitance per unit gate area, as shown in Equation 4. I_D (Equation 3) is relevant for this discussion because it allows us to make inferences about other important parameters, such as the carrier mobility and the On-resistance (R_{ds}) because they cannot be easily measured. However, measuring I_D is relatively easier in comparison to the other parameters (e.g., R_{ds}, μ_o), and from it we can understand the behavior

of the transistor in the linear mode as bias and environment conditions change (e.g., cryogenic temperature discussed in the later chapters).

2.2 Single-Pole Single Throw

2.2.1 Design Procedure

The SPST switch was designed for applications that require high isolation and moderate insertion loss. A novel topology is proposed shown in Figure 5, and it is based on an alternating shunt-series configuration. This switch topology differs slightly from the standard symmetrical design configuration that only uses a single series-shunt topology [13]. The main benefit of this new topology is to provide high isolation by using two shunt transistors, M_1 and M_3. The topology also provides a tuning lever to improve the input matching (S_{11}) of the switch. Specifically, the M_1 transistor can be sized differently than the M_3 shunt transistor in order to achieve the desired input matching. For multi-throw switches in multiband applications, this tuning lever becomes an important feature as each switch throw-arm can be individually configured for a certain frequency and bandwidth. While the use of two shunt arm transistors achieves high isolation, the additional shunt arm degrades the insertion loss. To compensate for the insertion loss degradation, isolated triple-well (TW) devices were used for the series arms (M_2 and M_4). A body floating technique (adding a large resistor to the terminal) was used on all the transistors to improve both the insertion loss and linearity of the switch. The advantages and drawbacks of using TW in RF switches are outlined in [1, 2].
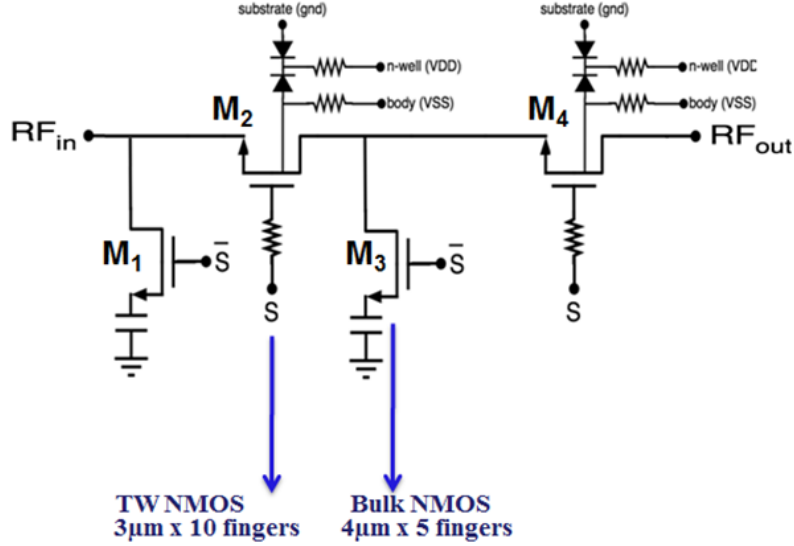
Figure 5: Schematic of single-pole single-throw (SPST) switch using triple-well and bulk nMOS devices.

Standard bulk nMOS transistors were used for the shunt arms, M_1 and M_3 transistors, because TW devices do not provide any added improvements in isolation [1], [17] (this was verified through simulation). The devices were sized to maximize isolation and to provide acceptable insertion loss at the bandwidth of interest (6 to 23 GHz). The gate widths for the series transistors M_2 and M_4 were selected to be 30 μm with the minimum gate length of 0.120 μm. The shunt arms M_1 and M_3 also used the minimum gate length and were 9 μm and 20 μm wide, respectively.

The source and drain of the devices were biased to 1.2 V using a 10 kΩ resistor, to enable the transistor to quickly go from the cut-off region to triode region (switching speed). The gates of the transistors were RF-floated using the same value resistors, and this helps to improve dc bias isolation [15] and device reliability [1]. The gates were controlled using on-chip, buffered inverters, and an external digital signal. The digital signal is represented as "S" in Fig. 1 and 2. To turn-on the switch, "S" is set to 2.4 V, establishing the maximum recommended V_{GS} at the series transistors, M_2 and M_4, to 1.2 V. The shunt arms M_1 and M_3 are turned off because their V_{GS} is set

to 0 V. The opposite is true when the S signal is low (1.2 V) and the switch is in the off-state. Since the drains were biased to 1.2 V, dc blocking capacitors were used on the shunt transistors, M_1 and M_3, in order to prevent current from flowing through the shunt arm when the transistors were turned on. The capacitors were sized to look like an electrical short over the desired operating frequency range.

2.2.2 Simulation and Measured Results

The switches were fabricated in a 130 nm SiGe BiCMOS technology (IBM 8HP) to enable integration with other RF blocks using SiGe HBTs. The switch characterization was performed directly on-wafer using a custom-built, integrated S-parameter, noise figure, and load-pull probing station, as shown in Figure 6. The station allows for a single probing of the DUT with the capability of RF switching between the Agilent network analyzer (E8363B) used for the S-parameters measurements, and the Agilent E4446A spectrum analyzer, and two Agilent E8257D signal generators for the linearity measurements. A probe level calibration using an Short-Open-Load-Through (SOLT) calibration standard was performed along with an RF power calibration using a power sensor to account for all losses.
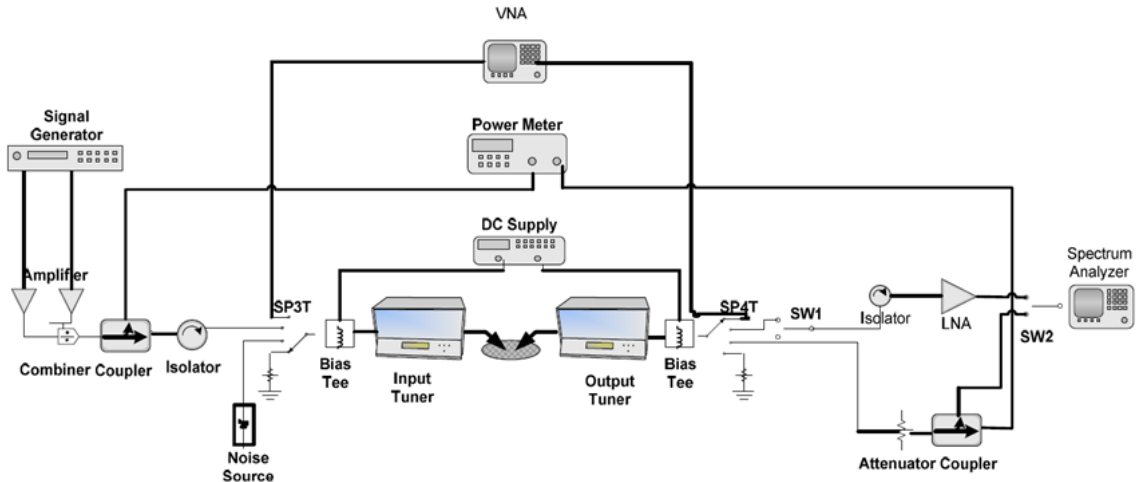
Figure 6: Block diagram of the test setup used: An integrated S-parameter, Noise Figure, and Load-Pull System for up to 40 GHz.

Figure 7 (a) shows the measured and simulated insertion loss and isolation of the SPST switch. The measured insertion loss (S_{21} when the switch is on) varies from 2.8 dB at 6 GHz to 4.5 dB at 23 GHz, the return loss (S_{11}) and isolation (S_{21} when switch is off) were measured to be greater than 13 dB and 46 dB at 23 GHz, respectively. The insertion loss closely matches the simulation results; however, the measured isolation and return loss shown in Figure 7 (b) differs from the simulation results. This difference is attributed to the lack of substrate capacitance contribution in the silicon substrate models in the design kit. Another important metric for switches is the linearity, which was measured by the input third-order intercept (IIP3) and the input 1-dB compression point (P_{1dB}). The results are plotted in Figure 8 (a) and Figure 8 (b), respectively. At 20 GHz, an extracted IIP3 of 19.4 dBm with a frequency offset of 1 MHz, and a P_{1dB} of 6 dBm was achieved.
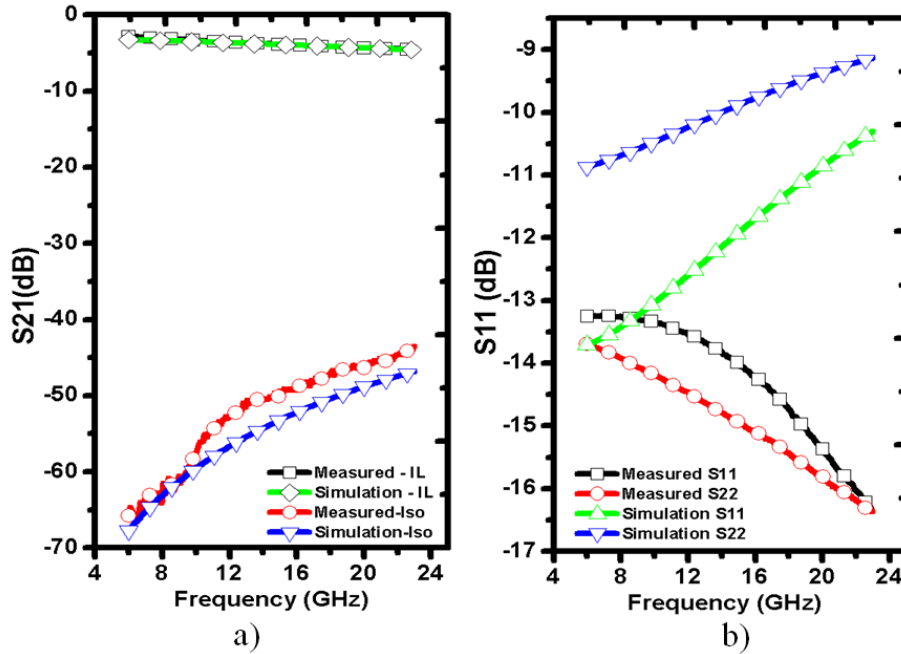
Figure 7: Measured and simulated insertion loss (IL) and isolation (Iso.) (a), and (b) the input and output return loss of the SPST switch.
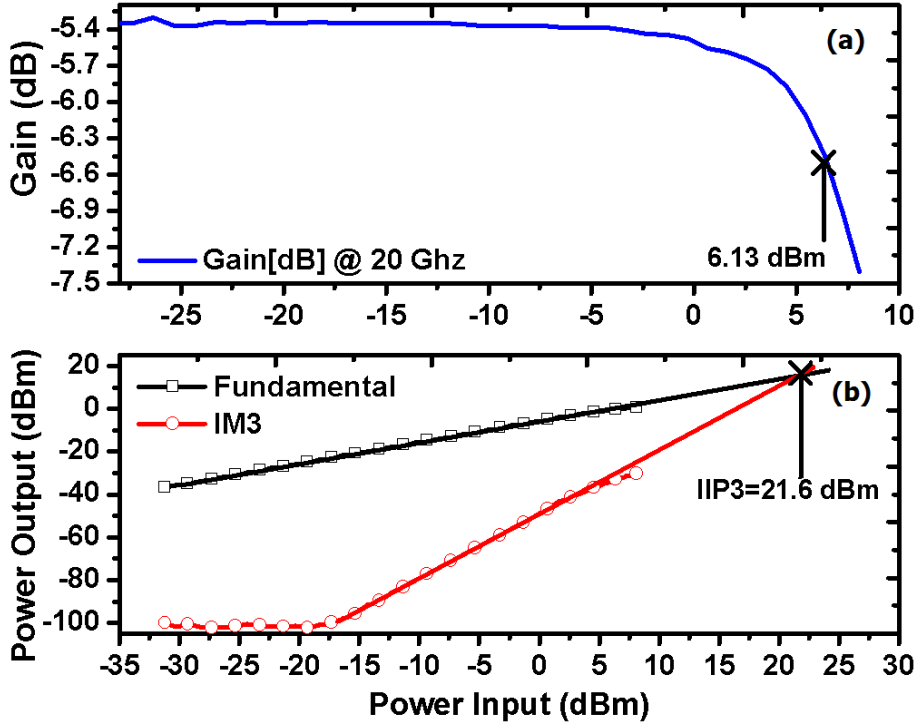
Figure 8: Measured (a) IIP3 and (b) P1dB at 20 GHz for the SPST switch.

2.3   Single-Pole Four-Throw Switch

2.3.1   Design Procedure

The SPST described in the previous section was used as a building block for the SP4T switch. Figure 9 shows the SP4T block diagram. Not shown in the diagram are the CMOS inverter blocks that were used to drive the gates of the devices and a 2-4 decoder block designed to reduce the number of digital inputs required for measurement. The main challenge in combining the SPST block into an SP4T switch was to keep the insertion loss within an acceptable range without degrading the high isolation. In addition, to achieve an acceptable return loss at the output node, the M_4 transistor at each of the arms had to be individually optimized.
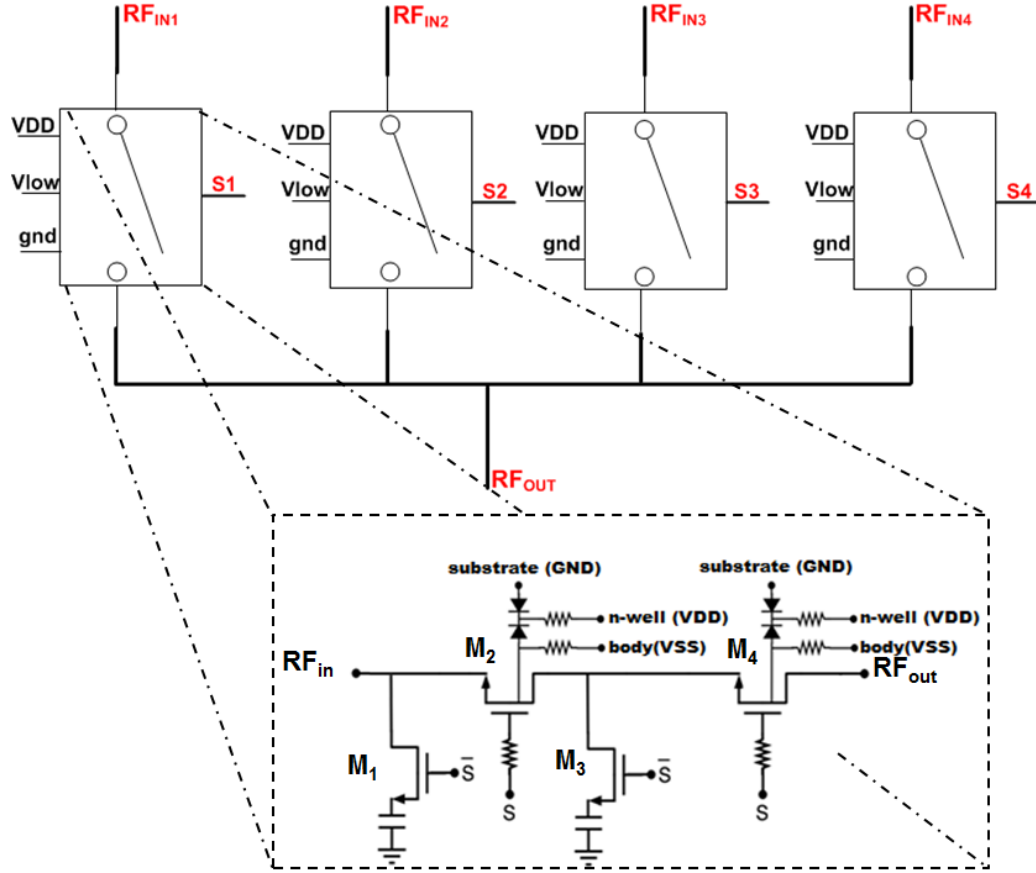
Figure 9: Simplified block diagrams of the SP4T switch topology showing the zoomed-view schematic of the individual throw arms.

The RF lines were implemented using grounded CPW lines. The transmission lines were designed and simulated using the full wave EM modeling Sonnet ⓡ. The simulation results showed a mutual coupling of less than -70 dB at 40 GHz, while maintaining a 50 Ω impedance match at the input port and at the output ports. To further minimize coupling and increase isolation between adjacent input ports, the layout was carefully planned so that each adjacent throw-arm was placed horizontally shifted in an alternating pattern, as shown in the photomicrograph Figure 10.
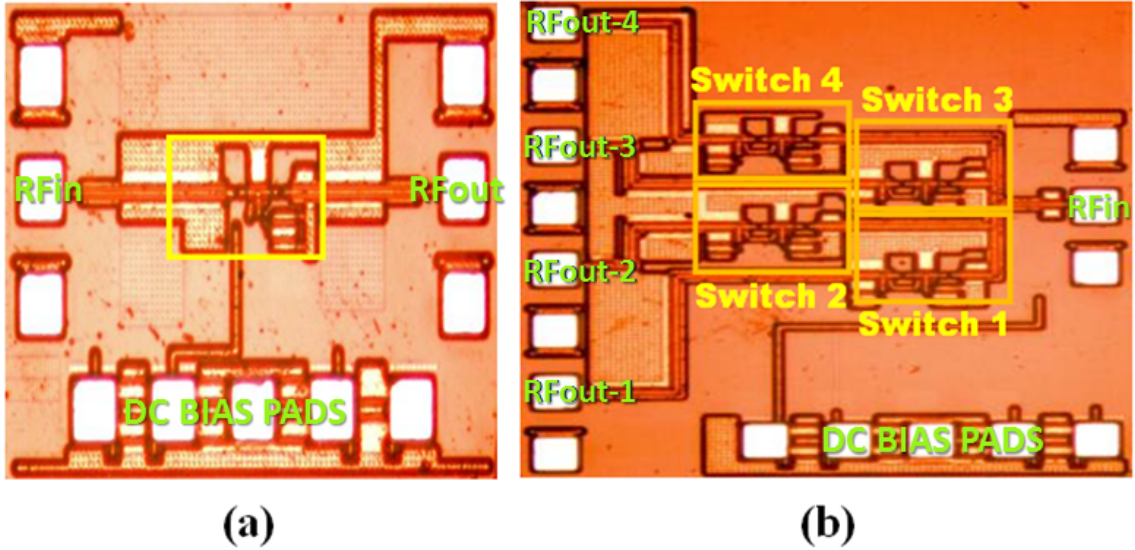
Figure 10: Photomicrograph of (a) SPST and (b) SP4T switches.

2.3.2 Measured Results

The SP4T demonstrated a measured isolation between adjacent inputs of better than 40 dB between 6 and 23 GHz (Figure 11). The measured isolation values between the individual input ports and the output port are shown in Figure 12 (a), and greater than 40 dB were attained for the RF_{IN1}, RF_{IN2}, and RF_{IN3}. The RF_{IN4} port was the lowest at 35 dB at 40 GHz. The non-adjacent ports (Figure 12 (b)) achieved isolation of more than 40 dB at 40 GHz for all ports. This indicates that even though non-adjacent inputs were pushed closer together by using the alternating shifted-pattern as described in Figure 5, the isolation between non-adjacent ports does not limit in the overall switch isolation. The reason the isolation decreases at high frequencies is mainly due the change in impedance of all the capacitances at the particular switch branch, including the total off capacitance (C_{OFF}) of the series arm [9], [18]. As the capacitances change the RF signal that is should be shunted to ground gets routed to the nearest ports.

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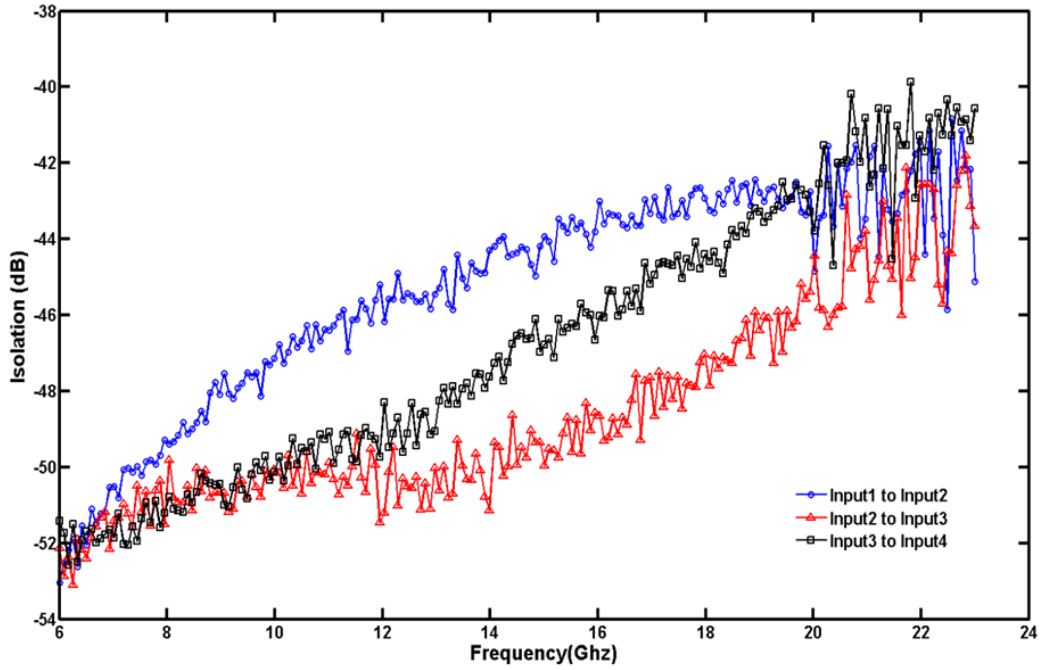
Figure 11: Measured isolation (S21) between adjacent input ports for the SP4T switches.
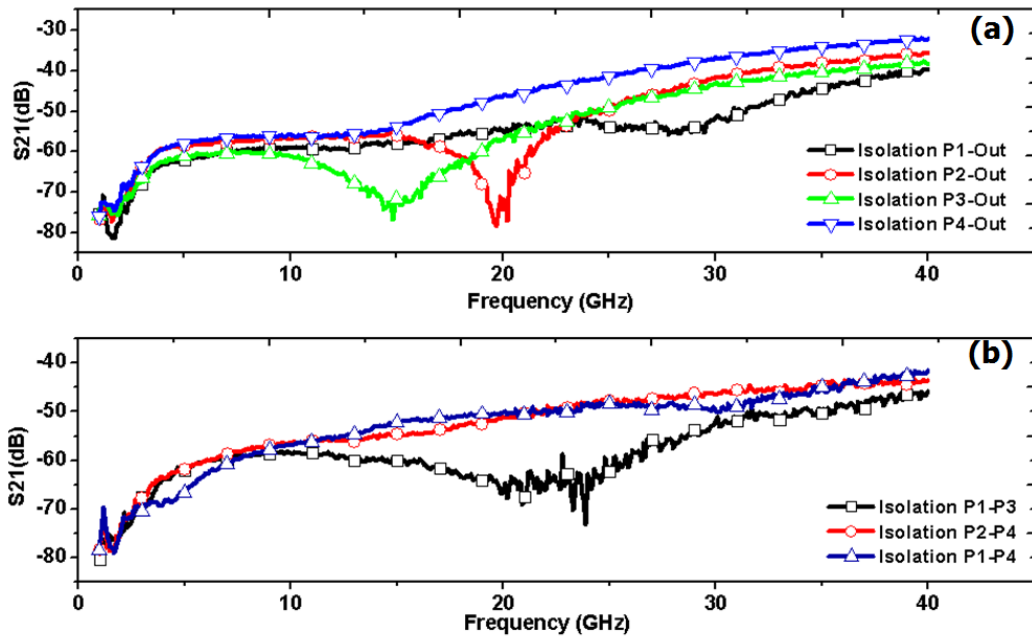
Figure 12: Measured SP4T switch (a) isolation between the input ports and output port (b) isolation between nonadjacent input ports.

The linearity of the SP4T switch was measured at 20 GHz with a frequency offset of 10 MHz, Figure 13 (a) shows. An IIP3 of 19.4 dBm and a P1dB of 6.1 dB were achieved. The limiting factor of power handling capability of the SP4T switch is the junction diodes of the bulk nMOS transistors, M_1 and M_3 [19], [17]. All four input ports show a return loss of better than 11 dB at 1 GHz and it continues to improve up to 15 dB at 40 GHz (see Figure 14). The insertion loss shown in Figure 14 varies from 2.8 dB at 1 GHz to 14 dB at 40 GHz, for M_3 port which show the worst performance. Since the goal of this design is to achieve high isolation and then compensate for the loss this is an acceptable design result.
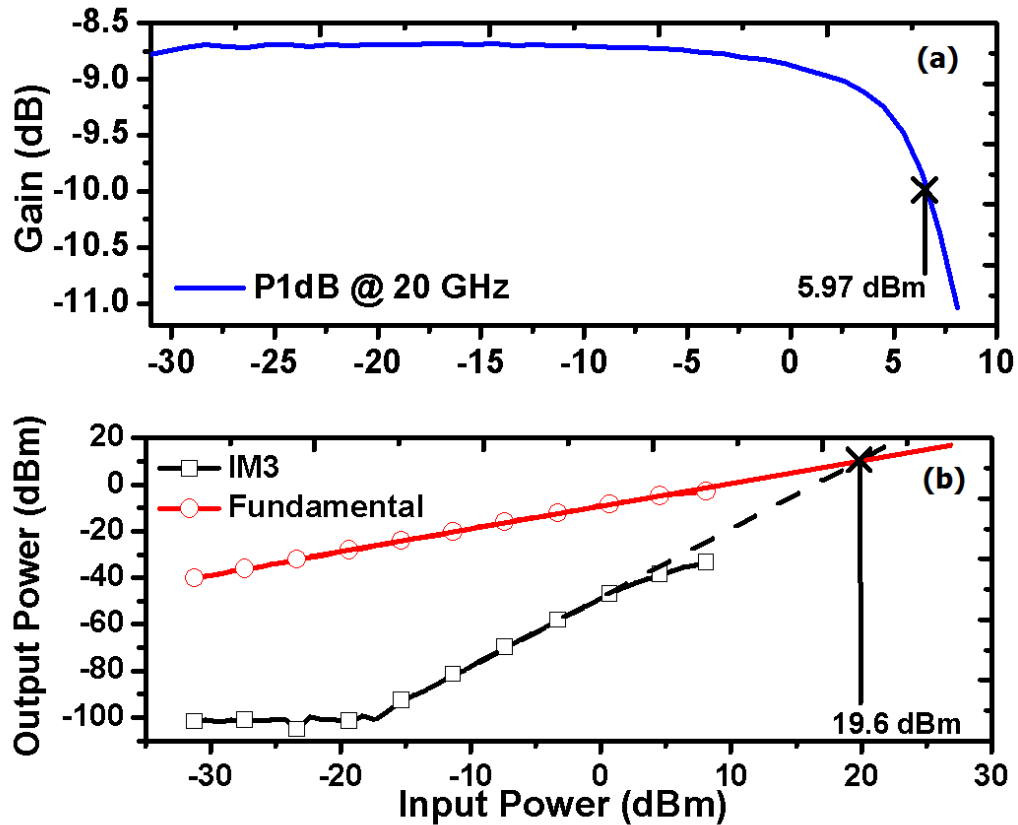
Figure 13: Measured (a) IIP3 and (b) P1dB at 20 GHz of the SP4T switch.
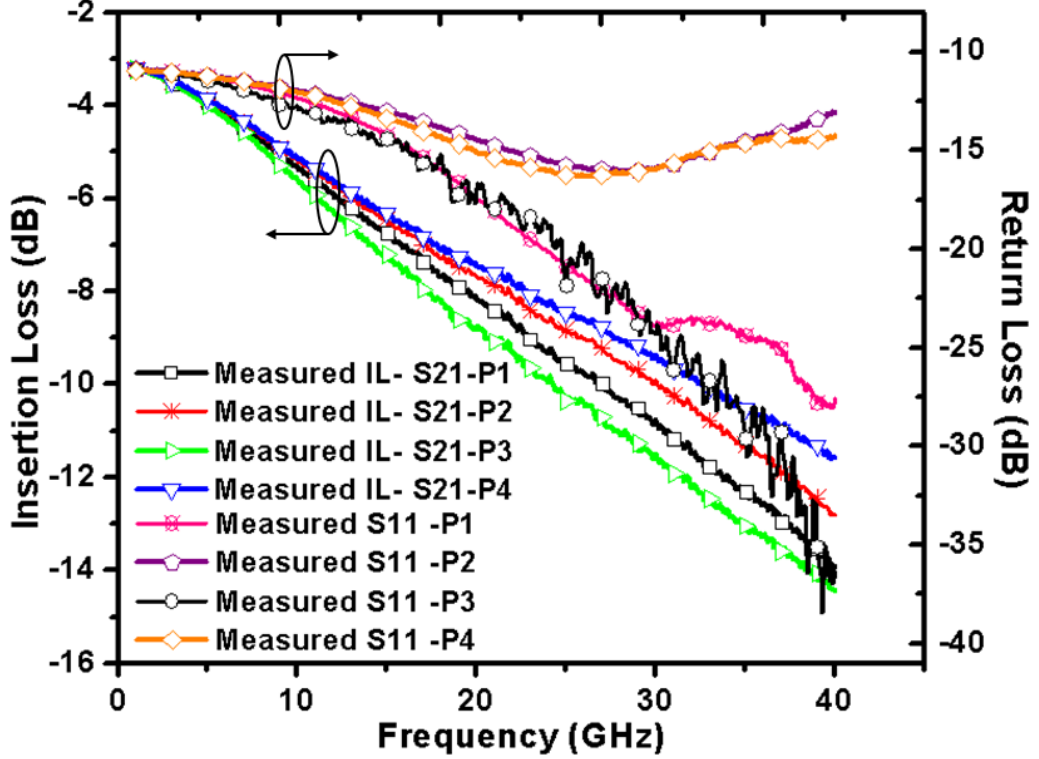
Figure 14: Measured Insertion and Return Loss of the SP4T switch.

2.3.3 Benchmarking

A comparison of recently published wideband SP4T CMOS switches is presented in Table 1. The table includes two Figure-of-Merits (FoMs) that were calculated to benchmark the works listed. The FoM in equation 5 takes into account the magnitude of the input-to-output isolation and insertion loss. The second FoM, equation 6 considers the same parameters as the equation 5 however, it also accounts for the linearity (IIP3) of the switches. For both FoMs, a higher number represents better switch performance. The table shows that the presented SP4T switches exhibits the highest input-to-output isolation, pole-to-pole isolation, and switch FoMs.

$$FoM_1 = \frac{Iso.(mag)}{I.L.(mag)} \tag{5}$$

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$$FoM_2 = \frac{Iso.(mag) * IIP3(mW))}{I.L.mag} \tag{6}$$

2.4 Summary

A novel SPST switch configuration was proposed and the measured results demonstrated exceptionally high isolation with excellent input matching and good linearity. The SPST demonstrated a measured isolation of greater than 46 dB at 23 GHz. The SP4T switch achieved isolation between inputs ports of more than 40 dB and input to output port isolation of 35 dB at 40 GHz. Good linearity results were also achieved, with the SPST and the SP4T switches achieving a measured IIP3 of 21.6 dBm and 19.6 dBm, respectively.

Table 1: SP4T Switch Performance Comparison

Ref.	Freq. (GHz)	Iso. input-to-output (dB)	Iso. pole-to-pole (dB)	I.L. (dB)	R.L. (dB)	P_{1dB} (dBm)	IIP3 (dBm)	FoM_1	FoM_1	Technology
This Work	1 to 40	75 to 35	> 40	2.8 to 14	11.5 to 25	6	19.4	32	275	130 nm BiCMOS
[20]	5 to 24	> 39 to 26	N.R.	1.8 to 2.7	> 14	9	21	16	195	130 nm CMOS
[8]	50 to 70	> 30 to > 20	27	< 2.5 to 2.8	> 13	14	> 23	8	150	130 nm CMOS
[10]	DC to 70	>25	>28	<3.5	>15	10	21	12	153	130 nm CMOS
[11]	45 to 75	> 31	N.R.	<4.5 to 7	> 10	N.R.	N.R.	21	N/A	130 nm CMOS

CHAPTER III

THE EFFECTS OF CRYOGENIC TEMPERATURE ON NFET BASED RF SWITCHES

RF switches are ubiquitous circuit blocks in a variety of cryogenic commercial and space based applications, e.g., receiver front ends, radar transceivers, medical electronics, radio astronomy, sensors and actuators operating in cryogenic environment. Cryogenic electronics is a well developed area, it has more than six decades of research experience and a multitude of published works. But, the core focus in this area have ranged mainly from material properties to semiconductor devices, and only most recently (within the last decade) the research community have investigated the performance of analog, digital, and RF circuits at cryogenic temperatures. However, there is still a dearth of literature on the effects of cryogenic temperatures on FET based RF switches. This chapter focuses on understanding the low-temperature operation (liquid nitrogen, 77K) of FET based RF switches for some of the aforementioned applications.

The physics of FET devices are well understood at both room and cryogenic temperatures; however, based on our knowledge, no published work has been presented that investigates the RF performance and effects of operating FET based RF switches at cryogenic temperature. This chapter will attempt to present new insights on this area by examining the measured RF performance, S-parameters and power handling (P_{1dB}) of the individual transistors (bulk and TW) and the switch circuits (SPST and SP4T) at room temperature and cryogenic temperature. The chapter begins by discussing the measured DC performance of nFET devices at cryogenic temperature, which have received sizable attention [21–25], followed by a discussion of the

measured RF performance of single transistors (the test structure that were used in the circuit design of switch circuits), and finally the results for the SPST and SP4T switch circuits are analyzed.

3.1   Cryogenic Operation of nFET Devices

In this section, measured DC performance is presented to help understand the cryogenic results obtained from the nFET based RF switches. We begin by presenting a brief overview of the benefits and performance enhancements of operating FET devices at cryogenic temperatures. It is well established that the main advantages of operating bulk CMOS transistor at Liquid Nitrogen (LN) performance are the reduction in power delay product, lowering the chance of latchup, increase switching speeds (i.e., the required time to charge and discharge circuit capacitances), mobility and threshold voltage improvement [21]. The mobility and threshold voltage parameters are particularly important for switches because it allows us to easily relate them to the circuit performance (i.e., insertion loss, S_{21}) through the measured device transconductance (g_m) and transfer characteristics.

3.1.1   DC Cryogenic Performance

Figure 15 shows typical DC measurements, gm and I_D vs. V_{GS} of the bulk nFET biased in the linear region measured at three different temperatures. These results confirm the literature findings which states that for the same bias condition both the carrier mobility and threshold voltage increases as the temperature is reduced. The reason V_T increases is because as temperature is reduced, the magnitude of ϕB increases. This evident in the threshold voltage Equation 10 for a n-channel MOSFET, where Q_{EFF} is the effective oxide charge per unit area, ε_{Si} is the dielectric constant of silicon, V_s is source-to-body voltage, N is the channel surface concentration, ϕ_{ms} is the work function difference between gate and channel, C_{OX} is the gate-oxide capacitance, ϕ_B is the Fermi potential of the bulk silicon with respect to the intrinsic

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Fermi level, and q is the electron charge [21].

$$V_{TH} \cong \frac{1}{C_{OX}}[-Q_{EFF} + \sqrt{2\varepsilon_{Si}qN(2|\phi_B| \pm Vs)}] + 2|\phi_B| + \phi_{ms} \qquad (7)$$

Figure 15: Measured transconductance (a) and transfer characteristics (b) of a bulk nFET in linear mode at 3 different temperature points.

The devices used for measurements are of similar dimensions (0.12 μm length and 10 μm width) as the ones used on the switches design circuits presented in the previous chapters. From Figure 15 we can deduce that the reason the carrier mobility improves with decreasing temperature from 300 K to 90 K is because of the reduced carrier scattering mechanisms [21]. There are three main scattering mechanisms that dictate the carriers mobility in the inversion layer of transistors - the Coulomb, surface, and phonon scattering [26]. The Coulomb scattering is mainly due to charge impurities, whereas the surface scattering is caused by the roughness of the surface, crystal defects, foreign atoms, open bonds, and/or phonon scattering, also known as lattice vibrations. Lattice vibration is related to how a charge carrier transverses through a semiconductor crystal [16]. The authors in [26] state that only the Coulomb and the surface roughness mechanisms prevail at low temperature, and phonon scattering/lattice vibrations are more evident at room temperature however,

in [16] and [21] the calculations are shown that the carrier mobility due to phonon scattering does indeed increase as temperature decreases, and this is because of the reduced number of phonons.

The TW nFET shows the similar improvements as the bulk devices, as shown in Figure 16. The gm, I_D, and V_{TH} increase as the temperature decreases. However, the TW device shows better performance than the bulk at cryogenic temperature because of the increased substrate resistance and smaller parasitic influences. But, we cannot confirm this assumptions because the devices have different dimensions. The TW transistor is approximately three times wider than the bulk transistor, it is 32 μm wide while the bulk is only 10 μm, and minimum gate length was used both transistors, 0.12 μm.
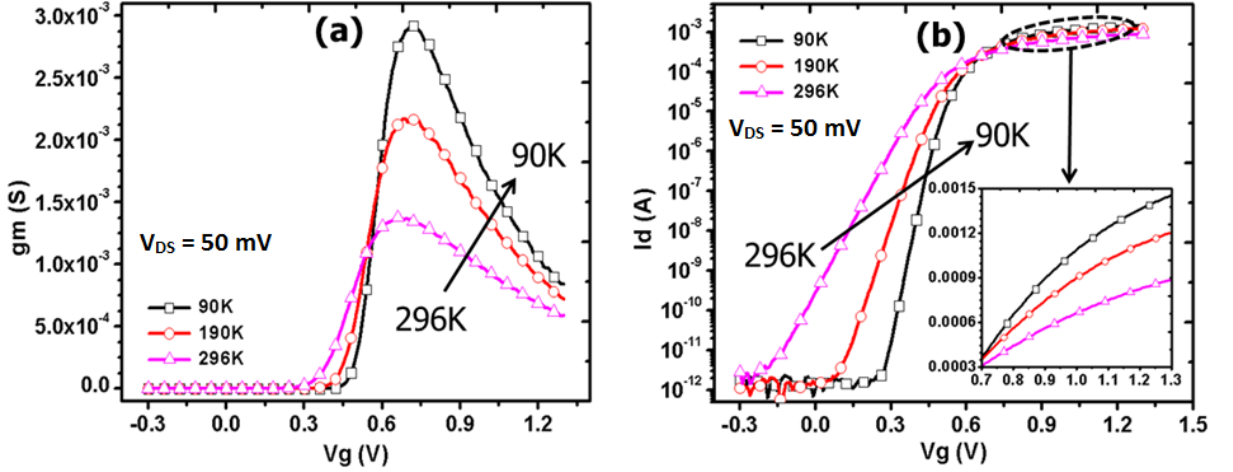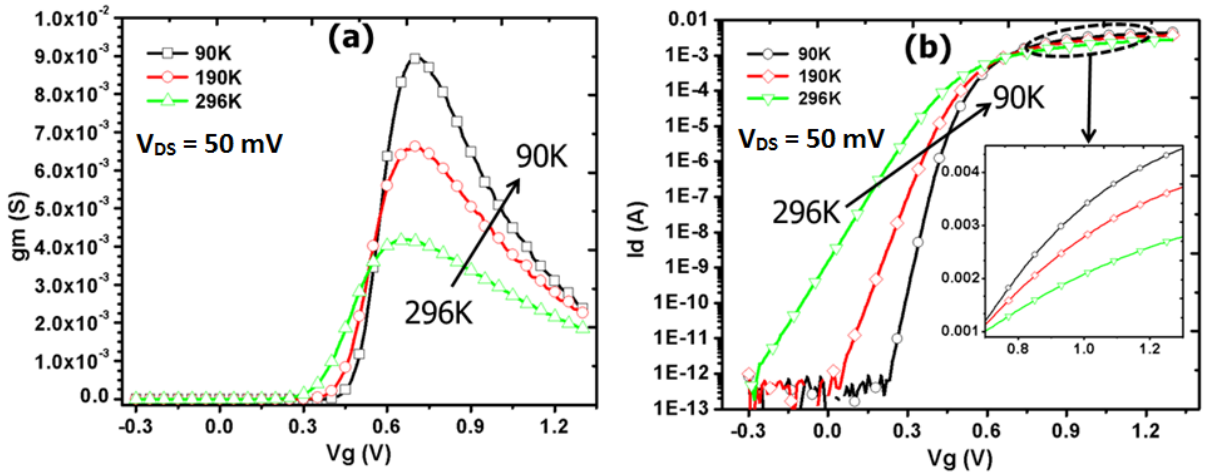

Figure 16: Measured transconductance (a) and transfer characteristics (b) of a TW nFET in linear mode at 3 different temperature points.

3.1.2 RF Cryogenic Performance

Relating the fact that the conductivity of the inversion layer is fundamentally dependent on the the carrier mobility, and since the mobility improves with decreasing temperature, it is expected that the RF performance of the transistors will improve

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at lower temperatures. The results shown in Figure 17 verifies these assumptions, the insertion loss, S_{21} of the bulk FET at three temperature points, 90 K, 190 K, and 296 K are presented. As stated previously, the R_{on} of the switch directly influences the insertion loss, and the response of R_{on} versus temperature can be analyzed using the triode current equation, Equation 2 (presented in Chapter 2.1). Since V_{DS} is closed to zero (because both drain and source are biased at the same voltage), the R_{on} can be found to be as shown in Equation 8. If we take the ratio of this equation at cold temperature (COLD) and at room temperature (RT), the ratio results is given in Equation 9. These results confirms that as temperature reduces the electron mobility increase and R_{on} will improve (decrease) for nFET devices. The equation also shows that as the threshold voltage, V_{TH} rises at low temperatures the on-resistance will increase, degrading the insertion loss. However, the electron mobility increases exponentially with decreasing temperature, while the threshold voltage only increases linearly [21]. Thus, the mobility ratio dominates the trend, causing an overall decrease in on-resistance which in turn decreases the insertion loss of the devices at low temperatures.
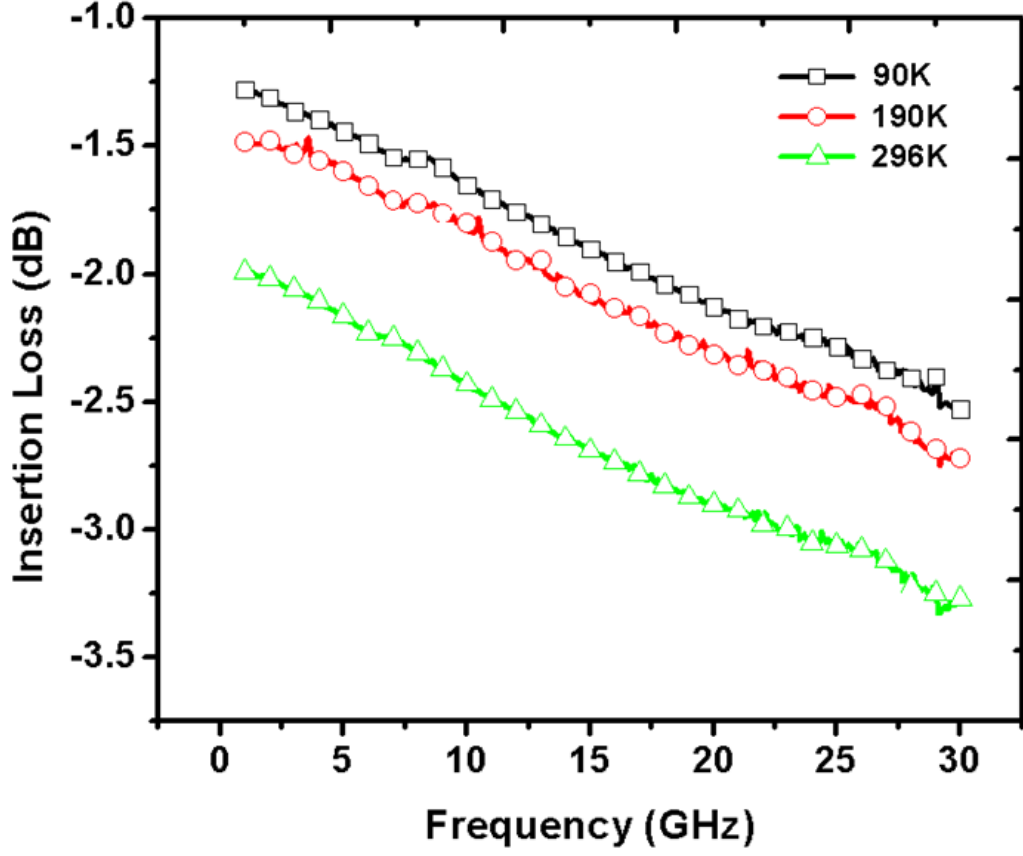
Figure 17: Measured insertion loss (S_{21}) of a single bulk nFET device.

$$R_{on} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{L}{\mu_o C_{ox} W (V_{GS} - V_{TH})} \tag{8}$$

$$\frac{R_{on-COLD}}{R_{on-RT}} = \frac{\mu_{RT}}{\mu_{COLD}} \frac{(V_{GS} - V_{TH-RT})}{(V_{GS} - V_{TH-COLD})} \tag{9}$$

In Figure 18 the measured RF performance of the TW nFET configured as an RF switch at different temperature points are shown, and as expected the results show similar improvements as the bulk devices. Once again, the improvements of the insertion loss is directly related to the improvement of carrier mobility as temperature reduces, which in turn is directly proportional to the current, I_D and the R_{on} of the transistor. The S_{21} enhancement for the TW device is significantly higher than the bulk, ($\sim$1.1 dB) versus ($\sim$0.6 dB), respectively. This can be attributed to the TW

device having a higher substrate resistance and lower parasitic capacitances effects. However, because the devices do not have the same dimensions we cannot confirm this assumptions.
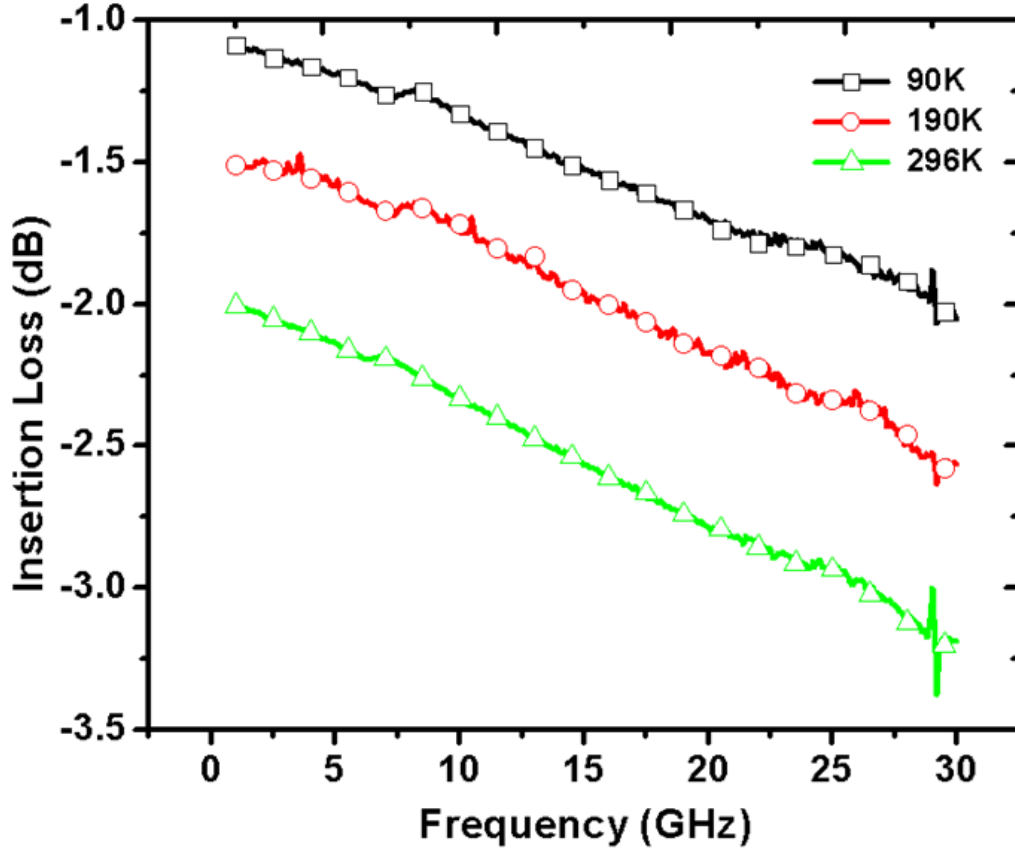
Figure 18: Measured insertion loss (S_{21}) of a single TW nFET device.

3.1.3 Cryogenic Measurement Facilities

The cryogenic measurements were performed using the TTP6 cryogenic (Figure 19), a open-cycle cryogenic station manufactured by Lakeshore Cryotronics, Inc. The devices and circuits were characterized over temperature range of 300 K to 77K. The system allows the use of either liquid nitrogen (LN_2) or liquid helium (LHe) depending on the temperature range needed however, for this work only LN_2 was used. The system has four manipulated probe arms available, two DC and two RF probe

arms suitable for measurements up to 40 GHz. Standard GSG probes and Multi-contact DC probes were used to characterize the circuit and device test structures. An Agilent 4155C along with GPIB cables and MATLAB programs were used for DC measurements; for the RF measurements an Agilent E8364B 4-port PNA Series Network Analyzer was used to capture the S-parameters, and for the power measurements a HP-E83732A Signal Generator was used.

Figure 19: Photo of the open-cycle TTP6 cryogenic station.

3.2 Cryogenic RF Switch Performance

The measured cryogenic temperature RF performance of both SPST and SP4T circuits are presented and analyzed in this section. Using the information learned from the single device (both bulk and TW) discussed in the previous sections, the insertion loss S_{21} of the switches circuits are expected to follow the same trend with temperature - that is, at any giving frequency range the insertion loss decreases as the temperature reduces. Thus far, the discussion has focused mainly on only one of the main metrics of RF switches, the switch insertion loss (S_{21} when the switch is on). However, two other key metrics are presented in this section, the isolation (S_{21} when switch is off), and the power handling capability measured by the power 1-dB compression point (P_{1dB}).

3.2.1 Measured SPST Cryogenic Results

Figure 20 and 21 shows the measured SPST insertion and return loss, respectively at three different temperature points, 90 K, 190 K, and 296 K. The schematic of the switch circuit is the same as the one shown in Figure 5 in Chapter 2.2.1. The series arms use TW NFETs while the shunt arms use standard bulk NFETs. At lower frequencies, below 15 GHz, the insertion loss decreases with reducing temperatures however, at high frequencies (greater than 15 GHz) at the 190 K and 90 K temperature points the insertion loss does not follow the same trend. One possible reason for this results, is the chance that the circuit bias changes at lower temperature points but, further work needs to be done in order to confirm this assumptions. The return loss improves by more than 2 dB at 20 GHz from room temperature to 190 K and again at 90 K.
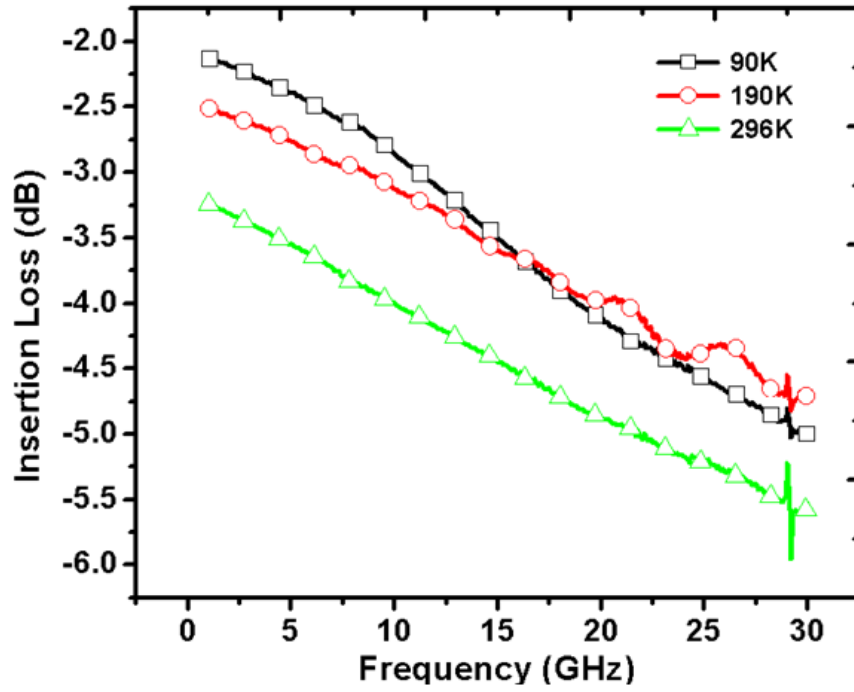
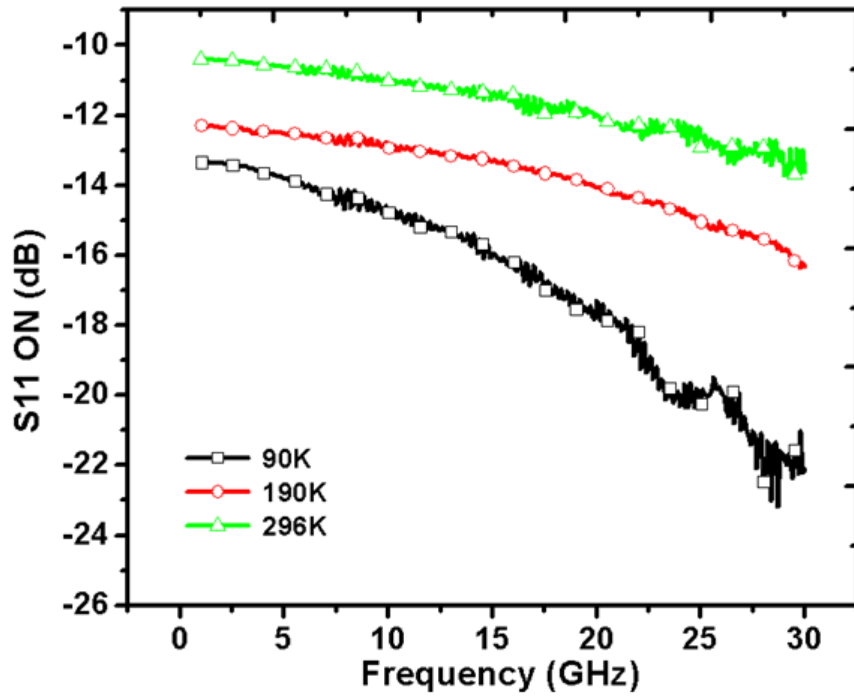Figure 20: Measured SPST insertion loss (S_{21}) during cryogenic operation.

Figure 21: Measured SPST return loss (S_{11}) during cryogenic operation.

The measured isolation of the switch is shown in Figure 22, and it is measured by the S_{21} when the switch is off. The isolation is defined from from input-to-output terminals. From a cursory glance of Figure 22, one may deduce that the switch isolation does not show the same improvements as the insertion loss at cryogenic temperatures. But, by taking a close look as the inset graph in Figure 22 shows the isolation does indeed improve as the temperature decreases (e.g., at 28 GHz the isolation is approximately -37 dB at room temperature (296 K), and at 190 K and 90 K it improves to -38.5 dB and -40 dB, respectively). The switch isolation is also dependent on the carrier mobility of the shunt transistors, which are turned on when the switch is configured in the off state.

The isolation is also affected by the R_{DS} of the series transistors operating in the cut-off region (off-state) and the parasitic capacitances of these transistors (see Figure 2 discussed in Chapter 2.1). For all intents and purposes the oxide capacitance is temperature independent however, the junction capacitances C_j of a nFET (given by Equation 10) are temperature dependent [16], [23]. This is because the built-in voltage increases as temperature is reduces, which in turn increases the depletion width due to freeze-out [16]. Equation 10, W_{rb} is the thickness of the depletion region, A is the area of the p-n junction, ε_{Si} is the dielectric constant of silicon, V_{bi} is the built-in-potential, V is the reversed-bias voltage, and V_t is the thermal voltage [16].

$$C_j = A(\frac{\varepsilon_{Si}}{W_{rb}}) = A(\frac{\varepsilon_{Si}}{\sqrt{\frac{2\varepsilon_{Si}}{qN_B}(V_{bi} + V - 2V_t)}}) \tag{10}$$
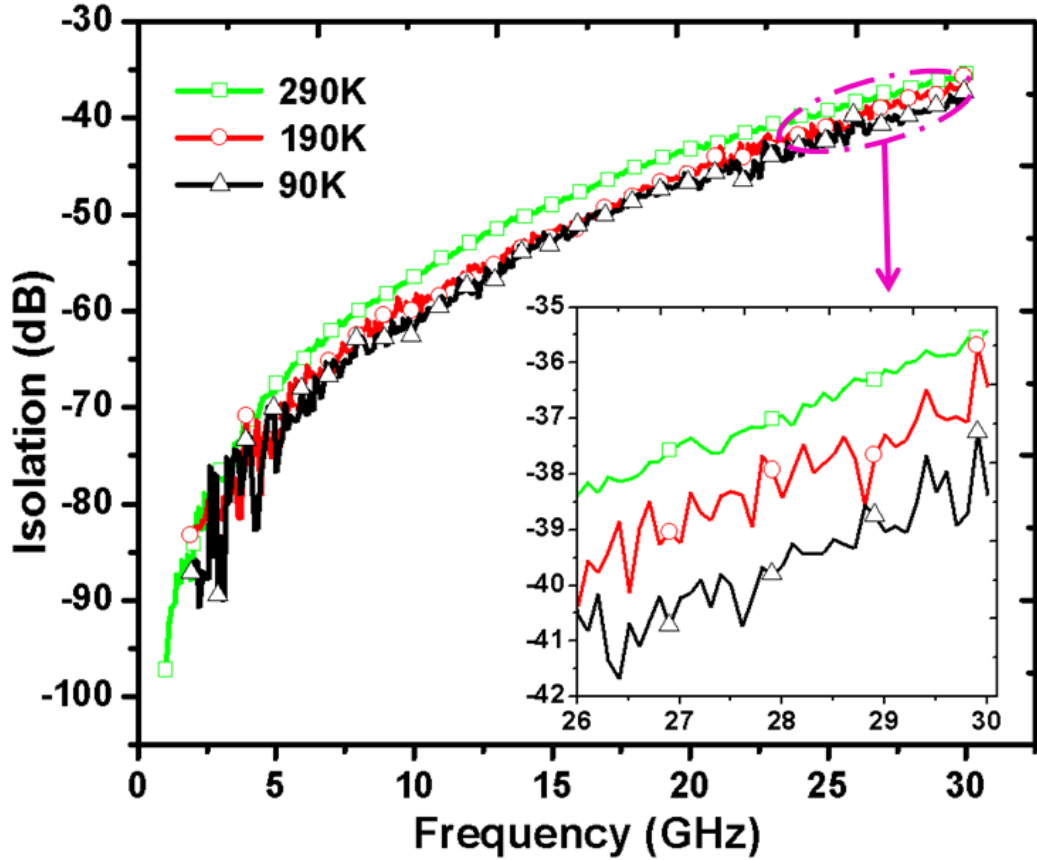
Figure 22: Isolation for SPST switch during cryogenic operation.

The power handling capability is another important figure-of-merit, and as stated previously, it is measured by P_{1dB}. P_{1dB} is determined with large-signal excitation therefore, it takes into account higher order terms (n $\geq$ 3) [27]. The measured P_{1dB} of the SPST switch as a function of temperature at three different frequencies, 10 GHz, 15 GHz and 20 GHz are shown in Figure 23. For all three frequencies the power handling capability improves as the temperature decreases. Using nFET P_{1dB} Equation 11 originally derived by [27], it is evident that the carrier mobility of the devices play a large influence on the device P_{1dB}. The effective carrier mobility, μ_1 is a term in the numerator of Equation 11 and it is raised to the power of 4, while the mobility terms in the denominator are only raised to the power of 2. Therefore, we can conclude that the numerator term is more dominant, and threfore the reason

why P_{1dB} improves at cryogenic temperatures. However, this conclusion may be true only for this type of device, nFETs. This equation also shows that v_{sat} increases as temperature decreases (due to reduce lattice scattering), and thus, limiting the carrier mobility, which in turn limits P_{1dB} improvement.

$$P_{1dB} = \frac{(1 + \frac{\mu_1 V_{od}}{2v_{sat}L})^4}{2R_s(\frac{\mu_1}{2v_{sat}L})^2[V_{od}(1 + \frac{\mu_1 V_{od}}{4v_{sat}L}) + \frac{6.88v_{sat}L}{\mu_1(1+\frac{\mu_1 V_{od}}{2v_{sat}L})^2}]} \tag{11}$$

where,

$$\mu_1 \triangleq \mu_0 + 2\theta v_{sat}L \tag{12}$$
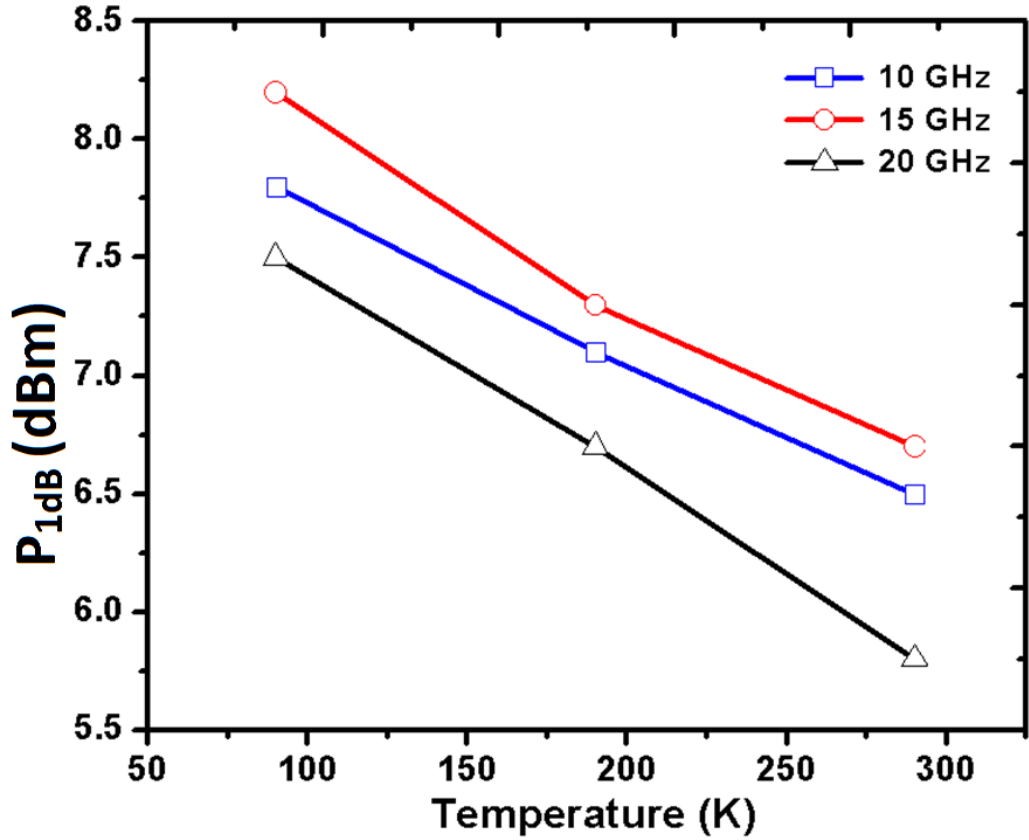
$$V_{od} = V_{GS} - V_{TH} \tag{13}$$

Figure 23: Measured P_{1dB} of the SPST switch during cryogenic operation.

In Equations 11, 12, and 13, v_{sat} is the saturation velocity, μ_0 is the low-field mobility, "L" is the transistor gate length, R_s is the input impedance (e.g., assume

a 50 Ω), and θ is the mobility factor due to the applied perpendicular electric field. According to Equation 11, P_{1dB} can be improved by increasing V_{od}, the gate over-drive voltage however, this causes the power consumption to increase, which can be a problem for certain applications where power is a concern. Cryogenic operation provides the enhancements (P_{1dB}, insertion loss and isolation) without the penalty of additional power consumption. Another interesting observation in Figure 23 is the improved power handling response of the switch at 15 GHz in comparison to the other two frequency points, 10 GHz and 20 Ghz. One possible explanation is the impedance of the switches been better better matched at 15 GHz (closer to 50 Ω), in contrast to the other two frequency points. However, further investigation is needed to confirm this assumption.

3.2.2 Measured SP4T Cryogenic Results

As anticipated, the insertion loss of the SP4T switch also improves as temperature is lowered to cryogenic temperatures (Figure 24). For instance, at 20 GHz the insertion loss is approximately -8 dB at room temperature, and for the same frequency point it reduces to -6.5 dB and -4.8 dB at 190 K and 90 K temperature points, respectively. The SP4T circuit show more than 3 dB insertion loss improvement from 10 to 40 Ghz. The return loss (S_{11}), also improves with decreasing temperature at low frequencies (Figure 25). However, at around 25 GHz the data shows some oscillations at 190 K and 90 K, and it is probably because of loss of calibration at these two temperature points.
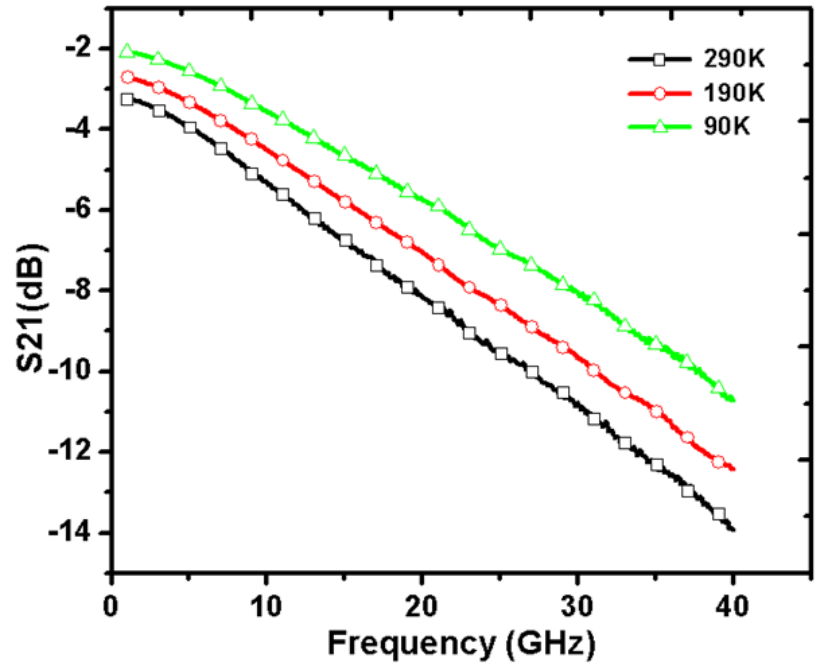
Figure 24: SP4T insertion loss (S_{21}) during cryogenic operation.
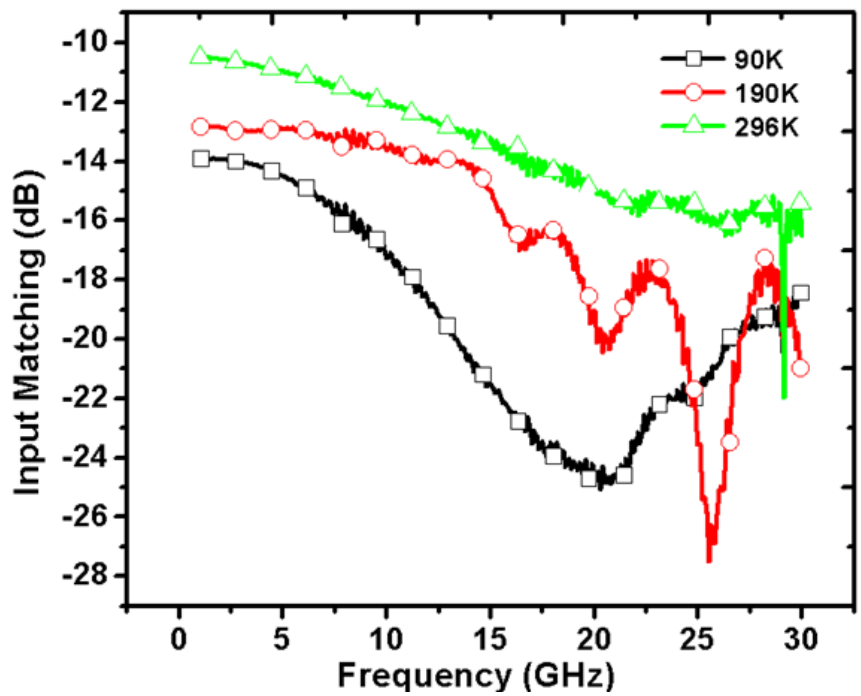
Figure 25: SP4T return loss (S_{11}) during cryogenic operation.

The isolation (S_{21} when switch is off) from input-to-output terminals follows similar trend as the SPST data at low frequencies (< 5 GHz) and at high frequencies ($>$ 25 GHz. However, at mid-band frequencies (10 GHz to 25 GHz) the data shows a higher isolation improvement with the decreasing temperature, approximately 10 dB at 15 GHz. One possible explanation for this mid-band isolation improvement is the constructive interaction of the parasitic capacitances at the output node of the SP4T circuit (see Figure 9) presenting a better impedance matching at these frequencies. But, it does not follow the same trend at lower and higher frequencies.
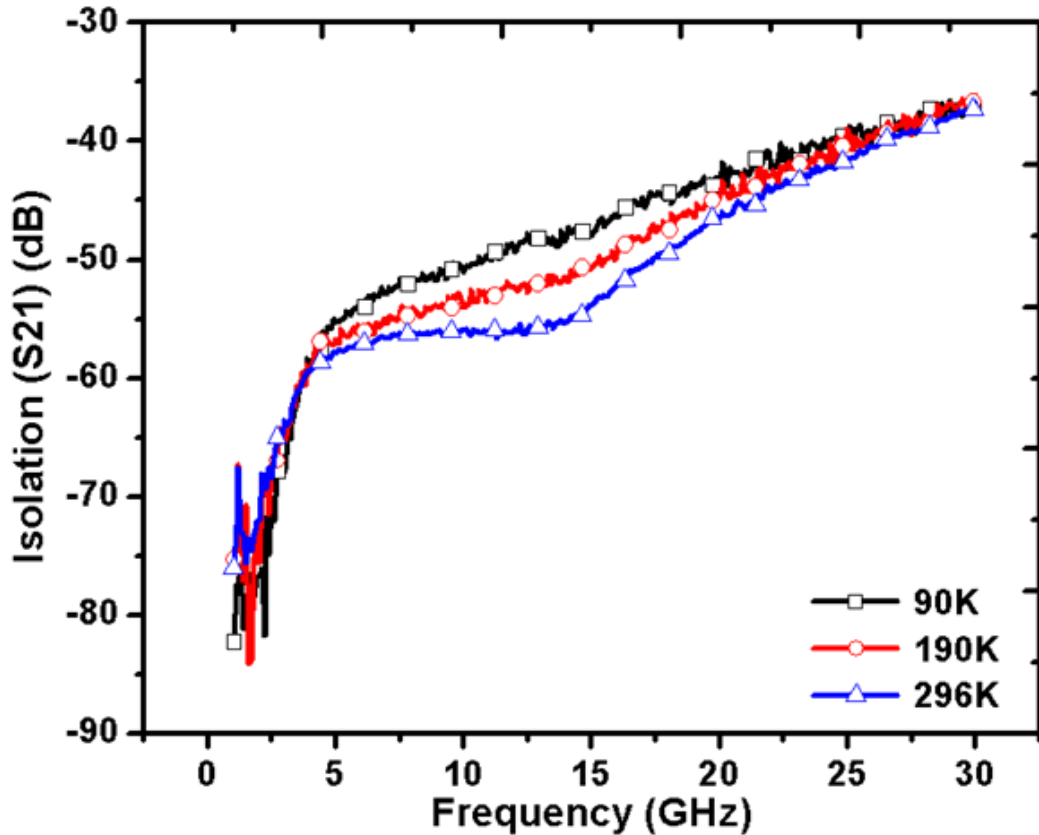
Figure 26: Isolation for SP4T switch during cryogenic operation.

The SP4T P_{1dB} plot, Figure 27 is comparable to the SPST switch power handling capability graph in Figure 23). For all the three frequency points, 10 GHz, 15 GHz and 20 GHz, P_{1dB} improves more than 1.5 dB from room temperature (300 K) to

cryogenic temperature (90 K). As stated previously, the reason for this improvement is attributed to the direct dependence of P_{1dB} to the effective carrier mobility shown in Equation 11 as "μ_1". This is particularly attractive to multiband applications, since the switch is likely to be interfaced with different type of circuits (e.g., Power Amplifiers, Low Noise Amplifiers) that may have a wide range of power handling demands. Once again, the P_{1dB} plot shows higher power handling at 15 GHz in contrast to the other two frequency points. As mentioned before, this maybe because the switch is better matched at this particular frequency in comparison to the other two frequencies, 10 GHz and 20 GHz.
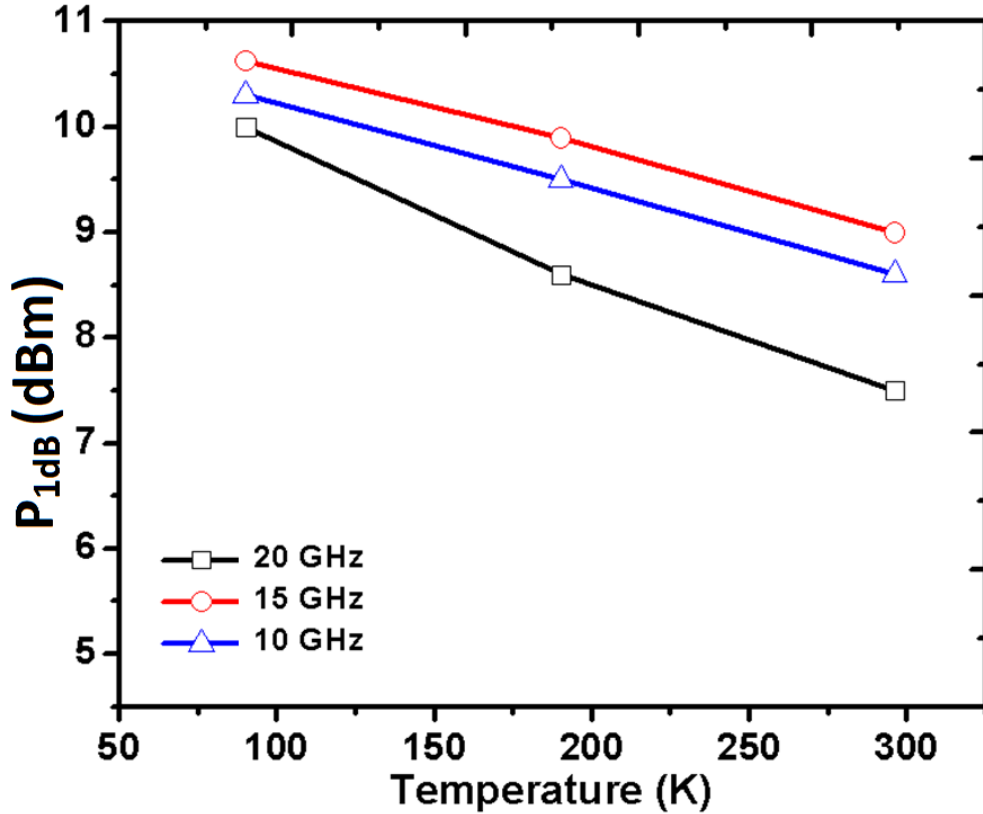
Figure 27: Measured P_{1dB} of the SP4T switch during cryogenic operation.

3.2.3 P_{1dB} Measurement Setup Methodology

For the room temperature measurements presented in the previous chapters, an integrated S-parameter, noise figure, and load-pull system (see Figure 6) was used to characterize the power handling capability (P_{1dB}) of the switches. However, the same setup is not available for an on-wafer characterization using the open cycle cryogenic station TTP6 (see Figure 19), and because of this a "2-tier fixture calibration" procedure is required. This procedure allows us to accurately account for both input and output losses added by components (e.g., coupler, isolator, cables, probes).

The probed power measurement setup shown in Figure 28, consists of a signal generator (HP E83732A), a power meter (Agilent E4419), a wideband amplifier (HMC-C004), bi-directional coupler (Agilent 87301D), and a on-wafer cryogenic dewar chamber (TTP6). The isolator (shown in dashed red lines) was not needed since the Device Under Test (DUT) was well matched ($>$ -10 dB across the frequency of interest). This setup allows us to known the actual power measured at the input of the DUT (the through path of the coupler) while using the coupled port as reference.

Figure 28: On-wafer probed power measurement setup used on a open-cycle cryogenic station.

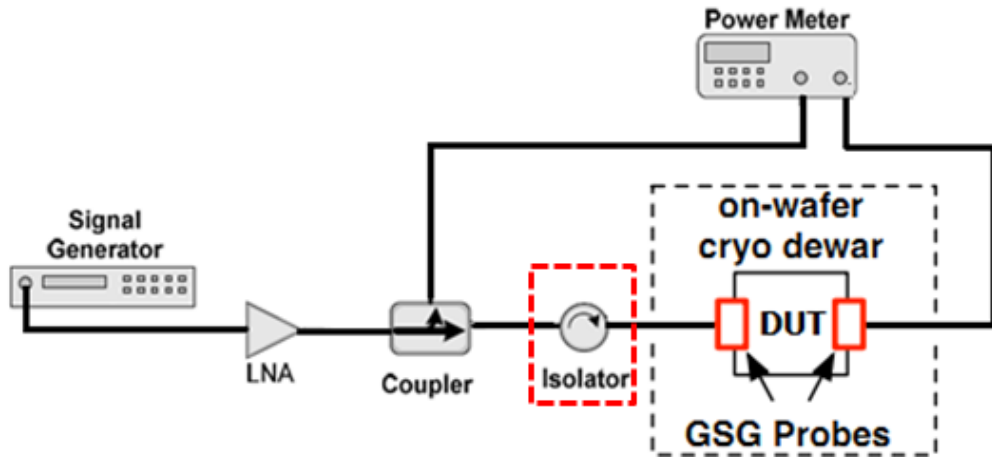To account for the losses between the signal generator and the DUT (switch test structures), a "2-tier fixture calibration" procedure needs to be performed. At the end of this procedure, three files will be created: an input file, an output file and a input-coupled path file that will be used to deembed the measurement to the reference plane at the DUT pads. The first step is to verify the input coupled path using a VNA (Agilent E8364B PNA); Figure 29 shows the test setup used. The red dash lines around the "isolator" block means that it was not used on this experiment, however, it is recommend in case the DUT has a poor input match (S_{11}). The result file needs to be saved in units of dB using the ".s2p" file format (e.g., file name "Input-Coupled-Path"). The coupling factor depends on the loading termination (return loss, S_{11}) of the output port of the coupler; therefore, a 50 Ω termination is needed at the "thru" path of the coupler. In case of poor input match an isolator should be used (marked in red dashed lines in Figure 29), and if it used, it needs to be accounted for in the input-coupled path measurement. The next step after verifying the input coupled path is to perform a cable level calibration using coaxial calibration standards and the results is to be saved in the ".s2p" file format (e.g., file name "Cable-Cal.s2p").
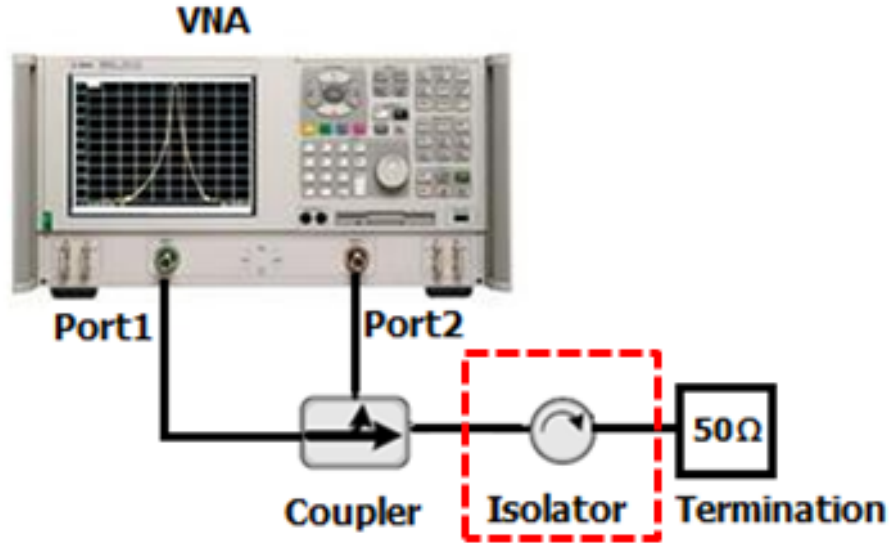
Figure 29: Measurement setup to verify the input coupled path loss.

The final step in this procedure is to perform a probe level calibration using the setup shown in Figure 30. . In this test setup, the coupled path of the coupler is terminated using a 50 Ω termination standard, SOLT calibration substrate is used with an VNA to capture the S-parameters. The files need to be saved as ".s2p" file format (e.g., file name "Probe-Tip-Cal.s2p"). Once this calibration is complete, the VNA (Agilent E8364B) can be used to create the input and output deembedding fixture files. The procedure is as follows (please note that this instructions are specific to this particular Agilent E8364B VNA):

- Go to System $\rightarrow$ Macro $\rightarrow$ AdapterChar

- Select Calset1 as the "cable-cal.s2p"

- Select Calset2 as the "probe-tip-cal.s2p"

- Port 1 setting creates the Input Fixture Deembed Loss file (IFDL file)

- Port 2 setting creates the Output Fixture Deembed Loss file (OFDL file)

The results from the IFDL and OFDL files can either be transferred to the Agilent power meter over frequency manually or by using a GPIB directly into a table. Another option is to manually subtract the losses using an excel sheet and the following two Equations, Actual Input-Power (AIP) Equation 14 and Actual Ouput-Power (AOP) Equation 14, both referencing to the input pads of DUT:

$$AIP = (MeasuredPoweratPortA) - (Input - Coupled - Path) + (IFDL) \quad (14)$$

$$AOP = (MeasuredPoweratPort1) - (Input - Coupled - Path) + (OFDL) \quad (15)$$

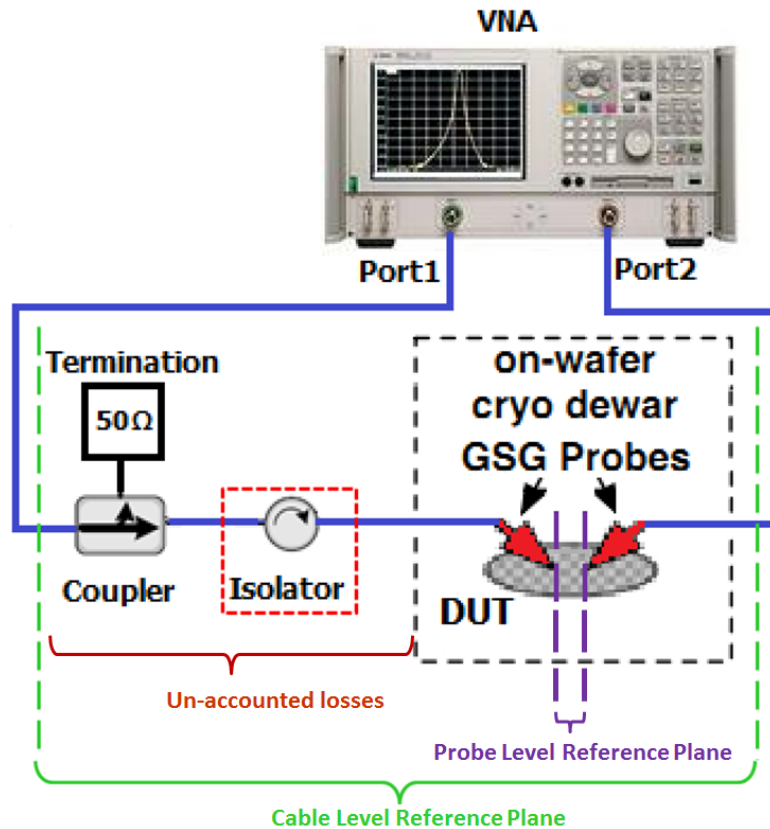where, "PortA" and "PortB" refers to the output ports of power meter.

Figure 30: Probe level calibration measurement setup to deembed for un-accounted equipment and cable losses.

CHAPTER IV

CONCLUSION AND FUTURE WORK

This thesis has presented the design, simulation, measurement results of single-pole single-throw switches (SPST), and single-pole four-throw (SP4T) switches, based on bulk and Triple-Well n-channel Field Effect Transistors (nFETs). According to the results presented, several of the key-figures-of-merit for a switch, like insertion loss, isolation, and power handling capability (P_{1dB}) improve at cryogenic temperatures. These results are important for several applications, including space-based extreme environment application where FET based circuits would need to operate reliably across a wide-range of temperature.

The novelty of this work lies in the proposed new topology of an ultrahigh-isolation single-pole, single-throw (SPST) and a single pole, four-throw (SP4T) nMOS based switch for multiband microwave radar systems. This includes the effect of cryogenic temperature on these circuits and devices. To the best of the author's knowledge, this work investigates the effects of cryogenic temperature on the performance of RF switch circuits for the first time. Through characterization of device test structures (both standard bulk and TW nFETs) it leads to better understanding and analysis of the measured results observed on the switch circuits.

In summary, SiGe BiCMOS technologies have demonstrated great potential for extreme environment applications (e.g., space exploration, satellites communication, automotive, drilling). However, further investigation is warranted in order to have a more comprehensive understanding of nFET based RF circuits operating in extreme environments (i.e., radiation rich environments with wide temperature fluctuations, e.g., the moon -180 °C to + 120 °C). Consequently, the author would suggest the

following extensions to this work. First a detailed study of high temperature and radiation effects on nFET based switches. Next step would be to combine low and high-temperature and radiation studies in a radiation measurement setup. This would entail irradiation of the circuits over a wide operating temperature while monitoring their RF performance. Such experiments would provide a comprehensive set of data to analyze the interaction of various factors involved. Lastly, to complement the measurements with TCAD simulations to analyze the design trade-offs and identify potential solutions that could mitigate adverse effects from extreme environment operation.

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