Polarization Based Digital Optical Representation, Gates, and Processor

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Polarization Based Digital Optical Representation, Gates, and Processor

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SUMMARY

A complete all-optical-processing polarization-based binary-logic system, by which any logic gate or processor could be implemented, was proposed. Following the new polarization-based representation, a new Orthoparallel processing technique that allows for the creation of all-optical-processing gates that produce a unique output once in a truth table, was developed. This representation allows for the implementation of all basic 16 logic gates, including the NAND and NOR gates that can be used independently to represent any Boolean expression or function. In addition, the concept of a generalized gate is presented, which opens the door for reconfigurable optical processors and programmable optical logic gates. The gates can be cascaded, where the information is always on the laser beam. The polarization of the beam, and not its intensity, carries the information.

The new methodology allows for the creation of multiple-input-multiple-output processors that implement, by itself, any Boolean function, such as specialized or non-specialized microprocessors. The Rail Road (RR) architecture for polarization optical processors (POP) is presented. All the control inputs are applied simultaneously, leading to a single time lag, which leads to a very-fast and glitch-immune POP. A simple and easy-to-follow step-by-step design algorithm is provided for the POP, and design reduction methodologies are discussed. The algorithm lends itself systematically to software programming and computer-assisted design.

A completely passive optical switch was also proposed. The switch is used to design completely passive optical gates, including the NAND gate, with their operational speeds only bound by the input beams prorogation delay. The design is used to demonstrate various circuits including the RS latch.

Experimental data is reported for the NAND and the Universal gate operating with different functionality. A minute error is recorded in different cases, which can be easily eliminated by a more dedicated manufacturing process. Finally, some field applications are discussed and a comparison between all proposed systems and the current semiconductor devices is conducted based on multiple factors, including, speed, lag, and heat generation.

CHAPTER I

INTRODUCTION

1.1 The problem

Binary logic operations rely on systems that can produce only two states of output: zero and one. It is important for physical systems to have both values be non-zero quantitatively, and be easily distinguishable from one another. The current electronic binary logic systems use a low voltage as zero, and a higher voltage as one. This representation has reached its physical limits with the current semiconductor industry, mainly due to excessive heat and attenuation problems. Those problems have not only limited the speeds of microprocessors but have also imposed design restrictions. In an effort to find new solutions to the problem, scientists have turned to quantum and optical computing.

In this dissertation, we introduce a set of new devices, as well as a novel representation for binary logic. The devices consist of electro-optical simple logic gates, electro-optical gates representing complex Boolean expressions via a standardized procedure, a novel all-optical polarization switch, and passive all-optical simple gates. These devices address many of the problems that have made optical computing less feasible, such as optical regeneration. For many decades optical regeneration has been the major problem that prevented the embodiment of optical

computers. The problem prevents optical gates from being easily cascaded, requiring frequent conversions between optical building blocks and creating immense delays in the system, preventing it from benefiting from the speed of an optical device. The essence of the problem lies within the intensity based representation, which could be avoided all together with the new proposed representation.

Even though the advantages of optical computing are many, the most important and obvious one is speed. First and foremost, the speed of operation would be limited only by the speed of light, which becomes evident in passive designs. Other advantages include parallelism, reversibility, jamming resilience, and the removal of the design constraints forced by transistor losses. The latter also allows for the introduction of the proposed Rail Road architecture, in non-passive systems, for computation designs that result in simultaneous switching, causing any complex calculation to go only through one cycle of switching no matter how complex the system is.

1.2 Origin and History of the Problem

The use of the two horizontal and vertical polarization states of an electromagnetic wave to implement binary logic gates has been of great interest since the 1980s. The two states of polarization were used to represent logic one and logic zero. A speculative account of the combination of nonlinear optics and polarization optics that held good promise for binary optical logic [1], a logic based on spatial

filtering polarization [2], a suggested implementation of the 16 logic functions of two input patterns based on the birefraction of uniaxial crystals [3], a suggested implementation of the 16 two-input logic operations by use of the recording and readout of photoinduced volume gratings in photorefractive crystals [4], only XOR and XNOR realization utilizing ferroelectric liquid crystals [5], vertical/horizontal input logic representation and on/off output logic representation for N-input gates [6], 2D data array logic gates using an improved polarization-logic algebra [7], shadow-casting logic units using masks and on/off logic representation [8-10], shadowgram-based Boolean logic gates [11-12], logic gates using laser-excited gratings [13],and logic gates based on digital speckle pattern interferometry [14], are examples of concerted efforts devoted to the subject.

The majority of the previous work focuses on representing digital systems optically by intensity. The previous polarization-based representation converts the signal to intensity-based representation at some point within the system. Moreover, no one was able to represent any gates other than the special case of the two gates XOR and XNOR [5], due to the symmetric translation of their truth table [15]. The latter marks the road block and the end of the previous work on polarization-based representations.

While research on polarization-based representation slowed down, various intensity-based representations were implemented, none of which is an actual digital system. The gates require masks at the output to interpret the results. These masks not only slow down the system, but also prevent the gates from being cascaded, and

impose the requirement of signal regeneration at every zero representation, slowing the system even further [8-12]. Other more complex solutions were proposed to improve the feasibility of intensity-based systems, but the results always are non-digital, prevent cascading, require machine interpretation, and have a direct effect on reducing the speed.

1.3 Organization

This dissertation is organized into 8 chapters. The first chapter discusses optical computing, associated problems, the previous work and the motivation behind the research.

The second chapter introduces the new general representation for digital logic and examines the system under different specific cases. It also examines and investigates the various components that can be used for the representation. This chapter also includes the optical gate designs for simple XOR and XNOR, the only 2 gates that do not require the Orthoparallel representation.

Chapter 3 Introduces and discusses the Orthoparallel representation. The Orthoparallel representation is used to design all 16 basic logic gates including the NAND which is considered the building block for digital logic circuits.

Chapter 4 introduces and discusses the polarization optical processor along with the general algorithm. The algorithm allows for a systematic approach to design any digital system, given its operational truth table. Multiple step-by-step examples

are provided for demonstration. The chapter also discusses electro-optical elimination and cascading.

Chapter 5 introduces and discusses passive all optical switches and gates. The stationary passive switch operates at the speed of light with no moving parts and immediate response. The switch is used to create gate designs, including the NAND gate, which is considered the building block for digital logic circuits.

Chapter 6 reports on the performance of laboratory constructed gates. Construction and components used are also discussed.

Chapter 7 Introduces and discusses the reconfigurable Universal gate. The gate demonstrates the versatility of optical systems, by having various modes of operation. The performance of the gate is also reported.

Chapter 8 discusses and compares the various gates and designs introduced against semiconductor based devices. Finally, future work is also discussed and conclusions are reported.

CHAPTER II

GENERAL REPRESENTATION

2.1 Introduction

Binary logic operations rely on systems that can produce only two states of output: zero and one. It is important for physical systems to have both values be non-zero quantitatively, and be easily distinguishable from one another. The current electronic binary logic systems use a low voltage as zero, and a higher voltage as one.

We propose using any polarization state and its negation, orthogonal state, as zero and one. Such representation allows the creation of extremely fast optical gates and binary systems that are far more superior to current semiconductor-based systems.

The new proposed system representation allows the implementation of much faster systems, since its output is bound by the speed of light and its input by the optical, electronic, or mechanical control system. It is important to note that the gate processing virtually generates no heat, and accordingly does not suffer from heat problems as in semiconductors. Furthermore, the system can be optimized to minimize the control parts, in many cases to a single element delay even in cascaded systems that represent complicated Boolean functions.

Due to the fact that the unforced new representation produces an output in the form of a beam that mainly retains the original intensity but only differ in polarization

state, the system can be infinitely cascaded to produce the desired functions. Such advantages allow the design and implementation of self sufficient units of microprocessors that include inverters, XOR, and XNOR gates.

Our system, in one of its realizations, only utilizes two different cheap components as needed: thin-film wave retarders, and thin-film wave polarizers. The materials of the thin-film system can be selected to optimize various aspects of the operation, including cost. Previous polarization-based optical logic realizations do not satisfy the general input/output condition at which the difference between logic zero and one is always 180° in the ρ plane, or alternatively polarized in the negative direction, orthogonal. Only work with the special case of parallel and perpendicular polarizations to the system of axes, p and s polarizations, is reported. The new representation allows for easily inverting the input or the output without altering the operation of the system, following the well established digital logic rules. Furthermore other systems incorporate expensive materials such as uniaxial crystals or nonlinear optical elements, or incorporate complicated parallel procedures of beam splitting and interference. Most of these previous systems also rely on the intensity of the output beam to distinguish between the logics zero and one, which prevents cascading (requires regeneration of the beam) and involves semiconductor-based photo-detectors at each gate which significantly add to the cost, and slows down and complicates the system.

2.2 Components

In this section we discuss the two types of components that compose the system; retarders and polarizers. In general, the most complex architecture of the logic gates discussed in this dissertation employs a general polarization device (GPD). It introduces a relative amplitude attenuation of any chosen value, tan ψ, and a relative phase shift Δ also of any chosen value, between the two orthogonal components of the electric vector of the electromagnetic wave parallel (p) and perpendicular (s) to the plane of incidence or transmission. In the case of reflection from a thin-film system (TFS), the polarization transfer function ρ (PTF) is given by

$$\rho = R_p / R_s = \tan \psi \exp (j \Delta), \qquad (1)$$

where R_p and R_s are the complex amplitude reflection coefficient [16, 17]. A similar expression for the case of refraction through a TFS is given in terms of τ_p and τ_s, the complex transmission coefficients [18]. The TFS might be a film-substrate system, an unsupported film (pellicle), a bare substrate, or any other optical device.

In addition to TFSs, a GPD can also be made of birefringent crystals in the standard common way, and electro-optic devices may also be used.

Retarders and polarizers are special cases of the GPD, as we discuss in the following subsections.

The input-output amplitude transfer function (ATF) for any TFS is equal to $|\rho|$. For a succession of TFSs, the resultant TFS for the system is the product of all.

The absorption losses in a TFS depend on the choice of materials. If we choose a transparent, i.e. non-absorbing, material(s), then no absorption takes place. The coupling efficiency for a TFS is 100%. Also, the contrast, which is defined as the ratio between the input optical power and the output one when a 0 or 1 state is expected at the output is given by the relative intensity

$$RI = (|R_p|^2 + |R_s|^2), \quad (2)$$

where a TFS can be designed for an RI > 0.99.

2.2.1 Retarders

Retarders are devices that are designed to produce in the output wave a certain relative phase shift Δ while preserving the relative amplitude (magnitude) of the input wave unchanged; $\tan \psi = 1$. Therefore, no relative amplitude attenuation is introduced.

For the purpose of our application, we use one of three types of retarders, or a combination thereof, as needed; thin-film reflection type, thin-film transmission type, or non-thin-film type. Note that simple thin-film systems are used in logic implementation for the first time. In the following subsections, we briefly discuss all three.

2.2.1.1 Reflection-type retarders

This section discusses two different types of Reflection-type retarders: Thin-Film and Pellicle.

2.2.1.1.1 Thin-film (film-substrate) reflection retarders

Thin-film reflection (TFR) retarders are simply a film-substrate system where a thin film is deposited over a substrate, which operates in the reflection mode [16, 17, 19, 20]. The most widely used one is the SiO2-Si system, which is used in the semiconductor industry. When employed as a TFR retarder device, it produces the required retardation angle Δ to the electromagnetic wave, laser beam, upon reflection at the surface of the device at the design angle of incidence. For example, a quarter-wave TFR retarder produces a 90° phase shift between the two p- and s-components, TM and TE components, respectively. A general retarder produces a retardation value of Δ; accordingly, any light beam that is reflected from the device has an added phase difference of Δ between the two components of the electric vector of the input wave. For example, if the incident wave is a linearly polarized light at +45°, the reflected wave emerges a right-handed circularly-polarized wave if $\Delta = 90°$. On the other hand, if the incident wave is linearly polarized at -45°, the reflected wave emerges a left-handed circularly-polarized wave for the same value of Δ.

The film-substrate system is divided into three categories depending on the relative values of the optical constants of the ambient N_0, of the film N_1, and of the substrate N_2. When $N1<(N_0N_2)^{1/2}$ it is a negative system, when $N_1=(N_0N_2)^{1/2}$ it is a zero system, and when $N_1>(N_0N_2)^{1/2}$ it is a positive system. The performances of the

three categories in reflection and in transmission are drastically different as the film thickness and angle of incidence are changed [17].

TFR retarders can be realized using negative and zero film-substrate systems. They cannot be realized using positive film-substrate systems. Any TFR retarder of any retardation angle can be designed and realized using a negative film-substrate system; $0 \leq \Delta \leq 360°$ except $\Delta = 0$ and $\pm 180°$. With a reasonable tolerance, the TFR retarders of $\Delta = 0$ or $\pm 180°$ can be designed and implemented. For an exact retarder with a zero tolerance, two TFR retarders of $\Delta = \pm 90°$ can be used. Also, any two TFR retarders with the sum of their retardation angles equal to $\pm 180°$ can be used.

Only one exact TFR retarder can be designed and realized using a zero film-substrate system; a TFR retarder of $\Delta = 0$. That is a special case of TFR retarders where the retardation angle is zero, where it doubles as a polarization-preserving device (PPD). That device produces an electromagnetic wave polarization-identical to the input electromagnetic wave, hence a PPD.

Other TFR retarders with any selected retardation angles, within a certain range that is material and wavelength dependent, can be designed and implemented within a certain tolerance of choice using zero film-substrate systems [21].

2.2.1.1.2 Pellicle reflection retarders

Pellicle reflection (PR) retarders are retarders designed using a pellicle, which is an unsupported (embedded) thin film [16]. They provide the required retardation angle Δ upon reflection without introducing any relative amplitude attenuation. Their design procedure is similar to that of TFR retarders. Their performance differs from

that of TFR retarders in the tolerance of each device to changes in the design parameters; optical constant, film thickness, and angle of incidence.

2.2.1.2 Transmission-type retarders

This section discusses two different types of transmission -type retarders: Thin-Film and Pellicle

2.2.1.2.1 Thin-film (film-substrate) transmission retarders

Thin-film transmission (TFT) retarders are simply a film-substrate system, where a thin film is deposited over a substrate, which operates in the transmission mode [18, 22, 23]. When employed as a TFT retarder device it produces a required retardation angle Δ to the electromagnetic wave, laser beam, upon transmission through the device at the design angle of incidence. TFT retarders cannot be designed to produce any retardation angle. TFT retarders are also represented on the complex τ-plane in a similar way to that of the complex ρ-plane, see Section 2.3.

TFT retarders can be designed using negative, positive, and zero film-substrate systems. When using negative or positive film-substrate systems, TFT retarders can be designed and implemented to produce values of Δ in certain ranges depending on the optical constants and wavelength of operation of the device. When using zero film-substrate systems, the only TFT retarder that can be designed is that of a retardation angle of $\Delta = 0$. As for the case of a TFR retarder, the zero-retardation TFT doubles as a PPD [21].

2.2.1.2.2 Pellicle transmission retarders/transmission polarization-preserving device

The Pellicle transmission (PT) retarder is a retarder of a retardation angle of $\Delta = 0$, which is designed and realized using a pellicle. It is the only exact PT retarder that can be designed and implemented using a pellicle. As before, it also doubles as a PPD [24, 25].

2.2.1.3 Angle-of-incidence tunable retarders

Angle-of-incidence tunable (AIT) retarders are retarders that change their retardation angle Δ with the angle of incidence. That tunability allows for use of the same retarder at different angles of incidence to produce different retardation angles. Therefore, in an optical system, a single retarder can be designed and implemented to function at different parts of the system, and or at different angles of incidence, instead of designing and producing several designs for the same gate. That's easier to implement and more economical. It also provides for tuning the whole system in a practical way [26].

2.2.1.4 Non-thin-film retarders

Non-thin-film (NTF) retarders are made of birefringent crystals, or other systems, that would provide a retardation angle into the emerging beam, with reference to the incident beam, based on the crystal having two different optical constants depending on the direction of propagation of the beam within the crystal itself with reference to its optic axis. Those retarders are much more expensive and difficult to make.

The design of these devices is discussed more thoroughly in Reference [27]. It is important to note that the device can be constructed of several materials of choice.

2.2.2 Polarizers

Polarizers are devices that produce a linearly polarized light beam where the two components of the beam are in phase in the time domain.

2.2.2.1 Thin-film polarizers

As the retarders, or as any other thin-film polarization device, thin-film (TF) polarizers are of two main types, reflection and transmission. Each type is either constructed of a film-substrate system or of a pellicle (unsupported film). The only difference is in the value of the relative amplitude attenuation and relative phase shift produced by the device upon reflection or transmission. In the polarizer case, we have three categories, a p-suppressing polarizer, an s-suppressing polarizer, and a linear partial polarizer.

2.2.2.1.1 Linear-partial polarizer (LPP)

It is a TFS that produces a relative amplitude attenuation to the electromagnetic wave upon interacting with the device, in addition to a 0 or 180° relative phase shift. It is represented by the real axis of the complex ρ-plane, see Section 2.3.

2.2.2.1.2 p-suppressing polarizer (PSP)

It is a TFS that eliminates the p-component of the electromagnetic wave upon interacting with the device. It is represented by the origin of the complex ρ-plane, see Sec. 3. Note that it is a limiting case of the LPP where the emerging wave is TE polarized.

2.2.2.1.3 s-suppressing polarizer (SSP)

It is a TFS that eliminates the s-component of the electromagnetic wave upon interacting with the device. It is represented by the point at infinity of the complex ρ-plane, see Section 2.3. Note that it is also a special case of the LPP where the emerging wave is TM polarized.

2.2.2.2 Non-thin-film polarizers

Non-thin-film (NTF) polarizers are made of birefringent crystals, or any other system, and are sometimes called birefringent polarizers. They use the fact that the entering beam to the crystal is divided into two beams each traveling through the crystal at a different speed. The output of the polarizer is a linearly polarized beam with a specific relation between the two components parallel and perpendicular to the plane of incidence, retardation angle of $\Delta = 0$ and a relative amplitude determining the angle of inclination of the linearly polarized light to the plane of incidence. That angle can be changed by rotating the crystal around the beam axis.

An NTF polarizer only passes the electromagnetic wave component in its polarization direction. If the wave is linearly polarized perpendicular to the polarization direction of the polarizer, the output of the polarizer is then zero; no wave emerges.

2.2.2.3 Electro-optic devices

In general, an electro-optic device is one that provides interaction between an electric signal and an optical characteristic of the device. In that sense, it is a transducer/sensor. We only consider those electro-optic devices that provide a

rotation of the electric vector to represent an electric signal directly or indirectly. Examples of transducer/sensor phenomenon are Kerr effect, magneto-optic effect, or a faraday rotation due to propagation through a material. An example of the electro-optic device is the use of liquid crystals to produce a rotation of a polarized light in response to an electric signal.

2.3 Binary-Logic Representation

The complex ρ-plane is defined as the complex plane at which the ρ vector represents the relative phase difference and relative amplitude attenuation of the two components, p and s, of the electric vector of the electromagnetic wave discussed before. The complex ρ-plane is used to represent both the polarization state of the wave and the optical components discussed in the previous section; retarders, polarizers, and GPDs. In this study, we use the complex ρ-plane and ρ vector extensively to illustrate how the architecture of different designs can be achieved, and how they function, using the new binary logic representation. The complex ρ-plane is replaced by the complex τ-plane when we use transmission devices.

2.3.1 Polarization-state representation

Each point in the complex ρ-plane represents a different state of polarization of the electromagnetic wave. The positive (negative) real axis represents linearly-polarized waves, where there is a zero (180°) phase shift in the time domain between the p and s components of the wave, or light beam. Each point on the real axis

represents a light beam with a different relative amplitude; between the p and s components. That relative amplitude determines the polarization angle of the beam P, measured counterclockwise from the x-axis of the coordinate system. P is zero at the origin, increasing in the positive direction of the real axis to +90° at infinity, and decreasing in the negative direction of the real axis to -90° at negative infinity. Note that ±90° represent the same linearly polarized light.

Points on the imaginary axis of the complex ρ-plane represent elliptically polarized light with a phase difference in the time domain of +90° on the positive part of the axis and of -90° on the negative part. That leads to elliptically polarized light.

Any straight line passing through the origin represents different polarization states of equal phase shift in the time domain. Accordingly, each polarization has a different relative amplitude. On the other hand, any circle with its center at the origin represents different polarization states of equal relative amplitude; and accordingly of different phase shifts.

Some additional points of interest in the complex ρ-plane are the points ρ = (+1, 0), ρ = (-1, 0), and those on the unit circle. The point ρ = (+1, 0) represents a linearly polarized light with P = +45°. The point ρ = (-1, 0) represents a linearly polarized light with P = -45°. The points on the unit circle represent retarders with different retardation angles. Of special interest on the unit circle are the two points (0, +1) and (0, -1). The first represents right-handed circularly-polarized light, and the second represents left-handed circularly-polarized light.

Each of the two components of the two pairs of (+1, 0) and (-1, 0); and of (0, +1) and (0, -1), is orthogonal to the other. That orthogonality property is very important and is a key in our binary representation.

2.3.1.1 Orthogonal polarization states

Two polarization states are said to be orthogonal if, and only if, they satisfy the condition;

$$\rho_1^* . \rho_2 = 0, \qquad (3)$$

where ρ_1 and ρ_2 are the two ρ-vectors representing the two polarization states in the complex ρ-plane. ρ_1^* is the Hermitian adjoint of ρ_1; the transposed complex-conjugate. Accordingly, any two origin-symmetrical points on the unit circle; two points on the unit circle joined by a straight line through the origin, represent two orthogonal states.

In general, two points in the complex ρ-plane are orthogonal if they are joined by a straight line going through the origin and the magnitude of one is the reciprocal of the other; distance from the origin.

2.3.2 Polarization-device representation

We do have two types of polarization devices, thin-film (TF) and non-thin-film (NTF) types. We have two types of representation for each; passive device representation and active device representation.

2.3.2.1 Passive-device representation

The passive-device representation for both TF and NTF types is the same in the complex ρ-plane; by a point which represents the device polarization state. For example, a linear partial polarizer is represented by a point on the real axis representing its relative amplitude attenuation P, and a retarder is represented by a point on the unit circle representing its relative retardation angle.

2.3.2.2 Active-device representation

The representation of a device in action, active-device representation, is a manifestation of the device action in the complex ρ-plane. That is representing the effect of the interaction of the beam with the device.

2.3.2.2.1 Thin-film devices

The interaction of a beam with a thin-film (TF) device is represented by the resultant of the vector multiplication, dot product, of the two ρ vectors representing the beam and the device. For example, if a linearly-polarized light at +45° reflects at the surface of a TFR retarder of $\Delta = +90°$ (right-handed circular retarder), the output beam is a right-handed circularly polarized light. On the other hand, if the input beam is right-handedly circularly polarized, the output beam is then linearly polarized at -45°. Also, a left-handed circularly polarized beam comes out a TFR retarder of $\Delta = -90°$ (left-handed circular retarder) linearly polarized at +45°.

2.3.2.2.2 Non-thin-film (NTF) devices

The interaction of the beam with the device is represented by a ρ-vector derived using either Jones or Stokes matrix representation [28]. For any two orthogonal polarizations, the representing ρ vectors should satisfy Eq. (3). For simplicity, and to mention a few, we only consider the special cases of polarization states of linearly polarized at +45°, linearly polarized at -45°, right-handed circularly polarized, and left-handed circularly polarized. As mentioned before, the first two polarization states are orthogonal to each other and the second two are also orthogonal to each other. If one of the two polarization states is that of the beam and the other is that of the polarization device, the output is null; no beam outputs the device. If the laser beam and the polarization device are having the same state of polarization, the beam emerges from the device as is; unchanged.

2.4 System Realization

System realization is achieved through the design of logic gates that can be cascaded together. The most general design of a logic gate is one where the laser beam has its own polarization state, and where also each of the two components, e.g. thin-film substrate systems, comprising the logic gate has its own different polarization state. Since any polarization state is represented by a vector in the complex ρ-plane, then we have two parameters to work with; the magnitude and phase of the vector representing the relative amplitude attenuation tan ψ and relative

phase shift Δ of the laser upon reflection at, or transmission through, the film-substrate, or other, systems. For simplicity, we keep one of the two constant and change the other to achieve our design. Accordingly, we have two types of gate designs; constant-ψ and constant-Δ designs. Again, the simplest one of each type is discussed; the unit circle where tan ψ = 1 and the horizontal axis where Δ = 0 or 180°. Those two types of binary gates pave the way easily to the most general, and complex, case where both tan ψ and Δ simultaneously change.

We conclude, for each case, with the design of a general logic gate that satisfies the two conditions: 1) the laser beam carries the binary information on the optical input and output of the gate. That provides for cascading of an unlimited number of gates. 2) The two binary controls of a gate are provided by an electronic input signal.

A second gate architecture uses the laser beam as the medium carrying the information and as one of the two control inputs to the gate. The other control input is an electronic input signal.

2.4.1 Two-electronic-signal (TES) architecture

A general two-electronic-signal (TES) architecture binary gate is constructed of a collection of optical devices that are cascaded together, Figure 1. Each device is, for example, a thin-film polarization device that is designed to take two states, e.g. positions, and produce a cretin general retardation angle at one position (logic one: L1), and its orthogonal counterpart; orthogonal image through the origin at the second position (logic zero: L0). Therefore L1 and L0 are represented by two orthogonal states of polarization. The change of state is carried out using an electronic signal.

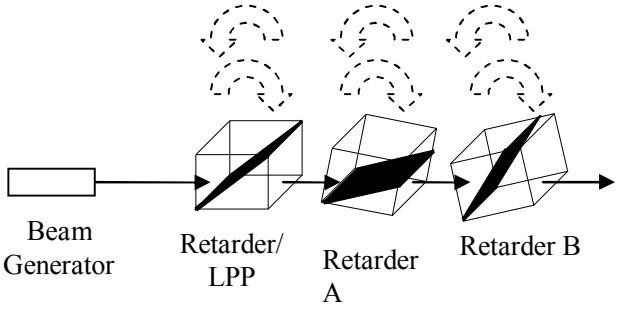

Figure 1 General two-electronic-signal (TES) binary gate architecture is constructed of a collection of optical devices that are cascaded together. Each device is a thin-film polarization device, or an electro-optic device, that is designed to take two states.

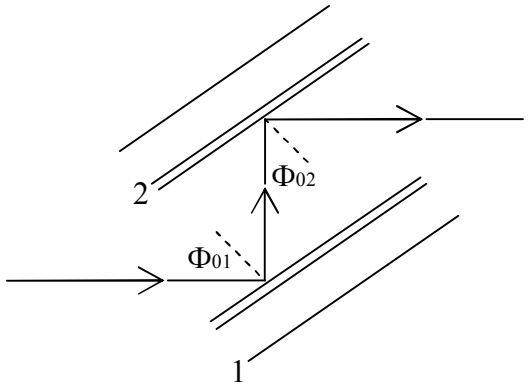

Figure 2 TES architecture, where the input and output beams are parallel. $\rho = \rho_1\rho_2$.

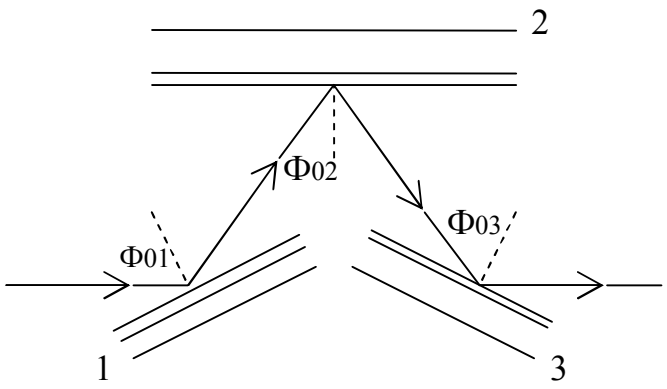

Figure 3 TES architecture, where the input and output beams are collinear. ρ = ρ1 ρ2 ρ3.

The TES architecture design is shown in Figure 2, where the input and output beams are parallel. The PTF for this architecture is $\rho = \rho_1 \rho_2$. If the input and output beams are required to be collinear, a third reflection is to be added for that purpose, Figure 3. In that case, the third element (thin-film system) could be designed to preserve the polarization properties of the beam emerging from the second element (thin-film system) or could be co-designed and co-controlled as needed with the second element (film-substrate system) to perform together the function of the second element (thin-film system) of Figure 2, where $\varphi_2 = 2\,\varphi_1 - \pi/2$ and $\rho = \rho_1 \rho_2 \rho_3$.

2.4.1.1 General retarder(R) gates

As we discussed above, we have two major special types of the TES gate architecture; the constant- Δ and the constant- ψ designs, see Figures 4 and 5. We start with the simplest, the constant- ψ design, which is the retarder (R) gate.

2.4.1.1.1 XOR retarder (R)-gate

The design of any general logic gate starts with the choice of the state of polarization representing the incoming Laser. For the R-gate type, it is represented in the complex ρ-plane by point A on the unit circle, $\Delta = \alpha$, Figure 4.

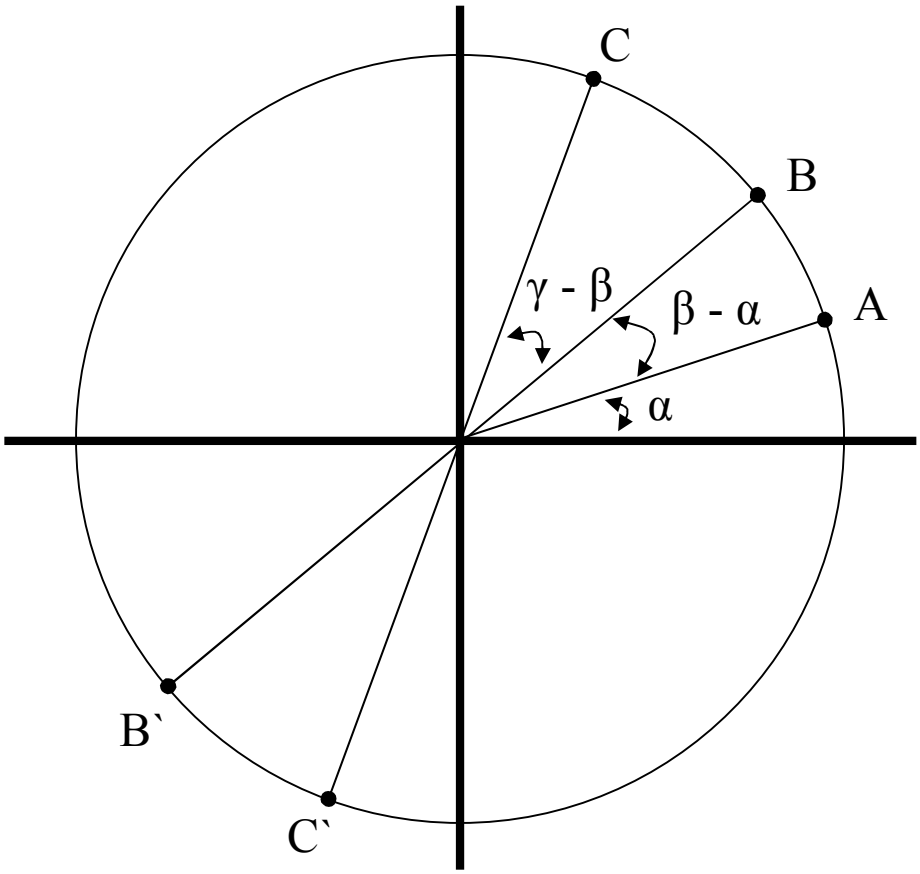

Figure 4 The complex ρ plane representation of the TES R-gate.

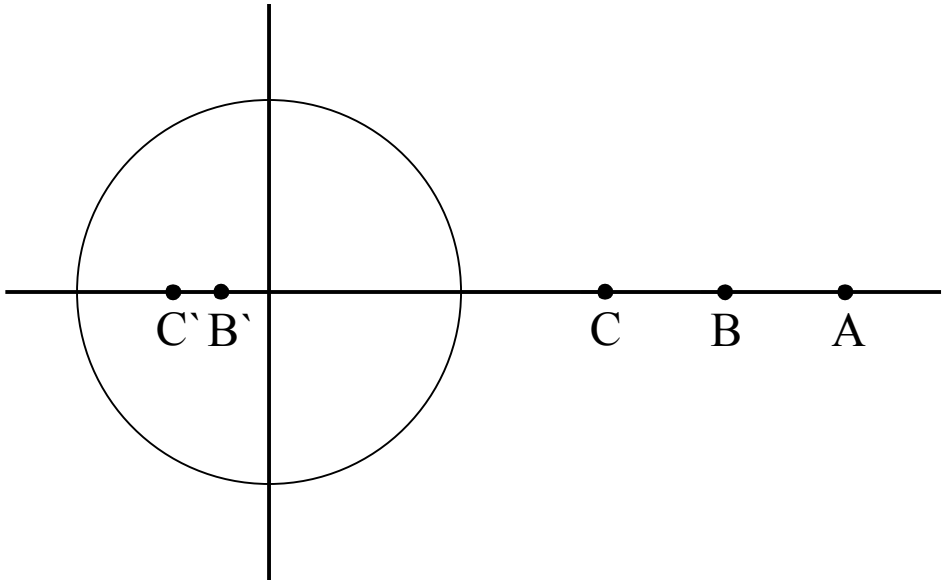

Figure 5 The complex ρ plane representation of the TES LPP-gate.

The second step is to determine the two polarization states representing the laser after each of the two film-thickness systems TFS_1 and TFS_2 of Figure 2, point B for $L1_1$, $\Delta = \beta$, and point C for $L1_2$, $\Delta = \gamma$, respectively. Accordingly, $L0_1 \equiv \beta + 180°$ and $L0_2 \equiv \gamma + 180°$ (the value of Δ); orthogonal to the β and γ polarization states, respectively. Those two polarization states are represented by points Ḃ and Ċ, respectively.

The third step is to determine the two polarization states representing each of the two reflections at TFS_1 and TFS_2 themselves. That is achieved through a quick study of the operation of the gate. For the operation of the gate, the laser's state of polarization A is first to be transformed into the state of polarization B or Ḃ representing $L1_1$ or $L0_1$, respectively, by interacting with TFS_1 in either of its two

controlled states 1 or 0, respectively. The state of polarization of the emerging beam from TFS_1 is changed upon interaction with TFS_2 in either of its two controlled states of 1 or 0. That interaction leads to a transformed polarization state of either C or Ć, depending on the controlled states of TFS_2, Table 1.

Table 1 Gate-design table, which includes the truth table and the constructed operation table of the R-gate type of the TES architecture of Figure 4; XOR gate.

A	TFS_1	B	TFS_2	C			
α	β–α+180°	β-180°	γ–β	γ+180°	0	0	0
α	β–α+180°	β+180°	γ–β+180°	γ	0	1	1
α	β–α	β	γ–β	γ	1	0	1
α	β–α	β	γ–β+180°	γ+180°	1	1	0

Table 2 Gate design parameters (transformations) derived from Table 1, for the two film-substrate systems TFS_1 and TFS_2, for the two control states 1 and 0 of each; for an XOR R-gate of the two-electronic-signal (TES) architecture.

	L1	L0
TFS_1	β – α	(β – α) + 180°
TFS_2	(γ – β) + 180°	γ – β

Table 1 gives the truth table of the R-gate type of Figure 4, which is clearly that of an XOR gate. Note that in generating Table 1, we use the starting point as point A and use the phase information we just discussed to determine the resultant transformations. Note also that vector multiplication is reduced to phase addition; magnitudes of both vectors are unity. Table 2 shows the obtained respective design parameters (transformations) of TFS_1 and TFS_2. Note that the transformations are obtained by use of a retarder of any type, see Section 2.2.1 above.

The following is an easy to follow step-by-step algorithm to do the design;

Algorithm:

1. Fill in columns A, B, and C with the info from Figure 4, corresponding to 0's and 1's of the truth table of the gate.
2. Fill in column TFS_1 by finding the difference B – A.
3. Fill in column TFS_2 by finding the difference C – B.

4. Identify the 0's and 1's corresponding to TFS_1 and TFS_2; transformations.

5. Construct the gate-design table.

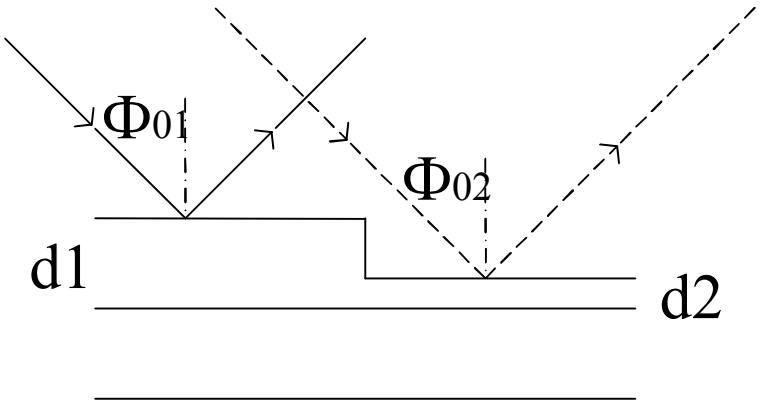

Figure 6 One possible realization of Table 2 using a film-substrate system.

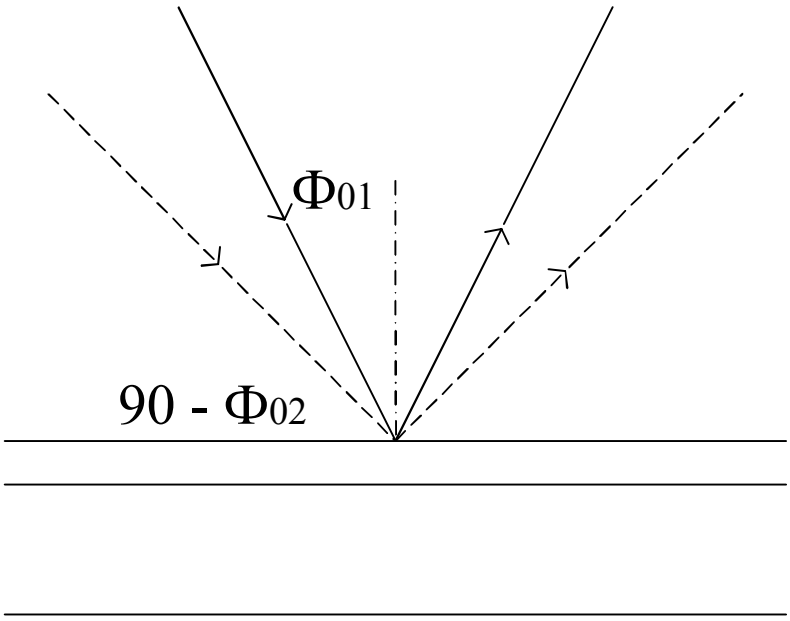

Figure 7 A second possible realization of Table 2 using a film-substrate system.

Figure 6 shows a possible realization of the PTFs of TFS_1 or TFS_2 of Table2. The two angles of incidence φ_{01} and φ_{02} might be equal or not. If they are equal, the two film thicknesses d_1 and d_2 provide two different PTFs of ρ_1 and ρ_2, corresponding to L1 and L0. If not, then we have an extra degree of freedom. Figure 7 shows a second possible realization, where the two angles of incidence are not equal, and each provides a PTF for L1 and L0. Those are only two possible configurations with others are under consideration. Also, remember that a liquid crystal, or any other electro-optic device, can be used for the same purpose.

2.4.1.1.2 XNOR retarder (R)-gate

To design a general XNOR R-gate, we can do either of three things. First, we can simply invert one of the inputs of the XOR R-gate discussed above by an inverter. Second, we can invert the output of the XOR gate by an inverter. For those two cases, an inverter is simply a TFS that produces a relative phase shift of 180° without producing any relative amplitude attenuation, simply a retarder. The above two cases amount to having the retarder at the input, output, in the middle, or even switching the corresponding 1 and 0 of one of the two electronic control inputs with respect to the associated TFS retardation of Table 2.

Third, we use the algorithm of the previous subsection to design the gate. Tables 3 and 4 are the gate-design table and the gate parameters table, respectively.

Table 3 Same as in Table 1, but for an XNOR TES-architecture R-gate.

A	TFS_1	B	TFS_2	C			
α	β–α+180°	B+180°	γ–β+180°	γ	0	0	1
α	β–α+180°	β+180°	γ–β	γ+180°	0	1	0
α	β–α	β	γ–β+180°	γ+180°	1	0	0
α	β–α	β	γ–β	γ	1	1	1

Table 4 Same as in Table 2, but for an XNOR TES-architecture R-gate.

	L1	L0
TFS_1	$\beta - \alpha$	$(\beta - \alpha) + 180°$
TFS_2	$\gamma - \beta$	$(\gamma - \beta) + 180°$

2.4.1.1.3 Cascading: the subsequent (S) gate

To cascade any number of the R-gates together, L1 and L0 are to be the same at the input and output of the gates. The general gate designed above does not satisfy this condition. Therefore, we have a different design for the subsequent (S) gates; the cascading design. For that S-gate, the input laser beam is the output of the first gate, or any other S-gate. That is a polarization state of either C or Ć. Therefore, TFS_1 of the S-gate should produce an uncontrolled retardation of $-(\gamma - \beta)$ to bring the input polarization state of the beam to either B or B′, Figures 2 and 4. TFS_2 of the S-gate should produce the controlled retardation of $\gamma - \beta$, as before. Now the logic inputs to the S-gate are the laser beam and the controlled electronic input through TFS_2. That is the case of one optical logic input and one electronic logic input. On the other hand, if the two inputs to the S-gate are both optical, we can use any of three methods for cascading: 1) convert one of the two input beams to an electronic signal through a photodetector and use the electronic signal as the input through TFS_2 as explained above, with a price paid in speed, 2) use the electro-elimination design methodology of Chapter 3 to keep the high speed of the gate unchanged [29], or 3) use an optical switch which also does not slow down the operation. This S-gate design can be indefinitely

cascaded. Operation and truth tables similar to Tables 1 – 4 are easily generated for the S-gates. They are not presented here.

2.4.1.2 General linear-partial polarizer (LPP)-gate

Again, as we discussed above, we have two major special types of the TES gate architecture; the constant- Δ and the constant- ψ designs. In the previous section, we discussed the simplest of the constant- ψ designs, which is the R-gate. Now, we discuss the simplest of the constant- Δ designs, which is the linear-partial polarizer (LPP) gate.

2.4.1.2.1 XOR LPP-gate

As we discussed above, the design of any general logic gate starts with the choice of the state of polarization representing the incoming Laser. For the LPP-gate, it is represented in the complex ρ-plane by a general point A on the real axis, $\tan \psi = \alpha$, where α now is the distance 0A from the origin, Figure 5. The second step is to select the two polarization states represented by the general points B for $L1_1 \equiv \beta$ and C for $L1_2 \equiv \gamma$. Similarly, β (γ) is the distance 0B (0C).Accordingly $L0_1 \equiv 0\acute{B}$ and $L0_2 \equiv 0\acute{C}$; orthogonal to the β and γ polarizations, respectively. Those two polarization states are represented by points $\acute{B}$ and $\acute{C}$, where $0\acute{B} = 1/0B$ and $0\acute{C} = 1/0C$, respectively.

Table 5 Same as in Table 1, but for a TES-architecture LPP-gate type; XOR.

A	TFS_1	B	TFS_2	C			
α	$1/\beta\alpha \llcorner 180°$	$1/\beta \llcorner 180°$	β/γ	$1/\gamma \llcorner 180°$	0	0	0
α	$1/\beta\alpha \llcorner 180°$	$1/\beta \llcorner 180°$	$\gamma\beta \llcorner 180°$	γ	0	1	1
α	β/α	β	γ/β	γ	1	0	1
α	β/α	β	$1/\gamma\beta \llcorner 180°$	$1/\gamma \llcorner 180°$	1	1	0

Table 6 Same as in Table 2, but for a TES-architecture LPP-gate type, XOR.

	L1	L0
TFS_1	β/α	$1/\alpha\beta\angle 180°$
TFS_2	$\gamma\beta\angle 180°$ and $1/\gamma\ \beta\angle 180°$	β/γ and γ/β

The same discussion of Section 2.4.1.1 holds for our three new points A, B, and C. Using the algorithm of the same subsection, and using division instead of subtraction, we derive Tables 5 and 6. Table 6 gives the design parameters for TFS_1 and TFS_2 for the two controlled states of each. Note that the transformations of Table 5 transform a linearly polarized light to a linearly polarized light with a different value of P. That is achieved by a linear partial polarizer TFS or electro-optically using a liquid crystal, for example, see Section 2.2.2.3 above.

By closely inspecting Tables 5 and 6, we recognize the fact that the TFS_1 design is physically correct; same required 0's and same required 1's. But for TFS_2, the design is not physically correct, because it requires two different 0's and two different 1's. To have only one state of 0 (1), we equate the two; $\beta/\gamma = \gamma/\beta$ ($\gamma\beta\angle 180° = 1/\gamma\beta\angle 180°$). Both lead to $\gamma = \beta = \pm 1$. Therefore, regardless of the position of point A, we have B = C = (+1, 0) and $B' = C' = (-1, 0)$, or vice versa. A second limiting case is of the two points of 0 and ∞, which is discussed in Section 2.4.3.3.2, and the following subsections.

2.4.1.2.2 XNOR LPP-gate

As before, to design a general XNOR LPP-gate, we can do either of three things. First, we can simply invert one of the inputs of the XOR LPP-gate discussed above by an inverter. Second, we can invert the output of the XOR LPP-gate by an inverter. For those two cases, an inverter is simply a TFS that produces a relative amplitude attenuation of $\gamma + (1/\gamma)$ without producing any phase shift, simply an LPP, which is

actually equivalent to 180° phase shift for the limiting case discussed in the previous subsection; (+1, 0) and (-1, 0). The above two cases amount to having the LPP at the input or output, in the middle, or even switching the corresponding 1 and 0 of one of the two electronic control inputs with respect to the associated TFS retardation of Table 6.

Tables similar to Tables 5 and 6 can be similarly generated using the same algorithm of Section 2.4.1.1.1.

2.4.1.2.3 Cascading

For the sake of conciseness, we do not repeat the discussion related to the cascading of the R gates. A similar discussion holds for an LPP gate, with proper referencing to points A, B, and C of Figure 5.

2.4.1.2.4 Magnitude information

The analysis and discussion of the previous subsections limited the LPP gate design to completely identical 0's and 1's, which led to the limiting case of B = C. We can do the design with a relaxed condition on the 0's and 1's, where we define the 0's as being of a phase of $\angle$ 180° with no restrictions on the magnitude, and the 1's as being of a phase of $\angle$ 0° also with no restrictions on the magnitude. That allows for more degrees of freedom in the design process, and affords the opportunity to use the magnitude to carry independent information that can be utilized for testing, logic, or reversible logic designs.

2.4.2 Single-electronic-signal (SES) gate architecture

From the above discussions, it becomes evident that combining points A and B, Figures 4 and 5, to represent the logic states of the laser beam provides an elegant

design architecture. In this case, the laser beam carries the information within the optical system as an input and output for the gate, in addition to being one of the controls of the gate. The second control is an electronic one, hence the single-electronic-signal (SES) gate architecture.

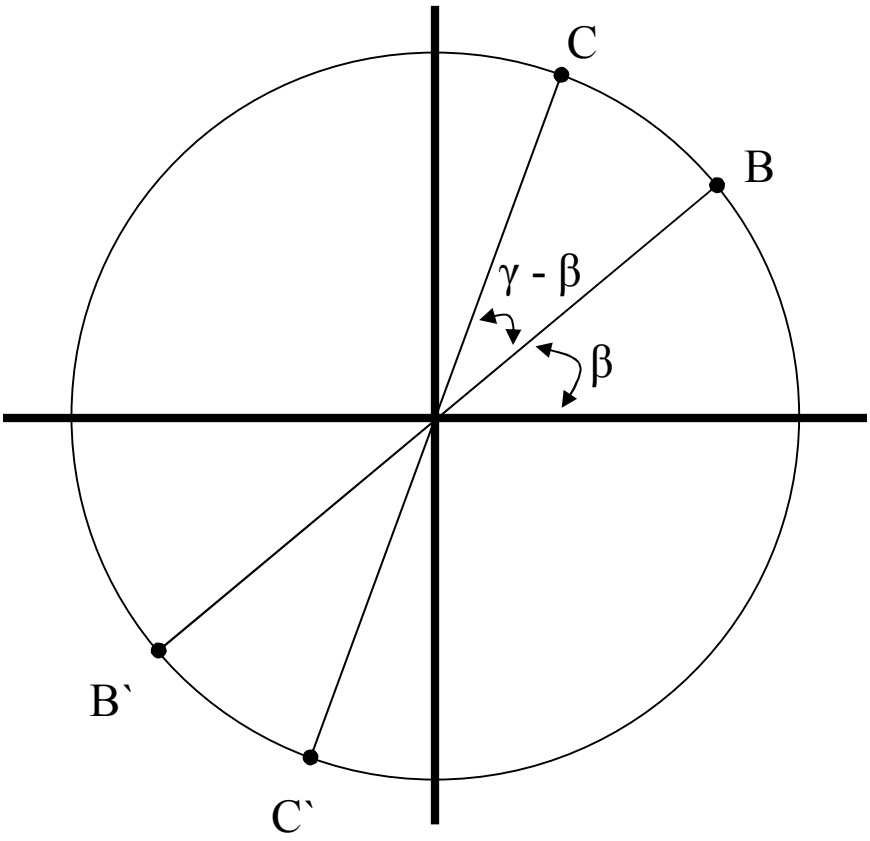

Figure 8 Complex ρ plane representation of the SES-gate architecture.

Now, in Figure 8 the input laser beam logic states 1 and 0 are represented by the polarization states B and Ḃ, and that leaving the single TFS is represented by the polarization states of C and Ć. It is easy to obtain the truth table for the SES gate architecture using the same algorithm used before and recognize that it is that of an

XOR gate. XNOR gates are obtained in a similar fashion as before, simply by an inversion or a redesign.

Cascading of the gates is evident in this architecture. The output polarization states are either C or Ć, where the input is always B or Ḃ. Accordingly, a second uncontrolled TFS is introduced at the output of the gate, or at the input, to return the polarization states to B or Ḃ, as we discussed above, Section 2.4.1.1.3.

2.4.3 Single-reflection single-electronic-signal (SRSES) gate architecture

The single-reflection single-electronic-signal (SRSES) gate architecture is achieved by making points B and C, and hence Ḃ and Ć, coincide together. That way, the input and output beams have the same L1 and L0 polarization state representation of C and Ć, respectively. In this case, cascading the gates does not require any additional manipulation of the beam since we only have two polarization states of C and C′, and we only have one kind of gate for each type; the S-gate design is not needed. That holds for both gate types, R and LPP.

2.4.3.1 R gate

For the R gate, Tables 7 and 8 give the gate-design and operation , and the retardation of the TFS, refer to Figure 9. It is clear from Table 7 that the gate is an XOR one. Two possible realizations for the TFS are those of Figures 6 and 7.

As we discussed before, XNOR gates of this design can easily be achieved.

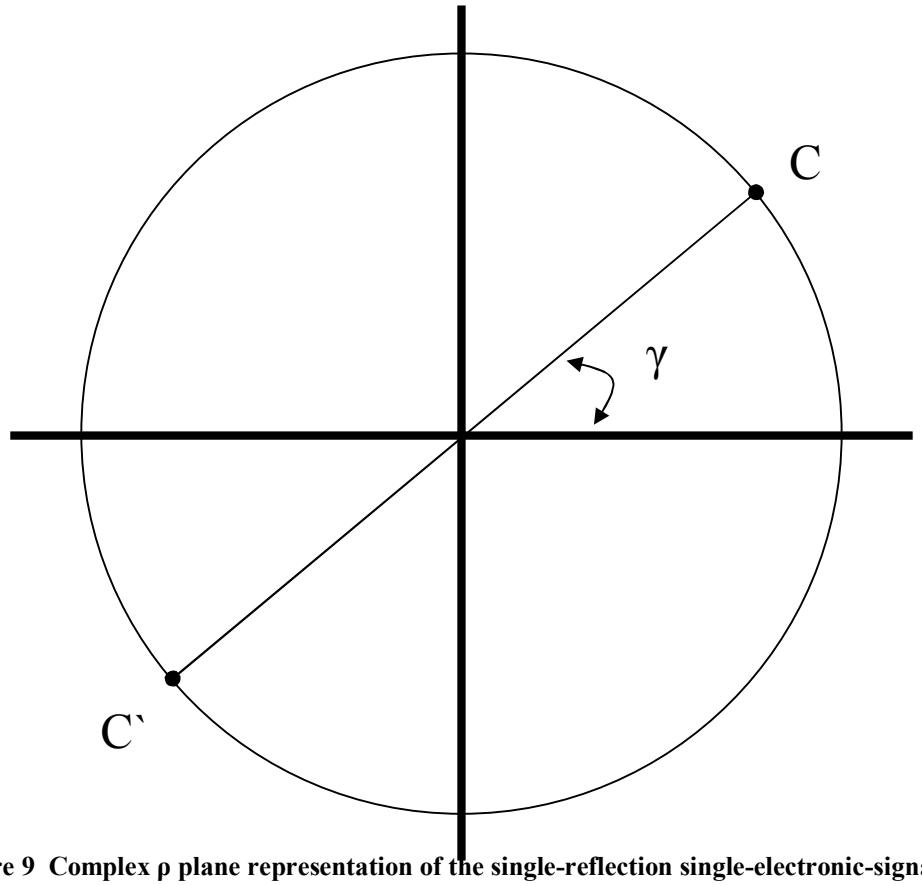

Figure 9 Complex ρ plane representation of the single-reflection single-electronic-signal (SRSES) R-gate architecture.

Table 7 Same as in Table 1, but for the single-reflection single-electronic-signal SRSES architecture R-gate, XOR gate, where LBI (LBO) is the laser beam input (output) polarization state; Figure 9.

LBI	TFS	LBO			
γ+180°	0	γ+180°	0	0	0
γ+180°	180°	γ	0	1	1
γ	0	γ	1	0	1
γ	180°	γ+180°	1	1	0

Table 8 Same as in Table 2, but for single-reflection single-electronic-signal (SRSES) architecture R-gate; XOR gate.

	L1	L0
TFS	180°	0

2.4.3.2 LPP gate

For the SRSES-architecture LPP-gate, Figure 10 gives the gate polarization-state representation. Tables 9 and 10 give the gate-design and operation, and retardation of the TFS. Note from Tables 9 and 10 that the TFS logic 1 is either of magnitude γ_2 and relative phase angle 180° or of magnitude $1/\gamma_2$ and of the same relative phase angle. On the other hand, for a TFS to produce this logic one operation it requires a condition of $\gamma = 1$, for the operation to hold correct; SRSES architecture. That means, C and Ć are both on the unit circle; points (+1, 0) and (-1, 0), respectively. That special case is to be discussed in the following subsection. It is clear from Table 9 that the gate is an XOR one.

As we discussed before, XNOR gates of this architecture can easily be achieved.

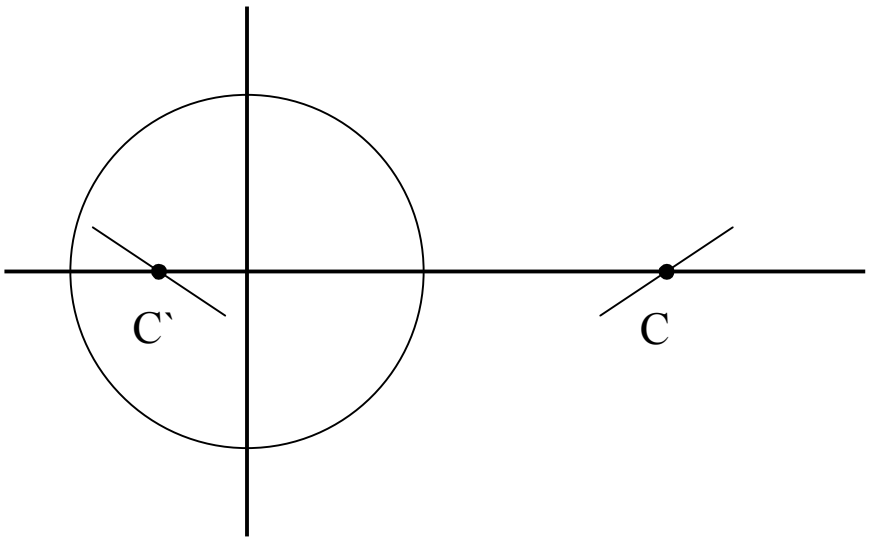

Figure 10 Complex ρ plane representation of the single-reflection single-electronic-signal (SRSES) LPP-gate architecture.

Table 9 Same as in Table 1, but for the SRSES architecture LPP-gate, XOR gate, where LBI (LBO) is the laser beam input (output) polarization state; Figure 10.

LBI	TFS	LBO			
$1/\gamma \angle 180°$	1	$1/\gamma \angle 180°$	0	0	0
$1/\gamma \angle 180°$	$\gamma^2 \angle 180°$	γ	0	1	1
γ	1	γ	1	0	1
γ	$1/\gamma \angle 180°$	$1/\gamma \angle 180°$	1	1	0

Table 10 Same as in Table 2, but for the SRSES-architecture LPP-gate, XOR gate; Figure 10.

	L1	L0
TFS	$\gamma^2 \angle 180°$ and $1/\gamma^2 \angle 180°$	0

A second case for the γ condition to be satisfied, is the limiting case where $\gamma = 0$ or ∞. That leads to the special case of p-polarized and s-polarized waves as our L1 and L0, which is the only case reported and discussed in the literature [1-14]. This case is also discussed in the following subsections.

2.4.3.3 Limiting and special cases

In the following subsections, we discuss several limiting and special cases, some of which are mentioned in the previous subsections.

2.4.3.3.1 Linearly-polarized light at ±45° (LPL45)

The special case of C and Ć coinciding with the points (+1, 0) and (-1, 0), respectively, is an intersection case between the R and LPP designs, Figure 11. Point (+1, 0) represents a state of polarization of a linearly polarized light at +45°. At the same time, it represents a TFS that produces a relative amplitude attenuation of one and a zero relative phase shift, a PPD device. It is both a retarder and an LPP. On the other hand, point (-1, 0) represents a state of polarization of a linearly polarized light at -45°.

It also represents a TFS that produces a relative amplitude attenuation of one and a relative phase shift of ± 180°. Also, it is both a retarder and an LPP.

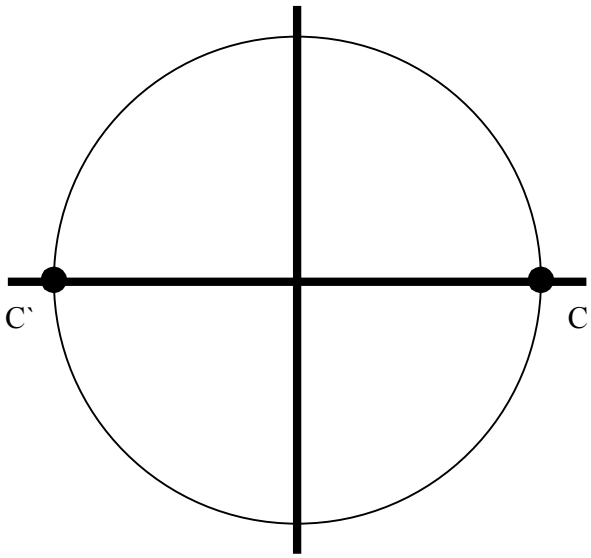

Figure 11 Special case of C and Ć coinciding with the points (+1, 0) and (-1, 0), respectively, in the complex ρ plane, is an intersection case between the R and LPP designs architectures.

Table 11 Same as in Table 1, but for the SRSES-architecture LPP45-gate, XOR gate, where LBI (LBO) is the laser beam input (output) polarization state; Figure 11.

LBI	TFS	LBO			
180°	0	180°	0	0	0
180°	180°	0	0	1	1
0°	0°	0°	1	0	1
0°	180°	180°	1	1	0

Table 12 Same as in Table 2, but for the SRSES-architecture linearly-polarized light at ±45° (LPP45), XOR gate; Figure 11.

	L1	L0
TFS	180°	0°

Tables 11 and 12 give the gate-design and operation, and the TFS functions of the gate. As can be clearly seen from Table 11, the truth table of the gate in this case is that of an XOR. As before, two possible realizations are given in Figures 6 and 7. Also, XNOR is easily obtained as discussed before.

Cascading of such gates is evident with no additional requirements; see the discussion of Section 2.4.1.1.3.

2.4.3.3.2 Linearly-polarized light at 0 and 90°

The linearly-polarized light at 0 and 90° is the limiting case of the LPP gate. The two polarization states are represented by the origin and the point at infinity, respectively. It is directly derived that L1 is the s-polarized light (90° polarization state) and that L0 is the p-polarized light (0 polarization state), or vice versa. L1 of the controlled signal is a rotation of 90° and that of the L0 state is a rotation of 0°, no action or a PPD. That gives an XOR gate. An XNOR gate is simply devised as discussed before.

Also, cascading of such gates is evident with no additional requirements as discussed above.

As mentioned before, that is the only case of polarization-based logic representation previously reported in the literature, with two controlling devices corresponding to the two-electronic-signal design but with no cascading possible without regenerating the output beam, and with zero intensity (no output beam or darkness) representing L0 and a measured intensity representing L1 at the output: on/off output logic representation. That seriously slows down the operation of the gates and greatly adds to the cost [1-14].

2.4.4 ρ-gates

We discussed the general cases of having a different polarization state for the laser beam, for TFS_1, and for TFS_2. That led to several special cases including the simplest and best, for our current purpose, of SRSES design architecture with its two varieties, constant-Δ and constant-ψ designs, and their special and limiting cases. For completeness, we discuss the design with a general polarization state ρ, represented by point C in Figure 12. Clearly, similar discussions to all other cases are in order.

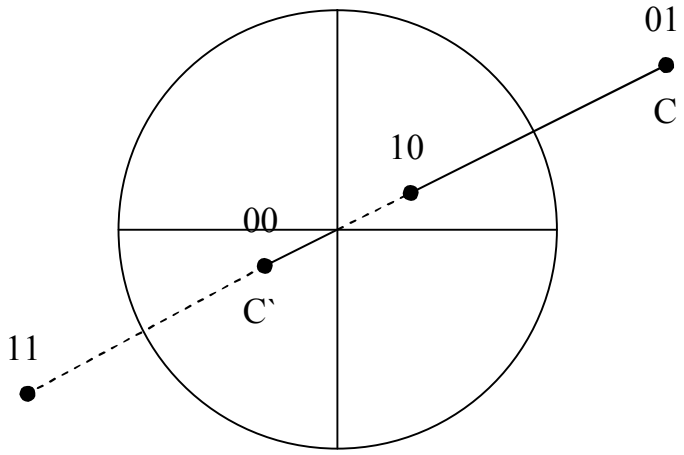

Figure 12 Complex ρ plane representation of ρ-gate architecture.

Table 13 Same as in Table 1, but for the SRSES architecture ρ-gate; XOR gate; Figure 12.

LBI	TFS	LBO			
Ć	1∟0	Ć	0	0	0
Ć	Γ/ Γ́∟ 180°	C	0	1	1
C	1∟0	C	1	0	1
C	Γ́/ Γ∟180°	Ć	1	1	0

Table 14 Same as in Table 2, but for the SRSES-architecture ρ-gate, XOR gate; Figure 12.

	L1	L0
TFS	$\Gamma/\acute{\Gamma} \llcorner 180°$ and $\acute{\Gamma}/\Gamma \llcorner 180°$	$1 \llcorner 0$

Tables 13 and 14 give the gate-design and operation, and the design transformations tables of the ρ-gate. As before, we see that the condition for proper operation and simplest cascading requirements is that $\Gamma = 1/\Gamma$. That condition is only satisfied for the retarder design; R-gate, and for the limiting case of $\Gamma = 0$, which is the parallel and perpendicular polarization case.

2.4.5 Inverter architecture

The architecture of an inverter gate is very simple. In the general case, it is a single TFS that produces 180° relative phase shift and a relative amplitude attenuation of the reciprocal of the state of polarization tan ψ. In the R-gate and LPL45 architectures, the inverter TFS is to induce only a 180° relative phase shift and no relative amplitude attenuation.

2.4.6 Simultaneous cascading, multiple input, and integrated optical architecture

It is important to realize that cascading any of the above discussed optical gate architectures is not sequential in time. It is simultaneous cascading. Therefore, all electronic signals are to be input simultaneously and the laser output-input delay is determined only by the speed of light. With today's manufacturing capabilities, and the nanotechnology moving into a more mature stage, delays in the order of femto seconds are achievable. That leads to bandwidths of several orders of magnitude of what is possible today.

Also, it is important to note that multiple input architectures are straight forward from the discussed two-input designs.

In addition, integrated optical architecture (IOA) is where any number of Boolean statements of XOR, XNOR, and Inverter operations is involved. IOA can be directly implemented using an integrated architecture employing photonic integrated circuits (PICs). For example an IOA can be designed to do switching, demultiplexing, or parity checking, to mention a few applications.

The gates can be cascaded independently or internally. Gates that has more than 2 inputs can be designed by adding one extra retarder for each extra input. A gate that satisfies the Boolean function A XOR B XOR C can be represented by 2 retarders and one polarizer. The polarizer will produce linearly polarized light at +45º and -45^{o} representing the input 0 and 1 respectively, while ρ_1 and ρ_2 logic 1 will be at angle 0 and logic zero will be at an angle of 180^{o} in the ρ plane. On the other hand, the Boolean expression A XOR B XNOR C will be very similar to the latter, but it requires an inverter to be added after the output of the first retarder, and ρ_2 logic 0 and 1 must be interchanged. As illustrated, multiple input Boolean expressions that rely on XOR, XNOR, Inverters or any combination of the latter can be easily cascaded by adding an extra layer or layers of thin films. The discussion of Section 2.4.1.1.3 on cascading holds here, obviously without the need for the uncontrolled TFS.

At the end of the whole cascaded system, or at the end of each gate, the output can be easily identified and turned into an electric signal, as and if required. For the simple case that is deigned to produce linearly polarized output at +45 and -45 degrees, a slightly off-axis polarizer or a thin-film-based system can be design to maximize the transmission or reflection of one case while minimizing the other. That, in conjunction with the use of a simple photodetector allows the photodetector to produce an electric

output of high reading representing logic 1, and low reading representing logic 0. Also, it allows for the integration of the new optical binary logic implementation with the current semiconductor based binary logic systems. Such integration at the input and the output provides great versatility for the new optical device, and allows the creation of hybrid technology that utilizes the advantages of the new system, without greatly altering current designs. Furthermore, communication between optical-based devices and semiconductor-based devices will not face any complications.

CHAPTER III

ORTHOPARALLEL REPRESENTATION

3.1 Binary-Logic Representation

In the previous chapter, a new optical-polarization-based representation and implementation of binary logic was introduced [15]. The representation system is based on the fact that logic one and logic zero both must exist and be quantitative. The proposed system, in one of its simplest implementations, employed the polarization of a beam at a general chosen relative polarization angle to be logic one while the logic zero is represented by another chosen fixed phase change relative to that of logic one. This representation allows the creation of optical gates that are much faster and more superior to their semiconductor counterparts. Only unforced gates which included inverters, XOR, and XNOR gates are possible to design and implement using that methodology.

In this chapter, we present a novel method to parallel-process optical beams to implement any gate and any Boolean function. The new system is based on splitting, or directing, the beam into either of two channels each of which only allows (maximizes the passage of) the beam with certain pre-specified polarization and blocks (minimizes the passage of) the beam with the other polarization. That allows for different processes to be independently applied to logic 1 and to logic zero beams with a single control

module for each. The two different beams are then steered to the output point, and the system is designed such that only one is active at a time.

Throughout, the information is polarization-encoded into the beam, where the intensity of the beam itself carries no information. Therefore, the strength or weakness of the beam plays no role in the operation of the devices.

The new parallel processing method retains all of the advantages of the previously introduced polarization optical system [15]. Unlike semiconductors, the optical devices produce virtually no heat, and are bound only by the speed of light and speed of the optical control elements that are only applied once: a single time lag. The system is fully integrable with the previously introduced optical gates along with the current widely used electronically based gates (semiconductor gates). The latter allows for the creation of hybrid systems or add-ons to systems currently in use. The optical output of the novel gates can be cascaded infinitely to implement complex Boolean functions using stand-alone gates. It can also be implemented into a single chip that contains various layers of optical elements. In such a case, the system operation is not only fast but all the components used in the representation are very cheap and are not complex to manufacture. Accordingly, advanced optical microprocessors can be easily and cheaply implemented.

In this chapter, we discuss the design and operation of all types of binary gates, including AND, NAND, OR, NOR, XOR, XNOR, and inverters. In addition, we discuss the concept of a general gate. That allows for all-optical processing of optical signals that applies the current cumulative knowledge of digital design. The same proposed design methodology can be used to design any future gates that are not known

today which might lead to simplified digital design for all-optical processing. An easy to follow step-by-step algorithm is presented in Chapter 4 for the proposed design methodology. We also discuss the design and operation of polarization optical processors (POPs) that implement any complex Boolean expression, and present a step-by-step design algorithm to do the design. An electro-elimination concept is introduced and applied for that purpose. It eliminates all intermediate output-input signals of microprocessor designs to have an all-optical microprocessor. That allows for smart and/or application-specific all-optical processing of input data.

We discuss in detail the design and operation of the logic gates and POPs using the special case of two orthogonal polarization states representation: orthoparallel logic (OPL) design, which leads to the Rail Road (RR) architecture.

In addition to the standard binary gates, we design and discuss multiple-input gates, and sequential and non-sequential Boolean expressions. We also discuss the design reduction, to simplify the designs, and the operation of all. To clearly explain the operation of any RR architecture POP, we use the simulation of a bullet train traveling at the speed of light over a Rail Road system preconditioned by crossovers pre-controlled by the control signals. It is important to note that the control signals are all applied simultaneously, eliminating the need for a timing diagram. Accordingly, no glitches can occur because of the non-existence of inherent propagation delay, and designs are glitch immune. Also, fan-in and fan-out problems encountered in digital system design are eliminated by the RR-architecture [30].

All three architectures are simple, direct, robust, very fast, glitch-immune, virtually consume no energy, require no heat dissipation, no masks, and no photon-

electron conversions; not carrier-frequency limited and easily operational in a spectroscopic mode.

As discussed in Chapter 2 in some detail, several publications exist that report on the efforts of other research groups on the use of polarization to represent binary logic and gates [1-14]. All used the two horizontal and vertical linear polarizations to represent the logic zero and logic one, some used spatial masks for beam manipulation, and all resulted in an on/off logic representation where the laser beam has to be regenerated for cascading purposes. In contrast, our current technology represents logic zero and logic one by any two orthogonal polarizations and manipulates the polarization of the light beam in accordance with the device performance. Therefore, the information is polarization encoded and the beam is polarization manipulated regardless of its intensity, which does not play any role in the device operation or performance.

3.2 System Components

The components used in the orthoparallel logic OPL and Rail Road RR architectures design and implementation of digital gates and POPs, to be discussed in the following sections, are beam splitters (BSs), retarders (R), and polarizers (P). A BS is used to split the beam into two identical beams. The R is used to introduce a prespecified relative retardation angle without changing the relative amplitude of the output/input two components of the electric vector of the electromagnetic wave parallel and perpendicular to the plane of incidence or transmission, and the P is used to generate a linearly polarized beam of a prespecified polarization angle of inclination

with the plane of incidence, or plane of transmission. The three components are available using the standard crystal-type [31]. They are also available using inexpensive film-substrate systems in reflection or transmission modes [16, 18, 19, 21-26, 32]. In Chapter 2, the Rs and Ps are discussed in detail along with their respective representation in both the complex ρ and τ planes. The BSs are discussed in some detail in References [33, 34].

A spatial mask, properly designed, maybe used to replace the stationary combinations such as BS/P/M/P and BS/P/M/P/R [35]. Polymer spatial masks are easily manufactured today. Also, a birefringent polarizer, linear, circular, or elliptical, can replace the BS/P/M/P combination bringing the efficiency of the device to the high upper nineties.

Hybrid devices such as magneto-optic, electro-optic, or liquid crystals can be used to effect polarization rotation, instead of using a retarder. The polarization control of the beam and not its intensity are the key in the current technology. Regardless of the beam intensity, the information continues to be present in its polarization state.

A polarization-preserving device (PPD) might be used to keep the polarization state of the beam unchanged, if and when needed for steering purposes [21]**.** Also, mirrors can be used for that purpose.

It is important to emphasize that the three devices of R, P, and BS are becoming, and will continue to become, commercially available in increasingly diverse forms and are not in any way to be limited to the discussed principles of operation now or in the future. The current industry standard processes are sufficient to produce high speed very large scale integrated chips of the proposed architectures.

3.3 Orthoparallel Optical Logic Representation

The complex ρ-plane is defined as the complex plane of the ρ vector representing the relative output/input phase difference Δ and amplitude tan ψ of the two components of the electric vector of the electromagnetic wave (laser beam) parallel and perpendicular to the plane of incidence. (The τ-plane has a similar definition for transmission.) This complex ρ-plane is used extensively to illustrate how different designs can be achieved using the new binary logic representation in conjunction with the new parallel processing methodology: orthoparallel logic OPL and Rail Road RR architectures. The XOR and XNOR are the only two gates that can be constructed by a series of components in parallel. On the other hand, a general gate is composed of similar devices but in parallel. Accordingly, two different optical-polarization operations (OPOs) can be performed on each branch after crossing out the polarization representing the other branch, a total of four OPOs [29].

For simplicity, we select the logic one L1 to be a linearly polarized light at +45° and logic zero L0 to be a linearly polarized light at -45° at both the input and output of any gate or chip. Naturally, an inverter is a simple retarder that introduces a 180° phase shift in the ρ-plane. Now, for each gate the desired output for each input must be determined. Since a two-input gate of this design includes a unique output to only one of four input possibilities of the AND, NAND, OR, and NOR gates, then one of the two branches does not require logic-controlled operations. On the other hand, a two-input gate that results in a unique output logic (L1 or L0) to two of the four input logics requires one operation in each branch: XOR and XNOR gates. In the following

subsections, a brief discussion of the representation, design, and operation of the gates AND, NAND, OR, NOR, XOR and XNOR is presented.

3.3.1 AND gate

An AND gate has the truth table shown in Table 15 [30]. The first input column is considered as the optical input (laser beam) and the second input column as the control input. As mentioned earlier, an AND gate requires only one operation at one of the two branches, since it outputs L1 at only one of four input possibilities.

Table 15 AND, NAND, OR, NOR, XOR, and XNOR gates

Input		**Output**		
A	B	AND	NAND	OR
0	0	0	1	0
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

A	B	NOR	XOR	XNOR
0	0	1	0	1
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

First, the optical input is generated outside the gate by a simple P that either produces a linearly polarized light at 45° or -45° to represent logic one (L1) and logic zero (L0), respectively, or by polarization rotation using, for example, a liquid crystal. Coming into the gate, the input is then split into two beams inside the gate using a BS

(Figure 13). One branch includes a polarizer (P) at a 45° angle and hence only passes light polarized at 45°. The other includes a P at -45° angle and hence only passes light polarized at -45°. A properly designed mask or a birefringent polarizer can be used to create the two branches. That results in a branch containing L0, logic zero branch (LZB), and a branch containing L1, logic one branch (LOB), with only one branch at a time having a light beam. In the LZB, no manipulation is necessary. In the LOB, a control retarder (R) is designed to introduce zero angle change in the complex ρ plane (zero relative phase shift) if the second input is L1 or introduce a 180° angle change if the second input is L0.

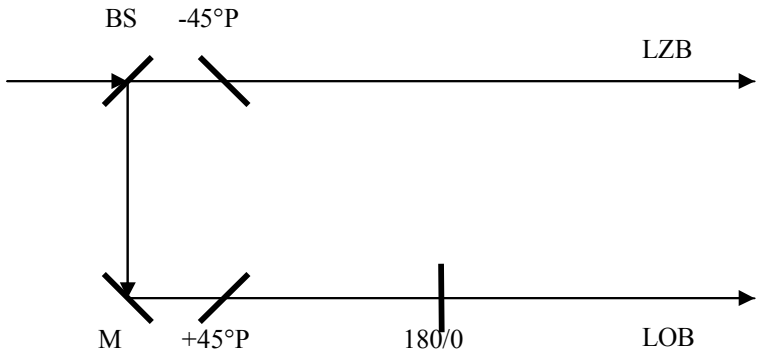

Figure 13 Orthoparallel Logic OPL architecture of an AND gate, where BS: beam splitter, P: polarizer, 180/0: retarder producing 180°/0 phase shift in the complex ρ plane, LZB: logic zero branch, and LOB: logic one branch. The BS/-45° P/M/+45° P device combination can be replaced by a single properly designed spatial mask or by an appropriate birefringent polarizer. The 180°/0 retarder can be replaced by a 90° polarization rotation electro-optic device such as a liquid crystal. Only one beam leaves the gate by simple steering.

The two beams are then steered to the same output point. Note that the output only includes one of the two beams at a time. No interference occurs. Remember that linearly polarized light and a P at 45° are represented in the complex ρ-plane by the point (+1, 0) and that linearly polarized light and a P at -45° are represented by the point (-1, 0): orthogonal polarization states and devices [15].

Therefore, the operation of the gate is very simple. When the input is L1, only the LOB has a signal and the output is L1 if the second control input is L1, and the branch device is a polarization preserving device (PPD) or nothing at all. If the second control input is L0, the output beam is polarization rotated 180° by a simple R device, and the output is L0. On the other hand, if the input is L0, only the LZB has a signal and the output is L0 in both cases of the second control input, and the branch device does not exist, or a PPD can be used.

3.3.2 NAND gate

While it is very easy to add a non-control inactive R that introduces a 180° angle in the ρ plane to the output of an AND gate to produce a NAND gate, the gate can otherwise be independently designed using knowledge of the complex ρ plane and the OPL architecture. The truth table of a NAND gate is shown in Table 15, and the OPL gate architecture is shown in Figure 14. (Note that the NAND gate contains one more optical component than the AND gate: the LZB component.) As always, the first input column is considered as the optical input (laser beam) and the second input column as the control input. Similar to the last design, we create two, branches one containing L0, LZB, and one containing L1, LOB. The LZB requires a simple inactive (unchanged) 180° R. The LOB requires a control R introducing a zero degree rotation at the second control input of L0, and a 180° rotation at the second control input of L1; both rotations are in the complex ρ plane. Note that the output contains one less operation than when adding an inverter to the output of an AND gate, while they contain the same optical components, where the 180° is within the gate instead of outside as an inverter.

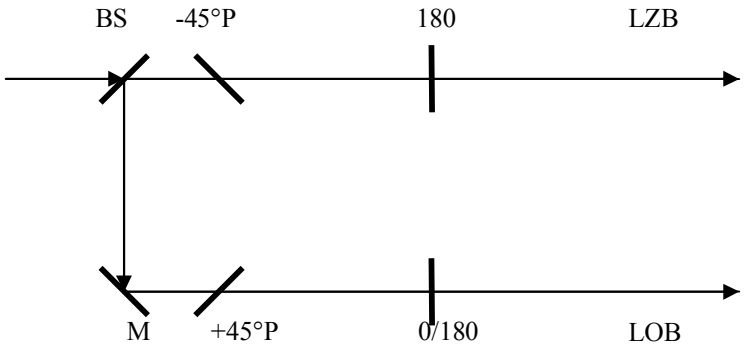

Figure 14 Same as in Figure 13, but for a NAND gate.

The operation of the gate is also straight forward. For an L0 optical input, only LZB contains an optical signal and the output beam is polarization rotated 180° for both of the control signals of L0 and L1: an inactive R. On the other hand, for an L1 optical input, only LOB contains an optical signal and the output beam is either unchanged, L1, or 180° polarization changed by the second control input, L0, see Figure 14. It is clear that the inactive R component is removed in the AND gate and that the second control input is reversed, as expected.

3.3.3 OR gate

An OR gate can be constructed using the previous gates and inverters, or using only NAND gates, or it can be designed using the knowledge of the complex ρ-plane and the OPL architecture. The truth table of an OR gate is shown in Table 15, and the OPL gate architecture is shown in Figure 15. First, as always, the first input column is considered as the optical input (laser beam) and the second input column as the control input. Similar to the previous designs, we create two branches, one containing L0 and one containing L1. The LOB requires no further control. On the other hand, the LZB needs a simple R that introduces a 180° relative phase shift at the second control input

of L1, and a zero relative phase shift at the second control input of L0. As always, the two beams are then steered, as needed, to the output point. Only one beam is active at a time.

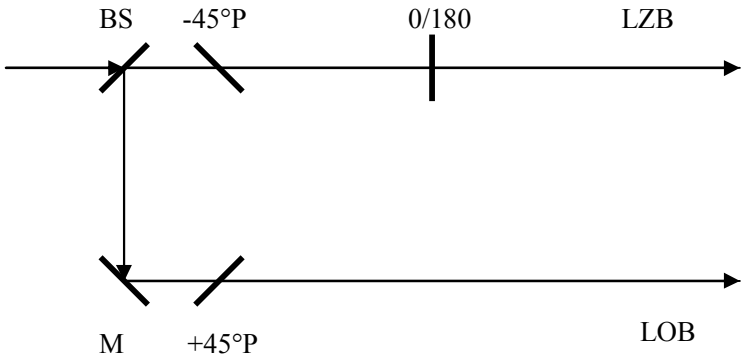

Figure 15 Same as in Figure 13, but for an OR gate.

The operation of the gate can be easily followed using Figure 15, along with Table 15. For an optical input of L1, the LOB is the only active branch and the output is L1 with no beam manipulation required: no optical component or a PPD if needed. On the other hand, for an optical input of L0, the output is either L0 if the second control input is L0 requiring a zero R (a PPD or no device), or L1 if the second control input is L1 requiring a 180° R. As always, the required optical component has two states of operation zero and 180° depending on the second control input.

In comparing the AND and OR OPL gate architectures, it is clear that they have the same optical components with one exception: the control R is moved from the LOB to the LZB with its two polarization states flipped.

3.3.4 NOR gate

A NOR gate can be constructed using the previous gate and an inverter, using only NAND gates, or it can be designed using knowledge of the ρ-plane and the OPL architecture. The truth table and OPL architecture of a NOR gate are given in Table 15 and Figure 16, respectively. First, as always, the first input column is considered as the optical input (laser beam) and the second input column as the control input. Similar to the previous designs, we create two branches one containing L0 and one containing L1. The LOB requires an inactive R that introduces a 180° phase change in the ρ plane. The LZB requires a control R introducing a 180° phase change at the second control input of L0 and zero phase change at the second control input of L1.

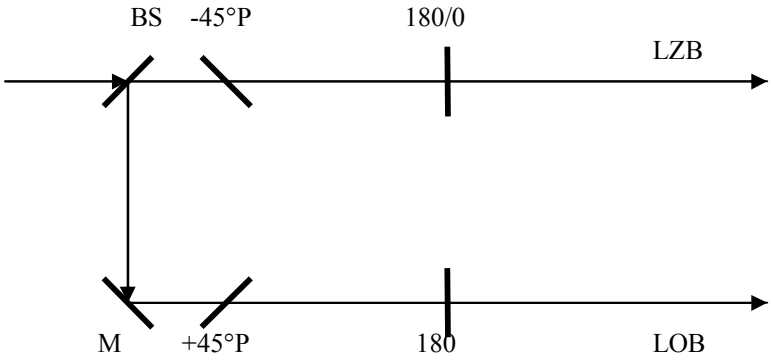

Figure 16 Same as in Figure 13, but for a NOR gate.

For this gate, and for an optical input of L1, the output is always L0 for both states of the second control achieved by the inactive 180° R. But for the L0 optical input, the output is L1 for the second control state of L0 (achieved by a 180° phase change of the control R) and is L0 for the second control state of L1 (achieved by a zero phase change of the control R.)

Note that the NOR gate contains one more optical component than the OR gate, which is the same as when an inverter is used with the OR gate. In this case, the R is inside the gate and not of a separate inverter gate, as compared to the OR gate cascaded with an inverter. Also, the output contains one less operations.

Note also that the NAND and NOR gates are having the same number of optical components, with the optical components interchanged branches, and the two states of the active R also interchanged.

3.3.5 XOR and XNOR gates

The XOR and XNOR unforced simple realizations were introduced in Chapter 2. The two gates can also be easily implemented by using the above gates, or by using only NAND or NOR gates. What differentiates between the XOR/XNOR gates and the gates above is the fact that the XOR and XNOR gates require control operations that are symmetric in the LZB and LOB. That fact allows for the creation of the XOR and XNOR logic gates without branching and parallel operations, and by only having one controlled operation on any optical input (L1 or L0). That explained, it is obvious that the XOR and XNOR gates can be implemented using a special case of OPL architecture, by simply having the same controlled retarder on both branches. While usually that is not necessary, there are cretin cases that can benefit from such representation such as the all optical non-single-dimension implementation of complicated Boolean functions that will be discussed later.

3.4 Parallel Architecture

The parallel architecture is a special case of the OPL architecture where the polarization operation on the signals of both branches is identical. In this section the parallel architecture designs of the XOR and the XNOR gates are discussed.

3.4.1 XOR gate

An XOR gate can be constructed using the AND or OR gates along with inverters, using only NAND or only NOR gates, or it can be designed using knowledge of the complex ρ plane and the OPL architecture, as all other gates. The truth table of an XOR gate and its OPL architecture are shown in Table 15 and Figure 17, respectively.

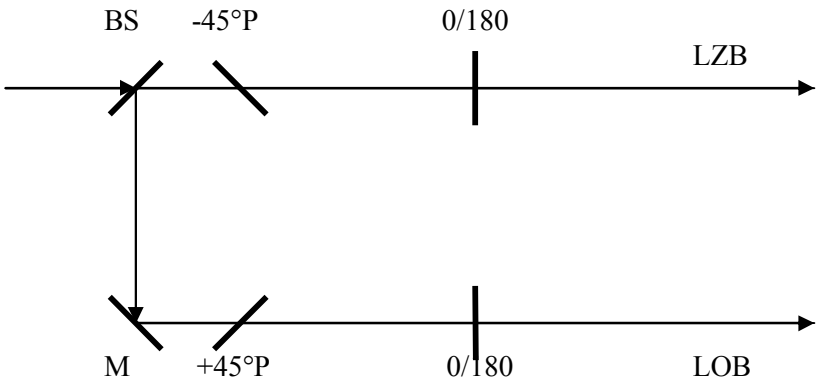

Figure 17 Same as in Figure 13, but for an XOR gate.

First, as always, the first input column is considered as the optical input (laser beam) and the second input column as the control input. Similar to the previous designs, we create two branches one containing L0 and one containing L1. From the truth table, it is clear that both branches perform the same operations using similar components. In the case where the optical input is linearly polarized at +45° or -45°,

each branch requires a simple R that introduces a 180° phase change at the second control input of L1, and zero phase change at the second control input of L0.

As can be seen from Table 15, and Figure 17, for an L0 optical input, the output is L0 for a second control input of L0 (achieved by a zero phase change R, or no optical component at all), and is L1 for a second control input of L1 (achieved by a 180° phase-change R). On the other hand, for an optical input of L1, the output is L1 for a second control input of L0 (also achieved by a zero phase change R, or no optical component at all), and is L0 for a second control input of L1 (achieved by a 180° phase-change R.) The parallelism is obvious and can be used to simplify the design to single-branch architecture, as we discuss in Section 3.5.

3.4.2 XNOR gate

As the XOR gate, the XNOR gate can be constructed using the AND or OR gates along with inverters, using only NAND or only NOR gates, or it can be designed using knowledge of the complex ρ plane and the OPL architecture, as all other gates. The truth table of an XNOR gate and its OPL architecture are shown in Table 15 and Figure 18, respectively.

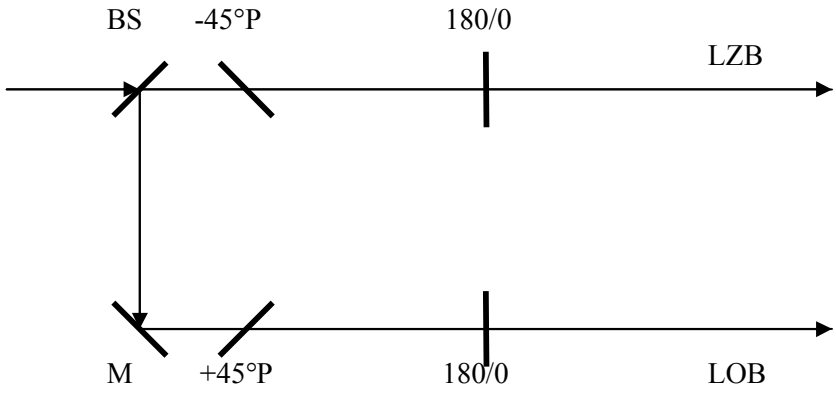

Figure 18 Same as in Figure 13, but for an XNOR gate.

First, as always, the first input column is considered as the optical input (laser beam) and the second input column as the control input. Similar to the previous designs, we create two branches one containing L0 and one containing L1. From the truth table, it is clear that both branches perform the same operations using similar components. In the case where the optical input is linearly polarized at +45° or -45°, each branch requires a simple R that introduces a 180° phase change at the second control input of L0, and zero phase change at the second control input of L1.

The operation of the gate is easily followed using Table 15 and Figure 18. For an optical input of L0, the output is L1 for the second control input of L0 (achieved by a 180° phase change R), and is L0 for the second control input of L1 (achieved by a zero phase shift R, or no component at all). On the other hand, for an L1 optical input, the output is L0 for a second control input of L0 (achieved by a 180° phase shift R), and is L1 for the second control input of L1 (achieved by a zero phase shift R, or no component at all.) The parallelism is clearly apparent.

Note that the XOR and XNOR of the OPL architecture type are having the same components in both LZB and LOB, with the same two states of the R interchanged.

3.5 Single-Branch Architecture

As we discussed above, the identical parallel branches of the OPL architecture design of the XOR and XNOR gates lead to a greatly simplified design, where no branching is required and accordingly only one component is used: single-branch architecture.

3.5.1 XOR gate

Figure 19 shows the single-branch (SB) architecture of an XOR gate. When the optical input is L0, the output is L0 for a second control input of L0 (achieved by a zero phase change R, or by no component present), and is L1 for a second control input of L1 (achieved by a 180° phase-shift R.) When the optical input is L1, the output is L1 for a second control input of L0 (achieved by a zero phase change R, or by no component present), and is L0 for a second control input of L1 (achieved by a 180° phase-shift R.)

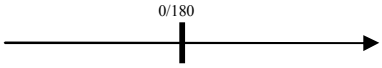

Figure 19 Single-branch architecture of an XOR gate.

3.5.2 XNOR gate

Figure 20 shows the SB architecture of an XNOR gate. When the optical input is L0, the output is L1 for a second control input of L0 (achieved by a 180° phase-shift R), and is L0 for a second control input of L1 (achieved by a zero phase change R, or by no component present.) When the optical input is L1, the output is L0 for a second control input of L0 (achieved by a 180° phase-shift R.), and is L1 for a second control input of L1 (achieved by a zero phase change R, or by no component present.)

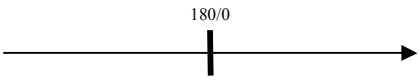

Figure 20 Single-branch architecture of an XNOR gate.

3.6 Generalized Gate

To generalize, we consider a general gate with any truth table designed using the orthoparallel architecture concept, where the laser beam carries the information into and out of the gate, and where L1 and L0 are represented by the +45° and -45° linearly polarized light: points (+1, 0) and (-1, 0) of the complex ρ plane. That special case of linearly polarized light simplifies the design and reduces the cost drastically.

As the laser beam enters the gate it is split into two beams of the same polarization properties using a BS. In the LZB, a -45° P is present to only pass -45° linearly polarized light L0. In the LOB, a +45° P is present to only pass +45° linearly polarized light L1. Alternatively, we can use a properly designed spatial mask, or a proper birefringent polarizer, to replace the three optical components and mirror, as discussed in Section 3.2.

Table 16 Collective table of the control retarder (R) for all gates, Figures 13 – 18. LZB is the logic zero branch, top branch, LOB is the logic one branch, lower branch, and L0/L1 are the two states of the control R corresponding to the logic zero L0 and logic one L1 states.

	AND	NAND	OR	NOR	XOR	XNOR
LZB (L0/L1)		180	0/180	180/0	0/180	180/0
LOB (L0/L1)	180/0	0/180		180	0/180	180/0

In each branch, an R which acts as a polarization rotator introduces two optical rotations corresponding to the two states of the second control signal. Therefore, we have 4 degrees of freedom to design any gate. One special case is zero and 180° phase-shift retarder. As discussed in Section 3.2, a liquid crystal can be used instead of the R.

Table 16 summarizes the design and operation information of the ±45° OPL special case architecture. The changes from any gate design and operation to its NOT complement is evident in the table. Also, the corresponding changes from an AND gate to a NOR gate is evident. In addition, the parallelism of the XOR and XNOR gates is clear.

The generalized gate opens the door to reconfigurable microprocessors and to programmable optical logic gates.

3.7 N-input Gates

The n-input gates are treated as a gate that represents a specific selected Boolean expression. That is treated as a simple special case of a Polarization Optical Processor (POP) in Sec. 5, and a 3-input AND gate is discussed as an example.

3.8 General Orthoparallel Optical Logic (GOPL) Realization

As discussed in detail in Reference [15], for any general state of polarization of the light beam represented by the ρ vector, $|\rho| \angle \theta°$, there exists an orthogonal polarization state represented by a vector of magnitude $1/|\rho|$ with a 180° phase shift. Therefore, those two orthogonal polarizations can be used in the OPL architecture discussed above. Figure 21 shows the architecture of a general OPL (GOPL) AND gate. As before: 1) the input laser beam carries the optical information to the gate, L1 or L0; 2) the LZB has an elliptical polarizer to eliminate the L1 beam; 3) the LOB has an elliptical polarizer to eliminate the L0 beam; 4) the LZB has no control component and

L0 beam leaves the gate as is; 5) the LOB has a controlled elliptical polarizer to introduce $1/|\rho|^2 \angle 180°$ for L0 and introduce no polarization change (PPD) for L1. All gates can be designed and their operation analyzed using the GOPL, similar to the AND gate just discussed. Also, a corresponding table can easily be derived, similar to Table 16.

An interesting special case of $\theta = 0$, where both polarizations are on the real axis of the complex ρ plane, works with only orthogonal linear polarizations. The limiting case is where one polarization is perpendicular to the plane of incidence, or transmission, and the other is parallel, represented by the origin and the point at infinity on the complex ρ plane, respectively. Also of interest is the case of linearly polarized light at ±45°, which is discussed in detail in Section 2.4.3.3.1.

Another interesting case is where the two orthogonal polarizations lie on the unit circle at any general angle of θ and θ+ 180°, with the two special cases of linearly polarized light of ±45° and of circularly polarized light of ±90°.

For most cases, if L0 and L1 of the optical carrier are required to be of any specified polarization state, an R can be used at the output.

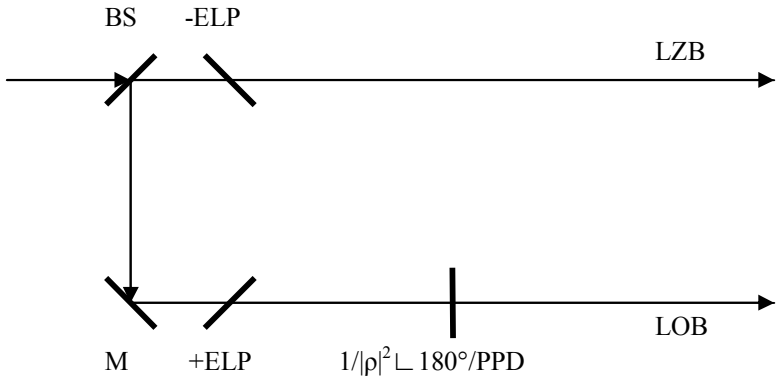

Figure 21 General OPL architecture of an AND gate.

CHAPTER IV

POLARIZATION OPTICAL PROCESSING AND GENERALIZED ALGORITHM

4.1 Introduction

In this chapter we discuss the systematic cascading and electro-elimination for electro-optical systems. We present an algorithm via which any functions truth table can be systematically designed and implemented with no electrical interconnects. Multiple step by step examples are provided to enhance the understanding of the algorithm as well as demonstrate its systematic functionality.

4.2 Polarization Optical Processor (POP), Electro-Elimination, and Rail Road Architecture

Any Boolean expression can be designed and implemented using the all-optical processing polarization logic gates discussed in the previous sections along with the well established design rules of digital logic. Also, polarization optical processors (POPs) that represent any sets of Boolean expressions or instructions as a single device can be designed and implemented. In the following subsections, we present an algorithm to do the design and then apply it to three cases. First, a three-input AND gate is discussed as a simple example. Second, a sequential Boolean expression where only one optical output of a gate is the input to another is presented. Third, a non-sequential expression where two optical gate outputs are inputs to another is presented

last. Accordingly, the concept of electro-elimination is introduced, where the Boolean expressions are designed as a single entity. This leads to the Rail Road (RR) architecture. We also discuss some principles of design reduction to reduce the number of optical elements and branches employed in any design.

4.2.1 Design algorithm

To systematically design any Boolean expression, we present a simple step-by-step algorithm that can be easily applied to any design problem. It is also easily programmed into a software design program to run on any general purpose PC.

1. Start with the truth table of the given Boolean expression and split the optical input column; first column A of the truth table.
2. Work with the top half of the truth table, the 0s.
3. Split the 0s and 1s of column B.
4. Check the output column for translation. (A translation is defined as moving every element a fixed distance in the same direction.)
5. If translation exists, then column B has no effect.
6. If translation does not exist, then invert optical-carrier polarization @ B = 1 and add a new branch. Do not add a new branch for the last input.
7. Repeat steps 3 – 6 for all other input columns in sequence.
8. Check the last optical carrier column to be identical to the output column: use an R if needed.
9. Repeat steps 3 – 8 for the bottom half of the truth table: the 1s.

4.2.2 Three-input AND gate

The three-input AND gate is a simple case to apply the design algorithm. We start with the truth table, given in Table 17. We generate a new truth table containing the state of the optical carrier, optical beam, as it travels through the POP, by adding a new column after each input column: optical-carrier column a after input column A, optical-carrier column b after input column B, and so on, Table 18. The purpose of introducing the optical-carrier column is to make it easy to identify the polarization state of the laser beam at any point within the system. Now we apply the design algorithm; always refer to Tables 22 and 23, and to Figure 22.

Table 17 Truth table of a three-input AND gate.

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 18 Extended truth table for the three-input AND gate.

A	a	B	b	C	c	Z
0	0	0	0	0	0	0
				……		...
0	0	0	0	1	0	0

0	0	1	0	0	0	0
				……		...
0	0	1	0	1	0	0
1	1	0	1	0	1	0
				……		
1	1	0	1	1	1	0

1	1	1	0	0	0	0
				……		...
1	1	1	0	1	1	1

4.2.2.1 Design

1. A. Split the input column A: horizontal continuous line of Table 18 and BS1 and two branches containing two polarizers LZB and LOB of Figure 22.

   B. Fill out optical-carrier column a, identical to input column A.

2. Focus on the top half of the truth table, the 0s.

3. Split the input column B, the horizontal dashed line of the upper half of Table 8.

4. Check the output column for translation: it exists.

5. A. Then, input column B has no effect.

   B. Accordingly, the carrier beam travels unchanged.

   C. Fill out the upper half of the optical-carrier column b; identical to optical-carrier column a.

6. Does not apply.

7. For input column C: It is divided into two quarters (Qs) by the dashed line that divided column B. Each quarter is dealt with separately.

   Q1:

   3. Split Q1; horizontal dotted line of upper half of Table 18.

   4. Check the output column for translation: it exists.

   5. A. Then, input column C has no effect.

      B. Accordingly, the carrier beam travels unchanged. (We will continue to use carrier instead of optical-carrier for simplicity.)

      C. Fill out the upper Q, Q1, of the carrier column c: identical to carrier column b.

8. Last carrier checks: carrier column c and output column are identical. Therefore, an R is not needed.

   Q2: Repeat as for Q1. The result is identical.

9. Repeat 3 - 8 for lower half of Table 18: the 1s.

Now we start at Step 3 applied to the lower half.

3. Split the input column B, the horizontal dashed line of lower half of Table 18.

4. Check the output column for translation: it does not exist.

5. Does not apply.

6. A. Then invert carrier polarization @ B = 1 and add a new branch.

   B. Accordingly, fill out the lower half of the carrier column b: inverting carrier column a states when B = 1, Table 18.

   C. Add a new branch, Figure 22.

7. Now, for input column C we have two branches, LZB and LOB. First, we work with the LZB: 0s of the carrier b Q4 (last two states of carrier column b).

3. Split the column, the horizontal dotted line separating last two states of input column C, Q4.

4. Check the output column for translation: it does not exist.

5. Does not apply.

6. A. Then invert carrier polarization @ C = 1 and add a new branch.

B. Accordingly, fill out the last two states of carrier column c: inverting carrier column b state when C = 1, Table 18.

C. A new branch is not needed because this is the last input.

8. Last carrier checks: carrier column c and output column are identical. Therefore, an R is not needed.

Second, we work with the LOB; the 1s of the carrier b Q3 (last two L1 states of carrier column b).

3. Split the column, the horizontal dotted line separating the two-before-last states of input column C, Q3.

4. Check the output column for translation: it exists.

5. A. Then, input column C has no effect.

B. Accordingly, the carrier beam travels unchanged.

C. Fill out the rest of the carrier column c: identical to carrier column b.

8. Last carrier does not check, then add an R, Figure 22.

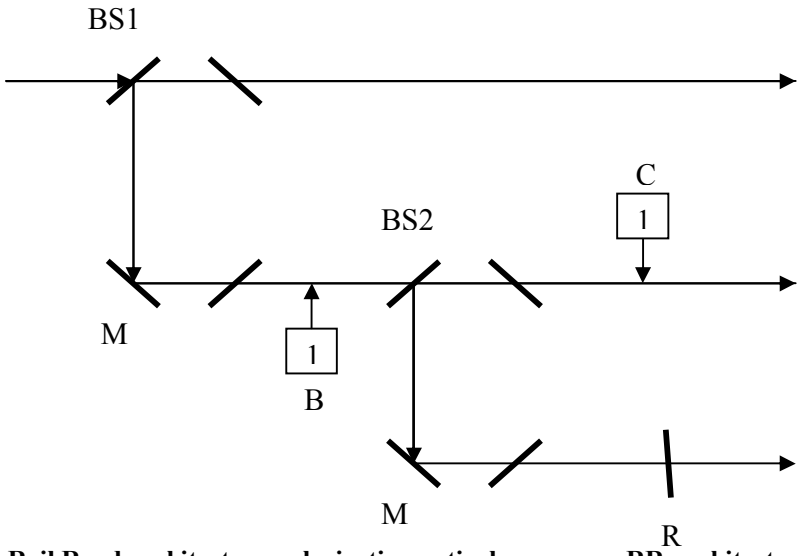

Figure 22 Rail Road architecture polarization optical processor, RR-architecture POP, design of a three-input AND gate.

4.2.2.2 Design reduction

As is clear from Figure 22, the R in the lower branch can be combined with the B carrier-polarization-inversion box inverting @ 1 (CPIB1) before BS2; actually it is a controlled R, and both replaced by a B-CPIB0, with an added C-CPIB0. That requires removing the C-CPIB1, Figure 23. That design reduction can be systematically achieved by always using a CPIB1 in the upper half of the carrier column A, the 0s, and a CPIB0 in the lower half, the 1s. Table 19 shows the lower half of the extended truth table for that case.

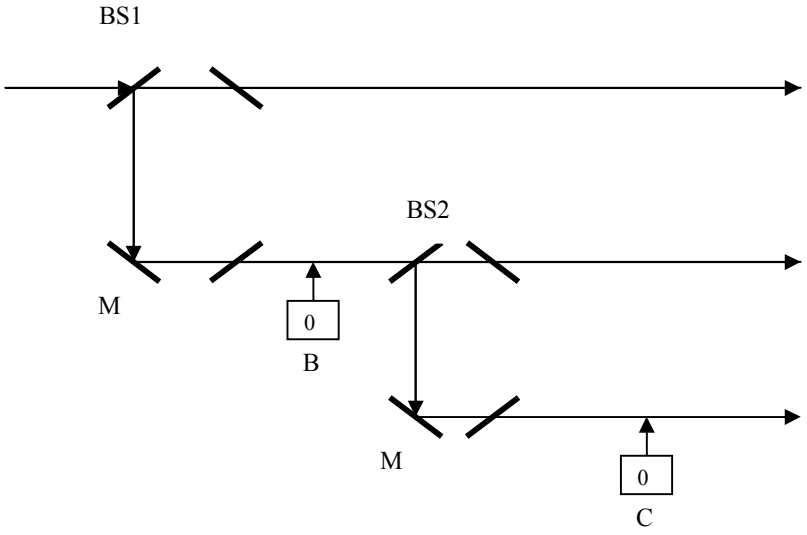

Figure 23 Reduced design of Figure 22.

Table 19 The lower half of the extended truth table of the three-input AND gate, inverting @ B = 0

A	a	B	b	C	c	Z
1	1	0	0	0	0	0
				. ……..		
1	1	0	0	1	0	0

1	1	1	1	0	0	0
				. ……		
1	1	1	1	1	1	1

4.2.2.3 Operation

The operation of the three-input AND gate design of Figure 23 is easily understood by following the laser beam as it travels through the gate. First, it is important to realize that all control-input signals are applied simultaneously, leading to a single time lag, the time taken to apply only one signal.

When a carrier signal of L0 is applied to the gate, it is split into two by BS1. The lower signal into the LOB is blocked by the polarizer, and the upper signal into the LZB passes through the polarizer into the output unchanged, L0. Note that the B and C signals are not applied to that branch. That case represents the first four rows of the truth table.

On the other hand, when a carrier signal of L1 is applied to the gate, it is split into two by BS1. The upper signal into LZB is blocked by the polarizer and the lower signal into the LOB passes through the polarizer, unaffected by CPIB0 for a B input of L1, and then is split into two by BS2. As an L1 carrier signal, it is blocked by the polarizer of the upper branch (LZB) and passes through the polarizer in the LOB, lower branch. For a C signal of L1, the carrier passes unchanged, (last row of Table 19); and for a C signal of L0, the carrier state changes to L0, (one-before-last row of Table 19). All other combinations of input signals can be understood in the same way.

4.2.2.4 Rail Road architecture

The process of changing the carrier path according to the control signal, if and where needed, is similar to the Rail Road (RR) crossover, hence the Rail Road architecture. The carrier in this case is similar to a bullet train traveling at the speed of light on a RR system that is preconditioned by crossover actions of the control signals to determine its destination, the output polarization state.

The RR-architecture lends itself easily to software control, leading to a RR-reconfigurable architecture in which the hardware is computer controlled to change the architecture to any desired one in real time, for rapid prototyping purposes, for

example. This provides ultra fast adaptability and optimization for application-specific needs.

4.2.3 Sequential Boolean expressions

The sequential Boolean expression is defined here as one that is represented by gates that all have one optical input and one electrical input, and hence can be cascaded in sequence. As an example, Figure 24 shows the digital design of the Boolean expression ABC+D.

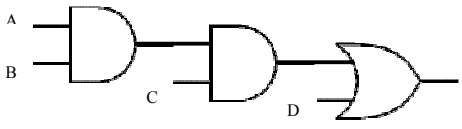

Figure 19 Digital circuit design of the sequential Boolean expression ABC + D.

That design can be implemented using the all-optical processing standard gates discussed in Section 3.3, where the microelectronic gates are replaced with the optical ones. It can also be implemented as a RR-architecture POP. Table 20 shows the extended truth table for that expression and Figure 25 shows the reduced design as a RR-architecture POP, following the design algorithm of Section 4.2.1 and the design reduction rules of Section 4.2.2.2.

Note that only three BSs are used, along with five CPIBs. The number of CPIBs required is only two, where the three upper CPIB1s are to be combined into one by directing the output of the three polarizers of the three LZBs together through one CPIB1. Therefore, the design is actually composed of three BSs, two CPIB0, and one

CPIB1. Always remember that the output carrier is only one carrier, and that all output paths converge into one by steering. They are left unsteered for clarity.

Table 20 Extended truth table for the sequential Boolean expression ABC+D.

A	a	B	b	C	c	D	d	Z
0	0	0	0	0	0	0	0	0
						.-.-.-.-.-.-.		
0	0	0	0	0	0	1	1	1
				…….....				
0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	1	1	1

0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	1	1	1
0	0	1	0	1	0	0	0	0
0	0	1	0	1	0	1	1	1
_____								
1	1	0	0	0	0	0	1	0
						.-.-.-.-.-.-.		
1	1	0	0	0	0	1	0	1
				…….....				
1	1	0	0	1	0	0	1	0
1	1	0	0	1	0	1	0	1

1	1	1	1	0	0	0	1	0
						.-.-.-.-.-.-.		
1	1	1	1	0	0	1	0	1
				…….....				
1	1	1	1	1	1	0	1	1
						.-.-.-.-.-.-.		
1	1	1	1	1	1	1	1	1

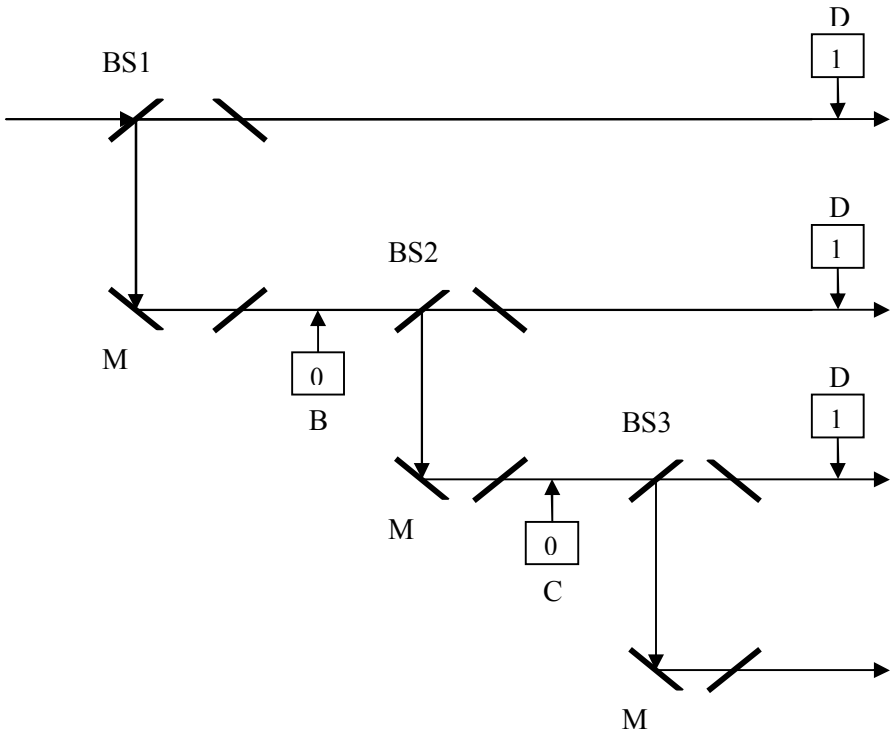

Figure 24 RR-architecture POP design of the sequential Boolean expression ABC+D.

4.2.4 Non-sequential Boolean expressions and electro-elimination

The non-sequential Boolean expression is defined here as one that includes gates with two optical inputs. For example, see Figure 26, which represents the Boolean expression AB+CD. Such a Boolean expression can be implemented using the all-optical processing gates, discussed in Section 3.3, as gates of one optical input only when one gate output is converted to electrical input. On the other hand, it can also be implemented using the RR-architecture POP discussed above by applying the design algorithm of Section 4.2.1, eliminating the need to convert any gate output into electrical input, hence electro-elimination. The results are given in Table 21 and Figure 27. As always, the bullet train simulation simplifies understanding the operation of the design.

The RR-architecture POP design of Figure 27 clearly invites elimination and reduction. It is clear that it reduces to a three-BS three-CPIB design.

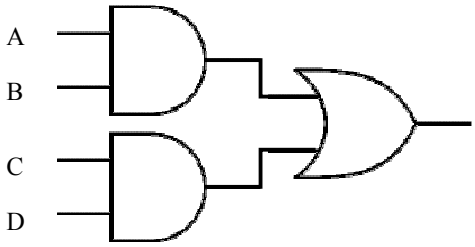

Figure 25 Digital circuit design of the non-sequential Boolean expression AB+CD

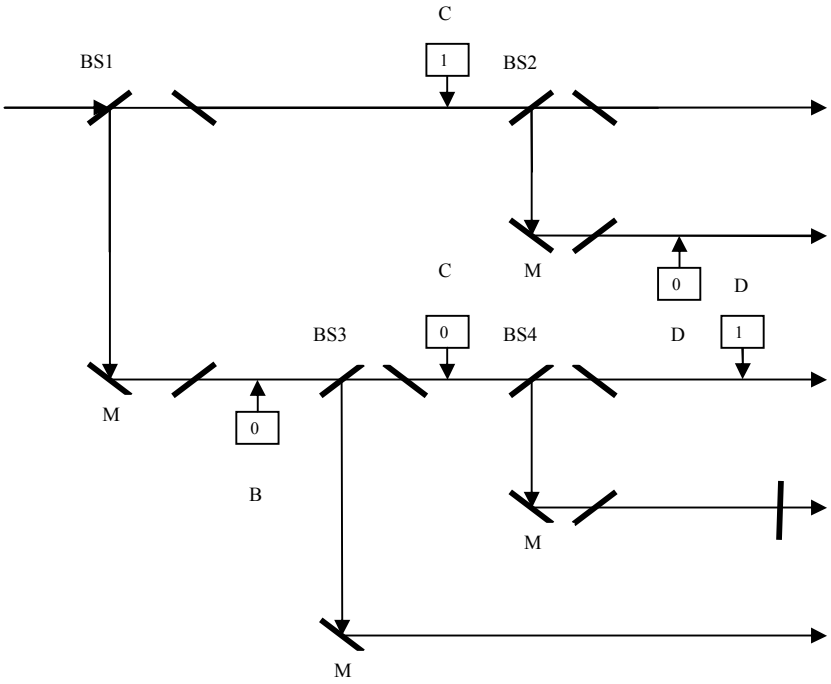

Figure 26 RR-architecture POP design of the non-sequential Boolean expression AB+CD

Table 21 Extended truth table for the non-sequential Boolean expression AB+CD.

A	a	B	b	C	c	D	d	Z
0	0	0	0	0	0	0	0	0
						.-.-.-.-.-.-.-		
0	0	0	0	0	0	1	0	0
						……..		
0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1

0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0
0	0	1	0	1	1	0	1	0
0	0	1	0	1	1	1	0	1
1	1	0	0	0	1	0	1	0
						.-.-.-.-.-.-.		
1	1	0	0	0	1	1	1	0
						……..		
1	1	0	0	1	0	0	1	0
1	1	0	0	1	0	1	0	1

1	1	1	1	0	1	0	1	1
						.-.-.-.-.-.-.		
1	1	1	1	0	1	1	1	1
						…….		
1	1	1	1	1	1	0	1	1
						.-.-.-.-.-.-.		
1	1	1	1	1	1	1	1	1

4.3 Practical Design Examples

This section includes useful practical designs that are obtained using the algorithm previously introduced in Section 4.2.1. Applying the algorithm as explained, one can obtain the designs for practical circuits such as the POP half adder in Figure 28 [36], the POP Full adder in Figure 29 [36], and threshold gate in Figure 30.a and Fig 30.b [37].

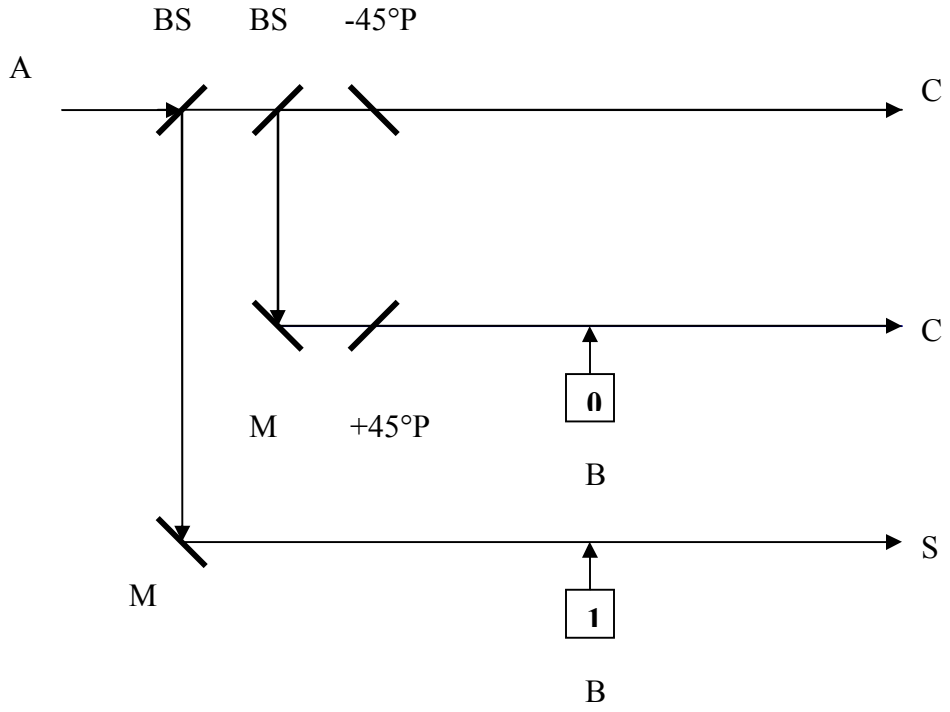

Figure 27 RR-architecture POP design of a half adder

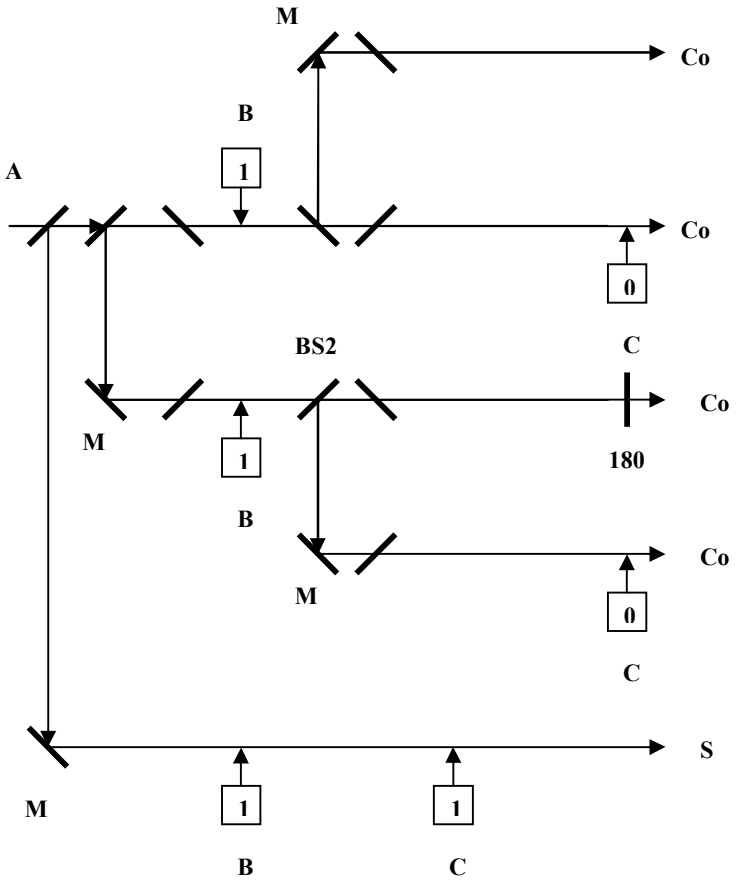

Figure 28 RR-architecture POP design of a full adder

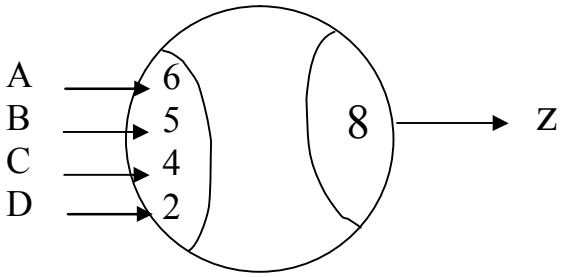

Figure 30.a A 4-input threshold gate

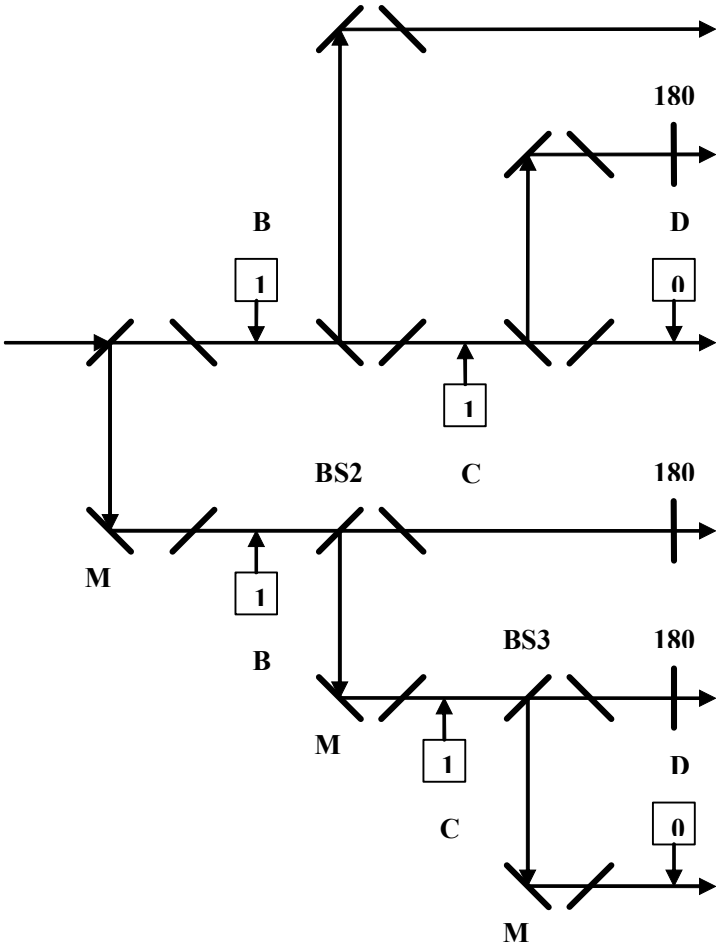

Figure 29.b RR-architecture POP design of the 4-input threshold gate in Figure 30a.

CHAPTER V

PASSIVE ALL-OPTICAL SWITCHING AND GATES

In this section, we introduce the passive all-optical polarization switch, which includes no electro-optic element and modulates light with light. That switch is used with feedforward to construct all optically any and all of the binary logic gates of two or more inputs and a single output. We discuss the design concepts and the operation of the AND and OR gates as two examples. The direct designs of other gates, such as the two important NAND and NOR gates, are also given. The rest of the 16 logic gates are similarly designed, but are not included. Cascading of such gates is straightforward as shown and discussed in the paper. Cascading in itself does not require a power source, but feedback at this stage of development does. The design and operation of an SR (set reset) Latch is presented and briefly discussed as one of the popular basic sequential devices used for memory designs in digital logic today. That completes the essential components of an all-optical polarization digital processor. The speed of such devices is well above 10 GHz for bulk implementation, and is much higher for chip-size implementation.

5.1 Introduction

The possibility of using light polarization to represent binary logic was first proposed in 1986 by providing a speculative account of combining nonlinear optics and

polarization optics [1]. In 1987, the same author suggested spatial filtering logic based on polarization [2]. Also, in 1987, other authors introduced polarization-based optical parallel logic gate utilizing ferroelectric liquid crystals, where the two parallel and perpendicular polarizations were used to represent the two states of binary logic, where only the XOR and XNOR gates could be realized [5]. In the same year, other authors introduced polarization-encoded optical shadow-casting logic units and its design [8]. Masks and on/off logic representation were used, and multiple-valued logic based multiprocessor using polarization-encoded optical shadow-casting were later developed in 1993 [10]. In 1990, polarization-based optical logic using laser-excited gratings were introduced, [13] and in 1992 polarization-coded optical logic gates for N-inputs using vertical/horizontal input logic representation and on/off output logic representation were introduced [6]. The polarization encoding was not carried through to the output in such a design. In 1993, polarization-encoded optical logic operations in photorefractive media were considered [4]. Theory of an improved polarization-encoded logic algebra used for the design of an optical gate for a 2D data array was introduced in 1995 [7]. That algebra is completely different from the well established and widely used digital logic [30]. Also, in 1994, implementation of the 16 logic functions of two input patterns based on the birefraction of uniaxial crystals was suggested as integrated polarization-optical logic processor [3]. In 1996, logic gates based on digital speckle pattern interferometry were introduced as the digital polarization-encoded technique for optical logic gate operations [14]. Shadow-gram based Boolean logic gates are introduced in 1997 and related analysis and evaluations of logical instructions called in parallel digital optical operations based on optical array logic are introduced in 2004 [11, 12].

In 2007, optics inspired logic architecture, which is similar to the Fredkin and Toffoli conservative logic, is introduced [38]. In 2008, ultrafast all-optical logic gate using a nonlinear optical loop mirror based multi-periodic transfer function, where a complete set of all-optical logic gate operations are reported, is introduced [39]. In all the published literature, only the horizontal and vertical polarizations are used to represent logic 1 and logic 0, which limits the usefulness of an infinite complex plane to only two points, one at the origin and the other at infinity [15, 29]. In the suggested gates, 1) some form of nonlinearity is used, 2) many require special untested algebra that is completely different from the well known and matured digital logic, 3) many use spatial masks which drastically reduces the speed of operation of the gates and impede cascading, 4) none uses other than the two vertical and horizontal polarizations, if any, and 4) none carries the polarization representation through to cascading and on/off representation is defaulted to, which is actually intensity representation, leading to drastically reduced speed of operation.,

In the previous chapters, we introduced the use of any two orthogonal polarization states of an electromagnetic wave to represent logic 1 (L1) and logic 0 (L0) of two-valued binary logic. We also introduced several design architectures including the ortho-parallel design of any, and all, digital binary gates in which an electro-optic switch was used to input the second signal to the gate. The designs were easily cascadable because the information is carried on, and manipulated as, the signal polarization, and not as its intensity [15, 29].

In this chapter, we introduce the all-optical polarization switch, which has two optical inputs and one optical output, in which no electro-optic element is used. We

also introduce binary logic gate designs using such a switch and feedforward within the gate itself. The use of feedback leads to the design of sequential logic devices, and we close by a design for an SR Latch.

The all-optical polarization designs of sequential and non-sequential logic devices clearly leads to the all-optical polarization digital processor. Such a processor, as its components, is of a very high speed of operation only determined by the speed of light. This is due to the fact that we are modulating light with light. A bulk device speed is to start at a higher speed than the current 10 GHz of semiconductor devices. A chip-size device speed is at a much higher value.

Because the operation of the all-optical polarization (AOP) gates and devices is achieved through routing of the optical signals and polarization manipulation of it, and because polarization is well theoretically and experimentally developed and understood for more than a hundred years today, the operation and performance is guaranteed as explained.

5.2 Passive All-Optical Polarization Switch

The passive all-optical polarization switch, shown in Figure 31, has two input signals (X_1 and X_2) and one output signal (Z). The operation of this switch is based on changing or keeping the input polarization state of one signal X_1 depending on the polarization state of a second signal X_2. Keep in mind that the two polarization states represent L0 and L1, and that they are two orthogonal polarization states. For the case of $\pm 45^o$ polarization states representing the L1 and L0, respectively, we use a horizontal polarizer (HP) in the X_1 input, a vertical polarizer (VP) in the X_2 input, and a

beam splitter acting as a beam collector (BC) as shown in Figure 31.a. The output of the BC (shown by Z in Figure 31.a) is the switch output.

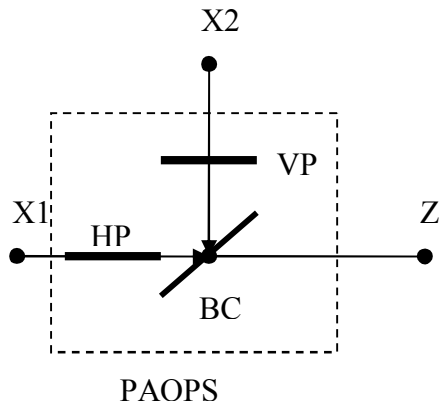

Figure 30.a Passive all-optical polarization switch (PAOPS). The two inputs are X1 and X2: X1 inputs the horizontal component of its input wave and X2 inputs the vertical component of its respective input wave. Z is the output signal combining the two input horizontal and vertical components. Instead of using two input polarizers and a beam splitter as a beam collector BC, as shown in figure for clarity, a polarizing beam splitter is used in practical implementation, as in Figure 31.b.

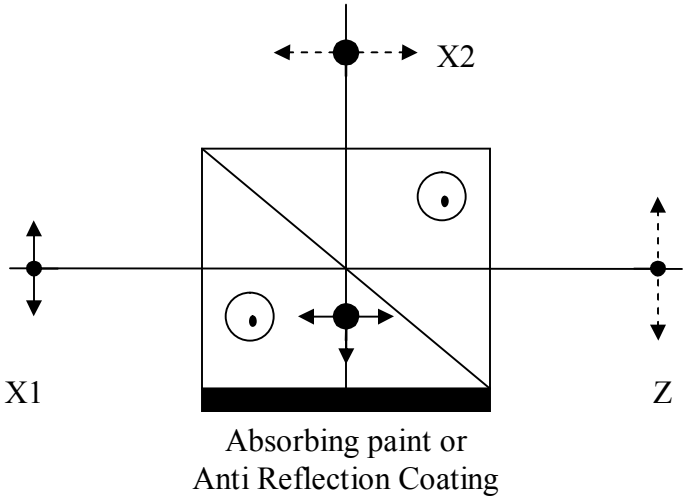

Figure 31.b A birefringent-polarizer implementation of the passive all-optical polarization switch (PAOPS).

Instead of using two input polarizers and a beam splitter as a beam collector (BC), a polarizing beam splitter (PBS) can be used in the actual implementation, as shown in Figure 31.b. A birefringent polarizer (BP) of the Glan-Foucault (sometimes called Glan-Air) type with or without a Taylor modification, or of the Glan-Thompson type, may be used for that purpose [28, 40]. The optic axes of the two prisms are parallel to each other and perpendicular to the page plane. The two input signals, X_1 and X_2, are decomposed into two components one parallel to the optic axis (horizontal-polarization (HP) component) and the other perpendicular to the optic axis (vertical-polarization (VP) component). The HP component of each of the two optical signals goes straight through the device unchanged, and the VP component of each totally internally reflects at the diagonal of the BP. The absorbing paint or anti-reflection coating shown in Figure 31.b absorbs the falling optical signal on it, and the BP output Z is an optical signal composed of the HP component of the X_1 optical signal and the VP component of the X_2 optical signal.

The operation of the switch is very simple. For the case of X_1 = L0 (-45^o polarization state) the output is 1) Z = L1 ($+45^o$) for X_2 = L1, and 2) Z = L0 for X_2 = L0. That is a $0^o/180^o$ switch activated by an L0/L1 control signal [15, 29]. On the other hand, if the negation of the output is required ($180^o/0^o$ switch), the output signal is simply inverted using a 180^o retarder R (HWP) or by negating the two inputs. The input/output signals are X_1/Z and the control signal is X_2. For case 1) above, as the X_1 signal goes through HP, only its horizontal component reaches the BC; as the X_2 signal goes through VP, only its vertical component reaches the BC. The BC combines both components into a $+45^o$ output signal polarization: L1. On the other hand, for case 2)

the same takes place with an output signal polarization of -45°. It is clear that the vertical component of X_2 determines the polarization state of the output signal Z.

For the other case of X_1 = L1 (+45° polarization state) the output is 1) Z = L1 (+45°) for X_2 = L1, and 2) Z = L0 for X_2 = L0, which is a 180°/0° switch activated by an L0/L1 control signal. Again, if the negation of the output is required (0°/180°), either the output signal is negated or the two input signals are. Still the input/output signals in this case are X_1/Z, and the control signal is X_2. The operation of the switch is the same as above.

As we discussed above, a properly aligned polarizing beam splitter PBS can replace the three-element combination of HP, VP, and BC. The operation of the switch in this case is as explained in the previous paragraphs. It is important to realize that the switch does not require a power source to operate, hence a passive switch. It functions on the signals themselves. One of the useful applications of the passive all-optical polarization switch is to build binary logic gates, any and all of them. In the following section, we use the passive all-optical polarization switch to build some of the important gates.

5.3 Passive All-Optical Polarization Binary Logic Gates

Figure 32 shows one possible construction of a passive all-optical polarization AND gate. Two polarizing beam splitters PBS_1 and PBS_2 that are adjusted to direct polarized input beams of polarizations ± 45° into two separate branches (as shown schematically in Figure 32) are used. In addition, two passive all-optical polarization switches ($PAOPS_1$ and $PAOPS_2$) are used to switch the respective beam polarizations

as needed with outputs D and F, respectively. The inputs to $PAOPS_1$ are X_1 and X_2, and the output is Z, which is composed of the HP component of X_1 and the VP component of X_2, as discussed in Section 5.2. Similarly, the inputs to $PAOPS_2$ are X_1' and X_2', and the output is Z', which is composed of the HP component of X_1' and the VP component of X_2'. The inputs to the overall gate are signals A and B, and the output is a single beam obtained by using a beam splitter as a beam collector BC to collect Out_1 and Out_2 of Figure 32. That BC is not shown in Figure 32 for clarity.

The operation of the gate is straightforward. Table 22 gives the polarization state of the beams as they travel through the gate, including the two input signal beams A and B, and the two output signals Out_1 and Out_2, where only one is active at a time and both are never active simultaneously. Therefore, the BC output, which is the gate output, is composed of either Out_1 or Out_2. A polarizer P in the path of Out_1 is fixed at $+45^o$. Note that the combination of a beam splitter and the two $\pm 45^o$ polarizers (e.g., BS_1, $+45^o$ P, and -45^o P) is replaced by a polarizing beam splitter (PBS) for practical implementation. Here we prefer to use the combination of BS and 2Ps for better understanding of the gate operation. It is assumed here that the BS is lossless and divides its input beam into two equivalent beams (same polarization as the input and 50% of the incident power for each beam). All polarizers are assumed to be ideal (zero loss in the desired polarization and perfect absorption of the undesired one).

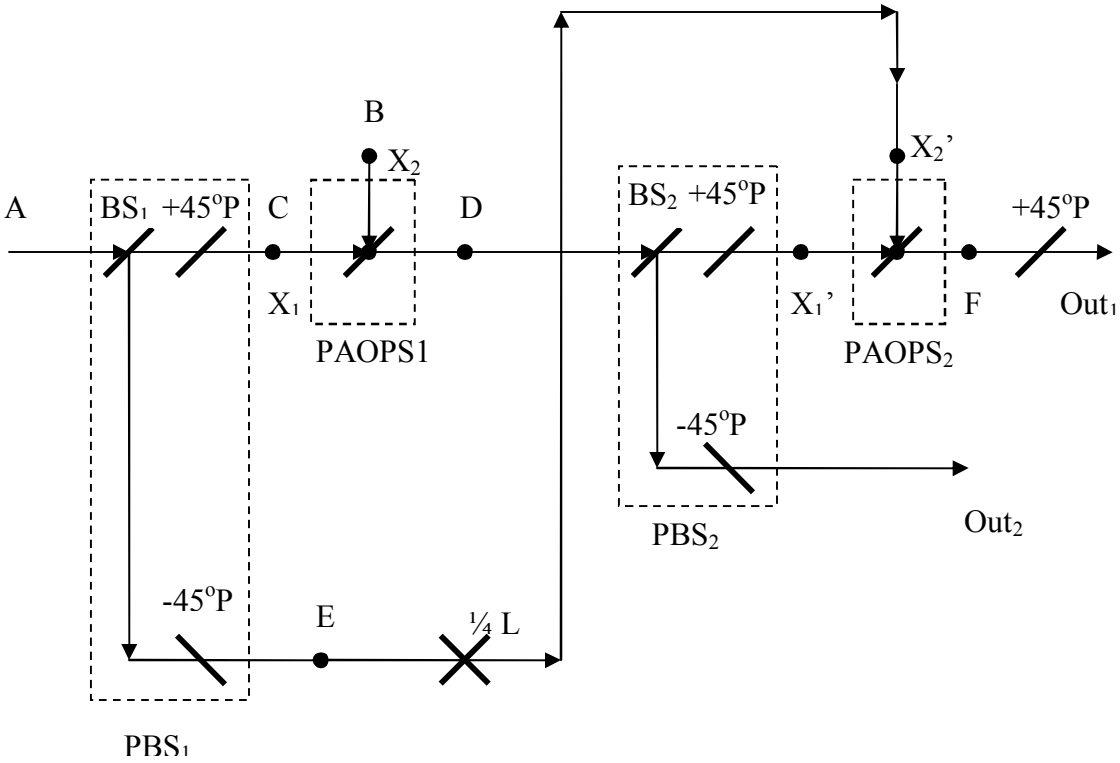

Figure 31 Passive all-optical polarization AND (PAOP AND) gate. The two beam splitters BS1 and BS2 are followed, each, by a + 45o and a – 45o polarizers. The BS and two polarizers can be replaced by a single polarizing beam splitter PBS. The ¼ L is a ¼ intensity attenuator. PAOPS1 and PAOPS2 are two passive all-optical polarization switches (see Figure 31). The beam is routed using mirrors that are not shown here for clarity. The output signal of the gate is a single beam obtained using a beam splitter (not shown here for clarity) acting as a beam collector of Out1 and Out2. For gate operation, see Table 22.

Table 22 Operation table of a PAOP AND gate showing the polarization state of the signal beam at different points through the gate, see Figure 32. The output signal intensity Iout is also shown, as a ratio of the input intensity Io, for the 4 logic states of the gate. The polarization of the output signal of the gate Z is given, which is the output of a beam collector (BC) collecting the two signals Out1 and Out2 (not shown in Figure 32).

A	B	C	D	E	F	Out_1	Out_2	I_{out}	Z	A	B	Z
-45	-45	0	↓	-45	-45	0	-45	$I_o/4$	-45	0	0	0
-45	+45	0	↑	-45	-45	0	-45	$I_o/4$	-45	0	1	0
+45	-45	+45	-45	0	0	0	-45	I_o	-45	1	0	0
+45	+45	+45	+45	0	→	+45	0	$I_o/4$	+45	1	1	1

To understand the operation of the logic gate shown in Figure 32, we consider a case when both inputs A and B are of -45^o linear polarization (representing L0). For this choice of input polarizations there is no signal at point C, and all of signal A is routed to point E. Therefore, the beam at point E has a polarization of -45^o with the full input beam intensity I_o. An attenuator is placed after point E to attenuate the signal intensity to one quarter of the input signal intensity (i.e., $I_o/4$). That attenuated signal reaches input X_2' of the $PAOPS_2$, leading to Out_1 signal. The two inputs to $AOPS_1$ are $X_1 = C = 0$ and $X_2 = B$, which is the second input signal beam. The output of $PAOPS_1$ at point D is therefore the vertical component of signal B, which is the vertical component of a -45^o polarized beam of intensity $I = I_o$, at D the intensity is therefore $I_D = I_o/2$. This signal travels to the PBS_2 (BS_2 and two $\pm 45^o$P combination) and passes through as a $+45^o$ polarized beam into the upper branch with an intensity of $I_o/4$ and a

– 45° polarized beam into the lower branch with an intensity of $I_o/4$ also. The + 45° component inputs to $PAOPS_2$ through X_1' (the HP input). Therefore, the output of $PAOPS_2$ is a beam of -45° polarization which is then crossed by the output polarizer. Accordingly, $Out_1 = 0$, and no signal exists in that output branch. The – 45° component exits the gate at Out_2 with an intensity of $I_o/4$ and is collected by the output BC. The output is, therefore, L0. Accordingly, the first row of Table 22 represents the first row of an AND gate: A B Z / 0 0 0, where Z is the gate output signal. The performance of the gate represented in the second row of Table 22 is similar to the explanation of the first row just discussed.

For the case of an A input of L1 (i.e., + 45°) polarization, that input beam is directed to the upper branch. Therefore, the signal beam at point C is of a + 45° polarization and an intensity of I_o, that of the input beam A. The lower branch receives no signal by PBS_1 and no signal exists at point E or the X_2' input to $PAOPS_2$. The signal beam of point C inputs $PAOPS_1$ at input X_1' (HP input) and the input signal B of a – 45° polarization (L0) inputs $PAOPS_1$ at input X_2 (VP input). The signal at point D is the output signal of $PAOPS_1$ and is, therefore, a – 45° signal of intensity $I = I_o$, that of the input beam. Signal D now is directed by PBS_2 into the lower branch, Out_2, and exits the gate through the BC at the output, which is not shown in Figure 32. Accordingly, the output beam is of a - 45° polarization and intensity I_o. The upper branch at PBS_2 receives no signal, and accordingly the X_1' input of $PAOPS_2$ receives no signal. Therefore, as both the two inputs of $PAOPS_2$ receive no signal, Out_1 will carry no signal, and only Out_2 is active. In this case, the two inputs to the gate A and B are L1

and L0, respectively, and the output is L0, which is the third row of Table 22. The fourth row of Table 22 can simply be understood in a similar way as row 3.

From Table 22, it is clear that the structure shown in Figure 32 is an AND gate. It is also clear that the intensity of the gate output signal is not equal in all four input combinations: $I_o/4$, $I_o/4$, I_o, $I_o/4$, respectively. Therefore, for cascading purposes, 1) an optical amplifier, saturating at I_o, is to be used at the output to bring all to the same intensity of I_o, 2) a 4X optical amplifier is to be used within the gate to bring all to I_o, 3) a ¼ attenuator is to be used within the gate to continue to use the gate as a passive device, with no power source required; as discussed in Section 5.4. Finally, a NAND gate can be obtained from the AND gate discussed above by simply adding a 180^o retarder (HWP) in the gate output: after the output BC.

Figure 33 and Table 23 show the construction and operation of an OR gate. Clearly, a NOR gate is the same as the OR gate with an added retarder, inverter, in the output.

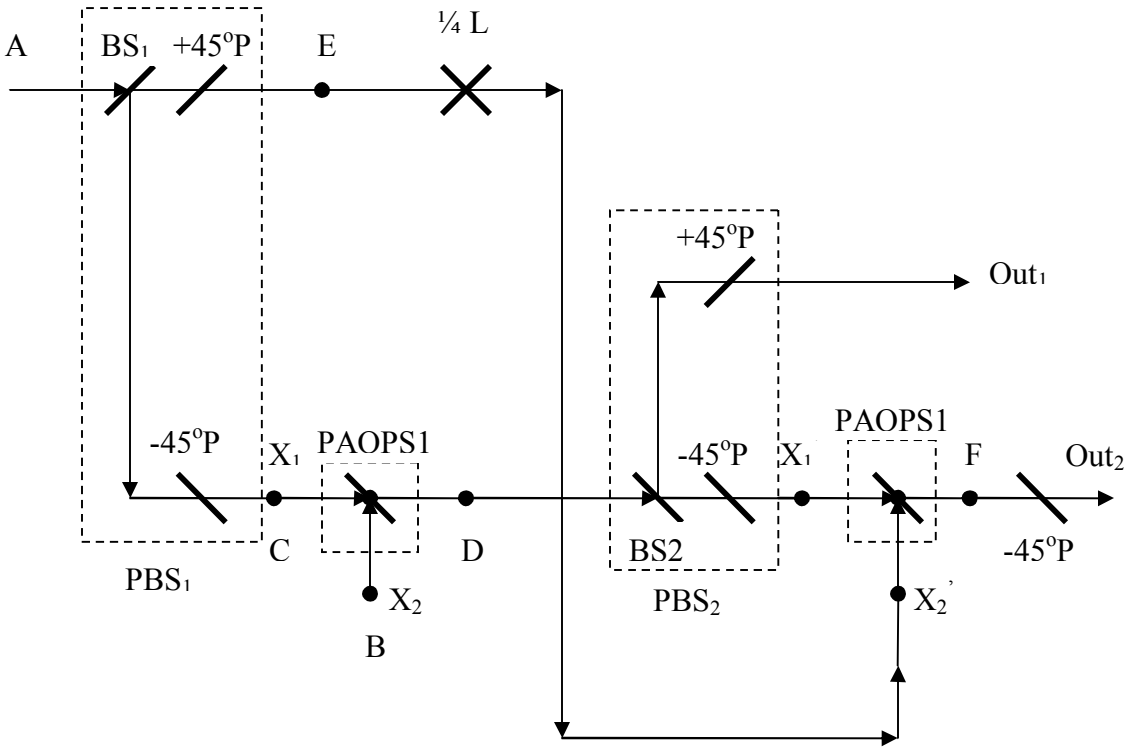

Figure 32 Same as in Figure 32, but for a PAOP OR gate, see Table 23.

Table 23 Same as in Table 12, but for a PAOP OR gate, see Figure 33.

A	B	C	D	E	F	Out_1	Out_2	I_{out}	Z	A	B	Z
-45	-45	-45	-45	0	↓	0	-45	$I_o/4$	-45	0	0	0
-45	+45	-45	+45	0	0	+45	0	I_o	+45	0	1	1
+45	-45	0	↓	+45	+45	+45	0	$I_o/4$	+45	1	0	1
+45	+45	0	↑	+45	+45	+45	0	$I_o/4$	+45	1	1	1

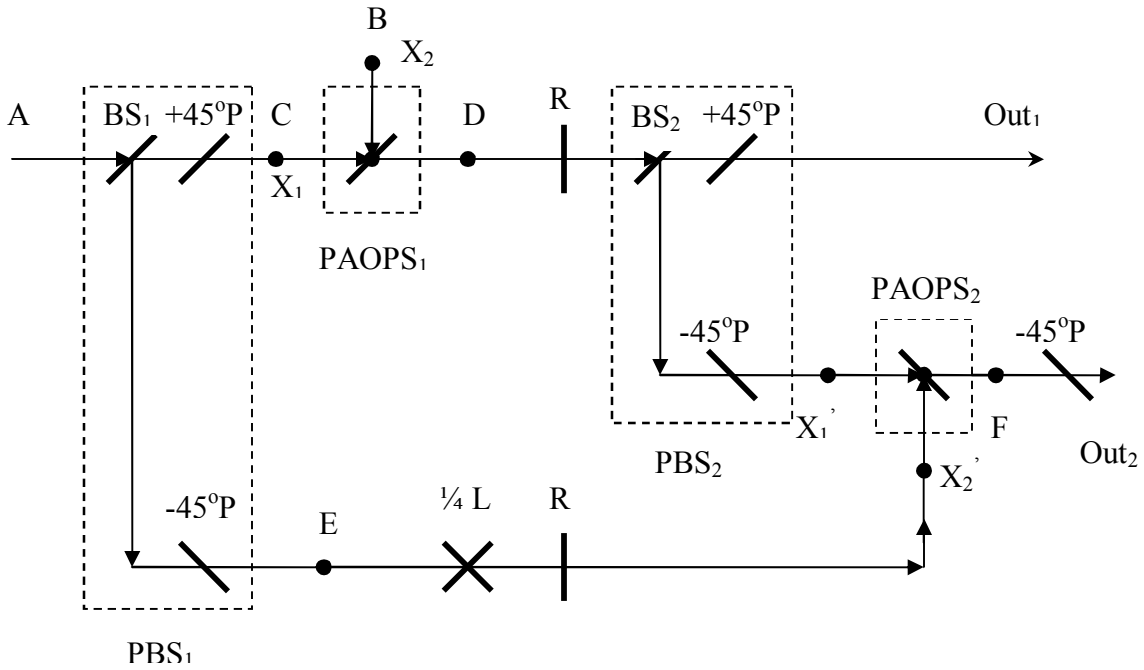

Figure 33 Same as in Figure 32, but for a PAOP NAND gate. R is a 180° retarder (e.g., HWP), and ¼L is an I/4 attenuator.

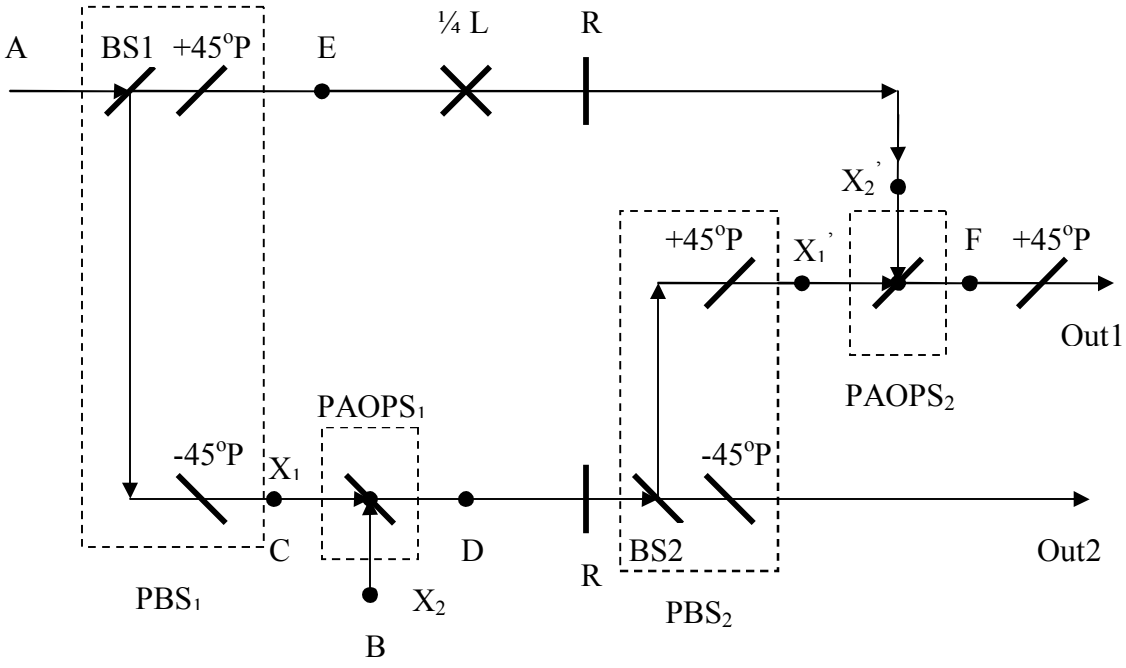

Figure 34 Same as in Figure 32, but for a PAOP NOR gate.

Figures 34 and 35 give direct independent designs of NAND and NOR gates, which includes two retarders within the gate itself in each design. As an example, to understand the operation of the logic gate shown in Figure 34 (PAOP NAND), we consider a case when both inputs A and B are of -45^{o} linear polarization (representing L0). For this choice of input polarizations there is no signal at point C, and all of signal A is routed to point E. Therefore, the beam at point E has a polarization of -45^{o} with the full input beam intensity I_o. An attenuator is placed after point E to attenuate the signal intensity to one quarter of the input signal intensity (i.e., $I_o/4$). The polarization of this attenuated signal is transformed to $+45^{o}$ by passing through the retarder R (e.g., a HWP) and reaches input X_2' of the $PAOPS_2$. The two inputs to $PAOPS_1$ are $X_1 = C = 0$ and $X_2 = B$, which is the second input signal beam. The output of $PAOPS_1$ at point D

is therefore the vertical component of signal B, which is the vertical component of a - 45^o polarized beam of intensity $I = I_o$: at D the intensity is therefore $I_D = I_o/2$. The polarization of this signal is changed to the vertical component of a + 45^o by passing through R. It then travels to the PBS_2 (BS_2 and two $\pm 45^o$P combination) and passes through as a + 45^o polarized beam into the upper branch with an intensity of $I_o/4$ as $Output_1$, and as a – 45^o polarized beam into the lower branch with an intensity of $I_o/4$, also. The - 45^o component inputs to $PAOPS_2$ through X_1' (the HP input). Therefore, the output of $PAOPS_2$ is a beam of + 45^o polarization which is then crossed by the output polarizer; remember that the input to X_2' is a + 45^o polarized signal of $I_o/4$ intensity as discussed above. Accordingly, $Out_2 = 0$, and no signal exists in that output branch. The + 45^o component exits the gate at Out_1 with an intensity of $I_o/4$ and is collected by the output BC. The output is, therefore, L1. Accordingly, the first row of a NAND gate is satisfied: A B Z / 0 0 1, where Z is the gate output signal. Similarly, the other three rows of the NAND gate are satisfied and can be similarly understood.

It is important to note that the gates action is achieved through propagation of the beams within the gate construction and that control of the gate is achieved through beam interaction: light is modulated with light. Also, the operation of the gates does not depend on the wavelength, and gates can be designed and operated at any desired frequency, as long as polarizers and beam splitters, or birefringent polarizaers, at the desired wavelength exist.

It is also important to realize that the gate does not require a power source to operate. The operation is achieved through routing of the beam, and the use of a switch

and a polarizing element that does not require power to operate, neither. See Section 5.4 for cascading considerations.

Because of the use of light modulation using light, and due to the fact that there are no electro-optic devices used in the designs, the speed of operation of all gates is only limited by the speed of light which determines the propagation delay. A bulk gate would, therefore, operate at a speed well above the current 10 GHz speed of microelectronics. A chip-size gate would operate at a much higher speed since the distances travelled by the signal within the gate are much smaller in this case, leading to much smaller propagation delays, and accordingly to much higher speeds of operation.

The feedforward used in the design, and feedback as shown in Section 5.5, allow direct design of sequential and non-sequential devices such as latches and flip flops for example. In addition, passive and non-passive AOP binary logic gates discussed in this and the following sections can be used for that purpose, using the well-developed regular digital design concepts already in use today for semiconductor devices.

5.4 Cascading

It is important to recognize that the two input signals to each logic gate described here, are of the same intensity I_o. From the operation tables of the AND and OR gates, (Tables 27 and 28, respectively) we see that the output intensity is not equal in the four states of the gate. Accordingly, for cascading purposes, we either make the output signal intensity equal to I_o for the four states, or make sure that the input signals

to the gate, two or more, are of the same intensity I_o. This can be achieved using several approaches. Figure 28 provides one possible solution. We use the output of a properly designed attenuator to feedforward ¾ of the signal at that point to Out_2, which renders that signal in the corresponding three gate states to I_o [21]. The output signal of the fourth state, of the last row of Table 22 for the AND gate, is brought to an intensity of I_o by a 4X amplifier, as shown in Figure 28. With that simple modification to the gate design, we now have the output intensity equal to the input intensity, neglecting any minute losses within the gate. Obviously, this solution requires power input to the gate, and the gate is not passive anymore. The 4X amplifier works only in the one case represented by the last row of Table 22, where both inputs to the gate are L1.

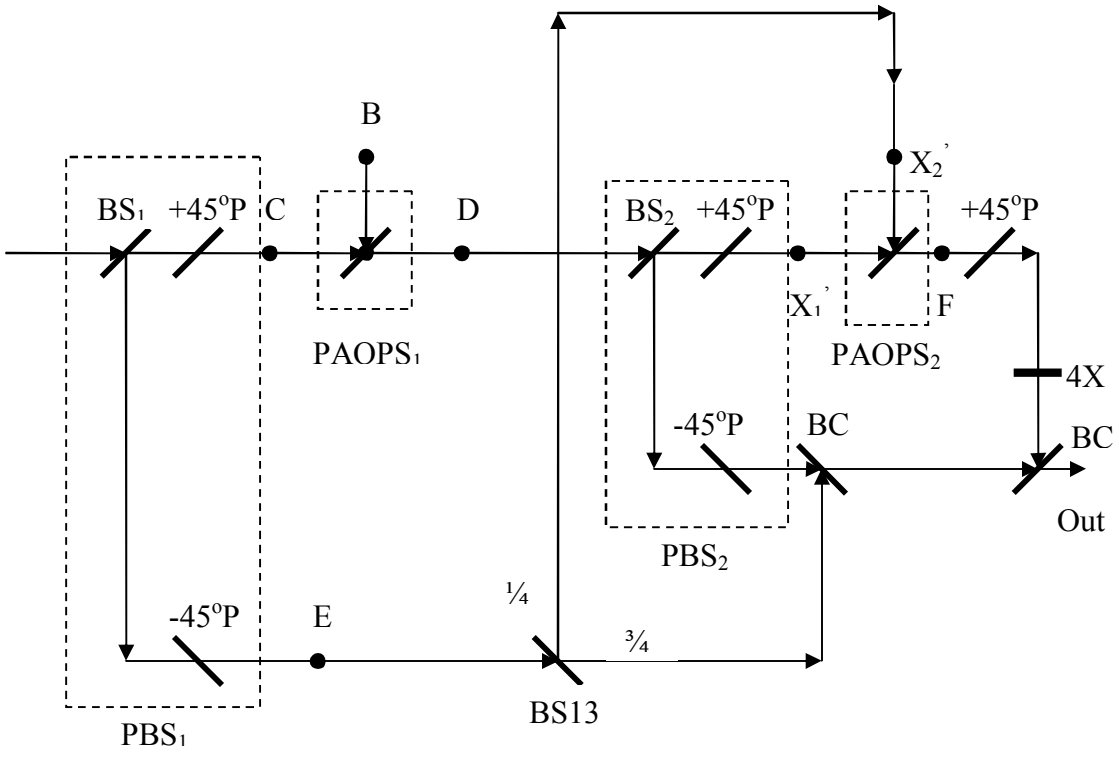

Figure 35 Same as in Figure 32, but for an AOP AND gate with an output signal of the same intensity as that of the input signals. 4X is an amplifier. BS13 is a ¼ and ¾ beam splitter, which is easily implemented using a Polarization Preserving Device (PPD).

A second possible solution is to use a saturation amplifier in the output of the gate to bring the intensity to I_o. In this case, the gate requires more power to compensate for the power lost in the I/4 attenuator (see Figure 32, for example). In this case, the saturation amplifier works in three of the four possible cases of operation of the gate. Another (similar but less economical) possible solution is to use two saturation amplifiers in the input beams to the gate to make sure that the input signals are of intensity I_o. Those solutions are presented just to show the simplicity of cascading. The use of amplifiers requires a power source. Regardless, a passive gate design that provides for cascading is to use an attenuator in Out_2, instead of an amplifier for Out_1, which requires no power source to operate. The gate output intensity is, therefore, reduced at each and every level of logic gates to $I_o/4$. If we start with a high input power, and the output power is reduced to one fourth the input power, we need to make sure in our digital design that the input to each and every gate is of the same power intensity by properly keeping track of the power level at every logic-design level (depth of the design). That is fine, since the intensity holds no information, and all information is in the polarization of the wave.

5.5 All-Optical Polarization Digital Processor

Possibility for the implementation of an all-optical polarization digital processor is evident at this point of discussion. The required memory element is easily achieved using a flip flop device which is a straight forward application of the discussions of Sections 5.3 and 5.4 above. Figure 37 shows an all-optical polarization SR Latch. SR Latches are the most popular digital sequential devices used to realize memories in

digital designs [30]. Following the operation of different gates discussed in Section 5.3, and using any of the cascading designs discussed in Section 5.4, one can easily follow the operation of the AOP SR Latch of Figure 37 which is composed of two cross-coupled NOR gates. Note that a 2X amplifier is added right before the exit BC to provide a signal of intensity I_o for both feedback and gate outputs. Also, note that the two inputs are S for set and R for reset, and the two outputs are Q and Q', which is the negation of Q. When S and R are both L1, the output state is undefined, as in any SR Latch [30].

Clearly, AOP S'R' Latches are similarly designed using two AOP NAND gates. Also, AOP SR Latches with control input using 4 AOP NAND gates, AOP D Latches using 4 AOP NAND gates and one AOP INV gate, etc can all be similarly implemented. In addition, the more complicated master-slave flip fop, and any other digital device (sequential or non-sequential), can all be similarly designed and implemented.

One simple and straight forward implementation of all AOP gates and devices uses fiber. In such a case, no mirrors are needed, and the 180^o retarder R is simply realized by rotating the fiber 90^o.

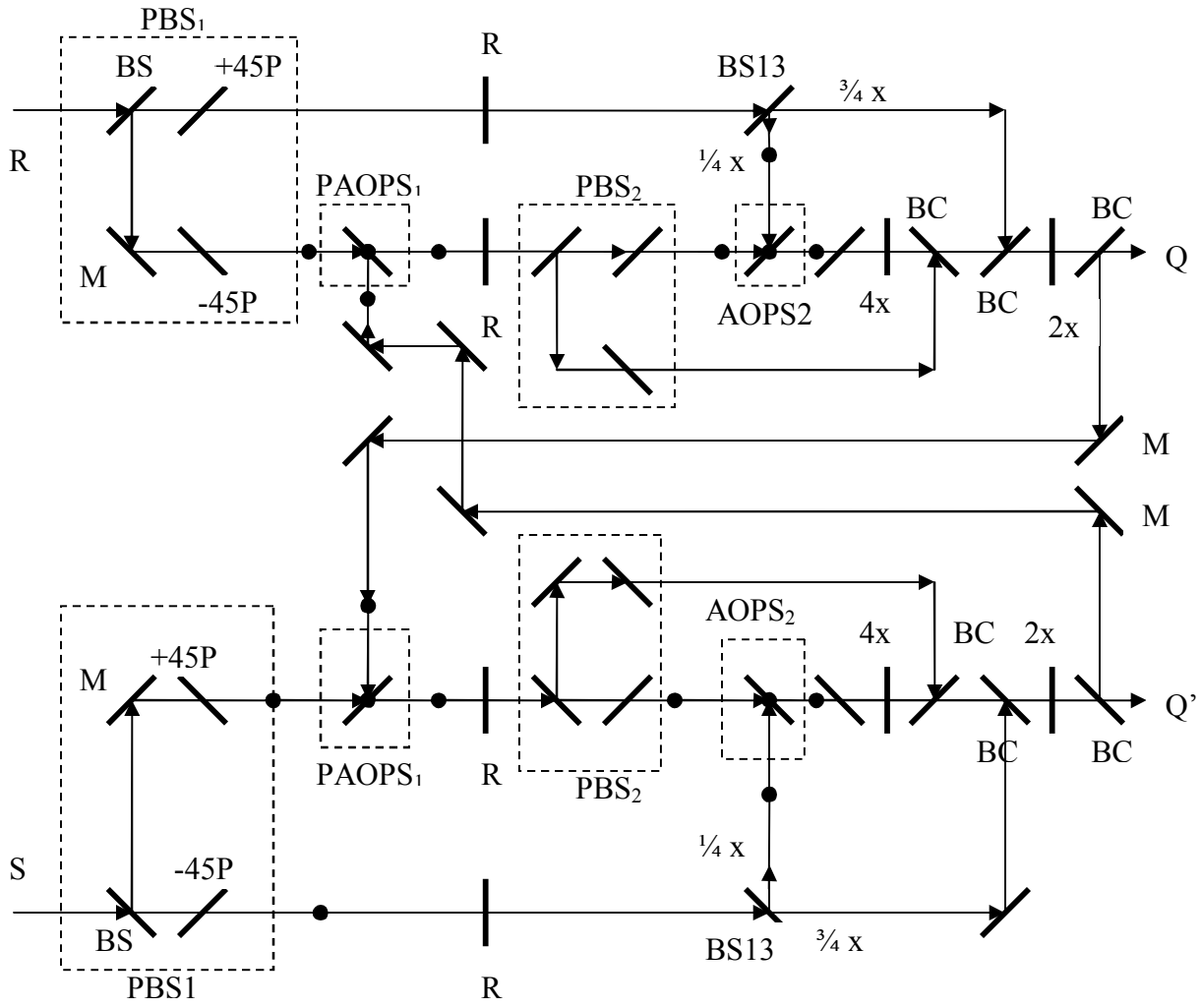

Figure 36 AOP SR Latch: two cross-connected AOP NOR gates, see Figure 35. The two inputs are S (set) and R (reset), and the two outputs are Q and Q', where each is the complement of the other.

CHAPTER VI

TESTING AND MEASUREMENTS

6.1 Introduction

In the previous chapters, a new optical-polarization-based representation and implementation of binary logic was introduced. We also introduced the Orthoparallel logic (OPL) architecture to design any and all of the binary logic gates, including the two global ones [15, 29]. In this chapter, we discuss the engineering, construction, and experimental verification of an all-optical-processing polarization NAND gate using this architecture. The implemented gate performed exactly as designed, with minimal errors that can be easily eliminated in a properly designed and optimized manufacturing process for volume manufacturing. We report here on only one implementation of the NAND gate using fiber optics technology and commercially available components. Other technologies are currently under active investigation.

We close by providing information on operating the implemented NAND gate as other binary logic gates, and on required minor modifications for the gate to perform as a Universal gate: one that can perform as any of the known binary logic gates.

6.2 Design and Operation

Figure 14 shows the design of a NAND gate using the Orthoparallel logic (OPL) architecture introduced in Chapter 3, [29]. The OPL architecture is based on representing the logic zero (L0) and logic one (L1) by two orthogonal polarizations,

and directing each one to a different branch of two parallel ones (logic zero branch LZB or logic one branch LOB) where the beam is manipulated differently to effect the required logic gate performance. For example, the input to the NAND gate shown in Figure 14 is an electromagnetic wave of any chosen frequency with a polarization of, say, - 45^o representing L0 which is then directed to the LZB by the polarization beam splitter (PBS) or + 45^o representing L1 which is then directed to the LOB by the PBS. The beam directed to the LZB undergoes a 180^o retardation in the complex ρ – plane (a half-wave plate for example) leading to a converted wave polarization of + 45^o, regardless of the control signal representing the second input to the gate. Accordingly, the output is L1 for both cases of L0 and L1 control signals. On the other hand, the beam directed to the LOB undergoes a 0^o or 180^o relative phase retardation depending on the control signal: control signal of L0 introduces a 0^o relative phase retardation and a control signal of L1 introduces a 180^o relative phase retardation. Such an operation is the two-level logic behavior of a NAND gate [29, 30].

6.3 Engineering and Construction

The currently reported realization of the first all-optical-processing NAND gate is decided to be implemented using the available components on the market for the OEM (Original Equipment Manufacturer). It is decided to be realized using optical fibers as one of the available technologies in the market. The wavelength of operation is selected to be 1550 nm, which is one of the popular wavelengths used in the telecommunications industry today. Figure 38 shows the implemented gate within the dashed box. In addition, Figure 38 also shows the external components used for testing

purposes. In the following subsections, we discuss in some details the components used.

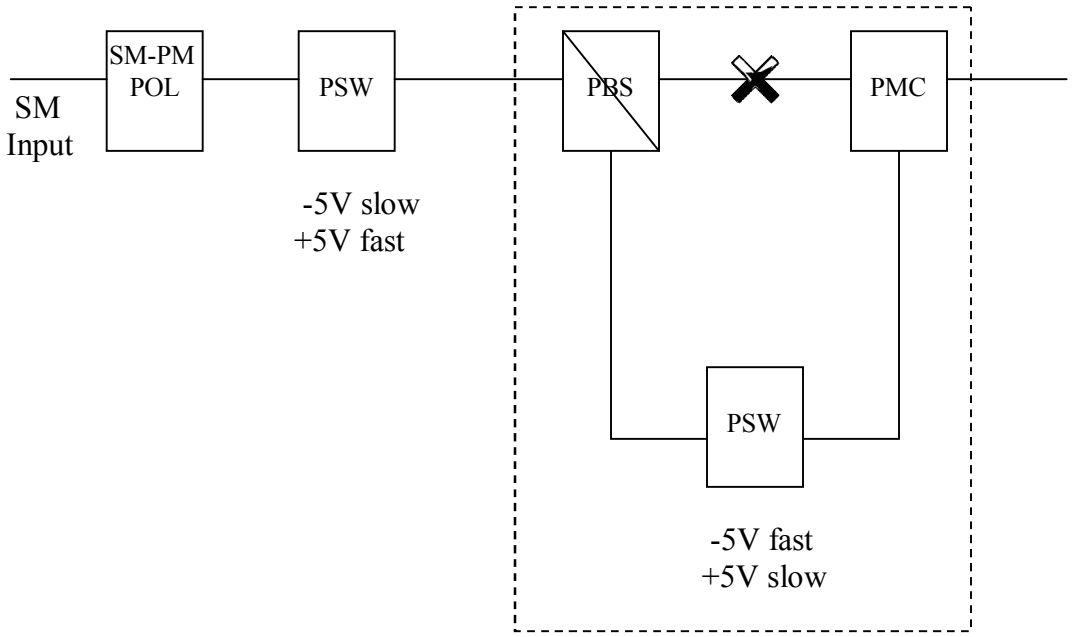

Figure 37 NAND gate: inside the dashed box. The in-line polarizer and polarization switch in the gate input are for testing purposes.

6.3.1 Components

Components used in the lab are divided into two groups: gate components and testing circuit components.

6.3.1.1 Gate components

In this section, we discuss in detail the components used to implement the gate.

6.3.1.1.1 Optical fiber

The Panda (Polarization-maintaining AND Attenuation-reducing) fiber is the fiber of choice because it is first and foremost a PM (Polarization Maintaining) fiber, see Figure 39 Single Mode (SM) fibers suffer from randomly introduced birefringence

by the manufacturing processes and bending of the cable. Therefore, the PM fiber is designed to introduce controlled strong birefringence to mandate the cable performance. Several PM fibers exist, including the Panda and Bo-Tie designs. The Panda has the advantages of low polarization crosstalk and low attenuation. The low polarization crosstalk is an important characteristic of the cable for our NAND, and other, gates. Polarization crosstalk, or cross polarization, takes place in the birefringent cable as the wave propagates through it. When the design of the Panda fiber is considered, we realize that a mechanical stress is introduced by the two stress-applying parts (SAPs) due to their being Boron doped and accordingly having a different thermal expansion coefficient than the cladding, Figure 39.

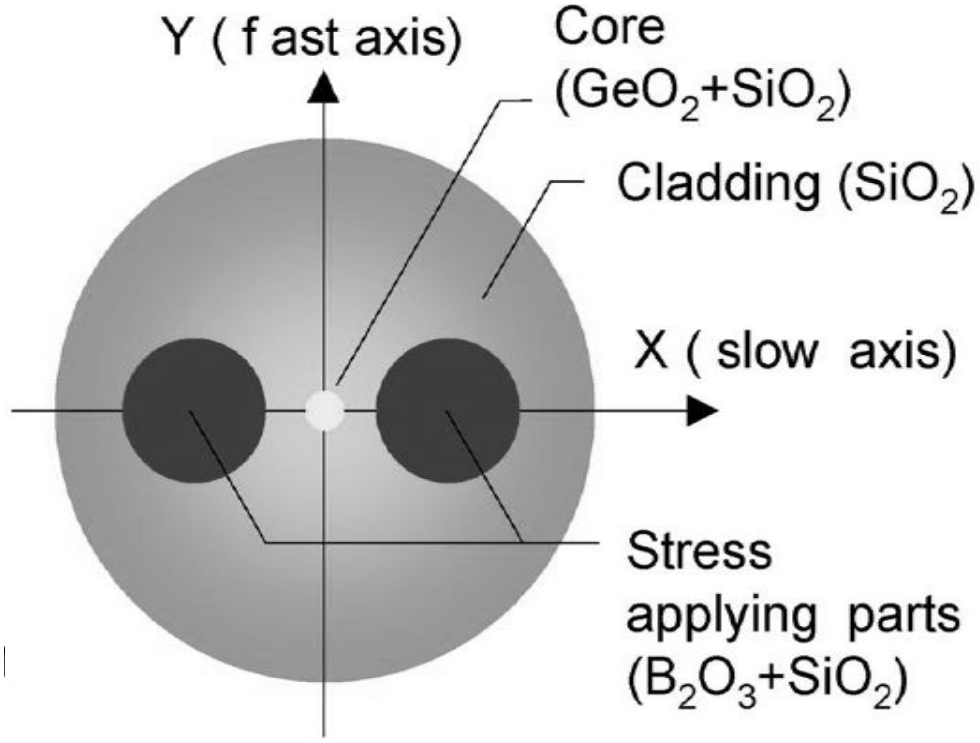

Figure 38 Stress-applying parts (SAP) are Boron doped, and have a higher thermal coefficient of expansion than the cladding. During the cooling of the drawing process, the SAP shrinks more than the cladding, and the introduced tensile stress remains in the core and produces a large stress birefringence.

The introduced stress induces a strong birefringence into the core due to the photo-elastic effect. The axis connecting the two SAPs becomes the slow axis (SA) and, accordingly, the perpendicular axis becomes the fast axis (FA), both are in the cross-section plane of the cable. When light propagates through the cable, its FA and SA components travel at two different speeds, due to the birefringence property of the cable. Therefore, depending on the length of the cable, the polarization of the output beam is determined. Polarization crosstalk is a non-desirable phenomenon where the two wave components interact together. If only one component of the wave, either FA or SA, is introduced into the cable the other component shows up as the wave propagates through the cable. The Panda cable is selected because of 1) its low polarization crosstalk we just discussed and 2) its low attenuation. Because the exit wave polarization depends on the cable length, we decided to use the vertical and horizontal logic representation of binary logic, see Chapters 2 and 3 [15, 29]. That leads to only one component traveling the cable parallel to the SA or FA. In addition, as the slow axis is the better controlled axis in the cable, we chose to have only components parallel to the SA to travel through the cable, be it the vertical (logic 1: L1) or the horizontal (logic 0: L0) component: one per cable.

6.3.1.1.2 Polarization beam splitter

The polarization beam splitter (PBS) is used in the gate architecture at the input of the gate to direct the input signal, being L0 or L1, to the proper corresponding branch, Figure 38. L0 is directed to the upper branch LZB, and L1 is directed to the lower branch LOB. Figure 40 shows a schematic of the PBS. Its common port fiber is PM, its insertion loss is 0.4 dB, its extinction ratio is 22 dB, its return loss is 50 dB, its

power handling is 500 mW, and its port 1 fiber type is PM Panda. Therefore, it is clear that this PBS has a low insertion loss, a low back reflection, and a high extinction ratio. The slow axis is aligned to port 3 of the PM Panda.

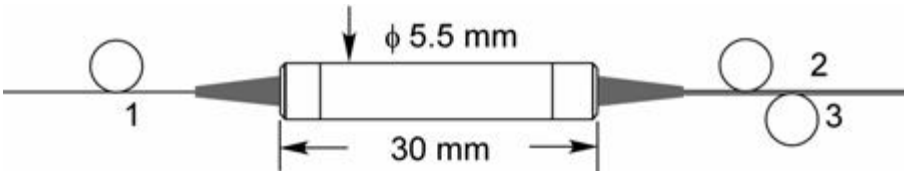

Figure 39 Schematic of the Polarization Beam Splitter (PBS).

6.3.1.1.3 Beam combiner

The beam combiner used is a polarization maintaining fiber coupler that combines the laser signals from 2 PM input fibers into a single PM output fiber. It is used in the construction of the NAND gate to combine the output signals of the LZB and LOB into one output signal. Remember that either LZB or LOB is active at a time, and not both. The polarization maintaining coupler (PMC) used has a maximum insertion loss of 0.7 dB, a maximum uniformity of 0.6 dB, a minimum extinction ratio of 20 dB, a split ratio of 50%, a return loss of 50 dB, an optical power handling of 300 mW, and a PM Panda fiber type. It has the same dimensions of the PBS shown schematically in Figure 40. As the PBS, it has a low insertion loss, a low back reflection, and a high extinction ratio.

6.3.1.1.4 Polarization switch

The polarization switch (PSW) used in the construction of the NAND gate is a PM to PM switch that rotates the polarization state of the input 90^{o}: equivalent to a 180^{o} relative phase shift [15, 29]. Therefore, if the input signal to the switch is L0, the output signal becomes L1, and vice versa. It has a polarization rotation of $90^{o} \pm 0.5^{o}$, an insertion loss of < 0.5 dB, a return loss > 55 dB, a switching current of < 130 mA, a switching voltage of 3.5 – 5 V, a latching current of ~ 80 mA, a latching voltage of 2 – 3 V, a switching time of 100 s, and an extinction ratio of > 18 dB. Figure 41 shows the dimensions of the switch. The polarization switch has no moving parts and a low insertion loss.

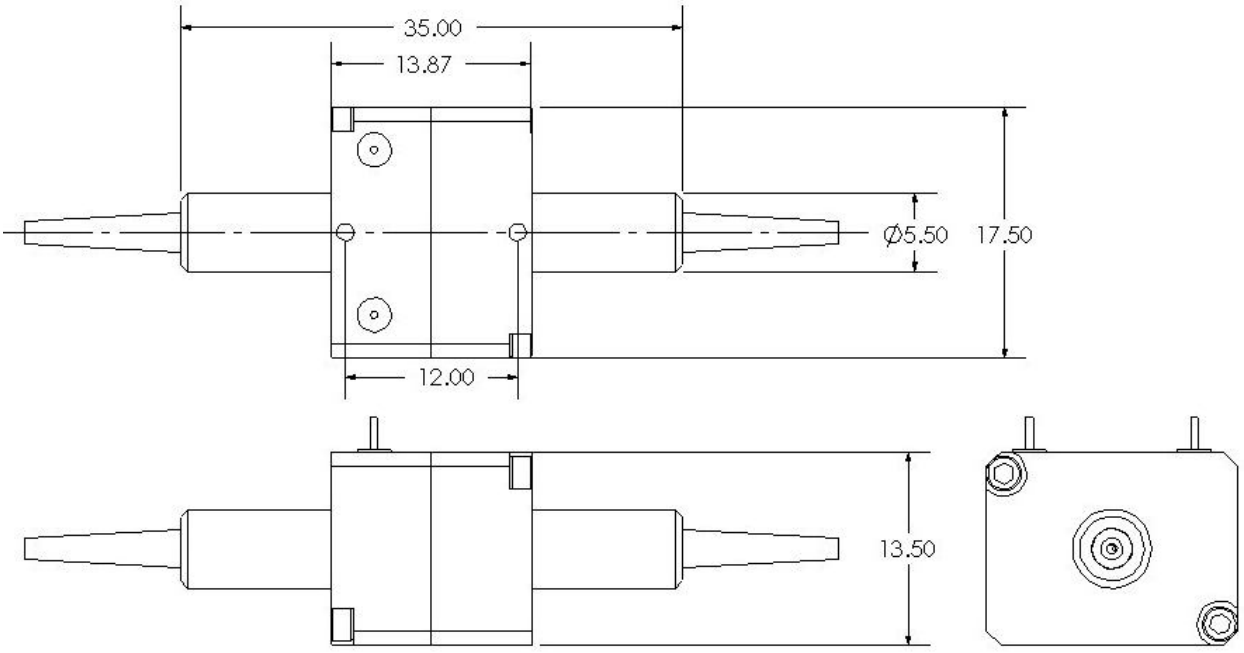

Figure 40 Schematic of the Polarization switch.

6.3.1.2 Testing circuit

The testing circuit includes extra components added to the NAND gate to control the input signal and test the gate under different input signals. Four components are used, a laser source, a polarizer, a polarization switch, and a power meter.

6.3.1.2.1 Laser source

The laser source used is a 1550 nm one with a linearly polarized output beam. Because the angle of polarization of the beam is not known, a polarizer is used to align the input beam with the slow axis of the testing polarization switch. The fiber connecting the laser source to the input polarizer is single mode (SM).

6.3.1.2.2 Polarizer

An in-line SM to PM polarizer (SM-PM POL) is used to effect the polarization of the laser input signal parallel to the input slow axis (SA) of the PSW. The used in-line polarizer has an insertion loss of 0.3 dB, a minimum extinction ratio of 28 dB, a return loss of 55 dB, an optical power handling of 300 mW, and a Fujikura PM Panda fiber. Figure 42 shows the dimensions of this in-line polarizer.

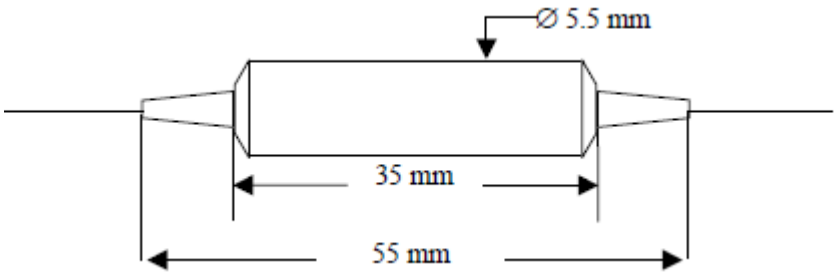

Figure 41 Schematic of the In-line polarizer

6.3.1.2.3 Polarization switch

The PSW output is aligned with the SA of the input PBS of the NAND gate when the electrical input signal is -5 V: representing L0. The output is aligned with the FA of the output PM fiber when the electrical input signal is + 5V: representing L1. Therefore, the input electrical signal controls the logic input to the gate represented by the polarization of the laser beam.

6.3.1.2.4 Power meter

A power meter is used to measure the polarization of the output signal of the gate: the output of the PMC. A polarizer is used at the power-meter input to cross the gate output beam, therefore measuring its polarization angle.

6.3.2 Structure

The NAND gate is structured as shown in Figure 38 . The following subsections discuss the structure of the gate and the testing circuit.

6.3.2.1 Gate

The gate is structured by connecting the input PBS to the PMC by a PM Panda cable comprising the LZB, and to the PSW by a PM Panda cable comprising the first section of the LOB. We effected a 90^{o} cross splice in the LOB to replace the 180^{o} retarder, shown in Figure 14 . Therefore, we eliminated one component and accordingly reduced the cost of manufacturing. The second section of the LOB is a PM Panda cable connecting the output of the PSW to the second input of the PMC. The optical input to the gate is the input to the PBS, and the optical output of the gate is the output of the PMC. The electrical input to the gate, which is the second input to the gate, is the electrical control signal to the PSW.

6.3.2.2 Testing circuit

The testing circuit is constructed by connecting the SM-PM in-line polarizer to the input of the testing PSW. The output of the testing PSW is then connected to the input of the gate PBS. On the output side of the gate, the output laser beam is crossed by a polarizer that is followed by a power meter. In the next subsection we discuss the cross splicing of the PM Panda cables and port connections of the PBS, PSW, and PMC of the gate itself.

6.3.3 Construction and implementation

All PM Panda cables used in the gate construction are regularly spliced, except the LZB cable. The LZB cable is 90^{o} cross spliced to do away with the 180^{o} retarder. For the PBS: the output signal on Port 1 slow axis is the LZB signal, the output signal on Port 2 slow axis is the LOB signal going to the PSW, and the input signal to the PBS is either aligned with the SA or the FA, representing the two logical input states to the gate. The output of the gate PSW is along the FA when its input control signal is -5 V, and is along the SA when its input control signal is +5 V. This voltage-axis relation is required for the NAND gate. On the other hand, the control signal inputs to the testing PSW are such that its output is along the SA when the control signal is -5 V, and is along the FA when the control signal is +5 V. The polarization of the input to the testing PSW is aligned to the SA of its Panda cable. That is ensured by the use of the input SM-PM polarizer. Note that the PMC requires both SA and FA active.

6.4 Experimental Measurements

Table 24 gives the experimental measurements obtained in the lab on operation of the implemented NAND gate. Note that the results represent the truth table of a NAND gate, where: - 5 V is L0, + 5 V is L1, slow-axis polarized light is L0, and fast-axis polarized light is L1. From the results of Table 24 , it is clear that the error in the gate operation is minute: between 0.2 and 0.3^{o}. When the manufacturing of such a gate is put into production techniques, such an error is easily driven to a much lesser value than 0.001^{o}. Such a number is well established in manufacturing of polarization components used in commercially available ellipsometers, with 0.0001^{o} available upon customer request. Table 24 is obtained by using a power meter at the output of the gate, preceded by a rotatable polarizer to extinguish the output beam, thus determining the polarization angle of the linearly polarized output beam.

Table 24 Experimental results for operation of the implemented NAND gate. PSW1 and PSW2 are the testing and gate polarization switches, respectively, α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents a NAND truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	α (^{o})	Axis
- 5	- 5	89.3	Fast
- 5	+ 5	89.2	Fast
+ 5	- 5	89.2	Fast
+ 5	+ 5	0.23	Slow

6.5 OR, AND, NOR, and the Universal Gate

The implemented gate can be operated as an OR gate. Its operational truth table can be simply changed to that of the OR gate by properly manipulating the control inputs of the two PSWs. By reversing the two control inputs to both PSWs, the gate functions as an OR gate. That can be simply achieved by an inverter connected to the control input of the PSWs.

The implemented gate can simply be converted to an AND gate by introducing a 90^{o} cross splice into the output fiber. The gate now performs as an AND gate. The NOR gate can be simply obtained from the implemented gate by introducing a 90^{o} cross splice into the output fiber in addition to properly manipulating the control inputs of the two PSWs, as we just discussed.

The Universal gate can be simply implemented by replacing the 90^{o} cross splice in the LZB with a second PSW. Table 16 shows the operational states of those two PSWs.

A different construction of the global gate can be simply implemented by adding a second PSW at the NAND gate output. This way, we can have any of the gates by simply inverting the input and/or the output as required [41].

6.6 Closing Remarks

We discussed in details the engineering, construction, and implementation of an optical polarization NAND gate using the introduced Orthoparallel Logic (OPL) architecture. The gate is implemented using the fiber optics technology. Commercially available components and well developed industrial techniques are used. The

experimental gate performance in the laboratory is reported, which is exactly as designed. A minute error is recorded, which is easily removable by properly designing and optimizing dedicated manufacturing processes. A discussion of how to operate the gate as other binary logic gates is presented, and proposed minor changes to the gate construction to function as a Universal gate is also discussed. A Universal gate is defined as one that can be operated as any of the known binary logic gates in a real time environment.

CHAPTER VII

RECONFIGURABLE ARCHITECTURE AND THE UNIVERSAL GATE

In this section we discuss the design, construction and testing of the Universal Gate. Due to the fact that the Rail Road architecture presented in previous chapters relies on the path of the light to perform consecutive computations, the system lends itself automatically to be reconfigurable. With the use of a simple controlled switch and a polarization beamsplitter, the light can be forced to one of two branches containing different circuitry. The optical nature of the architecture not only allows for reconfigurability but also for reversibility, and multiple wavelength operation. The following sections examine the Universal gate, illustrating the versatility and advantages of having controlled reconfigurable hardware architecture.

7.1 Introduction

Reconfigurable computing is based on transferring some of the software flexibility to the hardware it is running on. The idea is to use hardware to run compute intensive parts, including repetitive computations, to harness the speed associated with hardware use. On the other hand, reconfiguration execution in itself is a slow process that counters the speeding up effect of use of the hardware. Properly optimized, a reconfigurable computing system can be real fast. In some cases, it can be 500-time

faster than an optimized software running on a general purpose computer, with an FPGA clock 40-time slower than that of the computer [42].

Reconfigurable hardware is based on reconfigurable memory arrays, and a look up table (LUT). Connections are selected to configure a certain gate. And gates are connected to configure a certain digital device. Two main memory technologies are used: flash and SRAM. That is field programmable gate array (FPGA), in which reconfiguration is done by the user, hence field programmable. Prior devices were factory configured. Three programming technologies are used today: static memory programming technology, flash programming technology, and anti-fuse programming technology. The anti –fuse programming technology has the major drawback of not being able to reprogram the device. The device can only be programmed once using this technology. It has the major advantage of being secure, since the design info is transmitted only once [43].

Most of today's devices use processor blocks to connect and reconnect using connector blocks [44-48]. We know of no products that reconfigure the gates themselves, as switching a NAND to a NOR, or vice versa, using semiconductor technology: a universal gate. There exist some attempts at adding other than transistor devices to achieve a universal gate, and most are using threshold logic and gates [49-54]. Reconfiguring the gates themselves, in addition to their connections, saves a lot of time which is consumed in building the gates through interconnections of memory arrays and in using LUTs: on both levels of software and hardware. In addition, it positively controls the system architecture. This is the ultimate reconfigurability providing flexibility and non-ASIC (non-Application Specific Integrated Circuit)-like

characteristics. It saves time and does not penalize flexibility. Such designs, when exist, improve on the dynamic properties of FPGA, leading to true dynamic structures where hardware is changed in real time depending on the compute problem being dealt with. Coupled with the fact that our optical gates are much faster than semiconductor gates, it leads to unprecedented speeds of reconfigurable computing.

7.2 Design

In this section, we introduce a universal gate, which follows the same design architecture as the standard gate designs we discussed Chapter 3. Here we use the Orthoparallel gate architecture and two switches to design the Universal gate. Two designs are possible. The first design includes the two switches in the two branches, one in each branch. The second design includes one switch in one of the two branches, and the second switch at the output of the gate.

Figure 43 shows the first design, where a switch exists in each branch. Combining the design with Table 25 previously introduced in Chapter 3 one can clearly see the operation of the Universal gate. For example the table shows that for an AND gate the zero branch requires no switches while the one branch requires a reversed switch. That can be easily achieved by connecting PS1 to a fixed low (-5V) which would cause the switch to have no polarization difference between the input and the output. While the operation of PS2 can be easily altered by simply switching its positive and negative terminal connections resulting in the desired operation.

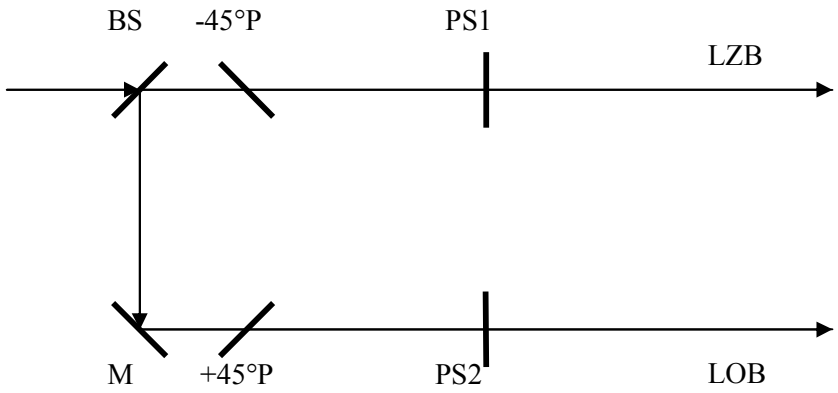

Figure 42 The Universal gate.

Table 25 Collective table of the polarization switches PS1 and PS2 for the Universal gate of Figure 43. L0/L1 are the two states of the PS corresponding to the logic zero L0 and logic one L1 states.

	AND	NAND	OR	NOR	XOR	XNOR
PS1 (L0/L1)		180	0/180	180/0	0/180	180/0
PS2 (L0/L1)	180/0	0/180		180	0/180	180/0

Another example would be the NOR operation, as one can see in the table, the zero branch of the NOR gate requires a reversed switch while the one branch requires a fixed 180 degrees shift. The PS1 would only require the reversal of its positive and negative terminals, while PS2 has to be set to a fixed high (+5V) to achieve the desired operation. Finally, the XOR operation only requires the terminals of PS1 and PS2 to be connected in parallel.

7.3 Implementation

The actual implementation of the Universal gate uses a second design. Instead of having the two switches one in each branch, we use one switch in the one branch, a

90^o cross splice in the zero branch, and a second switch at the output, after the beam collector as can be seen in Figure 44. The operation and the table are easily developed to represent the implemented gate as we discuss in the next section, this design is only used to optimize the fiber implementation of the gate.

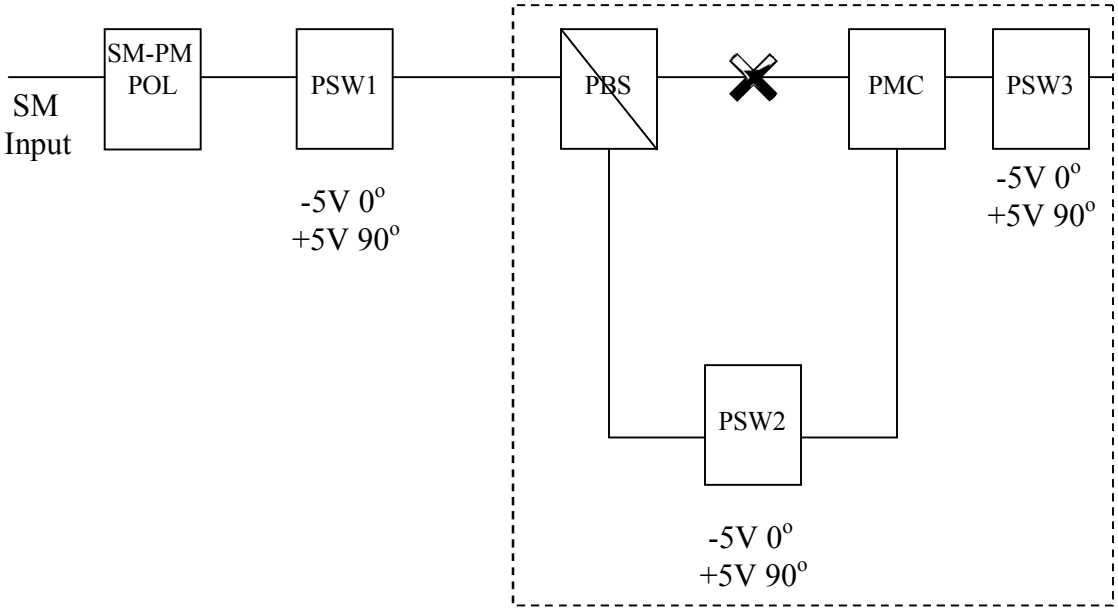

Figure 43 Universal gate: inside the dashed box. The in-line polarizer and polarization switch in the gate input are for testing purposes.

Table 26 Collective table of the polarization switches PSW1 PSW3, and PSW3 for the implemented Universal gate of Figure 44. L0/L1 are the two states of the PS corresponding to the logic zero L0 and logic one L1 states.

	AND	NAND	OR	NOR	XOR	XNOR
PSW1 (L0/L1)	0/180	0/180	180/0	180/0	0/180	0/180
PSW2 (L0/L1)	0/180	0/180	180/0	180/0	180	180
PSW3 (L0/L1)	180	0	0	180	180/0	0/180

7.4 Performance and Testing

The following tables demonstrate the various gate operations of the Universal gate and give the experimental measurements obtained in the lab on operation of the implemented Universal gate. Note that the results represent the truth table of the corresponding gate, where: - 5 V is L0, + 5 V is L1, slow-axis polarized light is L0, and fast-axis polarized light is L1.The following tables are obtained by using a power meter at the output of the gate, preceded by a rotatable polarizer to extinguish the output beam, thus determining the polarization angle of the linearly polarized output beam.

Table 27 Experimental results for operation of the implemented Universal gate as a NAND gate. PSW1 and PSW2 are the two testing and gate polarization switches, respectively, PSW3 is the functionality control switch (set to -5 V to produce the NAND function), α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents a NAND truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	PSW3 (V)	α (^{o})	Axis
- 5	- 5	-5	89.3	Fast
- 5	+ 5	-5	89.2	Fast
+ 5	- 5	-5	89.2	Fast
+ 5	+ 5	-5	0.23	Slow

Table 28 Experimental results for operation of the implemented Universal gate as an AND gate. PSW1 and PSW2 are the two testing and gate polarization switches, respectively, PSW3 is the functionality control switch (set to +5 V) to produce the AND function), α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents an AND truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	PSW3 (V)	α (^{o})	Axis
- 5	- 5	+5	0.41	Slow
- 5	+ 5	+5	0.62	Slow
+ 5	- 5	+5	0.62	Slow
+ 5	+ 5	+5	89.7	Fast

Table 29 Experimental results for operation of the implemented Universal gate as an OR gate. PSW1 and PSW2 are the two testing and gate polarization switches (where the both switch terminals are connected in reverse in this case), respectively, PSW3 is the functionality control switch (set to -5 V to produce the OR function), α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents an OR truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	PSW3 (V)	α (^{o})	Axis
- 5	- 5	-5	0.23	Slow
- 5	+ 5	-5	89.2	Fast
+ 5	- 5	-5	89.2	Fast
+ 5	+ 5	-5	89.3	Fast

Table 30 Experimental results for operation of the implemented Universal gate as a NOR gate. PSW1 and PSW2 are the two testing and gate polarization switches (where the both switch terminals are connected in reverse in this case), respectively, PSW3 is the functionality control switch (set to +5 V to produce the NOR function), α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents a NOR truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	PSW3 (V)	α (^{o})	Axis
- 5	- 5	+5	89.7	Fast
- 5	+ 5	+5	0.63	Slow
+ 5	- 5	+5	0.63	Slow
+ 5	+ 5	+5	0.42	Slow

Table 31 Experimental results for operation of the implemented Universal gate as an XOR gate. PSW1 and PSW3 are the two testing and gate polarization switches (where either the PSW1 or PSW3 switch terminals are connected in reverse in this case), respectively, PSW2 is the functionality control switch (set to +5 V to produce the XOR function), α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents an XOR truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	PSW3 (V)	α (^{o})	Axis
- 5	+ 5	- 5	0.32	Slow
- 5	+ 5	+ 5	89.43	Fast
+ 5	+ 5	- 5	89.43	Fast
+ 5	+ 5	+ 5	0.32	Slow

Table 32 Experimental results for operation of the implemented Universal gate as an XNOR gate. PSW1 and PSW3 are the two testing and gate polarization switches, respectively, PSW2 is the functionality control switch (set to +5 V to produce the XNOR function), α is the polarization angle of the output beam, and Axis is the direction of the linearly polarized output light. Obviously, the table represents an XNOR truth table where: - 5 V is L0, + 5 V is L1, slow axis polarized light is L0, and fast axis polarized light is L1.

PSW1 (V)	PSW2 (V)	PSW3 (V)	α (^{o})	Axis
- 5	+ 5	- 5	89.43	Fast
- 5	+ 5	+ 5	0.32	Slow
+ 5	+ 5	- 5	0.32	Slow
+ 5	+ 5	+5	89.43	Fast

The previous tables illustrate the operation of the Universal gate as NAND, AND, OR, NOR, XOR and XNOR only, but it is important to note that the Universal gate can be set via the 3 PSW switches to produce any of the 16 2-input logic gates.

CHAPTER VIII

COMPARISONS, FUTURE WORK, AND CONCLUSIONS

In this chapter we start with a detailed comparison between the proposed optical technologies and equivalent semiconductor counterparts. The comparison will entail speed, lag time, propagation delay, heat generation, design flexibility, along with other advantages and disadvantages accompanying optical systems. In this chapter we also discuss conclusions and future work, projects, and research direction.

8.1 Electro-Optical Rail Road Architecture

The speed of the proposed electro-optical Rail Road architecture explained in Chapters 3 and 4 is bound by two factors. The first of which is propagation delay (PD), the time taken by the optical beam to travel across the desired path from the input point to the output point. The second is the switching speed of the polarization switch, the lag time taken for the switch to produce the desired polarization effect. It is important to note that in such a system, the second factor or the switch lag (SL) only comes into effect once and is the same for any design. All the switches' electrical input comes in simultaneously to all switches in the system when the algorithm in Chapter 4 is used. That eliminates the domino effect of consecutive lag found in semiconductor designs. The two factors, combined, result in the total delay that is described by the following equation:

Total Delay RR= PD + SL (4)

While the propagation delay (PD) varies based on the size of the design, the switch lag (SL) is a constant for any design, no matter how complex it is.

In semiconductor-based gates, there are three different propagation delay times associated with a logic gate, t_{PLH} which is the time between a change in an input and a low to high change on the output, t_{PHL} which is time between a change in an input and a high to low change on the output, and finally t_{PD} which is the average propagation delay:

$$t_{PD}=(t_{PLH}+ t_{PHL})/2 \quad (5)$$

The following table gives the typical and maximum delay values for the semiconductor-based NAND gate [41]:

Table 33 Typical and maximum delay values for semiconductor-based NAND gate

	Typical	Maximum
t_{PLH}	9ns	15ns
t_{PHL}	10ns	15ns

From Table 33, we can calculate the typical t_{PD} to be 9.5 ns. In a design containing a number of N gates consecutively, the total delay of:

Total delay Si = N.(t_{PD}) = 9.5 N ns (6)

Furthermore, the RR total delay for the same design, assuming a chip length of 45nm would be:

$$\text{Total delay RR} = N.(45nm/c) + SL, \quad (7a)$$

$$= N.(1.5*10^{-16}) + SL, \quad (7b)$$

where c is the speed of light. By equating the total delay of both designs, we can solve for the equilibrium point at which the two systems would operate at the same speed.

$$N_{eq}.(1.5*10^{-16}) + SL = 9.5 * N_{eq} * 10^{-9}, \quad (8)$$

$$N_{eq} = .105 * SL * 10\text{^}9 \quad (9)$$

To further compare the performance of the 2 systems, we calculate the equilibrium point (Neq) for various switching speeds ranging from 100µs to 10ns. For each, we calculate the speed defined as the reciprocal of the total delay at the equilibrium point and at twice the equilibrium point for each of the architectures as can be seen in the following table:

Table 34 Comparison of Si and RR architectures operational frequency at different switching speeds

SL	Neq	Speed @ Neq	Si Speed @ 2Neq	RR Speed @ 2Neq
100u	10,500	10 kHz	5 kHz	10 kHz
1u	105	1 MHz	500 kHz	1 MHz
100n	10.5	10 MHz	5 MHz	10 MHz
10n	1.05	100 MHZ	50 MHZ	100 M HZ

From Table 34, it is clear that as N increases past the equilibrium point, the Si-based architecture becomes slower, while the RR architecture speed remains the same. The equilibrium point defines the point where both systems operate at the same speed. Below the equilibrium point, N_{eq}, the Si-based system is faster, while above the equilibrium point, N_{eq}, the RR speed is faster. It becomes transparent that, only for larger complex designs, the RR system is superior, since its speed remains relatively unaffected by the size.

Other advantages of the RR design include much lower heat generation and also the ability to design reconfigurable systems discussed in the previous chapter. The only drawback is that the system once built can not be easily modified, augmented, or cascaded while retaining the all-optical processing. On the other hand, with these advantages and the drawback discussed, the system lends itself automatically to specialized processors that require very fast response time, and perform complex operations, for example, a guidance chip for a missile, or a jet aircraft.

8.2 All-Optical Passive Architecture

Unlike the speed of the RR architecture, the all-optical passive (AOP) architecture is bound only by one factor: the propagation delay. Due to the fact that the system is totally passive and stationary, there is no additional switching lag involved, and the systems speed is only bound by propagation delay. The following equation shows the total delay for the architecture as a function of the chip length L, N and c:

$$\text{Total Delay AOP} = PD + 0 = N.(L/c) \quad (10)$$

Assuming a chip length of 45nm similar to the last section, we get :

Total Delay AOP =N.(45nm/c) = N.(1.5*10^-16) s (11)

While the total delay for Si remains

Total delay Si = N.(t_{PD}) = 9.5 N ns (12)

One can quickly deduce, by comparing the total delay for both systems, that when the chip size is fixed the AOP is seven orders of magnitude faster. If we equate the delays of both systems:

N.(L_{eq}/c)= 9.5 N ns, (13)

L_{eq} =9.5*c*10^{-9} (14a)

L_{eq} =2.85 m (14b)

This means that in order for the two gates to have the same speed, the length of the AOP gate must be 2.85 meters, which demonstrates the margin of speed difference and size requirement. Furthermore, the system produces less heat, is more resilient to jamming, can operate on multiple wave lengths simultaneously, and can operate in the reverse direction. To summarize, the system is superior to its silicon-based counterpart in every aspect considered in the comparison above, and its draw-backs are limited, if any.

8.3 Universal Reconfigurable Architecture

The universal reconfigurable gate contains either 2 or 3 switches and is similar to the RR architecture. The speed of the gate is bound by the same 2 factors as the RR, and the existence of the extra switch does not affect the speed, since all switches act simultaneously resulting in the same delay. Accordingly, Table 34 is also valid for the

comparison between the universal reconfigurable (UR) architecture and the silicon-based one.

The other aspect to consider is the reconfigurability. Most of the current reconfigurable architectures use interconnects to produce different hardware designs. Our universal reconfigurable gate, on the other hand, can change its operation based on the secondary input. The RR architecture lends itself automatically to rerouting of the signals, allowing different interconnects as explained in the previous chapter. The unique ability of controlling the operation of the gate based on the secondary input allows for many new possibilities that will be explored in future work.

8.4 Implementations and Applications

Four technologies are currently available to implement the proposed design of the polarization optical gates and devices: free space, fiber optics, photonic integrated circuits (PICs), and silicon photonics. Free space technology uses well established manufacturing tools to produce the needed optical components. Usually, the free space proof-of-concept prototypes are bulky and table-top mounted, with possibilities for miniaturization [28, 56, 57]. Fiber optics is a well established industry for telecommunications applications, with plenty of readily available off-the-shelf components that could be used for implementing our prototypes [58]. The components could be easily mounted on a board to yield a portable device. PICs and silicon photonics are two chip-size technologies that are well developed to mass produce sub-millimeter-, micro-, and nano-scale products [59, 60]. These two technologies are expensive and involve many industry-specific considerations, including process-flow

and mask design and manufacturing. The components used in our systems have all been previously implemented in the micro- and nano-scale including: a polarizer of a chip area of less than 20 μm by 20μm and an extinction ratio of 10^6 [61], a 40 μm-long retarder [62], a 10 μm-long PM waveguide [62], and a 10 μm-long polarization beamsplitter/combiner [63]. Several competing technologies are available with industrial scale production capabilities.

We can see that the experimental implementation of the suggested gates is straightforward with normal engineering considerations that depend on the technology to be used. If we consider implementation of any of the gates using silicon photonics, we see that all building blocks are available for prototyping, followed by manufacturing [59, 60]. That includes waveguides to maintain polarization [62]. In addition, a polarization gate is reported in the literature [64, 65].

The implemented fiber gates in the previous chapters were constructed using off-the-shelf components manufactured for the telecommunication industry. Naturally, for our applications, the components have high loss in intensity. Even though the latter does not affect the performance of the gate, it affects the maximum number of gates that can be cascaded. The beamsplitters and beam combiners have a 0.4 dB loss, the polarizer has a 0.3 dB loss, and the polarization switch loss is 0.4 dB. Adding all the losses in the circuit, we get an average loss of 1 dB. Assuming a receiver sensitivity RS of 28 dBm [66], we get the following number of maximum consecutive gates N based on the selected value of the source power SP [58]. For example, if the source power is 20 mW, the maximum number of cascaded gates N is 41. If the source power is 500 mW, the maximum number of cascaded gates N is 55. Based on the chosen

components, the maximum source power varies, affecting the practical number of maximum cascaded gates. The trade-off should be considered while the system is in design.

Table 35 Maximum number of gates N given the receiver sensitivity RS and source power SP

RS (dBm)	SP (mW)	N
-20	20	33
-20	500	47
-28	20	41
-28	500	55

Industrially, for the chip size gates, there are many parameters available to control the implementation to preserve the polarization fidelity of the signal. That is equally valid for devices and waveguides, in addition to controlling the path length itself. Obviously, tuning is critical and is done at the prototyping stage to reach a mask suitable for mass production. Also, material dispersion is one of the factors on which the wavelength bandwidth of the gate is determined. Keep in mind that, since only one branch of the gate is active at a time, no interference would take place within the gate. In general, this discussion on implementation holds for the other technologies, too.

For example, in a waveguide several parameters play an important role in determining its performance: dimensions, material homogeneity, and surface roughness as related to the wavelength [67]. In waveguide- and diffraction-based beamsplitters/beamcombiners, the same parameters apply, in addition to geometry.

Also, photodiodes are employed in receivers, where models are available for simulation in such applications [68]. In all cases, engineering trade-offs exist physically and due to the choice of technology and process flow. Taking those engineering trade-offs into account, we discuss in the following paragraph a few examples of applications of the new technology.

As one can clearly see, many applications of our new technology presented in the previous chapters are obviously directly related to its advantages, such as virtually no heat generated, resilience to jamming, and speed, to name a few. For example, when the radar signals are DSP processed using FPGAs, heat generated is a big limiting problem. Our technology would provide an elegant solution of deep reconfigurability to the gate level and virtually no heat generated, in addition to a welcomed higher processing speed. Another example of great importance in the military field is providing resilience to jamming as a solution to the current electromagnetic bomb problem where microprocessors are killed (totally disabled) using a very strong electromagnetic wave. Since light waves travel in insulators such as glass, the external electromagnetic wave would have no inductive effects on the light wave inside. Accordingly, jamming devices are rendered ineffective using our technology. A third example is to solve the optical network bottleneck problem faced by the telecommunications industry, where at every node within the network optical-electrical-optical (O-E-O) conversions take place. That drastically reduces the overall speed of the network. Our new technology provides the solution of processing the optical signal in the optical domain itself, doing away with the need for the O-E-O conversions. Also, an added element of speed is due to the fact that our optical

processor itself would be much faster than the microprocessors used in the electrical domain. The three examples mentioned in this paragraph are only representative, and many others do exist.

8.5 Future Work

Due to the fact that the proposed architectures and gates are very novel and revolutionary in nature, the future work is nearly endless. For example, it may include 1) the reconfigurability discussed in the last section, 2) the creation of multi wavelength WDM based devices that can utilize the full ability of such a technology, 3) the engineering of fast specialized processors, 4) the design and engineering of memory cells, and 5) putting the designs on a chip. These are some ideas and directions that the future work can move in, and the current markets are in dire need for all.

8.6 Conclusions

A new polarization-based digital binary representation is introduced. The representation is used to create two architectures. The first is the RR electro-optical architecture. A standardized algorithm that eliminates all electrical connects inside the system is also presented and discussed along with various designs and examples [55]. The second architecture is an all-optical passive system that is only bound by the speed of light. Various designs and examples are discussed. Also, the universal reconfigurable gate is presented and discussed. Such a gate is capable of changing its operation based on the second input.

Experimental verification of the Rail Road architecture is conducted and laboratory measured performance is reported. Various comparisons are performed

between the proposed technologies and the silicon-based counterpart, illustrating the advantages and disadvantages of using either. Finally, we conclude that the proposed architectures perform as designed and can be implemented in various applications utilizing their advantages such as speed, low heat generation, EMI resilience, and reconfigurability.

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