DEVELOPMENT OF A MODULAR PLATFORM FOR EMBEDDED CONTROL SYSTEMS LABORATORY COURSEWORK

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DEVELOPMENT OF A MODULAR PLATFORM FOR EMBEDDED CONTROL SYSTEMS LABORATORY COURSEWORK

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To the past and future students in ECE 4550

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NOMENCLATURE

BOM	Bill of Materials
JTAG	A serial interface used to program & debug a microcontroller
I/O	Input/Output
Motherboard	The portion of the system upon which the microprocessor resides
Daughtercard	A modular hardware element that interfaces with the motherboard
F28335	A TI C2000-series microcontroller, the TMS320F28335
ADCINxy	Analog to Digital Converter, input xy

SUMMARY

A new hardware system for the ECE 4550 Control System Design lab is proposed. The current hardware is examined and its shortcomings are documented. Design guidelines for the new system are put forth and interfaces between hardware elements are defined. Four hardware elements are developed: a motherboard, an I/O daughtercard, a DC motor driver daughtercard, and an AC motor driver daughtercard. Each of these systems is examined in depth from a design decision standpoint as well as from the standpoint of the design guidelines promulgated earlier. Technical limitations for each system are disclosed and examined in detail.

CHAPTER 1

INTRODUCTION

In this chapter, the environment in which the proposed hardware system will be used will be examined. Specific attention is paid to the laboratory curriculum of the ECE 4550 course and the role of the hardware system within the ECE 4550 curriculum.

The ECE 4550 Course & Lab

ECE 4550, Control System Design, is a relatively new course. It was begun as ECE 4884 in Spring semester 2011, with Dr. David Taylor as instructor. The course is a lab elective, and as such comprises 3 lecture hours and 3 lab hours per week. The focus of the lectures is on the design of state-space control systems, especially observer-based integral control systems and including application to motor drives, both DC and AC. The lab portion has three primary goals: to teach students to properly utilize the TI C2000 microprocessor family – and specifically the TMS320F28335 microprocessor, to teach interrupt-driven code architecture, and to teach the implementation of state-space control systems similar to those explained in the lecture. As this thesis focuses on the development of lab equipment, we will examine the lab structure in more depth. Table 1.1, below, shows the lab curriculum for the Spring 2012 semester, grouped by concept.

Table 1.1 Conceptual groupings for the Spring 2012 ECE 4550 lab curriculum.

Week	Lab Focus
1	Re-learning the C language
2	Programming the F28335 microprocessor
3-6	Interrupts and peripherals
7-8	DC motor control
9-10	AC motor control

Setting aside the first week, which is a review of the C programming language and requires no hardware support, we find four categories of labs: first, a basic programming lab that teaches students how to compile and run code on the F28335 microcontroller; second, a series of labs that teach how to use the F28335's hardware to effectively write controls programs; third, two labs that focus on the control of DC motors, and fourth, two labs that focus on the control of AC motors. (Additional labs may be developed around more advanced plants, but those labs have not yet been defined and are thus not listed here.) It follows, therefore, that there must exist hardware to support student learning in all four of these lab categories; furthermore, the hardware should be flexible enough to support any further developments or changes in the course curriculum.

The Role of Educational Hardware in ECE 4550

ECE 4550, which by nature is an applied laboratory, requires specific hardware to meet its educational goals. The hardware in 4550 must support all four categories of labs, but it must do so in a way that is transparent enough for students to be able to link the underlying control theory concepts taught in the lecture to the implementations performed in the lab. This leads us to the following definition of the hardware goals for ECE 4550: *The hardware in question must support learning how to program the F28335; the hardware must support learning about the peripherals and interrupts on the F28335; the hardware must support driving a reasonable-sized DC motor plant in a closed-loop feedback system; the hardware must support driving a reasonable-sized AC motor plant in a closed-loop system; the hardware must support all of these objectives in a transparent, testable, teachable, and flexible manner.* The development of hardware that meets these criteria is the focus of this thesis.

CHAPTER 2

DESIGN PRINCIPLES, SYSTEM ARCHITECTURE, AND INTERFACES

This chapter will focus on three things. First, it will examine the guiding principles chosen to inform the system design. Second, it will give a brief description of the core system architecture. Third, it will detail the three main interface sets that are used in the architecture.

Design Principles

The hardware development for this thesis was guided by three core principles. The first was *transparency*. Transparency, in this context, means that as many signals as possible should be testable from well-defined system test points (usually 100-mil headers). Transparency is the overriding key design principle in this work because the ultimate goal of the system is to teach students practical implementations; this goal requires that students be able to see the effects of their work in a real setting.

The second core principle for the hardware design is *flexibility*. This reflects the necessity of updating the lab curriculum to meet a changing academic and professional environment. While one set of exercises may be the focus one semester, the next semester may require a different set; similarly, plants may change or systems may be updated. Furthermore, the platform in question may be used for research or for other activities that the designer did not originally anticipate. Flexibility must be accomplished both at the hardware level, where the systems developed should support the maximum possible flexibility without altering the hardware systems, and at the interface level, where well-defined and complete interfaces should allow other researchers to easily and quickly develop additional hardware that works within the systemic context.

The third core principle for the hardware design is *ease of use*. Laboratory time is precious, both for the instructor and the student. Current solutions being used in the lab today have shown that, even if the hardware platforms are flexible and transparent, if they are not easy to assemble and maintain in a lab context, the overhead of time lost outweighs many gains in having the hardware. Thus, the system must have a minimum of connections; it should be easy to assemble correctly and difficult to assemble incorrectly; and it should be usable without need to reference manuals, datasheets, or other texts whenever possible.

Core System Architecture

The architecture that was developed to meet these needs is comprised of three classes of components; while the specifics of each implementation will be examined at length in Chapter 3, we will examine each briefly here in order to motivate the discussion of the interfaces in question. The first class of component is the controlCARD. A controlCARD is a Texas Instruments component which houses the F28335 chip, signal conditioning, and power management circuits on a DIMM-100 form factor card. The controlCARD has been an integral part of the ECE 4550 course from the beginning, and thus was chosen as the microprocessor element for the new hardware design.

The second class of component is the motherboard. The motherboard has five purposes: first, it must provide a stable interconnection between the controlCARD and the daughterboard; second, it must provide the students with a standard analog input interface that will function with the lab arbitrary waveform generators; third, it must provide space for the communications interfaces and bring those signals into the controlCARD; fourth, it must provide access to test points for standard signals; and fifth, it must provide power to standard system components.

The third class of component is the daughtercard. A daughtercard's purpose is to contain the correct power electronics drivers to translate controlCARD signals into

waveforms that can actuate a given plant or set of plants. The specific implementation of each daughtercard will be plant-specific (for instance, one would not develop a high-current AC daughtercard with parts designed for low-current DC applications) but the core principle is the same.

The overall system architecture can be seen in Figure 2.1 below.

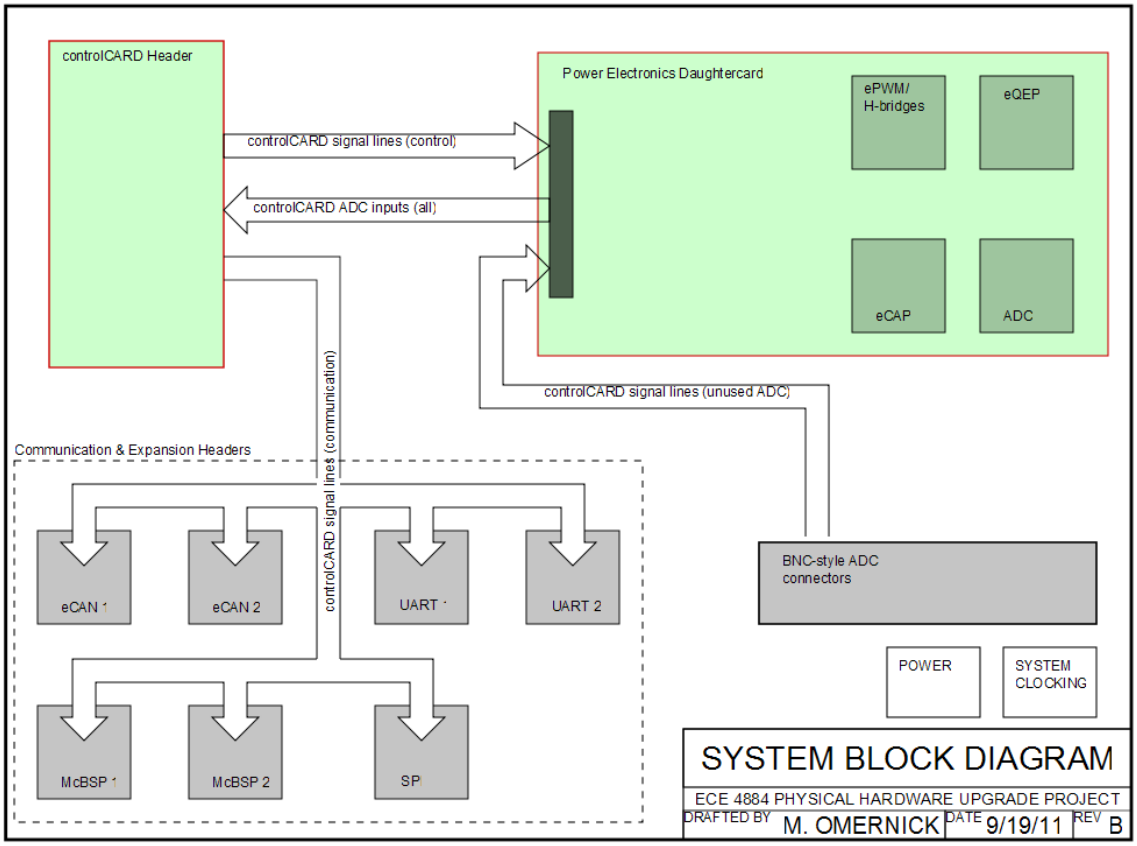

Figure 2.1: Architectural Block Diagram

This diagram demonstrates most of the interfaces required for the project, and thus motivates the next sections of this chapter. Observe that the Power Electronics Daughtercard, on the upper right, must receive the controlCARD signal lines relevant to control (that is, the signal lines which are used to generate waveforms that alter the output of power electronics). In addition, the Power Electronics Daughtercard must provide the

controlCARD with all of the ADC inputs, but that some of the ADC inputs must come from ADC connectors not on the daughtercard (and thus on the motherboard). These two requirements will define the daughtercard interface.

Also, observe that there is a selection of Communication & Expansion Headers which take the controlCARD signal input lines that are relevant for communication. These headers are designed to take advantage of the standard interface peripherals present on the F28335; however, to do so, they must each have a physical header with a defined interface. The interfaces for all of these communication ports will be examined in the later portion of this chapter.

One final element that does not exist on the block diagram, but bears mentioning, is the link between the controlCARD header and the student computer. This link is necessary for both programming and debug. For this project, an industry standard protocol (JTAG) was used; the specific JTAG interface is also documented later in this chapter.

Interface 1: Daughtercard Interface

The heart of this hardware system is the daughtercard/motherboard combination. This combination allows for flexibility in choosing the power electronics required to meet a goal, but maintains ease-of-use and transparency by requiring as little change as possible in the system when altering the power electronics. The interface between the motherboard and daughtercard, then, is the most critical aspect of the system, and deserves special attention.

The motherboard/daughtercard interface consists of two separate connectors, one for digital signals and one for analog signals. The motherboard holds the male connectors, which are sleeved to prevent damage to the pins, and the daughtercard is equipped with mating female connectors.

The digital connector is a 2x20 header with pins at 50 mil spacing; the male part used is a TE Connectivity 5-104068-4 and the corresponding female connector is a TE Connectivity 5-104078-2. This connector carries digital data as well as providing +3.3V and +5.0V power rails and the system's signal ground. The connector signal layout is in Table 2.1 below. Signal names are given prefaced with a number; this number represents the GPIO pin that the signal emanates from (thus, 00 EPWM1A is an EPWM 1A signal generated on GPIO pin 00). Some signals are postfixed with a –B; these are communications signals which are generated on the same line as one of the control signals. Thus, if the daughtercard designer does not need to use those control signals, the communications signals will be passed through and be usable. If, however, the design of the daughtercard requires the use of the control signals that are on those lines, these lines will not be usable for communications purposes (and will likely be left floating or pulled to ground, depending on implementation).

Table 2.1: Daughtercard Digital Header Pinout

1	21 EQEPB-1	25 EQEPB-2	
	20 EQEPA-1	24 EQEPA-2	
	23 EQEPI-1	27 EQEPS-2	
	22 EQEPS-1	26 EQEPI-2	
	MCLKX-A-B	GND	
	3V3	5V0	
	3V3	5V0	
	MFSX-A-B	GND	
	MDX-A-B	11 EPWM6B	
	MDR-A-B	10 EPWM6A	
	GND	09 EPWM5B	
	34 ECAP1	08 EPWM5A	
	48 ECAP5	07 EPWM4B	
	49 ECAP6	06 EPWM4A	
	GND	05 EPWM3B	
	I2CSCL-B	04 EPWM3A	
	33 I2CSCL	03 EPWM2B	
	GND	02 EPWM2A	
	I2CSDA-B	01 EPWM1B	
	32 I2CSDA	00 EPWM1A	40

The analog connector is a 2x15 header with pins at 50 mil spacing; the male part used is a TE Connectivity 5-104068-3 and the corresponding female component is a TE Connectivity 5-104078-4. This connector carries analog data and provides a link to the analog ground plane as well. It should be noted that the analog connection has both inputs and outputs – the motherboard was designed with six BNC analog inputs and two potentiometers. These signals are passed into the connector, and the connector provides 16 analog outputs – it is up to the daughtercard designer how he or she wishes to connect the inputs and outputs (and if he or she wishes to simply ignore them). However, the inputs were designed to be hooked up to certain outputs, and this is reflected in the nomenclature used in the diagram below. In the diagram, the alphanumeric digraph represents the ADC channel (so A0 represents the ADC input A0), a –I represents an input line (that is, a line which has a signal already generated before it reaches the board) and a –O represents an output line (that is, a line where the signal must be generated on the daughtercard. The pinout for the analog header may be found in Table 2.2 below.

Table 2.2: Daughtercard Analog Header Pinout

1	B0-O	B0-I	
	A0-O	AGND	
	B1-O	B1-I	
	A1-O	AGND	
	B2-O	B2-I	
	A2-O	AGND	
	B3-O	B3-I	
	A3-O	AGND	
	B4-O	B4-I	
	A4-O	AGND	
	B5-O	B5-I	
	A5-O	AGND	
	B6-O	B6-I	
	A6-O	A7-O	
	B7-O	B7-I	30

It should also be observed that the analog and digital headers have a specific orientation and spacing with respect to one another; this is specific to the motherboard implementation and is thus discussed further in Chapter 3.

Interface 2: Communication Interfaces

One of the major areas of improvement in this design is the improved accessibility of the communication peripheral interfaces. This adds an entire new dimension of flexibility and modularity to the design. They are grouped together in one section because they share a common form factor and purpose; each subsection will detail a specific interface. It should be noted that I have used the Texas Instruments naming convention for signal lines; these names may or may not conform to industry standard nomenclature.

All communications interfaces on the motherboard are accessible via male 100 mil headers. These headers are sleeved to protect the pins inside and keyed, but simple 100 mil female headers are perfectly suitable for accessing the signals. It should be noted that some communication lines are multiplexed with other communications lines or with control signal lines; these conflicts are spelled out in each subsection as needed.

Communication Interface 1: SCI (UART)

There are three available UARTs on the motherboard. (TI uses the term Serial Communication Interface (SCI) to refer to a UART; I will follow that convention from here on.) The SCI headers are 1x5 and provide both power and ground, as shown below.

Table 2.3: SCI/UART connector pinout

SCITX	GND	GND	SCIRX	3V3
1				

It should be noted that the SCI-A peripheral conflicts with the 4-position switch on the motherboard. If the 4-position switch is being used, no data will be transmitted through SCI-A. In addition, the SCI-B peripheral shares communication lines with the SPI peripheral, making the two mutually exclusive.

Communication Interface 2: CAN

There are two available CAN connectors on the motherboard. The CAN headers are 1x3 and provide only ground (no power) as shown below.

Table 2.4: CAN connector pinout

CANTX	GND	CANRX
1		

It should be noted that the CAN-B peripheral shares communication lines with the SPI peripheral. Because of this, use of the CAN-B peripheral and the SPI peripheral are mutually exclusive.

Communication Interface 3: SPI

There is one available SPI connector on the motherboard. The SPI header is 1x6 and provides both power and ground, as shown below.

Table 2.5: SPI connector pinout

SPISOMI	CLK	SPISIMO	SPISTE_N	GND	3V3
1					

It should be noted that the SPI peripheral shares pins with two other communications peripherals: SCI-B and CAN-B. When the SPI is in use, neither of those two peripherals may be used; similarly, if either of those peripherals is being used, the SPI peripheral will not receive data.

Communication Interface 4: I2C

There is one available I2C (nominally I^2C but written I2C in most documents) connector on the motherboard. The I2C connector is 1x4 and provides both power and ground, as shown below. Note, however, that it does NOT provide pull-up resistors – implementing these is the duty of the expansion designer.

Table 2.6: I2C connector pinout

I2CSDA	I2CSCL	GND	3V3
1			

It should be noted that the I2C peripheral shares GPIO lines with the ADCSOC signals. Because of this, the I2C lines are routed through the daughtercard connector. This means that the availability of the I2C peripheral is dependent on the design of the daughtercard currently in use.

Communication Interface 5: McBSP (Multichannel Buffered Serial Port)

There are two McBSP connectors available on the motherboard. (McBSP is a customizable serial port that can be used to emulate various other serial connectors.) The McBSP connector is 1x8 and provides both power and ground, as shown below.

Table 2.7: McBSP connector pinout

MCLKRA	MCLKXA	MFSRA	MDRA	MDXA	MFSXA	GND	3V3
1							

It should be noted that the McBSP-A peripheral shares several data lines with the eQEP-1 peripheral. Because of this, the McBSP-A lines are routed through the daughtercard connector. This means that the availability of the McBSP-A lines are dependent on the design of the daughtercard currently in use. It should also be noted that, since the

quadrature encoder is a critical part of most control systems, it will be a rare daughtercard that passes the McBSP-A lines through instead of using them for the eQEP-1 peripheral.

Interface 3: TI 14-Pin JTAG Interface

The final interface to examine is the JTAG interface that will be used on the board. JTAG is an industry standard protocol for debugging and programming microprocessors; it was for this reason that a JTAG interface was included on the motherboard. While JTAG is an industry standard, JTAG connectors are emphatically not standardized; it is often easier to select JTAG hardware, then design your connector based around that hardware's form factor, than it is to strive for any sort of flexibility. The JTAG hardware used in the 4550 lab is the XDS100v2 JTAG emulator; it uses the 14-pin JTAG header configuration found below [1].

Table 2.8: TI 14-pin JTAG Interface Connector Pinout

1	TMS	TRSTn	
	TDI	TDIS	
	VTRef	KEY	
	TDO	GND	
	RTCK	GND	
	TCK	GND	
	EMU0	EMU1	14

In this specific implementation, VTRef is pulled up to 3.3V through a 100 ohm resistor, and RTCK and TCK are connected to the TCK line going to the F28335. It should also be noted that pin 6, KEY, represents a filled hole on the female JTAG connector. This pin must be removed before the male connector can be used.

This interface was implemented using a 2x7 shrouded 100 mil male header, Molex part number 2514-6002UB.

CHAPTER 3

DEVELOPED HARDWARE

Chapter 3 will go into detail on the specific implementation of the architecture described in Chapter 2. Each of the four developed boards will be examined, subsystem by subsystem, to allow a greater understanding of the design choices made during implementation. In addition, any electrical limitations of each system will be clarified and documented here.

Card 1: Motherboard

The motherboard, shown below in layout view, is primarily an interconnect fabric and power supply.

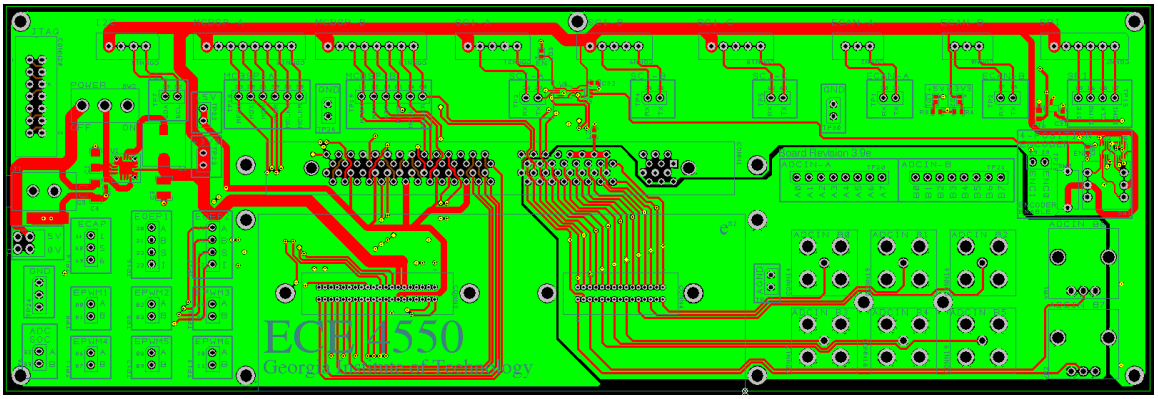

Figure 3.1: Motherboard (all layers)

It is implemented on 4-layer technology with a ground plane layer and 3 routing layers, to ease the burden of routing so many signals. Minimum space width is 7 mils and minimum hole size is 15 mils; this, along with the area, qualifies it for the Advanced Circuits $66 4-layer board promotion [2]. There are 5 major subsystems within the motherboard: the power subsystem, the communication ports, the digital test points and

switch, the analog inputs and testpoints, the daughtercard connection, and the controlCARD/JTAG interface. Each will be examined in turn.

Power

One of the primary duties of the motherboard is to provide power to all the connected subsystems. This can be challenging, as many different voltages and current levels are required. After examining the system requirements, it was decided to have an external +5.0V supply (a 'wall wart'), specified at 500 mA, which would be used to provide a +5.0V rail within the design and to provide the input to a buck converter circuit capable of outputting +3.3V. The external +5.0V supply can be connected either through a barrel jack (2.1mm ID, 5.5mm OD) or through a pair of screw terminals. This flexibility allows the motherboard to be mounted on a mobile system, using the screw terminals to accept power from the mobile system's internal power source, or to use common 120V AC line power and a step-down transformer to power the motherboard on a lab bench.

The 3.3V line is supplied by a Texas Instruments TPS62111 highly integrated buck converter. While the datasheet specs this part to up to 1A output, the limitations of the wall wart must be taken into account as well. Allowing 250 mA for the controlCARD and daughtercard circuitry, and assuming a 90% efficiency, there is approximately 340 mA available on the 3.3V rail before the power supply saturates. Note, of course, that should an application require more power on the 3.3V rail, a more powerful input supply would allow for increased output up to the thermal limitations of the TPS62111 package.

Communication Ports

Another of the primary duties of the motherboard is to route communications lines to the output connectors along the top of the board. These output connectors have

had their interfaces defined in Chapter 2, above, so that will not be revisited here; instead, implementation specifics will be examined.

One of the unfortunate limitations of the controlCARD is the lack of options when choosing which GPIO pin will carry which signal. Because of this, there are several conflicts between the communications ports. While it is possible to use any one port in isolation, certain port combinations will not be possible. These limitations are described below.

Table 3.1 Communications Module Conflicts

Mutually Exclusive Modules		
Module	Conflict 1	Conflict 2
eCAN-A		
eCAN-B	SPI-A	
SPI-A	eCAN-B	SCI-B
SCI-A	4-POS SW.	
SCI-B	SPI-A	
SCI-C		
ADCSOC	I2C	
I2C	ADCSOC	
McBSP-A	EQEP1	
McBSP-B		

Note that there are three modules – eCAN-A, SCI-C and McBSP-B – that are always available.

Most of the time, the conflicts are handled in software – either a GPIO pin is assigned to SPI or it is assigned to CAN-B, for instance – but there are a few cases where there are physical forbiddances involved. These three cases are McBSP-A, I2C, and SCI-A. The first two cases occur because their conflicts are against control line signals; this means that these signals have been routed through the daughtercard connector. Depending on the daughtercard design, the user may not have the option to utilize these

signals for communications purposes, as the daughtercard designer selects whether to use these signals on the daughtercard or to connect them through to the communication ports in question. The case of SCI-A vs. the 4-position switch is slightly different; since both of these elements exist on the motherboard, a switch has been provided to toggle between the two. Labeled ENCODER ENABLE, when it is active the SCI-A input and output lines are tri-stated; when it is low, the 4-position switch lines are tri-stated. This allows either element to function without interference.

It should also be observed that each communications port is fully testable, with test points grouped and labeled as described in the next section, 'Digital Test Points & Switch'.

Digital Test Points & Switch

One of the key improvements in this hardware platform over extant hardware solutions is the increase in digital test points. These test points exist in the lower left corner of the motherboard, and are clustered for easy access and location. Most critically, all of the test points are clearly grouped and labeled for maximal ease of use. As shown in the figure below, test points are grouped into functional categories, and are labeled both with the name of the signal (below, for instance, you can see the EQEP1-A, -B, -S, and –I signals) as well as the GPIO pin number associated with that signal. Labeling with both will assist in flexibility, as it frees daughtercard designers to use control signals as GPIO lines with no loss of clarity in test.

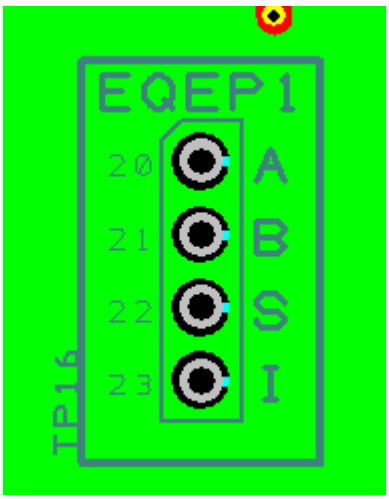

Figure 3.2: Grouped and labeled test point for Quadrature Encoder 1.

Testable signal groupings are: eCAP (1, 5, and 6), eQEP1 (all), eQEP2 (all), ADCSOC (A and B), ePWM1 (A and B), ePWM2 (A and B), ePWM3 (A and B), ePWM4 (A and B), ePWM5 (A and B), and ePWM6 (A and B). In addition, all communication port lines are testable; these test points are located near each communication header, but follow the same grouping and labeling guidelines as discussed above.

In addition to the bevy of digital test points available, there is a digital 4-position switch implemented on the motherboard. This is intended to allow daughtercard designers to ignore the need for basic stateful digital inputs and focus on the development of the power electronic circuitry. The 4-position switch is connected to pins 29 and 28 through a series of OR gates that result in the truth table below.

Table 3.2: 4-Position Switch Outputs

Switch Position	GPIO 29	GPIO 28
0	0	0
1	0	1
2	1	0
3	1	1

It should be noted that when the switch is transitioning from 1 to 2, the output transitions from 1 to 3 to 2. This is a fundamental defect in the switch manufacture; to overcome it, the switch should be sampled very slowly.

Analog Inputs and Testpoints

The motherboard also handles a selection of analog signals. To the front and left of the controlCARD socket is the analog section of the board. This section has a segregated ground plane, which is joined to signal ground through a ferrite bead (100 ohm at 100 MHz). Within this section are six analog input jacks, two potentiometers, and sixteen analog testpoints.

The six analog input jacks are labeled ADCINB0-ADCINB5; note, however, that this is merely a recommendation and it is possible to connect these inputs to other analog input pins on the F28335 by using the fact that all analog signals, including the ones that originate on the motherboard, pass through the analog input socket on the daughtercard. To avoid confusion, all ADCINBx signals should be connected directly through the daughtercard, as discussed in Chapter 2. The choice of BNC jacks for ADCINB0-B5 was motivated by the fact that BNC is a standard output for arbitrary waveform generators, including the ones we have in the ECE 4550 lab; thus, having BNC connectors eliminates the need for special adaptors.

The two potentiometers on the motherboard exist to provide a ready-made human actuated analog input. These potentiometers are labeled ADCINB6 and B7; they are also subject to the daughtercard design as it relates to the BNC input jacks. The potentiometers are fed from an ultra-precise 3.0V DC source, with the wiper attached to the ADC input of the F28335. This effectively allows a linear voltage ramp with respect to angular position of the potentiometer. Note that, since the internal voltage reference for the ADC is 3.0V, a 3.0V potentiometer top voltage will fit perfectly within the system.

There are also 16 analog testpoints (and an additional two points that allow connection of scope ground to analog ground instead of signal ground). Each testpoint is labeled in accordance with the rules described earlier in this chapter. It should be noted that the testpoint is situated between the analog daughtercard socket and the F28335 ADC input, so whatever is seen on the testpoint is precisely what is being measured by the ADC – the daughtercard design has no effect here.

Daughtercard Connection

The daughtercard connection is arguably one of the more important sections of the motherboard. The electrical interface definition was explored at length in Chapter 2; however, the physical constraints of the interface design as implemented on the motherboard are equally important. Because the interface requires two connectors, the relative spacing between them is critical to a daughtercard designer; furthermore, since the daughtercard is intended to sit atop the motherboard, there are limits to how far the daughtercard can extend in certain directions before it conflicts with other board elements like testpoints, the controlCARD, or the analog input jacks. The figure below represents an accurate mechanical drawing detailing these restrictions. Note that the size and orientation of the connectors is not represented; they are oriented horizontally with pin 1 in the upper right hand corner.

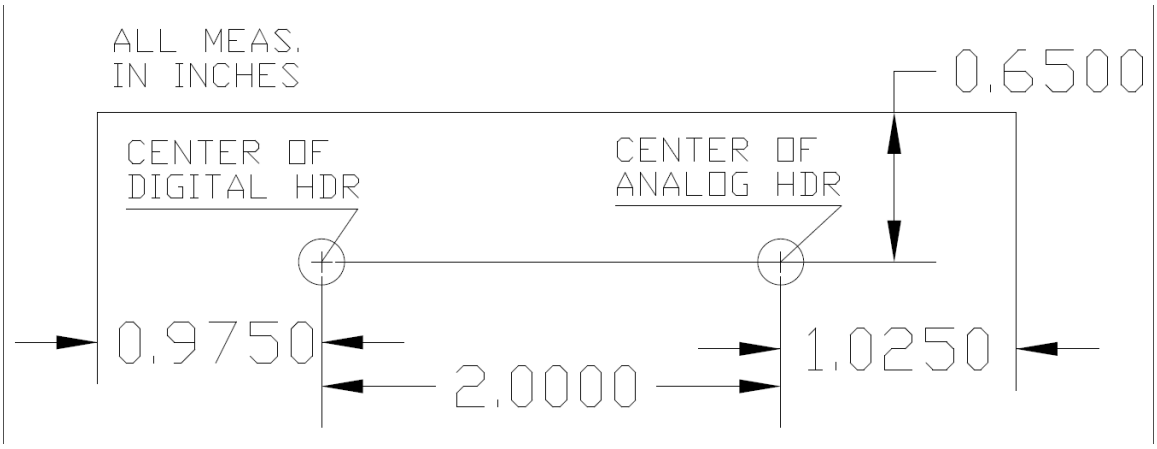

Fig. 3.3: Size limitations for daughtercard header interface.

ControlCARD/JTAG Interface

The final subsystem in the motherboard is the controlCARD connector and the JTAG interface. The JTAG interface has been described at length in chapter 2, and the implementation on the board is simply a connection line-to-line between the JTAG connector and the controlCARD, so it will not be mentioned further here. This section focuses instead on the implementation of the TI controlCARD interface.

The controlCARD interface was not mentioned as part of Chapter 2, as it is essentially irrelevant to anyone save the original system designer. However, it has some relevance to the system as a whole and is thus included here as part of the design decisions for the motherboard.

The controlCARD interface is based around the DIMM-100 form factor. This is a key drawback, as the Molex DIMM-100 connectors that the form factor specifies are no longer in production; the only way to purchase these connectors is through the TI web store. However, the choice to use the controlCARD as part of this system forces this form factor on the motherboard.

The controlCARD socket has 100 pins (as would be expected from the form factor); each of these pins has multiple uses. However, due to the constraining nature of physical implementation, each pin has had its functionality limited based on what precisely that pin is connected to on the PCB. Below is the pinout of the controlCARD connector.

Table 3.3: controlCARD Interface.

1	V33D-ISO	V33D-ISO	51
	NC	NC	
	NC	NC	
	NC	NC	
	NC	NC	
	GND_ISO	GND_ISO	
	ADCIN-B0	ADCIN-A0	
	AGND	AGND	
	ADCIN-B1	ADCIN-A1	
	AGND	AGND	
	ADCIN-B2	ADCIN-A2	
	AGND	AGND	
	ADCIN-B3	ADCIN-A3	
	AGND	AGND	
	ADCIN-B4	ADCIN-A4	
	NC	NC	
	ADCIN-B5	ADCIN-A5	
	58 MCLKR-A	59 MFSR-A	
	ADCIN-B6	ADCIN-A6	
	60 MCLKR-B	61 MFSR-B	
	ADCIN-B7	ADCIN-A7	
	62 SCIRX-C	63 SCITX-C	
	00 EPWM1A	01 EPWM1B	
	02 EPWM2A	03 EPWM2B	
	04 EPWM3A	05 EPWM3B	
	06 EPWM4A	07 EPWM4B	
	GND	+5V	
	08 EPWM5A	09 EPWM5B	
	10 EPWM6A	11 EPWM6B	
	48 ECAP5	49 ECAP6	
	NC	NC	
	NC	+5V	
	12 MDX-B	13 MDR-B	
	15 MFSX-B	14 MCLKX-B	
	24 EQEPA-2	25 EQEPB-2	
	26 EQEPI-2	27 EQEPS-2	
	GND	+5V	
	16 CANTX-B	17 CANRX-B	
	18 SCITX-B	19 SCIRX-B	
	20 EQEPA-1	21 EQEPB-1	
	22 EQEPS-1	23 EQEPI-1	
	NC	+5V	
	28 ENC0	29 ENC1	
	30 CANRX-A	31 CANTX-A	
	32 I2CSDA	33 I2CSCL	
	34 ECAP1	+5V	
	GND	TDI	
	TCK	TDO	
	TMS	TRSTn	
50	EMU1	EMU0	100

It should be noted that some of these lines are shared. The table below summarizes this sharing.

Table 3.4 Shared controlCARD Lines.

Shared Lines	
16 CANTX-B	SPISIMO
17 CANRX-B	SPISOMI
18 SCITX-B	SPICLK
19 SCIRX-B	SPISTE_n
32 I2CSDA	ADCSOC A
33 I2CSCL	ADCSOC B
20 EQEPA-1	MDX-A
21 EQEPB-1	MDR-A
22 EQEPS-1	MCLKX-A
23 EQEPI-1	MFSX-A
28 ENC0	SCITX-A
29 ENC1	SCIRX-A

Card 2: I/O Daughtercard

The first I/O daughtercard, shown below in layout view, is primarily a vehicle for learning basic microcontroller concepts.

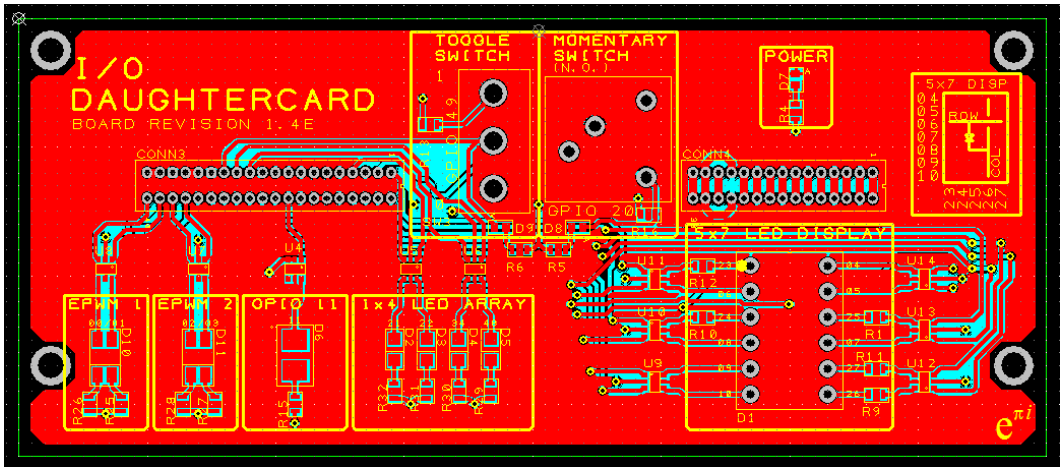

Figure 3.4: I/O Daughtercard (all layers)

It is implemented using a 2-layer process. The minimum space is 7 mils and the minimum hole is 16 mils. There are only two main components of the I/O daughtercard: the LED line drivers and the LEDs and switches.

LED Line Drivers

One of the key limitations of the F28335 as a microcontroller is the low availability of output current. Most F28335 output pins can drive no more than 3 mA. Because of this, any optoelectronic indicator that requires more than 3 mA to activate, like the LEDs used in this design, will require a buffer IC capable of sourcing or sinking more current than the F28335 itself. In this design, the Fairchild Semiconductor NC7WZ16P6X in a SC70 form factor was chosen. This IC is capable of sinking or sourcing up to 24 mA and is thus more than adequate for the task at hand.

It should be noted, however, that (like most buffers) the NC7WZ16 does not include any sort of internal pull resistors. Furthermore, if an input line is left to float, the NC7WZ16 will generate large amounts of noise, injecting it into the ground plane and causing problems with measurements. Because of this, any inputs to the NC7WZ16 that will not have deterministic states at all times should be pulled either up or down through relatively large-valued resistors. This can be seen on the EPWM1 and EPWM2 LED inputs on the I/O daughtercard.

LEDs and Switches

The sole function of the I/O Daughtercard is to provide a rich set of student-usable inputs and outputs for the first several labs. By having many inputs and outputs, labs will become less tedious, as novel outputs can be required each week. There are five different LED output arrays: the EPWM1 and EPWM2 bicolor LEDs, the GPIO 11 LED, the 1x4 LED array, and the 5x7 LED display.

The EPWM1 and 2 LEDs are identical in form and function and will thus be addressed together. These LEDs are bicolor (red/green) and thus are most useful when students are learning PWM – changing duty cycles on the 1A and 1B or 2A and 2B lines will provide a changed color on the LED, allowing students feedback without requiring a scope for duty cycle examination.

The GPIO 11 LED, a large red LED, is used in the first, most basic exercise: read a switch and light an LED. This LED is designed to be easy to find, as it is difficult enough for students to come to terms with MMR and GPIO concepts required to light the LED.

The 1x4 LED array consists of 4 individual green LEDs in a single line. This is intended to provide a way-forward for current lab exercises using the 1x4 LED array on the current hardware. It is especially useful in the context of counting from 0x0 to 0xF, as all these numbers can be displayed in binary on the array.

The 5x7 LED display is more complex and more challenging to use. It consists of 35 individual LEDs, arranged such that to light one LED, you must pull the row high and pull the column low. The purpose of the display is to provide a 2-dimensional LED array that can be used in conjunction with the two potentiometers to provide a motivating exercise in the ADC introduction lab. It should be noted, also, that the current-limiting scheme used on the 5x7 LED display is such that the more LEDs are lit in a single column, the dimmer each LED will become. This is a necessary hardware solution to the array's construction. If more complex patterns are desired, illuminating single dots quickly should provide a more-than-adequate solution.

Card 3: DC Motor Driver Daughtercard

The DC Motor Driver daughtercard, shown below alone, can drive up to two DC motors. It is implemented using a 2-layer process. The minimum space is 7 mils and the minimum hole is 16 mils. There are seven main components of the DC motor driver

daughtercard: the channel 1 motor driver, the channel 2 motor driver, the channel 1 current sense circuit, the channel 2 current sense circuit, the quadrature encoder inputs, the power switch, and the brake resistor circuitry; they will each be examined in turn.

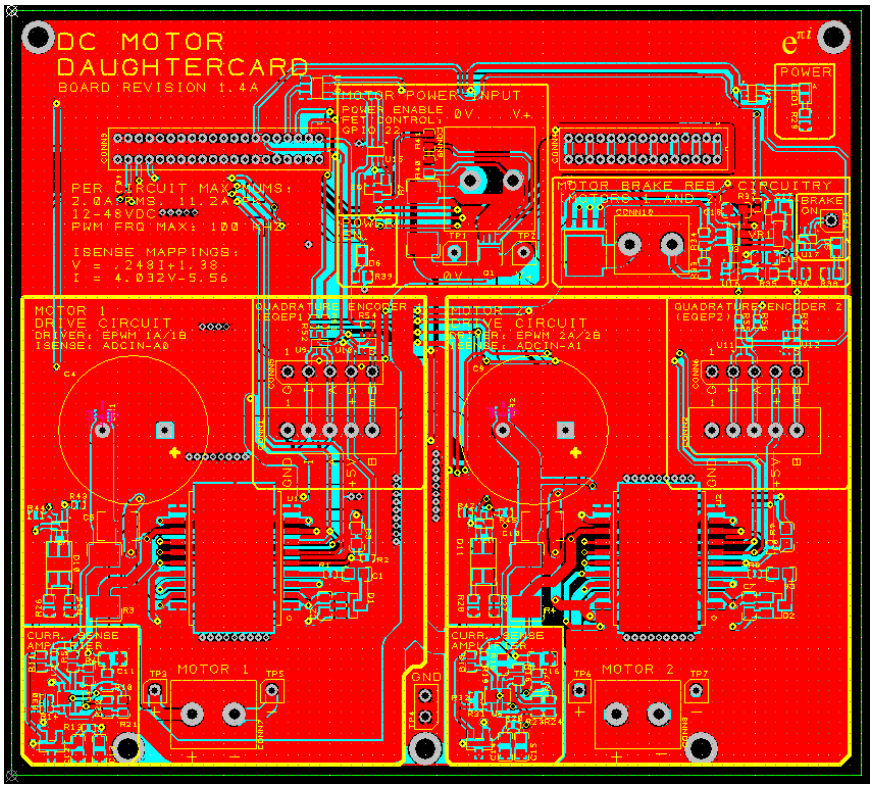

Figure 3.5: DC Motor Daughtercard (all layers)

The Channel 1 Motor Driver

The heart of the DC daughtercard is the motor driver circuitry. The channel 1 driver is implemented around a ST Microelectronics L6205 dual H-bridge IC in the PowerSO-20 package, connected with both H-bridges in parallel for better thermal characteristics. The implementation follows closely to the reference schematic in the L6205 datasheet, figure 15, and to the components recommended for the charge pump on page 8 of the datasheet [3]. One notable change is the substitution of a Fairchild Semiconductor MMBD7000 dual-diode in a SOT-23 package for the 1N4148s

recommended in the datasheet; the recommended diode was not available in such a small package, and empirical evidence indicates that the substitution is perfectly acceptable. Furthermore, pull-down resistors (4.7K) have been added to the PWM lines to reduce line driver noise in the circuit. If operation becomes problematic, these may be depopulated.

It should also be noted that, as part of the drive circuitry, a bicolor LED identical to the one on the GPIO daughtercard has been implemented. It is driven by the same lines (EPWM1A and 1B) and thus provides a bridge for students between the PWM concepts learned on the I/O Daughtercard and their application in motor-drive situations.

There are several limitations to this design. First, the motor driver circuit is fed by hard-wired EPWM1A and EPWM1B lines, which must be in an inverting configuration; it is not possible to change this. Second, the maximum supply line voltage (that is, the motor driver supply line voltage) is 48 VDC; there exists a small amount of room above this, but under no circumstances should the DC voltage rise above 50VDC for an extended time period. Third, there are limits on both the RMS and peak current values for the IC. The peak current is limited by the bond wires in the IC (and is thus absolute); it is 11.2 A max. The RMS current is restricted by the unit's thermal characteristics; while the unit is rated at a (conservative) 2.0A RMS, it may be possible to run the unit at higher RMS current values so long as the IC does not get too hot. (For a more complete discussion of thermal profiles, see [3].)

The Channel 2 Motor Driver

The channel 2 motor driver is schematically identical to the channel 1 motor driver, and the layout differs in minor senses only. Beyond the fact that the channel 2 driver is controlled by the EPWM2A and EPWM2B lines, the limitations are also identical.

The Channel 1 Current Sense

Current sensing is a critical part of motor control circuitry, and thus an analog current sensing circuit has been implemented for each motor driver channel on the DC motor driver daughtercard. The current sense resistor, a 20 milliohm, 1 watt 2512 surface mount part, generates a voltage during normal motor operation. This is used to drive the input of a Texas Instruments OPA2348, which has been biased to a virtual ground of .121 V using a precision (.1% or better) voltage divider off of a precision 3V reference (the TI REF3030AIDBZR). It should be noted that the ground of the resistive divider that makes up this virtual ground is tied to the low end of the resistor, providing superior noise rejection.

Using a standard inverting op-amp configuration with the .121 V virtual ground, the signal is amplified by -12.4x. However, in an effort to better expose the real current-voltage relationship, the amplified signal is fed through another op amp (the second op-amp in the dual-amp OPA2348 package), which has a gain of -1 and is biased at 1.5V virtual ground. This results in a final voltage-current relationship illustrated by the equations below.

Table 3.5: Current-Voltage Equations for DC Daughtercard

$$V = .248I + 1.38$$

$$I = 4.032V - 5.56$$

Critical to this current sensing circuit is the knowledge that the ADC input for the F28335 saturates at 0V and 3V. Thus, the maximum *senseable* current range is -5.56A to 6.536A. However, experiencing peaks above or below this range will not cause the op-amp to suffer; the current limits on the op amp inputs will be exceeded only after the drive IC has self-destructed from overcurrent.

The current sense circuit is hooked up to ADCINA0; like the drive channels, this is a hardwired element of the board design and may not be changed. Experiments on existing board prototypes show that this configuration is capable of sensing within 10 mA

at 2.2 amps of load. It is notable, too, that the error could have been a result of an inaccurate power supply current reading, as we do not have the tools to accurately read DC current flows in the lab in which this experiment was performed.

The Channel 2 Current Sense

The channel 2 current sense circuitry is schematically identical to the channel 1 motor driver, and the layout differs in minor senses only. Beyond the fact that the channel 2 sense circuit is hooked up to ADCINA1, the limitations are also identical.

The Quadrature Encoder Inputs

This daughtercard contains two quadrature encoder inputs. These inputs use the standard quadrature encoder interface, as seen in the table below.

Table 3.6: Quadrature Encoder Interface

GND	I	A	+5V	B
1				

It should be noted, however, that while this interface provides for an index line (I), it is only necessary for the encoder to provide the A and B lines for operation. Naturally, eliminating the index line will eliminate the index line's functionality, but the core system will still work.

Each quadrature encoder input contains two headers: a sleeved 1x5 100 mil header and an unsleeved 1x5 100 mil header. These headers share a 1:1 connection between pins. The motivation behind the second, unsleeved header is to enable additional lab equipment, like the external tachometer and radial angle sensor, to be connected to the system without the use of Y-cables or similar 'hacks'.

All three signal inputs, which are assumed to operate at +5V logic, must be stepped down to +3V3 logic before they can be interfaced with the F28335, since the

F28335's I/O pins cannot tolerate +5V logic levels. To accomplish this, a pair of NC7WZ16 buffers are used; these buffers can be powered by the 3.3V rail (and thus output 3.3V logic levels) while still accepting +5V logic levels on their inputs. However, the use of these buffers necessitates pull-down resistors on all encoder signal lines; these 4.7K resistors ensure that no noise is generated by floating high-impedance lines (for instance, if an encoder was not plugged in). It is also notable that, since the buffers are being driven by +3.3V logic, it would be possible to accept +3V3 logic level signals. However, the fact that the connector provides only +5V may require additional workarounds.

The power system for the quadrature encoders contains another subtlety to address. Because the additional encoder-based lab equipment used in 4550 (the external tachometer and angular distance sensor) can supply +5V when the equipment is attached to an encoder connector, it would be plausible to have the external equipment power the +5V rail, and thus the +3V3 rail and the rest of the system even if core power is turned off. To avoid this, the encoder power structure is segregated from core power by an ON Semiconductor MBRA210LT3 power diode, placed such that any power source connected to the encoder inputs cannot power the system. It should be noted, however, that the MBRA210LT3 causes a voltage drop of .26V at 100 mA and 25 degrees C; this is within 10%, but may cause problems if the encoder chosen requires very strict tolerancing on its supply lines. (The current encoders chosen do not show any problems with this voltage drop.)

The Power Switch

During preliminary testing of the DC driver daughtercards, it was observed that during programming the F28335's PWM lines enter into arbitrary states. If the motor driver is active, these arbitrary states are interpreted as H-bridge commands, resulting in spurious motor movements while the F28335 is in its programming phase. To avoid this

occurrence, a power switch circuit was implemented on the card. This circuit is comprised of a Vishay SI7113DN P-channel MOSFET across the positive (+VDD) motor power line, and a circuit to drive this FET. The SI7113DN was chosen for its low on-resistance of .134 ohms at 13.2 A. In order to drive the SI7113DN with a standard GPIO pin from the F28335, additional circuitry is required. The gate of the SI7113DN is tied to a resistive divider with a ratio of 1:0.7; this divider is then switched with a NXP Semiconductor BST82,215 N-channel MOSFET such that when the BST82's gate is driven high, VDD is placed across the resistive driver. It should be noted that, given the configuration, the maximum negative voltage between gate and source on the SI7113DN is -18V, well within the -20V limit of the component.

The BST82 N-FET is driven by a NC7WZ16 buffer which is in turn driven by an NC7ST04 single inverter. The inverter translates the 3.3V signals from the F28335 into 5V output signals, which are sufficient to drive the buffer and thus the BST82. The line that drives the power switch is GPIO 22; the circuitry must be active low as this line has an integrated pull-up resistor.

There are pads for a non-populated 2512 surface mount resistor, R7, on the top of the board. Because there was insufficient time to test the switch circuitry, the entire module may be bypassed by the removal of the SI7113DN (component Q1) and adding either a 2512 0-ohm resistor or simple wire between the open pads.

The Brake Resistor Circuitry

The DC daughtercard has 1,640 microfarads of total bulk capacitance on the motor drive rail. While this is more than sufficient to absorb regenerative braking transients from lower-voltage motors with low rotor inertias, high-voltage motors with large rotors will easily require some way to burn off additional power. Assuming that the supply in question is non-regenerative, this power must be burnt off in a brake resistor or else the voltage will rise to a point where the drive ICs will be damaged. This is a special

concern when operating at or near the 48V maximum, as the absolute maximum IC voltage of 60 V allows the capacitors to absorb only 1.063 J of energy before the drive ICs are damaged, compared to 2.47 J of energy when operating at 24VDC nominal. To protect the drive ICs, a brake resistor circuit is included in the design. The circuit does not contain the actual resistor – a resistive element capable of any reasonable absorption would not fit on the board – but instead contains a voltage sense circuit which activates a NXP BUK9Y30-75B,115 power FET. This FET shunts a screw terminal in parallel with the motor. This screw terminal should be connected to a resistor of suitable size and wattage for the application at hand.

The voltage sense circuit is based around a Texas Instruments OPA348AIDBVT single op-amp in a comparator configuration. The motor driver line voltage is run through a resistive divider and reduced to a ratio of 1:0.0586; this reduced voltage is then compared to a value generated by a precision 3.0V reference. The reference is slightly raised when the power FET is turned off, so in order to turn on the reduced motor line voltage must be above 3.117V, or more usefully the raw motor line voltage must be above 53.171V. However, once the FET is on the reference is no longer raised, and in order for the FET to turn off the reduced line voltage must be below 3.0V, that is, the raw motor voltage must be below 51.175V. This provides enough hysteresis to ensure that the FET will not rapidly cycle between on and off states.

The hysteresis in the voltage sense circuit is provided through an inverter and a resistive divider. The inverter input is tied to the comparator output, so when the comparator is off the inverter is outputting +5V, and when the comparator is on the inverter is outputting 0V. A resistive divider drops this voltage down to a usable level, and the output of this divider is used as the ground for the precision reference. While this approach does add some amount of noise to the precision reference's output, high-precision sensing is not a large concern in this circuit.

Card 4: AC Motor Driver Daughtercard

The AC Motor Driver daughtercard, shown below in layout view, can drive one three-phase AC motor in delta or floating-wye configuration.

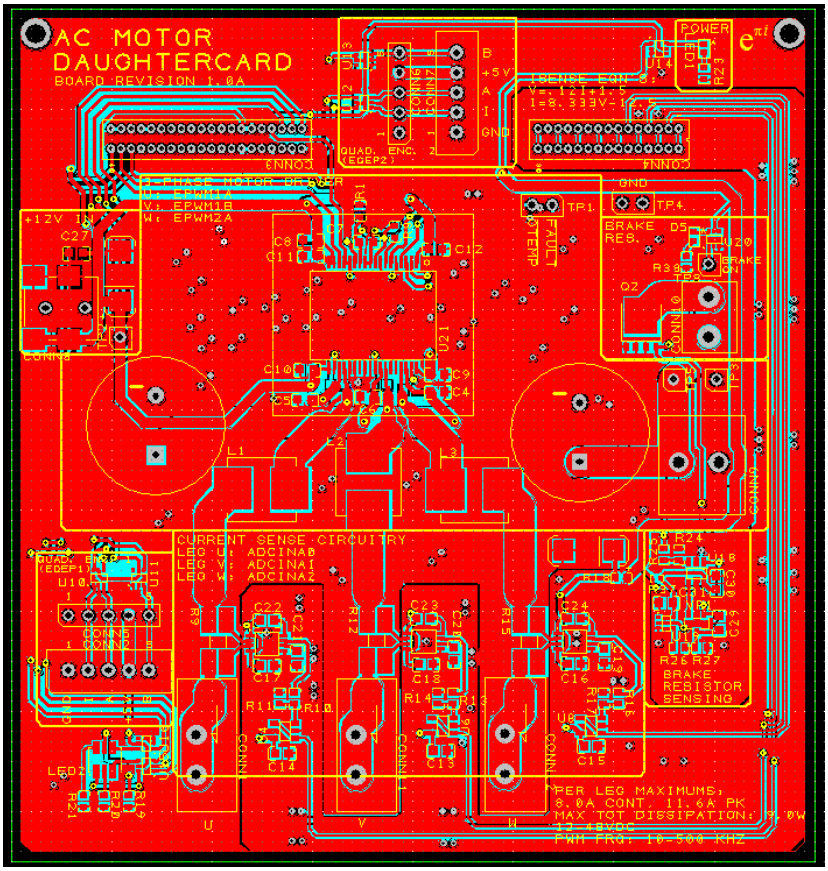

Figure 3.6: AC Motor Daughtercard (all layers)

It is implemented using a 2-layer process. The minimum space is 7 mils and the minimum hole is 16 mils. There are five main components of the AC motor driver daughtercard: the motor driver circuitry, the thermal management system, the current sense circuitry, the quadrature encoder circuitry, and the brake resistor circuitry. Each will be examined in turn.

The Motor Driver Circuitry

Like the DC driver card, the AC driver card is built around the motor driver circuitry. The AC driver card has only one drive circuit, due to space constraints. That circuit is implemented around a Texas Instruments DRV8332DDW 3-phase motor driver IC in a PowerPAD HSSOP package. The implementation on the AC motor driver daughtercard follows the reference implementation shown in the schematic in Figure 7 on page 14 of the DRV8312/8332 datasheet [4]. In the AC driver card implementation, chip channel PWMA, which is tied to the U output on the connector, is driven by EPWM1A; chip channel PWMB, which is tied to the V output on the connector, is driven by EPWM1B; chip channel PWMC, which is tied to the W output on the connector, is driven by EPWM2A; and the RESET_N lines for all three channels are tied together and driven by GPIO 22.

There are several areas of design choice in the reference schematic. These are the MODE pin selections, the overcurrent limit resistor selection, and the current limiting inductor value; each will be examined in turn. For the MODE pin selections, a review of the table "Mode Selection Pins" on page 3 of [4] reveals that M3 should always be 1 and M2 should always be 0; the M1 pin can be 1 to enable cycle-by-cycle current limiting and can be 0 to enable latching absolute current limiting. Because each method has advantages, the implementation contains pads to place a 0-ohm resistor such that the M1 pin is pulled high (for a 1) or low (for a 0). Only one resistor should be populated at a time. The default schematic population pulls M1 high, enabling cycle-by-cycle current limiting.

The overcurrent resistor must be chosen from the selection of values in Table 2 on page 12 of [4]. Because the absolute maximum value of surge current is 13A, the next lower surge value was chosen – 11.6A, which requires a 22K resistor. It should be noted that, with M1 set to cycle-by-cycle current limiting, this can effectively prevent current spikes caused by too-large eigenvalues; however, it does mask this problem from

students. If it was desirable to have students see that their eigenvalues were too high directly, it would be better to swap the M1 population option and have the chip go into overcurrent lock.

The current limiting inductors must follow the equation described in page 19 of [4], and reproduced below. Since the DRV8332 has a high current limit, these equations must be evaluated; since this is a broad-application lab setup, the evaluation must be at the worst-case of I_{ave} = 8A continuous current and VDD = 48V. This results in a L_{oc_min} of 2 microhenries.

Table 3.7: Current Limiting Inductor Equation.

$$L_{oc\_min} = \frac{VDD * (250 * 10^{-9})}{15 - I_{ave}}$$

While this is eminently achievable at low currents, the inductive element chosen must maintain an inductance above 2 microhenries at currents up to 15A without saturating. The Vishay-Dale IHLP-3232DZ-01 3.3 microhenry inductor meets all of these criteria in a relatively compact (~.320" square) shielded package.

The current limits on the power electronics are constrained in three ways. The first is the hard current limit specified by the resistor selected above. This resistor, which effectively limits surge currents to 11.6A, is a cycle-by-cycle peak current limitation. The second limitation is on maximum continuous current in each leg. This limit is due to internal chip heat limits and is specified at 8.0A. Under no circumstance should any leg continuously conduct more than 8 A, even if it is the only active leg on the IC. The final limit is due to the overall temperature rise in the package; this limit is a function of the thermal management system and will be examined in more depth there; here, we simply note that the absolute maximum power dissipation in the IC is 9.0 W, which will put the junction temperature at approximately 117 degrees C above ambient. Assuming ambient

is 25 degrees C, and allowing for some error in the thermal calculations, results in a T_j of 150 degrees C – the maximum allowable before thermal shutdown occurs. For reference, the R_{ds_on} of the internal power FETs is 80 milliohms.

An additional element of the motor driver circuitry is the existence of two pins, OTEMP_N and FAULT_N, that have been brought out to labeled test points on the motor driver board. These test points may be probed to determine failure modes of the IC, should the device cease to function when running a program. The specific meaning of each signal combination may be found in Table 1 of [4]. It should be noted that OTEMP_N is referred to as OTW_N in the datasheet; the name was changed on the silkscreen to better reflect its function.

The final element of the motor drive circuitry that deserves discussion is the 12V power rail. The DRV8312 requires an external 12V source, unlike the DC driver IC which is powered from the VDD rail internally. Creating 12V on the board presented a significant challenge due to the very wide range of the power supply rail (12-48V as spec'd, possibly reaching higher during regenerative current transients). Because of this, it was decided to generate the 12V supply off-board using a wall-mounted commercial buck converter (wall-wart) and feed it into the board via a power jack. This approach was not only simpler but also proved more cost-effective than attempting to generate 12V within the daughtercard. The wall mount converter specified can source 500 mA, which is more than sufficient to run the IC. It should also be noted that the jack for the 12V rail is of a different size than that for the 5V rail; this is to prevent dangerous misconnections. The jack was placed such that the power input should cause minimal interference with the test points on the motherboard.

The Thermal Management Solution

The DRV8332 requires an external thermal solution. This design uses a Cool Innovations 3-101015G pin-fin heatsink designed for natural convection cooling (0

LFM). The thermal resistance of this heatsink is 12.18 degrees C per watt. The heatsink is mechanically fastened to the board in order to improve thermal connectivity and prevent students from damaging the heatsink-IC connection by grasping the heatsink; in order to reduce noise, the heatsink is also grounded. The thermal junction between the IC and the heatsink is covered with Prolimatech PK1 thermal compound, with a thermal resistance of 0.017 degrees C per watt per square inch. The IC has a thermal slug of area 0.124 in^2; this gives a total thermal resistance for the compound layer of 0.0021 degrees C per watt. The IC itself has a thermal resistance junction-to-case of 0.9 degrees C per watt; summing the three resistances results in a theta junction-to-ambient of 13.0821 degrees C per watt. Assuming that the heatsink has a constant thermal resistance across temperature and assuming that the ambient air temperature is 25 degrees C results in a maximum dissipation of 9.555 W internal to the driver IC before the junction reaches 150 degrees C and the IC shuts down. The silking on the driver board specifies a 9.0W total dissipation, which is intentionally conservative.

It should be noted that both the high-side and low-side FETs in the DRV8332 have an R_{ds_on} of 80 milliohms, increasing linearly to 120 milliohms as T_j increases to 125 degrees C. Thus, the total power dissipated in the chip must be calculated as seen in the equation below.

Table 3.8: Power Dissipation in the DRV8332

$$P_{dis} = I_A^2 * R_{dson} + I_B^2 * R_{dson} + I_C^2 * R_{dson}$$

The Current Sense Circuitry

On the AC driver daughtercard, great care was taken to ensure precision current sensing; this will enable accurate sensorless AC motor control should the labs be brought in that direction. Each leg has its own sense circuit, and each sense circuit is identical

save for the ADC input to which it is attached. The first circuit, sensing leg U, is read by ADCINA0; the second, sensing leg V, is read by ADCINA1; the third, sensing leg W, is read by ADCINA2.

Each sensing circuit is comprised of three parts: a resistor, a high-precision differential amplifier and a drive buffer. The resistors are 1W Ohmite LVK24-series .01 ohm resistors with Kelvin (4-terminal) connections and 0.5% precision. To select the resistor, it was observed that a .01 ohm resistor would dissipate less than 1W at 8A continuous and that a .02 ohm resistor would dissipate less than 2W at 8A. However, the 2W/.02 ohm resistor was over $15/unit, so the 1W/.01 ohm resistor was selected.

The resistor is connected to a Linear Technology LT1999-20 differential amplifier, which offers 20 V/V amplification between its positive and negative terminals and is capable of handling up to 80V of common-mode DC. The output of the LT1999-20 is automatically centered around a 2.5V steady state due to the design of the IC, so the full sensing range of the amplifier/resistor combination is +/- 12.5A, which is outside the current limit of the motor driver IC.

The output of the device is fed into a precision resistive divider of ratio 1:0.6, effectively reducing the output swing from 0-5V to 0-3V, which is the range of the ADC on the F28335. However, to ensure that current draw on the ADC would not affect the readings, a Texas Instruments OPA348 op amp was placed in a unity-gain configuration between the resistive divider and the ADC input. Overall, the current-voltage relationship equations are as follows.

Table 3.9: Current-Voltage Equations for AC Daughtercard

$$V = .12I + 1.5$$

$$I = 8.333V - 12.5$$

It is also worth noting here that special care was taken to provide a low-noise sense circuit. Signal and analog grounds are fully segregated and switched power lines never cross analog ground – in fact, the connectors chosen were selected in order to ensure that the switched PWM output was output to wires before it crossed the analog ground plane.

The Quadrature Encoder Circuitry

The quadrature encoder circuitry is identical to the circuitry implemented on the DC driver daughtercard. Because of this, it will not be discussed further here save to note that despite having only one motor drive circuit, the card is equipped with two quadrature encoder inputs.

The Brake Resistor Circuitry

The AC daughtercard has 1,820 microfarads of total bulk capacitance on the motor drive rail. Like the DC card, however, additional regenerative dissipation may be needed if the circuit is being driven at or near 48V. To accomplish this, a brake resistor circuit identical to that of the DC card has been implemented; since it is identical in implementation, it will not be discussed further here.

CHAPTER 4

CONCLUSIONS

This thesis described a modular system of educational hardware to support the instruction in the ECE 4550 laboratory section. The hardware system, which is comprised of four separate PCB board designs, will meet the goals proposed in Chapter 1 of this document as follows.

Criterion 1: *The hardware in question must support learning how to program the F28335*. The base motherboard, with its JTAG connection, allows for programming the microprocessor alone; however, any daughtercards used will enhance the process of learning how to program the F28335.

Criterion 2: *The hardware must support learning about the peripherals and interrupts on the F28335*. This criterion is supported most closely by the I/O Daughtercard. The rich set of I/O options offered on this card allow a diversity of laboratory exercises that teach students how to use GPIO to get data into and out of the microcontroller, how to create and use an interrupt-based timing system, how to use the ADC, and how to use the PWM to generate arbitrary duty cycle waveforms.

Criterion 3: *The hardware must support driving a reasonable-sized DC motor plant in a closed-loop feedback system*. The DC motor daughtercard is designed to support this criterion. With a 2.0A constant-current rating from 12-48VDC, this card can drive a motor of up to 96W. The current DC motors used in the lab draw a mere 100 mA; the design of this card allows for a wide range of new DC plants to be introduced. In addition, the brake resistor circuitry allows for the driving of heavily loaded plants or plants with high rotor inertias. Finally, the dual-driver setup allows for the creation of systems that utilize the F28335 for dual-axis motor control investigations.

Criterion 4: *The hardware must support driving a reasonable-sized AC motor plant in a closed loop system*. The AC motor daughtercard was developed to support this criterion. With an internal dissipation of over 10W and the capability of handling 8A constant current or 11.6A peak current, the driver should be able to handle most lab-appropriate AC plants. Also, the AC motor driver IC's rich set of protective features – overtemperature and overcurrent cause shutdowns instead of damaging the IC – make the card uniquely suited for a laboratory environment. Finally, the precision current sensing hardware in the AC daughtercard allows exploration of sensorless control of AC systems.

Criterion 5: *The hardware must support all of these objectives in a transparent, testable, teachable, and flexible manner.* All of the designs in this system support transparency, testability, and teachability. Transparency is achieved by ensuring that all signal lines are testable, and that circuits are labeled on the silkscreen whenever possible. Circuits which exist to 'black-box' elements of the control process have been eliminated through design choices and part selection.

Testability has been designed into the fabric of the system from the ground up; the motherboard provides a testpoint-rich environment where students can observe any signal that exists in the system (save for those which exist only on the daughtercards).

Teachability is a consequence of the transparent, testable nature of the system; labs designed to motivate nearly any concept can be designed with ease, since any and every control signal going into or out of the microcontroller can be observed in a simple, standardized fashion. In addition, because the system is flexible, plant-specific control needs can be easily met by simply designing another daughtercard for the system.

Flexibility, the final goal, is clearly met by the creation and use of standard, modular interfaces. The system is not some massive, monolithic controls platform where all of the hardware investment is tied to a single plant or class of plants. If a lab setup needs to have its driver hardware swapped out, all that needs to happen is for the lab instructor to pop out the unneeded daughtercard and pop in the correct one. This

flexibility extends to design; by offering a standardized interface for controls, power, and analog signals, new power electronics suites can be developed quickly and at low cost. This extends the use of the system beyond simple instructional labs and into the realm of research and thesis implementation work.

Overall, the modular system presented here offers a strong basis in transparency, teachability, and flexibility in the ECE 4550 lab, while solidly meeting the requirements for plant drive electronics for the 4550 lab curriculum. In addition, the hardware's ease of use is orders of magnitude beyond existing solutions. All together, the system presented here is a clear win in nearly every area for the ECE 4550 instructional laboratory environment.

APPENDIX A

SCHEMATICS, LAYOUT, & BOMS: MOTHERBOARD

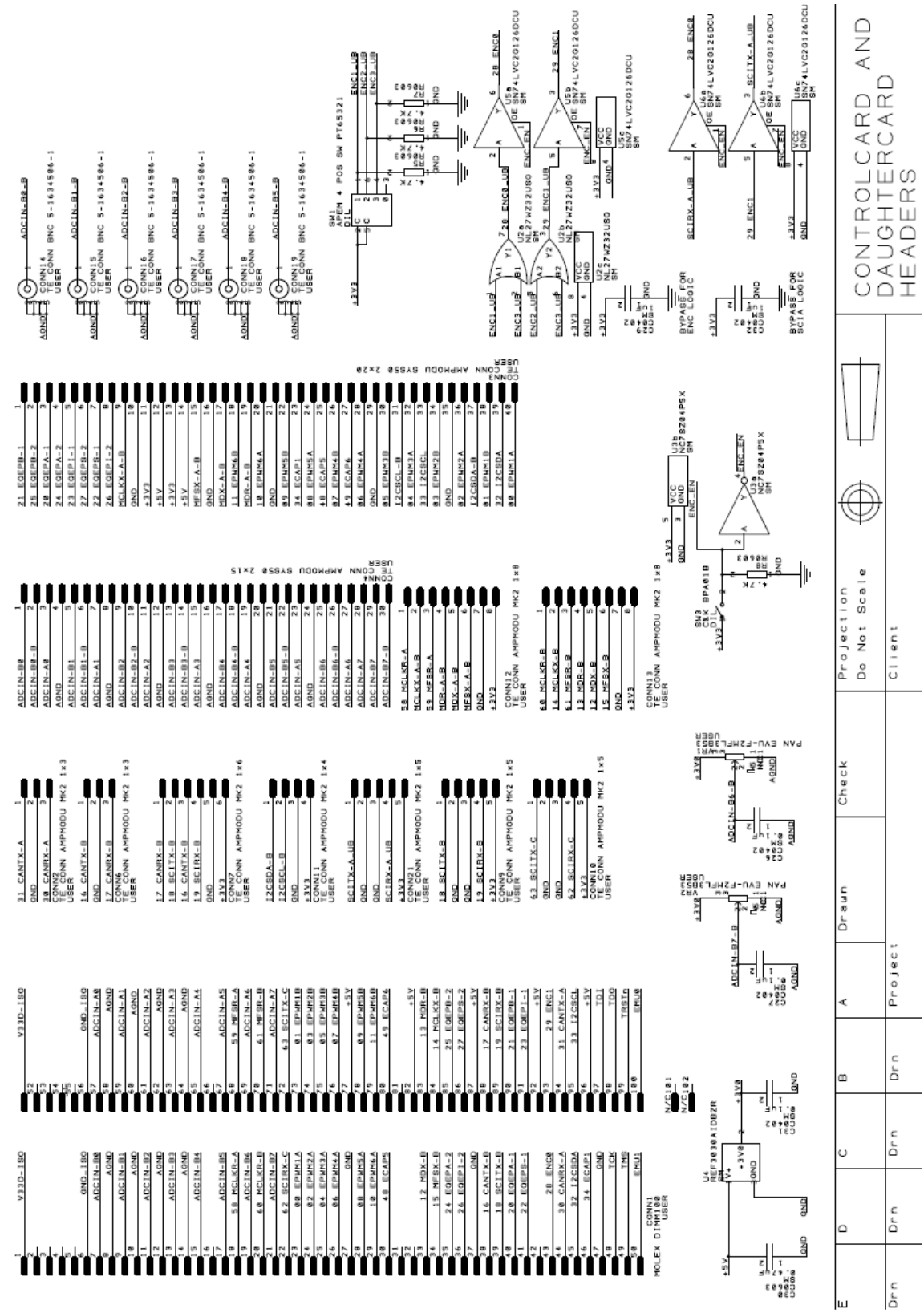

Figure A.1: Motherboard Schematic (1 of 2)

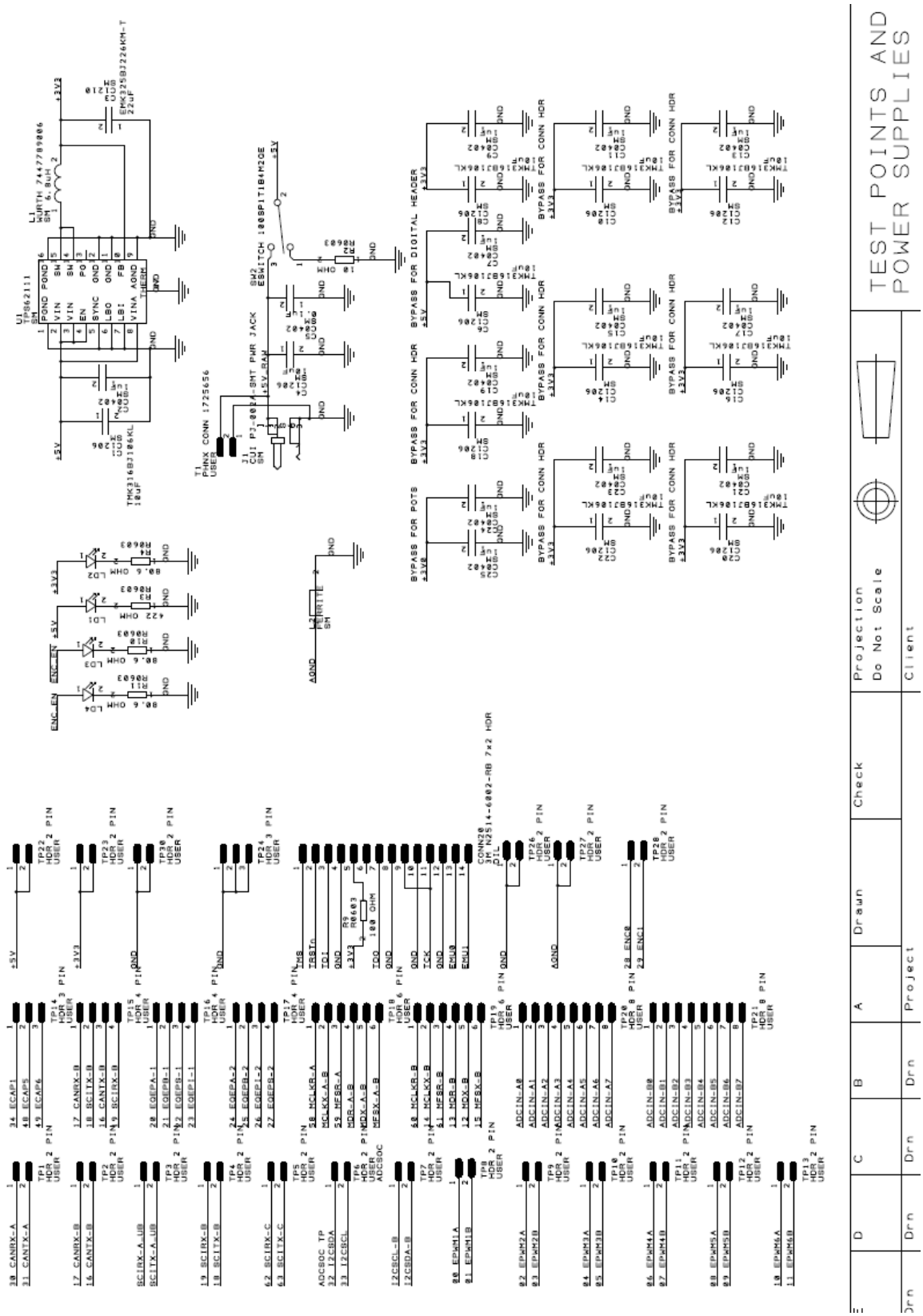

Figure A.2: Motherboard Schematic (2 of 2)

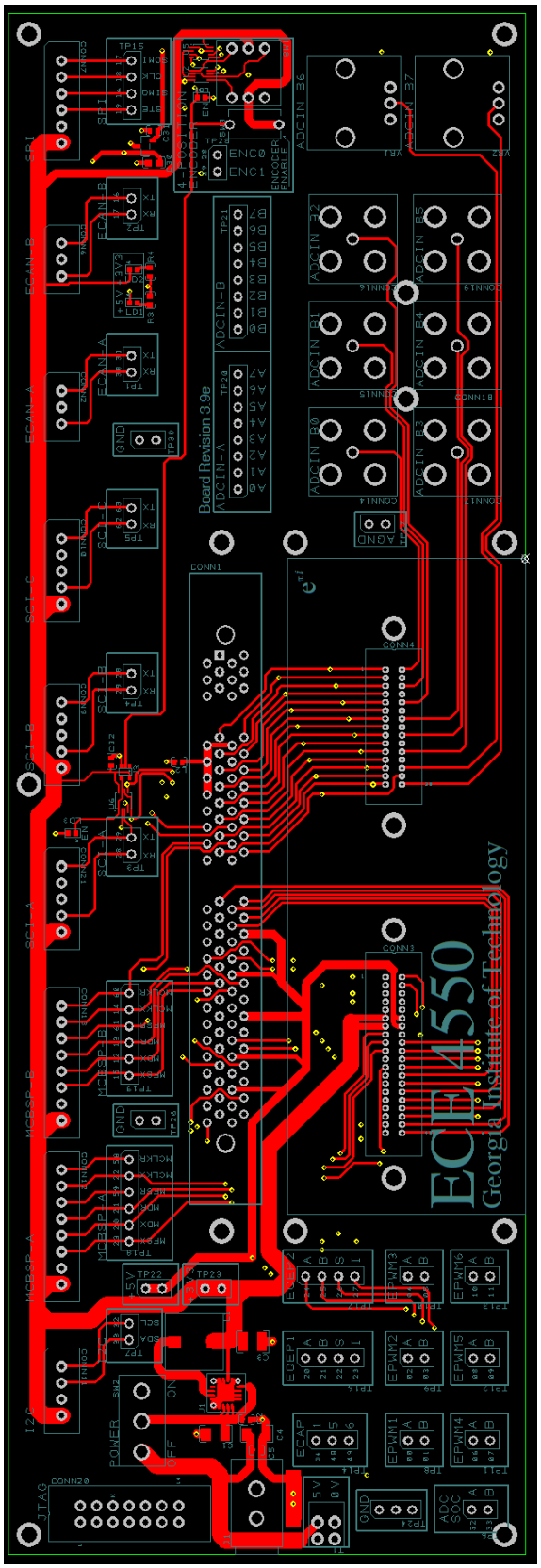

Figure A.3: Motherboard layout, top copper & top silk

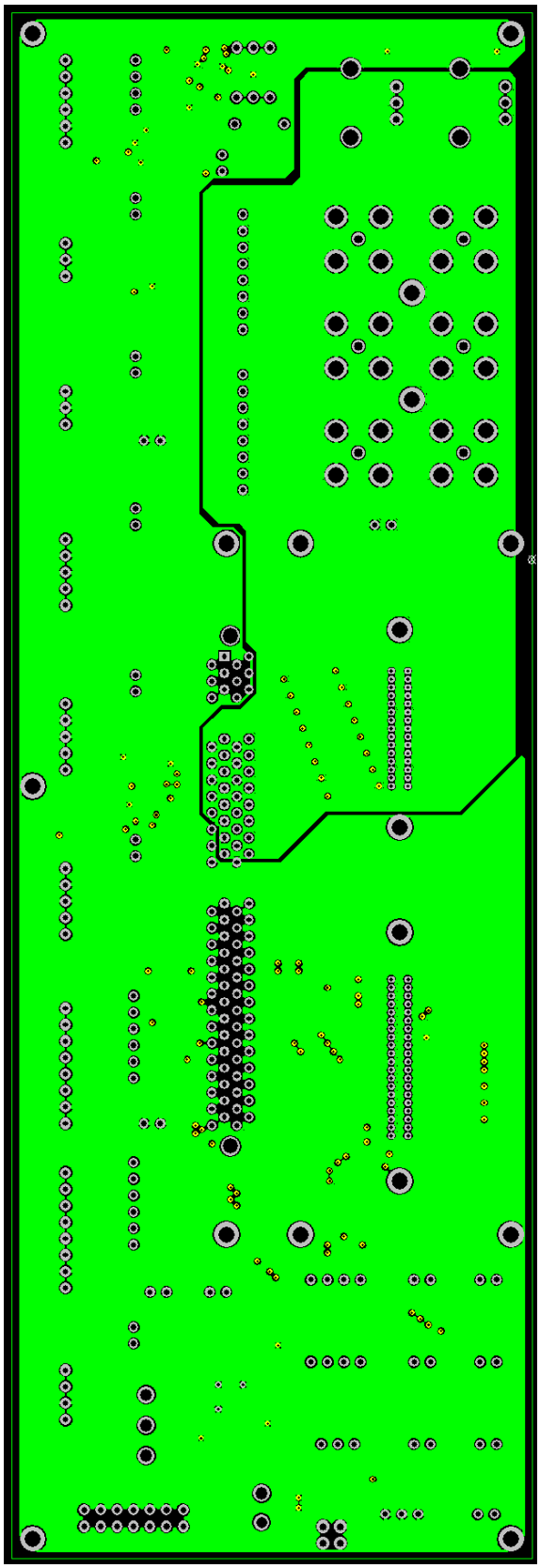

Figure A.4: Motherboard layout, ground plane (layer 2)

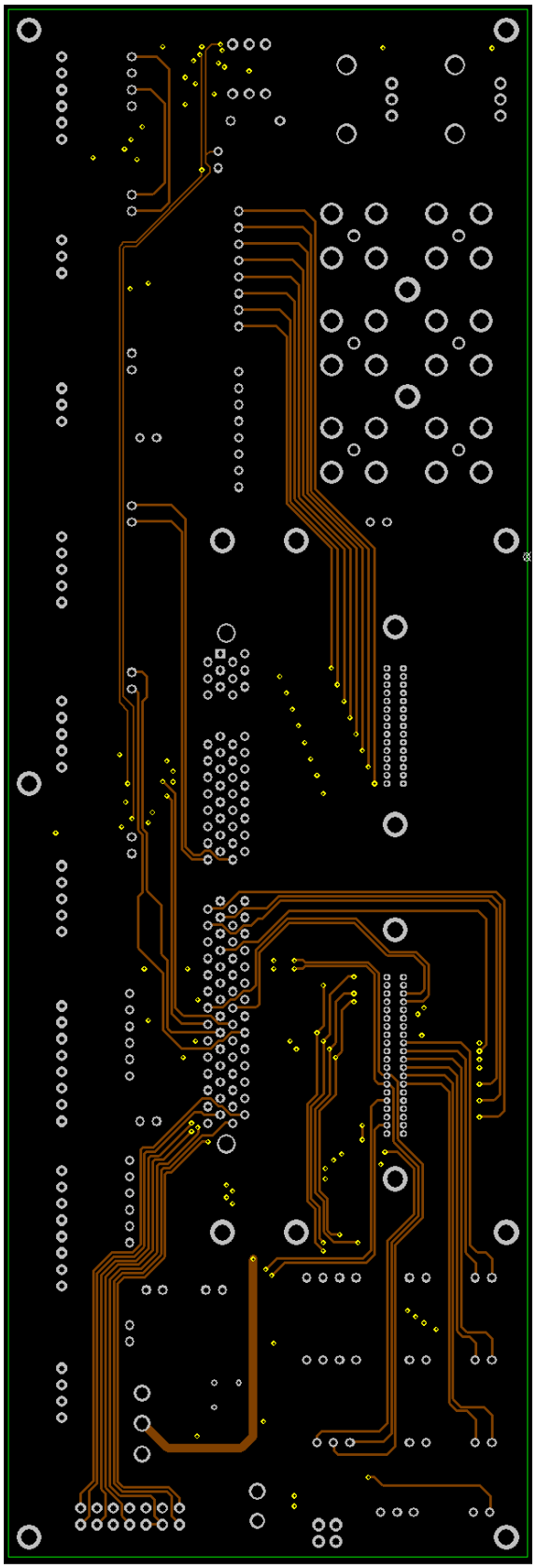

Figure A.5: Motherboard layout, layer 3

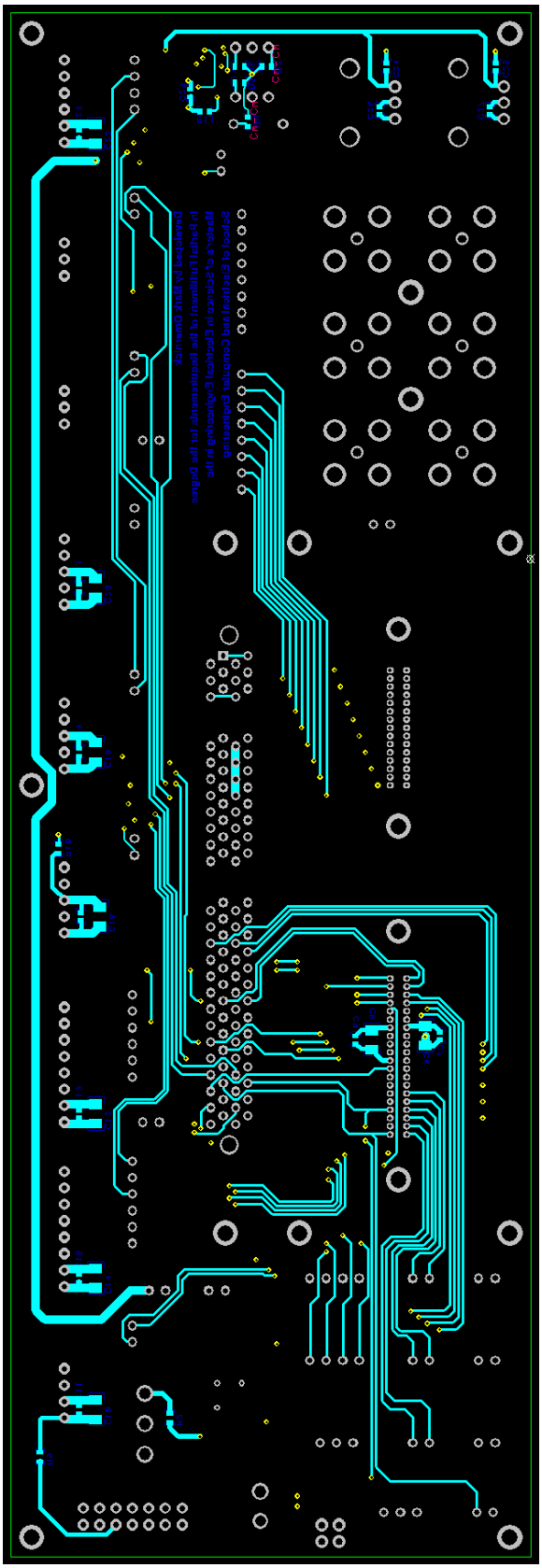

Figure A.6: Motherboard layout, bottom copper & bottom silk

Table A.1: Motherboard Bill of Materials

Component	Value	Qty	Cost	Total	Digi Part No.	Notes
3M N2514-6002-RB 7x2 HDR		1	2.21	2.21	MHC14K-ND	Remove pin 6.
APEM 4 POS SW PT65321		1	6.55	6.55	679-1940-ND	
C&K BPA01B		1	1.34	1.34	CKN10346-ND	
C0402	0.1uF	4	0	0		
C0402	1uF	14	0	0		
C0603	0.47uF	1	0	0		
C1206	10uF	11	0.44	4.84	587-1337-1-ND	
C1210	22uF	1	0.86	0.86	587-2713-1-ND	
CUI PJ-002A-SMT PWR JACK		1	1.74	1.74	CP-002APJCT-ND	
ESWITCH 100SP1T1B4M2QE		1	2.38	2.38	EG2355-ND	
FERRITE		1	0.36	0.36	732-2372-1-ND	
HDR 2 PIN		19	0	0		
HDR 3 PIN		2	0	0		
HDR 4 PIN		3	0	0		
HDR 6 PIN		2	0	0		
HDR 8 PIN		2	0	0		
MOLEX DIMM100		1			Buy at TI online store.	
NC7SP04P5X		1	0.44	0.44	NC7SP04P5XCT-ND	
NL27WZ32USG		1	0.58	0.58	US8_493NL27WZ32USGOSCT-ND	
PAN EVU-F2MFL3B53		2	1.2	2.4	P3G7502-ND	
PAN LNJ926W8CRA BLUE LED		4	0.71	2.84	P13484CT-ND	
PHNX CONN 1725656		1	1.13	1.13	277-1273-ND	
R0603	4.7K	4		0		
R0603	10 OHM	1		0		
R0603	80.6 OHM	3		0		
R0603	100 OHM	1		0		
R0603	422 OHM	1		0		
REF3030AIDBZR		1	2.1	2.1	296-26323-1-ND	
SN74LVC2G126DCU		2	0.54	1.08	296-12555-1-ND	
TE CONN AMPMODU MK2 1x3		2	1.05	2.1	A32977-ND	
TE CONN AMPMODU MK2 1x4		1	1.56	1.56	A32979-ND	
TE CONN AMPMODU MK2 1x5		3	2.61	7.83	A32981-ND	
TE CONN AMPMODU MK2 1x6		1	2.31	2.31	A32983-ND	

Table A.1: Motherboard Bill of Materials (cont'd)

TE CONN AMPMODU MK2 1x8		2	2.64	5.28	A32988-ND	
TE CONN AMPMODU SYS50 2x15		1	5.64	5.64	A33557-ND	
TE CONN AMPMODU SYS50 2x20		1	7.92	7.92	A32570-ND	
TE CONN BNC 5-1634506-1		6	2.03	12.18	A97583-ND	
TPS62111		1	5.25	5.25	296-20670-1-ND	
WURTH 7447789006	6.8uH	1	2.7	2.7	732-1176-1-ND	
				83.62		

APPENDIX B

SCHEMATICS, LAYOUT, & BOMS: I/O DAUGHTERCARD

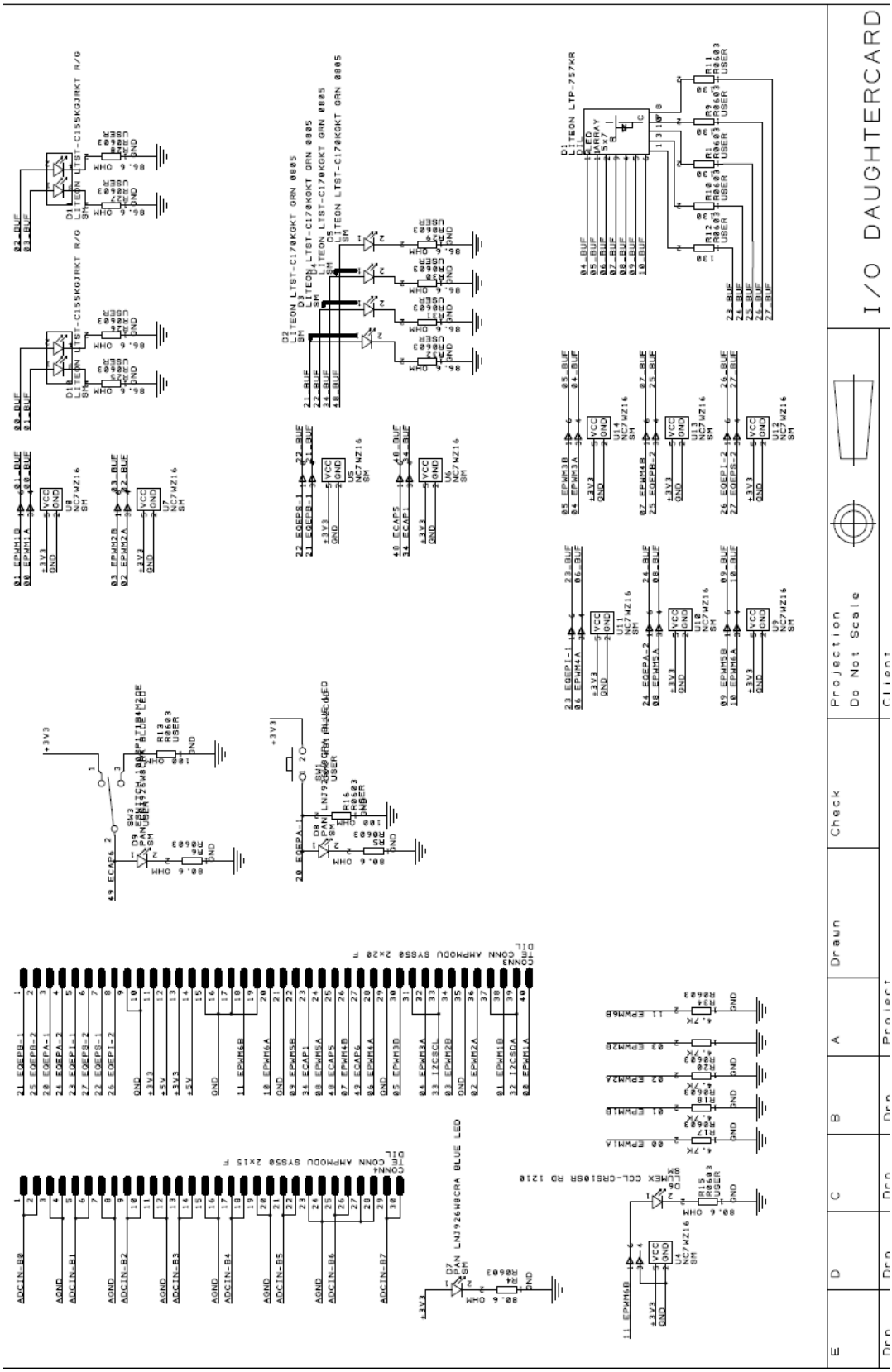

Figure B.1: I/O Daughtercard Schematic (1 of 1)

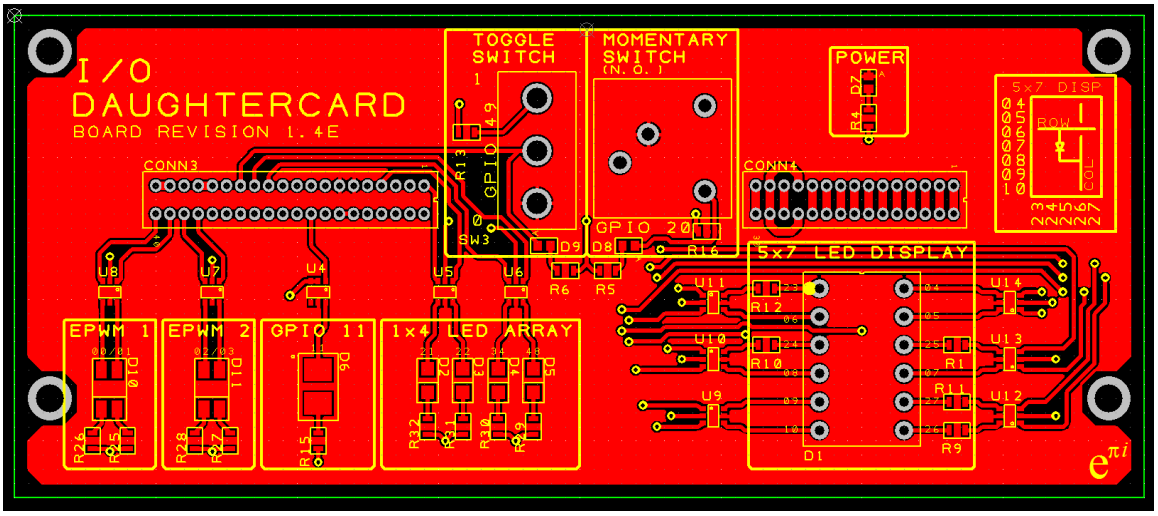

Figure B.2: I/O Daughtercard, top layer & top silk

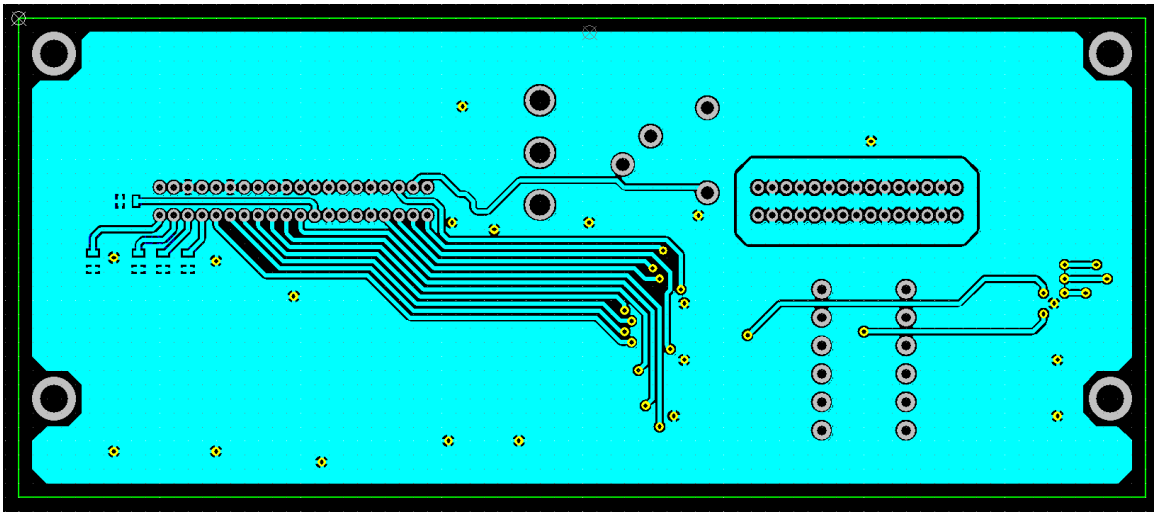

Figure B.3: I/O Daughtercard, bottom layer & bottom silk

Table B.1:I/O Daughtercard Bill of Materials

Component	Value	Qty	Cost	Total	Digi Part No.
C&K KS11R22CQD		1	1.69	1.69	CKN4080-ND
ESWITCH 100SP1T1B4M2QE		1	2.55	2.55	EG2355-ND
LITEON LTP-757KR		1	3.75	3.75	160-1002-ND
LITEON LTST-C155KGJRKT R/G		2	0.46	0.92	160-1409-1-ND
LITEON LTST-C170KGKT GRN 0805		4	0.52	2.08	160-1414-1-ND
LUMEX CCL-CRS10SR RD 1210		1	1.17	1.17	67-1345-1-ND
NC7WZ16		11	0.47	5.17	NC7WZ16P6XCT-ND
PAN LNJ926W8CRA BLUE LED		3	0.71	2.13	P13484CT-ND
R0603	100 OHM	2		0	
R0603	4.7K OHM	5		0	
R0603	80.6 OHM	4		0	
R0603	86.6 OHM	8		0	
R0603	130 OHM	5		0	
TE CONN AMPMODU SYS50 2x15 F		1	5.46	5.46	A33562-ND
TE CONN AMPMODU SYS50 2x20 F		1	7.29	7.29	A31873-ND
			Total:	32.21	

APPENDIX C

SCHEMATICS, LAYOUT, & BOMS: DC DAUGHTERCARD

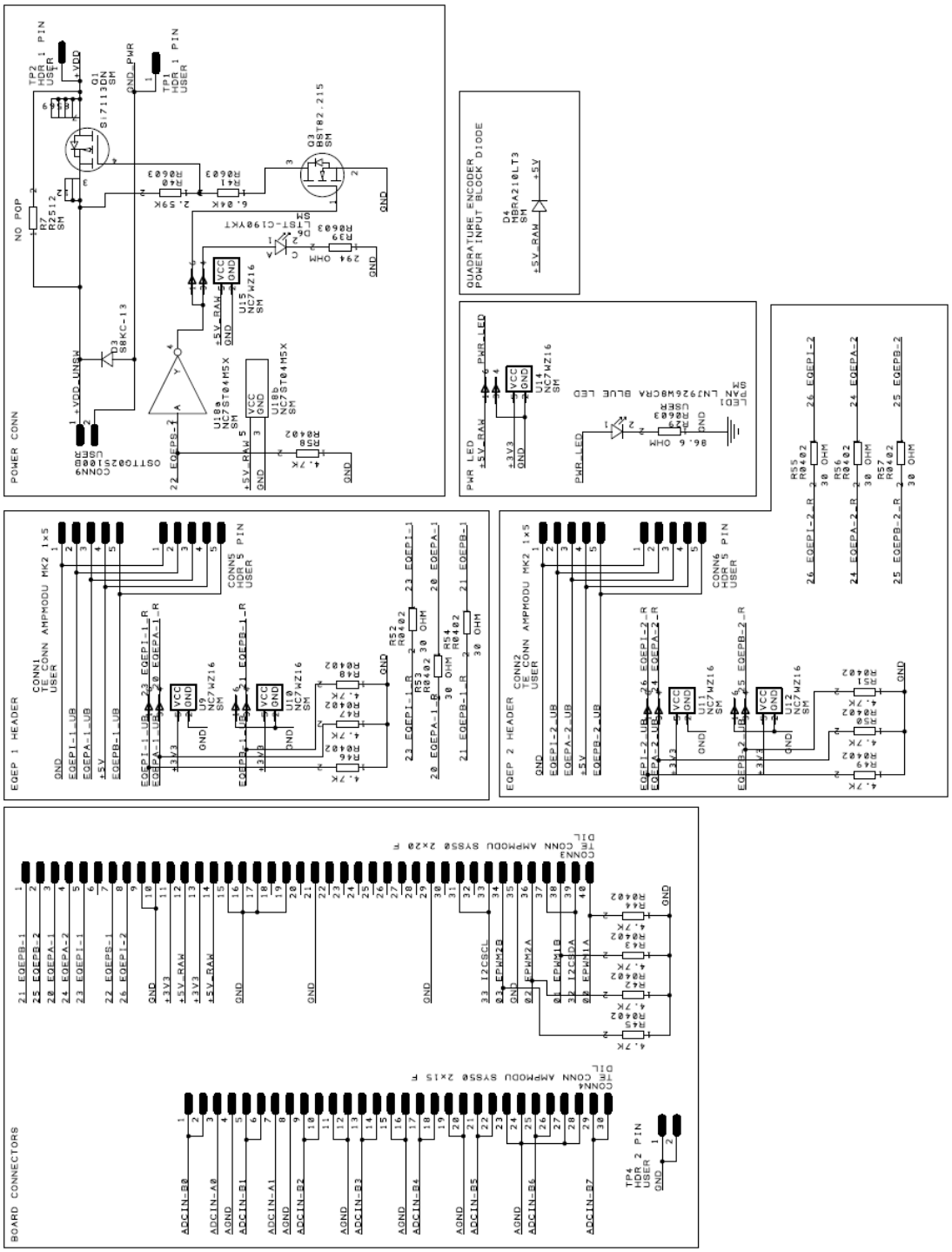

Figure C.1: DC Daughtercard Schematic (1 of 2)

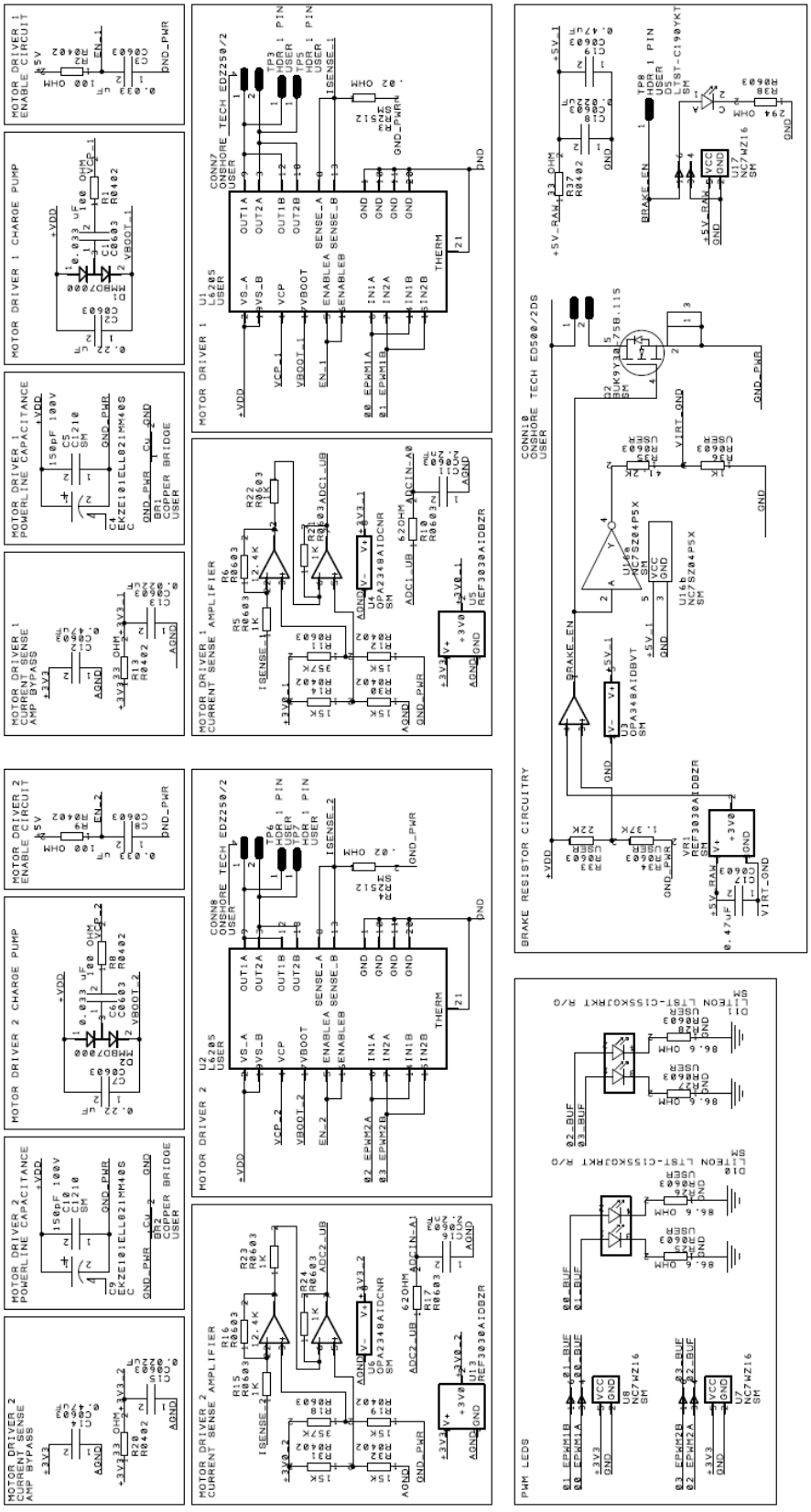

Figure C.2: DC Daughtercard schematic (2 of 2)

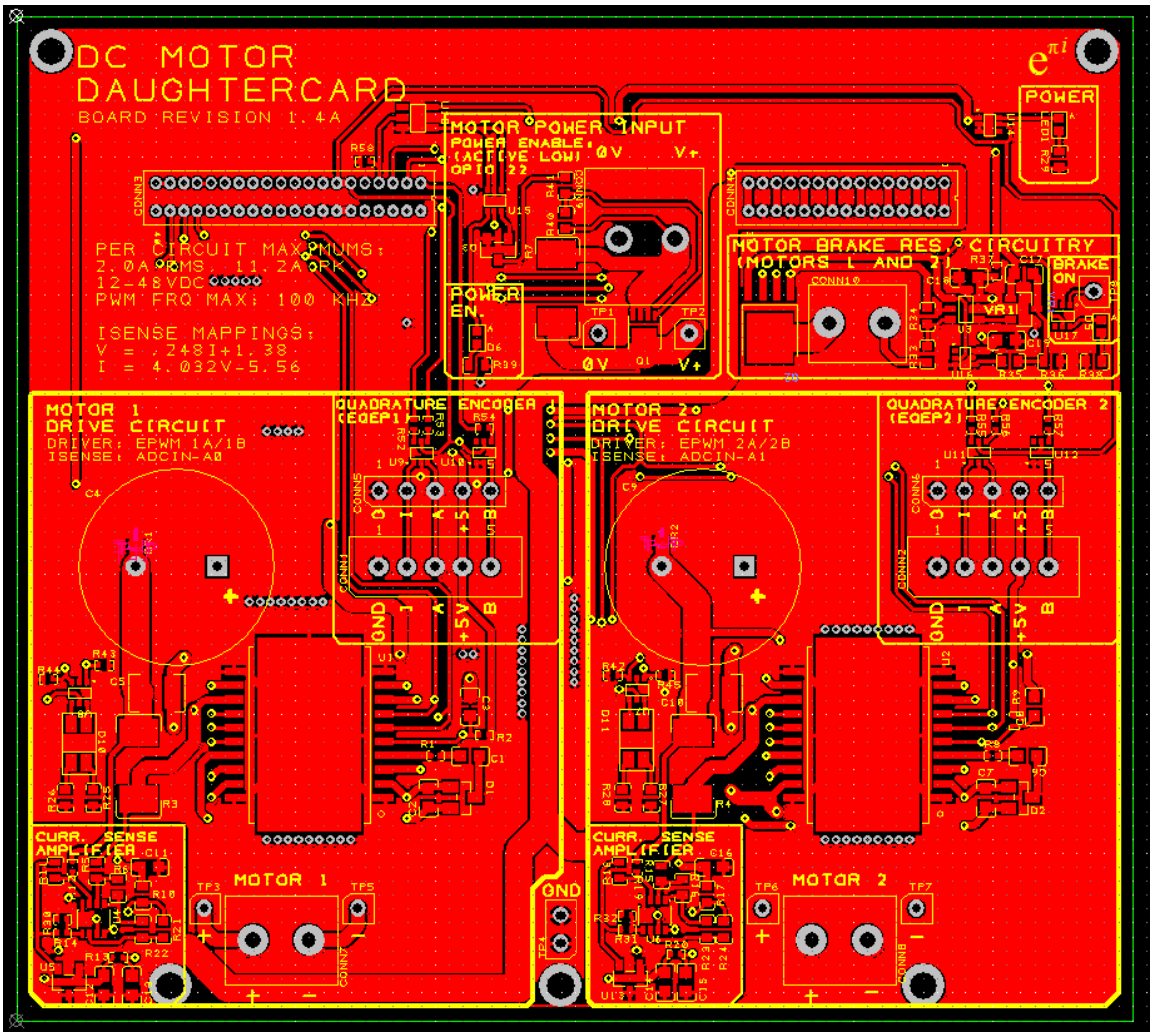

Figure C.3: DC Daughtercard, top copper & top silk

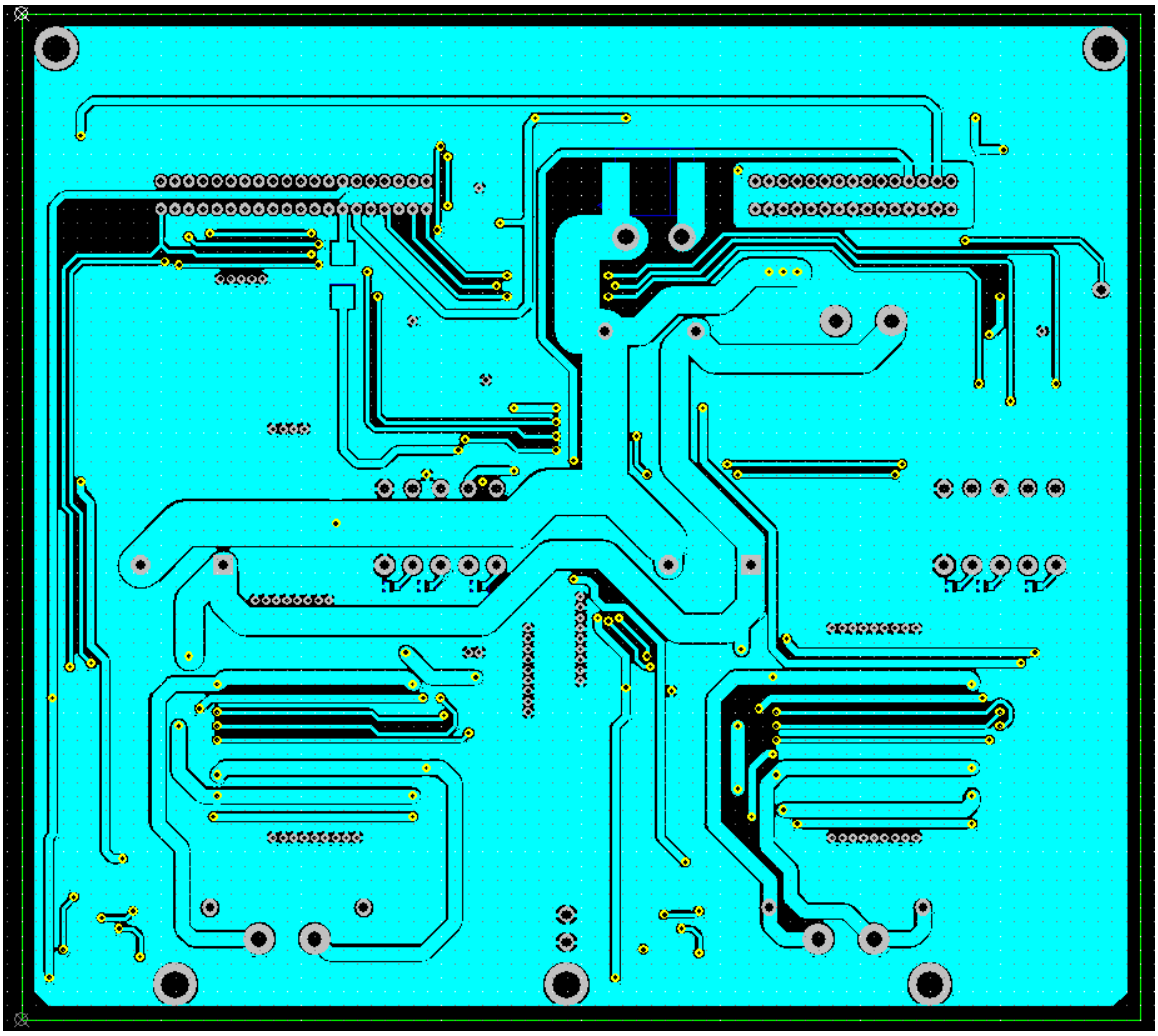

Figure C.4: DC Daughtercard, bottom copper & bottom silk

Table C.1: DC Daughtercard Bill of Materials

Component	Value	Qty	Cost	Total	Digikey No.
BST82,215		1	0.56	0.56	568-6229-1-ND
BUK9Y30-75B,115		1	1.25	1.25	568-6236-1-ND
C0603	0.22 uF @ 25V	2	0.21	0.42	587-1246-1-ND
C0603	0.47uF	4	0	0	
C0603	0.022uF	3	0	0	
C0603	0.033 uF @ 100V	4	0.42	1.68	399-3478-1-ND
C0603	2.2nF	2	0	0	
C1210	150pF 100V	2	0.56	1.12	445-4500-1-ND
EKZE101ELL821MM40S		2	1.85	3.7	565-1746-ND
HDR 1 PIN		7	0	0	
HDR 2 PIN		1	0	0	
HDR 5 PIN		2	0	0	
L6205		2	11.87	23.74	497-3642-1-ND
LITEON LTST-C155KGJRKT R/G		2	0.47	0.94	160-1409-1-ND
LTST-C190YKT		2	0.45	0.9	160-1184-1-ND
MBRA210LT3		1	0.71	0.71	MBRA210LT3GOSCT-ND
MMBD7000		2	0.38	0.76	MMBD7000FSCT-ND
NC7ST04M5X		1	0.52	0.52	NC7ST04M5XCT-ND
NC7SZ04P5X		1	0.43	0.43	NC7SZ08P5XCT-ND
NC7WZ16		9	0.47	4.23	NC7WZ16P6XCT-ND
ONSHORE TECH ED500/2DS		1	0.92	0.92	ED1623-ND
ONSHORE TECH EDZ250/2		2	0.74	1.48	ED1973-ND
OPA348AIDBVT		1	0.85	0.85	296-12276-1-ND
OPA2348AIDCNR		2	1.12	2.24	296-26256-1-ND
OSTTG025100B		1	0.35	0.35	ED2703-ND
PAN LNJ926W8CRA BLUE LED		1	0.71	0.71	P13484CT-ND
R0402	4.7K	11	0	0	
R0402	15K 0.5%	6	0.6	3.6	P15KDCCT-ND
R0402	30 OHM	7	0	0	
R0402	33 OHM	2	0	0	
R0402	100 OHM	4	0	0	
R0603	1K 0.5%	7	0.51	3.57	P1.0KDBCT-ND

Table B.1: DC Daughtercard Bill of Materials (cont'd)

R0603	1.37K	1	0.125	0.125	311-1.37KDCT-ND
R0603	2.59K	1	0	0	
R0603	6.04K	1	0	0	
R0603	12.4K 0.5%	2	0.04	0.08	P12.4KHCT-ND
R0603	22K	1	0.37	0.37	A103066CT-ND
R0603	41.2K 0.5%	1	0.52	0.52	RG16P41.2KBCT-ND
R0603	62OHM	2	0	0	
R0603	86.6 OHM	5	0	0	
R0603	294 OHM	2	0	0	
R0603	357K 0.5%	2	0.148	0.296	RR08P357KDCT-ND
R2512	.02 OHM	2	0.56	1.12	P20MCT-ND
R2512	NO POP	1	0	0	
REF3030AIDBZR		3	2.1	6.3	296-26323-1-ND
S8KC-13		1	0.7	0.7	S8KCDICT-ND
Si7113DN		1	1.82	1.82	SI7113DN-T1-GE3CT-ND
TE CONN AMPMODU MK2 1x5		2	2.61	5.22	A32981-ND
TE CONN AMPMODU SYS50 2x15 F		1	5.46	5.46	A33562-ND
TE CONN AMPMODU SYS50 2x20 F		1	7.29	7.29	A31873-ND
				83.421	

APPENDIX D

SCHEMATICS, LAYOUT, & BOMS: AC DAUGHTERCARD

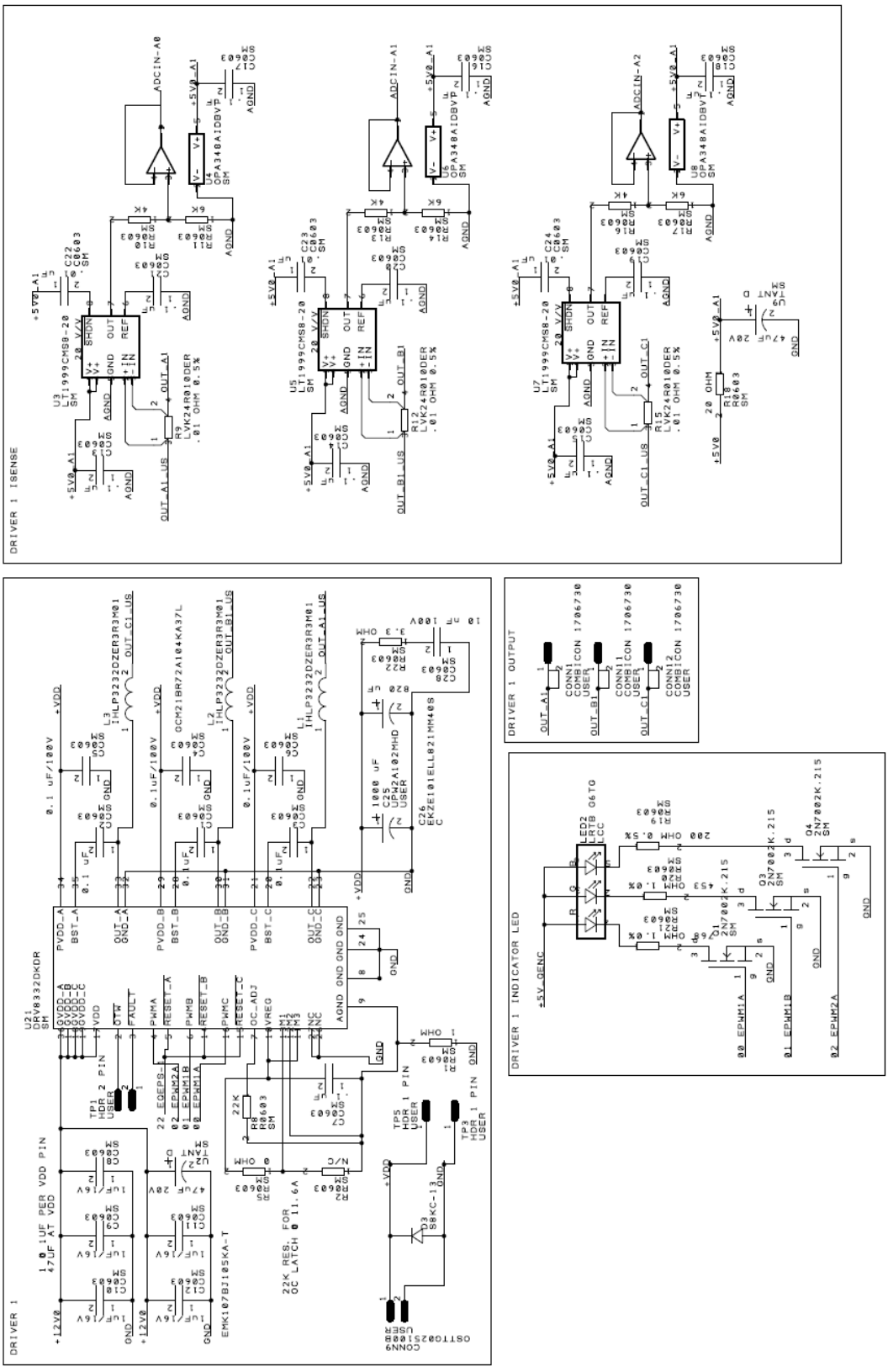

Figure D.1: AC Daughtercard Schematic (1 of 2)

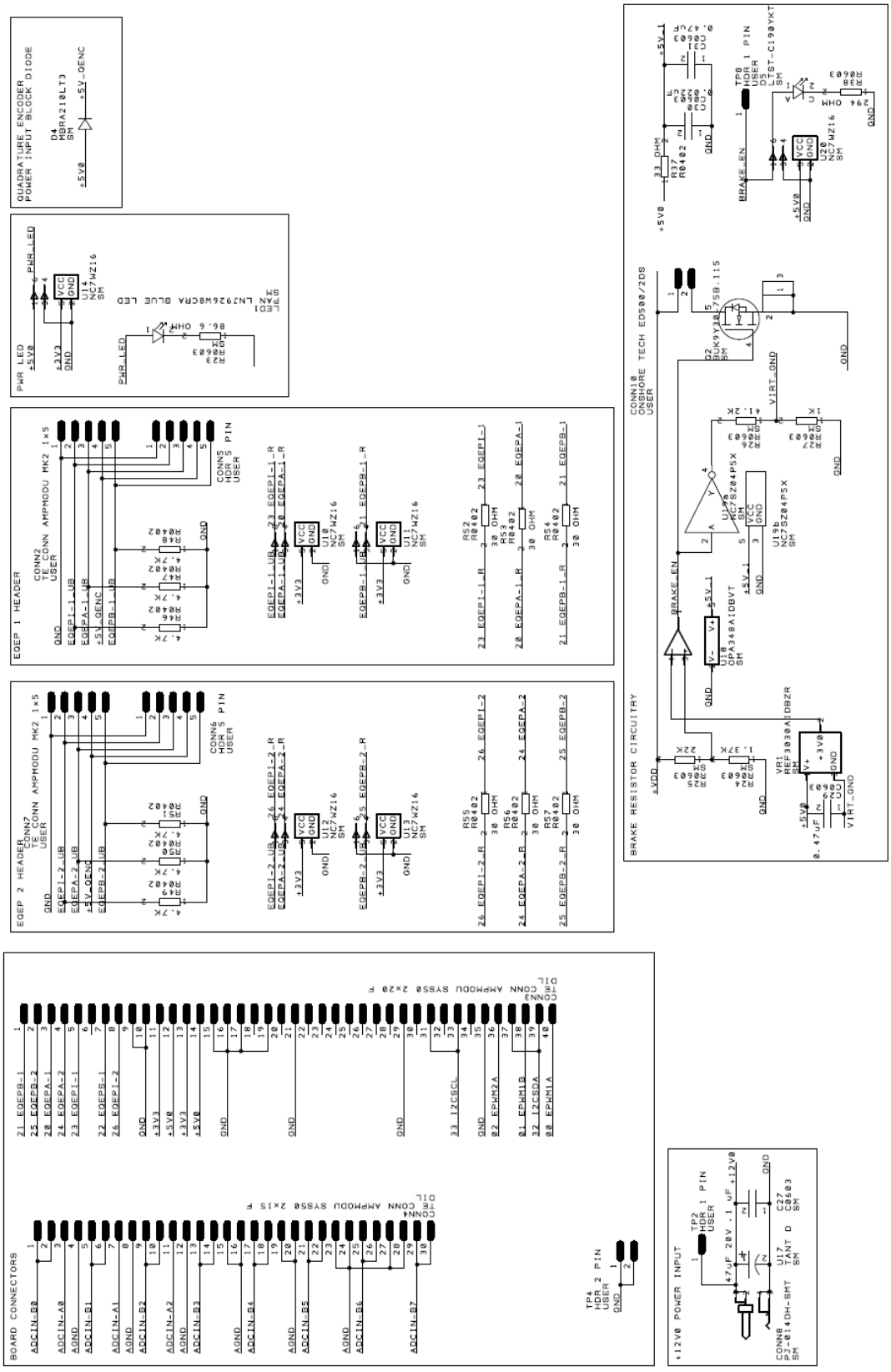

Figure D.2: AC Daughtercard Schematic (2 of 2)

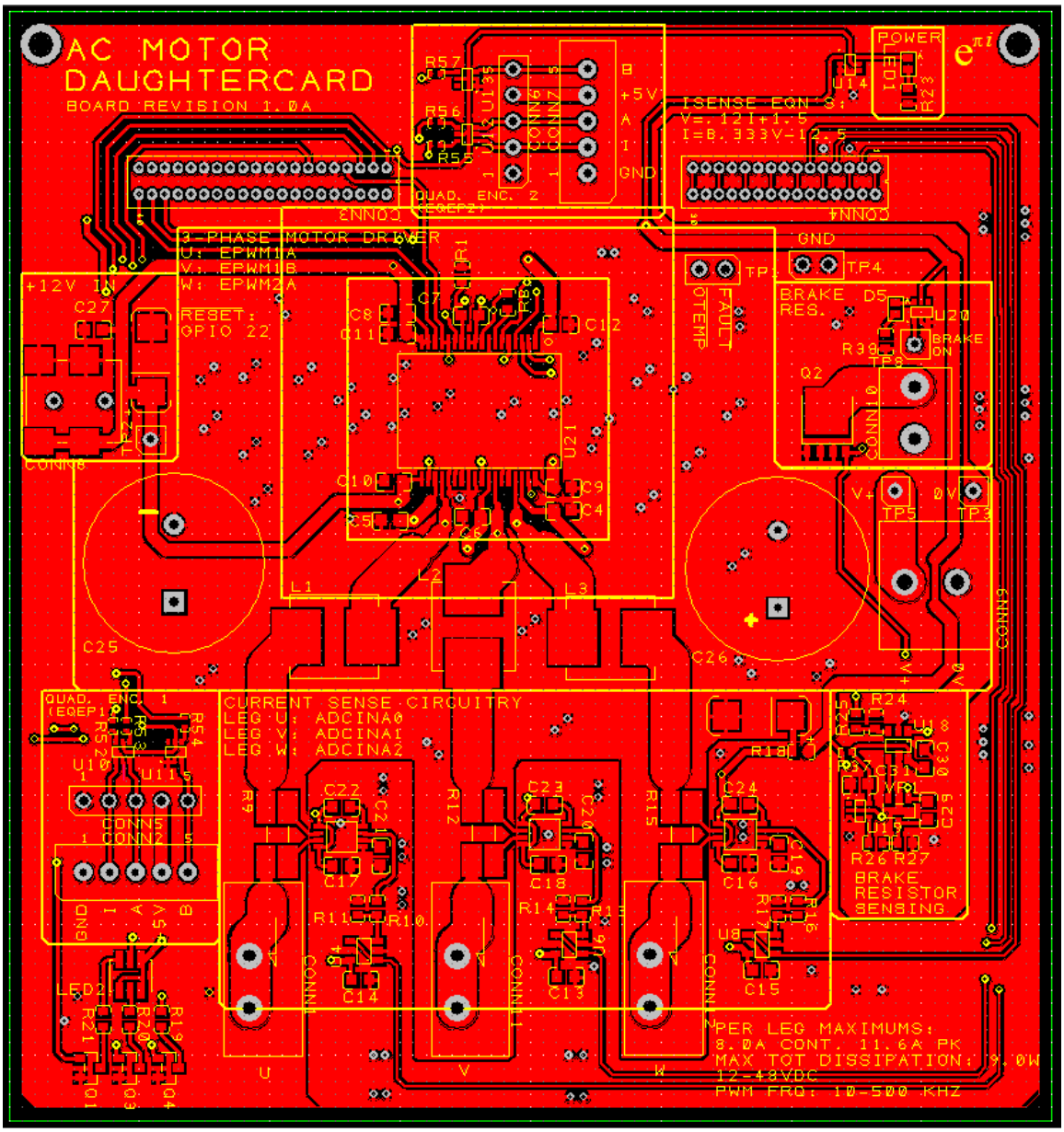

Figure D.3: AC Daughtercard, top copper & top silk

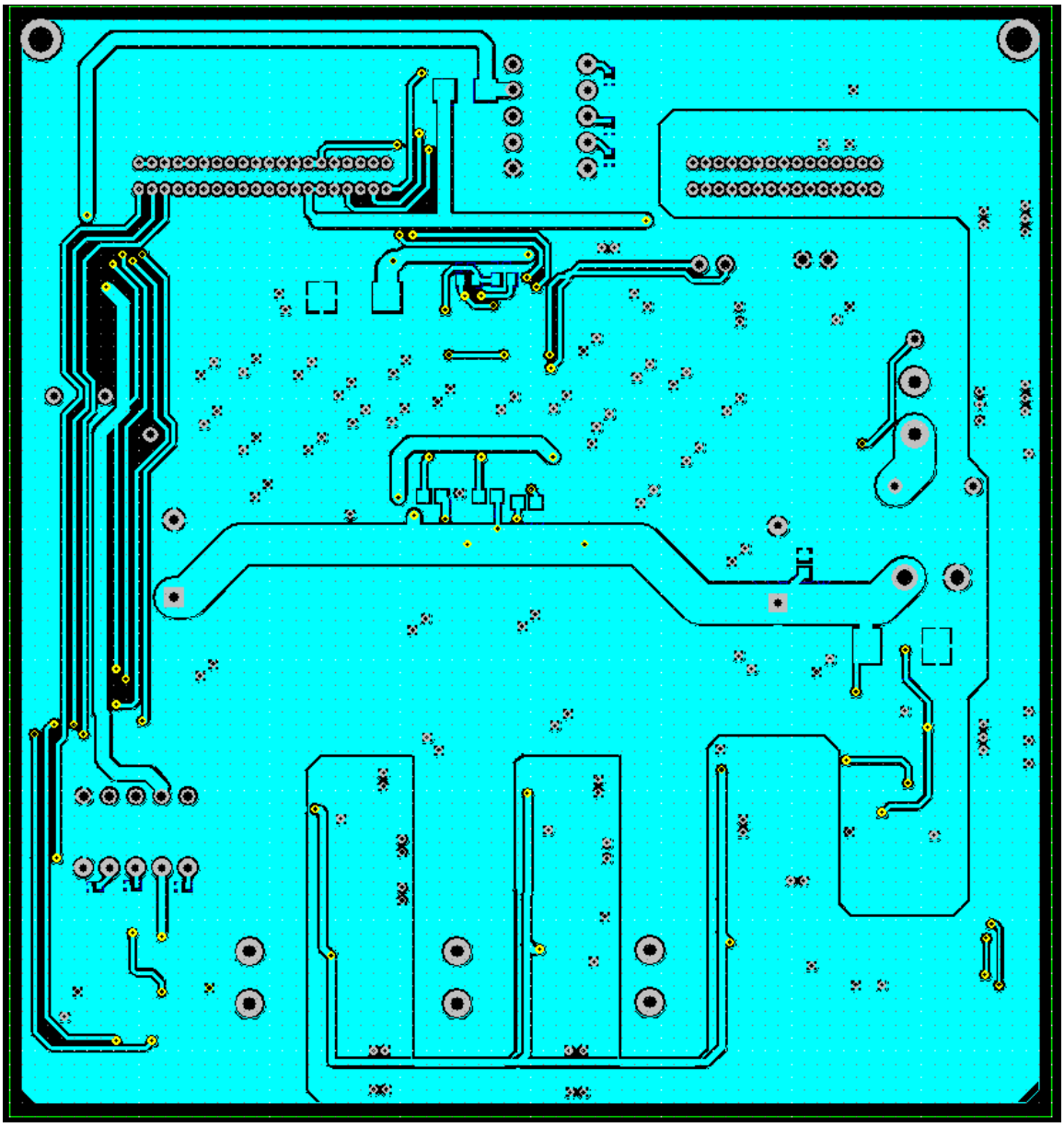

Figure D.4: AC Daughtercard layout, bottom copper & bottom silk

Table D.1: AC Daughtercard Bill of Materials

Component	Value	Qty	Cost	Total	Digikey No.
2N7002K,215		3	0.28	0.84	568-4984-1-ND
BUK9Y30-75B,115		1	1.25	1.25	568-6236-1-ND
C0603	0.1 uF	14	0	0	
C0603	.01 uF	3	0	0	
C0603	0.1uF/100V	3	0.3	0.9	445-6938-1-ND
C0603	0.47uF	2	0	0	
C0603	0.022uF	1	0	0	
C0603	1uF/16V	5	0.2	1	587-1251-1-ND
C0603	10 nF 100V	1	0.18	0.18	445-5199-1-ND
COMBICON 1706730		3	0.56	1.68	277-1317-ND
DRV8332DKDR		1	12.43	12.43	296-27518-5-ND
EKZE101ELL821MM40S	820 uF	1	1.85	1.85	565-1746-ND
HDR 1 PIN		4	0	0	
HDR 2 PIN		2	0	0	
HDR 5 PIN		2	0	0	
IHLP3232DZER3R3M01		3	1.59	4.77	541-1373-1-ND
LRTB G6TG		1	1.75	1.75	475-1319-1-ND
LT1999CMS8-20		3	4.08	12.24	LT1999CMS8-20#PBF-ND
LTST-C190YKT		1	0.45	0.45	160-1184-1-ND
LVK24R010DER	.01 OHM 0.5%	3	1.23	3.69	LVK24R010DERCT-ND
MBRA210LT3		1	0.71	0.71	MBRA210LT3GOSCT-ND
NC7SZ04P5X		1	0.74	0.74	NC7SZ04P5XCT-ND
NC7WZ16P6X		6	0.47	2.82	NC7WZ16P6XCT-ND
ONSHORE TECH ED500/2DS		1	0.92	0.92	ED1623-ND
OPA348AIDBVT		4	0.85	3.4	296-12276-1-ND
OSTTG025100B		1	0.7	0.7	ED2703-ND
PAN LNJ926W8CRA BLUE LED		1	0.71	0.71	P13484CT-ND
PJ-014DH-SMT		1	1.31	1.31	CP-014DHPJCT-ND
R0402	4.7K	6	0	0	
R0402	30 OHM	6	0	0	
R0402	33 OHM	1	0	0	
R0603	0 OHM	1	0	0	

Table D.1: AC Daughtercard Bill of Materials (cont'd)

R0603	1 OHM	1	0	0	
R0603	1K	1	0	0	
R0603	1.37K	1	0	0	
R0603	3.3 OHM	1	0	0	
R0603	10K 0.1%	3	0.51	1.53	P10KDBCT-ND
R0603	15K 0.1%	3	0.51	1.53	P15KDBCT-ND
R0603	20 OHM	1	0	0	
R0603	22K	2	0	0	
R0603	41.2K	1	0	0	
R0603	86.6 OHM	1	0	0	
R0603	200 OHM 0.5%	1	0.11	0.11	RR0816P-201-D
R0603	294 OHM	1	0	0	
R0603	453 OHM 1.0%	1	0.04	0.04	P453HCT-ND
R0603	768 OHM 1.0%	1	0.04	0.04	P768HCT-ND
R0603	NO POP	1	0	0	
REF3030AIDBZR		1	2.1	2.1	296-26323-1-ND
S8KC-13		1	0.47	0.47	S8KCDICT-ND
TANT D	47uF 20V	3	2.1	6.3	718-1525-1-ND
TE CONN AMPMODU MK2 1x5		2	2.61	5.22	A32981-ND
TE CONN AMPMODU SYS50 2x15 F		1	5.46	5.46	A33562-ND
TE CONN AMPMODU SYS50 2x20 F		1	7.29	7.29	A31873-ND
UPW2A102MHD	1000 uF	1	3.03	3.03	493-1988-ND
				87.46	

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[1] Anon., “Pinout”, http://processors.wiki.ti.com/index.php/JTAG_Connectors#Pinout (Accessed February 25, 2012).

[2] Anon., “66-Each-4-Layers”, http://www.4pcb.com/index.php?load=content&page_id=131 (accessed February 25, 2012).

[3] Anon., “L6205 DMOS Dual Full Bridge Driver”, http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/DATASHEET/CD00002345.pdf (accessed February 25, 2012).

[4] Anon., “DRV8312/DRV8332 Three Phase PWM Motor Driver (SLES256)”, http://www.ti.com/lit/ds/symlink/drv8312.pdf (accessed February 27, 2012)