MEMS-based Phase-Locked-Loop Clock Conditioner

A Dissertation
Presented to
The Academic Faculty

By

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In Partial Fulfillment
Of the Requirements for the Degree
Doctor of Philosophy in Electrical and Computer Engineering

Georgia Institute of Technology

May 2012

MEMS-based Phase-Locked-Loop Clock Conditioner

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I dedicate this dissertation to the best persons that God could select to take care of me:

Dad, Mom, and Lili

"Porque mis viejos en mi alma infundieron sanas costumbres y a ser como soy. Por el amor tan grande de mis padres buenos y el gran aprecio que mis amigos me dan"

-Modified from a colombian folkloric song
by Marciano Martinez.

ACKNOWLEDGEMENTS

I want to express my sincere gratitude to my mentor and advisor, Professor Farrokh Ayazi for his support, encouragement and especially for showing me how research has to be done. It has been a pleasure to be one of his students and to measure my work with the highest quality standards that will make me unique. Especially, I want to thank for the conversations that we had that were more than research guidance to become lessons for life.

I thank my dissertation defense committee members, Professor Gabriel Rincón-Mora, Professor Kevin Kornegay, Professor Maysam Ghovanloo and Professor Levent Degertekin for their help in preparing this dissertation and finish my doctorate degree. In particular, I want to thank Professor Rincón-Mora for considering helping to develop projects in my home country looking to develop a research program that will help other latin-americans in the pursuit to be in the cutting edge of knowledge.

In this regard, it is my honor to present my gratitude and respect to my sponsor Fundación Universidad del Norte that opened a lot of doors for me to be able to come to this marvelous school and gave me the best gift of all, my graduate studies. Today, I can say that it will be a privilege to go back, fully prepared, and work together for what we believe our bright students deserve.

In particular, one of the things that I have learned is that teamwork make things happen, and my colleagues and friends in the IMEMS Research Group deserve all my gratitude for helping me unconditionally to succeed in this research. All of them, previous and current members of the group, thank you.

Lastly, I dedicate these lines to my wonderful family, dad, mom and Lili. I love you so much, thank you. All I am is due to the love, teaching and guidance that you gave me without reserves. You have showed me that there is a God that protects us and that will allow our projects to succeed by trusting Him along to hard work, courage and honesty.

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SUMMARY

Ultra narrow-band filters and the use of two loops in a cascade configuration dominate current clock conditioners based on phase-locked-loop (PLL) schemes. Since a PLL exhibits a low-pass transfer function with respect to the reference clock, the noise performance at very close-to-carrier offset frequencies is still determined by the input signal. Although better cleaning can be achieved with extremely narrow loops, an ultra low cut-off frequency could not be selected since the stability of the configuration deteriorates as the filter bandwidth is reduced. This fact suggests that a full-spectrum clock conditioning is not possible using traditional PLL architectures, and an alternative scheme is necessary to attenuate the very-close-to-carrier phase noise (PN). In addition, ultra-narrow loop filters can compromise on-chip integration because of the large size capacitors needed when chosen as passive. Input signal attenuation with relaxed bandwidth requirements becomes the main aspect that a comprehensive clock cleaner must address to effectively regenerate a reference signal.

This dissertation describes the Band-Reject Nested-PLL (BRN-PLL) scheme, a modified PLL-based architecture that provides an effective signal cleaning procedure by introducing a notch in the input transfer function through inner and outer loops and a high-pass filter (HPF). This modified response attenuates the reference-signal PN and reduces the size of the loop-filter capacitors substantially. Ultra narrow loops are no longer required because the notch size is related to the system bandwidth. The associated transfer function for the constitutive blocks (phase detectors and local oscillators) show that the output close-to-carrier and far-from-carrier PN sections are mainly dominated by

the noise from the inner-PLL phase detector (PD) and local oscillator (LO) located in the outer loop, respectively. The inner-PLL PD transfer function maintains a low-pass characteristic with a passband gain inversely proportional to the PD gain becoming the main contribution around the carrier signal. On the other hand, the PN around the transition frequency is determined mainly by the reference and the inner-PLL LO. Their noise contributions to the output will depend on the associated passband local maxima, which is located at the BRN-PLL transition frequency. Hence, in this region, the inner-PLL LO is selected so that its effect can be held below that of the outer-PLL PD.

The BRN-PLL can use a high-Q MEMS-based VCO to further improve the transition region of the output PN profile and an LC-VCO as outer-PLL LO to reduce the noise floor of the output signal. In particular, two tuning mechanisms are explored for the MEMS-VCO: series tuning using varactors and phase shifting of a resonator operating in nonlinear regime. Both schemes are implemented to generate a tunable oscillator with no PN-performance degradation.

CHAPTER 1

INTRODUCTION

1.1. Overview

Designers rely on clock conditioners to minimize the effect of clock jitter on the signal to noise ratio (SNR). The function of these blocks is to reduce jitter and improve the spectral purity of the clock signal in communication systems. A phase-locked loop (PLL) can be used as a clock cleaner because it behaves as a highly-selective tunable band-pass filter. When locked, the PLL allows the phase noise (PN) of the reference signal to pass close to the carrier frequency, while the local oscillator (LO) PN will dominate at large offset frequencies [1].

For a clock conditioner, the loop-filter bandwidth should be narrow to minimize the effect of the reference PN, and further reduction in the bandwidth is achieved by using dividers at the PLL input, an approach popular in industry [2]. Recently, a cascade-type PLL architecture has been employed to clean the clock signal in two steps using two loops [3, 4]. In this approach, if the input signal PN can be divided into two regions, the two associated LOs can be utilized to target each section independently, instead of relying on one LO with excellent overall PN performance.

Noise simulations based on phase models [5] reveal that the cascade-type PLL is capable of producing an output signal, whose PN can be defined by the performance of the two LOs used in the scheme. However, since stability of the architecture deteriorates as the loop bandwidth is narrowed, the noise at very close-to-carrier offset frequencies determined by the reference signal cannot be removed totally. This fact suggests that

complete clock conditioning is not possible using traditional PLL configurations, and an alternative scheme is necessary to attenuate the very close-to-carrier PN.

Besides the potential stability issues derived from an ultra-narrow band PLL, on-chip integration can be compromised due to the large size capacitors needed to configure the cleaner, if passive filters are used to reduce noise. Attenuation of the input-signal PN with relaxed bandwidth requirements becomes the main aspect that a full-spectrum clock cleaner must address to effectively regenerate a timing signal.

In addition to the modified PN shaping capability, the alternative configuration utilizes the PN characteristics of two voltage-controlled oscillators (VCOs) to improve the spectral purity of the incoming signal. A combination of a micro-electro-mechanical-system (MEMS) VCO and an LC VCO can produce the best results. The LC-based VCO is built with a negative-resistance cross-coupled generator [6] and a resistive biasing network [7] to suppress the noise of the current source. The possibility of an off-chip tank circuit enables the use of external components with higher quality factors. For the MEMS VCO, a topology based on a transimpedance amplifier (TIA) is selected, but compared to the well-known tuning mechanisms for LC VCOs, frequency-pulling strategies for MEMS-based VCOs are rather complex and limited. Two options are explored, a series-tuning scheme with varactors and a phase-based frequency pulling of nonlinearly-operated resonators [8]. An evaluation of both strategies is conducted for the best trade-off between tuning range and PN performance.

Simulation of PLL-based systems deserves special attention due to the intrinsic nonlinear nature of the feedback loop. Several tools have been created to facilitate the design and analysis of PLLs, and some examples include MATLAB and SIMULINK for

stability and transient analyses, respectively [9]. Literature has shown that the development of alternative tools is extensive [10-13]. Some designers have used software outside the transistor-level simulation program to have more flexibility and powerful libraries; however, most of these options are not standard, and therefore not available to any designer.

When PLL-based systems are intended for IC fabrication, although several strategies can be used during the top-level stage of the design, the implementation will need to be transferred to platforms for the bottom-level stage of the process (i.e. Cadence). Hence, designers need to keep track of the results during the design procedure, which imposes a method to share and transfer files from the different tools. The use of many programs can become a disadvantage depending on the portability of the reports.

Additionally, it is possible that manipulation of different programs and simulation settings generate misleading results, if proper configuration for each tool is not done properly. At the end, designers can be pushed to carry out extensive transistor-level simulations that not only are resource and time consuming, but also can have convergence problems due to the nonlinear nature of the PLL.

Since [5,14] offers a comprehensive set of element modeling for Verilog-A and a methodology for phase-noise simulations, this research project includes an initiative for including all PLL-design stages in a single kit using the simulation tool Spectre. The simulator selection is based on the fact that Cadence contains complete analog libraries (lumped elements) and supports Verilog-A as hardware description language. Once the modeling has been defined, basic analyses (AC, noise, transient) will be used to provide a quick and accurate analysis of a PLL-based system.

Pole-zero locations for stability analysis and transfer functions for different noise sources are modeled with lumped circuit elements, under the assumption that the PLL scheme is a continuous system in steady state. On the contrary, since the lock-in process is by nature nonlinear, the building blocks are modeled with Verilog-A units for transient analysis. Finally, for phase-noise performance, the noise behavior of each component is captured in additional Verilog-A files employing phase modes. A detailed procedure is available in [5].

1.2. Origin and History

Since timing signals are fundamental in the performance of synchronous systems, clock jitter is a figure of merit in digital applications, such as data communications, networking, and high-definition video transmission. Typically, the clock signal is embedded with the data, and the effect of jitter can alter the cycle time causing the data to be latched incorrectly and/or limiting the speed of transmission. Careful design of clock recovering systems (and clock regenerators when the information is carried over long distances) becomes essential to guarantee system specifications such as the bit error rate (BER).

Clock quality is usually described by jitter or PN. Clock jitter is defined as the time-domain instability of the clock signal, while PN is the frequency-domain representation of the clock noise. A mathematical relationship between jitter measured in time and the phase-noise measured in frequency can be established. This quantitative relationship between the two measurements helps in the design of a clock cleaner. Thus, a

clock conditioner can be viewed as a highly selective tunable filter that removes sidebands improving the spectral purity of the timing signal.

Two possible approaches to build such a filter can be found, either using delay-based circuits or PLL schemes. Arkas et al. propose a jitter filter based on delay units and logic circuitry [15]. This circuit narrows the reference-signal spectrum by applying the logic AND operation to delayed versions of the input clock. The basic unit with a delay of *x* seconds should equal the period of the signal of interest. When the AND operation is applied, the input clock is pulled to the ideal frequency determined by the system. The output signal will have an uneven duty cycle after this processing, which implies that a flip-flop can be used to obtain a 50% duty-cycle; although, this technique halves the frequency of the signal. A frequency doubler can be placed at the backend of this architecture to restore the original value of the frequency. An improved filtering action

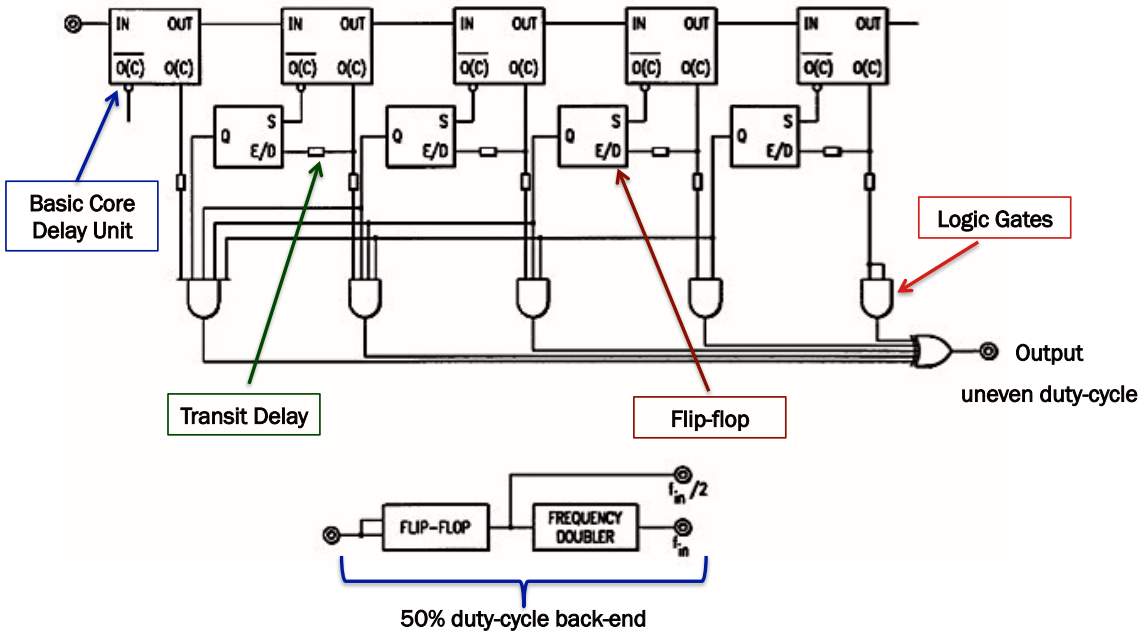


Figure 1. Time-domain jitter cleaner based on delay units [15].

can be achieved when the basic unit cell is cascaded, at the cost of reducing the operating frequency range. Even though the input signal is cleaned, this scheme has limited tracking capability [15]. Figure 1 shows a schematic of the delay-cell based jitter cleaner.

On the other hand, a PLL is a circuit that synchronizes an output signal (generated locally) with a reference or input signal in frequency as well as in phase. It can be used as a clock cleaner because it behaves as a highly selective tunable band-pass filter when is locked to that input signal. Hence, the PLL allows the PN of the reference signal to pass close to the carrier frequency, while the LO PN will dominate at large offset frequencies. The loop filter of the configuration defines the passband of the architecture, and therefore the transition point between the two PN profiles.

For a clock conditioner, the filter bandwidth should be narrow (without making the system unstable) to minimize the effect of the reference PN. A further reduction in the bandwidth is achieved by dividing the input signal, since the PLL bandwidth is directly related to the operating frequency, approach that has been used in industry [16].

Examples of PLL cleaning circuits are CDCL6010, CDCE62002, and CDCM61001 from Texas Instruments (TI). Product information indicates the possibility to choose between a bank of on-chip filter components and the use of a complete off-chip filter [17]. In the CDCE62002 device, not only the filter can be external, but also the dividers and the LO can be placed outside the chip [18]. Table 1 shows the achievable PN output employing a crystal LO interfaced with these integrated circuits (ICs).

Table 1. Example of PN performance for the TI CDCE62002 Jitter-cleaner [18].

Phase Noise for 25MHz Crystal Reference

Phase Noise Specifications under following configuration: VCO = 2000.00 MHz, AUX-REF = 25.00MHz, PFD Frequency = 25.00MHz, Charge Pump Current = 1.5mA Loop BW = 400kHz 3.3V and 25°C.					
Phase Noise at	**Reference 25.00MHz**	**LVPECL-HP 500.00MHz**	**LVDS-HP 250.00MHz**	**LVCMOS-HP 125.00MHz**	**UNIT**
10Hz	—	–72	–72	–79	dBc/Hz
100Hz	—	–97	–97	–103	dBc/Hz
1kHz	—	–111	–111	–118	dBc/Hz
10kHz	—	–120	–120	–126	dBc/Hz
100kHz	—	–124	–124	–130	dBc/Hz
1MHz	—	–136	–136	–142	dBc/Hz
10MHz	—	–147	–147	–151	dBc/Hz
20MHz	—	–148	–148	–151	dBc/Hz

As another example, National Semiconductor Corporation (NSC) presents two options for clock cleaners, the LMK03000 family based on one-PLL systems, and the LMK04000 family that includes a cascade-type PLL architecture. The LMK03000s use a similar approach to the TI ICs, but with passive loop filters to suppress the noise associated with active implementations. The LMK04000s aim for the reduction of the

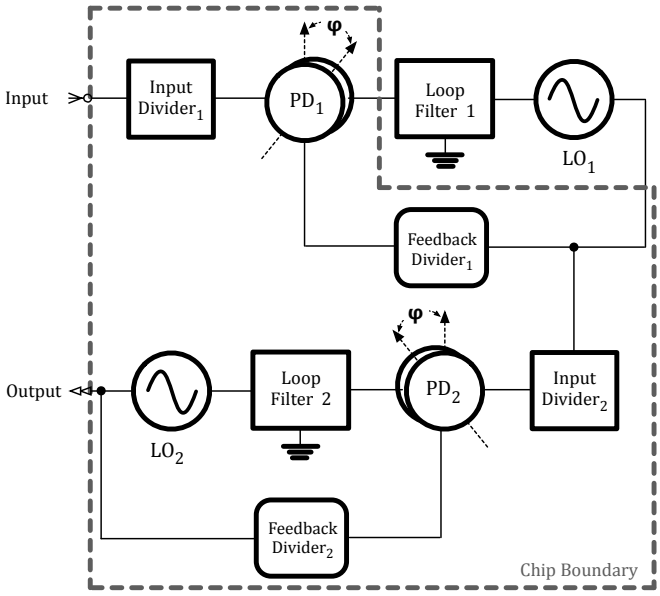


Figure 2. Dual-PLL architecture implemented in the NSC LMK04000s cleaners [3].

reference PN in two consecutive steps (Figure 2). In this approach, the input signal PN is divided into two regions, and each LO is utilized to address each section independently.

Since jitter cleaners have been dominated by PLLs with narrow loop-bandwidth, ultra-clean LOs have been the challenge for the feasibility of the different cleaner architectures. Figure 3 shows the performance between integrated and external LO and the two families of clock cleaners, and reveals that the best performance for both single and cascade options is obtained using a crystal (XTAL) LO.

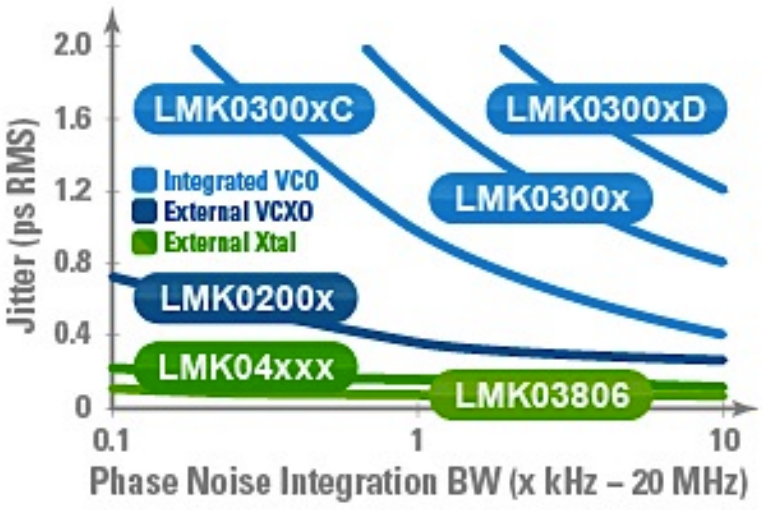


Figure 3. Comparison between single-PLL and cascade-PLL clock cleaner systems. The performance is highly dependent on a high quality LO [19].

Quartz crystals offer very-high quality factor (Q), but their large size does not allow practical integration with electronics in a single chip. MEMS devices have emerged as a viable alternative because they can be fabricated on silicon wafers similar to integrated circuits. MEMS resonators have proven to offer excellent noise performance close-to-carrier, but rather high PN floor [20]. It is important to notice that the effect of

fluctuations in temperature, adsorbing/desorbing molecules, outgassing, Brownian motion, Johnson noise, drive power and self-heating, and random vibration that are negligible in macroscopic resonators become large as the dimensions shrink [21]. Thus, successful insertion of MEMS devices into cost and power sensitive consumer applications requires tuning, trimming and compensation techniques [22].

Frequency pulling mechanisms have been proposed when a MEMS oscillator is intended for the reference signal (process-voltage-temperature variations) [23, 24]. However, if this oscillator is conceived as an LO, its gain will be highly limited. Frequency tuning is still a field of study because high quality is inversely proportional to tuning capability, and with increased LO gain usually the PN performance deteriorates.

A basic approach for a tunable MEMS LO consists in a switching architecture using a resonator bank with lithographically defined frequency offsets [25]. The PLL tuning-voltage is used to choose the appropriate resonator in the array. A flash ADC cn be used because enables fast switching time, which does not interfere with the loop dynamics; however, the resulting piecewise VCO gain will limit the frequency resolution (Figure 4).

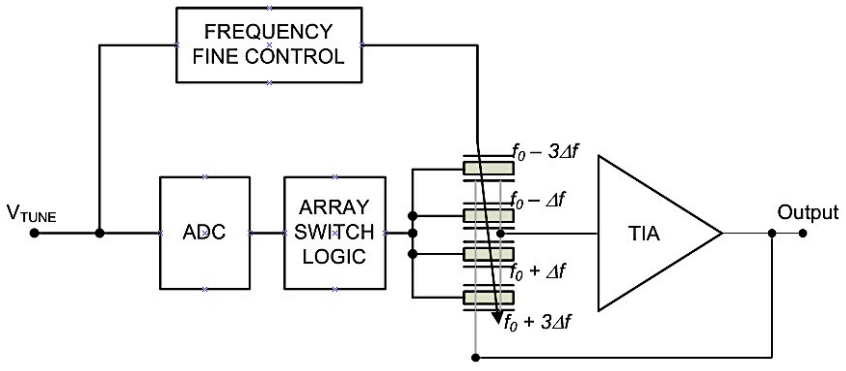


Figure 4. Approach for a MEMS-based VCO using a switching scheme.

Both frequency and quality factor of a MEMS resonator can have strong temperature and process dependencies. The uncompensated temperature coefficient of frequency (TCF) for a native silicon resonator is on the order of -30ppm/°C [26], which is greater than that of quartz resonators. Even though temperature variations must be compensated for reference oscillators, this characteristic allows another technique for a tunable MEMS LO known as micro-oven tuning, as presented in Figure 5 [27]. A DC current is passed through the body of the resonator to heat the structure inducing a frequency shift. Considering the given TCF, a total frequency tuning of ~3000 ppm is within reach when operating in the -20°C to 80°C temperature range [27]. The power consumption becomes a concern for the applicability of this technique.

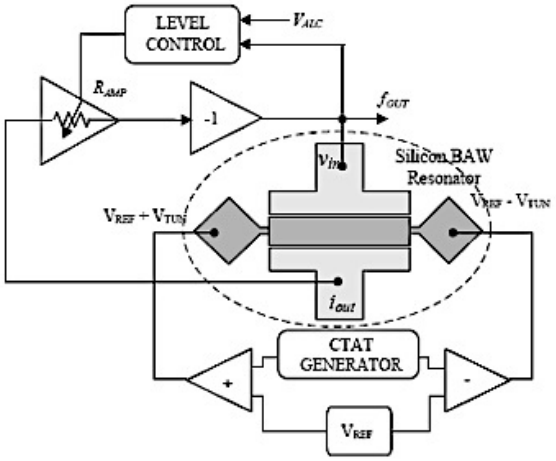


Figure 5. Block diagram of the oven-controlled frequency tuning [27].

1.3. Motivation

The distinguishing characteristic of a precision clock conditioner is the noise performance. Since a low-quality clock signal can be viewed as reference signal with

poor spectral purity, a clock cleaner can be viewed as a highly selective band-pass filter with frequency tracking capabilities.

In PLL-based clock conditioners, most of the noisy clock signal is filtered leaving the LO noise as the dominant contribution; therefore, jitter cleaner applications have more stringent requirements for the locally generated signal. Since a PLL has a pole at the origin (due to the integrating action of the LO), as the loop bandwidth is narrowed, the dominant pole associated with the filter moves to lower frequencies affecting the stability of the closed-loop system. As the bandwidth cannot be zero, some range of frequencies will exist for the input noise to pass unaffected through the configuration. As a result, a full-spectrum clock conditioning is necessary to address all the sections of the PN performance. In addition, it is desirable to have relaxed bandwidth requirements to favor system integration for cost and reliability.

This dissertation presents the Band-Reject Nested-PLL (BRN-PLL) as a mechanism to provide complete clock cleaning by introducing a notch in the transfer function for the noise of the input signal through inner and outer loops and a high-pass filter (HPF). This modified response simultaneously attenuates the reference-signal PN and reduces the size of the loop-filter capacitors. Ultra narrow loops are no longer required because the notch size is related to the system bandwidth. Additionally, this alternative configuration utilizes a combination of a MEMS VCO and an LC VCO to produce an ultra-clean output signal.

Given that the tuning method for LC VCOs is well-known and based on varactors, the development of frequency pulling options for MEMS-based VCOs needs to be addressed with minimum effect in the PN performance. In this research project two

methods are considered, the first strategy involves the addition of tunable elements to modify the resonance frequency, while the second one exploits the nonlinear behavior of a MEMS resonator while the operating phase is changed [8, 28].

This dissertation is organized in seven chapters that describe the step-by-step development of a full-spectrum clock cleaner. **CHAPTER 1** briefly introduces the approaches for clock-conditioning architectures and the motivation behind this work. It introduces the cascade-type PLL, a state-of-the-art configuration intended to provide an improved cleaning for clock signals. In addition, the cascade-type PLL will provide a testbench to compare the performance of the alternative scheme proposed in this work. Since both architectures are based on PLLs, a set of basic definitions is presented in **CHAPTER 2.** This chapter also introduces MEMS devices as a potential replacement for crystals in oscillators. The insight gained with the description about the design of an oscillator provides strategies for the implementation of a tunable oscillator using microresonators, but also the main challenges of this task are presented. Additionally, **CHAPTER 2** presents a simple set of tools that expedite the design of a full-spectrum clock cleaner using the same platform. **CHAPTER 3** addresses the stability of closed-loop schemes justifying the necessity of alternative architectures for complete clock cleaning. **CHAPTER 3** describes how the divider of a basic PLL can be modified to introduce a notch in the noise response of the input signal for attenuation, along with the corresponding effect in the response to other noise sources within the architecture. Therefore, the design of this new scheme is analyzed from a stability point of view. Once, the alternative system has been tested for stability, the design guidelines are also presented in **CHAPTER 3**. **CHAPTER 4** and **5** are devoted to the description of the

building blocks for the complete system (PFD, charge pump and VCOs). For the VCO treatment, **CHAPTER 4** explains the approach taken for the LC version of the tunable oscillator. On the other hand, **CHAPTER 5** presents the implementation of the two strategies proposed to generate a high-Q tunable MEMS oscillator, both series tuning and the modification of the phase in nonlinear regime. The MEMS device used in this work is described and characterized, so that the information derived from the resonator can be used in the selection of the suitable tuning mechanism and the design of the proposed clock-cleaner architecture. **CHAPTER 6** shows the set-up, test and results for two experiments with the proposed clock cleaner architecture. Finally, **CHAPTER 7** summarizes the research contributions and gives recommendations for future work in this field.

CHAPTER 2

PHASE-LOCKED LOOPS

BASIC DEFINITIONS AND BUILDING BLOCKS

A PLL is classified as digital when it contains a digital phase-detector (PD), an analog filter and a local oscillator (LO) (Figure 6). The LO is called voltage-controlled oscillator (VCO) when the controlling signal is a voltage. The digital PLL is a feedback system that maintains the phase error between the LO and the reference equal to zero or a constant. If the phase error increases, a control mechanism (tuning signal) acts on the LO to minimize the phase difference.

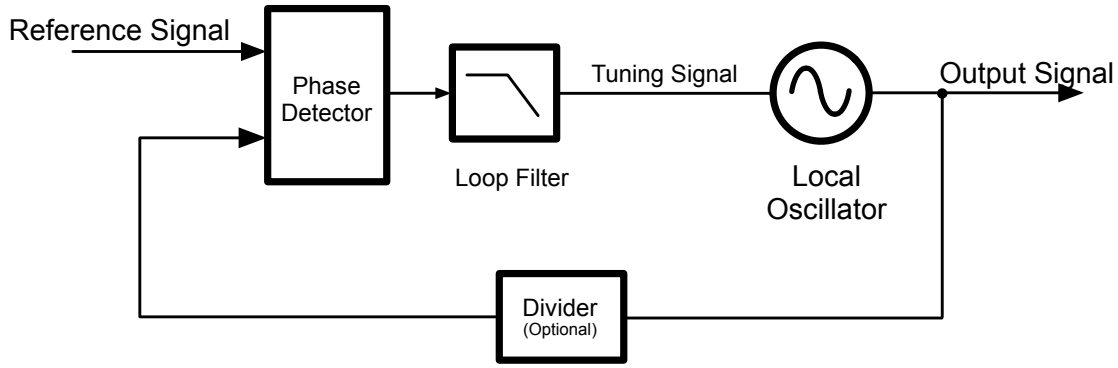


Figure 6. Basic Digital PLL Block Diagram

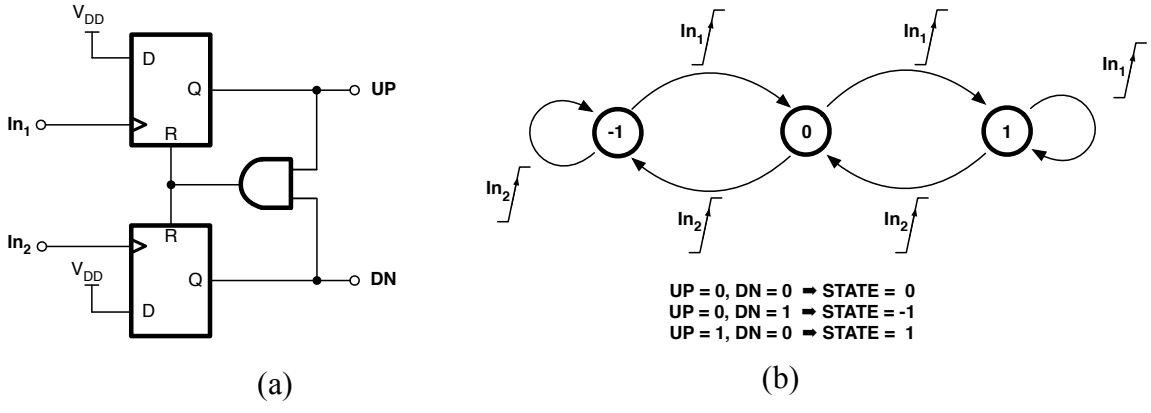
2.1. Basic Building Blocks

2.1.1. Phase-Frequency Detector and Charge Pump

Several options for a digital PD are available and based on characteristics such as operation speed, power consumption, duty-cycle independence, and capture range.

A PLL having a PD will lock only if the frequency error is small; however, the time required to match frequency and phase could be exponentially large (i.e. months, years). An auxiliary frequency discriminator can be used to pull the VCO frequency helping the locking process. A phase-frequency detector (PFD) is a type of PD with embedded frequency detection capabilities, and the basic implementation is built with a *triflop*, which is configured with two flip-flops and an AND gate in feedback configuration (Figure 7a) [1].

When the signal applied to the port In_1 leads (higher frequency) the one applied to the port In_2, the PFD sets the 'UP' port while resets the 'DN' (down) port. If the signal applied to the port In_1 lags (lower frequency) the one applied to the port In_2, the PFD resets 'UP' and sets 'DN'. Finally, if frequency and phase match, the PFD resets both ports. Only three states are allowed, since a reset signal is applied to the flip-flops for the "11" case (Figure 7b).



(a) (b)

Figure 7. PFD based on a triflop digital circuit. The AND gate disables the "11" possibility in the architecture.

The output generated by the PFD is not suitable for the next block, the loop filter. A charge-pump (CP) is a three-position current switch that can be used as an interface stage (Figure 8) [29]. When the UP (DN) position is set, a pump current is delivered (extracted) to (from) the loop filter. Otherwise, the switches are open isolating it. When a CP is used, the loop filter must work as a transresistance network and provide the required compensation for PLL stability.

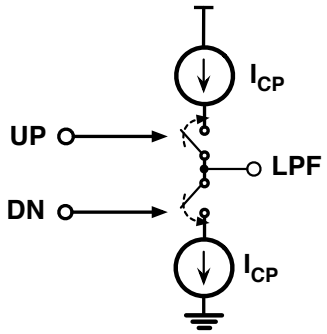


Figure 8. CP modeled as a three-position electronic switch.

Ideally, the case UP=1/DN=1 does not appear in the structure; however, due to the transit delay through the AND gate, this state will be present for some instant interacting with the CP. Although it can be thought as a disadvantage; actually, this behavior can be used to eliminate a more harmful problem known as the dead-band zone [6]. The dead-band zone is defined as a range of small phase differences where the PFD is not able to generate any information for correction.

The smallest phase error that the PFD is capable of sensing depends on the rising

and falling times resulting from the total capacitance at the PFD outputs. For example, if the signal In_1 leads closely the signal In_2, the UP pulse could not have enough time to surpass the established threshold level that activates the required switch of the current-based interface block. Thus, the CP injects no current, which does not produce the command for correction contributing to jitter [6] (Figure 9a). When the short pulses due to the UP=1/DN=1 case are present, the switches are considered to be precharged, and any small difference can be detected and processed by the CP [6] (Figure 11b). When the PLL is locked, the voltage converted by the transresistance loop-filter will not change only if the UP and DN currents are matched.

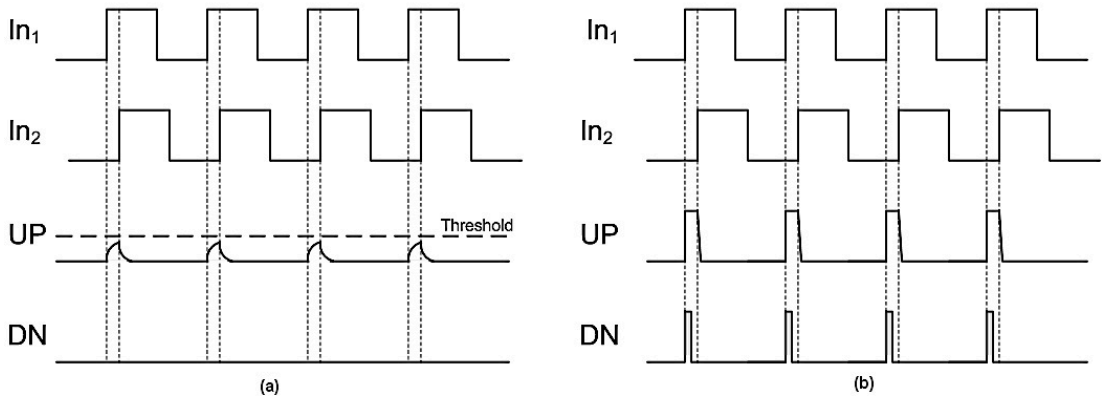


Figure 9. Ideal PFD: without and with load capacitance.

When the two currents are not equal, the output spectrum exhibits spurious tones due to a nonlinear term associated with the difference between the pumping and sinking currents and the phase error at the PFD [30]. Such behavior becomes progressively worse when the PLL is intended for fractional frequency. This problem can be alleviated with the injection of a controlled amount of additional current each time a correction pulse is

generated (Figure 10) [30], which compared to the traditional CP of Figure 8 constrains the nonlinear term to only fabrication mismatch. To use this linearization technique, the PFD must be modified to produce the two additional control signals UPED and DPED. Figure 11 presents the alternative architecture [30].

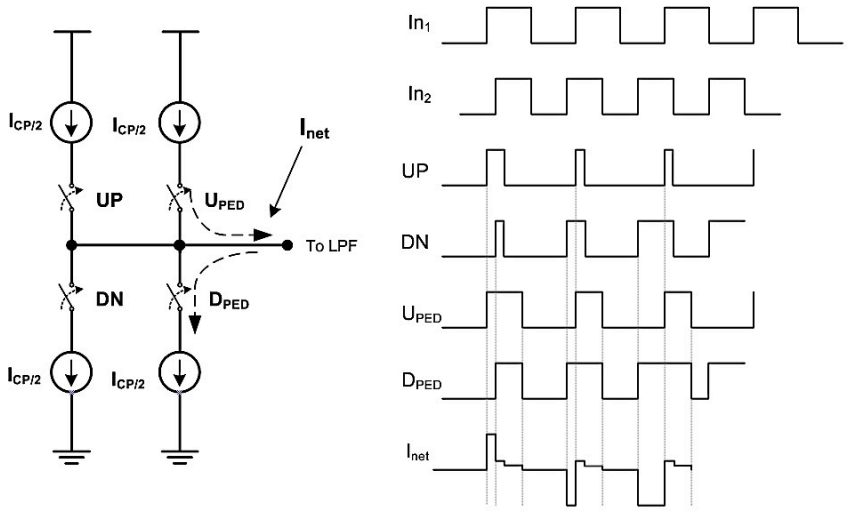


Figure 10. CP linearization technique using a controlled amount of injected current [30].

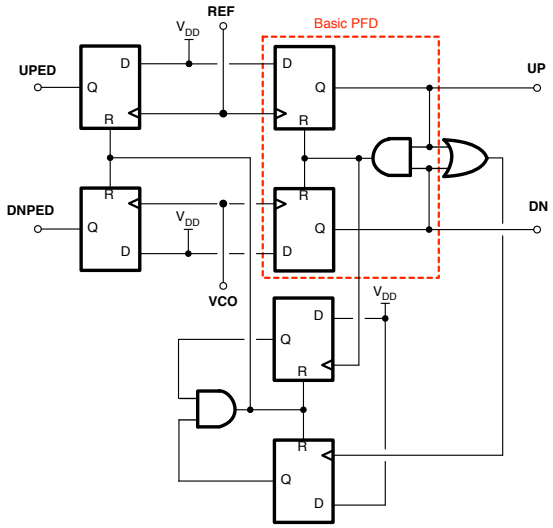


Figure 11. Modified architecture for the PFD-CP to use the CP linearization scheme [30].

2.1.2. Voltage-Controlled Oscillator (VCO)

A VCO is a circuit whose frequency is a linear function of a controlling voltage expressed as

$$\omega = \omega_0 + K_{VCO} \cdot V_{control}, \tag{1}$$

where ω_0 represents the free-running frequency and K_{VCO} is the gain or sensitivity in rad/s/V. The tuning range is defined as the span of ω.

As in the case of any other oscillator, spectrum purity quantified in terms of jitter or PN is an important parameter determined by the requirements of a particular application. For this work, excellent noise performance is highly desirable because the tunable LO will determine the output PN of the generated clock. Improving the PN can come from resonators with high Q and/or a large output oscillation amplitude to make the waveform less sensitive to noise as predicted by [31]. Others aspects such as center frequency, tuning range and power consumption will be directly dictated by the system specifications. Finally, tuning linearity, supply and common-mode rejection will control the linearity and the sensitivity of the LO gain. This dissertation focuses in two types of VCO, MEMS-based and the LC-based tunable oscillators.

2.1.2.1 MEMS-based VCO

A crystal is a piezoelectric material that exhibits electromechanical resonance that is very stable (with time and temperature) and highly selective (very-high Q). The circuit symbol and its basic equivalent circuit are presented in Figure 12. Given the high Q of the crystal, the resonance properties are characterized by a large inductance L_s, a very small series capacitance C_s, a series resistance R_s, and a parallel capacitance C_p.

Capacitor C_p represents the electrostatic capacitance between the two parallel plates of the crystal. Notice that $C_p >> C_s$.

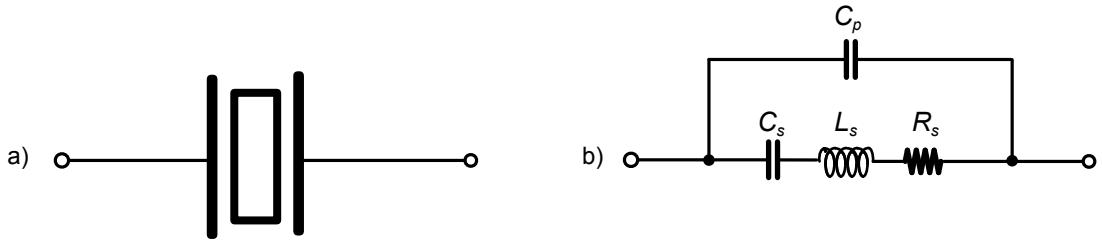


Figure 12. Crystal resonator: a) circuit symbol and b) equivalent circuit

Assuming a very-high Q, R_s can be neglected so that the equivalent impedance of the crystal can be expressed as

$$Z(s) = 1\Big/\left[sC_p + \frac{1}{sL_s + 1/sC_s}\right] = \frac{1}{sC_p}\frac{s^2 + \left(1/L_sC_s\right)}{s^2 + \left[\left(C_p + C_s\right)/L_sC_sC_p\right]}, \tag{2}$$

which indicates that the crystal device has two resonance frequencies: a series resonance at ω_s,

$$\omega_s = 1\Big/\sqrt{L_sC_s} \tag{3}$$

and a parallel resonance at ω_p,

$$\omega_p = 1\Big/\sqrt{L_s\left(\frac{C_sC_p}{C_s + C_p}\right)}. \tag{4}$$

Equations 3 and 4 show that $\omega_p > \omega_s$; however, since $C_p >> C_s$, the two resonance frequencies are very close to each other. Expressing s as $j\omega$, the equivalent impedance of

Equation 2 can be expressed as $Z(j\omega) = jX(\omega)$, which produces an inductive reactance over the very narrow frequency band between ω_s and ω_p as observed in Figure 13.

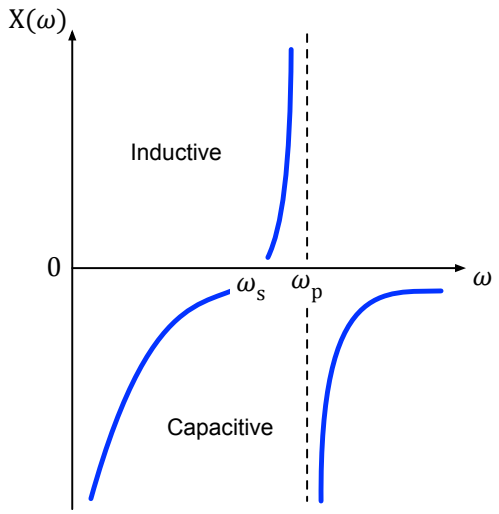


Figure 13. Crystal reactance vs. frequency.

Figure 13 shows that the crystal reactance can be used to replace the inductor of a Colpitts oscillator (Figure 14a) [32]. The resulting circuit (Figure 14b) will oscillate at the resonance frequency of the crystal inductance L_s with the series equivalent of C_s and

$$C_p + \frac{C_1 C_2}{C_1 + C_2}. \tag{5}$$

Since C_s is much smaller than the other three capacitances, it will be dominant and the oscillation frequency becomes

$$\omega_{osc} \approx 1/\sqrt{L_s C_s} = \omega_s, \tag{6}$$

which implies that the crystal can be consider as a series resonance device for building oscillators.

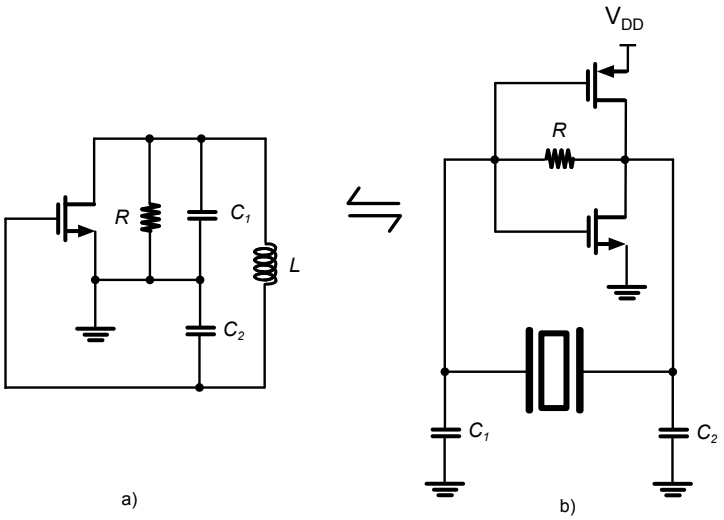


Figure 14. a) Basic Colpitts configuration b) using a crystal as an inductor replacement

The architecture of Figure 14a can be implemented as well as a shunt-shunt feedback amplifier interfacing a resonator in a closed-loop configuration as shown in Figure 14b. Considering steady state, if at a specific frequency ω_o, the loop gain exhibits no losses and the total phase equals $n \cdot 2\pi$, the system will amplify its own noise and will produce a finite output for a zero input signal. This condition is known as the Barkhausen criterion [33].

Thus, the basic MEMS-based oscillator uses a micromechanical resonator as a crystal replacement. The analysis approach as shunt-shunt amplifier is preferred because the input and output impedances are decreased to minimize Q degradation with loading [23].

Because both the frequency and Q of a micromechanical device have strong temperature and process dependencies, effective crystal replacement requires additional compensation schemes. To compensate for temperature and process sensitivity, both system level [34] and device level [27], [35] techniques have been proposed with system-level techniques being used in existing products.

In addition, the frequency of MEMS resonators is also dependent on the physical dimensions of the vibrating structure, which causes the resonance to deviate from a designed target value due to variations in photolithography, etching and film thicknesses. Therefore, adding a frequency-tuning network is required to pull the frequency, so that the resonance can be brought back to the intended value (Figure 15). Frequency tuning strategies can also be made at device or sustaining-amplifier level.

When electronics-level tuning is selected as pulling mechanism, the resonance frequency of a high-Q resonator becomes hard to modify with low-Q tunable elements, while maintaining the quality of the resonance frequency. Thus, the design of a MEMS-based LO becomes the main challenge for integration of high-performance clock cleaners.

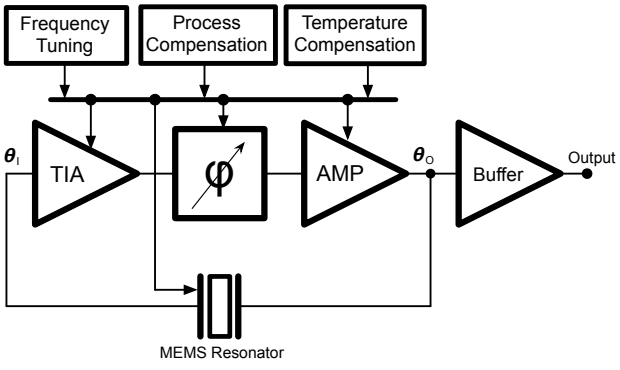


Figure 15. Block diagram for a MEMS oscillator.

MEMS Resonators

MEMS resonators are vibrating mechanical devices that can use IC processes to favor size and integration allowing a cost-effective high-*Q* solution for high performance systems. Acoustic waves are generated in silicon devices by using electrostatic transducers (capacitive) or thin films of piezoelectric materials such as aluminum nitride (AlN). Figure 16 shows images of microresonators using both types of transducers.

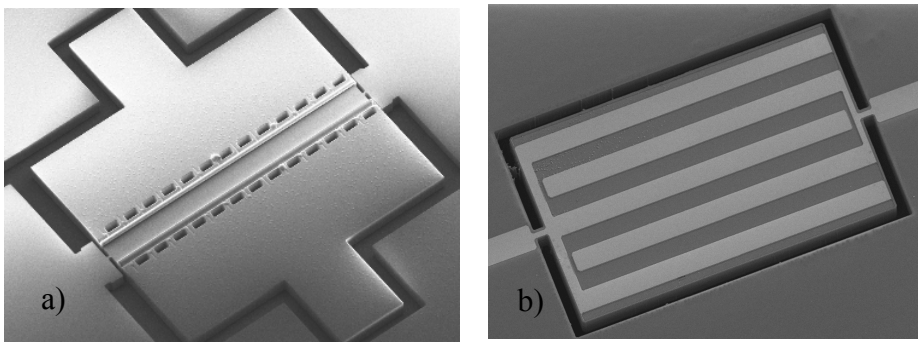


Figure 16. Micrographs of MEMS resonators: a) electrostatically and b) piezoelectrically transduced devices

Microresonators can be designed to operate in different acoustic modes, such as transverse flexural wave (TFW) [36], bulk acoustic wave (BAW) [26], and surface acoustic wave (SAW) [37]. TFW is most suitable for low frequency resonators (tens of kHz to low MHz) and the frequency typically depends on at least two geometrical dimensions of the device (e.g., thickness and length). On the other hand, BAW resonators are more convenient for higher frequency applications and have frequencies

primarily defined by a single geometrical dimension, for example, the thickness of the piezoelectric film [38] or the width of the resonator body [39].

A thin film of a piezoelectric material can be deposited on the surface of a silicon resonator to excite a lateral BAW mode through the transverse piezoelectric coefficient [39]. The thickness of the silicon layer is typically chosen to be much thicker than that of the piezoelectric layer, so that the resonator frequency is predominantly determined by silicon [40]. The superior acoustic properties of this material translate to very high-Q factors and large power handling [41]. The large electromechanical coupling of the thin film piezoelectric material results in a low motional impedance for these devices.

A MEMS resonator can be modeled as a two-port admittance network Y_{21} in which the applied voltage is v_1 and the output motional current is i_2. There are three components to the admittance Y_{21}, the input transduction, the mechanical response, and the output transduction. For piezoelectric devices, the admittance has the same form as the one of a series RLC resonator. The equivalent model is presented in Figure 17, where η_1 and η_2 are the input and output electro-mechanical coupling coefficients [42].

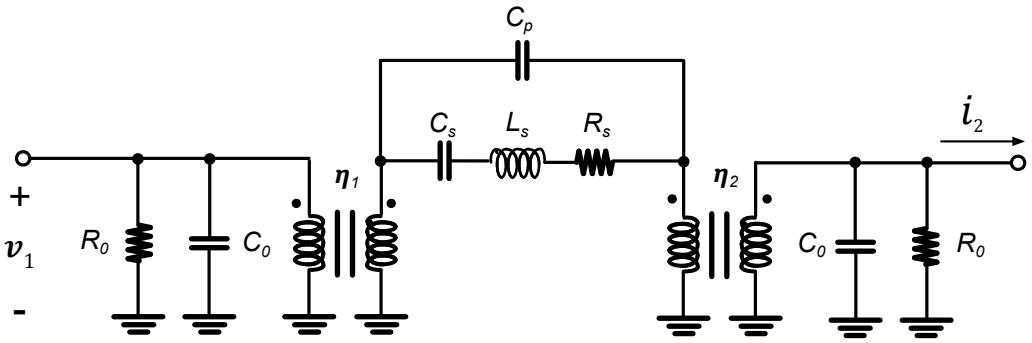


Figure 17. Equivalent lumped element model for a MEMS resonator in two-port operation [42].

When the input and output transformers are symmetric $\eta_1 = \eta_2$, the parameters RLC can be expressed as:

$$R_s = \frac{k_n}{\omega Q \eta_1 \eta_2},\ L_s = \frac{m_n}{\eta_1 \eta_2}, C_s = \frac{\eta_1 \eta_2}{k_n}, \tag{7}$$

where m_n, c_n and k_n are the effective modal mass, damping, and stiffness, respectively. A more detailed description and procedure to determine the values for the lumped element model can be found in [42].

When measured data is available, for example via S-parameters taken with a vector network analyzer (VNA) with 50Ω termination, the parameters for the RLC model can be approximated with the following equations:

$$R_s = \frac{100}{10^{\frac{IL}{20}}} - 100, \tag{8}$$

$$C_s = \frac{1}{2\pi f_s R_s Q}, \tag{9}$$

$$L_s = \frac{R_s Q}{2\pi f_s}, \tag{10}$$

where *IL* corresponds to the insertion losses exhibited by the resonator in dB.

Equation 10 reveals that the high-*Q* mechanical resonance for a MEMS device leads to a lumped-element model with small value for C_s, and a similar situation occurs when the operating frequency is increased. Thus, it can be concluded that connecting a tunable capacitor in series with the resonator, a series-impedance equivalent is produced equal to the smallest between C_s and the tunable element (C_{var}). If C_s dominates, the tuning is minimum. However, the scenario worsens when parasitics are considered in the total resonance-frequency estimation.

Tuning Strategies

A tuning mechanism can be obtained when a variable capacitor is placed in series with the MEMS device as shown in Figure 18. Neglecting the feedthrough capacitance C_p and shunt-parasitic capacitances C_0, the expression for the series resonance peak becomes

$$\omega_s \approx \sqrt{\frac{1}{L_s \cdot \frac{C_s \cdot C_{var}}{2C_s + C_{var}}}}. \tag{11}$$

Equation 11 reveals that the effect of the tuning strategy is minimized as the value of C_s decreases, which is the case for high-Q resonators. Thus, from C_{var} point of view, selecting low varactor-capacitance values (but looking for a large capacitance change), the effect of series pulling is maximized. From an equivalent impedance point of view, two varactors (one per side of the resonator) produce a combined effect of halving the value of C_{var}.

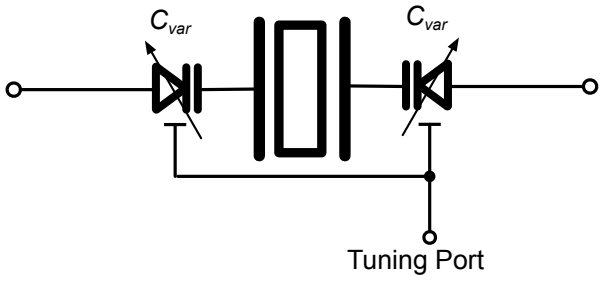


Figure 18. MEMS Resonator with series varactors to configure a MEMS-based tunable oscillator.

However, modeling of MEMS devices indicates that actual resonators require at least the inclusion of both feedthrough capacitance C_p and shunt-parasitic capacitances C_0 that will affect the definition of Equation 11. On one side, C_p is very small (<50fF) and its effect can still be neglected in the tuning range estimation; but, on the other hand, C_0 can be large (≈ 1pF) deteriorating the tuning range considerably. Large values for C_0 are obtained due to an increased transduction area to reduce the motional resistance (R_s) of the resonator.

To calculate the tuning, when only C_0 is considered, the equivalent circuit to determine the resonator impedance can be simplified as shown in Figure 19.

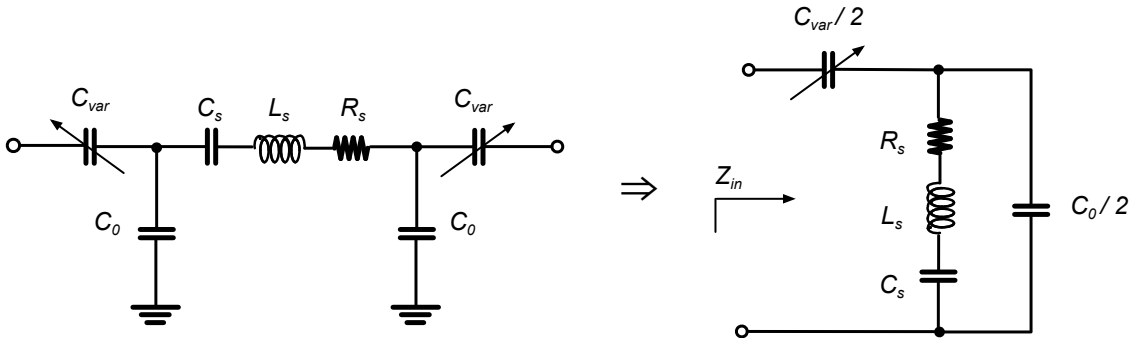


Figure 19. Equivalent resonator to calculate the impedance of the resonator

As observed, the shunt-parasitic capacitances appear in parallel with the series-resonance tank creating anti-resonance. Figure 19 reveals that the signal path given by C_0 becomes preferred compared to the one through the resonator. Even, at the case of series resonance where the impedances of L_s and C_s cancel out, the motional impedance R_s could not dominate if the impedance $2/\omega_{res}C_0$ is comparable. This last observation is

demonstrating that, also from a phase point of view, the effect of the angle of the shunt-parasitic capacitance will deviate the series resonance phase-shift from the expected value (0° or 180°). Phase-shifting capabilities in the oscillator loop are then required to satisfy Barkhausen criterion.

The expression for the series-resonance frequency, given the conditions displayed in Figure 19, becomes

$$\omega_s \approx \sqrt{\frac{1}{L_s \frac{C_s\left(C_0 + C_{var}\right)}{2C_s + C_0 + C_{var}}}}. \tag{12}$$

Equation 12 shows that if C_0 dominates both C_s and C_{var}, the resonance frequency equals $1/\sqrt{L_s C_s}$, and the pulling provided by C_{var} will have negligible effect. Since high-Q resonators have small C_s, the effect of the shunt-parasitic capacitances needs to be eliminated, so that the variable capacitor in series could apply some pulling to the frequency, and the expected tuning can still be estimated using Equation 11. Electronic compensation can be only targeted for a specific band of frequencies.

Inductors can be used to cancel the parasitic capacitances via resonance. Two additional tank circuits (one per shunt-parasitic capacitance) appear when the inductors are connected in parallel with the shunt capacitances. It can be observed that these two tank circuits will appear in parallel with the RLC tank of the resonator when the equivalent impedance is determined, as shown in Figure 20.

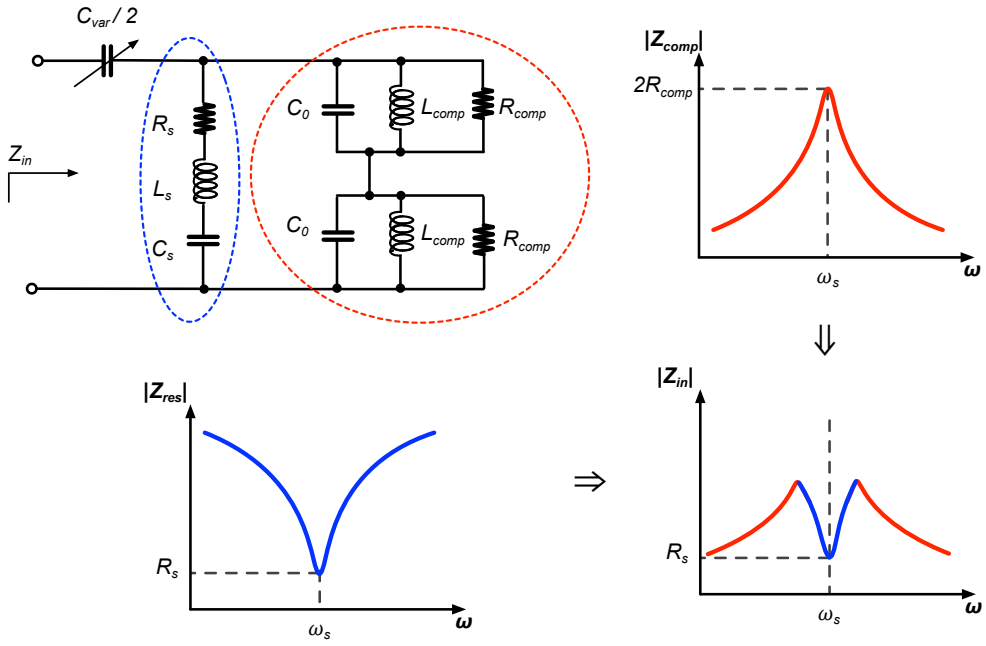


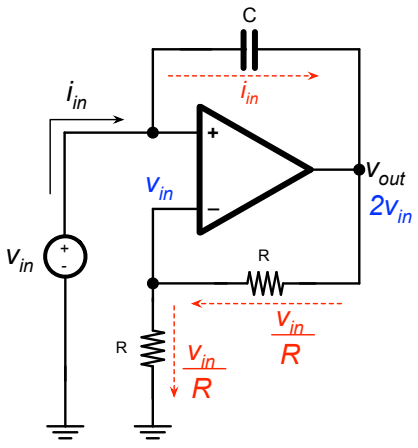
Figure 20. Equivalent resonator to calculate the impedance of the resonator.

Figure 20 shows the behavior of the *compensation tanks* from an impedance approach. The maximum value will equal the total losses (i.e. R_{comp} per tank), and analyzing how the signal current will flow through the circuit, the total impedance will exhibit he behavior displayed in the curve shown in the bottom-right corner of Figure 20. If the maximum resistance of the compensation tanks is selected at ω_s, then the signal current will prefer to follow the resonator path.

Thus, it can be observed that this compensation method will work properly if the resonance of the compensation tanks occurs at exactly ω_s; otherwise, the maximum impedance will not be appearing in parallel with the resonator increasing the insertion losses, as well as a phase shift from shunt-parasitic capacitances not fully compensated.

Additionally, it can be observed that the Q of the compensation tanks (Q_{comp}) defines the frequency range of the cancellation technique and the insertion losses of the complete resonator. If Q_{comp} is selected high, the losses of the total system at resonance will be dominated mostly by the resonator motional impedance, but the available frequency range for compensation will be reduced limiting the tuning. The latter condition could be considered irrelevant if the value of the varactors is not comparable to C_s.

An alternative compensation for the shunt-parasitic capacitances using active circuits comes in the form of a negative capacitor. Generation of a negative component requires positive feedback, and the circuit in charge of this operation is known as negative impedance converter (NIC). A NIC develops an inversion between the current and voltage applied to a circuit element. Figure 21 describes the basic operational-amplifier (OP-AMP) implementation of a NIC targeting a capacitor to generate its algebraic negative. It can be inferred that negative-capacitor compensation does not suffer from the limited band of operation as occurs in the active-inductor approach.



$$-v_{in} + i_{in} \cdot \left(1/sC\right) + v_{out} = 0$$
$$-v_{in} + i_{in} \cdot \left(1/sC\right) + 2v_{in} = 0$$
$$i_{in} \cdot \left(1/sC\right) + v_{in} = 0$$
$$Z_{in} = -\left(1/sC\right)$$

Figure 21. Basic NIC OP-AMP implementation.

However, series tuning is not the only available option to configure a MEMS VCO. Changing the total phase-shift provided by the sustaining amplifier can be used to modify the oscillator frequency. From Figure 15, if the gain of the loop (TIA + AMP) is enough to overcome the losses of the resonator (R_s), then a phase shifter can be used to provide tuning (Figure 22).

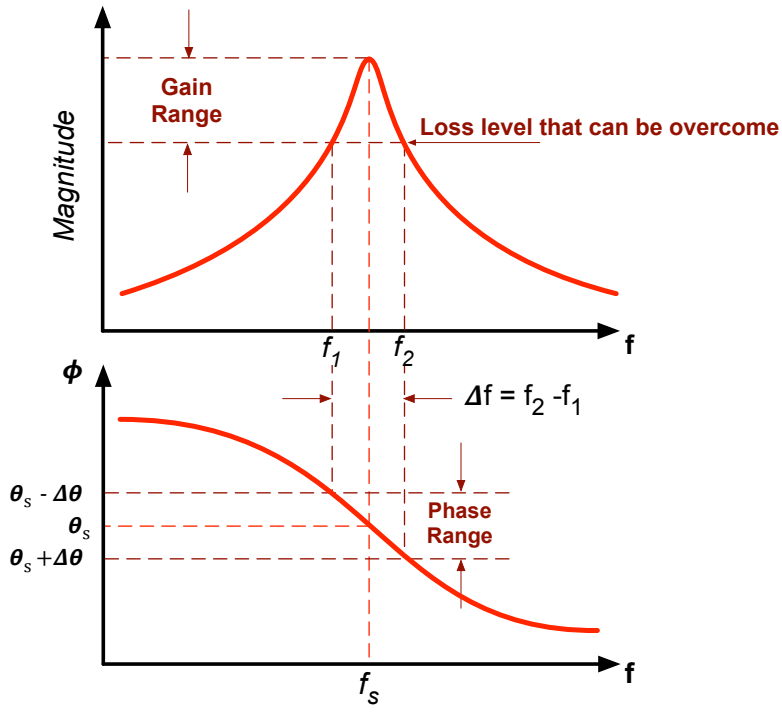


Figure 22. Phase-shift as a tuning mechanism for a MEMS-based oscillator.

The sustaining-amplifier phase determines the operating point of the system, and the phase of the output waveform remains constant when perturbations within the system are not considered. Thus, the spectrum of the oscillating signal is equal to that of a Dirac

function. However, the noise of the sustaining amplifier propagates through the closed-loop system and, having amplitude and phase components, will perturb the generated waveform broadening its spectrum.

If the noise sources are considered small signals [43], a slope can be defined at the vicinity of the operating point linearizing the phase-frequency relationship locally. Determining this slope corresponds to the definition of *open-loop Q* [44], and it is a measurement of how much the closed-loop system opposes variations in the oscillation frequency. Hence, it can be concluded that when the operating point deviates from the device resonance peak (where the slope is maximum), the noise perturbations will have a more pronounced effect deteriorating the oscillator PN.

Although at first glance, the phase-shift technique can appear to affect negatively the oscillator performance, the scenario changes completely when the resonator, and therefore the frequency-phase transfer function, exhibits nonlinearity. The advantage of the nonlinear regime is the ability to desensitize the oscillator frequency with respect to induced phase variations due to an increased value of the operating slope.

2.1.2.2. LC-based VCO

An inductor L placed in parallel with a capacitor C resonates at a frequency equal to $1/\sqrt{(LC)}$. At this frequency, the impedances of the inductor and the capacitor are equal and opposite producing the equivalent impedance to go to infinity, which is analogous to an infinite Q for the oscillator. In a real scenario, both L and C have losses that lower the quality factor. If the losses of this tank circuit are modeled by a resistor in parallel R_p, and the equivalent parallel impedance is plotted with respect to frequency, it can be

observed a well defined resonance peak in the magnitude, while the phase ranges from +90° to -90°.

At low frequencies, the reactance due to the inductor appears as the preferred path for the current and therefore the tank exhibits an inductive behavior (+90°). As the frequency is increased and the reactances of inductor and capacitor cancel each other, the tank circuit becomes a resistor, and the voltage and current will be in-phase. Finally, at higher frequencies, the capacitive behavior dominates and the tank circuit exhibits -90° phase-shift between voltage and current.

If the tank circuit is connected as a load for a common-source (CS) stage, and the output is connected to the input, the total phase-shift around the loop will be 180°, which does not satisfy Barkhausen criterion. When two CS stages (i.e. tuned stages) are cascaded, the required 360° phase-shift can be reached when the loop is closed, and the circuit can oscillate only if the losses of the two tank circuits are overcome by the active devices. The cascaded configuration can be re-drawn as the cross-coupled architecture shown in Figure 23 [6].

The cross-coupled configuration emulates a negative resistance due to positive feedback and its value is approximately $-2/g_m$, becoming a measure of the losses that the active circuitry is able to cancel.

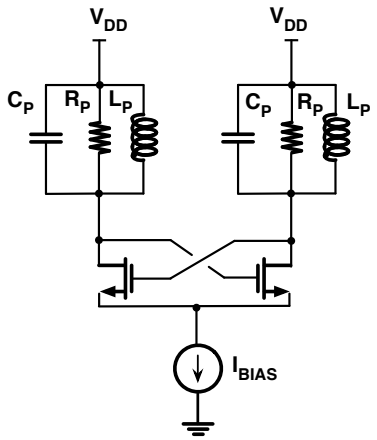


Figure 23. Crossed-Coupled topology for the generation of a negative-resistance-based oscillator [6].

From a noise behavior point of view, the noise factor *F* of an LC oscillator is equal to the total oscillator PN normalized to the PN due to the resonator loss [45]. In an ideal LC oscillator, the noise factor is equal to one if the tank is lossless. However, with a lossy tank circuit, the noise of the cross-coupled configuration is equal but uncorrelated to the noise in the resonator loss. This fact gives rise to a noise factor of 2, the sum of the unity noise factors of both tank circuits in the LC oscillator. In practice, the cross-coupled pair is comprised of nonlinear active devices; therefore, the noise factor of the whole oscillator becomes 1+ ϒ, where ϒ is the noise factor of the nonlinear active circuit [45]. In any case, the LC oscillator exhibits minimum noise factor, which makes it suitable for low-noise floor applications.

Thus, to improve the overall performance of this oscillator, the *Q* of the tank circuit must be maximized and the bias circuitry of the oscillator must be designed to provide low noise. Since capacitors with high *Q* are available in IC fabrication processes, the series resistor of the inductor will determine the PN performance as well as the output power.

Additionally, the tail current noise has been identified as an important contributor to the oscillator PN, since it is built with active devices. The switching differential pair acts as a single-balanced mixer for the current-source noise, which upconverts low-noise frequencies around the oscillation frequency. Since the LC oscillator is a balanced circuit, odd harmonics circulate in a differential path, while even harmonics flow in a common-mode path through the cross-coupled pair. Hence, filtering the noise due to the tail current can be made using a capacitor in parallel [45, 46]. Literature suggests also the complete removal of the current source and the use of a passive-resistive network [7].

Due to the fact that the tank circuit is connected directly to the power supply, the resonator will have one of its terminals to AC ground, which allows using varactors as tuning elements. The varactor *Q* usually is higher than that of the inductors. Filtering of the tuning port can be considered to improve the performance of the tunable oscillator as well. Figure 24 summarizes the noise-oriented design for an LC oscillator.

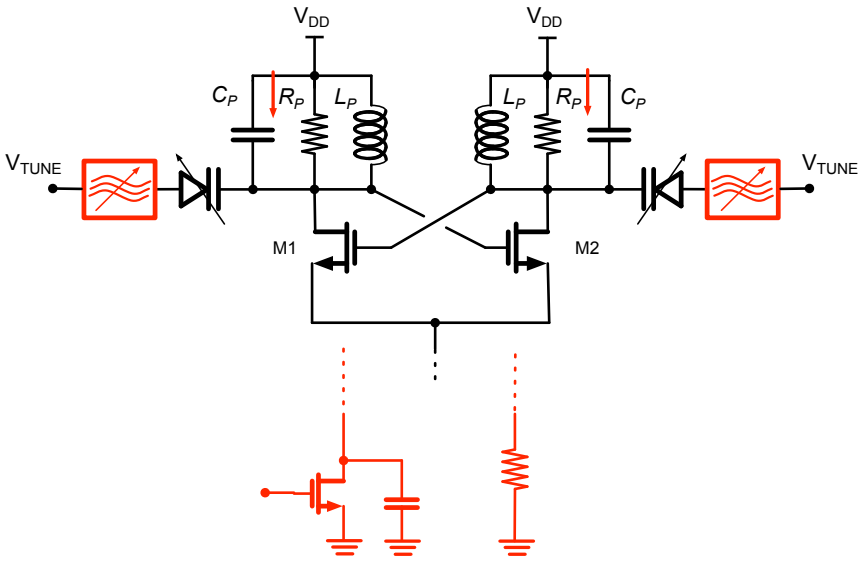


Figure 24. Noise-oriented design for an LC oscillator based on the crossed-coupled topology

2.2. Simulation Models For PLL-Based Systems

This dissertation describes a kit covering the design stages of a PLL using the simulation tool Spectre. The simulator selection is based on the fact that Cadence contains complete analog libraries (lumped elements) and supports Verilog-A as hardware description language. Following [5, 14], Verilog-A files are used to predict the PN performance using phase models. Basic analyses (AC and transient) will be used for stability and the estimation of the noise transfer-functions of a PLL-based system.

2.2.1. Model for Pole-Zero Analysis at Steady State

The Nyquist stability criterion is used as the primary strategy for the loop-filter design in a PLL. To apply the criterion, the closed-loop architecture is linearized around its operating point and considered as a continuous-time system at steady state. Determining parameters such as the LO and PD gains, the open-loop expression is utilized to locate the zeros and poles that allow a stable operation once the scheme is closed.

A generic open-loop expression is presented as

$$GH_{INNER}(s) = \frac{K_{\phi} \cdot K_{VCO} \cdot LPF(s)}{s \cdot N}, \tag{13}$$

where K_{ϕ} is the PD gain, K_{VCO} is the LO gain and N is the value of the divider. For this project, the PD is selected as a phase-frequency detector (PFD), and the LO as VCO without loss of generality.

The phase is emulated with an AC voltage source to build a stability model based on lumped elements. Then, the PFD-CP is modeled with a voltage-controlled current source whose gain equals K_{ϕ} (A/rad). Since the variable at the PFD-CP block output is

current; resistors, capacitors, and voltage-controlled voltage sources (to model OP-AMPs) can be used to describe the loop filter, whose output variable will be the tuning voltage that controls the VCO.

Next, for the VCO modeling, the gain units (rad/s/V) indicate that employing a voltage-controlled current source only produces frequency; therefore, integration is required to generate the desired physical quantity (phase). A capacitor provides such relationship in the following form

$$v(t) = \frac{1}{C}\int i(t)\,dt \xrightarrow{L} V(s) = \frac{1}{C}\frac{1}{s}I(s) \ , \tag{14}$$

when the value of the capacitor equals 1 F. Hence, a proper model for the VCO is presented in Figure 25. The voltage-controlled voltage source at the output prevents loading of the current source that otherwise modifies the intended integration.

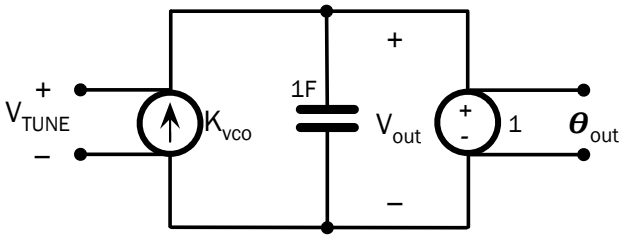


Figure 25. Lumped-element model for a VCO. The capacitor realizes the integration over the frequency to obtain the phase, which is emulated as a voltage.

Finally, as the divider uses the phase as input and output variables, a voltage-controlled voltage source provides a suitable model for this component.

To analyze the PLL stability, AC analysis is run on the open-loop model to generate the corresponding Bode plots to estimate the phase margin. Figure 26 shows an

example of the model for a PFD-CP-based PLL using a third-order loop filter [47]. It is possible to combine the buffer at the VCO output and the divider in one component.

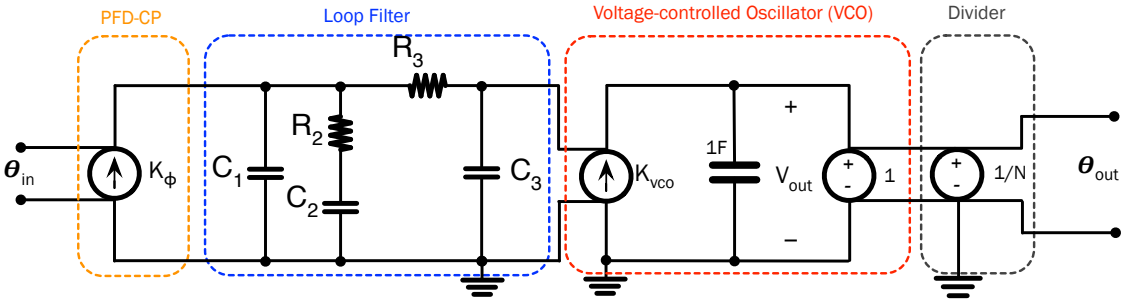


Figure 26. Lumped-element circuit model for a fourth-order PLL.

2.2.2. Model for Noise Transfer Functions

A PLL is a system that exhibits different behavior depending on the noise of the associated building block being considered. When the one-side noise transfer functions [48] are utilized, the PLL acts as a low-pass filter for the noise of the input signal, and as a high-pass filter for the noise of the LO. Additionally, the PLL presents a low-pass behavior with gain for the CP current noise.

To extract the transfer functions for the building blocks, the model described in Section 2.2.1 can be extended as follows. First, the PLL is configured as a closed-loop system through a block called *difference*. Using a voltage-controlled voltage source as an OP-AMP, the required arithmetic operation can be realized as shown in Figure 27a.

Once *difference* closes the loop using negative feedback, the Bode plot for the reference-noise transfer function is obtained at the output of the total system for an AC voltage applied to the input. For the VCO phase-noise, an AC voltage source will model

this perturbation, and it must be added after the integration prior to the output (Figure 28a). Therefore, a similar component to *difference* but with two adding inputs is required. Figure 27b depicts the *addition* block. The associated transfer function is plotted at the output of the system with only the VCO phase-noise activated (i.e. the reference terminal zeroed). Finally, the transfer function with respect to the CP current noise can be obtained by adding a voltage-controlled current source at the same node of the current source that models K_ϕ. The output current will add by KCL as shown in Figure 28b. Generation of the corresponding Bode plot requires zeroing both reference and VCO noise sources.

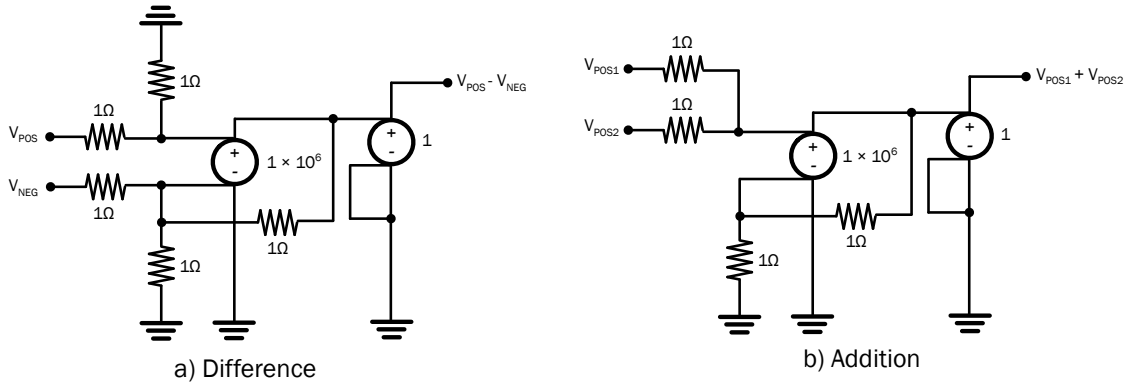


Figure 27. Lumped-element model for the difference and addition blocks. The first one allows the configuration of the closed-loop configuration; the latter enables the addition of the VCO phase noise.

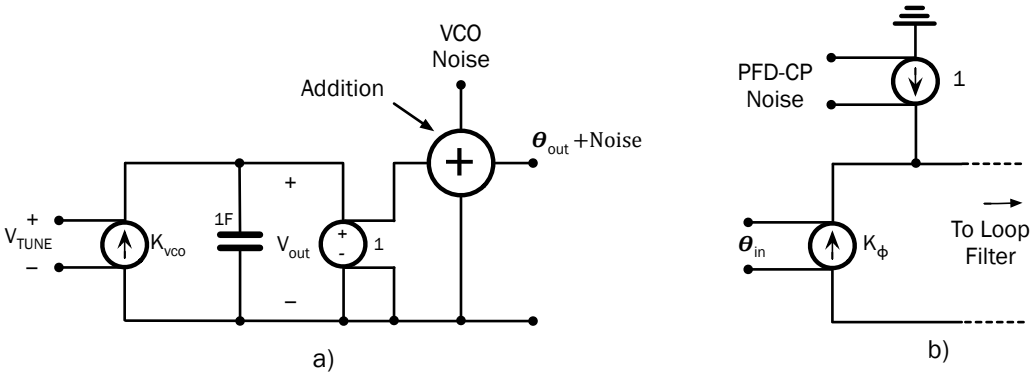


Figure 28. Extended lumped-element model for determining the noise transfer function: a) VCO Noise and b) CP current noise.

2.2.3. Model for Transient Simulation

Transient simulation provides a means to evaluate proper capture process and steady-state error for a PLL. Behavioral models written in Verilog-A are used to run this analysis without concerns about the order of the complete system.

Since the loop filter can be modeled with analog components; PFD, CP, VCO and divider need to be hardware described. Models for the VCO and divider with different levels of complexity are available in [14], whose Verilog-A listings are compatible with the version supported by Cadence. For the case of simple dividers (i.e. powers of 2), schemes using D flip-flops in feedback configuration can be used simplifying its hardware description.

For the PFD, the simplest architecture based on the *triflop* is selected requiring only codes for a D flip-flop and a AND gate. Models of D flip-flops and logic gates are also available in [14]. For the CP, a version with two switched current sources is employed. A code without delay transit is implemented; therefore, problems such as the dead-band

Table 2. Verilog-A model of the CP for transient analysis.

```
// VerilogA design for CP, Transient Analysis

`include "constants.vams"
`include "disciplines.vams"
module CP_va (vdd, gnd, icp, up,dn);
   parameter real fi = k_phi;                    // charge-pump current (A)
    parameter real vth = vdd/2;                  // threshold voltage dependent on the technology for IC fabrication
   input up,dn; voltage up,dn;
   electrical vdd,gnd,icp;
   analog begin
         if (V(up)> vth && V(dn) < vth)          //UP port active
            I(vdd,icp) <+ fi;                    // Pumping current
         else if (V(up)< vth && V(dn) > 0.9)     // DN port active
            I(icp,gnd) <+ fi;                    // Sinking current
         else I(icp,gnd) <+ 0;                   // PFD not active
                                                 // No current, high-Z,
    end
endmodule
```

zone do not become a concern, because the hardware-described CP responds instantaneously. The CP Verilog-A model is reported in Table 2.

2.2.4. Model for Phase-Noise Simulation

When PN simulations are required to predict how a particular system will conform the spectrum of the output signal, the frequency is assumed captured allowing the different blocks to be modeled in terms of how the phase is modified. In the simplest case, these models (called *phase models*) are linear and analyzed easily in the frequency domain [5], and they provide a quick tool to check how modifications in the different transfer functions are reflected in the output PN. Phase models are especially useful, because sometimes a PLL does not have a periodic solution leading to convergence problems in analyses that require the calculation of a steady-state operating condition, such PSS in the Spectre simulator.

Verilog-A models are preferred since the language contains the functions *white_noise*, *flicker_noise*, and *noise_table* that provide several levels of description for the noise of the different blocks comprising the PLL system. For accurate prediction, the *noise_table* function can be optimized using measurements. Preparation of these phase models includes [5]:

1. Using Spectre to predict the noise of the individual blocks that configure the PLL.
2. Building high-level behavioral models of each block using the *noise_table* function of the Verilog-A language.
3. Assembling the blocks to configure the PLL.

A detailed and complete procedure for each specific block can be found in [5].

CHAPTER 3

BAND-REJECT NESTED-PLL CLOCK CLEANER

Clock conditioners have been dominated by PLLs with narrow bandwidth to minimize the effect of the reference PN, including the cascade-type architecture that is devised to clean the signal in two steps. For these architectures, the stability of the basic PLL becomes the bottleneck to configure high-performance clock cleaners.

Figure 29 shows the stability problem for the case of a PLL using a CP. As observed, the PFD-CP generates a current related to the phase error between the input and output signals. The proportionality constant of this block equals the current of the CP. The generated pumping (sinking) current is delivered (extracted) to (from) the loop filter. If initially, this filter is built with only one capacitor (C_1), the voltage that appears as tuning signal will be directly proportional to the charge stored (removed) to (from) the capacitor. Therefore, at this point, one integration over the CP current is performed by the system.

The tuning voltage will affect the frequency of the LO trying to adjust the transition edge (phase) at the input of the PFD. If a phase error exists between the two signals at the input of the system, then the LO will be adjusted in frequency, which means that the elimination of the observed error is conceived as an average operation with respect to time (a second integration). The potential problem appears when a tuning voltage is reached and the signals at the PFD have the same transition edges. At this point, it is possible that the frequency of the LO and the input does not match, which will produce a new cycle of corrections that will eventually lead to the LO phase to wander around the

input-signal phase without acquiring lock. Hence, the loop filter must provide a correction of the tuning voltage adapting it to provide the required command to the LO momentarily to give the system the opportunity to recover from the change in frequency. Therefore, the configuration of the filter must include a zero that can be added as the series connection of additional resistor (R_2) and capacitor (C_2) in parallel with C_1.

The zero-pole notation of Figure 29a presents schematically the location of the different roots. If value of R_2 is selected large, the effect of the path configured by R_2 and C_2 will be negligible, and in the opposite case, the same path makes the capacitor C_2 to be in parallel with C_1 cancelling the desired effect. The associated Bode plot of Figure 29b shows that a trade-off is required to maintain proper value of the phase margin.

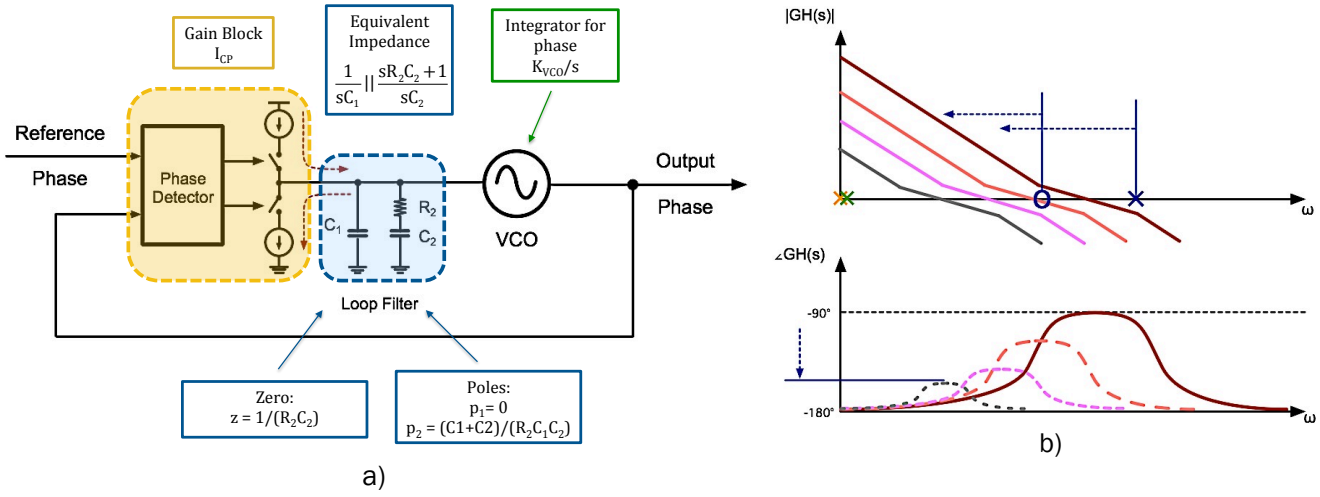


Figure 29. Stability problem as the loop bandwidth is reduced: a) basic CP-based architecture with the associated transfer function and b) Phase margin deterioration.

Noise simulations based on phase models indicate that for the cascade-type PLL, the first loop is still the bottleneck for stability, in addition to the problem associated with

on-chip integration of the filter required for narrow bandwidth. This fact suggests that PLL configurations require customization to attenuate the very close-to-carrier PN.

3.1. Band-Reject Nested-PLL (BRN-PLL) Architecture

A Band-Reject Nested-PLL (BRN-PLL) scheme provides a notch in the input transfer function to attenuate the reference-signal PN and to reduce the size of the loop-filter capacitors substantially. Ultra narrow loops are no longer required because the notch size is related to the system bandwidth. Figure 30 shows schematically how the BRN-PLL will behave compared to the cascade-type PLL.

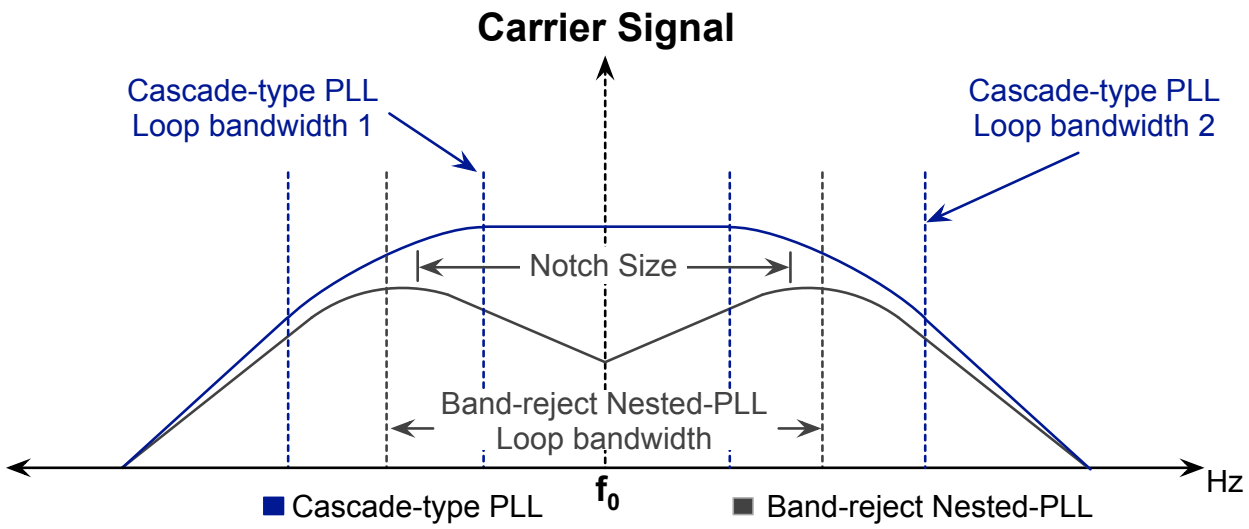


Figure 30. Reference transfer function comparison between the cascade-type PLL and the BRN-PLL.

The behavior of Figure 30 suggests that one cut-off frequency can be used to take advantage of the notch for attenuation. Thus, for this case, a wider loop can extend the

band-rejection range to higher offset frequencies. This modified PLL-based architecture can create such a notch in the input-signal response by introducing a zero through inner and outer loops and a high-pass filter (HPF) (Figure 31). The HPF is used as the divider of the inner loop, and this modified configuration is utilized as the divider of the outer loop [49]. Since it is assumed that the input is a digital signal, the BRN-PLL output is adjusted to the amplitude levels of the line-coding scheme used before is delivered to other parts of the system.

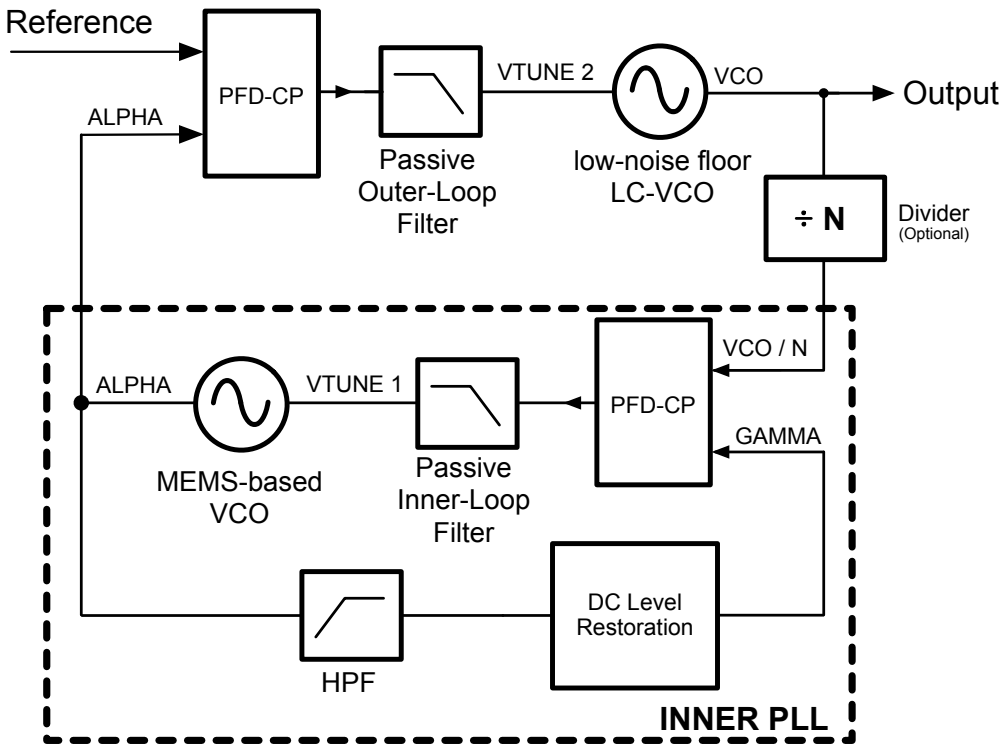


Figure 31. The BRN-PLL architecture for clock cleaners.

Negative feedback is satisfied in this closed-loop system by the appropriate connection of the phase-frequency detector (PFD) ports allowing the two loops to track each other concurrently to the reference signal. For the present description of the system, the LOs have been selected as voltage-controlled oscillators (VCOs) without loss of generality.

3.2. Stability Analysis for the BRN-PLL Architecture

Analysis of the stability for the BRN-PLL is required to assure the system will work cancelling the phase error with proper transient response. Since the system has a nested PLL, the stability analysis will be carried out in two steps. First, the inner PLL will be analyzed, and then the closed-loop behavior needs to be studied to determine the response of the outer PLL. Finally, the stability of the complete BRN-PLL will be addressed.

3.2.1. Inner-PLL Stability Analysis

Similarly to the case of a basic PLL, the CP current will be interfaced with the loop filter where the charge stored (removed) to (from) the filter will determine the value of the tuning voltage. Again, the additional pole and zero provided by the loop filter offer the required compensation to produce a stable system. Two integrations still take place in the system, the average of the phase error and the phase from the change in frequency. In this case, the presence of the HPF will introduce attenuation and up to 90° of phase shift. However, to allow the VCO signal to pass through the HPF, the pole of the filter should be located so that the signal amplitude is not reduced significantly avoiding its detection

by the PFD. Thus, it is expected that phase-shift induced by the HPF will not exceed 45°. Additionally, it is desired to select a wide bandwidth for the inner PLL, so that its inertia is reduced enabling fast outer-PLL capture and tracking processes. Figure 32 summarizes the zero-pole roots in the inner PLL.

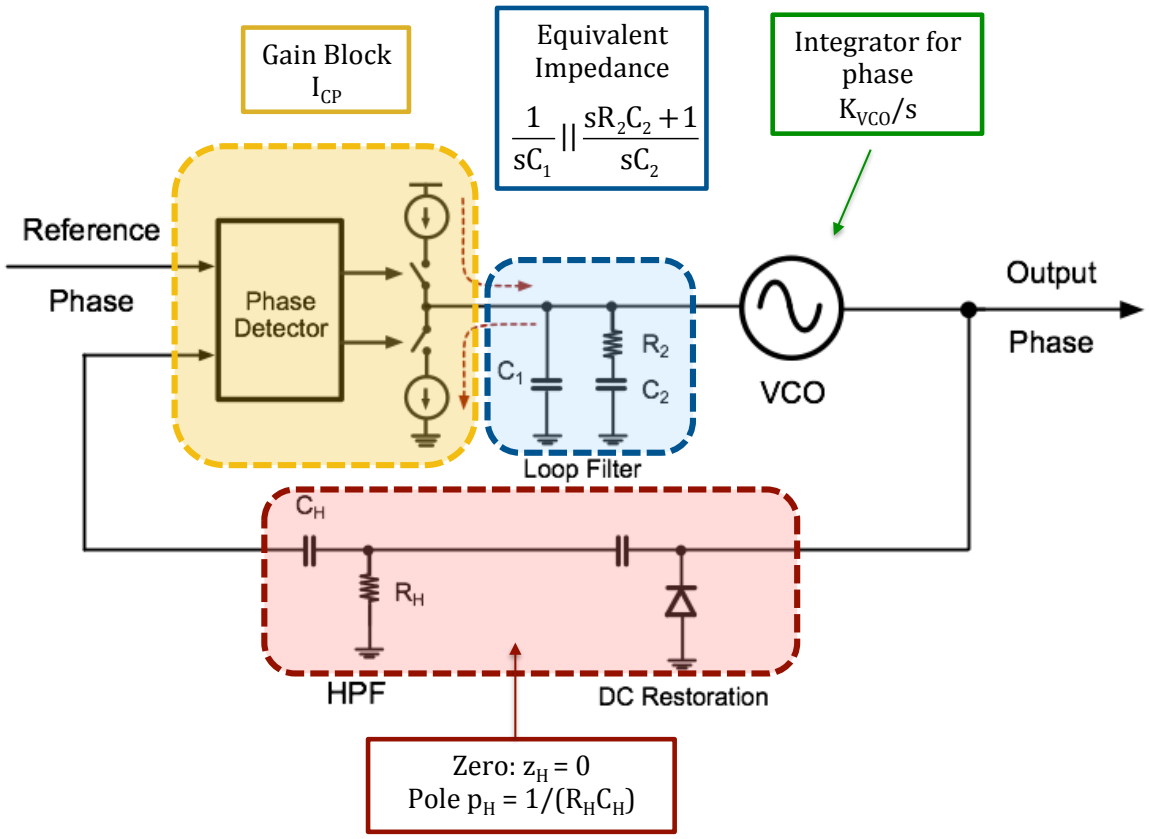


Figure 32. Pole-zero roots for the inner PLL.

As observed, two poles are located at the origin along to the zero of the HPF, which configures the inner PLL as a type-I system. Therefore, this closed-loop scheme will be able to eliminate up to the error produced by step function in the phase. Analyzing the

stability of the system, it can be observed that at low frequencies the gain drops with a defined slope of -20dB/dec and phase equal to 90°. Hence, the zero provided by the loop filter can be located around the transition frequency of the inner PLL, ω_T (the frequency where the open-loop magnitude crosses the 0dB marker) maximizing the phase margin. The remaining poles can be safely placed after the loop-filter zero, which is in agreement with the general consideration of wideband loop. Figure 33 shows the suggested root placement to improve the stability of the system.

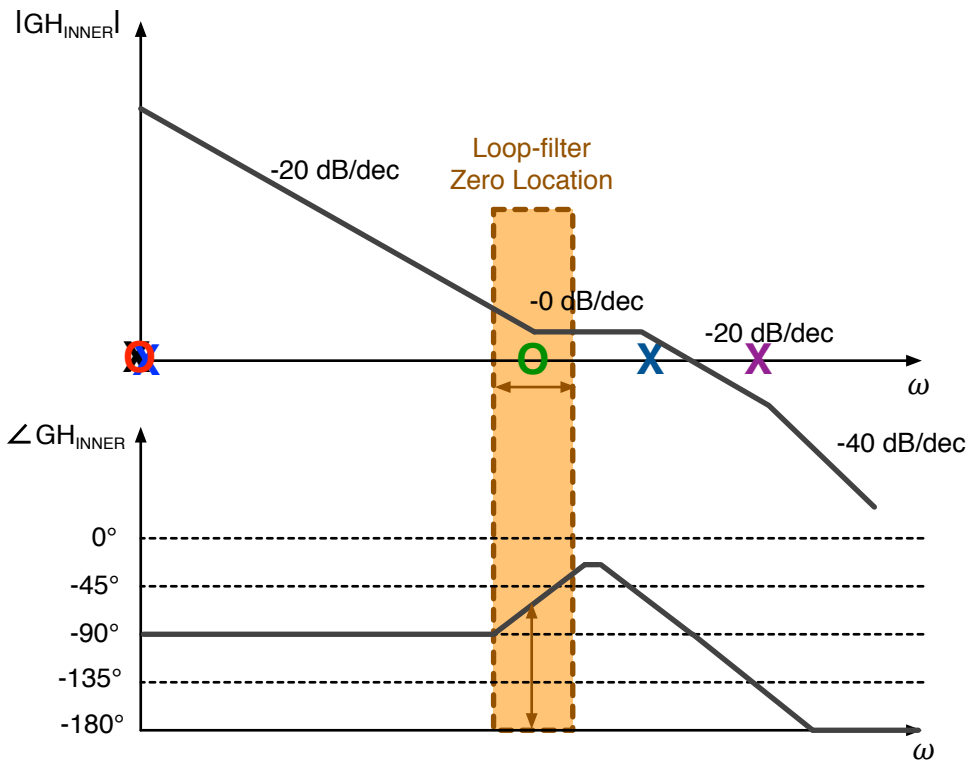


Figure 33. Bode plot displaying the effect of poles and zeros for the inner PLL.

3.2.2. Inner-PLL Closed-Loop Stability Analysis

Stability analysis is also required for the closed-loop equivalent of the inner PLL, since the final location of poles and zeros will affect the stability of the outer PLL. The closed-loop system (inner PLL) can be analyzed via root-locus to determine how the closed-loop poles move from the open-loop poles to the open-loop zeros with respect to the variables of the PLL. Thus, determining the characteristic equation of the inner-PLL, the root-locus of the system can be drawn and the gain k can be associated with the parameters of the PFD-CP and loop-filter components. From Figure 34, the transfer function for the filters used in the inner PLL can be defined as

$$LPF_1(s) = \frac{s(R_2 \cdot C_2) + 1}{s^2(C_1 \cdot C_2 \cdot R_2) + s(C_1 + C_2)}, \tag{15}$$

$$T_1 = \frac{1}{\omega_1} = R_2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2},\ T_2 = \frac{1}{\omega_2} = R_2 \cdot C_2, \tag{16}$$

$$HPF(s) = \frac{s \cdot R_H \cdot C_H}{s \cdot R_H \cdot C_H + 1}, \quad T_H = R_H \cdot C_H \quad . \tag{17}$$

The characteristic equation can be defined as follows,

$$1 + GH_{INNER}(s) = 0 \tag{18}$$

$$\frac{K_1 \cdot K_\phi \cdot T_1 \cdot T_H \cdot (1 + s \cdot T_2)}{C_1 \cdot s \cdot (1 + s \cdot T_1) \cdot (1 + s \cdot T_H)} = 1\angle\left(180° \pm k \cdot 360°\right) \tag{19}$$

$$\frac{k \cdot (s + \omega_2)}{s \cdot (s + \omega_1) \cdot (s + \omega_H)} = 1\angle\left(180° \pm k \cdot 360°\right), \tag{20}$$

where K_ϕ is the PFD-CP gain and K_1 is the gain of the VCO_1, and k will be equivalent to the gain parameter in the root-locus and it is defined as $K_1 \cdot K_\phi \cdot T_2 / C_1$. The root locus of Equation 20 can be observed in Figure 34.

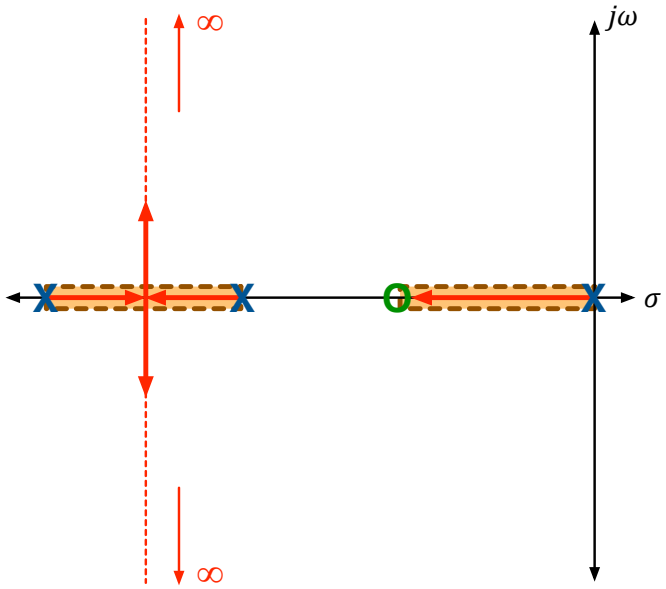


Figure 34. Root-locus for the inner PLL.

It can be observed that the selected location of the open-loop zeros and poles makes the root-locus of the closed-loop system to have two paths for the poles to move. The presence of the zero at the origin of the HPF makes the remaining pole to move directly to the available zero. The poles at higher frequency move close to each other and split to reach the two zeros located at infinity. It is important to notice that for all the values the k, the closed-loop poles remain in the left-hand side of the plane indicating that the

system is stable. The particular location of the pair of complex-conjugate poles will depend on the estimated value of k.

3.2.3. Outer-PLL Stability Analysis

Once the stability of the inner PLL has been checked (open- and closed-loop), its closed-loop equivalent is used as divider for the outer PLL, and the Nyquist stability criterion can be used to analyze its stability. For simplicity, it will be considered that the outer PLL employs a second-order current-based loop filter, which with a transfer function similar to Equation 15 provides two additional time constants, T_3 and T_4.

For this case, it is necessary to determine the location of the roots for the closed-loop equivalent of the inner-PLL, and therefore the gain k will determine the final location of the closed-loop poles and suitable locations for the two additional time constants. From the definition of the parameter k ($K_1 \cdot K_\phi \cdot T_2 / C_1$), it can be observed that the value is dominated by the inverse of the capacitor C_1; therefore it is expected a large number for the gain of the root-locus and most likely a pair of complex-conjugate poles due to the inner PLL. Figure 35 shows the proper location of the two additional time constants to obtain at least 45° of phase margin and how the selection is dependent on the relative location of the transition frequency. Figure 35 shows variations in the phase plot considering well-spaced roots; however, it can be observed that the pole of the outer PLL can be used to cancel the inner-PLL zero at higher frequency. In addition, the remaining zero of the outer PLL can be translated to higher frequency while the phase margin is still adequate.

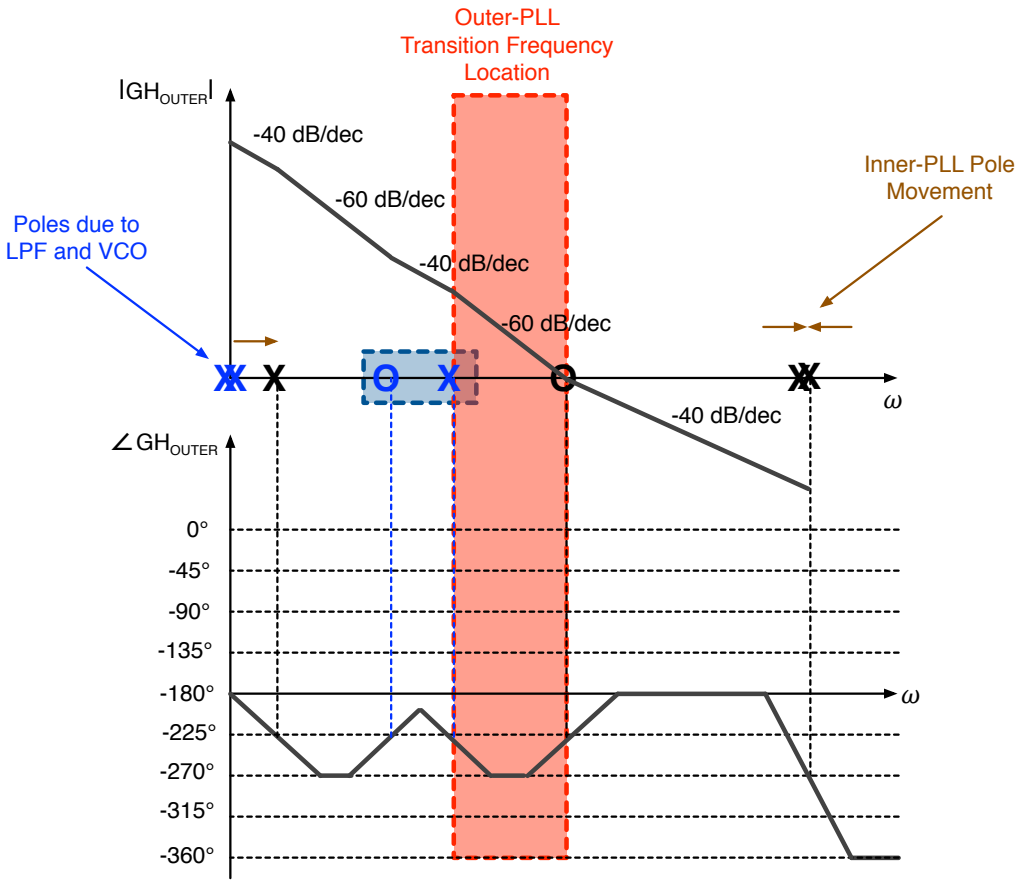


Figure 35. Outer-PLL root locations.

3.3. BRN-PLL Design Guidelines

From Section 3.2, it can be observed that the BRN-PLL architecture can be designed using the Nyquist stability criterion in two consecutive steps. The inner PLL is addressed first and replaced with its closed-loop gain expression to determine the outer-PLL loop filter. For any value of the gain *k,* the location of the closed-loop poles of the inner-PLL are in the left-hand side of the complex plane maintaining stability. For the present guidelines, third-order loop filters will be used to reduce reference-signal feedthrough, which will further handle adverse effects in the performance of the clock

cleaner. Any additional root must be located at high frequency with respect to the transition frequency of each loop.

3.3.1. Inner-PLL Design Guidelines

Along to the third-order current-based loop filter, a first-order HPF must be utilized for this PLL to maintain at least a type-I feedback system.

Based on (15-17), the inner-PLL open-loop gain ($GH_{INNER(s)}$) can be rewritten as (23):

$$LPF_1(s) = \frac{s(R_2 \cdot C_2)+1}{s^2(C_1 \cdot C_2 \cdot R_2)+s(C_1+C_2)} \cdot \frac{1}{s(R_3C_3)+1}, \tag{21}$$

$$T_1 = \frac{1}{\omega_1} = R_2 \cdot \frac{C_1 \cdot C_2}{C_1+C_2},\ T_2 = \frac{1}{\omega_2} = R_2 \cdot C_2,\ T_3 = \frac{1}{\omega_3} = R_3 \cdot C_3 \ , \tag{22}$$

$$GH_{INNER}(s) = \frac{K_1 \cdot K_\phi \cdot T_1 \cdot T_H \cdot (1+s \cdot T_2)}{C_1 \cdot s(1+s \cdot T_1) \cdot (1+s \cdot T_H)} \cdot \frac{1}{(1+s \cdot T_3)}, \tag{23}$$

where K_ϕ is the PFD-CP gain, K_1 is the gain of the VCO_1, and T_H is the time constant related to the HPF as defined by Equation 17.

Equation 23 reveals that the inner PLL has one zero and four poles (one at the origin). Since a wide inner-PLL bandwidth is preferred, but to maintain its treatment as a continuous system, the maximum bandwidth for the inner PLL can be set to the operating frequency divided by 20 [1].

For design purposes, the poles and the zeros are placed with respect to ω_T; however, it is more practical to start setting the loop bandwidth, which is the parameter that defines the passband for the noise transfer functions. Since the two frequencies are

closed to each other, the transition frequency is determined from the 3dB frequency with the relationship $\omega_T \approx \omega_{3dB}/1.33$ [1]. Even though, this ratio has been determined for second-order loops, experience has shown that this ratio stays nearly unchanged for higher-order loops when the extra poles are placed at higher frequencies that ω_T. [1].

For the discussion of stability, the location of the root at ω_H with respect to ω_2 can be used to determine the best trade-off between settling time and phase margin. Suitable root locations to satisfy the complex-conjugate poles location and to maximize the phase margin can be defined as

$$\omega_2 = \omega_T,\ \omega_1 = 10\omega_2,\ \omega_H = 2\omega_2, \omega_3 = 5\omega_1, \tag{24}$$

where the time constant related to ω_3 has been located as the highest frequency pole to minimize its effect.

3.3.2. Outer-PLL Design Guidelines

The outer-PLL loop filter is designed by applying the stability criterion for a second time. Similarly to the inner-PLL case, the outer PLL employs a third-order current-based loop filter, which with a transfer function analogous to Equation 15 provides three additional time constants, T_4, T_5, and T_6.

Following a similar procedure to that of Section 3.2.2, the inclusion of the extra time constant T_3 needs to be analyzed to determine how the root-locus of the inner-PLL is affected. From Figure 34, locating the root associated with T_3 at high frequency does not alter the path followed by the poles analyzed previously, which includes the poles that move to each other to become complex conjugate. However, the extra pole increases the number of asymptotes and their associated polar location (also affects the departure

angle) from ±90° to ±60° and 180°. The new angles indicate that even though the extra pole located at high frequency will move toward infinity following the 180° asymptote, the two poles next to each other will still split to become complex conjugate and given the ±60° asymptote-angles, there exists a value of the gain *k* that can produce instability. Thus, the value of *k* needs to be restrained and it can be controlled increasing the value of C_1 indicating that the bandwidth of the inner-PLL cannot be selected as wide as possible. Therefore, the selection of higher-order loop filters improves the performance with respect to the feedthrough, but includes the possibility of instability. Phase model simulations will dictate the optimum value of the inner-PLL bandwidth.

Given the final locations of the inner-PLL roots, it is observed that the one associated with ω_2 keeps being a zero, and, the pole at ω_4 can be used to cancel it reducing the number of roots to locate. Using this strategy, the root-locus of the complete BRN-PLL will resemble the one for the inner PLL. Depending on the desired bandwidth and the size of the capacitors obtained, both ω_5 and ω_6 can be placed close to the inner-PLL transition frequency, ω_T. Similarly, final locations for ω_5 and ω_6 will be determined using phase models for trading off peaking in the noise response and fast capture time.

3.3.3. Noise Transfer Functions

The behavior of the BRN-PLL is analyzed for the different noise sources appearing in the scheme. The set of transfer functions can be derived by activating each noise source at the time as shown in Figure 36. Sections 3.3.1 and 3.3.2 suggest that is possible to relate all root locations with ω_T allowing to express the system in terms of one frequency variable. Thus, using Equation 24, and, for illustration purposes, selecting

$\omega_4=\omega_T$, $\omega_5=\omega_T/50$ and $\omega_6=\omega_T/15$, the expressions for the filters of the architecture can be summarized in Equations 25-27, which produces a typical set of Bode plots for the transfer functions observed in Figure 37.

$$LPF_1(s)=\frac{50\left(sT_T+1\right)}{C_1 s\left(sT_T+10\right)\left(sT_T+50\right)} \tag{25}$$

$$LPF_2(s)=\frac{50sT_T+1}{50C_4 s\left(sT_T+1\right)\left(15sT_T+1\right)} \tag{26}$$

$$HPF(s)=\frac{sT_T}{sT_T+2} \tag{27}$$

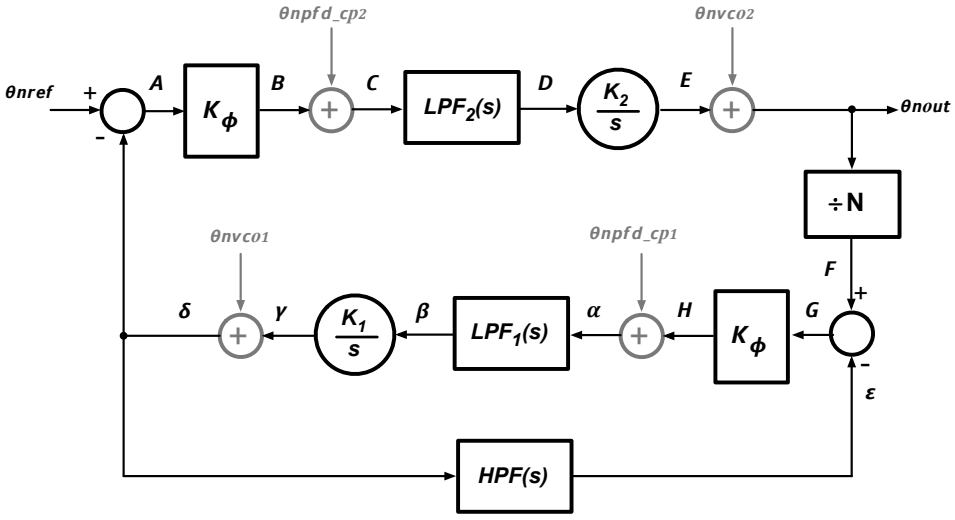


Figure 36. Steady-state equivalent block diagram for the BRN-PLL to determine the different noise contributions.

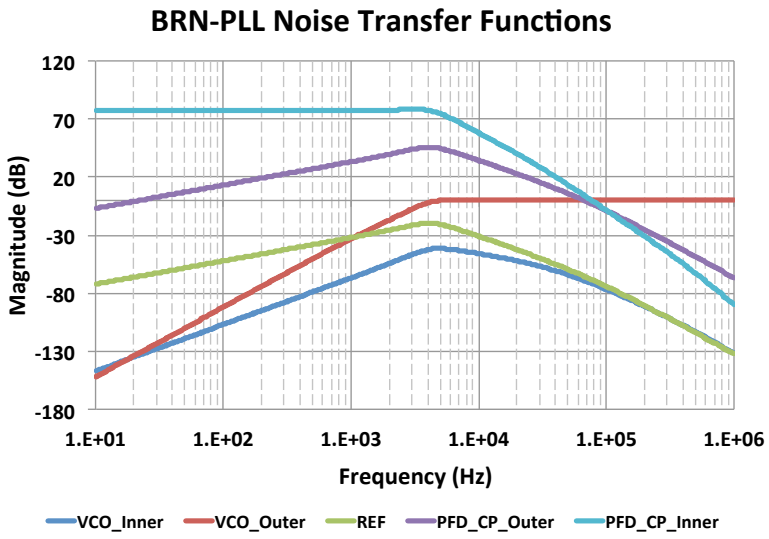


Figure 37. Behavior of the BRN-PLL to the noise of the different building blocks.

It can be noticed that the only one-side noise transfer function that behaves as low-pass filter is the one of the inner-PLL PFD-CP. The pass-band gain is proportional to the divider value *N* and inversely proportional to the CP current. This behavior is the same than that obtained with a traditional PLL system. On the other hand, the outer-PLL PFD-CP noise gets attenuated very-close-to-carrier, which reduces the overall effect of two PFD-CPs compared to cascade-type PLLs.

Figure 37 shows that the response for the input and VCOs noises does not exhibit gain, and it is clear that for both inner-PLL VCO and input, the BRN-PLL produces significant attenuation and consequently effective cleaning. The PN around the transition frequency will be determined by the input, inner-PLL VCO and outer-PLL PFD-CP, and their noise contributions depend on the associated pass-band local maxima, which correspond to the system bandwidth. Thus, the noise of the CP becomes critical for the

performance of this clock cleaner, and the LOs will be selected as LC-VCO for VCO_2 (for noise-floor performance), and a high-Q LO for VCO_1 (to reduce any *bump* or hard transition between the inner-PLL PFD and the LC-VCO). A MEMS-based VCO becomes a suitable candidate based on performance and footprint.

3.3.4. PN Performance

For PN simulation, linear operation is assumed and phase models are employed in the frequency domain. For a quick analysis each building block can be modeled using the *white_noise* and *flicker_noise* functions. However, for the reference PN model, two versions are generated to analyze how the BRN-PLL conforms the noise performance based on the transfer functions summarized in Figure 37.

First, the PN performance of an Agilent E4438C Vector Signal Generator was measured. The results were incorporated to a phase model labeled as *clean reference*. Second, a *dirty reference* phase model was generated with the measured PN of the VCO integrated in a 4046 PLL IC, which can be used because only the noise performance is required (the close-to-carrier noise in particular), not the actual operating frequency. This PN profile was chosen because, being a wide tuning VCO, it exhibits poor spectral purity.

Using phase models, the superior performance of the BRN-PLL over the cascade-PLL type scheme can be checked. Employing the *clean reference* set up, the cascade-type PLL and the BRN-PLL appear to have similar performance because the dominant noise source is the inner-PLL PFD-CP in both cases. However, when the *dirty reference* is used, the effect of the notch in the BRN-PLL scheme produces full-spectrum clock

cleaning. Phase-models simulations of the noise following the testbenches are presented in Figure 38. As expected for the BRN-PLL, the effect of a dirty reference is minimized.

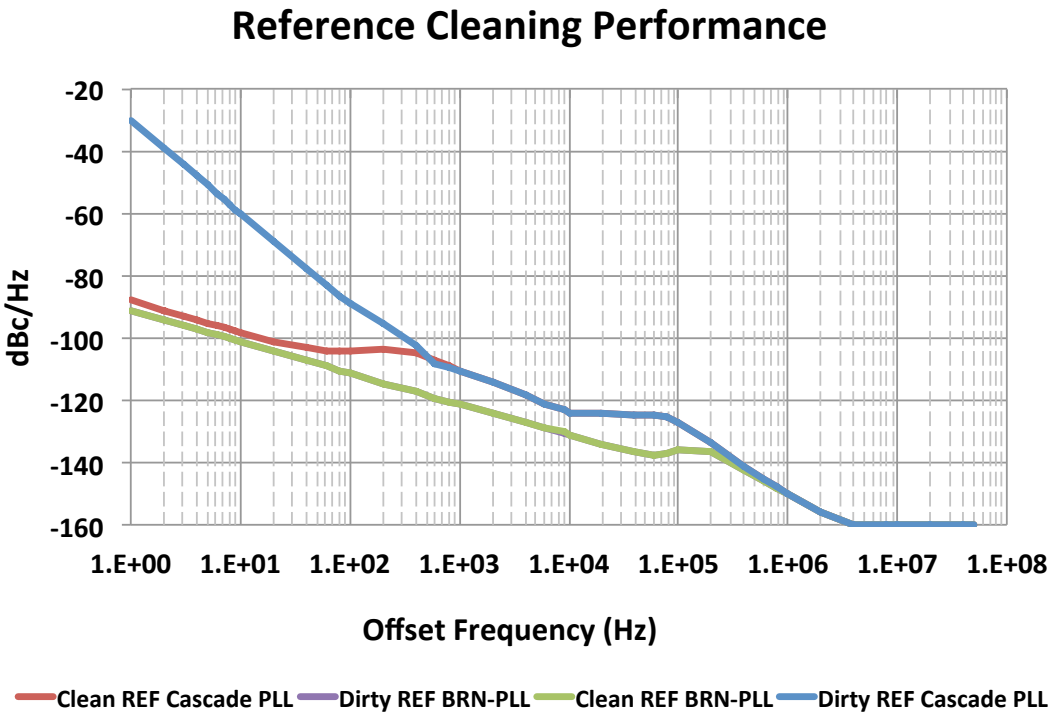


Figure 38. Performance of the cascade-type PLL and he BRN-PLL under clean and dirty reference PN set-ups.

CHAPTER 4

DESIGN OF PFD-CP AND DS LC-VCO

4.1. PFD-CP Design

Chapter 3 showed that the close-to-carrier PN of the BRN-PLL is dominated by the noise due to the PD, and it becomes critical for the overall system performance. Hence, since the PFD-CP block is employed, it can be determined that the PFD will only set the conditions to enable the required current sources in the CP. Therefore, the main contribution to the oscillator noise is due to the CP current noise. A single-ended CP is preferred due to its lower power consumption and autonomous operation without additional local amplifiers. A direct implementation of Figure 8 produces the basic CP architecture presented in Figure 39a. A bias circuit from a reference current source usually generates the bias voltages (V_P and V_N) for the best matching between pumping and sinking currents.

As commented in Section 2.1.1, the work by [30] can be used to ease the matching requirement via two CPs and a modified *triflop*. However, the inclusion of a second CP will increase the noise current, and therefore will deteriorate the performance of the BRN-PLL. Thus, the noise behavior of the CP needs to be addressed to maintain the linearity/matching technique proposed by [30].

The first attempt for noise performance is shown in Figure 39b, where the CP switches have been moved to the rails to alleviate the problem of direct charge-injection to the output nodes, and the inclusion of charge-removing transistors to assuage the charge-sharing problem [50]. Not only a large reduction in the phase offset is obtained,

but also reduction of the intrinsic $1/f$ noise is achieved with some sacrifice in the output linearity [51].

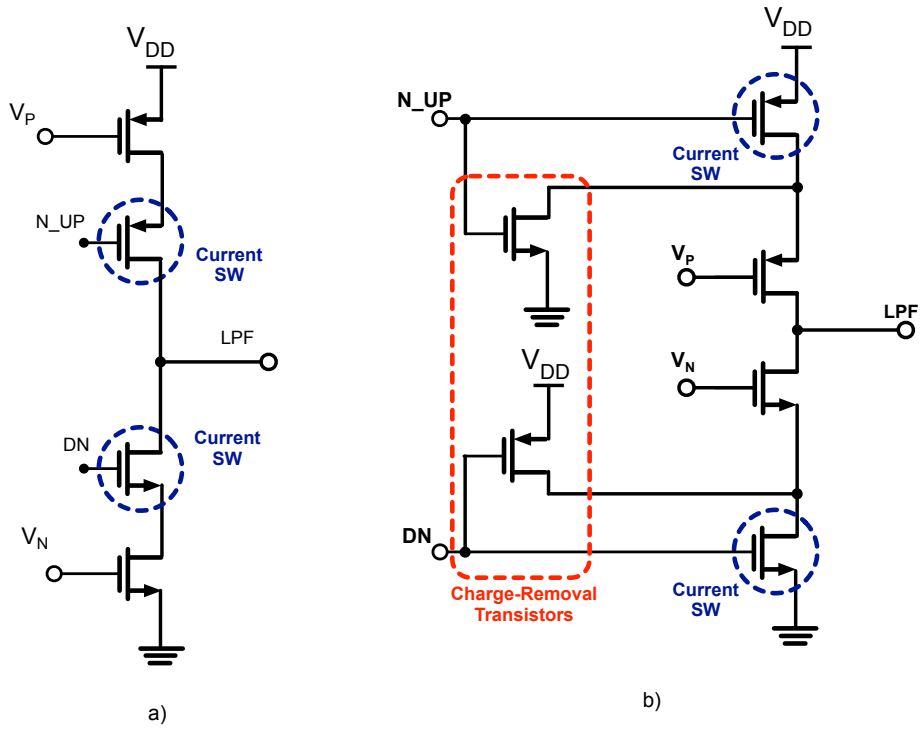


Figure 39. Single-ended architectures for the CP: a) basic implementation and b) scheme with switches located away from the output and charge-removal transistors inclusion

From Figure 39b, it can be noticed that the cascoded transistors maintain an active path for the output port, which involves interaction with their corresponding noise sources. Thus, a switching network is located at the output to maximize the isolation between the current sources and the loop filter to reduce noise. The switching network monitors N_UP (the negated version of UP) and DN signals and opens the connection anytime the PFD is idle. Hence, when the PLL system acquires lock, the CP is

disconnected isolating the main source of noise. In the case that the tuning voltage deviates from the desired value due to leakage of the loop-filter capacitors, the loop-dynamics will force the PFD to produce the required signal recovering it.

The addition of the switching network needs to take into account the resistors associated with the transistors that implement the required passgate. When the switching network is not included, the interconnection between CP and loop filter is able to process phase variations with current changes allowing the detection of very small differences between the signals at the PFD ports. On the other hand, when a resistor is placed before the current-based filter, the complete block becomes a typical voltage-voltage network and the phase information is then handled as a voltage signal that implies that the capacitances in the interconnection will have a more decisive effect increasing the possibility of spurious tones due to the dead-band zone. Hence, the switches included under this strategy must minimize the on resistance of the passgates without significant increase in the parasitic capacitances that otherwise would limit the bandwidth of the loop filter.

A complementary topology is employed to reduce the on resistance of the switches without concerns about the tuning voltage (i.e. it can swing to the rails). In addition, dummy switches are added to PMOS and NMOS transistors to alleviate the charge injection problem and to assuage clock feedthrough. The transistors for the switching network are selected minimum size (L) to increase the switch figure of merit [6].

For the generation of V_P and V_N, a self-biased cascoded current mirror is used to account for the stacking of the transistors in the CP. The cascoded current reference has a higher output resistance ($\approx g_m r_{ds}^2$) and its theoretical gain error is zero, which favors

matching of the currents in the CP [52]. The cascoded transistors M8 and M9 will be biased at about V_{th}-$2V_{ov}$, and when the current reference is interfaced with the CP, the current switch will be forced to work in triode region establishing emitter degeneration that improves linearity. Figure 40 shows the final implementation of this CP.

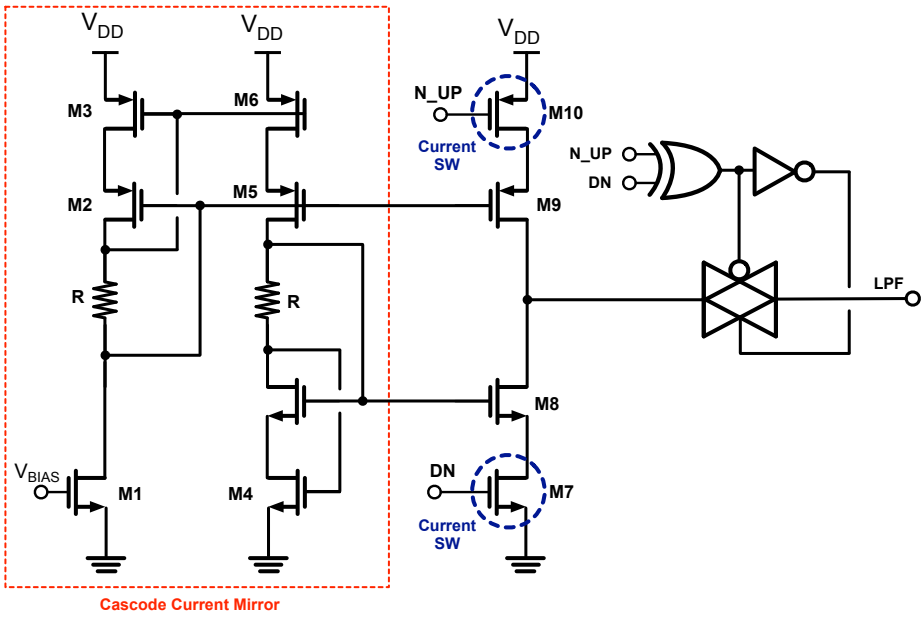


Figure 40. CP architecture with cascoded current mirror and isolation switching network

Since the PFD outputs are active in high, and the PMOS switches for the pumping current are active in low (N_UP/N_UPED), an inverter should be placed at the corresponding PFD outputs. However, with this inclusion, the delay between the PFD outputs and the CPs would be different affecting the linearity of the complete scheme. To compensate for this transit delay, the UP/UPED signals include an *always-ON* passgate, while the DN/DPED signals are interfaced with a double inverter, as shown in Figure 41.

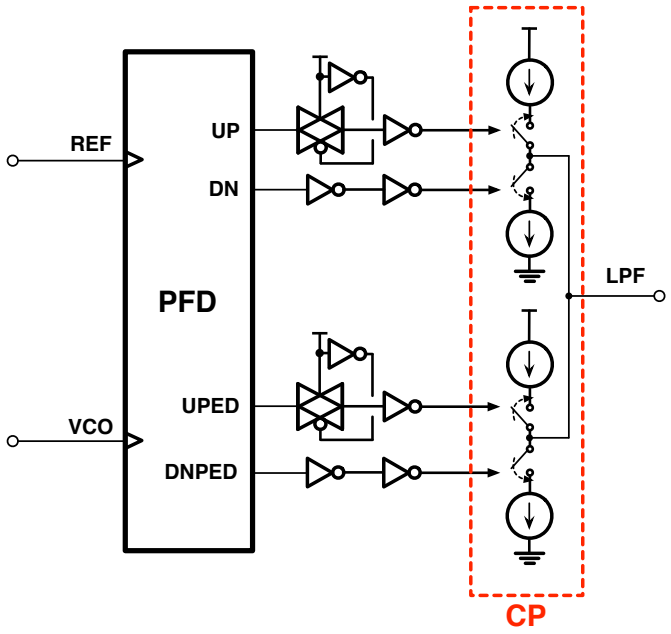
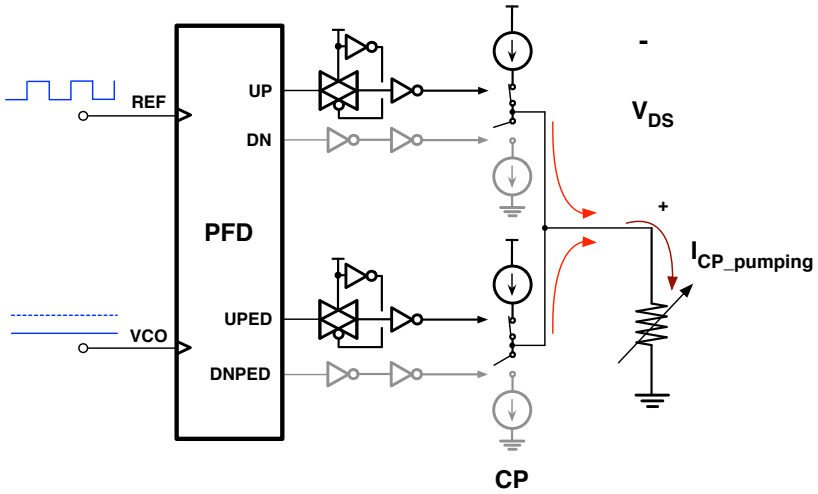


Figure 41. PFD-CP architecture using passgates to compensate the transit delay in the CP interconnections

From a simulation point of view, the noise of the PFD-CP can be obtained by driving this block with a periodic signal that produces representative switching at the output, so that PNoise analysis (Spectre) will produce a good estimate of the output-current noise. On the other hand, when the performance comparison of different PFD-CP architectures is based on lab tests, an indirect measurement technique estimating the very-close-to-carrier PN can be employed using a high-performance generator and a wide-band PLL. Since the pass-band gain for the reference transfer function is 0dB and the one for the PFD-CP equals $20\log(1/I_{CP})$ dB, when the reference input exhibits low PN and is maintained the same during the complete testing, the noise effect of different CP architectures can be obtained by comparison.

Using this indirect technique, two versions for the CP were prepared for tape-out and test (Figs. 39b-40). For the architecture of Figure 39b, the sizes of the transistors were designed looking for the best matching between pumping and sinking currents, while the number of inputs was reduced (for maximum currents, V_P and V_N were selected as GND and V_{DD}, respectively). The total current for the scheme is about 700µA. On the other hand, for the switching-network architecture of Figure 40, the self-biased cascode current mirror establishes a well defined V_P and V_N that set the CP current to approximately 270µA. For this estimated current, a R_{on} of 130Ω is calculated when the current switches (M7 and M10) are on.

The method used to determine the current (both simulation and testing) is based on the characterization of the current of a MOS transistor with fixed gate voltage. Therefore, sweeping the voltage at the drain, the current change is recorded. The selection of pumping or sinking current measurement is made by driving the PFD inputs with the proper set of signals as summarized in Figure 42.



a)

Figure 42. CP current characterization method for both a) pumping and b) sinking conditions

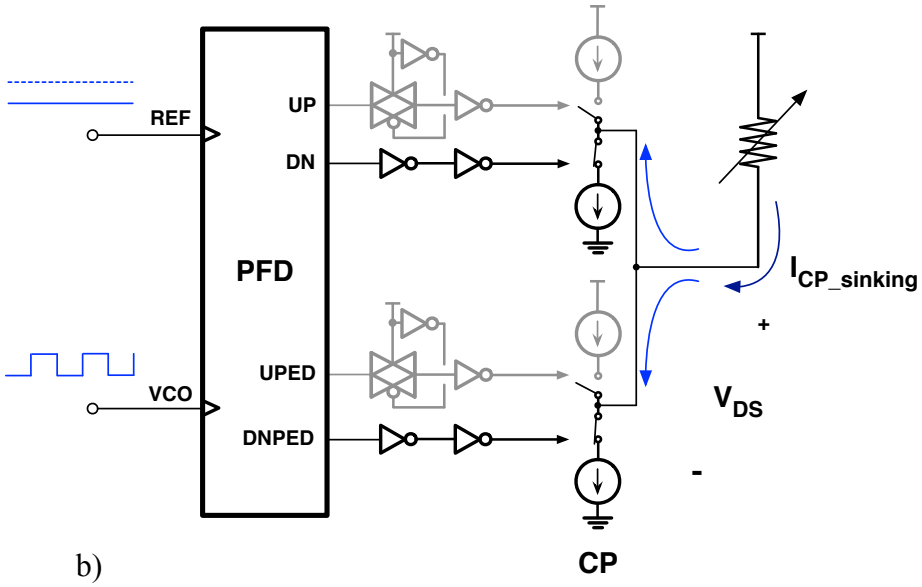


Figure 42 (Continnued)

The two options for the CP were fabricated in a 0.18µm 1P6M CMOS process producing the results of Figures 43 and 44, and for both cases, the linearization technique proposed by [30] was implemented.

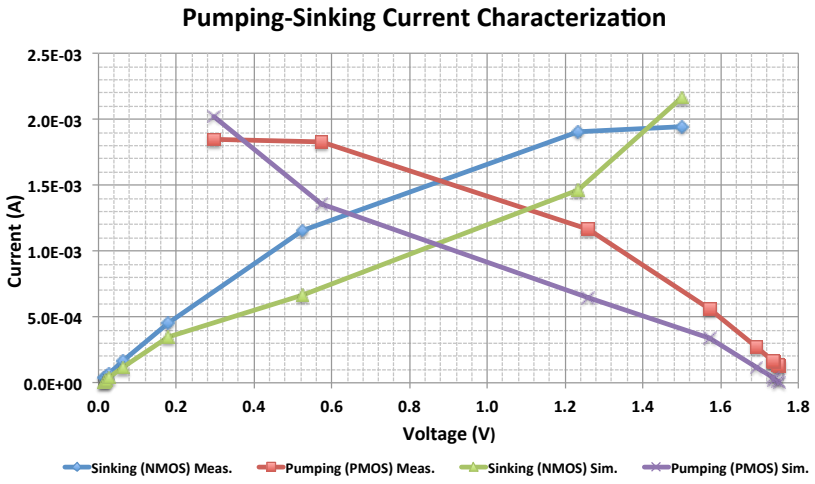


Figure 43. CP current characterization for the architecture of Figure 39b.

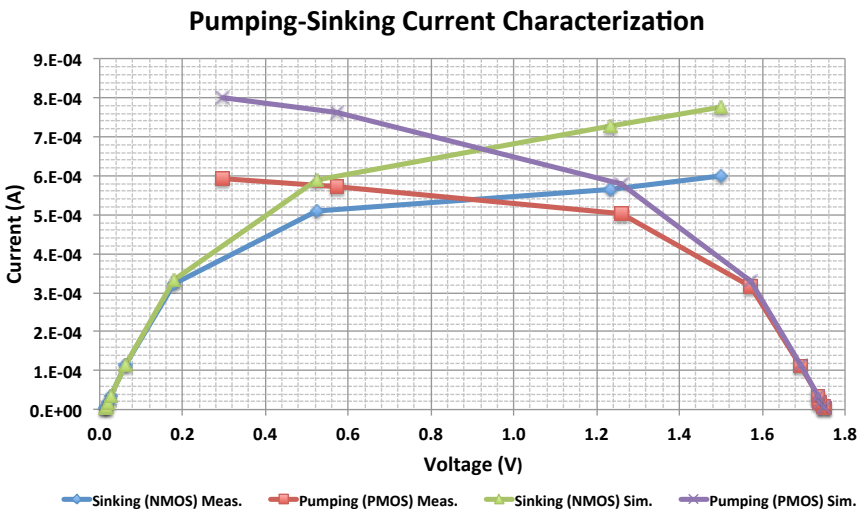


Figure 44. CP current characterization for the architecture of Figure 40.

The $V_{DD}/2$ output voltage is selected to provide an estimate for the current gain of the CP, because the tuning signal is expected to deviate from this value during closed-loop operation, and it is the point where the pumping and sinking currents intersect. Employing the architecture of Figure 39b in the setup of Figure 42 produces about 1.5mA, and the correlation coefficient between the sinking and pumping currents is 99.9712%. On the other hand, the architecture of Figure 40 exhibits 540µA with a correlation coefficient of 99.9835%. The correlation numbers support the matching current strategy described by [30], and the use of the self-biased current mirror allows lower current and higher correlation coefficient.

The two architectures were simulated in a PLL configuration (indirect measurement) using as LO an LC-based VCO running at 82MHz (see Section 4.2). PNoise analysis was used to characterize the very-close-to-carrier PN, and the simulation results are presented in Figure 45.

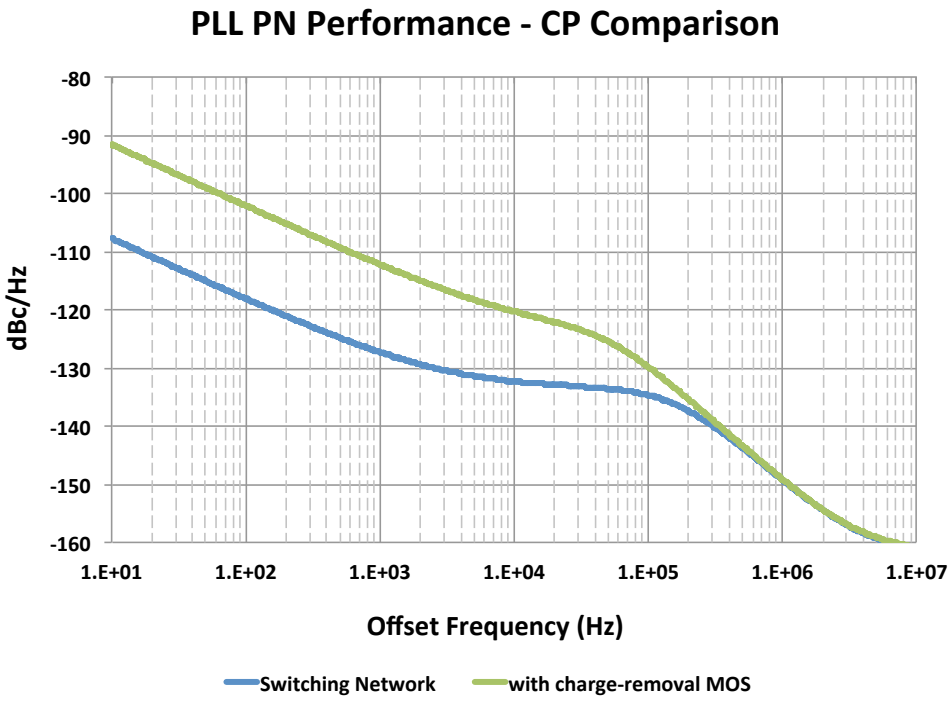


Figure 45. CP current characterization for the architectures of Figures 38b and 39.

It can be observed that although the current of the architecture of Figure 40 is about 3× lower, the PN very-close-to-carrier is approximately 15dB better that the architecture of Figure 39b. Considering the $20\log(1/I_{CP})$ gain by the PLL and given a common reference for the two testbenches, it can be estimated a total improvement of 23dB when the switching network technique is applied.

For testing, the reference source for both cases was an Agilent E4438C. The PN was measured using an Agilent E5500 PN analyzer system, and the results are summarized in Figure 46. It can be observed that the difference between the two architectures is close to 15dB, as predicted by simulation.

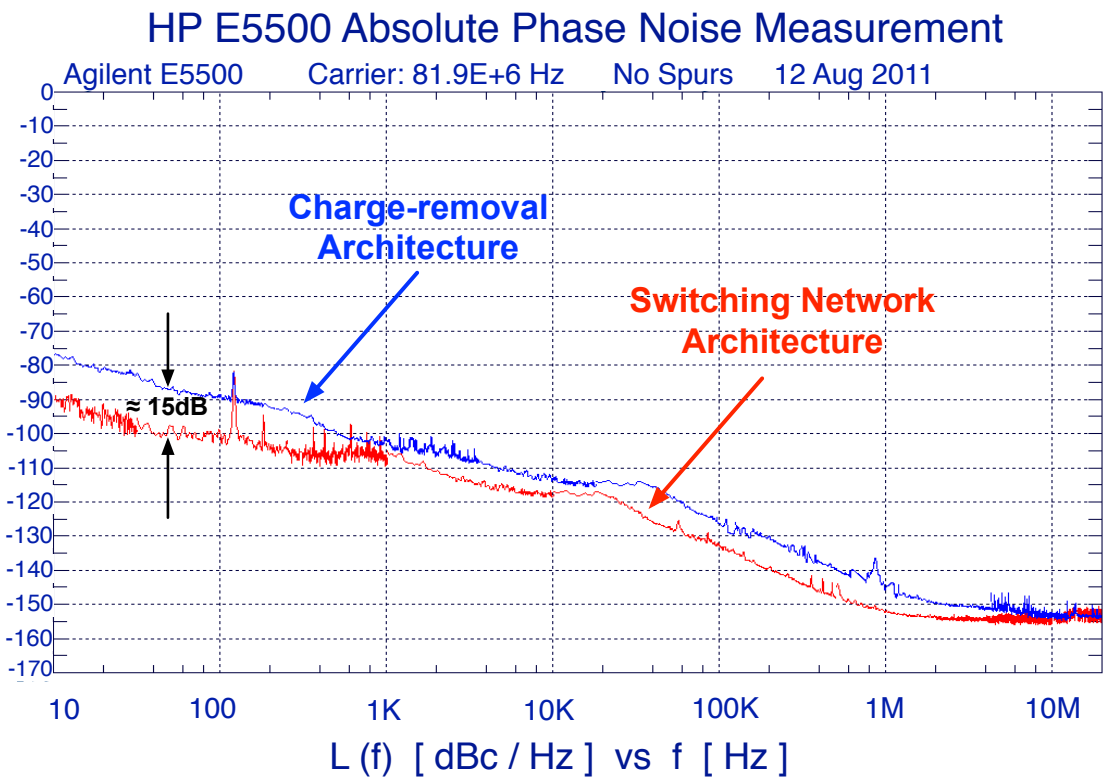


Figure 46. Measured PN performance of a wide-PLL to analyze the noise performance of the two CP configurations.

4.2. LC-VCO Design

Figure 23 shows the basic architecture for an LC VCO following the theoretical definition of the two tuned-gain stages configured in a cross-coupled architecture [6]. To minimize the number of tank elements, LC VCOs can be built using two possible versions of the negative-resistance generator, single-switching (SS) and double-switching (DS) pairs. In both cases, the tuning scheme is implemented with varactors and/or discrete frequency steps (see Figure 47).

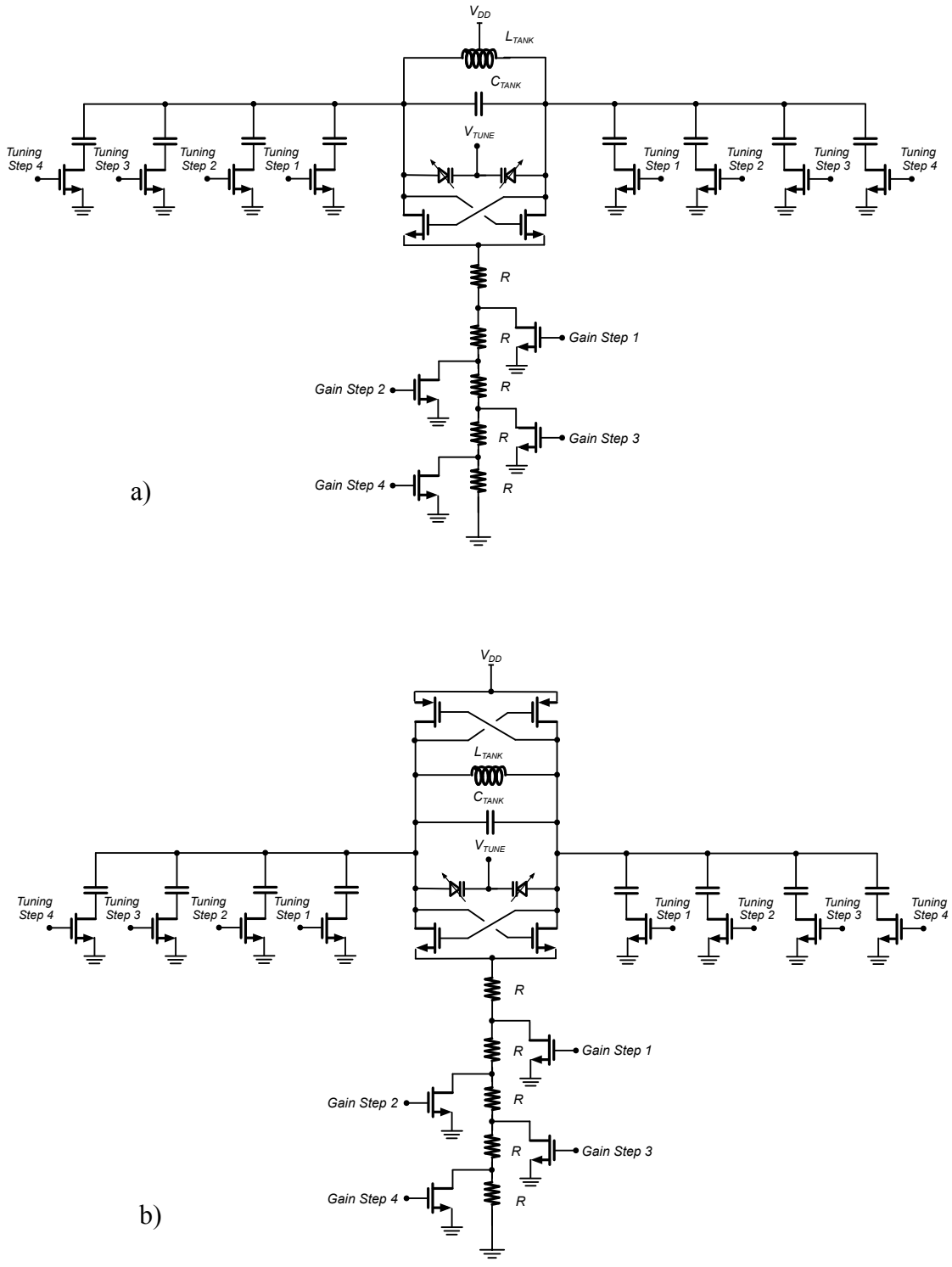


Figure 47. Architectures for LC-VCOs using only one tank circuit: a) SS and b) DS switching pairs.

Even though, it could be thought that the presence of two switching pairs add to the noise of the DS LC-VCO, actually each switch generates only half as much noise as the SS LC-VCO case, because the DS LC-VCO switches only operate half of the time [53]. Thus, it can be approximated that the only behavioral difference between the two architectures lies in the different oscillation amplitude, which is twice the one of the SS LC-VCO leading to a 6dB improvement in the PN.

From a power-supply point of view, the SS LC-VCO oscillation swings symmetrically above and below V_{DD}, while the DS LC-VCO does between V_{DD} and GND. If the oscillation amplitude is the same in both cases, V_{DD} in the SS LC-VCO is allowed to be half of the value used in the DS LC- VCO [53].

Compared to the size required for capacitors and active components, inductors in the 0.18μm 1P6M process are still bulky challenging complete on-chip integration. Since the area of the on-chip inductor increases proportionally with its value, interfacing an LC-VCO with a MEMS-VCO becomes problematic when the high-performance LO is running at a lower frequency. For this case, the inductor would be impractically big, or the clock cleaner scheme would require a large divider that would compromise noise performance.

An additional aspect to consider is the *Q* values of on-chip inductors. For example, a typical 0.18 μm CMOS process [54] offers inductors that exhibit *Q* values ranging from 9 to 20. Table 3 summarizes some characteristics of the available on-chip inductors for the process considered for illustration.

Table 3. Parameters for a sample of on-chip inductors in a 0.18μm 1P6M from a typical CMOS Process [54].

Ldc (nH)	Rdc (Ohm)	Qpeak	Fpeak (GHz)	Outer (um)	Width (um)	Space (um)	Turns	Density (%)
0.969	0.45	19.46	4.13	275	32	2	1.5	53.79
0.99	0.69	17.16	6.08	225	18	2	1.5	39.81
0.991	0.56	18.24	4.94	250	24	2.5	1.5	46.39
0.994	0.95	15.36	8.04	200	12	2.5	1.5	31.57
0.996	0.56	18.3	4.93	250	24	2	1.5	46.2
1	0.49	18.97	4.18	275	30	3	1.5	51.45
1.01	0.49	19.09	4.16	275	30	2	1.5	51.13
1.02	0.57	17.1	4.56	225	26	3	2	68.58
1.03	0.57	17.22	4.5	225	26	2	2	68.17
1.03	0.57	17.16	4.53	225	26	2.5	2	68.38
1.04	0.62	17.78	5.05	250	22	2.5	1.5	43.21
1.05	0.53	18.62	4.23	275	28	3	1.5	48.72
1.06	0.53	18.74	4.22	275	28	2	1.5	48.38
1.07	0.46	19.3	3.64	300	34	3	1.5	52.92
1.08	0.47	19.4	3.63	300	34	2	1.5	52.64
1.09	0.63	16.69	4.51	225	24	3	2	64.93
1.1	0.57	18.23	4.3	275	26	3	1.5	45.91
8.61	2.56	11.75	0.946	400	22	2	4.5	74.01
8.65	3.63	11.17	1.34	400	14	2.5	3.5	43.82
8.7	5.56	10.22	1.96	300	8	2	4	39.97
8.72	3.02	11.42	1.09	400	18	2.5	4	59.43
8.73	3	11.27	1.07	375	18	3	4.5	68.41
8.75	3.22	11.43	11.17	350	16	2	4.5	65.61
8.76	4.13	10.62	1.44	350	12	3	4	49.3
8.77	3.64	11.28	1.34	400	14	2	3.5	43.39
8.85	6.89	9.89	2.31	250	6	2	4.5	41.55
8.86	3.03	11.52	1.09	400	18	2	4	59.05
8.87	4.72	10.6	1.66	325	10	2	4	44.5
8.88	4.07	10.72	1.4	300	12	2.5	5	65.52
8.9	3.02	11.38	1.06	375	18	2.5	4.5	68.08
8.92	4.15	10.75	1.44	350	12	2.5	4	48.78
8.93	5.51	9.98	1.79	225	8	2.5	6.5	73.51
8.95	3.68	10.74	1.24	325	14	3	5	69.01

Table 3 shows that the Q of the inductor drops as the area bets bigger. Thus, if an LC VCO in the tens of MHz is desired, the biggest inductor reported in Table 3 indicates an area consumption of 325 μm × 325 μm with a Q of only 10. On the other hand, while integrated inductors exhibit Q around 10-20, external inductors can have quality factors of more than 35 for inductor values 20 times bigger, as shown in Figure 48. Since the operating frequency of VCO_1 cannot be determined accurately until the MEMS devices are fabricated and characterized, the option of external inductors favors user

customization of the BRN-PLL. For this work, the tank inductor will be selected external and it will be interfaced with a DS version of the negative resistance generator.

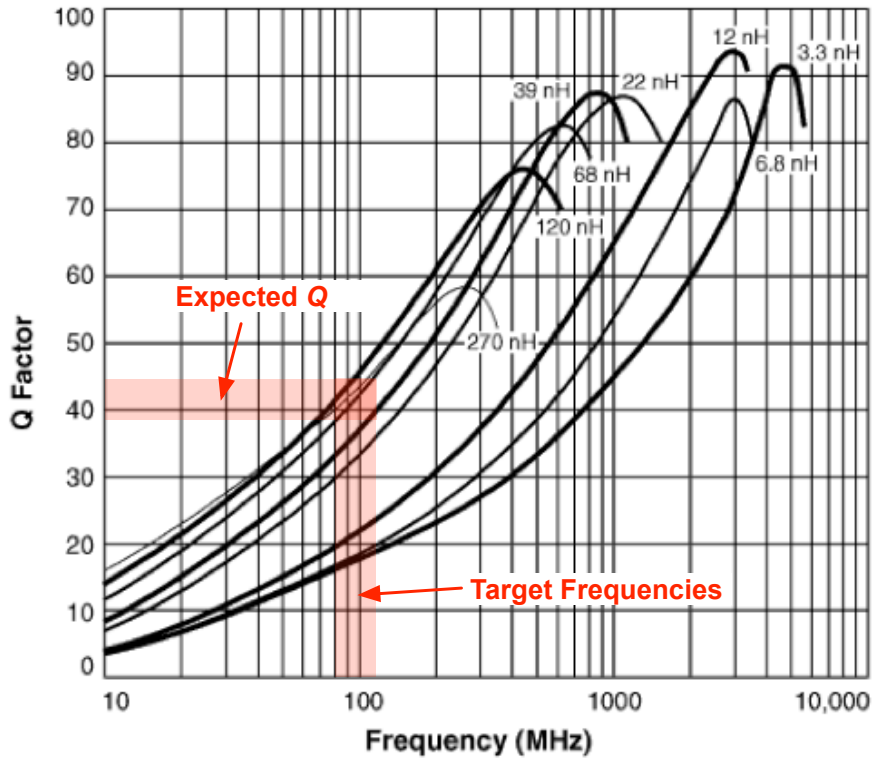


Figure 48. Quality factors vs. frequency for external Coilcraft inductors [55]

To test the performance of the DS LC-VCO, the proper negative resistance generator was taped out along to MIM capacitors with an approximated value of 2pF. An Agilent 54622D oscilloscope was used to capture the transient response of the oscillator. Since the maximum frequency for the measurement equipment is 100MHz, a frequency slightly lower to this limit was targeted. A selected frequency of about 82MHz is calculated using a 330nH inductor and additional 8pF of external capacitors. Figure 49

displays the measured transient response of the DS LC-VCO showing a symmetric waveform with proper amplitude to interface digital circuitry (e.g. PFD).

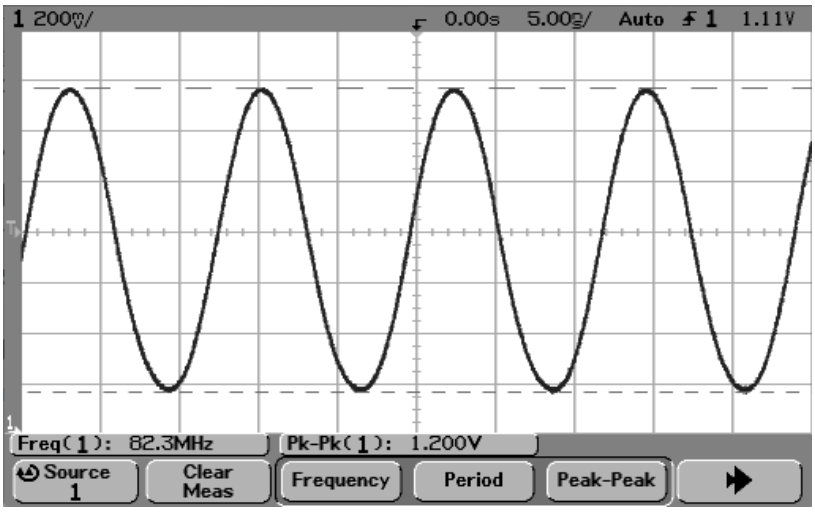


Figure 49. Measured waveform of a double-pair LC-VCO working at 82MHz

Figure 48 estimates that the external inductor will exhibit a Q of about 40 for the selected frequency. The measured PN is compared with a prediction using Leeson's model. The results are presented in Figure 50, and lab measurements follow the PN modeling closely (Figure 51).

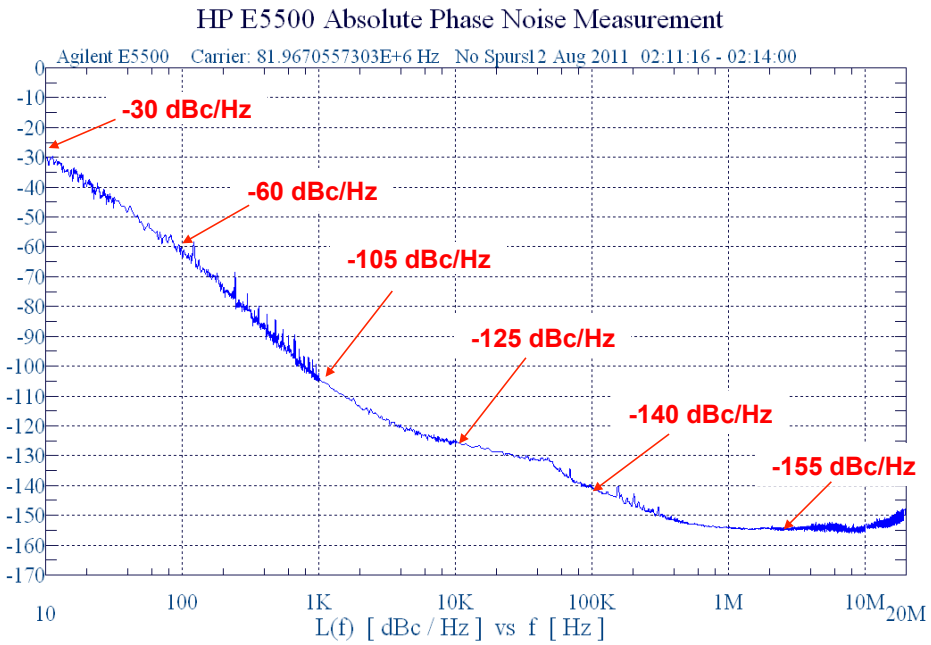


Figure 50. Measured PN of a double-pair LC-VCO working at 82MHz

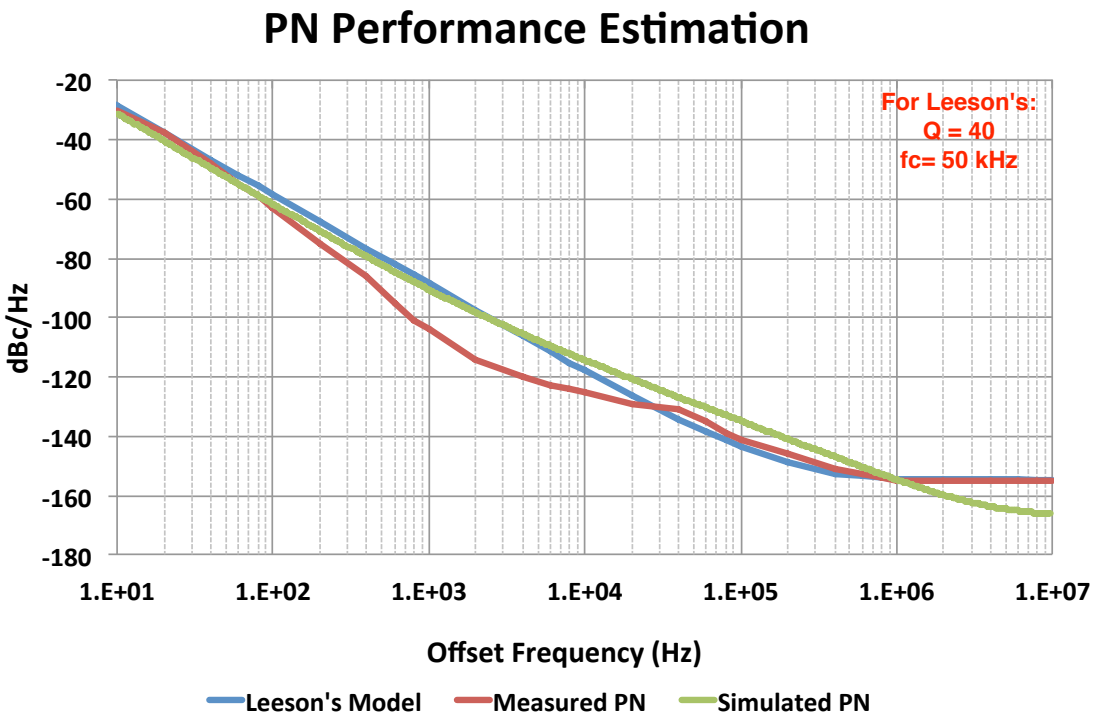


Figure 51. Comparison between the simulated and measured PN of a double-pair LC-VCO working at 82MHz along with the estimation using Leeson's model.

Tuning based on varactors is an effective way to modify the operating frequency. Figure 47 shows that the DS LC-VCO also provides discrete steps for frequency tuning. Thus, for a given discrete step of tuning, varactors are able to provide at least 500kHz without appreciable degradation in PN. Figure 52 reports the simulated and the measured tuning range.

a)

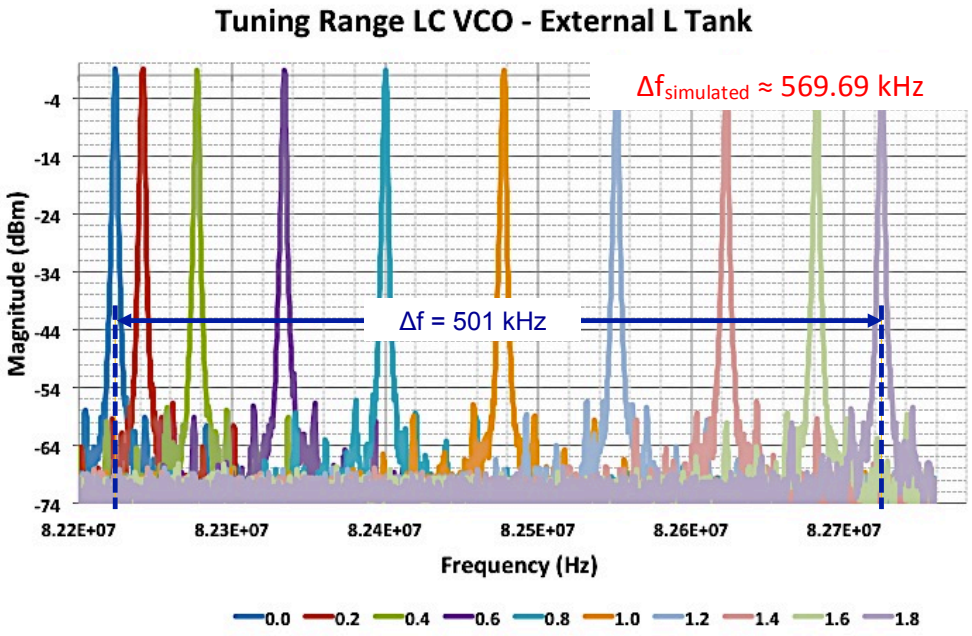


Figure 52. DS LC-VCO tuning range working at 82MHz.

CHAPTER 5

HIGH-*Q* MEMS VCO DESIGN

5.1. Series Tuning Mechanism

5.1.1. Series Varactor Implementation

This tunable element placed in series with the microresonator constitutes itself a challenge when implemented with electronics. As seen in Figure 53, a typical 2-port varactor cannot be used because one of the ports will become AC ground.

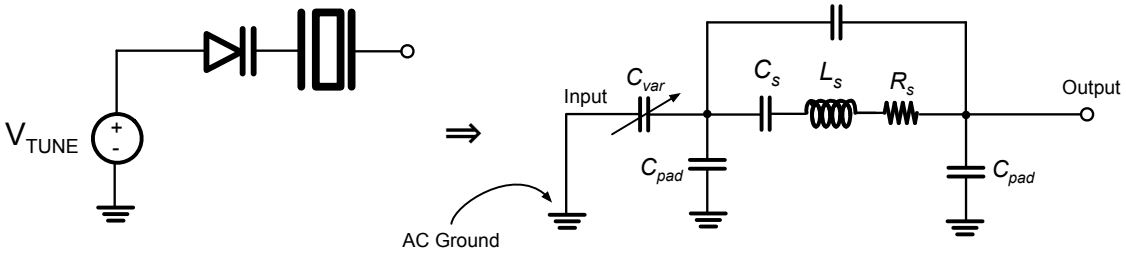


Figure 53. Effect of a typical 2-port varactor as a tuning element in series.

Mixed-signal IC processes such as the TSMC 0.18 μm 1P6M provide varactors that can maximize the range of capacitance change. The varactor is configured with two N^+ diffusions implanted on an N well [56]. In this manner, the strong inversion section is avoided, when a PMOS device is used for configuring the varactor. Figure 54 shows the schematic of the variable capacitor and the expected capacitance change versus voltage.

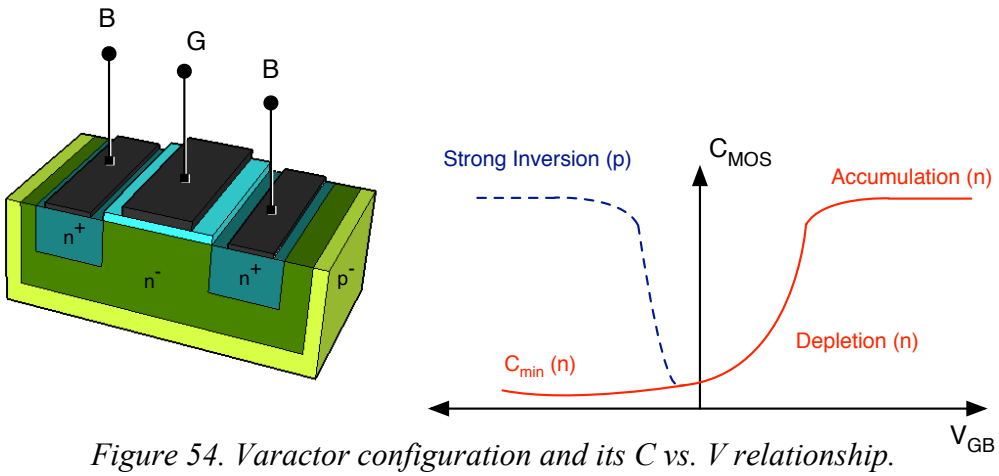


Figure 54. Varactor configuration and its C vs. V relationship.

By examining the equivalent circuit model for this component (Figure 55) [56], two varactors can be placed in series allowing the use of the common-gate terminal as tuning port via a big resistor (Figure 56) [57].

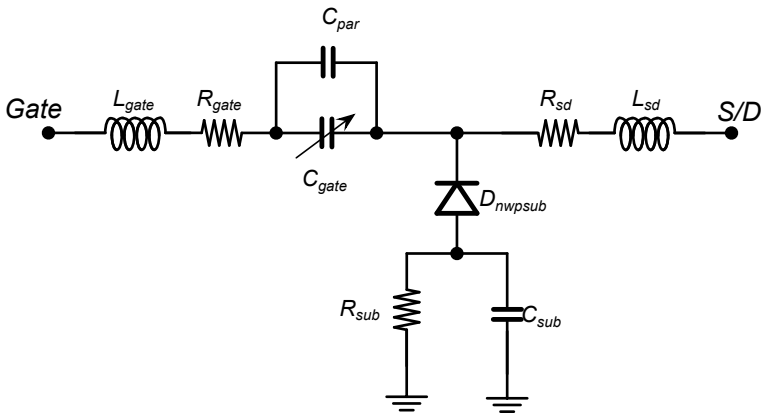


Figure 55. Equivalent circuit model for the TSMC 1P6M 0.18µm varactor [56].

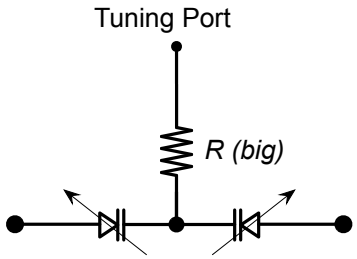


Figure 56. Approach for a series tuning element [57].

Using the model of Figure 55 in the series-varactor configuration of Figure 56, the possible paths for the signal to flow through this element can be observed in Figure 57.

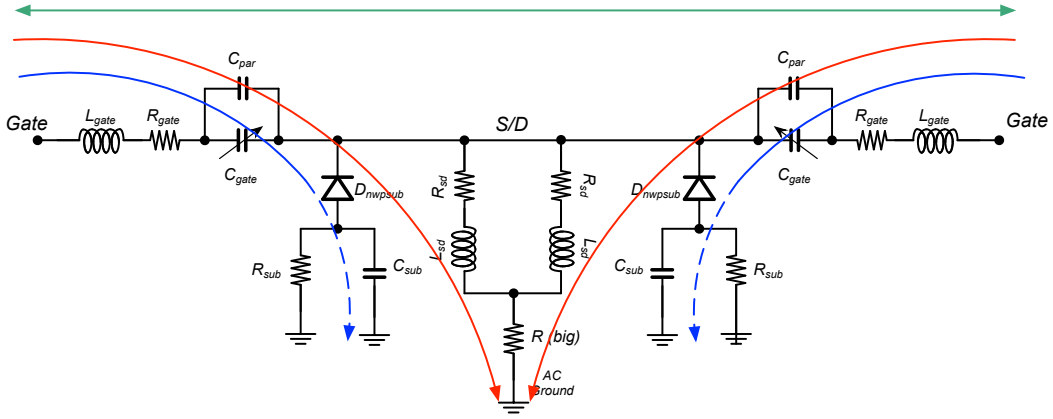


Figure 57. Signal paths through the series-varactor configuration

It can be noticed that the use of a resistor for the tuning port configures a path to ground that will attenuate the signal transmission. The quality factor for this two-port element can be found as [58]

$$Q_{varactor} = -\frac{IM(Y_{11})}{RE(Y_{11})}. \tag{28}$$

Simulation of $Q_{varactor}$ using a tuning resistance (approximately equal to 68kΩ) reveals a maximum value of about 95 at 250MHz and around 20 for the typical frequencies of the MEMS resonators used in this work (Figure 58). Alternatively, employing a reverse-biased diode as interface effectively cancels the losses due to the tuning path (Figure 59). Since the varactor contains capacitors in the forward path, the tuning diode will be floating from a DC point of view, and it will work as a blocking element in AC. The simulation results of Figure 60 show that $Q_{varactor}$ can be greatly improved depending on the operating frequency (100× at 27MHz).

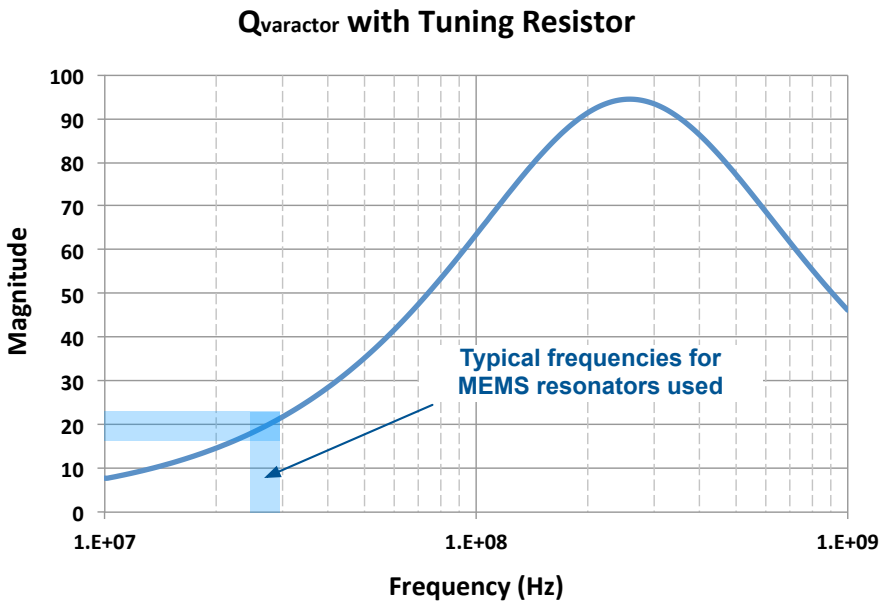


Figure 58. Simulation results for $Q_{varactor}$ using a resistor in the tuning port

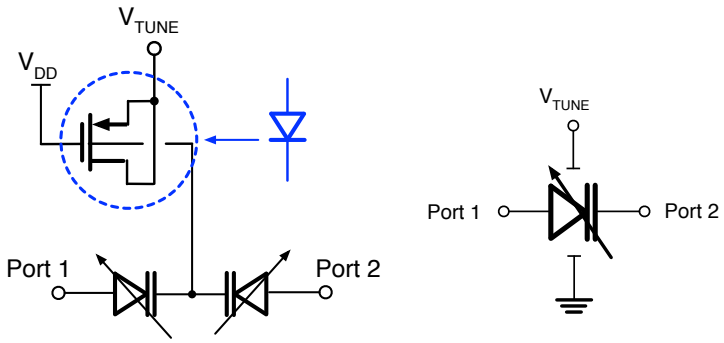


Figure 59. Modified series-varactor configuration using a diode at the tuning port

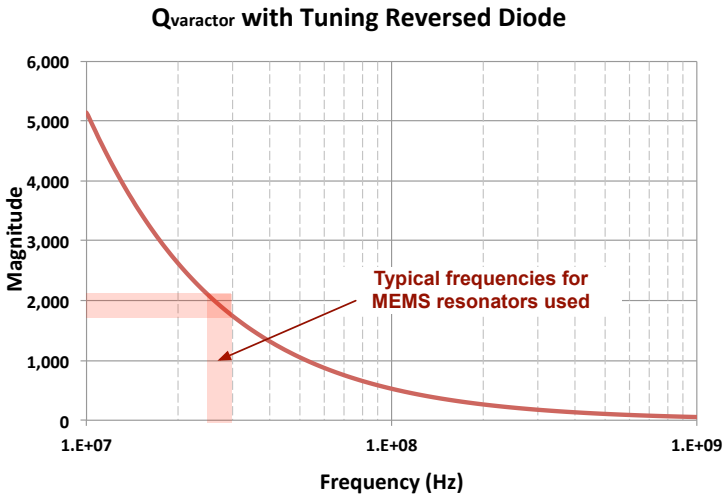


Figure 60. Simulation results for $Q_{varactor}$ using a reversed diode in the tuning port

The parameters for the varactors were selected by trading off capacitance change and absolute value of the element. Equation 11 shows that any capacitance change will have a more pronounced effect in the pulling of the resonance frequency when the absolute value of the varactor is reduced. However, the capacitance change is inversely

proportional to the absolute value indicating that small capacitances are desired but they are susceptible to parasitics. For example, a series-varactor with absolute value around 330fF and capacitance change estimated about 170fF was measured using an Agilent E4980A Precision LCR Meter. Although the maximum measuring frequency for the equipment is 2MHz, the total capacitance change is found to be around 140 fF with a clear tendency to increase with frequency (Figure 61). As observed, according to the varactor value, there is a feedthrough capacitance close to 1.5 pF. The main inconvenience of this situation is that any compensation scheme is not addressing this type of parasitics; therefore, the minimum size for varactors, with minimum capacitance change, does not yield to maximum frequency pulling in this case. Then, it can be seen that proper cancellation of the shunt-parasitic capacitance becomes even more critical.

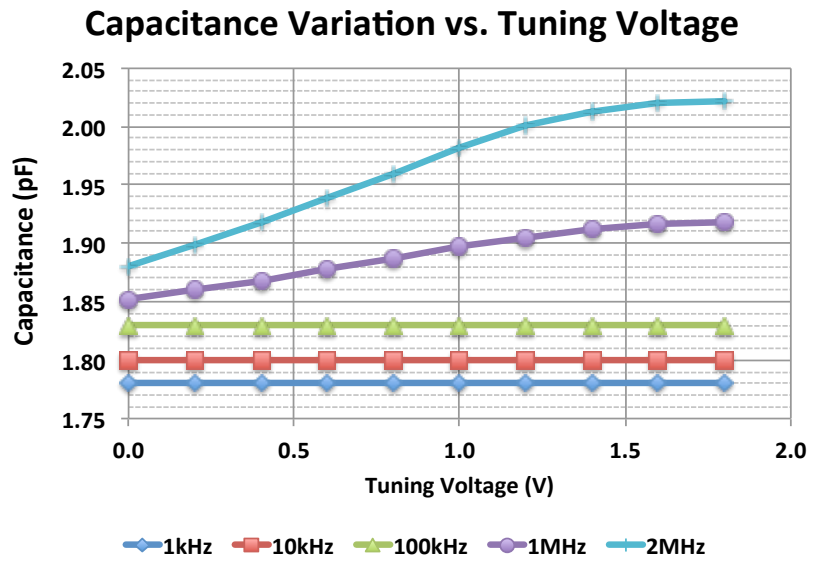


Figure 61. Capacitance change with respect to frequency and tuning voltage

5.1.2. Shunt-Parasitic Capacitance Compensation

The work by [59] offers a clear evaluation of the performance about shunt-parasitic compensation techniques, and focuses on the simplicity of the architectures to favor noise performance. Thus, it employs both single-transistor one-port active inductor and negative capacitor as shown in Figure 62.

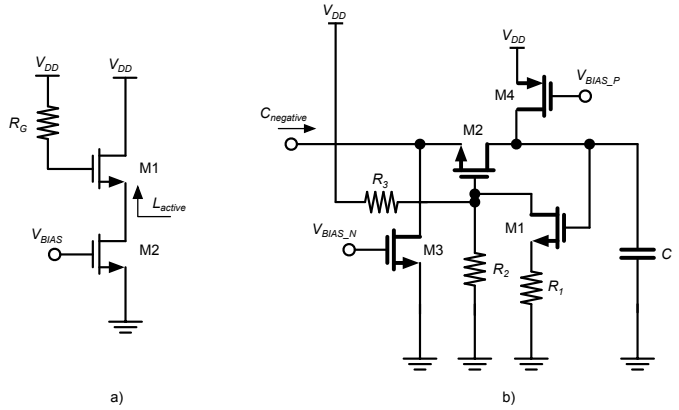


Figure 62. Single-transistor compensation circuits used in [59]. a) Active inductor and b) Negative capacitor.

The active inductor of Figure 62a emulates an inductance directly proportional to R_G and C_{gs1} and inversely related to g_{m1} [60]. The Q for this architecture is low and more suitable to produce large values of inductance. Therefore, although the range of compensation can be possibly wider than that using high-Q architectures, the loading of the resonator, the power consumption and the requirement for an exact value for resonance of the compensation tanks indicate that shunt-parasitic capacitance based on negative capacitor could provide better results. The circuit of Figure 62b is able to generate a negative capacitance [59]. A simplified expression to calculate its value can be

found as the multiplication of C and the ratio between R_1 and the parallel equivalent of R_2 and R_3.

The work of [59] uses the two options of Figure 62 to interface a 427MHz aluminum-nitride-on-silicon (AlN-on-Si) lateral micromechanical resonator, with Q and IL equal to 820 and -9dB, respectively (Equations 8-10 estimate R_s = 181.8Ω, L_s = 55.5μH, and C_s = 2.5 fF). The measured tuning range for the oscillator using active inductor was about 350ppm, while the negative-capacitor version produced a value close to 810ppm, or 2.3× larger tuning range.

Given the results, negative capacitance compensation will be employed for the MEMS-VCO of this work. It can be determined that the resonator will provide a floating node for the varactors; thus, the use of negative capacitors not only compensates the shunt-parasitic capacitance, but also provides proper biasing for the tuning elements. This condition is suggesting that if the negative-capacitor circuit is able to provide a low-voltage condition for the varactors, then the capacitance change will be maximized. Thus, the convenience of the current-inversion NIC for low-voltage applications proposed in [61] will be explored for the MEMS VCO (Figure 63).

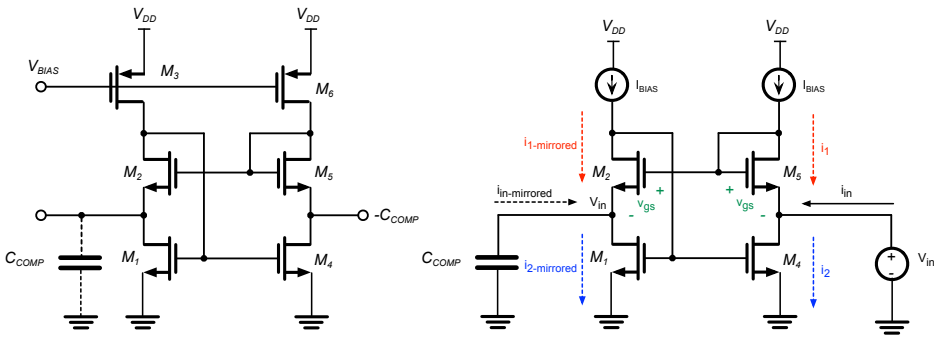


Figure 63. Selected architecture for the negative-capacitor compensation technique.

The architecture of Figure 63 is based on the *Sooch* cascode current mirror [52], which makes the gain error equal to zero, which means that the matching for the current flowing in both branches is maximized, and therefore a closer realization of the algebraic negative of the compensation capacitor. The inclusion of transistor M2 makes both M1 and M4 V_{DS} voltages minimum, which is the desirable condition to maximize the change in the varactors.

Even though, theoretically the current in both branches is the same, the circuit will provide this behavior while M2 remains in saturation, which will occur when V_t is higher that $V_{ov.}$ If this condition is not satisfied, M2 enters triode region and V_{GS} will depend strongly on V_{DS} affecting the theoretical gain voltage. Although in principle, this condition could be undesirable, it is possible to take the partially compensated capacitor and use the residue (C_0 - C_{neg}) to modify the total phase-shift of the resonator for further tuning. The topic of tuning via phase shifting will be covered in more detail in Section 5.2.

Finally, compared to the circuit of Figure 62b, the NIC presented in Figure 63 does not contain resistors which minimizes mismatch due to resistor fabrication.

5.1.3. Transimpedance Amplifier Design

For the case of series tuning, the total losses that the sustaining amplifier needs to overcome are increased by the addition of two series-tuning elements in the loop. Broadband current amplifiers have been proposed to increase the gain while the bandwidth is maintained without increasing excessively the power consumption [62].

A wideband TIA with at least 120dBΩ of gain is designed to interface MEMS devices using the series-tuning technique (Figure 64). The transimpedance stage contains three inverter-based amplifiers with shunt-shunt feedback decoupled from each other through a capacitor C_{DEC}. The inverter-based amplifiers are biased identically, which results in identical small-signal parameters for the transconductances and output resistances. A CS stage is included for extra gain and to provide 180° phase-shift, if needed. A comparator is placed at the oscillator output to work as a digital buffer and to maintain constant amplitude prior to the PN measurement equipment. The objective is to make the comparator as transparent as possible for measurements; thus, the process-independent threshold-voltage compensated comparator available in [63] is used.

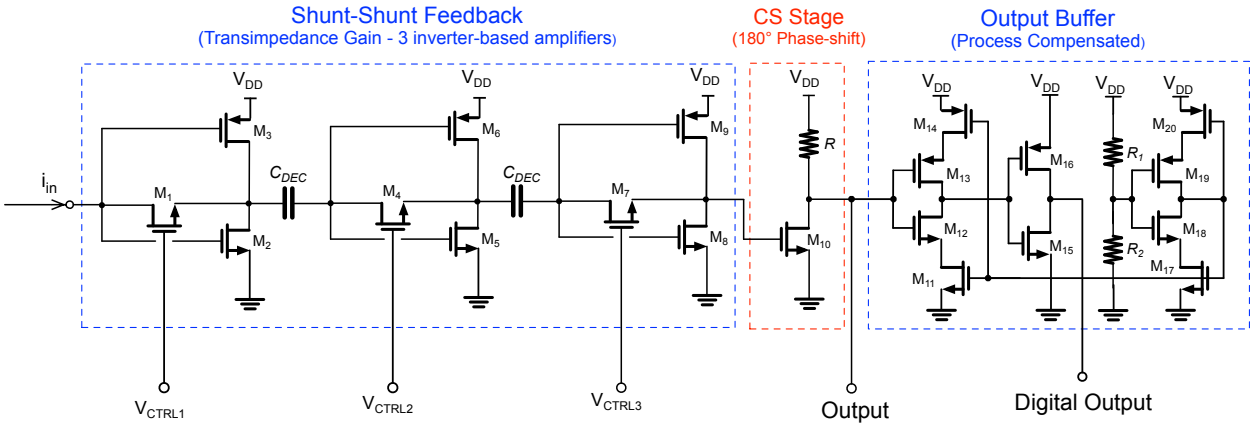


Figure 64. Wideband high gain transimpedance amplifier for interfacing MEMS resonators.

To find the total transimpedance gain for the shunt-shunt feedback stage, the derivation starts at the third inverter-based amplifier ($@V_{CTRL3}$) working toward the input. Hence, the transimpedance gain for this section can be approximated as

$$A_R = \frac{1 - r_{ds7}\left(g_{mn} + g_{mp}\right)}{\frac{1}{r_{dsn} \,||\, r_{dsp}} + g_{mn} + g_{mp}} \approx -r_{ds7} + \frac{1}{g_{mn} + g_{mp}} \approx -r_{ds7}, \tag{29}$$

and the input impedance can be calculated as

$$R_{in} \approx \frac{1}{g_{mn} + g_{mp}}. \tag{30}$$

Next, with Equation 30, the current gain for the second inverter-based amplifier ($@V_{CTRL2}$) becomes

$$A_i = \frac{-r_{ds4} + \frac{1}{g_{mn} + g_{mp}}}{\frac{1}{sC_{DEC}} + \frac{2}{g_{mn} + g_{mp}}}, \tag{31}$$

and working similarly, the current gain for the first inverted-based amplifier ($@V_{CTRL1}$) can be expressed with Equation 31 but replacing r_{ds4} with $r_{ds1.}$ Thus, the complete transimpedance gain can be approximated as

$$A_R \approx \frac{-r_{ds1} \cdot r_{ds4} \cdot r_{ds7}}{\frac{1}{sC_{DEC}} \cdot \frac{1}{sC_{DEC}}}. \tag{32}$$

It is important to notice that tuning the values for the active resistors also includes a phase-shift in the sustaining amplifier by modifying the associated poles with the gates capacitances of each inverter. If r_{ds4} and r_{ds7} are large, the associated poles will be located at low frequency inducing a phase shift close to 180° at the intended operating frequency of the MEMS resonator used in this work (i.e. tens of MHz). Notice that the movable poles associated with the active resistors offer a customizable phase-shifter to account for

the different sources of phase error (device fabrication, electronic compensation, interconnection, etc.).

The next stage of the TIA comprises a CS amplifier that will provide a voltage gain of $g_{m10}R$ and additional 180° of phase shift. Hence, the complete TIA gain can be made tunable between 120dBΩ and 300dBΩ, and becomes suitable to interface MEMS resonators with 0° at the resonance peak. Figure 65 summarizes simulations for the TIA gain and phase.

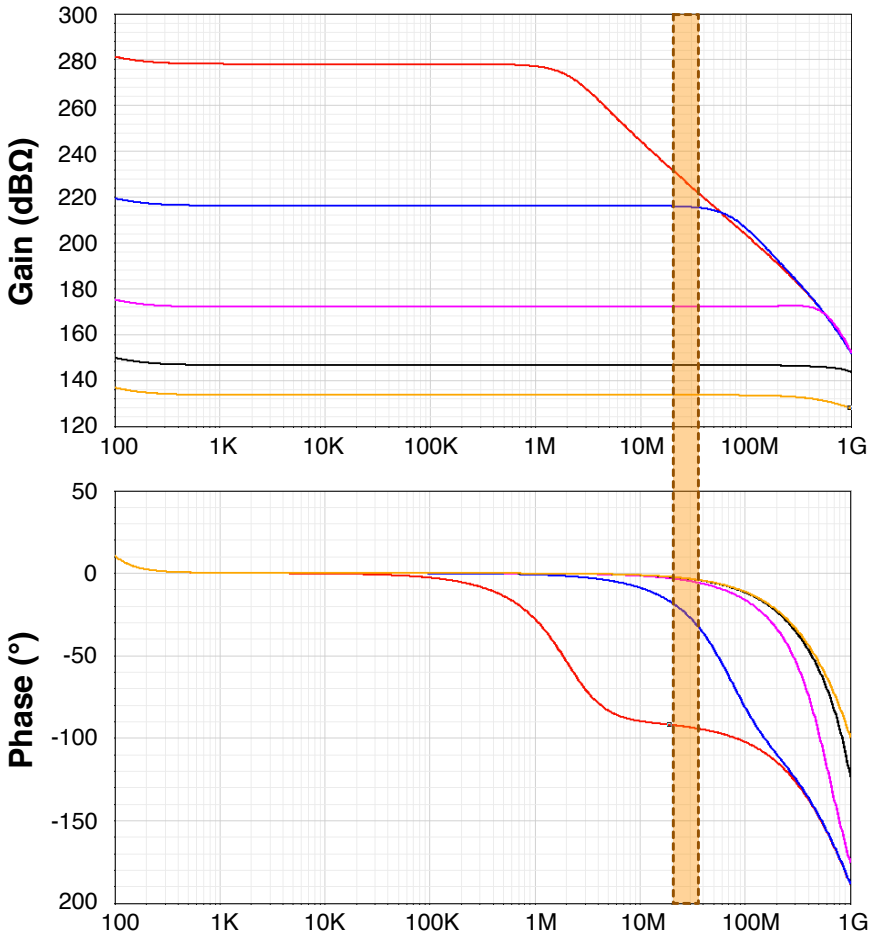


Figure 65. Simulation results for the TIA utilized for the series-tuning technique.

5.1.4. Piezoelectric MEMS Resonator

A composite AlN-on-Si lateral microresonator is employed in this work. The device is fabricated from a 10μm thick silicon-on-insulator (SOI) substrate, and its stack composition and thicknesses are 9/2/0.1/1/0.1μm of Si/SiO2/Mo/AlN/Mo, respectively. The MEMS device is a two-finger electrode design on top of a plate with lateral dimensions of 156μm×250μm. A detail of the device configuration is shown in Figure 66, while Figure 67 shows a scanning-electron-microscope (SEM) image of the resonator. The detailed fabrication process is described in [64].

The two-finger electrode configuration excites and senses an in-plane shear (IPS) mode at 23MHz and a longitudinal extensional (LE) mode at 26MHz. The IPS and LE modes are electrically 180° out of phase with respect to one another (LE mode presents 0° at resonance). The shape of the excited modes is presented on Figure 68. The outlines correspond to the peak displacements of each half cycle of oscillation.

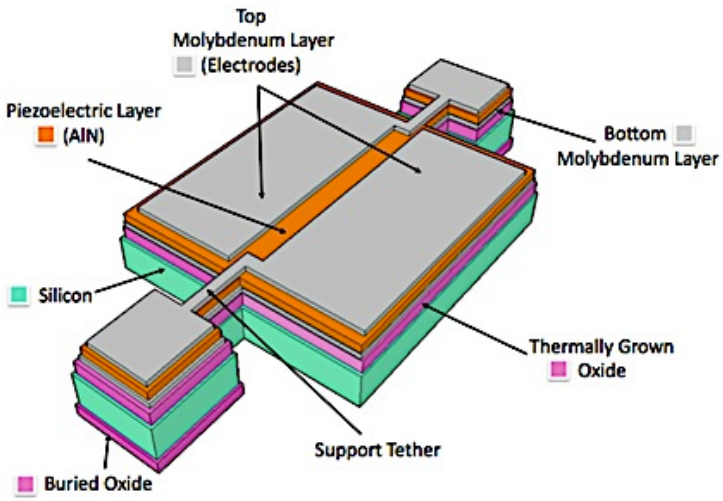


Figure 66. Schematic of the composite AlN-on-Si MEMS resonator illustrating the material layers of the composite stack.

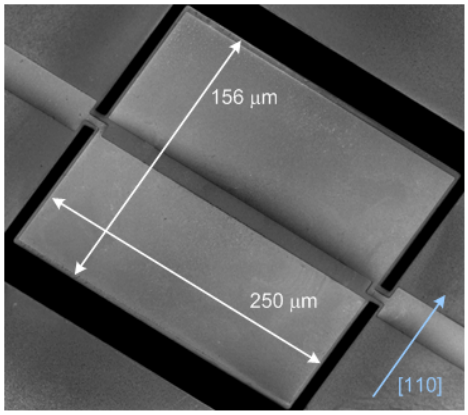


Figure 67. SEM view of the MEMS resonator used.

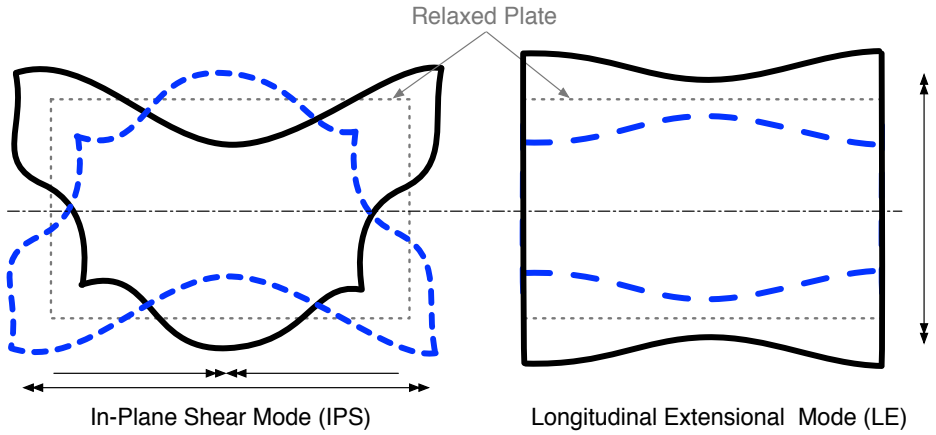


Figure 68. Representation of the IPS and LE resonance-mode shapes. The deformation of the plate is exagerated to reveal details.

Characterization of the modes is performed using an Agilent E5071C VNA for the estimation of the Q and the parameters for the resonator lumped-element model (Figure 69).

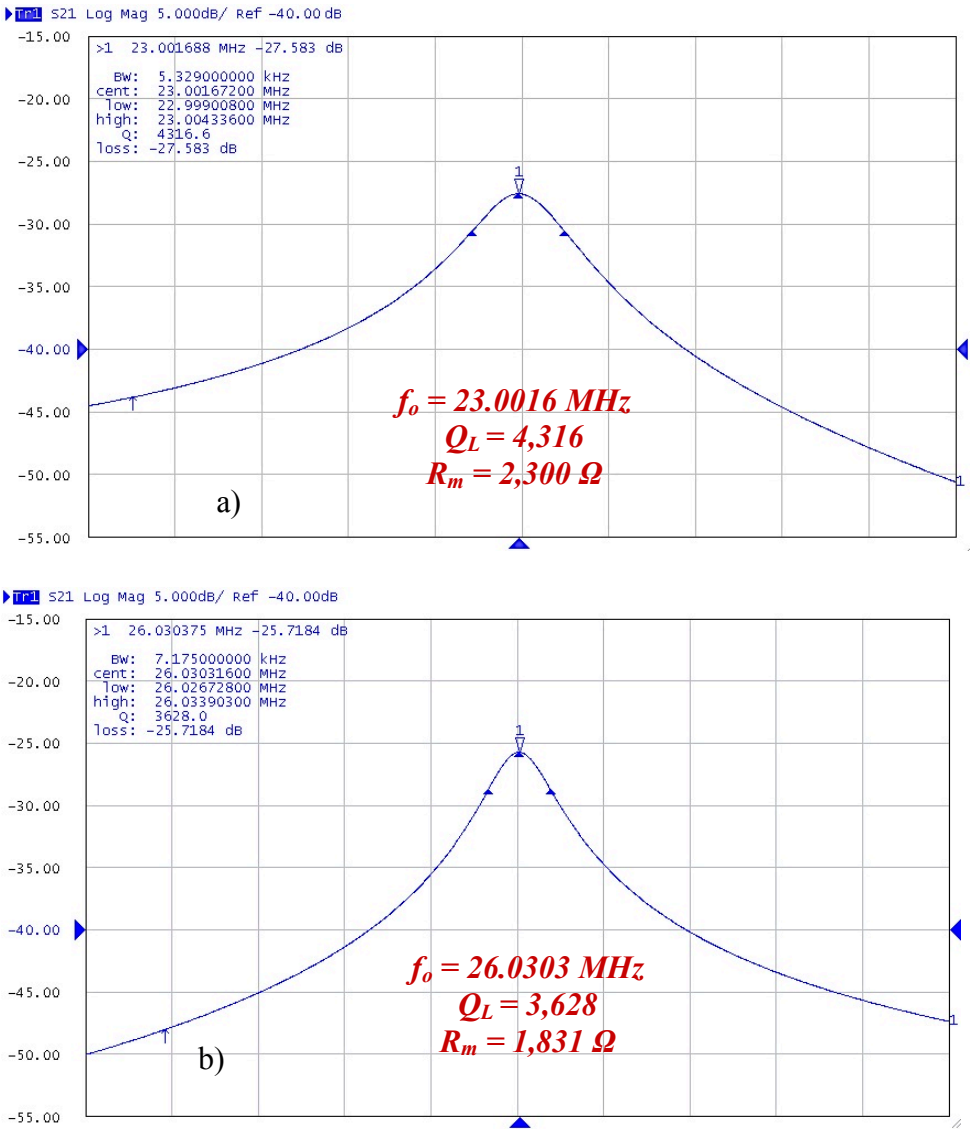


Figure 69. Characterization of the AlN-on-Si two-finger electrode design resonator used in this work. a) IPS mode and b) LE mode.

5.1.5. MEMS-based VCO Characterization

High-*Q* series varactors and the low-voltage negative capacitor of Figure 63 are used to configure the MEMS-VCO for this project. Due to the behavior of the TIA, the proper resonance mode for the selected device is the 26MHz LE, which exhibits 0° phase-shift at the resonance peak.

As commented, the use of negative capacitors not only compensates the shunt parasitic capacitance, but also will provide proper biasing for the varactors. A replica of the negative capacitor is connected at the other end to balance the DC conditions at both ports of the tuning elements; therefore, a blocking capacitor is needed to isolate the TIA. This blocking capacitor can also be used for series tuning, by configuring a discrete bank of capacitors. Schematic for the complete MEMS VCO is summarized in Figures 70 and 71. The described tuning-element set is connected at both ports of the resonator.

Considering a fixed discrete step, the measured tuning range is calculated to be 11.183kHz or almost 450ppm (Figure 72). It is important to notice that compared to the 810ppm tuning range reported in [59], the tuning range obtained for this MEMS VCO is significant given the fact that the estimated value for C_s is 2.5× smaller (for the MEMS resonator LE mode, Equations 8-10 estimate R_s = 1831.97Ω, L_s = 40.6mH, and C_s = 0.92fF). The PN performance was measured showing a consistent behavior for the entire tuning range (Figure 73).

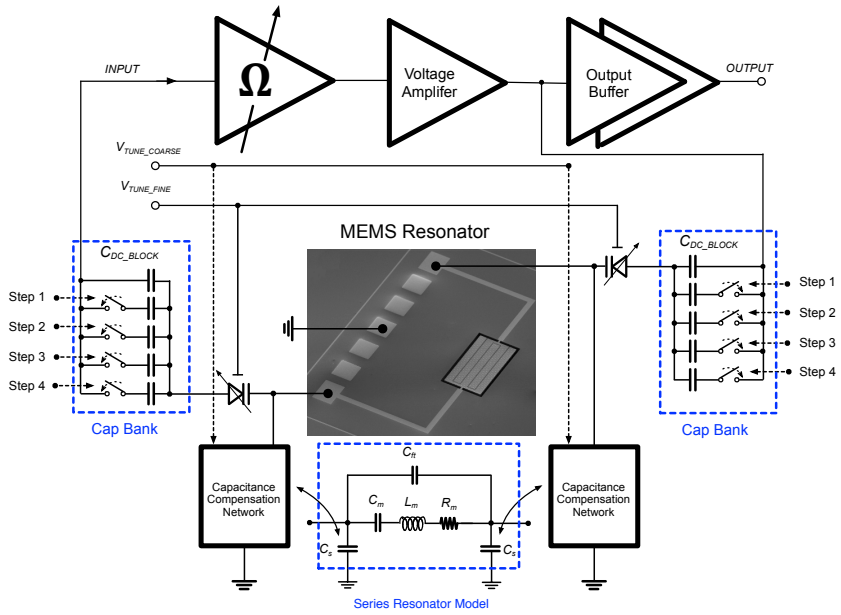


Figure 70. General Block Diagram of the MEMS-VCO

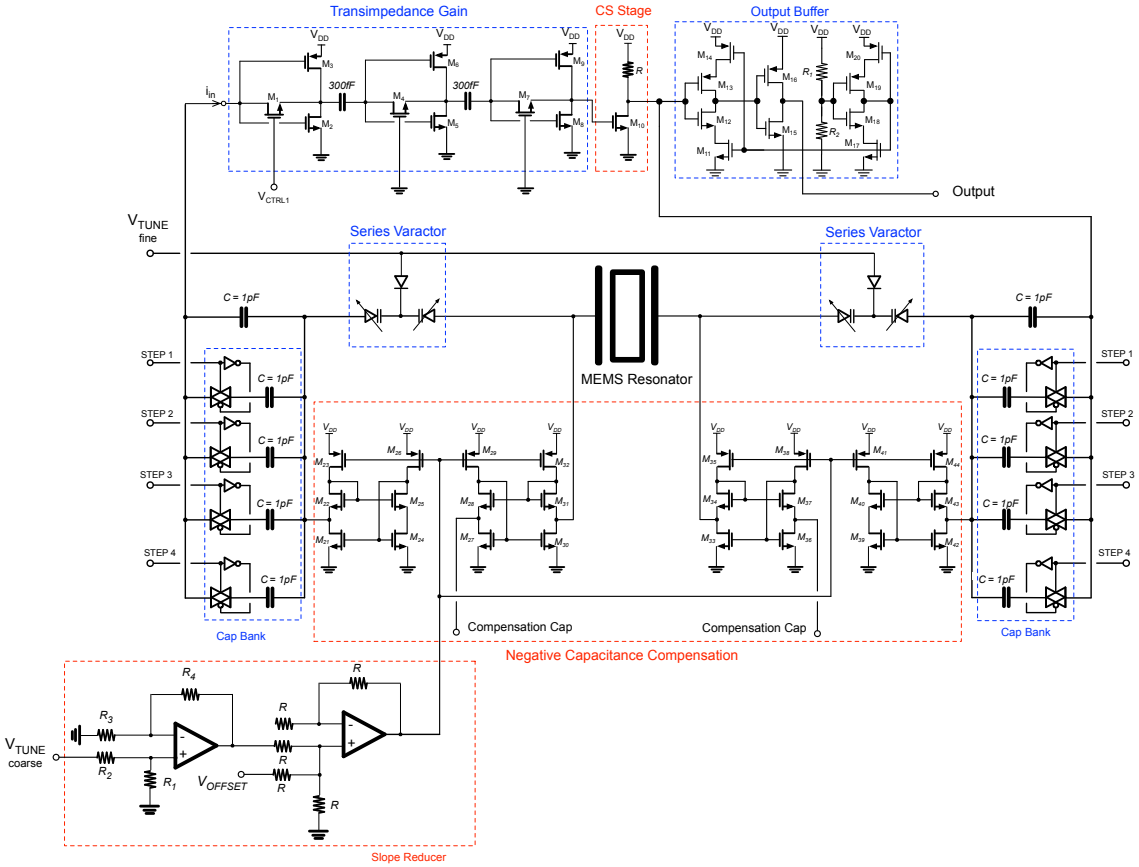


Figure 71. Detailed Block Diagram of the MEMS-VCO

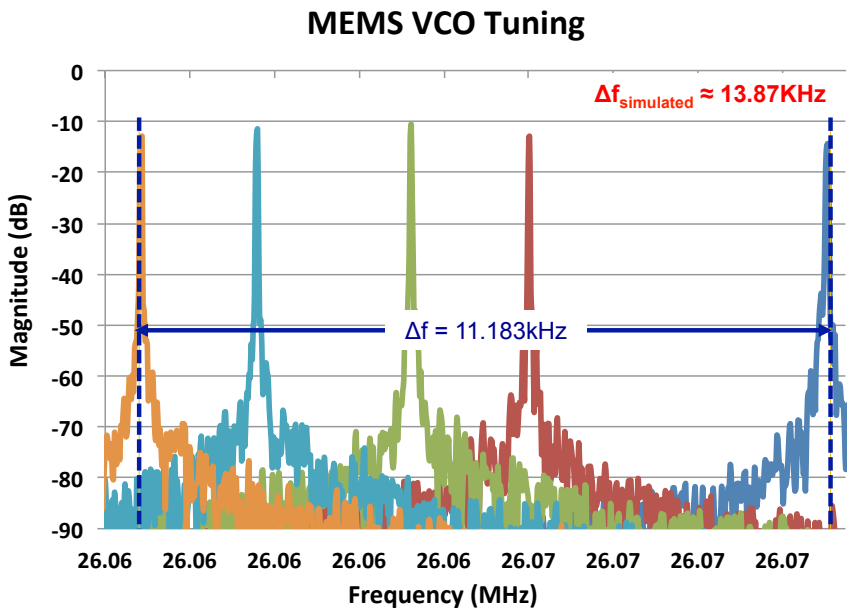


Figure 72. MEMS VCO measured tuning for the series-tuning technique

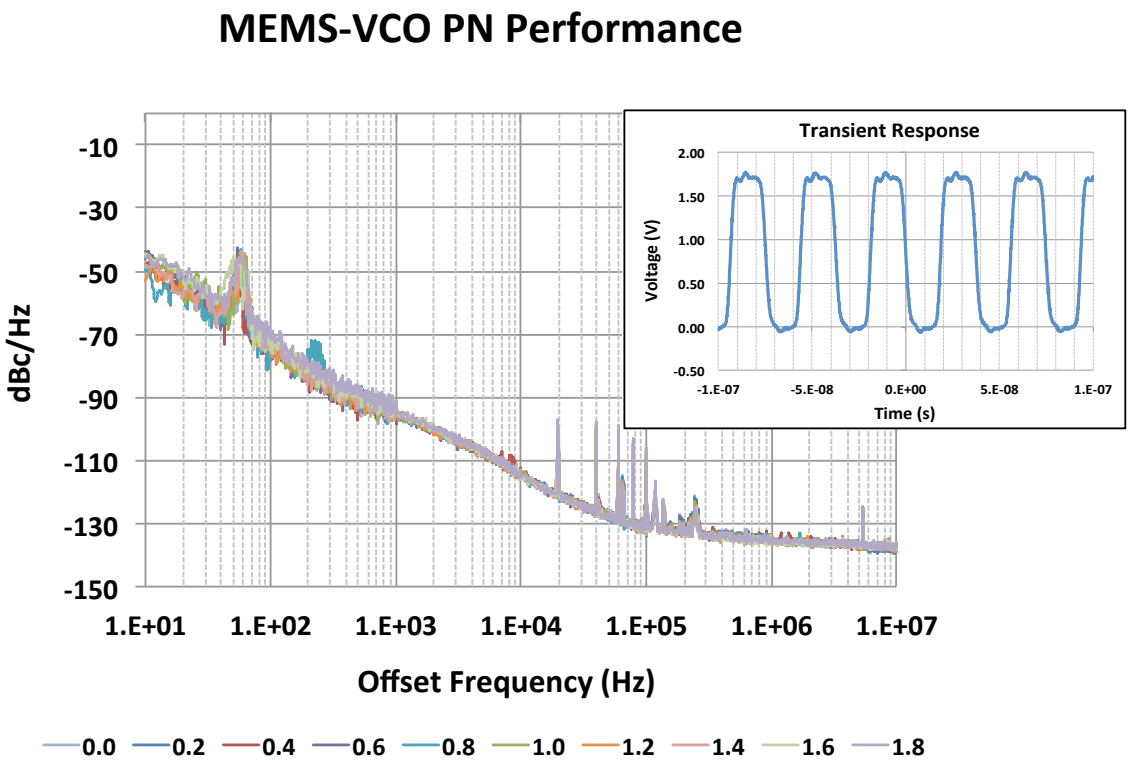


Figure 73. PN performance for the MEMS VCO using the series-tuning technique

5.2. Phase-Shift Tuning Mechanism using MEMS Resonator Nonlinearity

As commented in Section 2.1.2.1, the sustaining-amplifier phase can determine the operating point of the oscillator by matching the resonator phase at a desired oscillation frequency. By modifying the TIA phase satisfying Barkhausen criterion at all times, the oscillator frequency can be tuned following the phase-frequency relationship of the resonator.

With respect to PN performance, the sustaining-amplifier noise propagates through the closed-loop system with amplitude and phase components. However, the amplitude component can be neglected by means of a limiting mechanism, which makes the phase-noise component the main contributor to the sidebands of the oscillator spectrum. Notice that in a system where the amplitude is not well-defined by a limiter circuit, the presence of effects such as power-supply noise or variation may be not negligible due to AM-to-PM conversion mechanisms [65]. Careful circuit design is required to maintain the assumption of PM-only effect in the PN.

To avoid deterioration of the *open-loop Q*, nonlinear effects in a resonator are used to modify the phase-frequency response creating regions where the slope of the transfer function can have a higher value than that in linear regime. The measurement of such an oscillator shows that the PN performance is progressively improved when the phase-shift provided by the sustaining amplifier forces the operating point away from the mechanical resonance [66]. Detuning the oscillator allows the selection of a higher phase-frequency slope that emulates a higher-order filter, minimizing the effect of phase variations on the oscillator frequency [8].

5.2.1. Nonlinear Characterizations of MEMS Resonators

The concept of nonlinearity refers to the relation between the amplitude of vibration and the applied force (i.e., Hooke's law). In a real spring, this relationship is generally nonlinear and given by

$$F_{spring} = -k_1 x - k_2 x^2 - k_3 x^3 + O(x^4), \tag{33}$$

where F_{spring} is the restoring force, x is the displacement, k_1 is the linear term, k_2 and k_3 are the second- and third-order corrections, and $O(x^4)$ aggregates higher-order terms. The displacement-dependent spring constant $\bar{k}$ can be defined as $k_1+k_2x+k_3x^2+\ldots$.

The solution of the equation of motion describing a nonlinear resonator,

$$F_{ext} = M\frac{\partial^2 x}{\partial t^2} + b\frac{\partial x}{\partial t} + \bar{k}x, \tag{34}$$

can be solved considering two cases: unforced-undamped, and forced vibrations. An unforced-undamped resonator is expected to oscillate with constant amplitude at the resonance frequency ω_0. The nonlinear terms in the restoring force will control the amplitude, which changes the oscillation frequency to ω_0' according to the relationship

$$\omega_o{}' = \omega_o + \omega_o\left(\frac{3k_3}{8k_1} - \frac{5k_2^2}{12k_1^2}\right)X_o^2, \tag{35}$$

where X_0 corresponds to the magnitude of the vibration-amplitude distribution [67].

Considering the forcing function as $F\cdot\cos(\omega t)$, the vibration amplitude near resonance is given by

$$X_0 = \frac{F/m}{\sqrt{\left(\omega^2 - \omega'^2_0\right)^2 + \left(\omega\omega'_0/Q\right)^2}}, \tag{36}$$

with ω_0' defined by Equation 35 [67]. From this equation, it can be determined that for k_3 less than $(10/9)\cdot(k_2^2/k_1)$, the resonance peak will shift to lower frequencies. This case is known as *spring softening*, since it can be viewed as being produced by a spring with decreased stiffness. On the other hand, when k_3 is greater than $(10/9)\cdot(k_2^2/k_1)$, the resonance peak can be moved to higher frequencies becoming a case of *spring hardening* [67]. Since the stiffness of the nonlinear system is amplitude-dependent, the vibration-amplitude distribution will also exhibit *bending*. A measure of the maximum vibration amplitude is obtained by calculating the bifurcation point (critical drive) beyond which the amplitude-frequency relationship is no longer a single-valued function [8], [67]. Figure 74 summarizes the *A-f* effect and the corresponding modification of the phase response. More detailed equations for the nonlinear resonator can be extended to take into account the mode shape of the resonant structure [68].

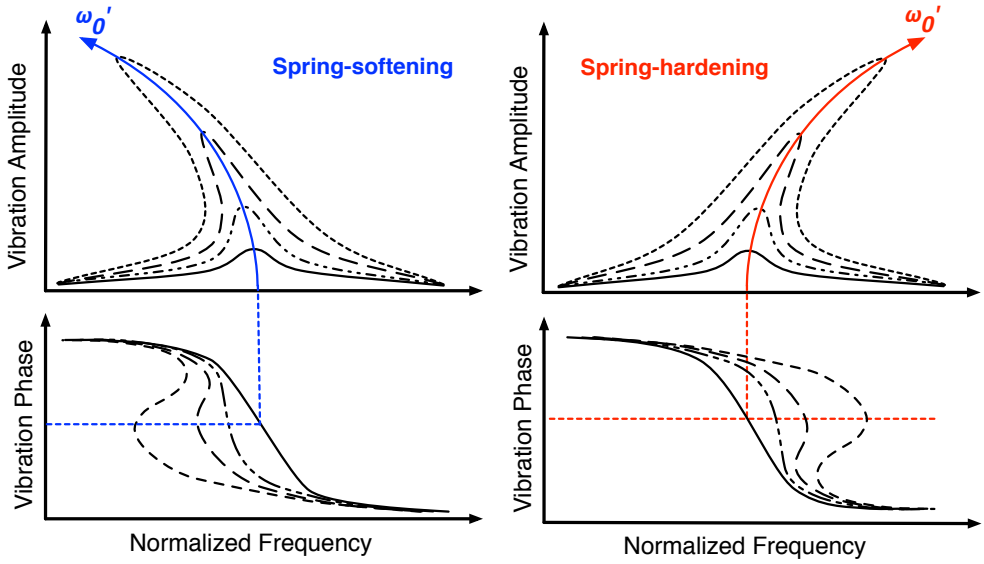


Figure 74. Amplitude and phase responses of a nonlinear resonator under different levels of the amplitude-frequency effect

MEMS resonators can be forced into the nonlinear elastic regime when sufficiently high power is applied to the device structure, creating high energy density [22], [28], [69], [70]. Intrinsic nonlinearities are dependent on effective acoustic velocity, stiffness coefficients, and propagation of the acoustic wave within the device, while induced nonlinearities may arise due to temperature, force, pressure, acceleration, vibration, among other sources [71].

The steepest selection of the phase-frequency slope can be observed in Figure 75. Notice that if the amplitude of the noise sources is not restrained, then the PN response at the output of the oscillator will start to deviate from the slope approximation requiring a more complex representation for the resonator phase transfer function.

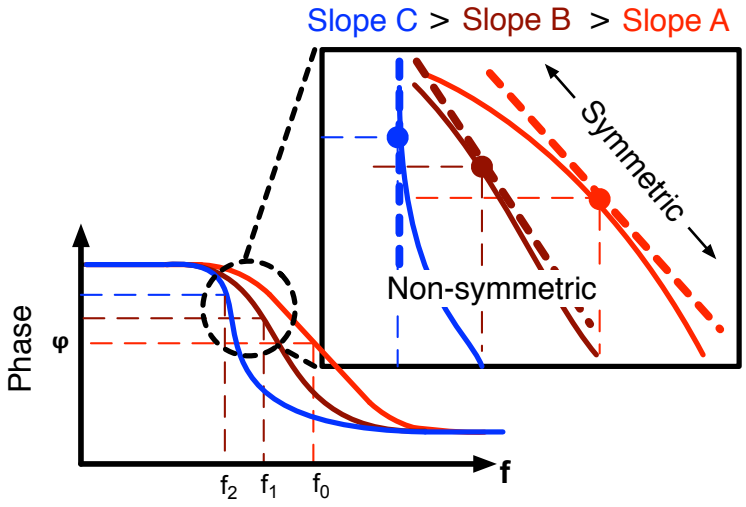


Figure 75. Progression of the phase-frequency slope with nonlinearity

5.2.2. Empirical Phase Noise Model for an Oscillator with a Nonlinear Resonator

An oscillator exhibiting beneficial PN shaping due to nonlinearity can be described by a higher effective Q compared to resonator operation in its linear regime. However, at frequencies very close-to-carrier, the PN is dominated by flicker noise effects [71] and approaches the same PN limit as in linear operation. As the offset frequency moves away from the carrier, the PN then approaches the high effective Q limit. Therefore, a PN formulation must include higher-order terms to describe this transition.

Available PN models [31, 72-74] cannot properly capture the progressive improvement observed in this work. This is because the highest order term described in these models is limited to $1/f^3$. In particular, the work from [73] uses the state-space mathematics to explain this term when an automatic amplitude control circuit is used to avoid the nonlinearity of the MEMS resonator. On the other hand, the model proposed by [74] acknowledges the possibility of improved PN due to proper phase tuning of a nonlinear resonator. The expected results are determined by a linear approximation to the phase-frequency slope at the operating frequency that ultimately yields a $1/f^3$ maximum PN term. The experimental results reported in [75] demonstrate this characteristic of the model.

Therefore, a comprehensive empirical PN model for resonator-based oscillators that encompasses both linear and nonlinear operation of the resonator will be presented.

5.2.2.1. Noise of the Sustaining Amplifier

Thermal noise of the amplifier is directly related to the noise factor F defined as the ratio of the output noise of the actual amplifier to that of an equivalent noiseless version

[76]. Using F and dividing by the available signal power P_s, its noise power-density is defined as

$$S_{wn\_amp}(\omega) \approx \frac{Fk_BT}{P_s} \ , \tag{37}$$

where k_B and T are the Boltzmann constant and temperature, respectively. The thermal-noise power density has a white spectrum with respect to the frequency.

In addition, the sustaining amplifier also contains non-white effects attributed to flicker noise. Transistor-based circuits, whose transconductance is dependent on the bias point, can inject phase shifts resulting in a low-frequency phase modulation [74]. The PN contribution due to the flicker noise is equal to

$$S_{flicker\_amp}\left(\omega\right) \approx \frac{\alpha}{\omega}, \tag{38}$$

where α is a fitting constant dependent on the active devices of the TIA [52]. Considering that white- and flicker-noise sources are uncorrelated, the total noise of the amplifier can be expressed as

$$S_{amp}\left(\omega\right) \approx \frac{\alpha}{\omega} + \frac{Fk_BT}{P_s}, \tag{39}$$

or equivalently

$$S_{amp}\left(\omega\right) \approx \frac{Fk_BT}{P_s}\left(1 + \frac{\beta}{\omega}\right), \tag{40}$$

with β defined as the corner frequency where the flicker- and white-noise components become equal. The estimation of β is empirical and about independent of the oscillation power. Thus, when the power is reduced, the thermal noise is increased creating the effect of a reduced the value of β [77].

5.2.2.2. Noise of the Nonlinear Resonator

The noise spectrum due to Brownian-motion noise can be approximated as [78]

$$S_{wn\_res}(\omega) \approx 2k_B T \,|\, Z_{tank}(\omega_o) \,|\,, \tag{41}$$

where Z_{tank} is the resonator series-equivalent impedance at the oscillation frequency ω_o. If ω_o matches the resonance frequency, the motional capacitance (C_s) and inductance (L_s) from the lumped-element model cancel out, and $|Z_{tank}|$ equals the motional resistance (R_s) (Figure 76). However, in the nonlinear regime, the resonator operates with a small detuning that increases $|Z_{tank}|$ and includes a phase shift that needs to be compensated by the sustaining amplifier to satisfy Barkhausen criterion. Thus, the white-noise contribution of the resonator scales with the motional impedance. The net effect of detuning will increase the noise floor of the oscillator, unless the dominant noise sources stem from the electronics.

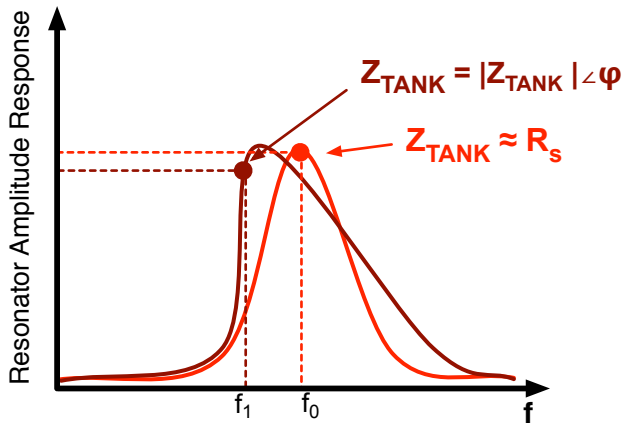


Figure 76. A detuned resonator can operate with increased phase-frequency slope. Gain and phase tuning are required to satisfy Barkhausen criterion.

Microresonators can have several sources of flicker noise when nonlinearity is attributed to elevated drive levels. The resonance frequency can be affected by stress in the deposited thin metal films in piezoelectric devices related to the third-order elastic coefficients of the structural material [69], [79], [80]. Dielectric materials present in the resonator (e.g. AlN) can exhibit hysteretic damping [81]. A resonator exhibits flicker noise given by

$$S_{res\_flicker}(\omega) \approx 2k_B T \frac{r}{1+4\pi^2 r^2 C^2} \frac{1}{f}, \tag{42}$$

where r is a coefficient capturing the hysteresis in the film due to dielectric loss, and C is the capacitance of the piezoelectric stack [81]. For the case of AlN, r is related to the dielectric loss tangent, which is approximately constant down to a few hundred Hertz [82], indicating that the resonator could produce additional flicker noise. Additionally, a form of Johnson noise can be present since self-heating becomes significant for microresonators. Elevated power generates a current associated with random motion of charge carriers in the body of the MEMS device that can be classified as white frequency noise [71].

Design of amplitude control circuitry could mitigate some of the non-white processes induced in the device [73], [83]; however, for piezoelectrically-transduced resonators, the drive level is the mechanism employed to induce beneficial nonlinearity, and the amplitude mechanism utilized is waveform clipping by the sustaining amplifier.

5.2.2.3. The Leeson Effect

A resonant device can be expressed as a selective band-pass filter with impulse response $h(t)$, resonance frequency ω_0 and quality factor Q. When the phase is the

variable of interest, the resonator can be expressed with an equivalent first-order low-pass version $h_{LP}(t)$ with a pole equal to $\omega_0/2Q$ defining the Leeson corner frequency, f_L [84].

After the oscillator is configured, and the gain of the sustaining amplifier reaches steady state, the PN transfer function $H_{LP}(s)$ of the closed-loop system can be derived as [77]

$$H_{LP}(s) = \frac{s + 2\pi f_L}{s}, \tag{43}$$

and the output noise spectral density can be found by multiplying the input spectral noise density and the squared magnitude of $H_{LP}(s)$. Therefore, the Leeson effect is defined as the multiplication by f^{-2} of the PN below the Leeson corner frequency. Equation 44 shows the expression for the output-noise spectral density for this case as

$$S_{\theta_o}(\omega) = S_{flicker+white}(\omega) \cdot \left[1 + \left(\frac{\omega_o}{2Q_L}\right)^2 \cdot \frac{1}{\omega^2}\right], \tag{44}$$

where $S_{flicker+white}(\omega)$ corresponds to the power spectral density of the flicker- and white-noise sources for both amplifier and resonator. Equation 44 is the well-known Leeson's model [31].

Figure 77a shows the squared magnitude of the closed-loop system, and Figure 77b depicts how the PN at the output will be configured when the output spectrum noise density is determined. Notice that Figure 77 shows the case of high-Q resonators, which is the case of the MEMS devices considered in this work, where the flicker noise corner is much higher that the Lesson corner frequency (f_L),

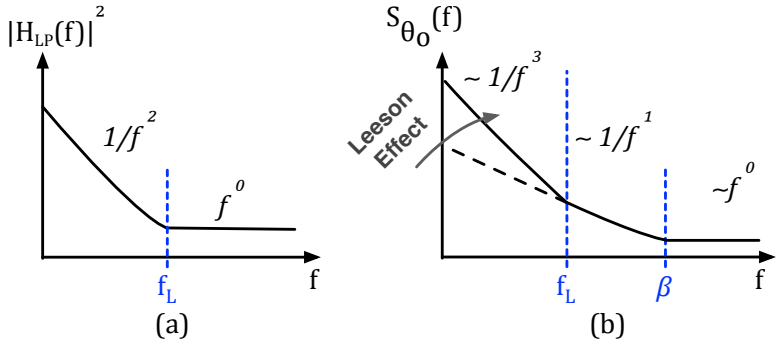


Figure 77. a) Squared magnitude of resonator as phase filter. b) The Leeson effect for a first-order equivalent low-pass resonator [77].

For a nonlinear resonator, the associated low-pass transfer function $H_{LP\_NL}(\omega)$ will be equivalent to a higher-order filter, with order proportional to the strength of the induced nonlinearity. The Leeson effect is more pronounced due to an elevated number of roots in the resonator transfer function that increases the slope roll-off (Figure 78).

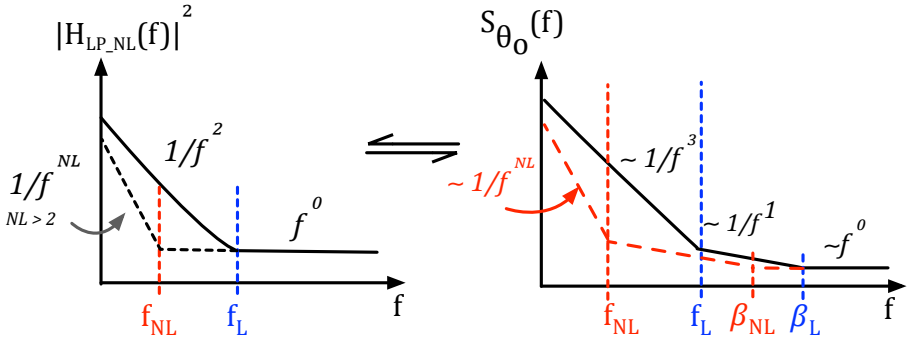


Figure 78. A higher–order phase filter reduces the frequency of the Leeson effect and produces a steeper slope close to the carrier.

Mathematically, the transfer-function of the higher-order filter can be described by using a truncated power series of the exponential function with a number of terms equal to the order of the filter. This selection also allows a description of how the noise sources are modified by the asymmetry in the nonlinear resonator transfer function. When the power series is used, a parameter N is defined as the ratio between the slopes in nonlinear regime at the detuned frequency and in linear operation at resonance. This series approximation uses a higher effective Q equal to $N \cdot Q_L$, where Q_L denotes the loaded quality factor in linear operation.

The parameter β in the associated input spectral density will be affected by several factors. From a resonator point of view, the detuning that selects the steeper phase-frequency slope also increases the equivalent motional impedance of the MEMS device, and therefore the associated white-noise contribution. However, if the elevated drive power generates a signal that makes the sustaining amplifier to operate as a hard limiter, then noise folding produced for this switching operation can dominate the far-from-carrier contribution. In any case, it is expected that the nonlinear oscillator will have an increased noise floor that will reduce the parameter β, configuring what is known as a noise-corrected oscillator [77].

Starting at linear operation, Equation 44 can be modified to give the form of the power series of the exponential function as

$$S_{\theta_o}(\omega) = S_{flicker+white}(\omega) \cdot \left[1 + \frac{1}{2!} \left(\frac{\sqrt{2}\omega_o}{1 \cdot 2Q_L} \right)^2 \cdot \frac{1}{\omega^2} \right]. \tag{45}$$

The second-order term ω^{-2} reflecting the Leeson effect and $S_{flicker+white}(\omega)$ containing noise processes that vary with ω and ω^{-1} can be viewed as the first three terms of the

series expansion for the first-order low-pass equivalent of the resonator. Hence, when operated in nonlinear regime, the required higher-order components can be obtained from the general term

$$S_{\theta_o}(\omega) = S_{flicker+white\_NL}(\omega) \cdot \left[1 + \sum_{k=2}^{N+1} \frac{1}{k!} \left(\frac{\sqrt{2}}{k-1} \frac{\omega_o}{N \cdot 2Q_L} \right)^k \cdot \frac{1}{\omega^k} \right], \quad (46)$$

which provides an approximation of the expression for the phase filter of order *N*. Notice that the power spectral density of white- and flicker- noise processes becomes $S_{flicker+white\_NL}(\omega)$ because their contribution is determined for the specific operating conditions (power and detuning). Equation 46 is a general expression that considers different levels of beneficial nonlinearity and reduces to Leeson's model for *N* equal to one (linear operation of the resonator). Thus, for the theoretical PN models that consider the transfer function of the resonator, the power series expansion can become an alternative to capture the effect of increased oscillator *Q*.

5.2.2.4. Experimental Verification of the Nonlinear Oscillator: Phase Noise and Tuning

The same MEMS resonator described in Section 5.1.4 is used for testing the nonlinear oscillator. Device characterization is performed using an Agilent E5071C VNA for the estimation of the Q_L and motional resistance (Figure 69). Power-induced nonlinearity is verified using a Mini-Circuits ZFL-1000VH power amplifier.

The onset of nonlinearity in the 23MHz IPS mode occurs close to +5dBm, and the device can withstand power levels of at least +30dBm. A similar onset is observed for the 26MHz LE mode, but the resonator fractures at about +20dBm, failing at the corners of the support tethers where the stress concentration is high. The IPS mode is more

susceptible to nonlinearity due to the controlling combination of third-order stiffness components of silicon, which is the main structural material of the resonators. For illustration, Figure 79 shows the progression of the nonlinear effect as the power supplied to the IPS mode is increased.

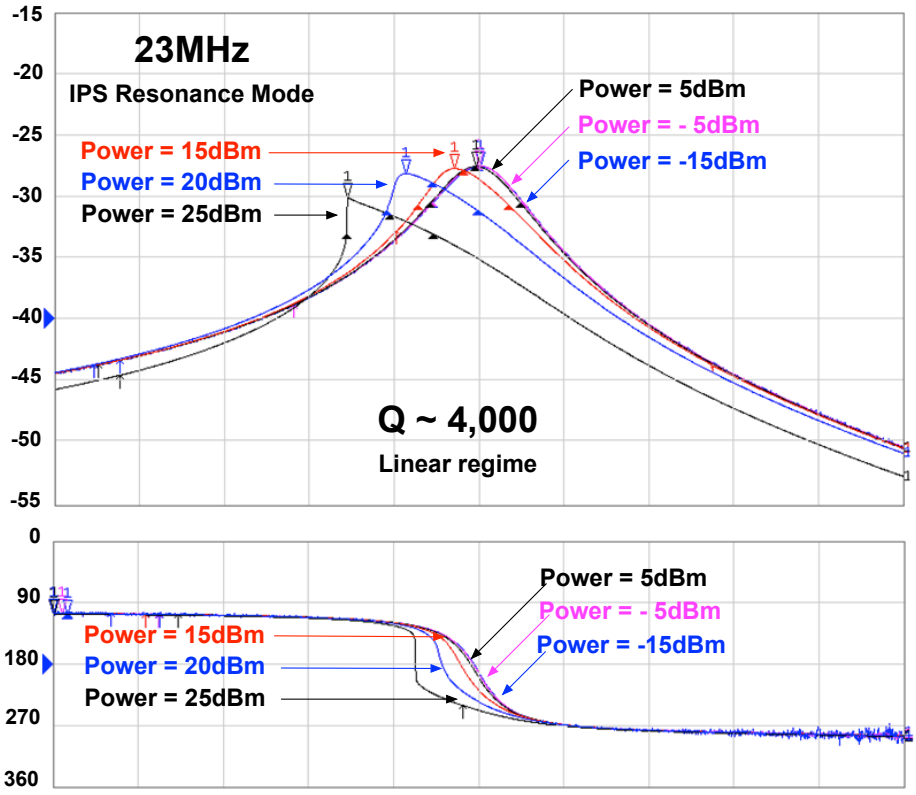


Figure 79. Magnitude and phase frequency plots of the resonator 23MHz-IPS mode for increased power levels

Since the IPS mode presents 180° at resonance and for modifying the oscillation frequency no tuning elements in series are required, a basic inverter-based TIA is used to

interface the MEMS resonator (Figure 80). This TIA also has a CS stage to make it suitable for the LE mode. Thus, the sustaining amplifier provides interface ports to operate with either 0° or 180° phase-shift resonance modes. Similarly, to the circuit of Figure 64, the input-stage feedback resistor is implemented with a MOS transistor whose operation is controlled by the gate voltage, V_{CTRL}, and simultaneously modifies the phase-shift provided by the TIA. This embedded phase shifter provides a means to move along the resonance curve to explore tuning and looking for steeper phase-frequency slopes that will improve the PN. Again, the comparator at the output works as a digital buffer and maintains constant amplitude prior to the measurements.

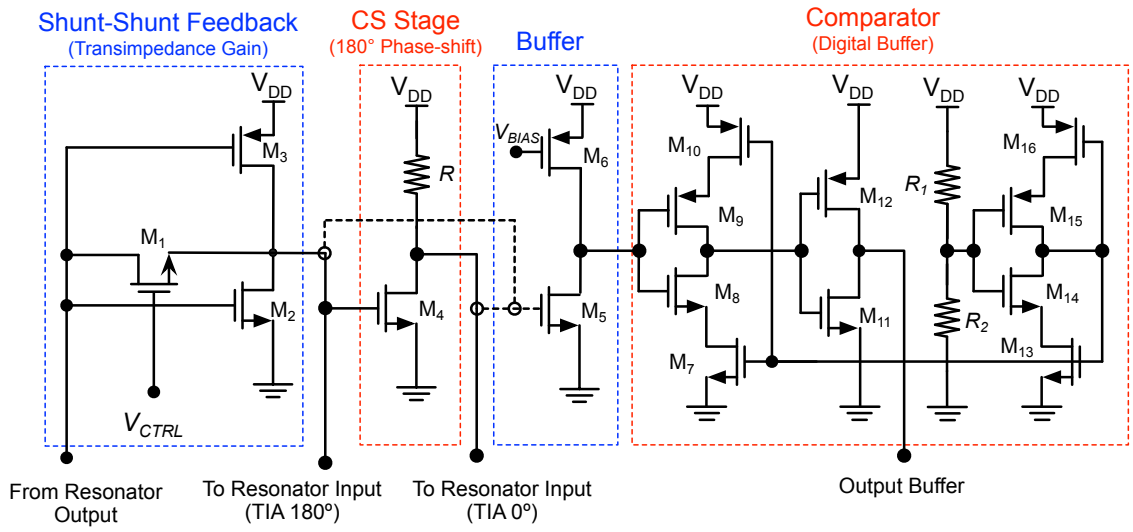


Figure 80. Transimpedance Amplifier Schematic. The generic TIA provides 0° and 180° ports to interface several MEMS devices and resonance modes.

The nonlinear nature of silicon becomes apparent for resonators driven at high amplitudes, and the nonlinearities are assumed to be stiffness-induced for the cases

considered. The silicon third-order elastic coefficients are negative for the modes of interest, and an adequate description of the resonator behavior can be obtained using a second-order displacement-dependent spring constant $\bar{k}$ $(k_1 + k_2 x + k_3 x^2)$. Nonzero k_2 and negative k_3 are identified [85] according to the nonlinear strain-dependent Young's modulus of the main structural material [86].

Equation 34 can be implemented with a large-signal S-parameter simulator (e.g. Advance Design System - ADS) to obtain an estimate of *N*. F_{ext} can be modeled with an independent current source, and spring and damping forces with voltage-controlled current sources [87]. Nonlinearity is taking into account by using a polynomial voltage-controlled current source for the spring force. The electrical-domain model for the nonlinear resonator can be described by Equations 47-49 that correspond to the equivalent circuit of Figure 83.

$$V_X = \frac{1}{sC} V_V = \frac{1}{s} V_V \qquad V_V = sV_X , \tag{47}$$

$$V_V = \frac{1}{sM} i_{total} , \; sV_X = \frac{1}{sM}\left(i_{ext} - bV_V - k_1 V_X - k_2 V_X^2 - k_3 V_X^3\right) , \tag{48}$$

$$i_{ext} = s^2 M V_X + bsV_X + k_1 V_X + k_2 V_X^2 + k_3 V_X^3 . \tag{49}$$

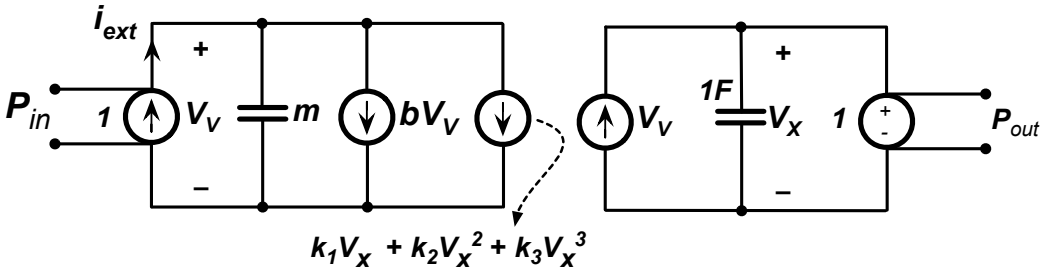


Figure 81. Circuit modeling for the nonlinear resonator using a large-signal S-parameter simulator (ADS).

The parameters for this electrical equivalent circuit can be determined from the S-parameter measurements of the considered MEMS resonator, which includes a calculation for k_1. Estimation of k_2 and k_3 can be done by fitting the measured S_{21} parameter at a specific power level by evaluation of the correlation factor between measurements and simulations. The factor N is calculated by the ratio of the maxima of the phase-response derivatives for both nonlinear and linear operation.

From Figure 69, the worst-case scenario for resonator losses corresponds to a motional resistance equal to 2,300Ω or about 68dBΩ. The sustaining amplifier of Figure 80 provides a transimpedance gain close to 100 dBΩ, which is sufficient to overcome such level of resonator loss. Since the sustaining amplifier does not include an amplitude control circuit, the waveform grows until the large signal saturates the amplifier, hard clipping the output. Amplifier saturation becomes an effective form of amplitude control and still allows increased power to drive the resonator. Due to clipping of the generated waveform, amplitude variations are minimized reducing the AM-to-PM conversion due to the *A-f* effect. Power delivered to the resonator will remain constant if the power-supply variation is negligible.

A 5V supply voltage is utilized to bias the electronics fabricated on a 0.5μm 2P3M CMOS process. To find the equivalent power that the VNA would deliver to the resonator during the parameter characterization, the transfer characteristic of the sustaining amplifier can be extracted. For the TIA offering 180° phase shift, the electronics only correspond the shunt-shunt feedback stage, and by lowering V_{CTRL} the gain is increased configuring the transfer characteristic closer to that of an inverter. In

this situation, it can be determined that the amplitude at the output can reach the rails producing nearly a $5V_{p\text{-}p}$ square waveform. On the other hand, if a TIA with 0° phase shift is used, the CS stage exhibits a different transfer characteristic due to its fixed load. The passive resistor employed has to be selected such that the symmetry of the transfer characteristic is maintained but at the same time to lower the output voltage at transistor M4 as well as the power consumption. Simulation of both transfer characteristics is presented in Figure 82.

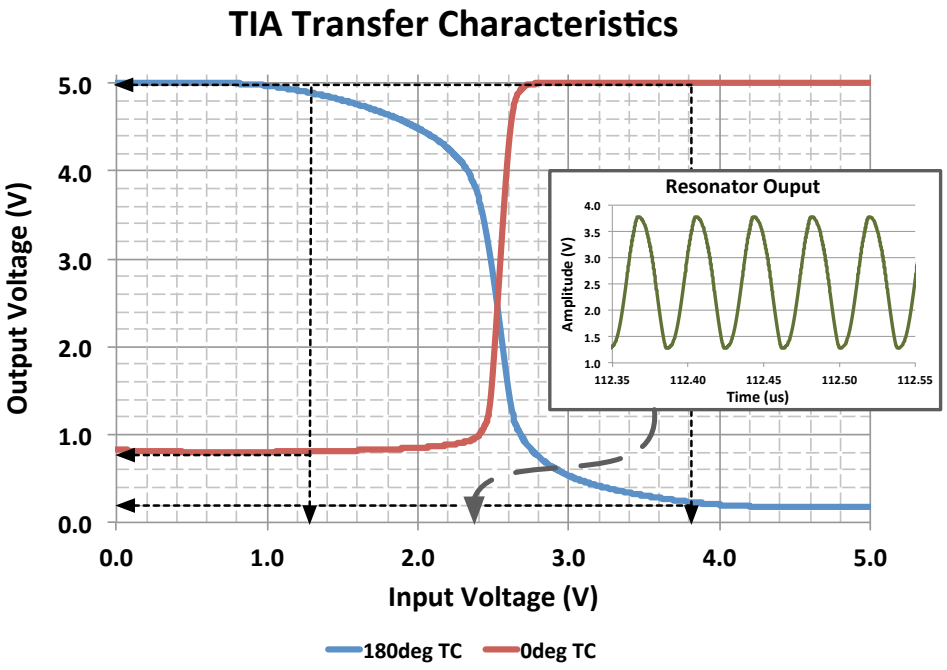


Figure 82. Transfer characteristic to estimate the power delivered to the resonator.

Thus, as a conservative estimate, selecting about $4V_{p\text{-}p}$ at the resonator input for both TIA versions and given the 50Ω termination of the measuring equipment, the

equivalent power at the VNA source is approximately 13dBm for the worst-case motional resistance considered. This drive level is above the onset of nonlinearity for the test resonator, and ADS predicts N equal to five for this estimated power level.

Figure 83 presents a schematic of the IC interfaced with a piezoelectric resonator through minimum-length aluminum bondwires. The oscillator started up properly with low transimpedance gain. As V_{CTRL} is reduced, the gain increases and the waveform reaches the saturation levels. Further decrease of V_{CTRL} only affects the TIA phase-shift to optimize the operating phase-frequency slope. Thus, the PN performance is measured for different settings of V_{CTRL} with an Agilent E5500 PN test set. The measurement summary includes a -30dB/dec slope line, which describes the flicker-noise processes using Leeson's formula at the limit of linear operation (Figure 84). The column labeled as V_{CTRL} in Figure 84 corresponds to the voltage applied to the gate of the feedback MOS resistor. It can be observed that under nonlinear regime, tuning and improved PN performance is possible. For the present demonstration, with a Q_L of about 4K, the maximum tuning obtained from this technique is about 200 ppm. Notice that the level of induced nonlinearity in the resonator can affect the expected tuning. For example, when the device is driven into the critical phase (when the operating phase-frequency slope becomes vertical), the oscillator will experience no change in frequency when the phase is varied. Therefore, an improved PN performance with tuning will require an appropriate selection of the operating point, which is estimated to be between linear operation and the critical drive.

The best Leeson's fitting estimates a noise figure NF (F_{dB}) of 45dB and β close to 50kHz. It is important to notice that the elevated NF stems from the noise folding due to

the TIA behavior as hard limiter causing noise components to be folded within the bandwidth of the resonator [44, 88]. Figure 85 shows simulated PN taking into account only the high gain of the TIA that makes the waveform to clip, while a linear RLC series tank is used as resonator model. Since Z_{tank} is 2,300Ω, and $F >> Z_{tank}$, it is concluded that the white-noise contribution of the oscillator PN is dominated by the electronics.

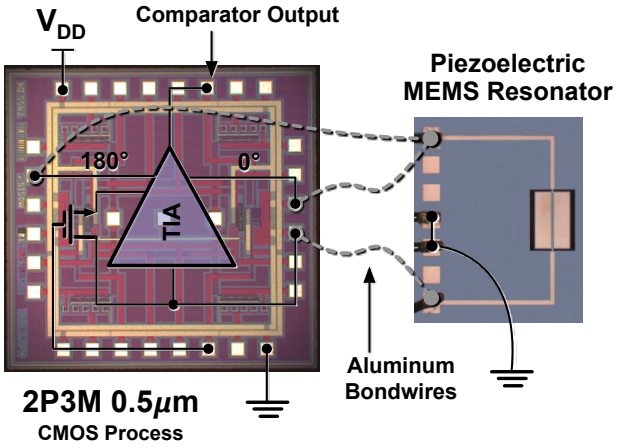


Figure 83. IC-resonator configuration via bondwires.

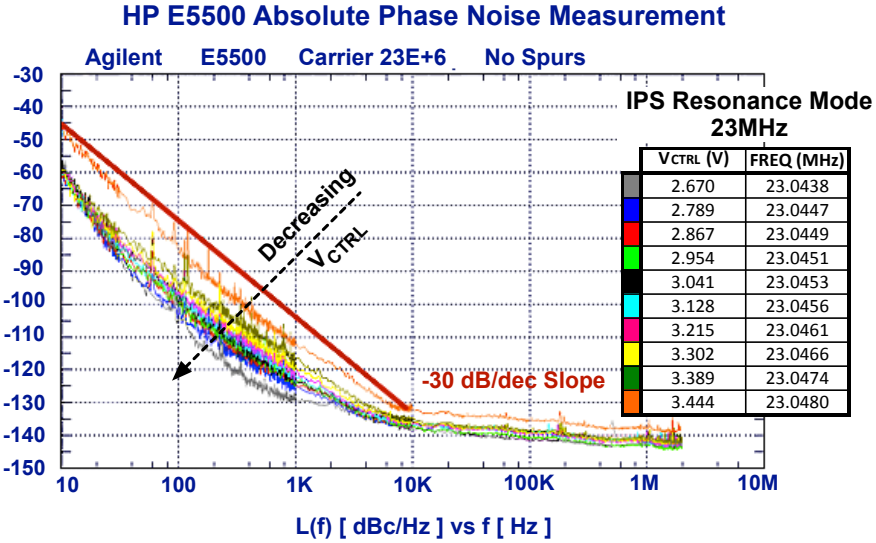


Figure 84. Tuning for a 23 MHz piezo-based oscillator using the phase-shift technique.

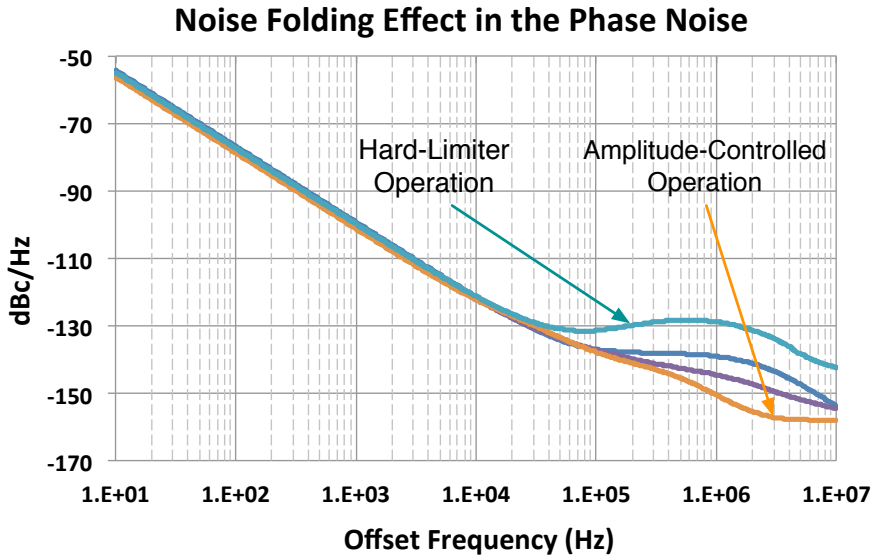


Figure 85. Noise folding effect due to the hard-limiting mechanism.

Once the parameters have been determined, Equation 46 is used to describe the PN performance for the nonlinear oscillator. The standard definition for PN uses the single-sideband expression of the output spectral power density [89] expressed in decibels per Hertz referred to the carrier power. The calculated factor N corresponds to the best-measured performance under this operating regime. As Equation 46 uses $S_{flicker+white\_NL}(\omega)$ to include white and flicker noises for amplifier and resonator, the flicker noise term will be presented explicitly to show the reduction in the parameter β, and a factor labeled as $S_{white}(\omega)$ will be used to represent the white noise of the complete oscillator. It is interesting to note that the best fitting for Equation 46 is given for an effective β equal to β /N, the same factor that increases the Q. Thus, the model for the 23MHz oscillator takes the form:

$$\mathcal{L}(\omega) \approx \frac{1}{2} S_{white} \cdot \left(1 + \frac{\beta/5}{\omega}\right) \cdot \left[1 + \sum_{k=2}^{6} \frac{1}{k!} \left[\frac{\sqrt{2}}{k-1} \cdot \frac{2\pi \cdot 23\times10^{6}}{5 \cdot 2 \cdot 4316}\right]^{k} \cdot \frac{1}{\omega^{k}}\right].$$

Figure 86 shows the model description of the measured results. The linear operation described by Equation 45 has been included for comparison. It can be observed that the induced nonlinearity in the MEMS resonator produces a maximum performance improvement of 20dB at an offset frequency of about 200Hz. Note that the nonlinear 23MHz oscillator, with an absolute figure of -130dBc/Hz at 1kHz offset frequency, is comparable to architectures with high-Q capacitive resonators [20] or state-of-the-art piezoelectric devices at higher frequencies [62].

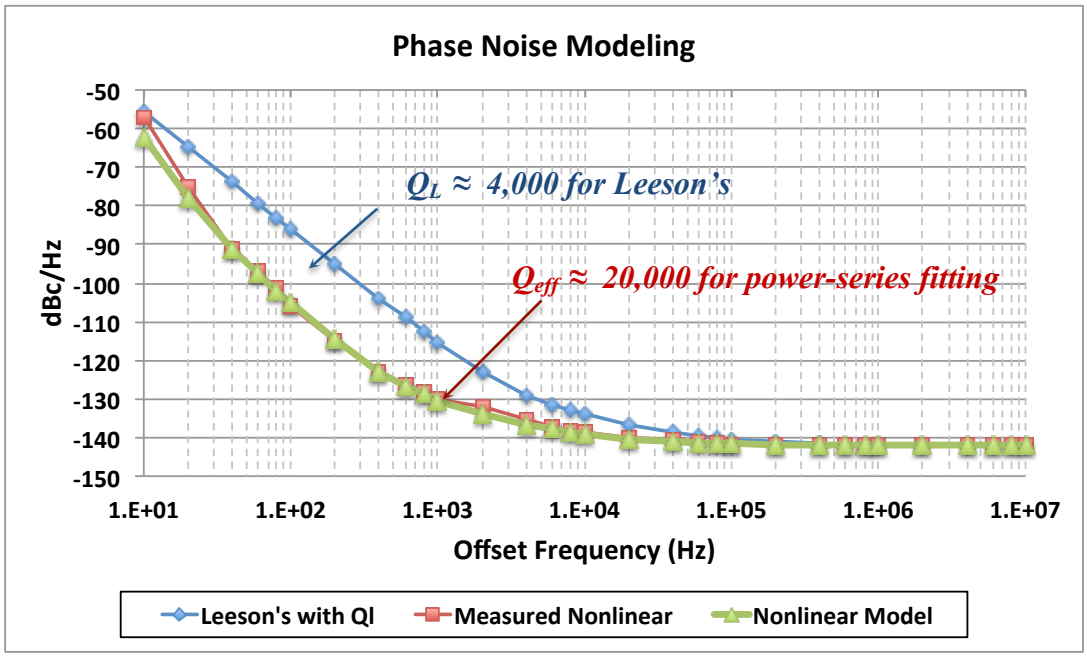


Figure 86. PN model fitting for the 23MHz IPS piezoelectric resonator

It can be observed that the presented model, restricted to linear operation, sets two limiting cases bounding the true PN of a nonlinear oscillator. In the first case, the close-to-carrier PN approaches a linear oscillator with Q equal to Q_L. In the second case, the far-from-carrier performance is better described by a linear oscillator with Q equal to Q_{eff} and reduced corner frequency. Thus, the nonlinear oscillator outperforms the linear oscillator with Q_L in terms of the integrated PN.

Finally, it can be noticed from Figure 84 that the circuit does not provide output for some sections of the full span of 0-5 V. To work as a VCO (especially during the PLL capture process), it is essential that the LO always produces an output regardless the condition of the tuning voltage. From Figure 84, if the controlling voltage is considered to be from 2.65 V to 3.45 V (ΔV=0.8 V), the full span for the ideal tuning voltage must be divided by 6.25 and moved upwards 2.65 V. The complete implementation for the MEMS VCO using the phase-shift in nonlinear regime is shown in Figure 87.

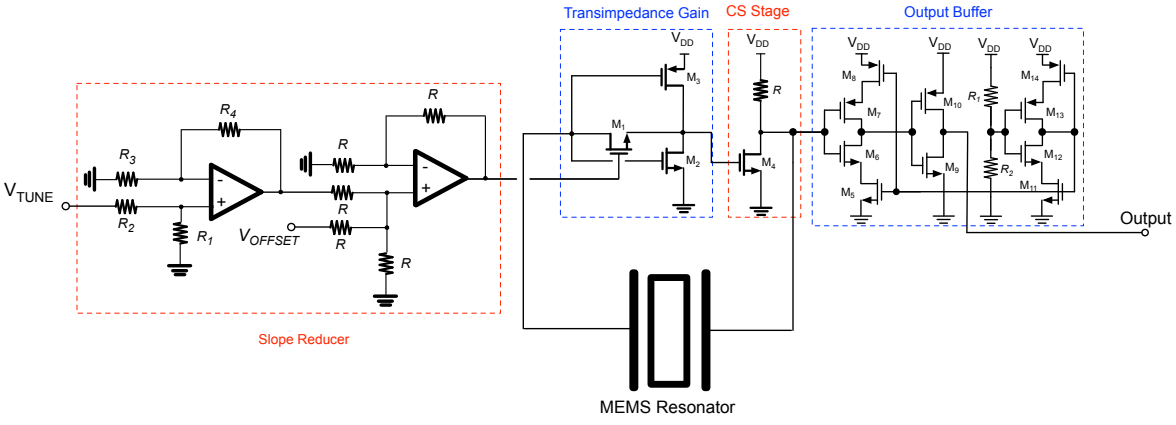


Figure 87. Phase-shift/Nonlinearity MEMS VCO architecture.

CHAPTER 6

BRN-PLL SET-UP AND TESTING

6.1. Cascade-type PLL vs. BRN-PLL for Clock Cleaner Applications

As a proof-of-concept, the BRN-PLL operation is demonstrated with an 82MHz clock cleaner configured through the design procedure outlined in Chapter 3 (Figure 88). The selected CP architecture is the one presented in Figure 39b, and the PFD employs the configuration of Figure 11 to take advantage of the linearization technique of [30]. For both LOs, the DS LC-VCO characterized in Section 4.2 is utilized. Dividers at either input or feedback path are not included in this demonstration to eliminate their contribution to PN.

A cascade-type PLL cleaner is also configured using the same building blocks (PFDs, CPs, and VCOs) following the procedure described in [47]. For this initial demonstration, both architectures use second-order passive loop filters optimized to produce the best performance for each case allowing a valid comparison between the two cleaning schemes. Preliminary designs for both configurations were refined with phase-model simulations in Cadence. Design constants and optimum loop-bandwidth values are reported in Table 4, producing the associated filter component values listed in Table 5.

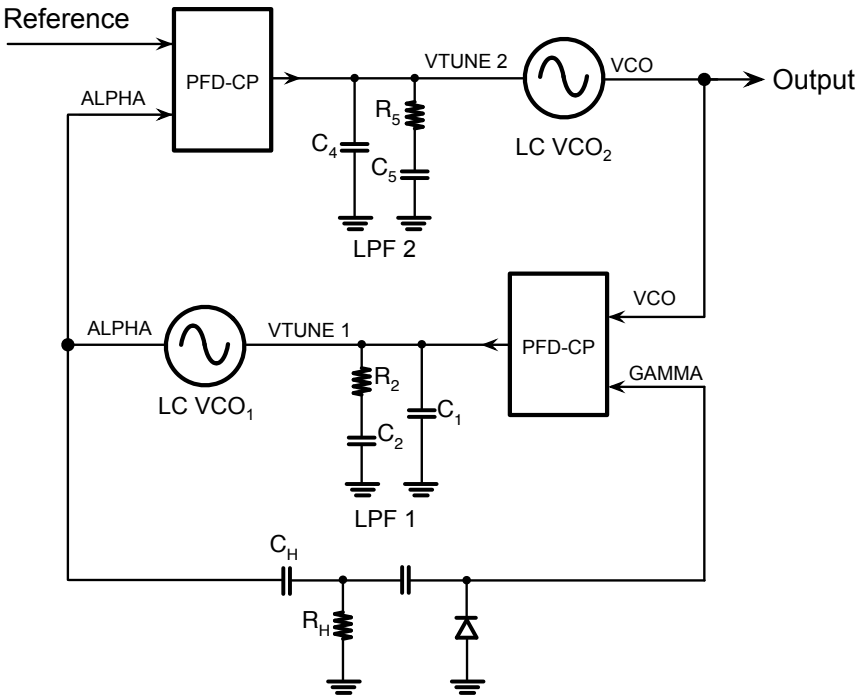


Figure 88. BRN-PLL architecture with second-order loop filters and DS LC-VCOs

Table 4. Design parameters for the clock cleaner architectures

	Cascade-type	BRN-PLL
I_{cp}	1.5 mA	
f_{VCO1}/f_{VCO2}	82 MHz	
K_{VCO1}/ K_{VCO2}	278.3 kHz/V	
Divider (N)	1	
BW Loop 1 (Inner)	1kHz	5 MHz
BW Loop 2 (Outer)	100 kHz	160 kHz

Table 5. Loop filter passives for the clock cleaner architectures

	Cascade-type	BRN-PLL
C_1 (Inner)	380 nF	1 pF
C_2 (Inner)	2.5 µF	15 pF
R_2 (Inner)	5.6 Ω	170 kΩ
C_3 (Outer)	457 pF	86.5 nF
C_4 (Outer)	2.3 nF	10 nF
R_4 (Outer)	1.8 kΩ	1.8 kΩ
R_H	N/A	100 Ω
C_H	N/A	100 pF

Table 4 reports that, after optimization, the bandwidth for both architectures is around 100kHz (since there is not a high-*Q* VCO). Following the guidelines of Section 3.2, Bode plots for both architectures are generated to quantify the effect of each building block on the output PN.

Figure 89a shows clearly that the BRN-PLL offers attenuation for the reference noise, and exhibits a +20dB/dec slope up to the selected bandwidth of the BRN-PLL. On the contrary, for the cascade-type PLL, it can be observed that the reference noise will pass unaffected through the first loop. The behavior of the PFD-CPs for the first loop and the inner-PLL is comparable, and the transfer functions have the same gain close-to-carrier. A similar conclusion can be derived for the VCO_2 transfer-function of both architectures. Figure 89b shows an additional advantage of the one-loop bandwidth of the BRN-PLL to provide extra filtering to VCO_1 and the PFD-CP_2 (outer PLL). Notice that the behavior is in agreement with the expected transfer functions displayed in Figure 37.

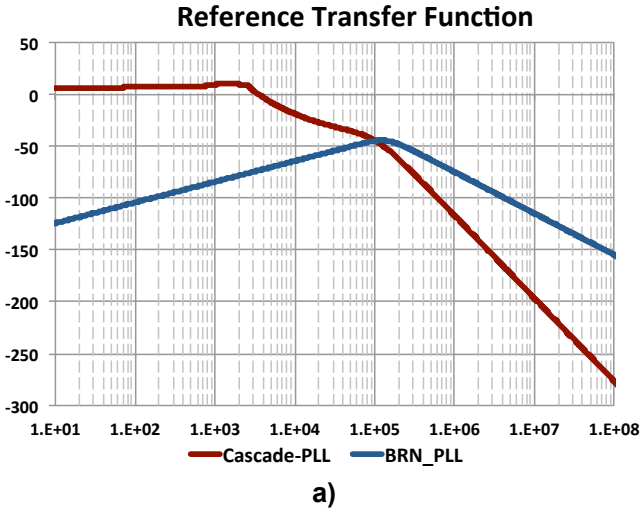


Figure 89. Comparison of the filtering for the Cascade-type PLL and BRN-PLL BRN-PLL. a) Reference noise transfer function and b) filtering for the remaining building blocks

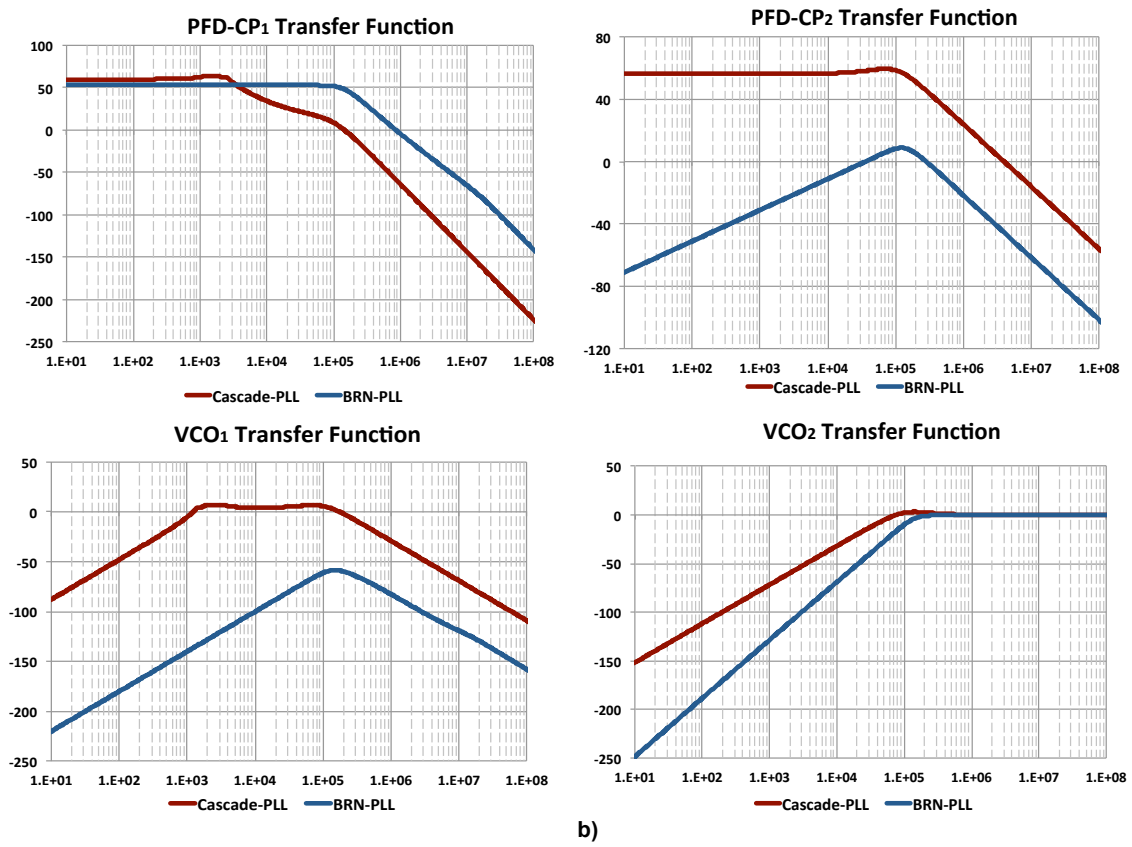


Figure 89 (Continued)

Figure 90 presents a micrograph of the test chip. The PLL building blocks were fabricated in a 1P6M 0.18 μm process provided by TSMC. The total power consumption for the ICs is 15 mW from a 1.8 V supply. Compared to single-PLL architectures, both cascade-type and BRN-based will consume significantly more power because they use twice the number of components. In particular, for the two-loops architectures, when the LOs are the same, it is possible to say that the power consumption is as high as twice the one of single-PLL schemes. However, compared to the cascade-type PLL, the power

consumption of the BRN-PLL is exactly the same because the two architectures employ the same building blocks in their configurations (the DC restorer in the BRN-PLL has been selected as a passive component. The test setup for measurements includes an evaluation board used to configure both cleaners (Figure 91), the Agilent E4438C Vector Signal Generator as a reference, and the Agilent E5500 PN analyzer system (Figure 92). The testing results are presented in Figure 93 and, although component tolerances and board parasitics shift f_T down, the measured output PN follows the trend predicted by phase-model simulations. For the cascade-type PLL, the transition region is observed as the flat response in the mid-section of the measured results.

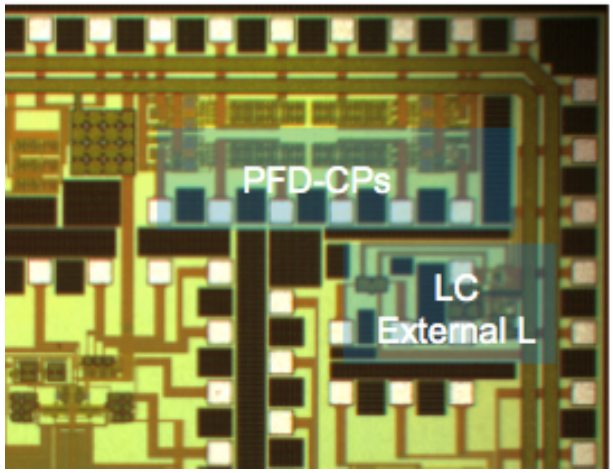


Figure 90. Micrograph of the PLL Building Blocks (Detail).

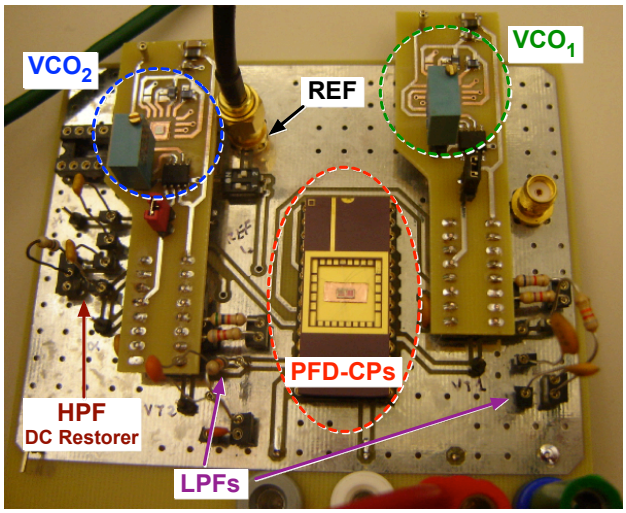


Figure 91. Evaluation board for the BRN-PLL using two LC-VCOs.

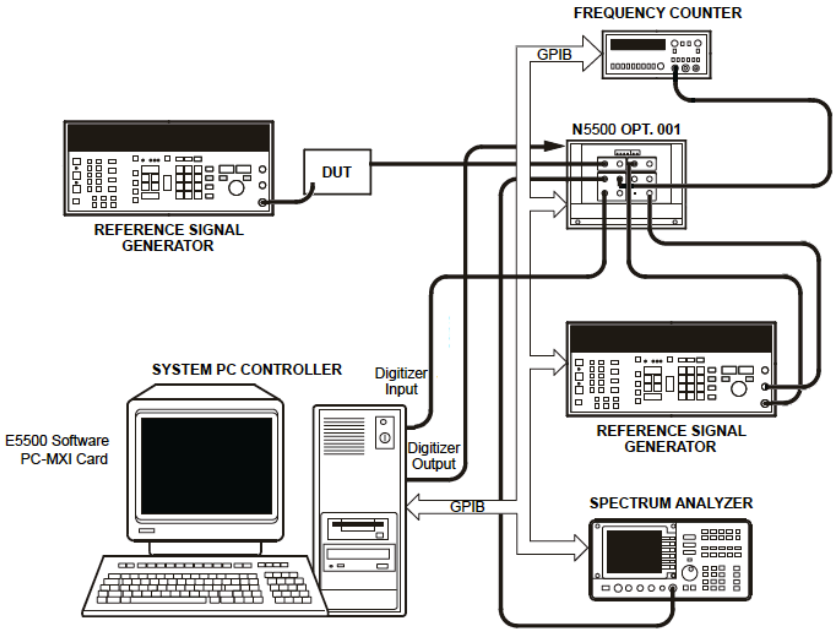


Figure 92. Configuration for PN testing (Agilent E5500N).

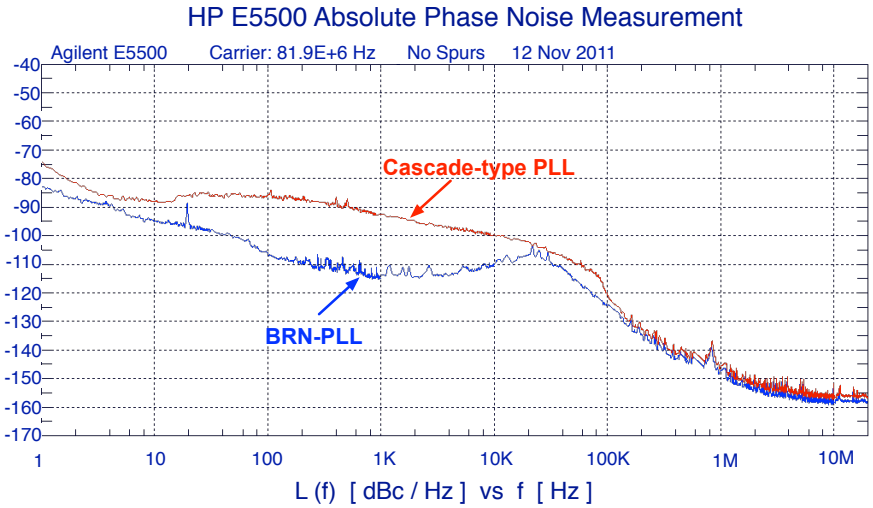


Figure 93. Measured performance of two clock cleaners based on BRN-PLL and Cascade-type PLL.

Figure 93 shows that the cascade-type PLL output PN can be divided in three regions. The first part is determined by the passband of the first PLL and dominated by the noise of the reference and the PFD-CP of the first loop (up to 50 Hz). Given the performance of the Agilent E4438C Vector Signal Generator, the PFD-CP noise becomes the dominant contributor to the PN. The second region can be defined between the first-loop cut-off frequency and the passband of the second loop (~50 Hz - ~20 kHz), and the PN is dominated by the contributions of both PFD-CPs and VCO_1. Finally, the far-from-carrier section is attributed to the noise of the VCO_2. On the other hand, only two regions are observed in the BRN-PLL PN response. The noise contributions due to the reference, VCO_1, and the outer-PLL PFD-CP are attenuated due to the generated notch making the inner-PLL PFD-CP dominant and main noise source for the close-to-carrier PN. Thus, it can be estimated an improvement of about 20dB at 1 kHz offset frequency indicating a superior performance for the BRN-PLL scheme.

The selection of the root locations for the BRN-PLL has been based on the stability guidelines discussed in Section 3.2. It is important to remember that the configuration of the root locus for the inner-PLL indicates a stable system for any value of *k* once the loop is closed. The location of the inner-PLL zero is around 62.5kHz, while the zero and the pole of the outer-PLL loop filter are at about 10kHz, which offers sufficient phase margin for the operation of the system.

The advantage of one BRN-PLL cut-off frequency is observed in the capacitor values listed in Table 5. Smaller loop-filter capacitors are achieved with similar values for the loop bandwidth when compared to the cascade-type PLL. Even though some values are in the tens of nanofarads (for stability), if the capacitors were to be integrated and the area per capacitor is calculated, the total footprint required for the BRN-PLL architecture is only 3.5% of the one required for the cascade-type PLL. It is important to notice that the BRN-PLL capacitor-area calculation includes the components used for the DC-level restorer.

6.2. MEMS-based BRN-PLL

MEMS-based BRN-PLL refers to the scheme including a tunable MEMS oscillator as VCO_1. Given the superior performance of this LO, the mid-area of the PN is expected to be lowered and it would allow the selection of a wider loop to further eliminate any peaking that can result due to the transition to the VCO_2 PN (for lower noise floor).

Selecting a wider loop imposes the use of a cleaner PFD-CP; therefore, the architecture presented in Figure 40 will be used. For the VCO_1, the IC fabrication process determines the selection of the method to be used for tuning. Since a 0.18μm 1P6M

CMOS process restricts the power supply of the complete system to 1.8V, the maximum power delivered to the resonator is estimated as 6dBm, which is at the edge of the onset of nonlinearity for the MEMS resonator considered in this work. Given this power estimation, it can be concluded that the drive level is not sufficient to exploit beneficial nonlinearity, and due to the fact that the selected process offers on-chip varactors, the series-tuning technique is more adequate for VCO_1. The operating frequency will be around 26MHz, which is determined by the MEMS device. Thus, the LC VCO is configured to operate at about 104MHz, which gives the best trade-off between divider (÷4) and inductor values.

Compared to the scheme of Figure 88, third-order loop filters will be used to carry out a complete design with the higher-order-loop guidelines of Section 3.3. Figure 94 presents the block diagram for the MEMS-based BRN-PLL.

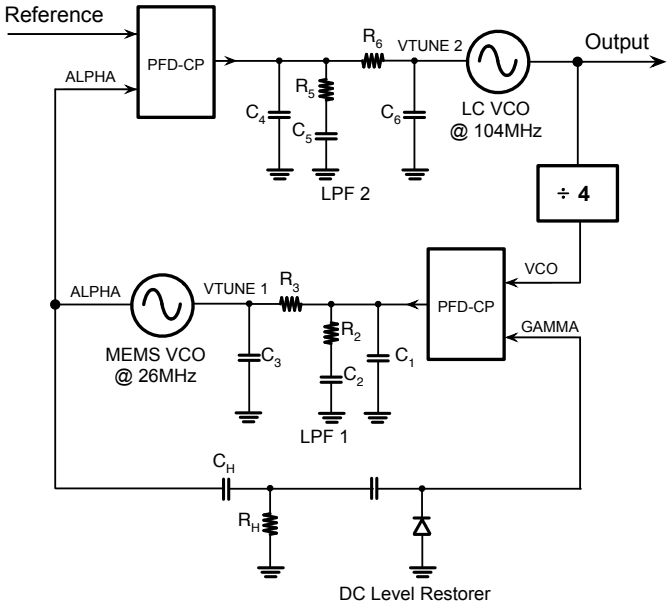


Figure 94. BRN-PLL Architecture with third-order loop filters, MEMS VCO and LC-VCO

The required design parameters to proceed with the configuration of the BRN-PLL need to be determined. From Figure 44, the CP current is estimated to be 540μA. Similarly, the gain of the MEMS-VCO can be extracted from the characterization of Figure 72. K_1 is calculated as 11.183kHz/1.8V ≈ 6.2kHz/V.

Finally, since the customization of the LC VCO was dependent on the selected tuning method for the MEMS VCO, characterization of the 104MHz DS LC-VCO is shown in Figures 95, 96, and 97. K_2 is approximated to be 949.5kHz/1.8V ≈ 527.5kHz/V.

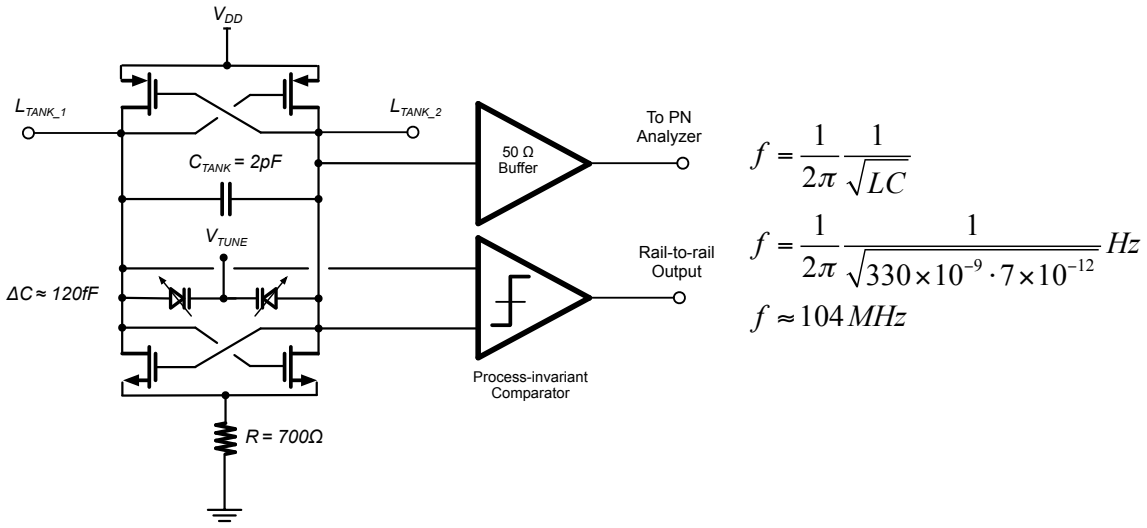


Figure 95. Block Diagram of the LC-VCO

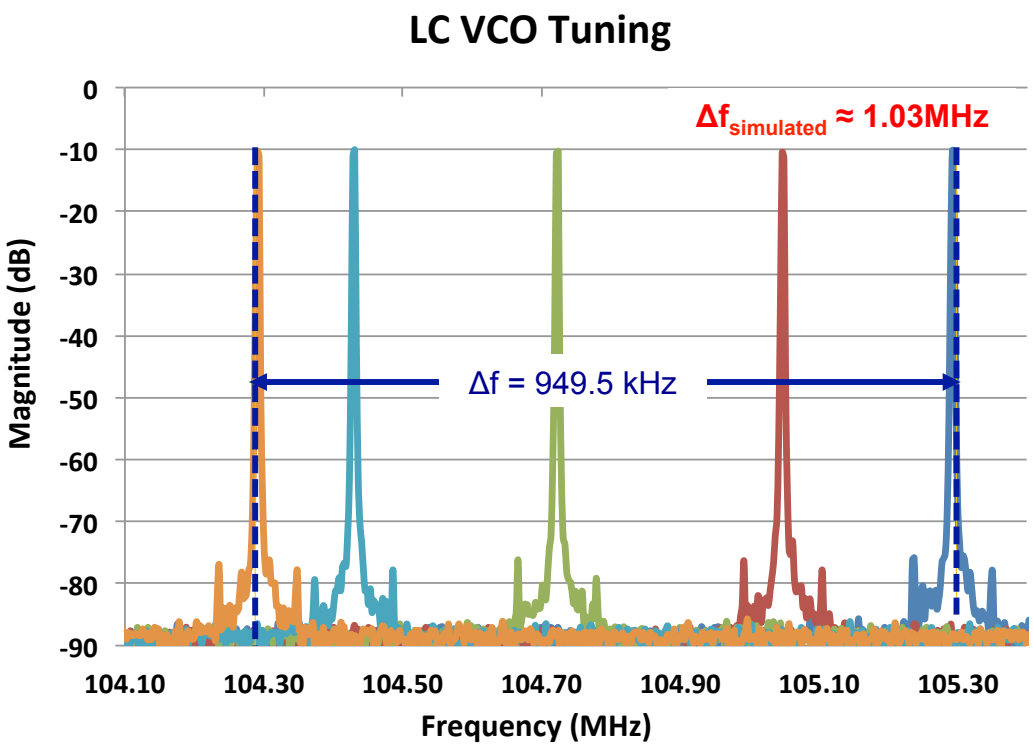


Figure 96. Measured LC-VCO Tuning

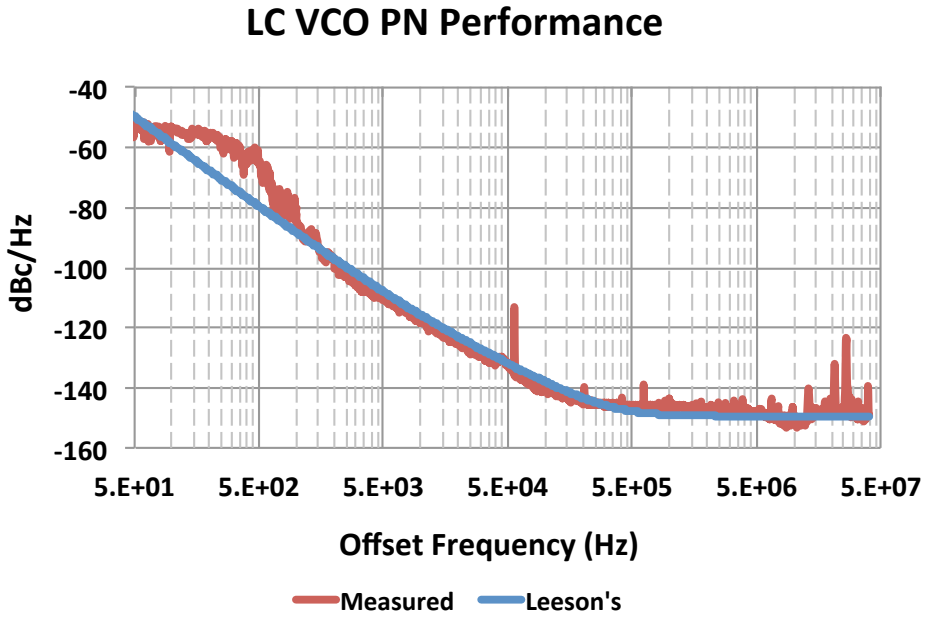


Figure 97. Measured LC-VCO PN Performance

Using the guidelines of Chapter 3, the inner-PLL is designed first. Using the Nyquist stability criterion, the first step is to determine the value for the capacitor C_1 when the gain equals 0dB. This operation reveals that the calculation of C_1 is directly proportional to K_1. Thus, although a wideband loop is desired for the inner PLL, due to the associated small value for K_1, the obtained values are extremely small to realize with practical components. In addition, in terms of stability of the closed-loop equivalent, a small value for the capacitor will produce a higher value for k, which can make to complex-conjugate poles to cross to the right-hand side of the complex plane. Therefore, a possible solution consists in increasing the gain for VCO_1; however; this operation could lead to a pronounced variation in the frequency within the loop. A trade-off between the component values and bandwidth is required for this case, while maintaining the relative locations of the roots as commented in Section 3.3. For the given design parameters, the value of the passives for the filters of the inner PLL are summarized in Table 6.

Simulation of the stability for the inner PLL was carried out using the pole-zero models described in Section 2.2. Figure 98 shows that the phase margin is close to 90° that can be viewed as a system with sluggish behavior; however, this is a consequence of the location of poles-zeros and to obtain a small value for k that keeps the complex-conjugate poles in the left-hand side of the plane for the inner-PLL closed-loop equivalent.

Table 6. Design Parameters for Inner-PLL (MEMS-VCO)

Parameter	Value
Operating Frequency	26 MHz
Charge-pump Current	540 µA
VCO Gain (K_1)	6.2128 kHz/V
Divider Value	1
3dB Bandwidth	90 kHz
f_1 (ω_1)	650 kHz
f_2 (ω_2)	65 kHz
f_3 (ω_3)	3.26 MHz
f_H (ω_H)	130 kHz
C_1	1 pF
C_2	9.5 pF
R_2	235 kΩ
R_3	8.8 kΩ
C_3	5 pF
R_H	10 kΩ
C_H	10 pF

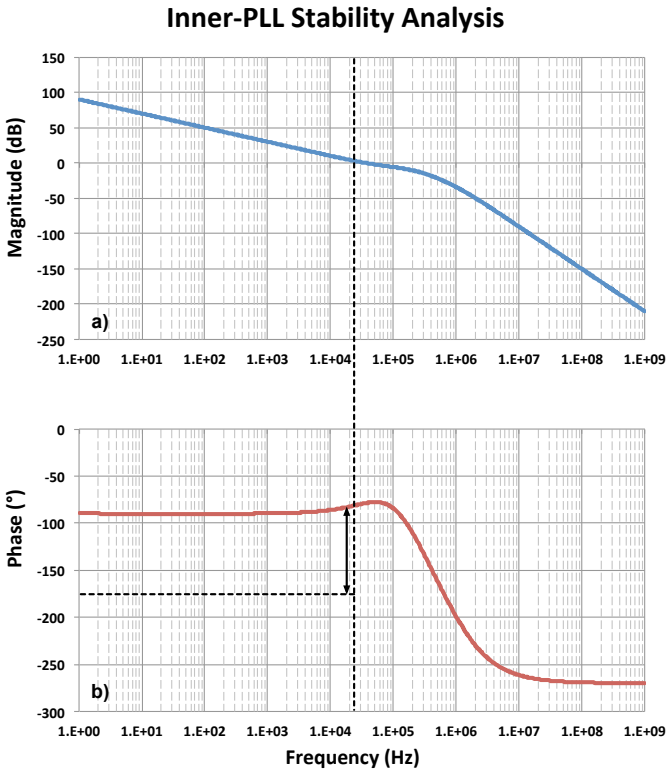


Figure 98. Stability Analysis for the Inner-PLL: a) Magnitude and b) Phase.

Figure 98 shows that the inner PLL will be stable once is closed, and it can be inserted in the outer PLL. Since the inner PLL works at 26MHz, a divide-by-4 block is required to interface the signal from the LC VCO. The selection of a power-of-2 divider eases its implementation. Figure 99 shows the architecture for this divider using D flip-flops.

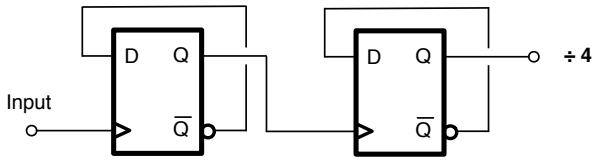


Figure 99. Divide-by-4 block diagram

The PN profiles of the MEMS and the LC VCOs can be used to determine a suitable BRN-PLL bandwidth. Figure 100 indicates that a cut-off frequency in the offset-frequency range from 3 kHz to 40 kHz can provide a smooth transition for the output-signal PN. Notice that proper location of the outer-PLL roots with respect to the already set inner-PLL poles and zeros will control any peaking observed in the PN response. Since the relation between peaking in the noise behavior and capture time is inversely proportional, the latter can be long when the PN performance is designed to avoid hard transitions between the different noise sources. From Chapter 3 and the required design parameters, the values of the passives for the outer-PLL filter are summarized in Table 7.

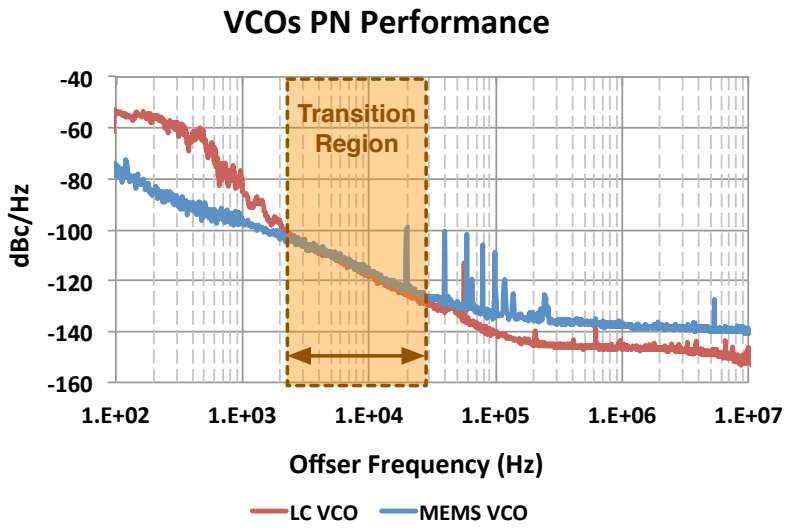


Figure 100. Optimum offset-frequency range for the BRN-PLL.

Table 7. Design Parameters for Outer-PLL (LC-VCO)

Parameter	Value
Operating Frequency	104 MHz
Charge-pump Current	540 µA
VCO Gain (K_2)	527.5 kHz/V
Divider Value	4
3dB Bandwidth	35 kHz
f_4 (ω_4)	65 kHz
f_5 (ω_5)	1.1 kHz
f_6 (ω_6)	4.33 kHz
C_4	4.5 nF
C_5	0.25 µF
R_5	500 Ω
R_6	2.5 kΩ
C_6	14 nF

Simulation of the stability for the outer PLL was carried out using the models for pole-zero analysis of Section 2.2 (Figure 101). It can be observed that there is no peaking in the response and a 90° of phase shift for low-offset frequencies, which is an indication

that the value for *k* is not enough to generate the conjugate-complex poles and to make the pole at the origin to deviate significantly from the origin, respectively. In particular, the resultant pole at the origin from the inner-PLL plus the two poles added by the outer-PLL will configure the BRN-PLL as a type-III system (-270° = 90°), which will produce a zero steady-state error for step, ramp and parabolic phase functions. Figure 102 shows the behavior of the tuning voltages for both VCOs for the capture process. It can be observed that for this 100MHz clock cleaner, the settling time is estimated about 750µs.

Figure 103 presents a micrograph of the IC fabricated in a 0.18µm 1P6M process provided by TSMC. The test setup includes an evaluation board allowing the connection of the different loop filters (Figure 104). The source used for testing is an Agilent E4438C Vector Signal Generator, and the Agilent E5500 PN analyzer system is used to determine the PN performance for the MEMS-based BRN-PLL (Figure 92).

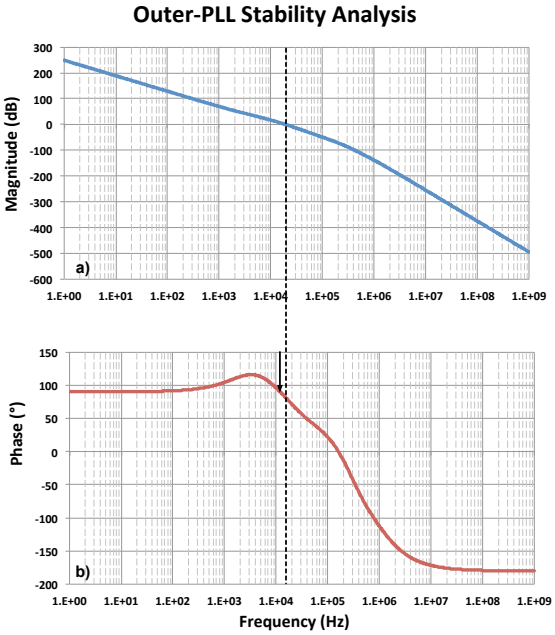


Figure 101. Stability Analysis for the Outer-PLL: a) Magnitude and b) Phase.

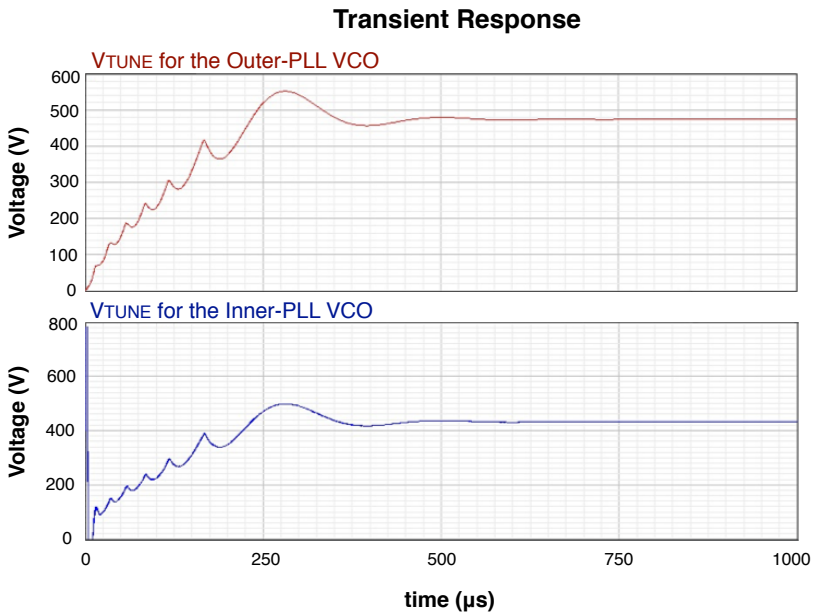


Figure 102. Capture Process for the BRN-PLL

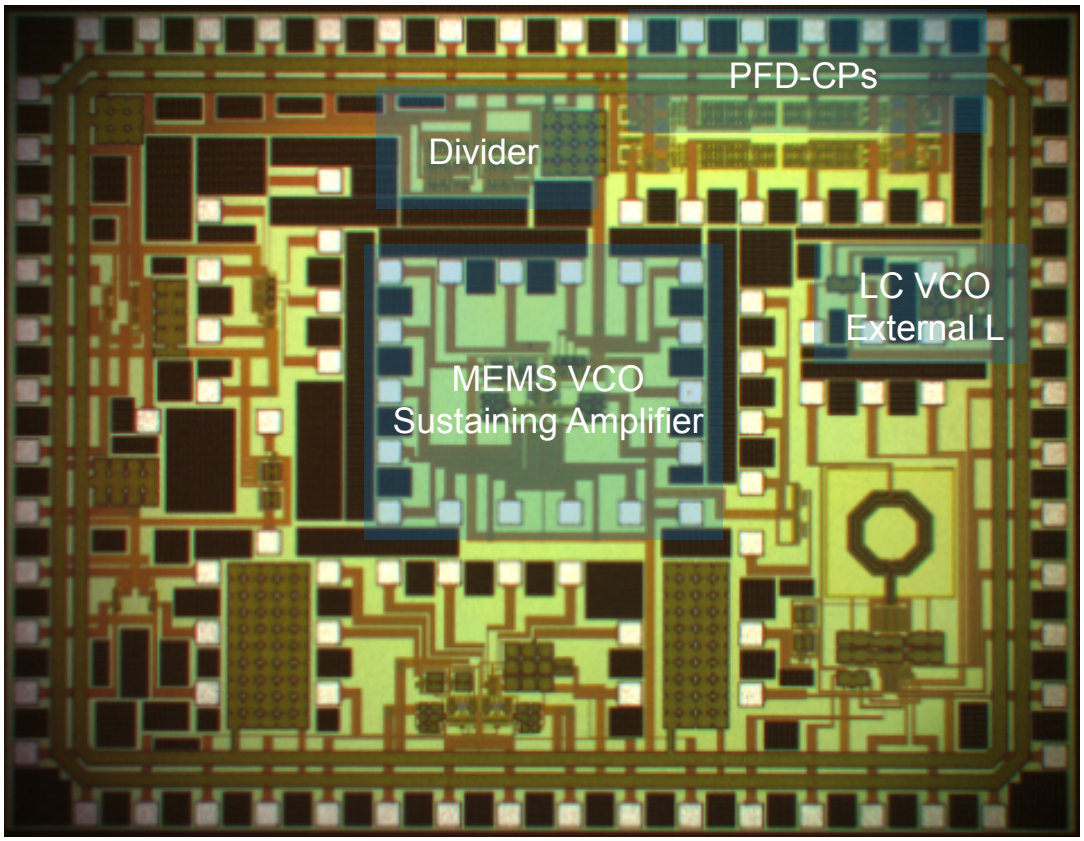


Figure 103. Micrograph of the PLL Building Blocks.

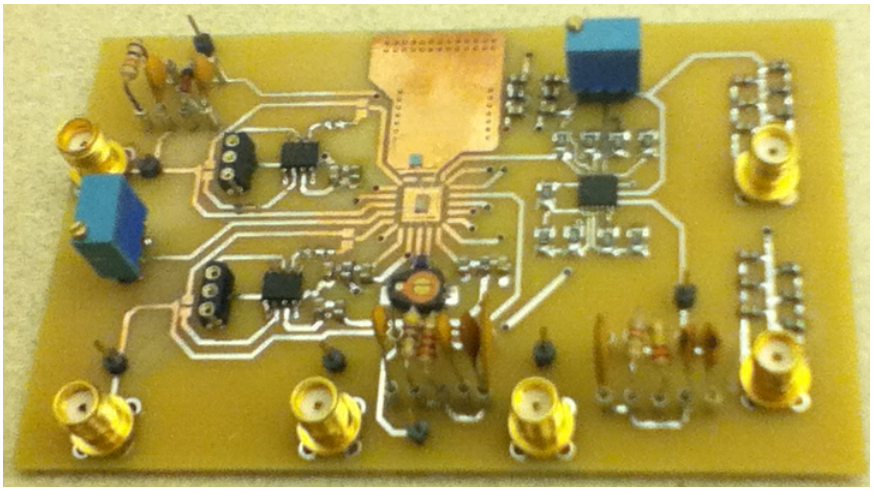


Figure 104. Evaluation board for the BRN-PLL.

Once the BRN-PLL is configured, the locked state is verified using a DSO6014A oscilloscope. Given its classification as type-III system, Figure 105 shows that the phase error for the reference and VCOs signals is zero as expected.

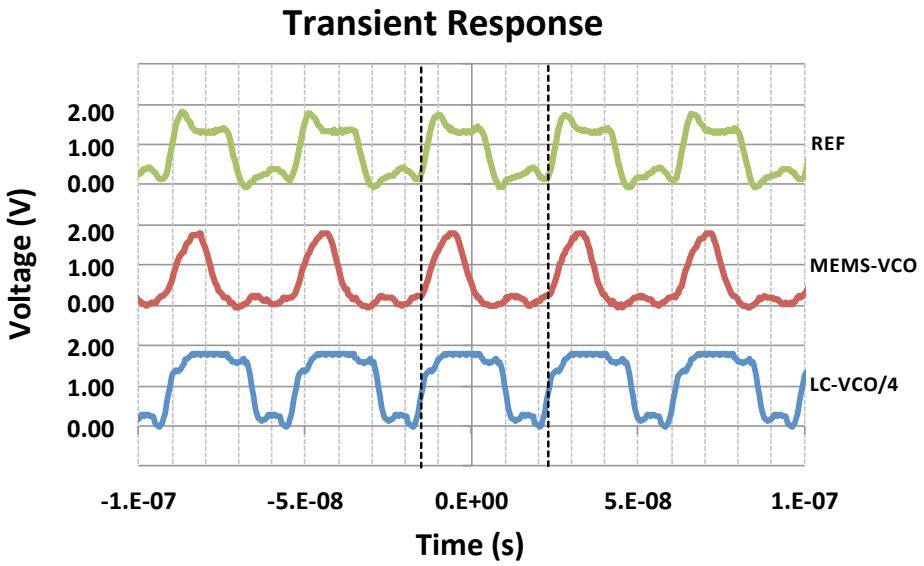


Figure 105. Transient response of the MEMS-based BRN-PLL

The different PN profiles for the building blocks that comprise the MEMS-based BRN-PLL are extracted, and phase models are generated to simulate the total PN of the proposed clock cleaner. The testing of the total BRN-PLL shows proper capture process and zero steady-state phase error. The measured PN performance is included along to the simulation results in Figure 106. A good agreement between prediction and measurement is observed, and the output PN profile has the expected slopes.

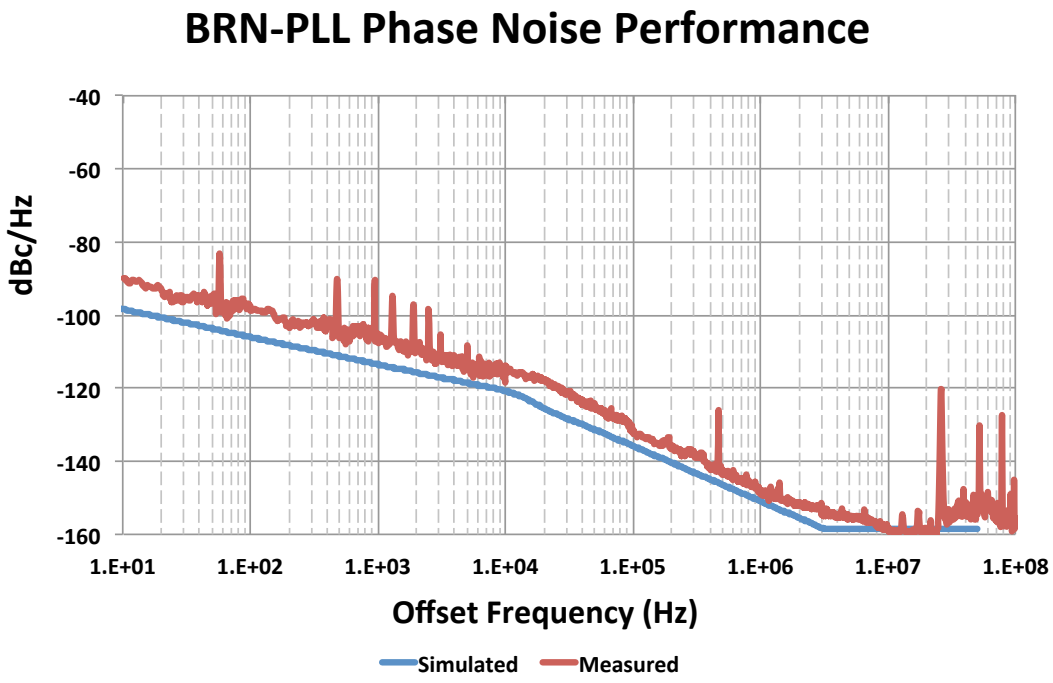


Figure 106. Measured performance the MEMS-based BRN-PLL

Compared to the performance reported in Figure 93, the careful selection of the location for the roots of the outer-PLL allow the reduction in the peaking in the PN

response. Figure 107 reveals that the performance of the two BRN-PLL examples is comparable, even when the MEMS-based scheme contains a divide-by-4 block that increases the noise by about 12 dB. Hence, it can be concluded that the response keeps being dominated by the inner-PLL PFD-CP, and the effect of the switching network in the CP proves to be beneficial for the whole system. No appreciable bumps are observed before the transition to the noise profile of VCO_2, which is an indication of effective filtering to VCO_1.

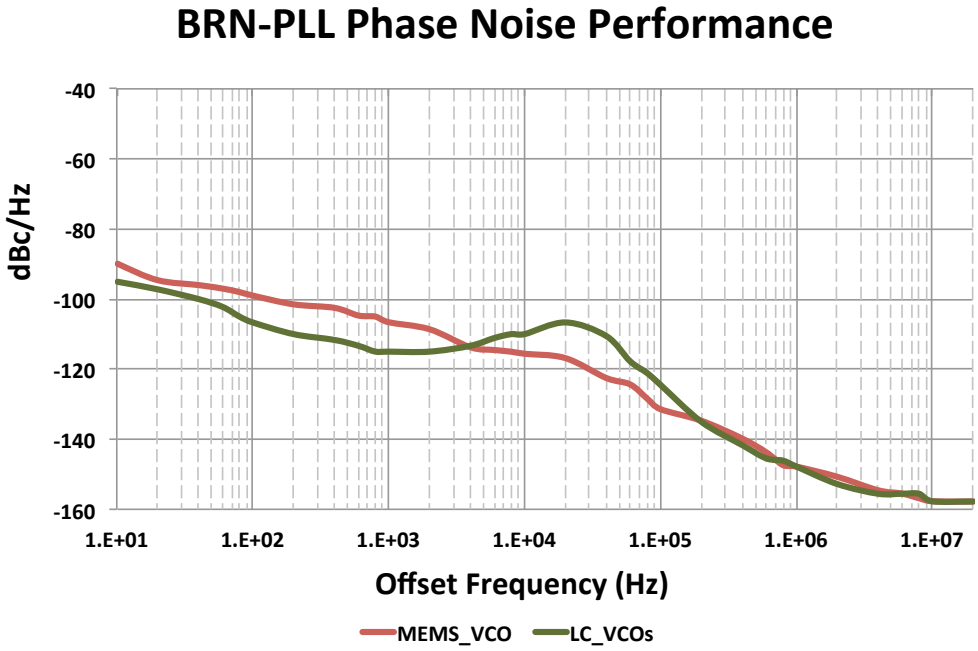


Figure 107. Comparison between the two tested versions of the BRN-PLL.

Table 8 compares the performance of the BRN-PLL with the alternatives offered by TI presented in Table 1. It can be observed that the use of a MEMS device ($Q \approx 4{,}000$)

as replacement for the crystal as reference is possible while maintaining optimum performance. In addition, it can be noticed the nature of the single-loop systems, the reference passes through the system dominating the PN profile of the oscillator very-close-to-carrier (≈ -20 to -30 dBc/dec). On the contrary, for the same region, the BRN-PLL exhibits the behavior of the PFD-CP, which minimizes the integrated PN of the system. However, removing the divider in the BRN-PLL is required to maintain a state-of-the-art performance. In addition, Table 8 includes a comparison with a DSP-based PLL used in SONET/SDH systems for switching receiver lines cards [90]. This work is interesting because, it keeps using a narrowband bandwidth that can be adjusted digitally. This PLL includes a LC-VCO with an estimated Q of 30, and it is intended specifically for clock cleaning applications. The BRN-PLL offers comparable performance with the analog filters, which is the reason why the DSP was included in [90] trying to avoid noise coupling.

Table 8. PN performance summary of single-loops systems and the BRN-PLL scheme

PN @	Reference	LVPECL-HP	LVDS-HP	LVCMOS-HP	BRN-PLL	BRN-PLL	DSP-based PLL	UNIT
	(25MHz)	500MHz	250MHz	125MHz	100MHz	@500MHz*	@600MHz*	
1.00E+01	-	-72	-72	-79	**-90**	**-76**	**-45**	dBc/Hz
1.00E+02	-	-97	-97	-103	**-98**	**-84**	**-54**	dBc/Hz
1.00E+03	-	-111	-111	-118	**-108**	**-94**	**-71**	dBc/Hz
1.00E+04	-	-120	-120	-126	**-114**	**-100**	**-100**	dBc/Hz
1.00E+05	-	-124	-124	-130	**-132**	**-118**	**-122**	dBc/Hz
1.00E+06	-	-136	-136	-142	**-149**	**-135**	**-143**	dBc/Hz
1.00E+07	-	-147	-147	-151	**-158**	**-144**	**-151**	dBc/Hz
2.00E+07	-	-148	-148	-151	**-160**	**-146**	**-152**	dBc/Hz

***PN upconverted from 100MHz to 500MHz**

With respect to two-loop systems, the idea is to locate the performance of the BRN-PLL in the performance summary of Figure 3. Thus, the RMS jitter needs to be calculated. The first step in calculating the equivalent RMS jitter is to obtain the integrated phase noise power over the frequency range of interest. Dividing the PN profile into areas, and integrating each individual area yields individual power ratios. The individual power ratios are then summed and converted back into dBc. Once the integrated phase noise power is known, the RMS phase jitter in radians is given by [91]

$$RMS\ Phase\ Jitter(radians) = \sqrt{2 \cdot 10^{Area/10}}\ , \tag{50}$$

and dividing by $2\pi f_0$ converts the jitter in radians to jitter in seconds [91]:

$$RMS\ Phase\ Jitter(seconds) = \frac{\sqrt{2 \cdot 10^{Area/10}}}{2\pi f_0}\ ; \tag{51}$$

thus, the approximated RMS jitter can be calculated as shown in Table 9, and in Figure 108. It can be observed how the performance of the BRN-PLL can be compared with two-loop systems and those that employ a crystal as reference.

Table 9. PN performance summary of two-loops systems (using a crystal) and the BRN-PLL scheme

PN @	**BRN-PLL 100MHz**	**Jitter (ps RMS)**
1.00E+01	**-90**	-
1.00E+02	**-98**	0.37011
1.00E+03	**-108**	0.41344
1.00E+04	**-114**	0.5297
1.00E+05	**-132**	0.44288
1.00E+06	**-149**	0.18383
1.00E+07	**-158**	0.12356
2.00E+07	**-160**	0.07611

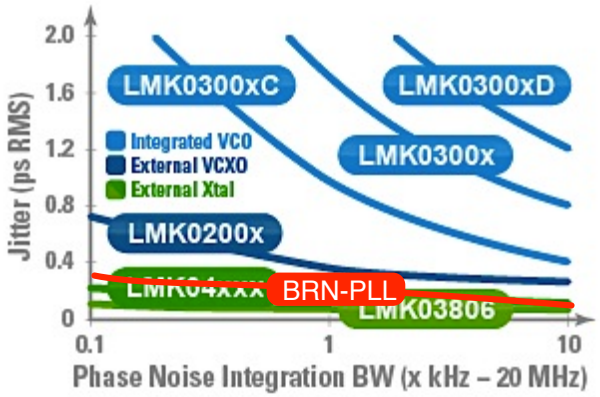


Figure 108. Location of the BRN-PLL with respect to state-of-the-art clock cleaners.

The hold-in range for the MEMS-based BRN-PLL is measured using an Agilent E4407B spectrum analyzer while the generator Agilent E4438C is slowly changed. Figure 109 summarizes the frequency range from this PLL. It can be observed that the hold-in range is limited by the MEMS VCO.

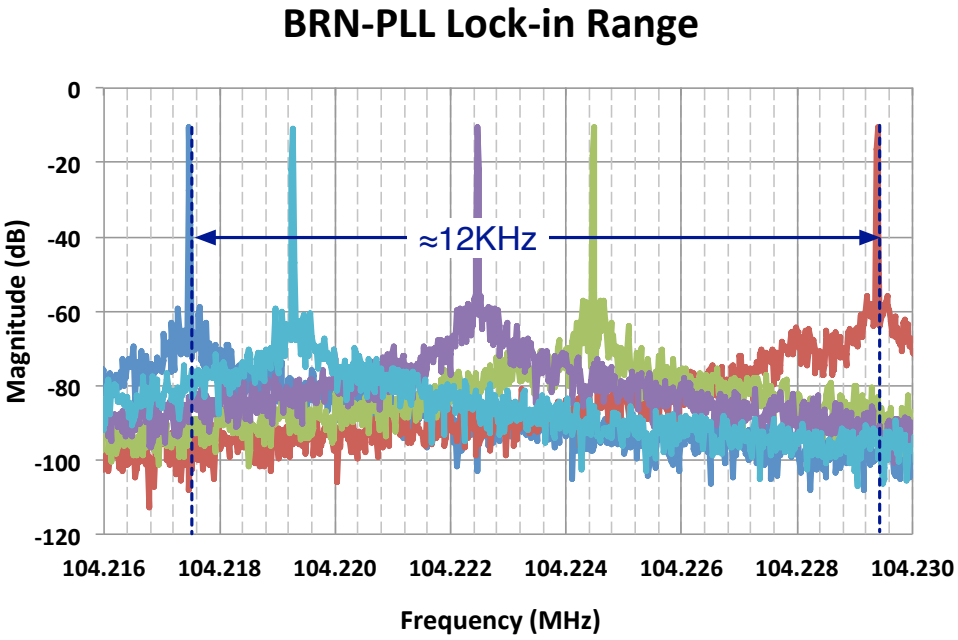


Figure 109. Measured hold-in for the MEMS-based BRN-PLL

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1. Contributions

In this dissertation, the design, characterization and implementation of a full-spectrum MEMS-based clock cleaner were investigated. The following is a list of contributions that have been achieved in this study:

1. Development of an architecture with a band-reject behavior in the reference transfer function that provides two advantages for clock cleaning at the same time. By using this composite architecture, the filtering to the input signal is improved and the requirements for the bandwidth of the PLL system are relaxed.
2. Utilization of a MEMS VCO in a BRN-PLL clock cleaner shapes effectively the transition region in the PN response and its contribution very close-to-carrier is further improved by the observed attenuation in the corresponding transfer function. In this way, a BRN-PLL scheme takes full advantage of a high-Q MEMS oscillator. This aspect becomes an improvement compared to cascade-type PLL clock cleaners, which only will work properly with ultra-narrow band filters.
3. A complete set of design and simulation tools under the same platform was presented. Based on the phase-model work by [5], Verilog-A was used to expand the high-level design of PLL-based systems. The use of multiple software is no longer required eliminating the need of portability of output reports, result files, etc. Using this set of tools reduces the computational requirements and simulation times for PLL design.

4. Attenuation of the reference signal makes the CP current noise to be the dominant factor in the very close-to-carrier PN performance for the BRN-PLL clock cleaner. A single-ended CP was maintained, and complementing the work by [30], a cascoded current mirror is used to improve the matching between pumping/sinking current. The addition of a switching network to isolate the CP during idle state proves to reduce the noise contribution by about 20dB. This fact translates directly in the possibility of trading off power consumption (less pumping current) with improved PN performance.
5. Development of a MEMS-VCO was explored using two different techniques to minimize PN degradation. For series tuning, the series varactor is implemented using two back-to-back varactors. The use of a reverse-biased diode in the tuning port effectively reduces the signal loss, which increases the Q of the series varactor with negligible effect in the change of capacitance.
6. Implementation of a MEMS VCO with improved PN performance by tuning the operating phase of a resonator working in nonlinear regime. An empirical model was presented to reveal that the Q of a nonlinear oscillator can be higher that the Q of the same oscillator working linearly. When the oscillator operates in nonlinear regime, the worst-case PN performance will correspond to the linear operation. From a LO point of view, since the tuning technique is based on the modification of the operating phase, the presence of shunt-parasitic capacitance does not affect the effectiveness of the technique.

7.2. Future Direction

Superior performance and a reduced footprint for the loop filters have been possible with the development of the BRN-PLL clock-cleaner architecture. Although the design of this scheme highly depends on the parameters defined by the PDs and LOs, the BRN-PLL architecture allows the possibility of full on-chip integration of filters. Since the microresonator is located outside the IC, its characterization (frequency, insertion losses, etc.) can exhibit variability and therefore, the estimation of the MEMS-VCO gain cannot be determined in advance. Therefore, tunability of the filters is required without compromising noise performance.

Current-based or digital filters become suitable options for changing the bandwidth of the BRN-PLL. Since the VCOs already have discrete tuning steps to minimize the gain of the continuous tuning elements to favor noise performance, digital filtering is expected to produce a cleaner tuning signal. Using these digital components, the BRN-PLL will become a system under a mixed-signal approach.

The addition of digital circuitry can also allow the configuration of a fractional BRN-PLL. Fractional-PLLs are needed when integer-PLLs cannot provide the required resolution for fine tuning. However, fractional division can only be conceived as an average operation with respect to time, and a sequence of integer dividers needs to be generated to obtain the desired result. The use of noise-shaping circuits, such as delta-sigma modulators (DSMs), can be used to produce such sequence, so that most of the noise content due to the change in dividers is pushed to higher frequencies. Therefore, the low-pass behavior to the PN can be used to filter the high frequency content [92]. Since first- and second-order DSMs cannot randomize enough constant inputs due to the finite

word-length of the digital modulator, stable third- and higher-order DSMs must be used to eliminate the spurious tones properly.

Stable higher-order DSMs can be obtained by cascading first-order stages configuring a multi-stage noise shaping (MASH) modulator. This dissertation provides the guidelines for the design of higher-order BRN-PLLs; however, it is still required to determine if third-order loop filter will work adequately with a MASH-based fractional BRN-PLL. In a negative case, design guidelines for fourth or higher order filters will be required.

A second aspect of this research is related to the tuning of the MEMS-based oscillator. Although most of the actual work on microresonators is focused on temperature compensation and improved linearity, this project opened the discussion about the nonlinear operation of MEMS resonators, and its application as tuning strategy. Thus, understanding how the PN is shaped in this regime deserves a dedicated line of research due to the potential of very high-Q oscillators from relatively low-Q resonators. The generation of a complete theoretical PN model encompassing nonlinearity is an expected product derived from this line of research. It is important to notice that the development of this initiative is highly dependent on the fabrication of MEMS devices that exhibit these effects at low onsets of nonlinearity. From the conclusions derived from this work, the generation of amplitude regulators that allow different settings for power delivered to the resonator will help to gain insight about the progressive improvement in the PN, but also in the reduction of the noise folding. In addition, if a dedicated phase shifter is included in the loop, more points of the phase-frequency transfer functions can be selected to observe the shaping of the PN under different operating conditions.

A third line of research derived from this project is related to the trade-off between the loop-filter component values and bandwidth of a MEMS-based PLL. As comment in Section 6.2, a low K_1 restricts how wide the inner-PLL bandwidth can be selected. Thus, for a MEMS oscillator, it is required to find alternatives to increase the capability of pulling the resonance frequency. Increasing the tuning range of a MEMS VCO can provide two beneficial effects for the BRN-PLL when used with caution. First, a larger value of the VCO gain leads to a wider loop bandwidth with filter-component values realizable on chip. Second, the MEMS VCO itself can compensate deviations on the resonance frequency due to fabrication variations without the need to rely on the fractional divider of the clock-cleaner to bring the output frequency to the expected value.

Even though the use of the phase-shifting technique for a nonlinear resonator can be effective with the presence of shunt-parasitic capacitance, this technique is dependent on the onset of nonlinearity for the resonator and the power that the TIA is able to deliver. Thus, for example, when the power supply for the MEMS oscillator was reduced to 1.8V, the delivered power was at the edge of the onset limiting the beneficial effects of this technique. In addition, the current tendency is the development of compensation techniques to achieve better power handling and linearity, such as the use of embedded silicon dioxide (SiO_2) pillars in the silicon body of the resonator [93]. Therefore, new options for fabrication of devices are needed to favor nonlinear effects, and similarly, an increased operating frequency of MEMS resonators can be targeted to eliminate the effect of the divider in the BRN-PLL PN.

Therefore, the series-tuning technique could be preferred; however, Chapter 2 describes that the compensation is only effective when the negative capacitance equals

exactly C_0 or the proper value of an emulated inductance creates compensation tanks that resonate at the same resonance frequency of the device. Since an exact value for C_0 could not be known a priori, tuning for any of these compensation circuits becomes a requirement to assure the maximum tuning range. Nevertheless, C_0 characterization can be carried out for several devices and close estimates could be obtained, there are error sources that can be added to the expected shunt-parasitic capacitance, for example due to the IC pads and tracks of a printed circuit board (PCB) or packaging. Usually, the IC and the MEMS device are interfaced via bondwires; therefore the length of these interconnecting structures can also add parasitic effects that can reduce the expected tuning.

Thus, an on-chip capacitance measurement unit needs be used to obtain a better estimation of the shunt-parasitic capacitance in situ. This measurement block will inject a current at a frequency different from the resonance of the device and will determine the observed impedance. This method will be run without including the compensation circuitry (active inductors or negative capacitors). The observed capacitance will be associated to a parameter (voltage or charge) that will provide the controlling signal to tune the compensation circuitry. Thus, it is proposed to have a compensation mode prior to the normal operation, and then disconnect the capacitance measuring unit to switch to the compensation element plus series-tuning elements for normal VCO operation.

Once the C_0 capacitances have been properly compensated, Equation 12 is simplified to Equation 11, and the next challenge to address is due to the value of the series-tuning element with respect to the motional capacitance C_s (C_{var} has to be comparable to C_s to achieve significant tuning). According to TSMC documentation, the

values for the varactor can range from 40fF to 1pF [56], which is not comparable to the parameters for a high-Q MEMS device. For example, considering a 100MHz resonator, whose S-parameter measurements report a Q of 5,000 and insertion losses close to -20dB, its lumped-element equivalent model is determined as R_s = 900Ω, L_s =11.8mH and C_s = 0.214fF using Equations 8-10. As observed, the value of C_s is two orders of magnitude less than the minimum value for the varactor. The situation worsens when the frequency of the resonator or the Q are further increased. However, it can be noticed that the value for L_s behaves the opposite way to C_s. Using Figure 19, a tunable inductor will add to the RLC equivalent circuit and its effect is not divided. Configuring a tunable series inductor can produce higher tuning than that of the series varactor.

A series tunable inductor can be implemented with a differential active inductor topology. There are five possible circuits available on [60], and the selection of the best option will be determined by the tuning and the Q of the architecture. For illustration purposes, the Lu Floating Active Inductor [60] is presented in Figure 110 along with its equivalent lumped-model elements. Equations 52-54 summarize the design equations for the differential active inductor.

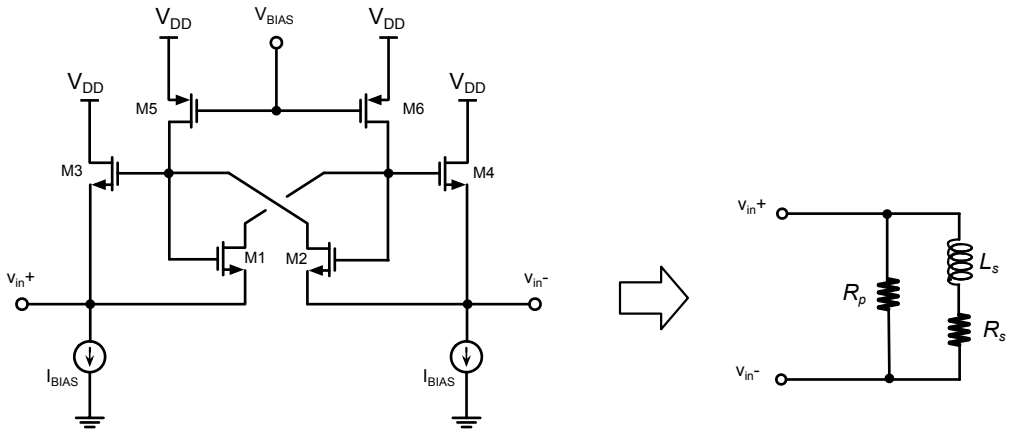


Figure 110. Measured performance the MEMS-based BRN-PLL

$$R_p = \frac{2}{g_{ds5}}, \tag{52}$$

$$R_s = \frac{2\left(g_{ds5} - g_{m1}\right)}{g_{ds5}\left(2g_{m1} + g_{m3} - g_{ds5}\right)}, \tag{53}$$

$$L_s = \frac{2\left(C_{gs1} + C_{gs3}\right)}{g_{ds5}\left(2g_{m1} + g_{m3} - g_{ds5}\right)}. \tag{54}$$

Equation 54 shows that the inductor can be made tunable by changing the transconductances g_{m1} and g_{m3} or by modifying the capacitance between gate and source at transistors M1 and M3. In particular, it can be observed that C_{gs3} can be increased using varactors. The use of series active inductors offers an interesting possibility for tuning MEMS oscillators.

APPENDIX A

ESTIMATION OF THE POWER DELIVERED TO THE RESONATOR

The estimation of the power delivered to the MEMS resonator was used in Chapter 5 to determine the onset of nonlinearity. Thus, given a signal to be delivered to the resonator, it can be established if the power is enough to induce the nonlinear behavior.

The IPS mode of the MEMS resonator was characterized using an Agilent 5071C VNA and a Mini-Circuits ZFL-1000VH power amplifier. Since the VNA manages the power in dBm, the absolute value for the power can be found as

$$P_{dBm} = 10 \cdot \log\left(\frac{P_{abs}}{1\,mW}\right) \rightarrow P_{abs} = 1mW \cdot 10^{\frac{P_{dBm}}{10}}. \quad \text{(A-1)}$$

Thus, assuming 0dBm, the absolute value for the power is equal to 1 mW. The selection of the 0dBm power at the VNA display corresponds to the power that is delivered to the load. Since the equipment expects a DUT with 50Ω input resistance, the effective voltage at the load can be calculated as

$$P_{abs} = \frac{V_{RMS}^2}{50\Omega} \rightarrow V_{RMS} = \sqrt{P_{abs} \cdot 50\Omega}. \quad \text{(A-2)}$$

As the Thévenin equivalent of the output port of the VNA is equal to a voltage source and a 50Ω resistor, the effective voltage that the internal source is delivering can be found as

$$V_{souce\_RMS} = 2\sqrt{P_{abs} \cdot 50\Omega} \rightarrow V_{p-p} = 2\left(\sqrt{2} \cdot \left(2\sqrt{P_{abs} \cdot 50\Omega}\right)\right), \quad \text{(A-3)}$$

where the RMS value has been converted to peak value, using the $\sqrt{2}$ term because the source is sinusoidal. The peak quantity has been doubled to obtain the peak-to-peak value of the voltage source. Therefore, the 0 dBm setting of the VNA corresponds to $1.26V_{p\text{-}p}$ approximately.

Taking the resonator described in this work, the IPS-mode motional resistance was estimated to be 2,300 Ω; therefore at resonance, the voltage at the MEMS device will be $1.24\ V_{p\text{-}p}$ as shown in Figure A-1.

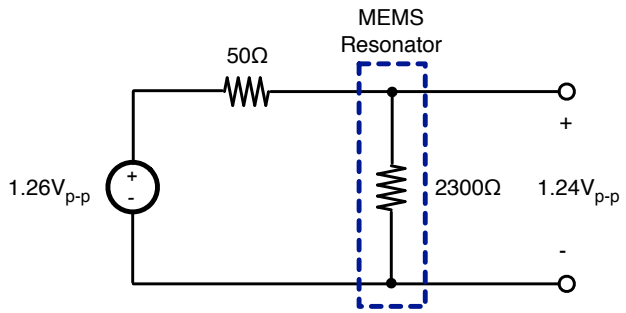


Figure A-1. Actual voltage signal delivered to MEMS resonator

When the resonator is inserted in the loop, the TIA will produce a voltage signal that will drive the resonator. The objective is to work backwards, so that the voltage level can be translated to the associated setting in the VNA. Thus, for $4V_{p\text{-}p}$ generated at the output of the TIA, the corresponding RMS value is 2V, because the signal is hard-clipped and resembles a square waveform. Using the value of the motional resistance and the 50Ω of the VNA, the RMS value for the voltage source is equal to 2.04V. The last value is the one that the VNA would generate internally, but the display of the measuring equipment

corresponds to the one at a 50Ω load. Dividing this value by 2, the power at the load is found to be close to 21mW, which is equivalent to 13.2 dBm. This value is in the onset of nonlinearity.

APPENDIX B

PHASE NOISE OF THE E4438C VECTOR SIGNAL GENERATOR

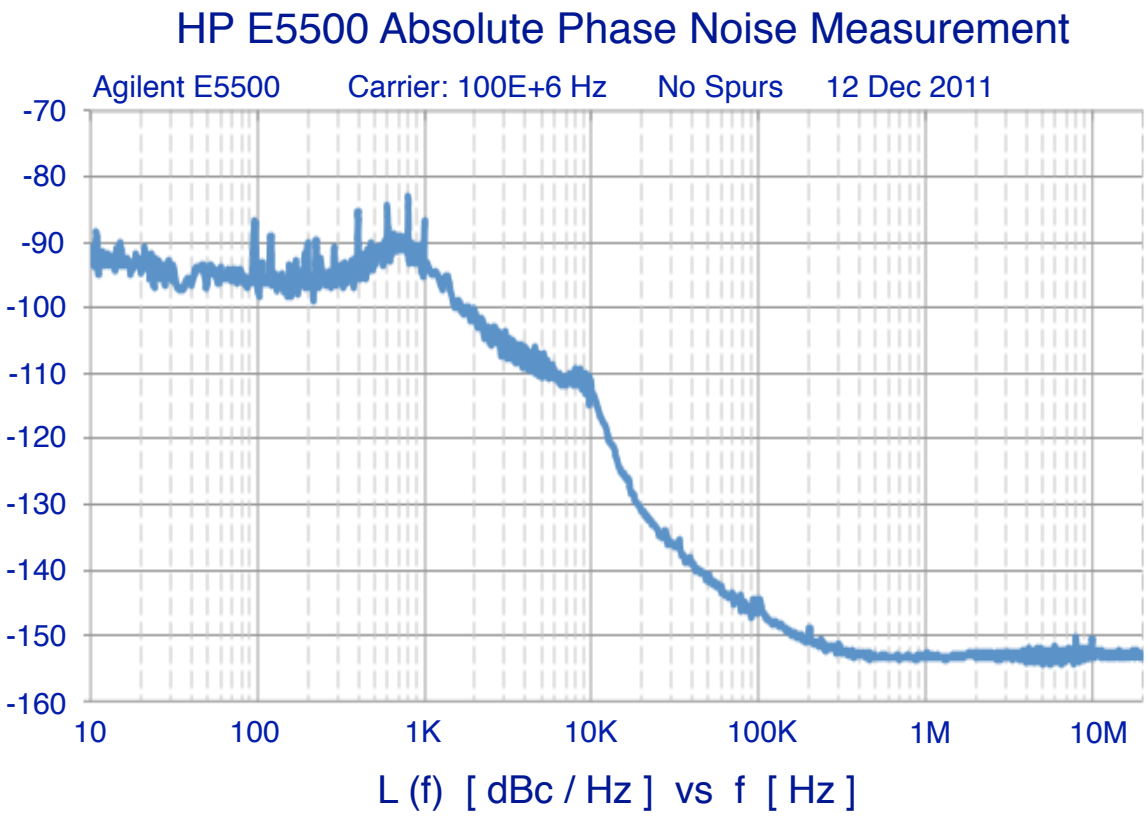


Figure B-1. Phase Noise Measurement at 100MHz

APPENDIX C

INNER-PLL FILTER COMPONENT DEPENDENCY ON K_1

Chapter 6 presented that the value of K_1 (gain of VCO_1) limits the selection of a wider bandwidth for the inner PLL. In this appendix, examples of sample values for the filter components are presented for different values of the K_1 for the widest bandwidth for the system to behave as a continuous system.

Table C-1. Inner-PLL filter components for the K_1 calculated in Section 6.2.

Parameter	Value
Operating Frequency	26 MHz
Charge-pump Current	540 μA
VCO Gain (K_1)	6.2128 kHz/V
Divider Value	1
3dB Bandwidth	1.3 MHz
C_1	5.7 fF
C_2	51.3 fF
R_2	3.2 MΩ
R_3	15.87 MΩ
C_3	0.2 fF
R_H	10 kΩ
C_H	10 pF

Table C-2. Inner-PLL filter components for twice the K_1 calculated in Section 6.2.

Parameter	Value
Operating Frequency	26 MHz
Charge-pump Current	540 μA
VCO Gain (K_1)	12.4 kHz/V
Divider Value	1
3dB Bandwidth	1.3 MHz
C_1	11.4 fF
C_2	102.6 fF
R_2	3.2 MΩ
R_3	7.9 MΩ
C_3	0.41 fF
R_H	10 kΩ
C_H	10 pF

Table C-3. Inner-PLL filter components for ten times the K_1 calculated in Section 6.2.

Parameter	Value
Operating Frequency	26 MHz
Charge-pump Current	540 μA
VCO Gain (K_1)	62.1 kHz/V
Divider Value	1
3dB Bandwidth	1.3 MHz
C_1	57 fF
C_2	513.1 fF
R_2	317.3 kΩ
R_3	1.5 MΩ
C_3	2 fF
R_H	10 kΩ
C_H	10 pF

Thus, it can be observed that for a MEMS-based inner PLL, the value of the bandwidth cannot be the theoretical maximum; instead, a lower bandwidth is required given the expected values for K_1.

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