MODELING, DESIGN, AND CHARACTERIZATION OF THROUGH VIAS IN SILICON AND GLASS INTERPOSERS

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MODELING, DESIGN, AND CHARACTERIZATION OF THROUGH VIAS IN SILICON AND GLASS INTERPOSERS

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To my grandparents, parents, and sister.

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SUMMARY

During the last decade, the trend in consumer electronics has been to develop products with better performance, smaller size, lower cost, and enhanced functionality. Convergent systems need technologies that can integrate digital, RF, analog, and sensor functions with minimal interference. Multi-function integration can be achieved by chip stacking, using 3D IC technology. The 3D IC technology requires very high-density chip-to-interposer interconnections. Organic interposers fail to achieve these targets because of poor dimensional stability, poor thermal performance, high co-efficient of thermal expansion (CTE) mismatch with silicon die, and high cost. Silicon and glass-based 3D interposers are potential candidates for fulfilling the requirements of next-generation ICs and 3D ICs.

The objective of this dissertation is to electrically model through vias in 3D interposers considering silicon biasing effects and, to address power and high-speed signal-integrity issues in 3D interposers.

Accurate electrical modeling of the through package via (TPV) in a 3D interposer is very important. An equivalent circuit-model representation of the TPV enables interposer design and analysis using circuit solvers which is much faster than full-wave 3D electromagnetic simulations. To generate an accurate circuit-model of the TPVs in Si interposers (Si TPVs), it is essential to model the MOS capacitance effect. This dissertation proposes, for the first time, an equivalent circuit-model of the Si TPV considering the bias-voltage-dependent metal-oxide-semiconductor (MOS) capacitance

effect. Important design guidelines and optimizations for the Si TPVs used in the signal-delivery network (SDN), power-delivery network (PDN), and as variable-capacitor elements are proposed.

Glass has excellent insulating properties (just like SiO_2) as compared with the semiconducting nature of silicon. This dissertation studies and compares the advantages and disadvantages of glass and silicon as electronic package substrate materials for 3D interposers. The TPVs in glass interposers (Glass TPVs) are modeled, designed, and simulated by using electromagnetic field solvers. Signal and power integrity analyses are performed for Si TPVs as well as for glass TPVs.

Power integrity plays an important role in driving system performance. Therefore, it is essential to acquire an in-depth understanding of the issues that impact the power integrity of 3D interposers. To provide clean power, decoupling capacitors need to be placed close to the chips. This dissertation presents PDN design in silicon interposers by using the MOS capacitance of Si TPVs for decoupling. In this way, the Si TPV is used not only as an interconnection and wiring element, but also as an important passive component in Si interposers.

High-speed signal-integrity is vital in any electrical system design. In 3D interposers, the issue of crosstalk between high-density TPVs is a concern. Silicon interposers suffer from high substrate loss and enhanced coupling between Si TPVs because of the finite conductivity of Si. This dissertation presents the comparative analysis of the signal-delivery network in 3D interposers for high-speed signal transmissions.

The electrical parasitics of traditional solder-based flip-chip interconnections (for chip-to-chip and chip-to-interposer applications) need to be reduced by at least an order of magnitude considering the clock frequency, supply voltage, and signal-to-noise ratio of future RF and analog mixed-signal systems. In addition, the losses associated with the chip-to-interposer interconnection transitions need to be minimized. To address these challenges, this dissertation presents the electrical modeling, simulation, and characterization of a novel ultra-fine pitch, nano-structured copper-based interconnection technique. Nano-structured electroplated copper is chosen as the interconnection material because of its excellent toughness, fracture strength, good electrical conductivity, and resistance to electromigration. The electrical performance of these interconnections are studied, and compared with traditional Pb-free solder interconnections for chip-to-chip and chip-to-interposer applications.

The major contributions of this dissertation are as follows:

1. Accurate equivalent circuit-model of Si TPVs considering MOS capacitance effects. Design guidelines for Si TPVs in (i) signal-delivery network, (ii) power-delivery network, and (iii) variable-capacitor applications.
2. Power-delivery network design in silicon interposers (using Si TPVs as decoupling capacitors) and glass interposers.
3. Modeling, design, characterization, and signal-integrity analysis of interconnections in glass and silicon interposers.
4. Modeling, design, and characterization of nano-structured copper-based (Nano-Cu) chip-to-interposer interconnections.

CHAPTER 1

INTRODUCTION

Advancements in very large scale integration (VLSI) technology, following Moore's Law, have led to unprecedented transistor and interconnection scaling. As a result, interconnection delay in long global wires is an increasing problem in ICs relative to delays in transistor switching [1, 2]. In the latest microelectronics technology nodes, interconnection delay has become the limiting factor in determining the speed of digital systems [3]. Further, miniaturization by traditional IC scaling in future planar-CMOS technology faces significant challenges [4]. Stacking of ICs using three-dimensional (3D) integration technology helps in significantly reducing wiring lengths, interconnection latency, and power dissipation while reducing the size of the chip and enhancing performance [3, 5-9].

Through silicon vias (TSVs), which are through vias in the IC, are a key enabling technology for 3D IC integration which helps in realizing highly miniaturized, complex, next-generation systems [4]. The 3D integration with TSVs [10-13] has several advantages over wirebonding such as shorter interconnection length, lower electrical parasitics and latency, and higher bandwidth. The TSVs can be formed as area arrays in contrast to peripheral wirebonding leading to greater vertical-interconnection density and reduced form factor [14]. The TSVs also enable heterogeneous integration by stacking ICs with different technologies (e.g., digital IC, analog IC, power IC, MEMS, sensor chips, etc.).

The 3D ICs require large number of I/O connections from the chip stack to the interposer (also known as the package). There is a need to develop low-cost interposer technology which can support this huge I/O need for next-generation 3D ICs. This requires fine-pitch lines, blind vias, and through vias in the interposer. The through vias in the interposer are known as through package vias (TPVs) [15]. The TSVs in stacked ICs as well as TPVs in glass or silicon interposers are important components of a 3D system. Figure 1 shows the schematic view of a 3D system consisting of several ICs and 3D ICs assembled on a high-density interposer which, in turn, is connected to the Printed Circuit Board (PCB).

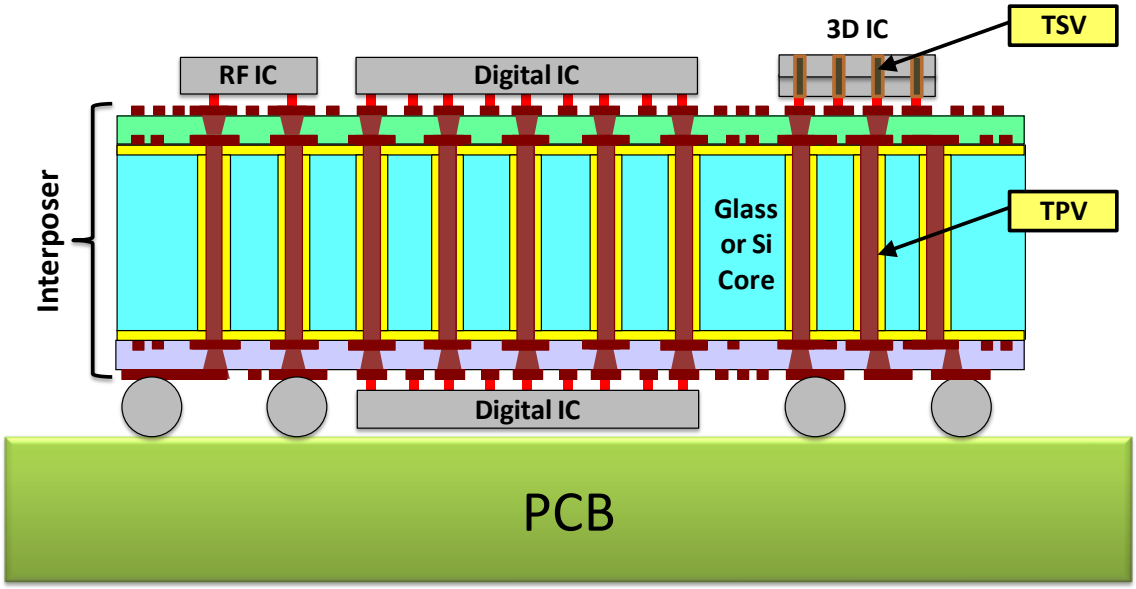


Figure 1. Schematic view of a 3D system (Source: 3D Systems Packaging Research Center).

Interposer technology from the 1960s to the early 1990s was based on ceramic substrates. In the early 1990s, the high performance IC packaging industry transitioned from thick-film-based ceramic substrates to thin-film-based organic interposers, primarily

for cost and performance reasons. Since then, much progress has been made in increasing the wiring density and high I/O capabilities, and reducing the cost of this technology [16, 17]. The organic interposer is now the standard and more than a billion units have been manufactured to package ICs.

Three major barriers are foreseen with organic interposers – (i) limitation in supporting high I/O requirements, (ii) thermal performance, and (iii) cost. All of these barriers limit the use of organic interposers to above 10 µm lithography technologies at about 50 µm pitch. In addition, as the number of layers are increased the organic interposer suffers from warpage [15, 18]. The 3D ICs require I/O pitch down to 10-30 µm with lithography ground rules around 1 µm. Therefore, the challenges for organic interposers are two-fold, as follows:

(i) Poor dimensional stability: Organic interposers suffer from poor dimensional stability which makes alignment of vias in one layer with vias in the next layer impossible without big capture pads. This prevents from achieving the necessary I/O densities.

(ii) High co-efficient of thermal expansion (CTE) mismatch: Organic interposers suffer from high CTE of 18 ppm/^{o}C as compared to silicon of 3 ppm/^{o}C. This large CTE mismatch leads to ultra-low k (ULK) reliability challenges within ICs and 3D ICs. Further, it creates a reliability concern for the interconnection between the interposer and the IC or 3D IC.

Silicon interposers overcome the above problems with organic interposers. They can achieve very high I/O densities because of their excellent dimensional stability and smooth surface finish [19, 20]. Other advantages of silicon interposers are the wide availability of fabrication equipment for wafer processing, and perfect match between the CTEs of the IC and the interposer. Table 1 compares the properties of organic and silicon interposers.

Table 1: Comparison between organic and silicon interposers in 2010.

Property	Organic Interposer	Silicon Interposer
IC-to-Interposer Interconnection Pitch	60-100 µm	40 µm
Interposer line width	20 µm	0.8 µm
IC-to-Interposer CTE match	3 ppm/^{o}C to 17 ppm/^{o}C	3 ppm/^{o}C to 3 ppm/^{o}C
Dimensional Stability	Poor	Good

Silicon interposers face a different set of challenges. They suffer from high electrical loss because of the semiconducting nature of the substrate. Silicon interposer is a costly technology because of expensive wafer-level back end of line (BEOL) facilities, tools, materials, and processes. These interposers are limited to 300 mm wafer sizes.

Glass interposer is a potential alternative to overcome the above-mentioned shortcomings of silicon interposer. Glass, like SiO_2, has very high electrical resistivity (10^{12}-10^{16} Ω-cm) and is dimensionally stable up to at least 500°C. The CTE of glass is close to the CTE of silicon die. Additionally, glass is available in ultra thin (less than 100 µm thickness) and ultra-large (more than 10 sq. meters) panels by a new process called

"Fusion Process" invented by Corning Glass [21]. Large glass panels used for high-definition liquid crystal displays (LCD) can be easily used for processing glass interposers to achieve low cost and high throughput. Availability of thin glass panels eliminates the cost of thinning down the interposer which is required for silicon interposer technology.

However, silicon has some advantages over glass such as superior thermal conductivity. The semiconducting nature of the silicon substrate can also be used for important and novel designs. For example, the voltage-dependent MOS capacitance associated with TPVs in silicon interposers (Si TPVs) can be utilized for power supply decoupling as well as for tunable capacitors and filters.

As mentioned earlier, 3D ICs require ultra-fine pitch interconnections between the IC and the interposer. Reducing I/O pitch and interconnection losses are the two key technological barriers identified by the ITRS [4] for micro/nano electronic modules. The state-of-the-art chip-to-interposer flip-chip interconnections have 30-50 μm diameters (60-80 μm pitch) whereas the substrate interconnections have 50-100 μm line width. Solder based flip-chip interconnections have parasitics (R, L, C) of 27-41 m-Ω [22], 0.1 nH (approximately), and 0.1-0.5 pF [22]. The solder alternatives (ACA/ACF) suffer from high cross-talk between the particles beyond 20 GHz [23].

The above parasitics should be reduced by at least an order of magnitude considering the clock frequency, supply voltage, and signal-to-noise ratio of future RF and analog mixed-signal systems. In addition, the losses associated with the chip-to-interposer interconnection transitions should be minimized. To address these challenges,

this dissertation proposes a novel, ultra-fine pitch chip-to-interposer interconnection technique based on nano-structured copper. Nano-structured electroplated copper is chosen as the interconnection material because of its excellent toughness, fracture strength [24], good electrical conductivity, and resistance to electromigration.

1.1 Previous Research on Through Package Vias in Si Interposers

Electrical modeling of Si TPVs is very important for 3D system design and analysis, and consequently there have been several publications focusing on Si TPV modeling and simulations. In [25-27], two-port vector network analyzer (VNA) measurements were performed on Si TPVs. An equivalent circuit-model of the Si TPVs was proposed and its parameters were fitted to match the measured data. In [28], 2-port VNA measurements were performed on a two Si TPV chain. The S-parameters of the Si TPVs were obtained by de-embedding the interconnection lines. An equivalent circuit-model was proposed and its parameters were fitted to the de-embedded measurement data. However, in these studies, the Si substrate was left floating without any bias on it. In [29], a simplified R-L model of a Si TPV was extracted from VNA measurement without biasing the Si substrate, as well.

In [30], Si TPVs were analyzed as parallel round wires. An equivalent circuit-model for Si TPVs was proposed based on this analysis and the results were compared with full-wave electromagnetic (EM) simulation results. The circuit-model correlated well with the simulation results only beyond 30 GHz. The Si substrate was not biased in either the analysis or the EM simulation. In [31], an equivalent circuit-model of four Si TPVs (in GSSG configuration) was proposed and its values were obtained by curve

fitting to simulation results. An analytical modeling of propagation delay in Si TPVs was presented in [32]. In [33], equivalent circuit-models of isolated and coupled Si TPVs were presented. The model parameters were expressed by empirical equations and extracted using a quasi-static electromagnetic field solver.

All the aforementioned papers related to Si TPV modeling have considered the Si substrate as a lossy dielectric material and ignored its semiconducting properties. These models neglect the voltage-dependent MOS capacitance associated with Si TPVs. Ignoring the semiconductor properties of the substrate and the resulting MOS capacitance introduces significant inaccuracies in the modeling of the capacitance in these structures.

This dissertation presents in-depth study of the semiconducting and biasing effects in silicon interposers. It presents a more accurate electrical model of a Si TPV by considering the MOS capacitance effects. The results are correlated with measurement data to validate the model. Design guidelines are proposed for designing Si TPVs in the signal and power-delivery networks as well as for Si TPVs in variable-capacitor applications. Power-delivery network in silicon interposers is designed using Si TPVs as decoupling capacitors.

1.2 Previous Research on Through Package Vias in Glass Interposers

Glass as an electronic packaging substrate has been investigated in the recent past. The research has mostly focused on the formation and metallization of interconnections in glass interposers. Fraunhofer IZM has reported on through via formation using different lasers and surface metallization in glass. Formation of optical waveguides on glass using ion exchange methods have been studied for photonic

applications [34-37]. The use of excimer laser machining for forming pads, traces, and microvias in glass substrates have also been explored [38].

Laminated glass substrates have been examined by Loughborough University for interconnecting ICs and photonic devices [39]. The key challenges addressed were via formation in glass using lasers, direct metallization in glass using self-assembled mono-layers (SAM), and glass-to-glass bonding to from a multi-layer interposer. The NEC Schott company has demonstrated the use of glass wafers with metalized tungsten vias providing electrical connection and hermetic sealing [40]. This approach is based on flowing glass over tungsten plugs resulting in through vias (approximately 100 μm in diameter) in glass substrate.

This dissertation focuses on the modeling, design, signal-integrity analysis, and characterization of TPVs in glass interposers. Electromagnetic modeling and simulations are performed for glass TPVs with different dimensions to study the signal loss and crosstalk. The electrical performance of glass TPVs is compared with Si TPVs. Re-distribution layer (RDL) line to TPV transition structures are designed and simulated to estimate the loss and crosstalk. The effect of varying different material and physical parameters of the interconnections in the glass interposer on the signal-integrity is studied.

1.3 Previous Research on Nano-Copper Interconnections

Nano-structured metal-based interconnections have been developed and studied [24, 41-43]. Most of the research in this area has focused on the fabrication and reliability of these interconnections. Nano-structured nickel-based chip-to-interposer interconnections have been developed at 200 µm pitch [41]. Resistance and inductance of the Nano-nickel interconnections were extracted from measured data and compared with solder based interconnection.

It has been reported that nano-structured copper interconnections have enhanced fracture toughness and fatigue resistance as compared with bulk copper [24]. Nano-structured metals usually have higher resistivity than bulk metals [44, 45]. However, it was shown that nano-structured copper with a high density of nanoscale growth twins have enhanced tensile strength but similar electrical resistivity as compared to pure copper [46]. The electrical parasitics of the Nano-Cu interconnections have been extracted from EM simulations [42, 43]. The simulated response was curve fitted to an equivalent circuit-model to extract the electrical parasitics.

This dissertation studies the high-frequency performance of nano-copper-based chip-to-interposer interconnections (with dimensions in the order of 15 to 0.5 µm) for chip-on-interposer and chip-on-chip configurations. Physical and material parametric studies are performed on this interconnection by means of full-wave EM simulations. Important interconnection and package design guidelines (obtained from the parametric analysis) are also presented for this nano-copper-based chip-to-interposer interconnection.

1.4 Outline of Dissertation

The dissertation is broadly organized as follows. Chapter 2 describes the modeling and design of TPVs in silicon interposers. Chapter 3 describes the modeling and design of TPVs in glass interposers. Chapter 4 presents the design and comparative analysis of power-delivery networks in Si and glass interposers. The characterization of interconnections in Si and glass interposers is presented in Chapter 5. Chapter 6 presents the modeling and design of ultra-fine pitch Nano-Cu chip-to-interposer interconnections. Chapter 7 concludes this dissertation and proposes future work.

CHAPTER 2

TPV IN SILICON INTERPOSERS

Three-dimensional (3D) integration of microelectronic systems reduces the interconnection length, wiring delay, and system size while enhancing functionality by heterogeneous integration. Through silicon vias (TSVs) are the vertical interconnections in 3D ICs. Through package via in silicon interposers (Si TPV) is a key building block for high performance 3D systems. Si TPVs are sometimes referred as TSVs in published literature. This chapter presents accurate electrical modeling of Si TPVs considering metal-oxide-semiconductor (MOS) capacitance effects. Parametric analysis of Si TPV capacitance is performed on several physical and material parameters. Design guidelines are proposed for Si TPVs used in signal and power-delivery networks as well as for Si TPVs as variable capacitors.

2.1 MOS Capacitance in Si TPVs

Through package vias in Si interposers (Si TPVs) have a cylindrical metal-oxide-semiconductor (MOS) structure as shown in Figure 2. The Si substrate has a layer of SiO_2 liner on its top and bottom surfaces. The through hole is lined with a dielectric material (usually SiO_2), and filled with a conductive material (typically a metal). The Si substrate is doped either n-type or p-type and is biased (usually to ground potential).

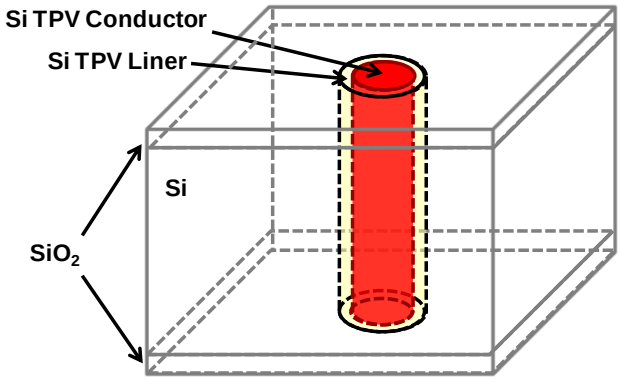


Figure 2. Structure of a through package via in Si interposer (Si TPV).

The inner conductor of the Si TPV acts as a metal electrode separated from the biased Si substrate by the dielectric liner - similar to the metal electrode in a MOS capacitor or the gate in a MOSFET. Figure 3 shows a typical capacitance (C_g) plot with change in the gate voltage (V_g) for a planar MOS structure in a p-type doped Si substrate. The C-V plot for the MOS capacitance effect in Si TPV also exhibits a similar trend [47].

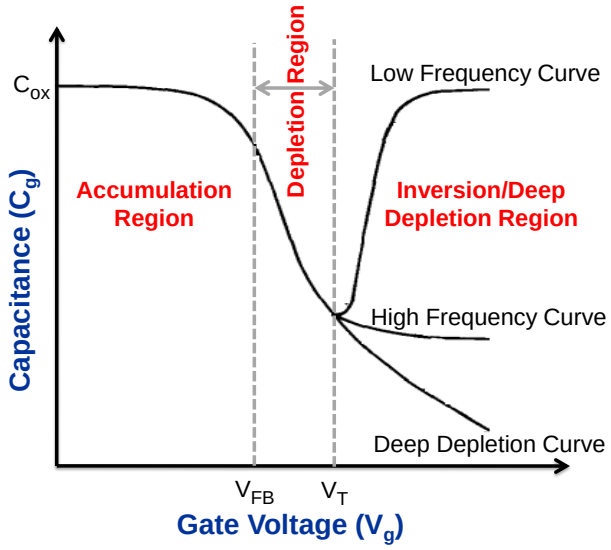


Figure 3. Capacitance-Voltage plot for a planar-MOS capacitor in p-type Si. (V_{FB}: Flat band voltage, V_T: Threshold voltage, C_{ox}: Oxide capacitance)

As shown in Figure 3, at high gate voltages the MOS capacitance has three possibilities - deep depletion, high frequency, and low frequency.

When the DC component of the gate voltage changes very fast (typically, > 5 V/s) the generation of minority carriers cannot keep up with the rate of change of the gate voltage [48]. Hence, no inversion region is formed. Any increase in the gate voltage is matched by an increase in the width of the depletion region resulting in the deep depletion mode of operation. Si TPVs in the signal-delivery network of digital systems carry high-frequency signals with sharp rise and fall time, and therefore follow the deep depletion C-V curve.

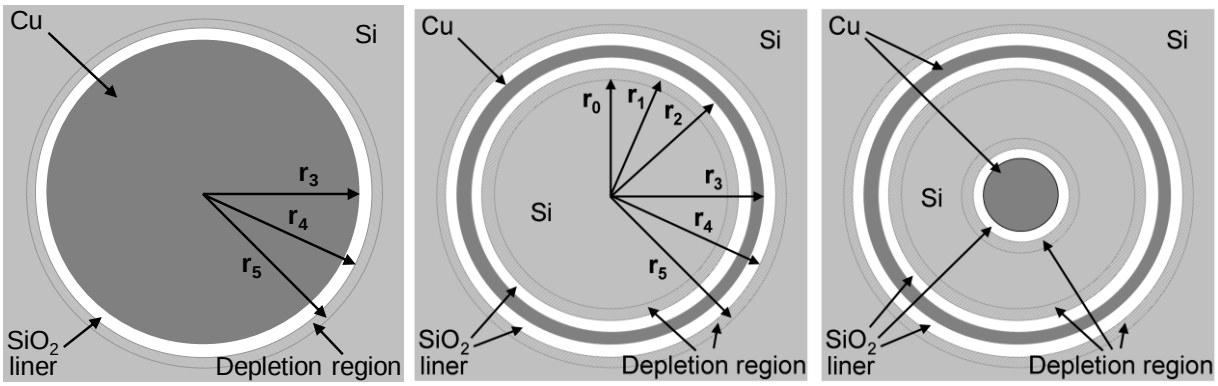
When the DC component of the gate voltage changes slowly, an inversion region is formed for high gate voltage. The MOS capacitor behavior is determined by the frequency of the small signal AC component of the gate voltage. The minority carrier generation rate cannot keep up with high-frequency (typically, > 1 MHz) small signal AC component of the gate voltage [48]. In this high frequency mode of operation, the depletion width changes with any AC change in the gate voltage. Si TPVs in the power-delivery network of digital systems carry DC power along with high-frequency noise (such as simultaneous switching noise). These Si TPVs follow the high frequency C-V curve.

When the gate voltage has a low frequency small signal AC component, the minority carrier generation rate matches any change in the gate voltage. The width of the inversion region changes with the gate voltage in this low frequency mode of operation. Si TPVs in an ideal power-delivery network (i.e., without any high-frequency noise) follow the low frequency C-V curve.

2.2 Electrical Modeling

The MOS capacitance of a Si TPV is analytically modeled in this section. The electric field, potential, and charge distribution around the Si TPV is obtained by solving Poisson's equation in cylindrical co-ordinates. The charges, if present, in the SiO_2 liner and the Si-SiO_2 interface are neglected. The Si substrate is modeled to be biased at ground potential. The analysis is performed for a p-type Si substrate but a similar analysis can also be performed for an n-type Si substrate as well.

Three types of Si TPV shapes are considered as shown in Figure 4. The MOS capacitance analysis is performed at (i) the inner surface and, (ii) the outer surface of the Si TPV. The cylindrical Si TPVs require only the second analysis while the annular and co-axial Si TPVs require both the analyses. The case of the cylindrical Si TPV (i.e., the analysis at the outer surface) is presented first.



(a) (b) (c)

Figure 4. Schematic cross-section diagram of Si TPV (with SiO_2 liner) biased in the depletion region of operation. (a) Cylindrical Si TPV. (b) Annular Si TPV. (c) Co-axial Si TPV.

2.2.1 Full Depletion Approximation Analysis

The analysis is first performed with the full depletion approximation (FDA). The FDA simplifies the analysis by assuming that the depletion region (formed in the semiconductor) is fully depleted (i.e., there are no mobile charge carriers in the depletion region). The more detailed analysis is presented in Section 2.2.2.

2.2.1.1 Outer Surface

The voltage on the Si TPV, V_{TPV}, can be expressed by the following equation:

$$V_{TPV} = \frac{Q_{TPV}}{C_{ox,out}} + V_{FB} + \varphi_S \qquad (1)$$

where,

Q_{TPV} = Charge on the Si TPV

$C_{ox,out}$= SiO_2 liner capacitance

V_{FB} = Flat band voltage

φ_S = Surface potential at the Si-SiO_2 interface.

For a Si TPV (as shown in Figure 4) with length L, the oxide layer capacitance at the outer surface ($C_{ox,out}$) can be expressed by the cylindrical capacitor formula as follows:

$$C_{ox,out} = \frac{2\pi\varepsilon_{ox}L}{ln\frac{r_4}{r_3}} \qquad (2)$$

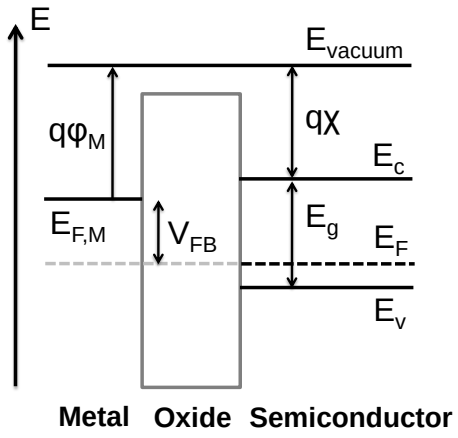


Figure 5. Energy diagram of a metal-oxide-semiconductor (MOS) junction at flat band condition. The semiconductor is doped p-type.

The flat band voltage (V_{FB}) is the voltage that needs to be applied on the Si TPV to obtain a flat band energy diagram as shown in Figure 5. In a flat band condition, there are no charges in the semiconductor. V_{FB} is the difference between the work function of the Si TPV metal (φ_M) and the silicon (φ_{Si}). It can be expressed by the following equation:

$$V_{FB} = \varphi_M - \varphi_{Si} = \varphi_M - X - \frac{E_g}{2q} - \varphi_t ln \frac{N_a}{n_i} \qquad (3)$$

where,

X = Electron affinity of Si (4.05 V)

E_g = Band gap energy of Si (1.12 eV at room temperature)

q = Electronic charge (1.6022×10^{-19} coulombs)

$\varphi_t = \frac{KT}{q} =$ 0.026 V (at 300 ^oK)

K = Boltzmann's constant = 1.3807×10^{-23} m^2 kg s^{-2} K^{-1}

T = Absolute temperature

N_a = Doping concentration of the acceptor ions

n_i = Intrinsic carrier concentration of Si (1.18×10^{10} cm^{-3} at 300 ^oK).

To calculate the surface potential (φ_S), the charge distribution around the Si TPV can be represented by Poisson's equation in cylindrical co-ordinates as follows:

$$\frac{d^2\varphi}{dr^2} + \frac{1}{r}\frac{d\varphi}{dr} = -\frac{\rho}{\varepsilon_S} \qquad (4)$$

φ and ρ are the potential and charge density at a radius r, respectively, and ε_S is the permittivity of Si. Due to geometry, the charge distribution is modeled to be axisymmetric and not varying along the length of the Si TPV.

Poisson's equation in cylindrical co-ordinates (Equation 4) can be solved with the full depletion approximation (FDA) to simplify the analysis. In the FDA, the depletion layer charge is approximated to be entirely because of the ionized acceptor atoms. Equation 4 can be re-written as following:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\varphi}{dr}\right)=\frac{qN_a}{\varepsilon_S} \qquad (5)$$

The potential and the electric field at the edge of the outer depletion region ($r = r_5$ in Figure 4) is zero. Integrating Equation 5 from r (where $r_4 < r < r_5$) to r_5,

$$-r\frac{d\varphi}{dr}=\frac{qN_a}{2\varepsilon_S}(r_5^2-r^2) \qquad (6)$$

Integrating from r_4 to r_5,

$$\varphi_S=\frac{qN_a}{2\varepsilon_S}\left(r_5^2 ln\frac{r_5}{r_4}-\frac{r_5^2-r_4^2}{2}\right) \qquad (7)$$

where φ_S = Surface potential at the Si-SiO_2 interface.

The charge on the metal, Q_{TPV} is equal to the charge in the depletion region.

$$Q_{TPV}=qN_a\pi(r_5^2-r_4^2) \qquad (8)$$

Equation 1 can be re-written using Equations 2, 3, 7, and 8 as the following:

$$V_G=\varphi_M-\chi-\frac{E_g}{2q}-\varphi_t ln\frac{N_a}{n_i}+\frac{qN_a}{2\varepsilon_S}\left(r_5^2 ln\frac{r_5}{r_4}-\frac{r_5^2-r_4^2}{2}\right)$$

$$+\frac{qN_a(r_5^2-r_4^2)}{2\varepsilon_{ox}}ln\frac{r_4}{r_3} \qquad (9)$$

The radius of the edge of the depletion region, r_5, is calculated from Equation 9. It is used to calculate the depletion capacitance.

$$C_{d,out}=\frac{2\pi\varepsilon_s L}{ln\frac{r_5}{r_4}} \qquad (10)$$

The total Si TPV capacitance (C_{TPV}) is a series combination of the oxide and depletion capacitance.

$$\frac{1}{C_{TPV}} = \frac{1}{C_{ox,out}} + \frac{1}{C_{d,out}} \qquad (11)$$

At threshold condition, the Si-SiO_2 surface potential is twice the bulk potential(φ_B).

$$\varphi_S = 2\varphi_B = 2\varphi_t ln\frac{N_a}{n_i} \qquad (12)$$

The radius of the outer depletion region edge at threshold ($r_{5,T}$) is calculated by equating Equation 7 to $2\varphi_B$.

$$\frac{qN_a}{2\varepsilon_S}\left(r_{5,T}^2 ln\frac{r_{5,T}}{r_4} - \frac{r_{5,T}^2 - r_4^2}{2}\right) = 2\varphi_B \qquad (13)$$

Using Equations 9 and 13, the threshold voltage can be calculated by the following equation:

$$V_{T,out} = \varphi_M - \chi - \frac{E_g}{2q} + \varphi_t ln\frac{N_a}{n_i} + \frac{qN_a\left(r_{5,T}^2 - r_4^2\right)}{2\varepsilon_{ox}} ln\frac{r_4}{r_3} \qquad (14)$$

2.2.1.2 Inner Surface

The inner surface analysis is applicable for annular and co-axial Si TPVs. The voltage on the Si TPV, V_{TPV}, can be expressed by the following equation:

$$V_{TPV} = \frac{Q_{TPV}}{C_{ox,out}} + V_{FB} + \varphi_S \qquad (15)$$

where,

Q_{TPV} = Charge on the Si TPV

$C_{ox,in}$= SiO_2 liner capacitance

V_{FB} = Flat band voltage

φ_S = Surface potential at the Si-SiO_2 interface.

For a Si TPV (as shown in Figure 4) with length L, the oxide layer capacitance at the inner layer ($C_{ox,in}$) can be expressed by the cylindrical capacitor formula.

$$C_{ox,in} = \frac{2\pi\varepsilon_{ox}L}{ln\frac{r_2}{r_1}} \qquad (16)$$

To calculate the surface potential (φ_S), the charge distribution around the Si TPV can be represented by Poisson's equation in cylindrical co-ordinates which can be simplified with the FDA to obatin Equation 5. The potential and the electric field at the edge of the inner depletion region (r = r_0 in Figure 4) is zero. Integrating Equation 5 from r_0 to r (where $r_0 < r < r_1$),

$$r\frac{d\varphi}{dr} = \frac{qN_a}{2\varepsilon_S}(r^2 - r_0^2) \qquad (17)$$

Integrating from r_0 to r_1,

$$\varphi_S = \frac{qN_a}{2\varepsilon_S}\left(\frac{r_1^2 - r_0^2}{2} - r_0^2 ln\frac{r_1}{r_0}\right) \qquad (18)$$

where φ_S = Surface potential at the Si-SiO_2 interface.

The charge on the metal, Q_{TPV} is equal to the charge in the depletion region.

$$Q_{TPV} = qN_a\pi(r_1^2 - r_0^2) \qquad (19)$$

Equation 15 can be re-written using Equations 3, 16, 18, and 19 in the following way:

$$V_G = \varphi_M - \chi - \frac{E_g}{2q} - \varphi_t ln\frac{N_a}{n_i} + \frac{qN_a}{2\varepsilon_S}\left(\frac{r_1^2 - r_0^2}{2} - r_0^2 ln\frac{r_1}{r_0}\right)$$

$$+ \frac{qN_a(r_1^2 - r_0^2)}{2\varepsilon_{ox}} ln\frac{r_2}{r_1} \qquad (20)$$

The radius of the edge of the depletion region, r_0, is calculated from Equation 20. It is used to calculate the depletion capacitance.

$$C_{d,in} = \frac{2\pi\varepsilon_s L}{ln\frac{r_1}{r_0}} \qquad (21)$$

The capacitance of an annular Si TPV is a combination of the inner and outer surface capacitances.

$$C_{TPV} = \left(\frac{1}{C_{ox,in}} + \frac{1}{C_{d,in}}\right)^{-1} + \left(\frac{1}{C_{ox,out}} + \frac{1}{C_{d,out}}\right)^{-1} \qquad (22)$$

At threshold condition, the Si-SiO_2 surface potential is twice the bulk potential(φ_B), as expressed in Equation 12. The radius of the inner depletion region edge at threshold ($r_{0,T}$) is calculated by equating Equation 18 to $2\varphi_B$.

$$\frac{qN_a}{2\varepsilon_S}\left(\frac{r_1^2 - r_0^2}{2} - r_0^2 ln\frac{r_1}{r_0}\right) = 2\varphi_B \qquad (23)$$

Using Equations 20 and 23, the threshold voltage is given as follows:

$$V_{T,in} = \varphi_M - \chi - \frac{E_g}{2q} + \varphi_t ln\frac{N_a}{n_i} + \frac{qN_a\left(r_1^2 - r_{0,T}^2\right)}{2\varepsilon_{ox}} ln\frac{r_2}{r_1} \qquad (24)$$

2.2.2 Exact Analysis

The full depletion approximation (FDA) enables a simple analysis but it does not provide the most accurate result. Poisson's equation in cylindrical co-ordinates (Equation 4) can be analyzed rigorously without using the FDA to obtain a more accurate result.

The charge distribution in the silicon is composed of fixed doping ions (N_a), holes (p), and electrons (n) in the semiconductor. The charge density can therefore be expressed by the following equations:

$$\rho = q(-N_a + p - n) \qquad (25)$$

$$\rho = qN_a\left(-1 + e^{-\frac{\varphi}{\varphi_t}} - e^{\frac{\varphi-2\varphi_B}{\varphi_t}}\right) \qquad (26)$$

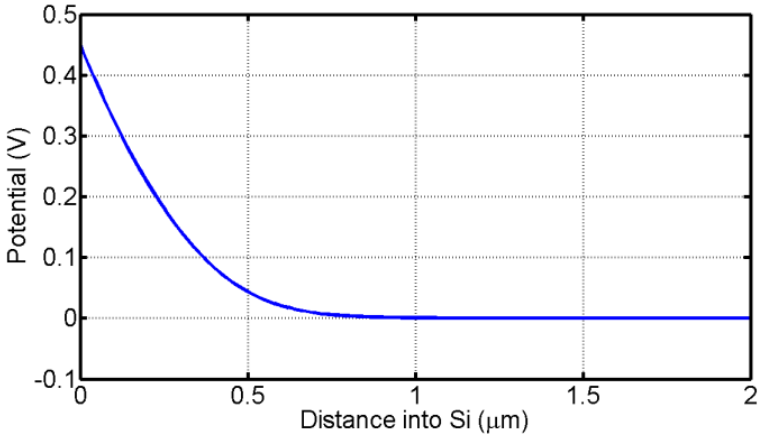
$$\varphi_B = \varphi_t ln\frac{N_a}{n_i} \qquad (27)$$

Equation 4 can be re-written using Equation 26 as following:

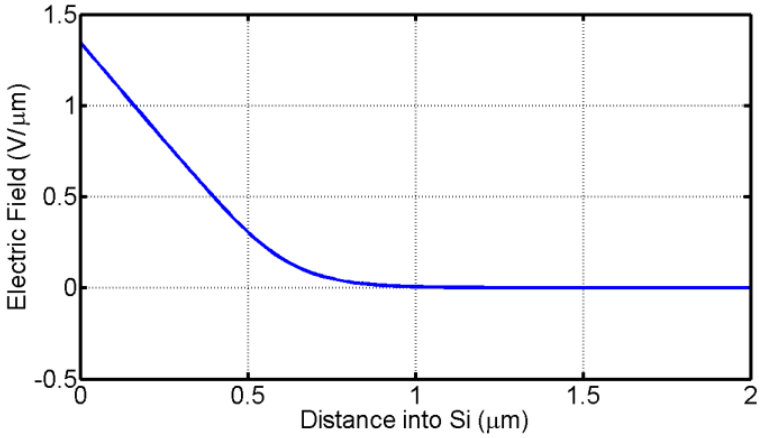
$$\frac{d^2\varphi}{dr^2} + \frac{1}{r}\frac{d\varphi}{dr} = \frac{qN_a}{\varepsilon_S}\left(1 - e^{-\frac{\varphi}{\varphi_t}} + e^{\frac{\varphi-2\varphi_B}{\varphi_t}}\right) \qquad (28)$$

There are no analytical solutions to Equation 28. Hence, this equation is solved numerically using the classical 4th order Runge-Kutta method [49] in MATLAB.

The initial conditions are the surface potential (φ) and electric field ($-d\varphi/dr$) at the Si-SiO_2 interface (r = r_4). For a given surface potential, the electric field at the Si-SiO_2 interface is obtained iteratively such that the potential and electric field distributions converge as shown in Figure 6 (a) and (b).



(a)



(b)

Figure 6. (a) Potential and, (b) Electric field distribution in Si as a function of the distance from the Si-SiO_2 interface when V_{TPV} = 0.6V. Oxide liner thickness = 0.1 μm.

The distance at which the potential and electric fields become zero represents the edge of the depletion region. Equation 26 along with the potential distribution can be used to plot the charge distribution in Si as shown in Figure 7.

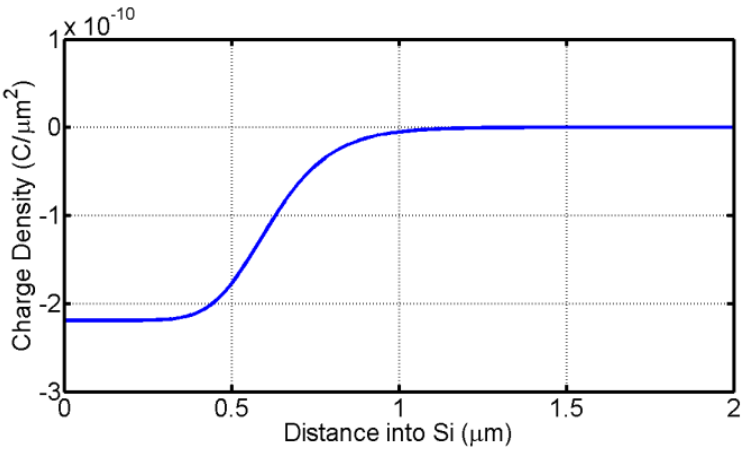


Figure 7. Charge distribution in Si as a function of the distance from the Si-SiO_2 interface when V_{TPV} = 0.6V.

The charge on the Si TPV (Q_{TPV}) is equal to the total charge in the Si.

$$Q_{TPV} = \varepsilon_S \oint_S E\, dS = -2\pi r_4 L \varepsilon_S \left.\frac{d\varphi}{dr}\right|_{r=r_4} \qquad (29)$$

In Equation 29, the value of the electric field at the Si-SiO_2 interface ($r = r_4$) is obtained from the numerical solution of Equation 28. Using Equations 1, 2, 3, and 29, the voltage on the Si TPV for a given surface potential can be calculated. The Si TPV capacitance for a given Si TPV voltage is also calculated from the potential and electric field distributions in Si.

$$C_{TPV} = \left.\frac{dQ}{d\varphi}\right|_{r=r_4} \qquad (30)$$

$$\Rightarrow C_{TPV} = 2\pi r_4\, \varepsilon_S \left.\frac{d}{d\varphi}\left(-\frac{d\varphi}{dr}\right)\right|_{r=r_4} \qquad (31)$$

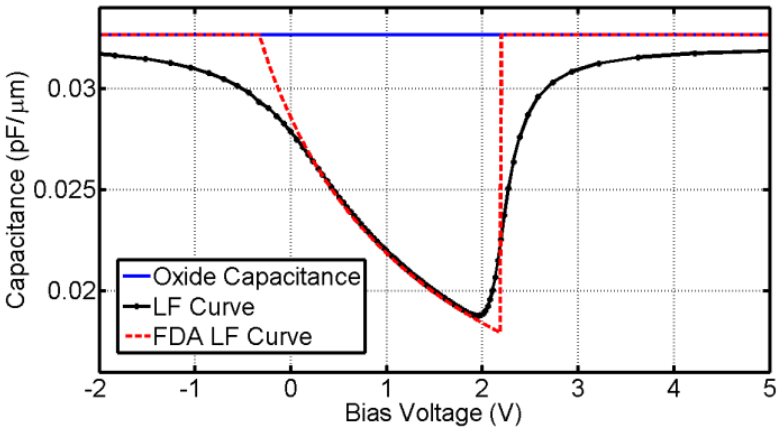
The threshold point is reached when $\varphi_S = 2\varphi_B$. At this point, the Si TPV voltage is called the threshold voltage (V_T).

In low frequency operation, the Si TPV capacitance is obtained from Equation 31. In high-frequency operation, beyond the threshold voltage, the Si TPV capacitance remains constant at the capacitance value reached at threshold point. In the deep depletion mode of operation, the inversion region (composed of minority charges) does not form due to the fast change in the DC component of the voltage carried by the Si TPV. The capacitance in this mode, beyond the threshold voltage, is obtained by neglecting the minority carrier density (n in a p-type doped Si substrate) in Equation 25.

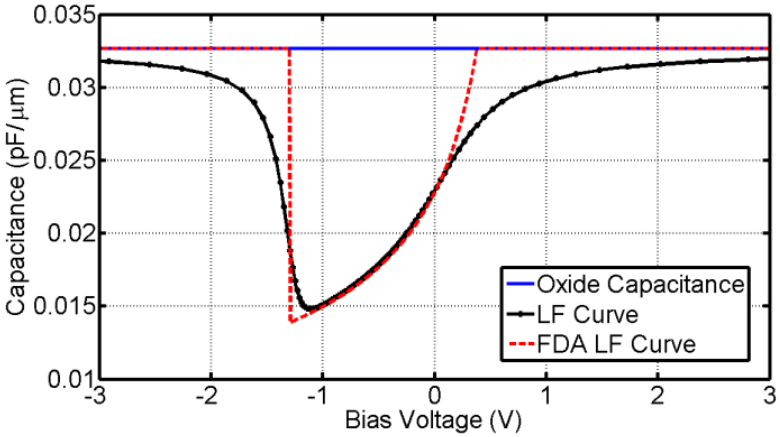
The low frequency, high frequency, and deep depletion Si TPV capacitance-voltage (C-V) curves are shown in Figure 8, Figure 9, and Figure 10 respectively. These figures compare the Si TPV C-V plots obtained by this analysis with those obtained by using the FDA. The Si TPV is modeled to be filled with copper. It is 30 μm in diameter with 0.1 μm thick SiO_2 liner. The resistivity of the Si substrate is 1 Ω-cm resistivity. In Figure 8, Figure 9, and Figure 10, the term 'Bias Voltage' refers to the voltage difference between the Si TPV and the Si substrate.

If the MOS capacitance effect is neglected then the Si TPV capacitance is equal to just the oxide capacitance. The solid blue curves in Figure 8, Figure 9, and Figure 10 represents this C-V plot. It is observed from these figures that neglecting the MOS effect in Si TPV can lead to significant inaccuracies in calculating its capacitance. Using only the oxide capacitance (by neglecting the MOS effect) results in over estimation of the

TSV capacitance. This can lead to errors while designing interconnections in 3D ICs and Si interposers.

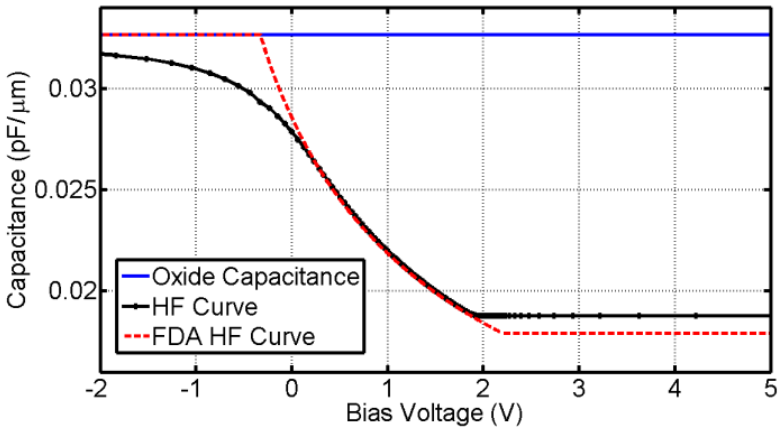


(a)

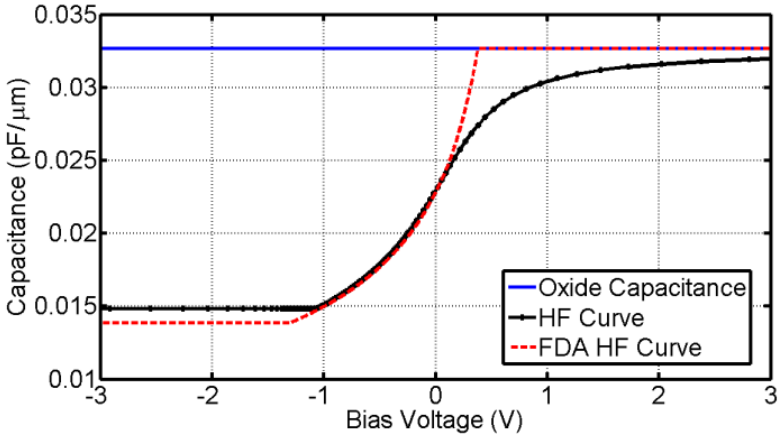


(b)

Figure 8. Per unit length Si TPV capacitance-voltage plots for low frequency operation in (a) p-type doped silicon, and (b) n-type doped silicon. Black solid curve with dots: Exact C-V plot. Red dotted curve: C-V plot assuming full depletion approximation. Blue solid curve: Oxide capacitance (C-V plot neglecting MOS effect).

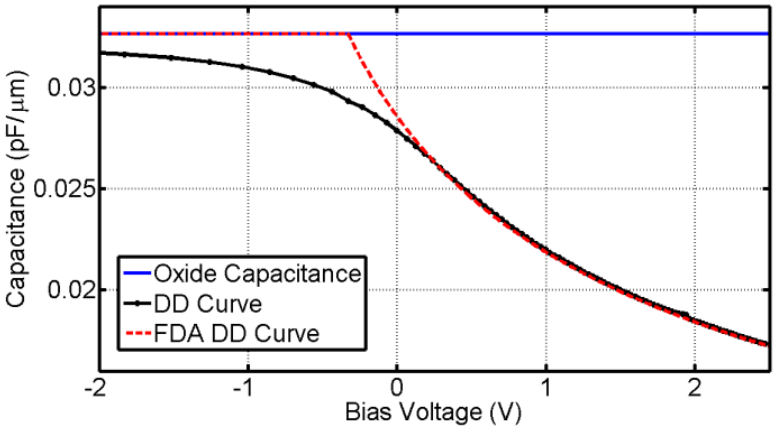


(a)

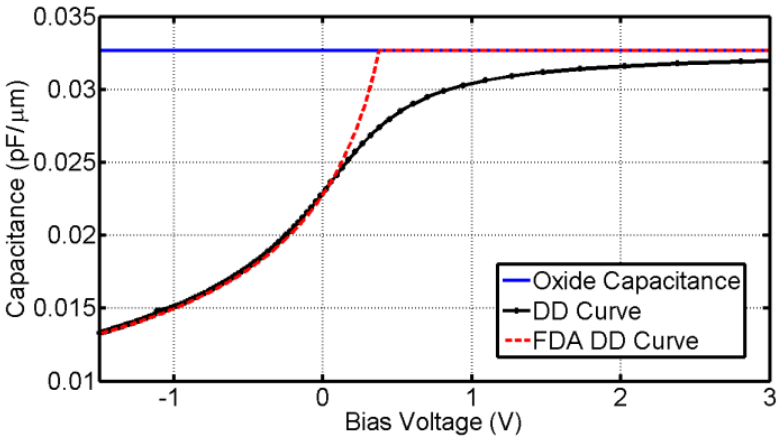


(b)

Figure 9. Per unit length Si TPV capacitance-voltage plots for high frequency operation in (a) p-type doped silicon, and (b) n-type doped silicon. Black solid curve with dots: Exact C-V plot. Red dotted curve: C-V plot assuming full depletion approximation. Blue solid curve: Oxide capacitance (C-V plot neglecting MOS effect).



(a)



(b)

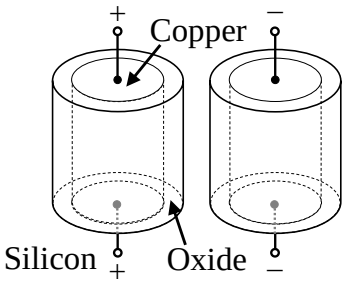
Figure 10. Per unit length Si TPV capacitance-voltage plots for deep depletion operation in (a) p-type doped silicon, and (b) n-type doped silicon. Black solid curve with dots: Exact C-V plot. Red dotted curve: C-V plot assuming full depletion approximation. Blue solid curve: Oxide capacitance (C-V plot neglecting MOS effect).

From Figure 8, Figure 9, and Figure 10 it is observed that the FDA solution results in considerable error near the flat band and threshold regions. The FDA assumes that there are no mobile charge carriers (holes or electrons) in the depletion region. In the low frequency operation FDA approximates the Si TPV capacitance to be equal to the liner capacitance in the accumulation and inversion regions.

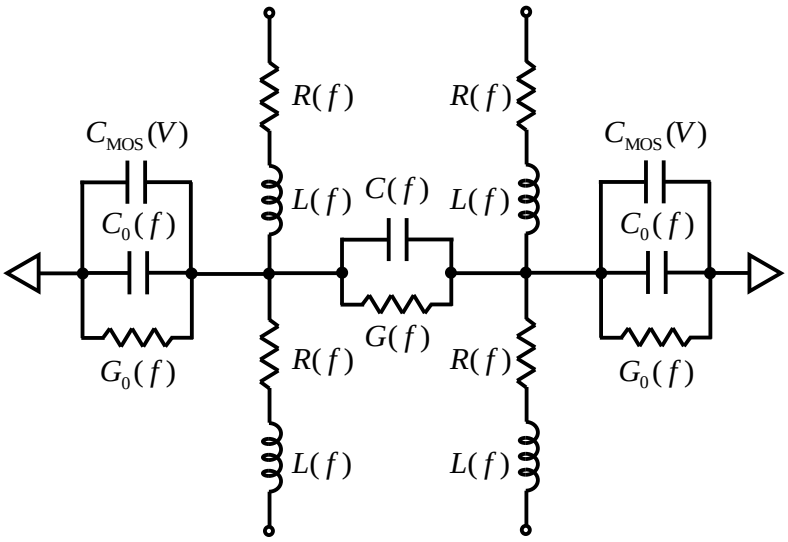
In reality, there are significant contributions from the mobile charge carriers near the flat band and threshold points. This is the cause for the inaccuracies suffered by the full depletion approximation. The numerical analysis of Poisson's equation considering the fixed and mobile charges in Si, as described in this section, captures the actual Si TPV C-V relationship. This analysis considers uniform doping in the Si substrate. The analysis for a non-uniformly doped Si substrate can be performed as a continuation of this research work in the future. The effect of generation-recombination can also be studied in detail as part of a future work.

2.2.3 Electrical Model

Modeling the MOS capacitance of the Si TPV is important in developing an accurate electrical circuit-model. Figure 11 shows the equivalent circuit-model of a pair of Si TPVs.



(a)



(b)

Figure 11. (a) Schematic view, and (b) Equivalent circuit-model of a pair of Si TPVs.

The frequency dependent parameters R(f), L(f), C(f), G(f), C_0(f), and G_0(f) are derived in [50]. R(f) and L(f) represents the resistance and inductance of the Si TPV. C(f) is the coupling capacitance between the Si TPVs while G(f) is the silicon substrate conductance between the Si TPVs. C_0(f) and G_0(f) are the capacitance and substrate conductance to ground respectively. C_{MOS}(V) represents the voltage-dependent MOS capacitance of the Si TPV.

Figure 12 shows the electrical parasitics of a pair of Si TPVs. The via diameter was 30 µm, via pitch was 60 µm, and via length was 100 µm. Four models were modeled – (i) 0.1 µm thick SiO_2 liner and 10 S/m Si conductivity, (ii) 0.5 µm thick SiO_2 liner and 10 S/m Si conductivity, (iii) 0.1 µm thick SiO_2 liner and 100 S/m Si conductivity, and (iv) 0.5 µm thick SiO_2 liner and 100 S/m Si conductivity. 10 S/m and 100 S/m conductivity corresponds to 10 Ω-cm and 1 Ω-cm resistivity, respectively.

The resistance and inductance varies with frequency, as shown in Figure 12 (a) and Figure 12 (b), because of proximity and skin effects. In Figure 12 (b), L_{11} represents the self inductance of the Si TPV. Mutual inductance between the Si TPVs is represented by the terms L_{12}, L_{13}, and L_{14}. The resistance and inductance plots are independent of the SiO_2 liner thickness and the Si resistivity because these terms are dependent only on the via (conductor) geometry.

Figure 12 (c) plots the equivalent conductance ($G_0(f) + 2G(f)$) of the Si TPV. The capacitance and conductance of the vias are influenced by the SiO_2 liner thickness and Si conductivity. The conductance at high frequencies depends strongly on the Si conductivity. The via conductance increases with increase in Si conductivity. Decreasing the liner thickness increases the equivalent conductance of the via because of more Si material between the vias.

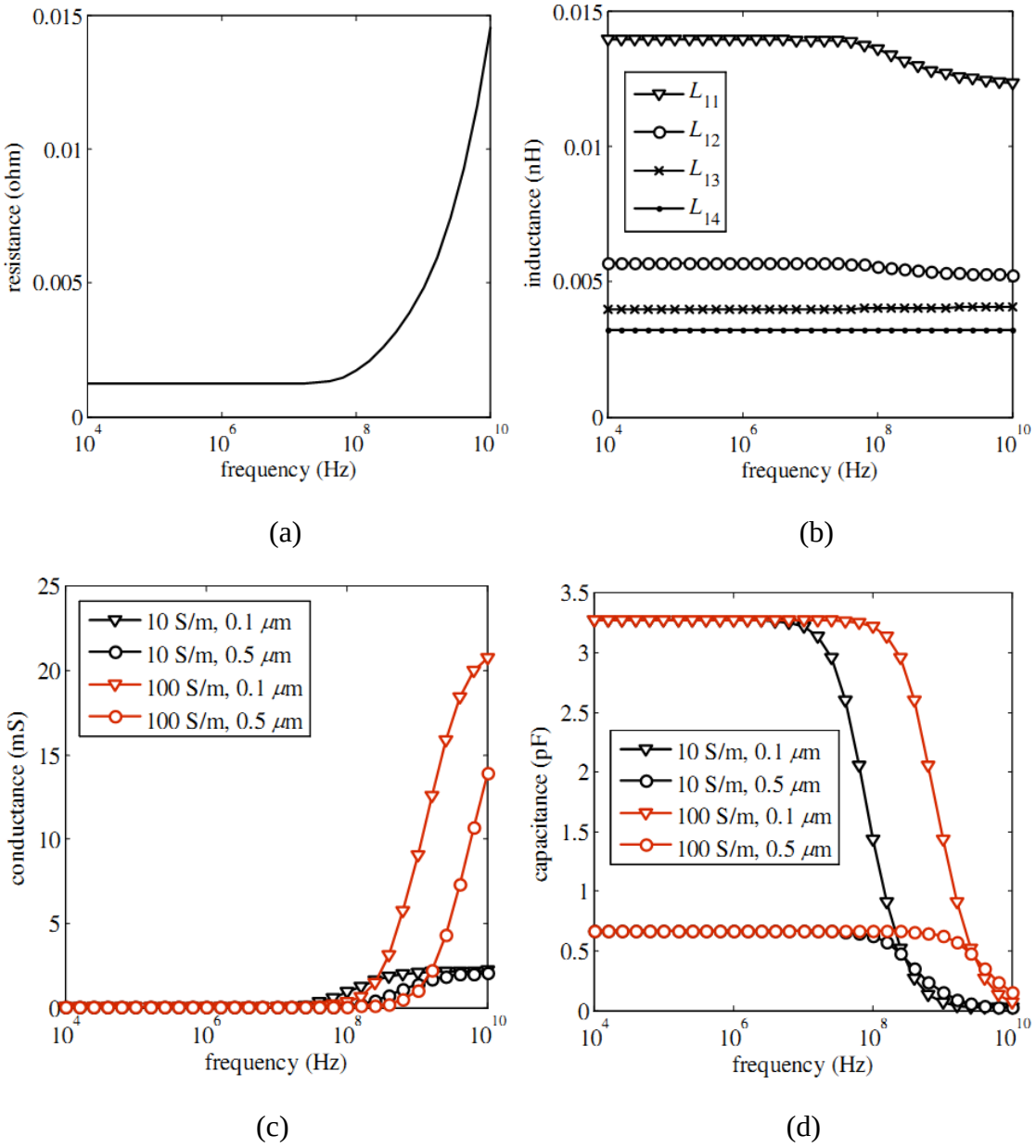
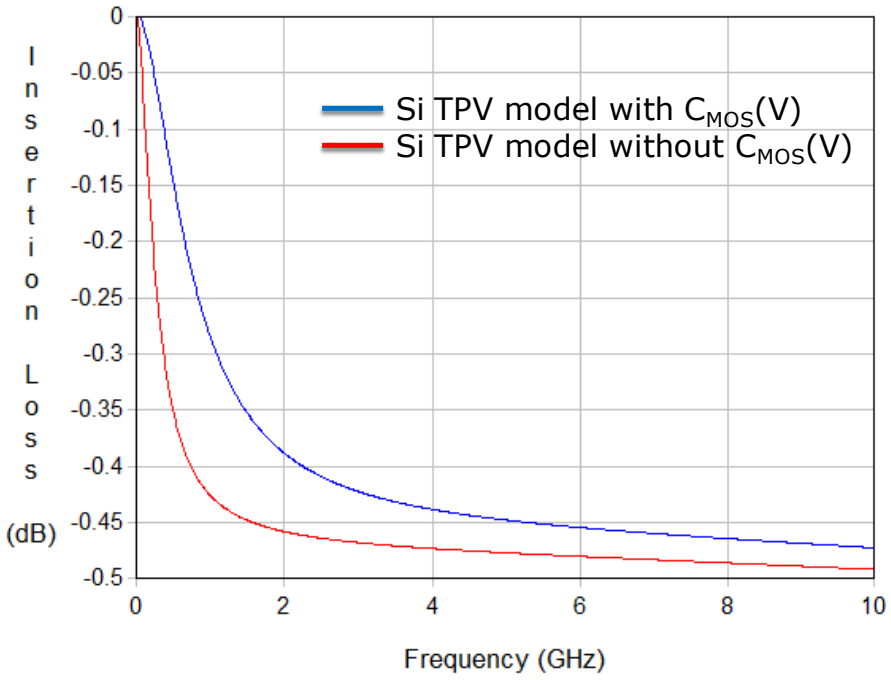


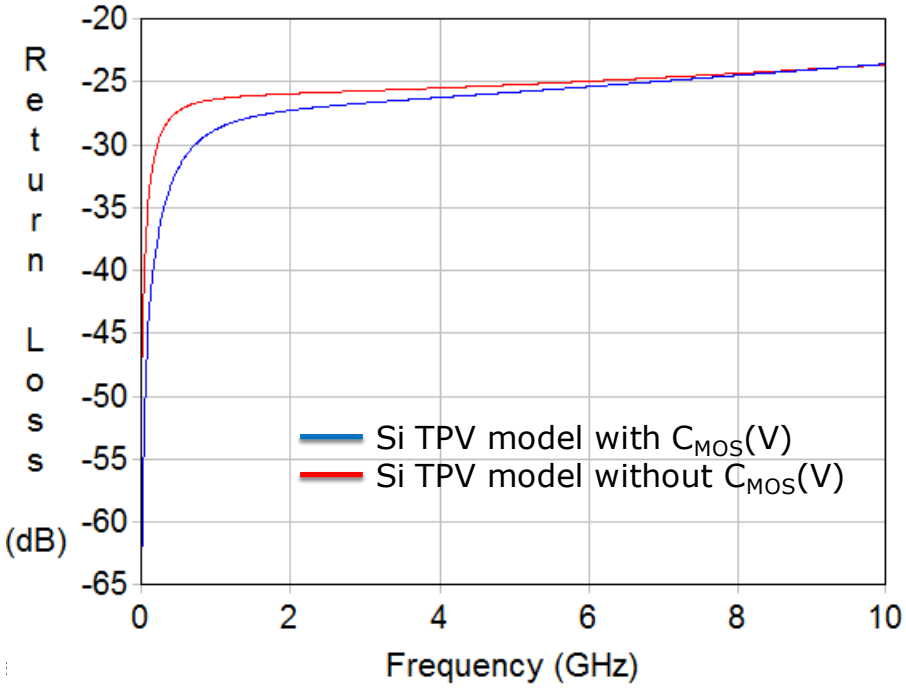
Figure 12. Parasitic elements of a pair of Si TPVs. (a) Resistance, (b) Self and mutual inductance, (c) Equivalent conductance, (d) Equivalent capacitance.

Figure 12 (d) plots the equivalent capacitance ($C_0(f) + 2C(f)$) of the Si TPV. The capacitance depends strongly on the liner thickness at low frequency and on the Si conductivity at high frequency. At low frequency, the capacitance increases with decrease in the liner thickness. At high frequency, the capacitance decreases with decrease in Si conductivity.

Figure 13 compares the s-parameters obtained from the circuit model of a pair of Si TPVs with and without the MOS capacitance element. The via diameter was 30 µm, via pitch was 60 µm, and via length was 100 µm. The Si TPV was modeled with 0.1 µm thick SiO_2 liner and 10 Ω-cm Si resistivity. It is observed that when the MOS capacitance is neglected it leads to higher insertion and return loss estimation of the Si TPVs because of overestimating the via capacitance.



(a)



(b)

Figure 13. S-parameter comparison of Si TPV model with and without MOS capacitance. (a) Insertion Loss, (b) Return Loss.

2.3 Parametric Study

The effect of different Si TPV physical parameters on its capacitance was studied based on the MOS capacitance analysis described in the previous section. This section discusses the results of these parametric studies on cylindrical Si TPVs. Similar trends were observed for annular [51] and co-axial Si TPVs as well. The different Si TPV parameters that were studied are (i) Si TPV diameter, (ii) Si TPV liner thickness, (iii) Si TPV liner material, (iv) Si resistivity, and (v) Si TPV metal. The Si TPV capacitance-voltage curves for high frequency operation are plotted for these comparisons. In this section, 'Bias Voltage' refers to the difference in voltage between the Si TPV and the silicon substrate.

2.3.1. Si TPV Diameter

The effect of varying the Si TPV diameter on its capacitance was studied. The Cu filled Si TPVs were modeled with 0.1 μm thick SiO_2 liner. The Si was modeled as a p-type substrate with 10 Ω-cm resistivity and biased to ground potential. Figure 14 shows the per unit length Si TPV capacitance plotted as a function of the (Si TPV to Si) bias voltage difference for different Si TPV diameters.

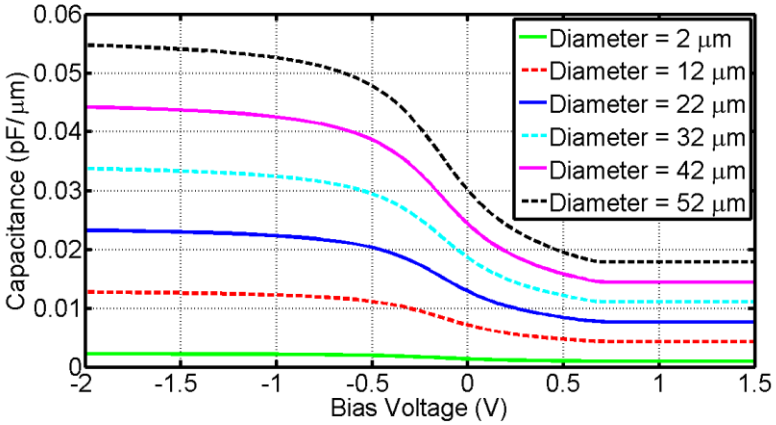


Figure 14. Per unit length Si TPV capacitance-voltage plots for different Si TPV diameters.

It is observed from Figure 14 that the Si TPV capacitance decreases with decrease in the Si TPV diameter. Further, the difference between the Si TPV capacitance in the accumulation and inversion regions decrease with decrease in the Si TPV diameter.

The Si TPV capacitance is a series combination of the liner capacitance and the depletion capacitance. In the accumulation region, the Si TPV capacitance is very close to the oxide capacitance value. The Si TPV capacitance in the depletion and inversion region is influenced by the depletion capacitance. As compared to the depletion capacitance, the liner capacitance reduces faster with reduction in the Si TPV diameter because the liner thickness was considered to be constant. This results in smaller difference in Si TPV capacitance between accumulation and inversion regions with decrease in Si TPV diameter.

In other words, a Si TPV with a smaller liner thickness to Si TPV diameter ratio leads to a larger difference between the Si TPV capacitance in the accumulation and inversion regions.

2.3.2. Liner Thickness

The effect of varying the Si TPV liner thickness on its capacitance was studied. The Cu-filled Si TPVs were modeled with a diameter of 15 µm and SiO_2 liner. The Si was modeled as a p-type substrate with 10 Ω-cm resistivity and biased to ground potential. Figure 15 shows the per unit length Si TPV capacitance plotted as a function of the (Si TPV to Si) bias voltage difference for different Si TPV liner thicknesses.

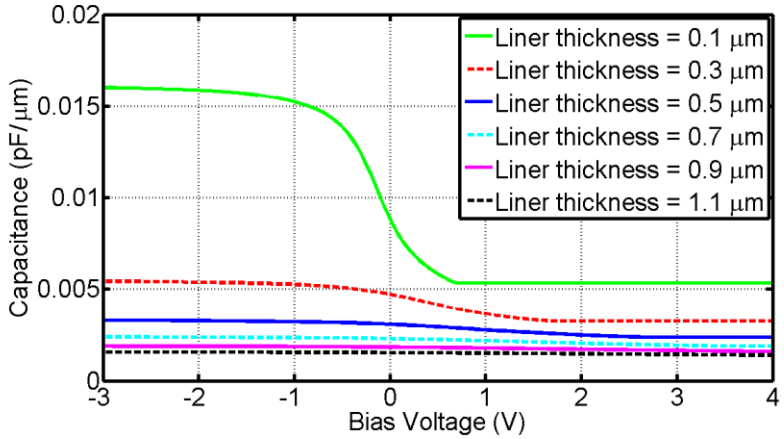


Figure 15. Per unit length Si TPV capacitance-voltage plots for different Si TPV liner thicknesses.

It is observed from Figure 15 that the Si TPV capacitance decreases with increase in the Si TPV liner thickness. Further, the difference between the Si TPV capacitance in the accumulation and inversion regions decrease rapidly with increase in the Si TPV liner thickness.

A thicker Si TPV liner reduces the liner capacitance. A thicker Si TPV liner also leads to a smaller electric field at the Si-liner interface. This creates a smaller depletion region which leads to a higher depletion capacitance. Due to these effects, the difference

between the Si TPV capacitance in the accumulation and inversion regions rapidly decrease with increase in the liner thickness. For Si TPVs with thick (> 1 μm) liner the MOS capacitance effect is negligible.

2.3.3. Liner Material

The effect of using different Si TPV liner materials on its capacitance was studied. The Cu-filled Si TPVs were modeled with a diameter of 15 μm and 0.1 μm thick liner. The Si is modeled as a p-type substrate with 10 Ω-cm resistivity and biased to ground potential. Figure 16 shows the per unit length Si TPV capacitance plotted as a function of the (Si TPV to Si) bias voltage difference for different Si TPV liner materials.

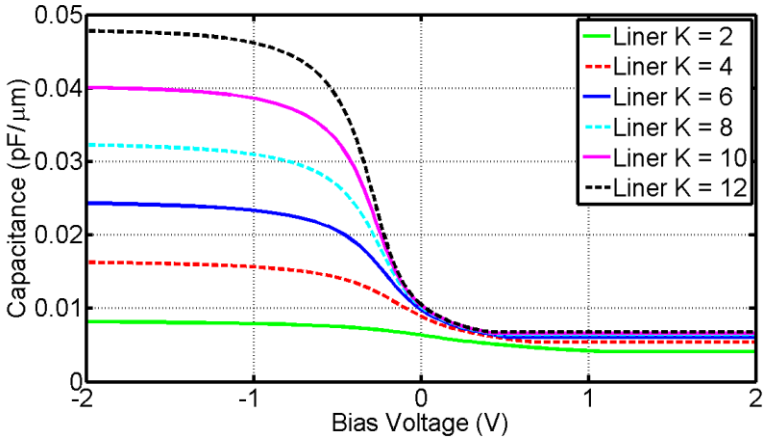


Figure 16. Per unit length Si TPV capacitance-voltage plots for different Si TPV liner materials.

It is observed from Figure 16 that the Si TPV capacitance decreases with decrease in the dielectric constant of the Si TPV liner material. Further, the difference between the Si TPV capacitance in the accumulation and inversion regions decrease with decrease in the Si TPV liner's dielectric constant.

Decreasing the dielectric constant of the Si TPV liner material decreases the liner capacitance but it has a negligible effect on the electric field in the Si-liner interface. Thus, it has a negligible effect on the depletion capacitance. Due to these reasons the Si TPV capacitance in the inversion region is almost unaffected by the change in the dielectric constant of the Si TPV liner although it drastically changes the Si TPV capacitance in accumulation.

2.3.4. Resistivity of Silicon

The effect of Si substrates with different resistivity on the Si TPV capacitance was studied. The Cu-filled Si TPVs were modeled with a diameter of 15 µm and 0.1 µm thick SiO_2 liner. The Si was modeled as a p-type substrate biased to ground potential. Figure 17 shows the per unit length Si TPV capacitance plotted as a function of the (Si TPV to Si) bias voltage difference for different Si resistivity.

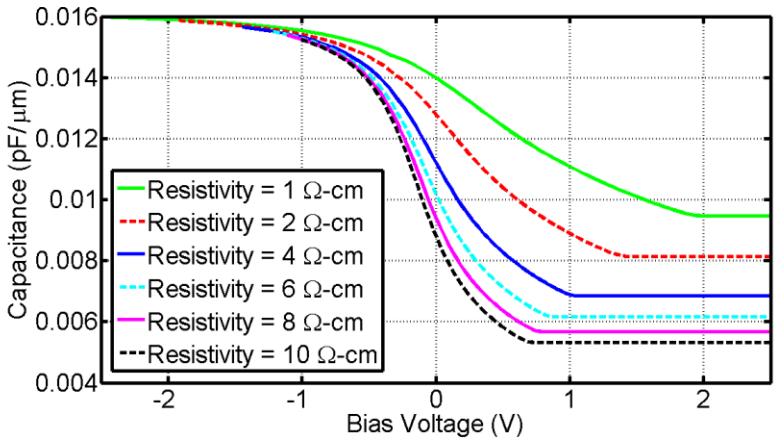


Figure 17. Per unit length Si TPV capacitance-voltage plots for different Si substrate resistivity.

It is observed from Figure 17 that the Si TPV capacitance in the depletion and inversion regions decreases with increase in the Si resistivity. The Si TPV capacitance in the accumulation region remains unaffected by the change in the Si resistivity.

The liner capacitance depends only on the liner dielectric constant, the liner thickness, and the Si TPV diameter. It is unaffected by any change in Si resistivity. Due to this reason, the Si TPV capacitance in accumulation is unaffected by change in Si resistivity. Increase in Si resistivity implies a lower doping level in the Si substrate. This leads to the formation of a wider depletion region around the Si TPV for the same voltage difference between the Si TPV and the Si. This reduces the depletion capacitance.

2.3.5. Si TPV Metal

The effect of using different metals (for filling the Si TPV) on the Si TPV capacitance was studied. The Si TPVs were modeled with a diameter of 15 μm and 0.1 μm thick SiO_2 liner. The Si was modeled as a p-type substrate with 10 Ω-cm resistivity and biased to ground potential. Figure 18 shows the per unit length Si TPV capacitance plotted as a function of the (Si TPV to Si) bias voltage difference for different Si TPV filling metals. Table 2 lists the work function values of the different metals that were considered for this parametric study.

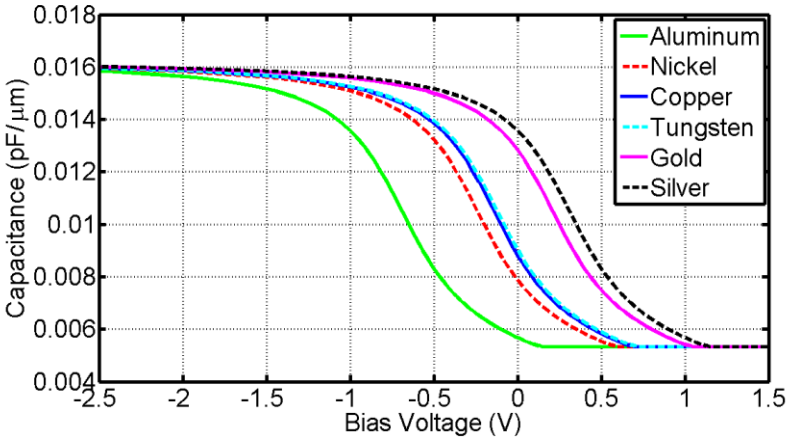


Figure 18. Per unit length Si TPV capacitance-voltage plots for different Si TPV filling metals.

Table 2: Work function of metals.

Metal	Work Function (V)
Aluminum	4.1
Nickel	4.55
Copper	4.65
Tungsten	4.67
Gold	5
Silver	5.1

It is observed from Figure 18 and Table 2 that the Si TPV capacitance-voltage curve shape remains unchanged by the change in Si TPV filling metal. Changing the Si TPV filling metal offsets the C-V curve. Lower work function metals move the curve to the left whereas higher work function metals move the curve to the right.

The liner and depletion capacitances are independent of the work function of the Si TPV metal. However, the flatband and threshold voltages are directly related with the Si TPV metal work function. Hence changing the Si TPV filling metal offsets the C-V curve without changing the capacitance values in accumulation or inversion.

2.4 Design Guidelines

Based on the results of the parametric study as described in the previous section some design guidelines for Si TPVs are proposed in this section.

2.4.1 Si TPVs in Signal Delivery Network (SDN)

In the SDN it is advantageous to have lower Si TPV parasitic capacitance to obtain a faster signal response and smaller signal distortion. To reduce the Si TPV capacitance, the Si TPV must be biased in the deep depletion region. This condition may be satisfied by applying an appropriate negative bias voltage on a p-type Si substrate or an appropriate positive bias voltage on an n-type Si substrate. Alternatively, the Si TPV can be filled with a low work function metal for p-type Si (high work function metal for n-type Si) such that it is biased in the deep depletion region by the given signal range.

The diameter of the Si TPV and the thickness of the Si substrate should be reduced to reduce the Si TPV capacitance. A thick liner should be used to reduce the liner capacitance. An appropriate liner material should be selected with a low dielectric constant for the same reason. Finally, a high resistivity Si substrate should be used to reduce the depletion capacitance.

2.4.2 Si TPVs in Power Delivery Network (PDN)

Unlike the SDN, the objective of Si TPV design in the PDN is to increase its capacitance to improve the decoupling behavior of the Si TPV. To increase the Si TPV capacitance, the Si TPV must be biased in the accumulation region. This condition may be satisfied by applying an appropriate positive bias voltage on a p-type Si substrate or an appropriate negative bias voltage on an n-type Si substrate. Alternatively, the Si TPV can be filled with a high work function metal for p-type Si (low work function metal for n-type Si) such that it is biased in the accumulation region by the given voltage on the power plane.

The diameter of the Si TPV and the thickness of the Si substrate should be increased to increase the Si TPV capacitance. A thin liner should be used to increase the liner capacitance. An appropriate liner material should be selected with a high dielectric constant for the same reason. Finally, a low resistivity Si substrate should be used to increase the depletion capacitance.

2.4.3 Si TPVs as Variable Capacitors

Si TPVs can be designed and used as variable capacitors by using the MOS capacitance effect. For an effective variable capacitor design, the range of Si TPV capacitance must be increased. The Si TPV must be operated in the depletion or deep depletion regions. This may be ensured by applying an appropriate bias voltage on the Si substrate such that the Si TPV operates in the depletion or deep depletion region for the range of voltages carried by the Si TPV. Another way to meet this objective is to use an appropriate metal for filling the Si TPV.

The difference between the accumulation and inversion capacitance must also be increased by increasing the diameter of the Si TPV. A thin layer of a high dielectric constant liner material should be used to increase the accumulation capacitance. Finally, a high resistivity Si substrate (resistivity greater than 100 Ω-cm) should be used to reduce the depletion capacitance.

2.5 Electromagnetic Simulation

2.5.1 Depletion Region Modeling

The importance of accurately modeling the depletion region in 3D electromagnetic (EM) simulations of Si TPVs is shown in this section. Cylindrical, annular, and co-axial Si TPVs were studied for their electrical signal loss characteristics by means of 3D full-wave EM simulations. CST Microwave Studio (CST MWS) [52] was used as a 3D full-wave EM simulator to study the system response up to 10 GHz. Figure 19 shows the via model simulated with two ports in CST MWS. The signal via is in the middle with a ground via on either side. The vias were excited with discrete (lumped) ports on its top and bottom surfaces.

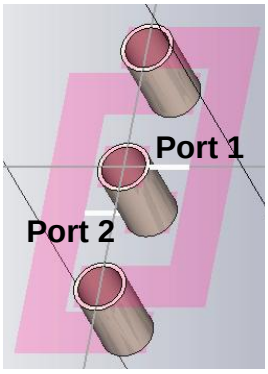


Figure 19. Two-port Si TPV model in CST Microwave Studio (CST MWS) [52].

The Si TPV length, diameter, and pitch were 100 µm, 15 µm, and 30 µm respectively. The Si TPVs were modeled with 10 ohm-cm resistivity Si substrate. The silicon substrate had 1 µm thick layer of SiO_2 on its top and bottom surfaces as shown in Figure 2.

Two Si TPV models with 0.1 µm SiO_2 liner were simulated and compared. The first Si TPV model was simulated without any depletion region in the Si substrate. In the second model, a depletion region was modeled around the Si TPVs. The thickness of the depletion region was determined analytically (using the analysis presented in Section 2.2.2). The depletion region in the Si substrate was modeled as loss-free Si in CST MWS because it is mostly devoid of any mobile charge carriers. Both the models were simulated and the results are presented in Figure 20, Figure 21, and Figure 22.

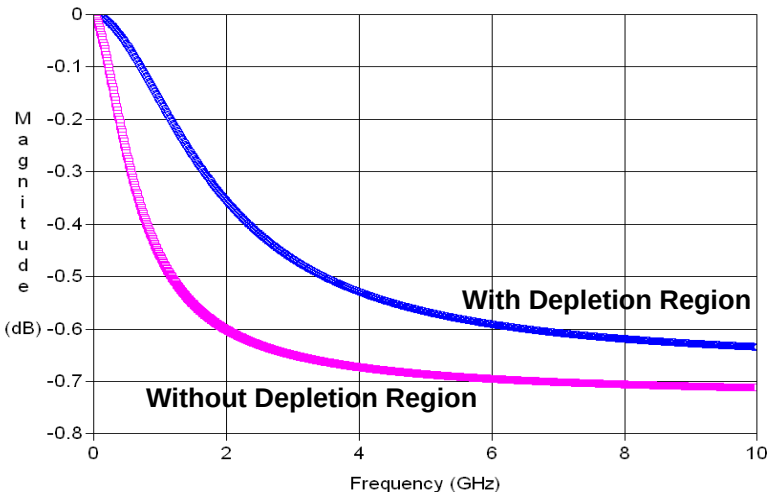


Figure 20. Simulation results (Insertion loss) obtained from CST MWS for Si TPVs with and without depletion region.

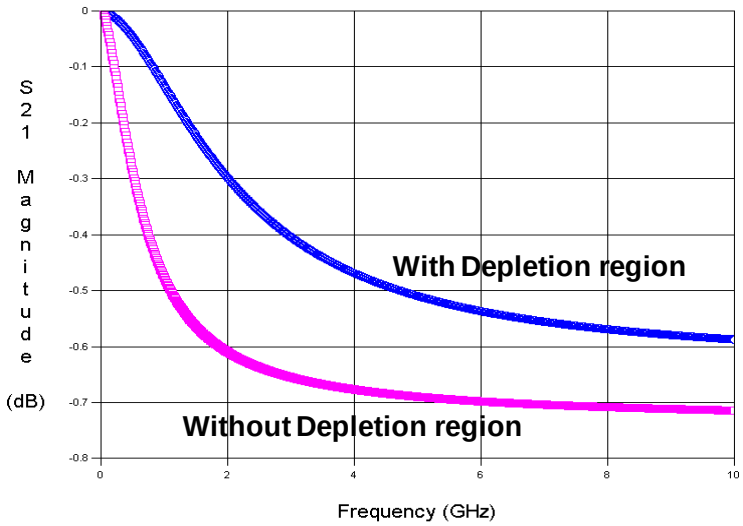


Figure 21. Insertion loss comparison of annular Si TPVs. The outer and inner diameter of the annular Si TPVs are 15 µm and 5 µm respectively while the via pitch is 30 µm.

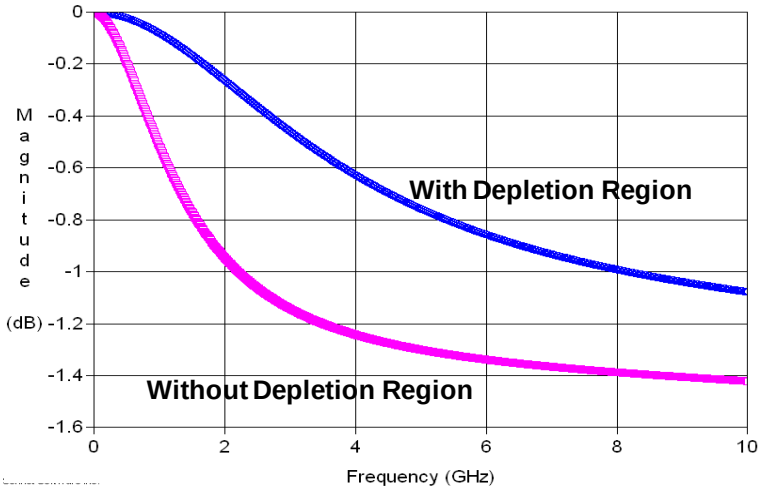


Figure 22. Insertion loss comparison of co-axial Si TPVs. The co-axial Si TPV had a core diameter of 15 µm. The inner and outer diameter of the Si TPV shell was 30 µm and 40 µm respectively.

It is observed from Figure 20, Figure 21, and Figure 22 that neglecting the depletion region while simulating the Si TPVs resulted in a difference of 0.08 to 0.3 dB (cylindrical Si TPV), 0.1 to 0.3 dB (annular Si TPV), and 0.3 to 0.6 dB (co-axial Si TPV) in the insertion loss plot up to 10 GHz. The depletion region is mostly devoid of any mobile charge carriers and thus, acts as a region of very high resistivity Si. The change in the Si resistivity around the Si TPV results in this difference in the insertion loss plot. This difference in the insertion loss will be more pronounced for signal paths passing through multiple Si TPVs (for example, communication between chips in a multi-layered chip stack and/or between chips on a Si interposer).

Co-axial Si TPVs can be designed using the low loss depleted Si region. In ICs, co-axial Si TPV can be designed such that the Si (between the core and shell) is completely depleted by the signal voltage on the Si TPV. In Si interposers, a negative bias (positive bias for n-type Si) can be applied on the Si substrate to completely deplete the Si between the core and shell. The result of such a design is showed in Figure 23. It compares two co-axial Si TPVs with identical dimensions – one with completely depleted Si and, the other with the Si only partially depleted. The Si TPV had 3 µm core diameter, 9 µm inner shell diameter, and 15 µm outer shell diameter.

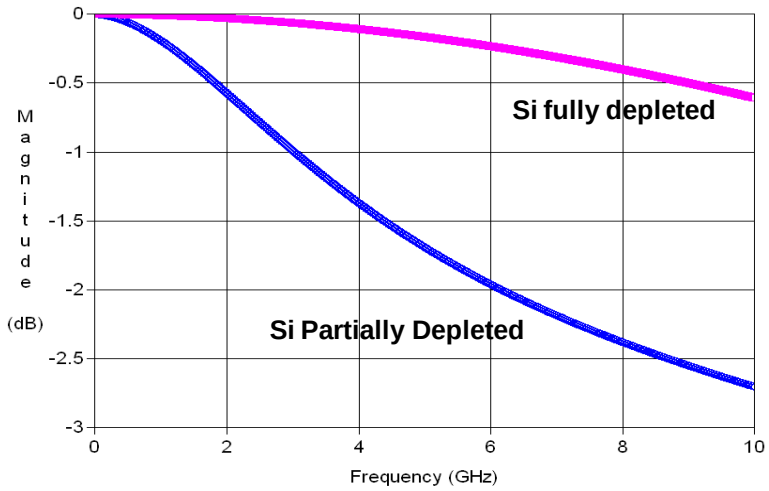


Figure 23. Insertion loss comparison of co-axial Si TPVs with the Si (between core and shell) either completely or partially depleted.

It is seen that completely depleting the Si reduces the signal loss by more than 0.2 dB. This effect is significant for signal paths through multiple Si TPVs (e.g., in 3D stacks with multiple chips).

2.5.2 TPVs in Wafer-Si and Panel-Si Interposers

In this section, electromagnetic modeling and simulation results are presented to compare the electrical performance of TPVs in panel-silicon and wafer-silicon interposers. The TPV model is shown in Figure 24. The model comprises of two signal vias (marked as ‘S’ in Figure 24) surrounded by four ground vias (marked as ‘G’ in Figure 24). The vias were excited with discrete (lumped) ports on their top and bottom surfaces.

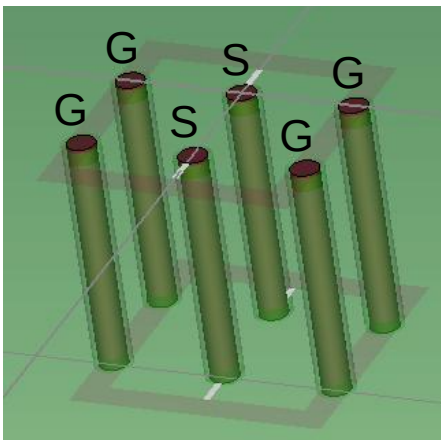


Figure 24. Si TPV model in CST Microwave Studio for loss and crosstalk studies.

The insertion loss and crosstalk between the vias in two types of Si interposers is compared in Figure 25 and Figure 26, respectively. The TPVs in polycrystalline panel-Si (0.15 Ω-cm resistivity) are compared with TPVs in wafer based CMOS grade Si (10 Ω-cm resistivity). The thickness of the Si substrate was 220 µm. The diameter and pitch of these Cu-filled vias were 30 µm and 120 µm, respectively. The TPVs in wafer-Si interposer were modeled with 1 µm thick sidewall SiO_2 liner, while the TPVs in panel-Si interposer were modeled with 5 µm thick sidewall polymer liner.

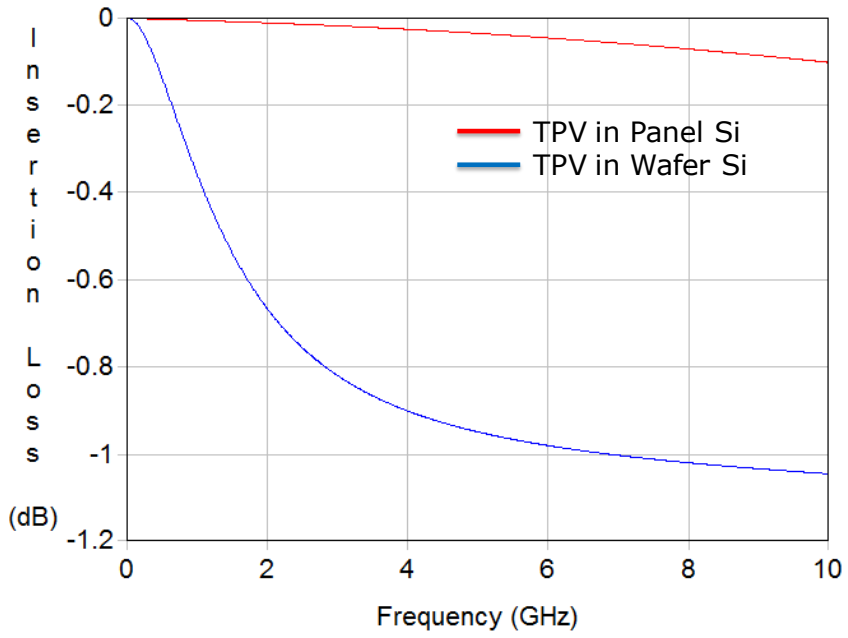


Figure 25. Insertion loss comparison between TPVs in panel-Si and wafer-Si interposers.

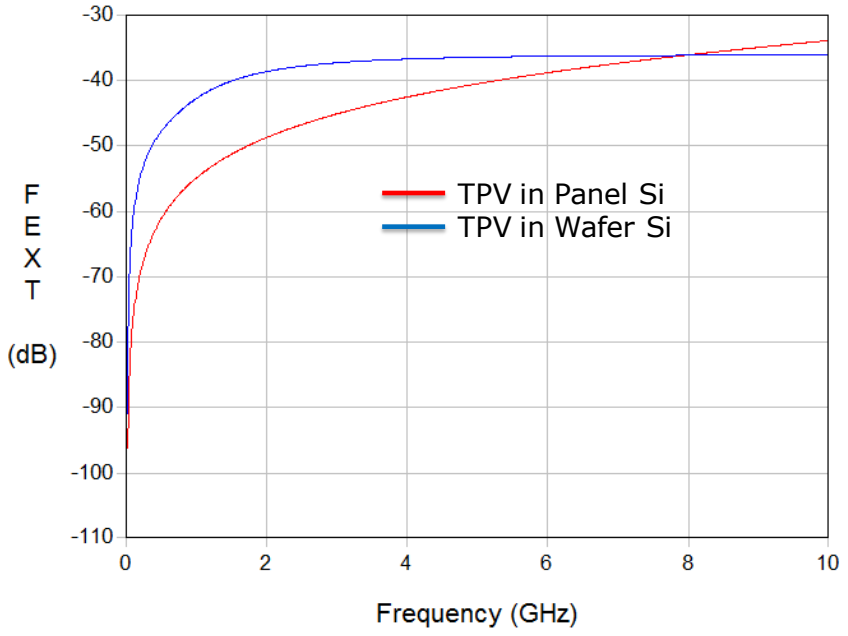


Figure 26. Far-end crosstalk comparison between TPVs in panel-Si and wafer-Si interposers.

It is observed that the TPVs in panel-Si interposer have lower loss (till 10 GHz) and crosstalk (till 8 GHz) as compared to the TPVs in wafer-Si interposer. The better electrical behavior of the TPVs can be attributed to the thicker sidewall and surface liner in these interposers. This helps reduce the substrate loss and coupling in the Si substrate.

The equivalent conductance of a Si TPV increases with increase in frequency as shown in Figure 12 (c). Beyond 8 GHz, the higher conductance of the TPV in panel-Si (high conductivity Si) as compared to that in wafer-Si (low conductivity Si) offsets the reduced crosstalk between panel-Si TPVs due to thick side-wall liner. Designing a TPV with thicker liner in panel-Si interposer will increase the frequency at which the crosstalk between the vias in panel-Si interposer become same as that in wafer-Si interposer.

2.5.3 Effect of TPV Liner Thickness

The effect of the sidewall liner thickness on the insertion loss and crosstalk in TPVs is studied in Figure 27 and Figure 28, respectively. The TPV diameter and pitch was 30 μm (diameter of the Cu filled region) and 120 μm respectively. The Si substrate resistivity and thickness was 0.15 Ω-cm and 220 μm respectively. It is seen that the insertion loss and crosstalk can be reduced by using a thicker sidewall liner.

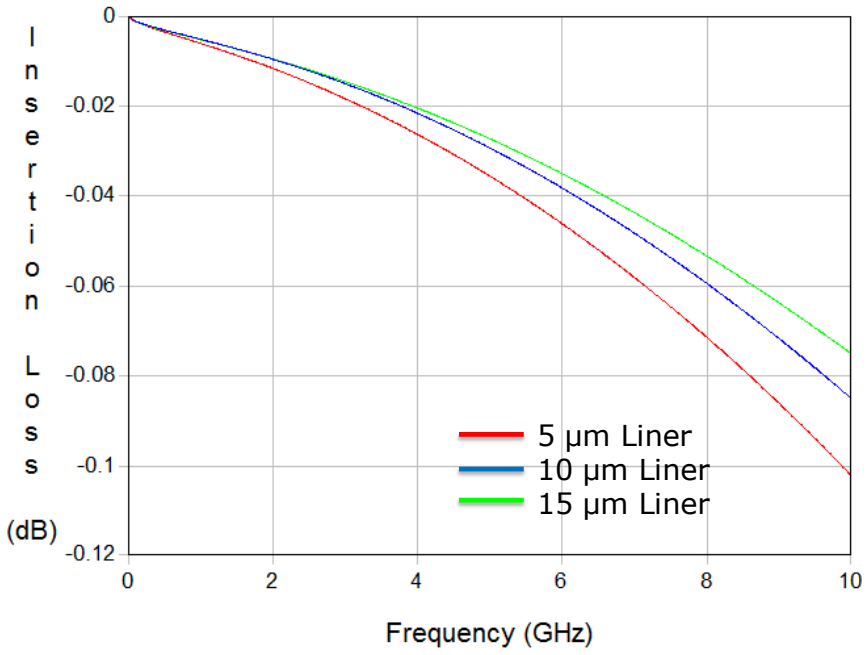


Figure 27. Insertion loss plots for TPVs with different liner thicknesses in panel-Si interposer.

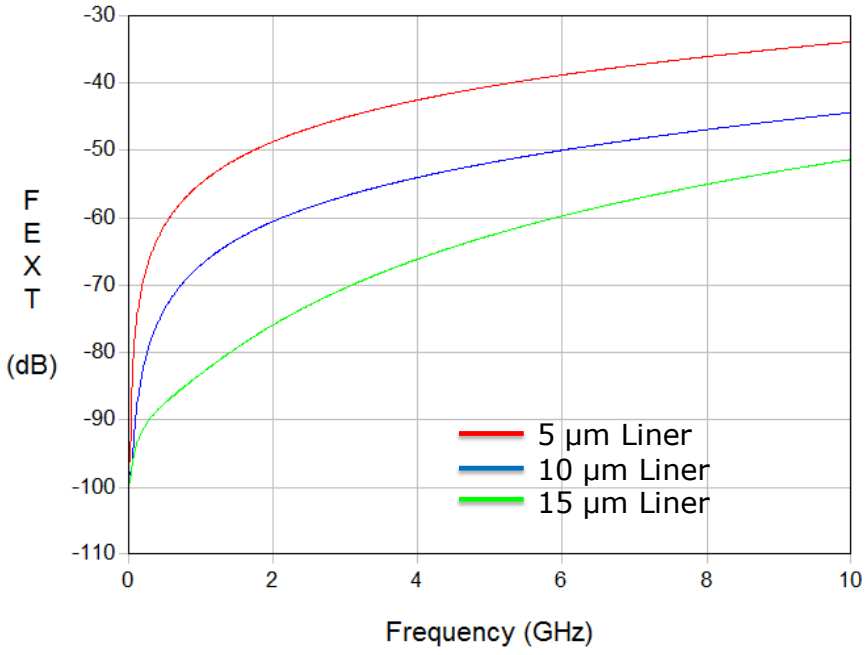


Figure 28. Far-end crosstalk plots for TPVs with different liner thicknesses in panel-Si interposer.

2.5.4 Effect of TPV Diameter

The effect of TPV diameter on its loss and crosstalk is studied in Figure 29 and Figure 30, respectively. The vias were modeled in 220 µm thick panel-Si (0.15 Ω-cm resistivity) with 5 µm thick polymer sidewall liner. The TPV pitch was 120 µm.

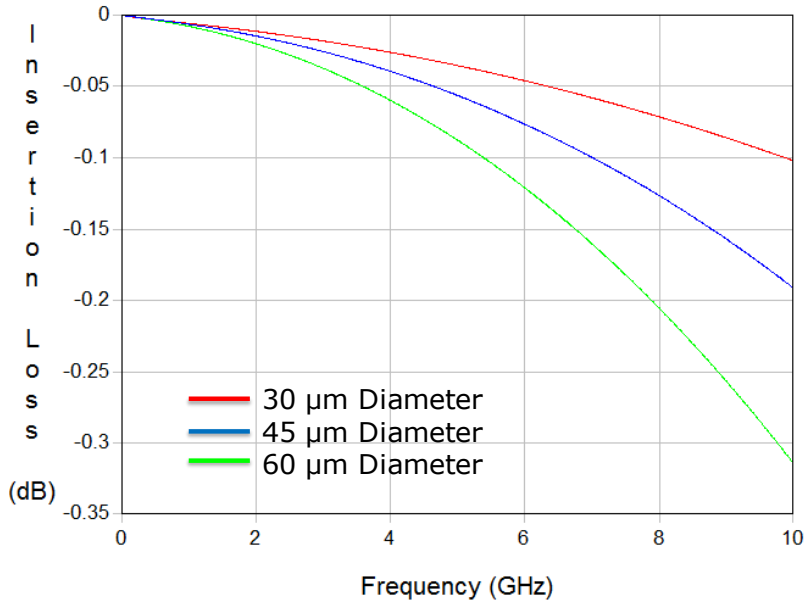


Figure 29. Insertion loss plots for TPVs with different diameters in panel-Si interposer.

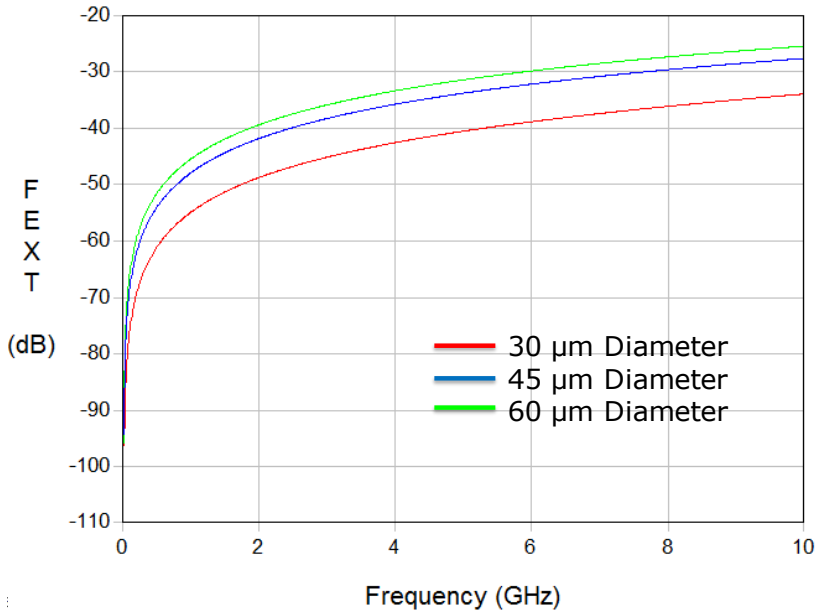


Figure 30. Far-end crosstalk plots for TPVs with different diameters in panel-Si interposer.

The loss in Si TPVs decreases with decrease in its diameter. Smaller Si TPVs have smaller sidewall capacitance (due to smaller diameter) and smaller substrate conductance (due to larger spacing between the TPVs). This helps in reducing the loss. Due to the greater spacing between the smaller TPVs, their crosstalk is lower as compared to the larger TPVs.

2.5.5 Microstrip Line to Si TPV Transition

This section presents modeling and simulation of Si TPVs connected with re-distribution layer (RDL) wiring on the silicon interposer. The RDL wiring was modeled as microstrip lines (MSL) on the top and bottom surfaces of the silicon interposer. These lines were connected by Si TPVs as shown in Figure 31. The MSLs on the top surface of the silicon interposer were excited in CST MWS by discrete (lumped) ports with respect to the ground (top) plane.

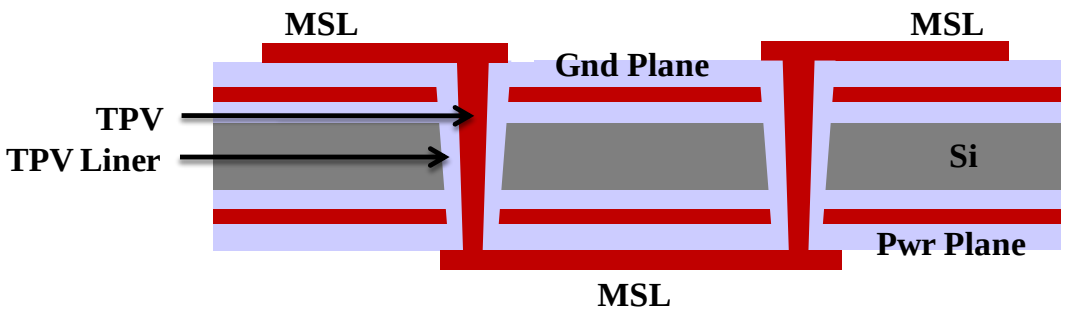


Figure 31. Schematic diagram of microstrip line (MSL) to TPV transitions in a four-metal-layer silicon interposer.

The TPVs were 30 µm in diameter. The Si core was 260 µm thick. The MSLs, TPVs, and the planes were made of copper. Three types of silicon interposers were modeled: (i) Panel-Si interposer with 25 µm thick via liner, (ii) Panel-Si interposer with 5 µm thick via liner, and (iii) Wafer-Si interposer with 2 µm thick via liner.

In panel-Si interposers, ZIF polymer (10 µm thick) was used for laminating the silicon surface (between the silicon core and the metal plane), as a build-up dielectric layer (between the metal plane and the MSL), and as the via liner. Each of the microstrip lines were 15 µm wide and 2 mm long. The panel-Si had a resistivity of 0.15 Ω-cm.

In wafer-Si interposers, SiO_2 (2 µm thick) was used as RDL build-up dielectric (between the silicon core and the metal plane, and between the metal plane and the MSL). Each of the microstrip lines were 3.5 µm wide and 2 mm long. The via liner was made of 2 µm thick SiO_2. The resistivity of the wafer-Si was 10 Ω-cm.

Figure 32 shows the insertion loss comparison of the signal path (as shown in Figure 31) in different silicon interposers. It is observed that the panel-Si interposer with thicker via liner has lower loss. As the thickness of the via liner is increased, it decreases

the substrate loss in Si, thus decreasing the total loss in the signal path. The glitch (below 5 GHz) in the insertion loss plot for the panel-Si interposers occur due to power-ground plane resonances.

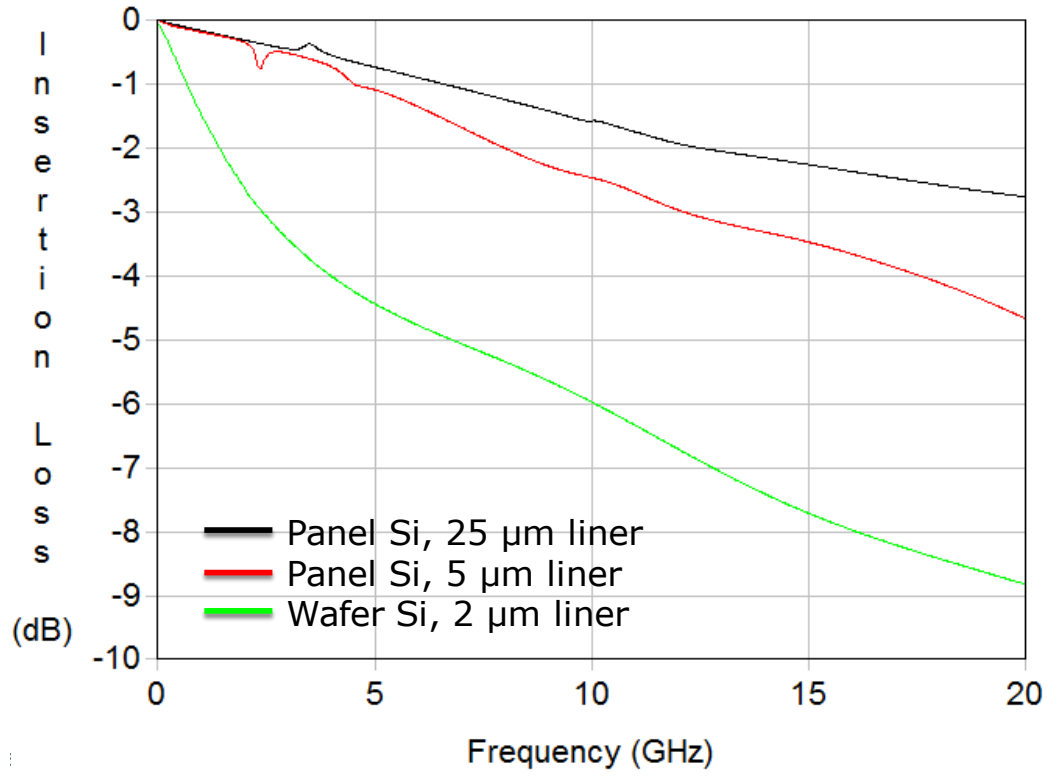


Figure 32. Insertion loss plots of MSL-TPV transitions in different silicon interposers.

It is observed that the loss of the panel-Si interposers is less than that of the wafer-Si interposer. The wafer-Si interposer has higher loss because of higher substrate loss (caused by the thinner via liner) and higher conductor loss in the MSL (caused by the smaller line width) as compared to the panel-Si interposer. From a cost and practicality point of view, the BEOL processing technique used in wafer-Si interposers limits the SiO_2 thickness (in the build-up layer and the via liner) to, typically, less than 2 µm. The smaller build-up layer thickness leads to smaller line width for a 50 Ω MSL.

All the three insertion loss plots have a smooth characteristic because the power plane resonances are suppressed in Si interposers.

2.6 Conclusion

Modeling the voltage-dependent MOS capacitance effect is important for accurate electrical modeling of Si TPV. The MOS capacitance is accurately modeled by numerically solving Poisson's equation in cylindrical co-ordinates. Parametric studies demonstrate that the Si TPV capacitance can be tuned by varying different physical and material parameters. The parametric results help in developing design guidelines for Si TPVs in 3D systems. Si TPVs can be used as a useful variable capacitor in 3D system design by using the MOS capacitance effect. Low-loss Si TPVs can be designed by using the concept of depleting the Si to reduce the dielectric loss. Si TPVs can be utilized as decoupling capacitors in 3D power-delivery networks by biasing the silicon substrate.

The performance of TPVs in panel based polycrystalline Si (with thick polymer liner) is better as compared to that of wafer based CMOS grade Si (with thin SiO_2 liner). The electrical performance of the Si TPVs can be improved by decreasing its diameter and by increasing the sidewall liner thickness.

Power-ground plane resonances are suppressed in Si interposers because of high substrate conductivity. This causes a mostly smooth insertion loss curve for signal paths passing through microstrip lines and TPVs. A high-speed digital signal propagating through such paths is expected to have smaller distortion and jitter.

CHAPTER 3

TPV IN GLASS INTERPOSER

Glass interposers are a potential low-cost, low-loss alternative to silicon interposers. This chapter presents the electrical modeling, design, and simulation of TPVs in glass interposers (Glass TPVs). Glass TPVs are compared with TPVs in silicon interposers (Si TPVs) for loss and crosstalk analysis. The glass TPV parasitics (resistance and inductance) are extracted from electromagnetic (EM) simulations. The effect of via diameter on its parasitics, loss, and crosstalk are studied. Transition model of co-planar waveguide (CPW) line to glass TPV to CPW line are modeled and simulated to study the effect of via diameter and line width on signal loss.

3.1 Electromagnetic Modeling and Simulation

TPVs were modeled and simulated by means of 3D full-wave electromagnetic (EM) simulations. CST Microwave Studio (CST MWS) [52] was used as a 3D full-wave EM simulator to study the system response of these vias up to 10 GHz. Borosilicate glass (BSG) with 200 µm thickness was modeled as the substrate, with 20 µm thick organic dielectric liner on its top and bottom surfaces. The TPV pitch was 250 µm and its diameter was 35 µm. Figure 33 shows the TPV model simulated with four ports in CST MWS. There are two signal vias (marked as ‘S’) which are surrounded by four ground vias (marked as ‘G’). The vias were excited with discrete (lumped) ports on their top and bottom surfaces.

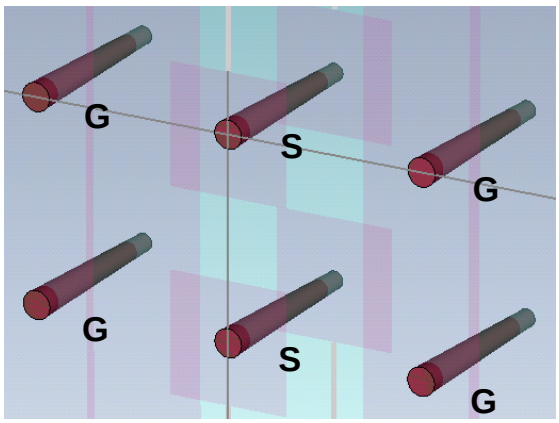


Figure 33. Glass TPV model in CST Microwave Studio for loss and crosstalk studies.

The model for the Si TPVs was also similar (same via diameter and pitch), as shown in Figure 24. The substrate material was changed from glass to silicon. In addition, the Si TPVs were modeled with a side-wall liner (which acts as an insulation layer). The TPV side-wall liner and the surface liner (on the top and bottom surfaces of the Si substrate) was the same material used in the glass TPV model.

3.1.1 TPVs in Glass and Silicon Interposers

Figure 34, Figure 35, and Figure 36 compares the insertion loss, near-end crosstalk, and far-end crosstalk of TPVs in different interposers respectively. The glass interposer is compared with high resistivity, and low resistivity silicon interposers. The effect of TPV side-wall liner thickness on the loss and crosstalk is also studied in these figures.

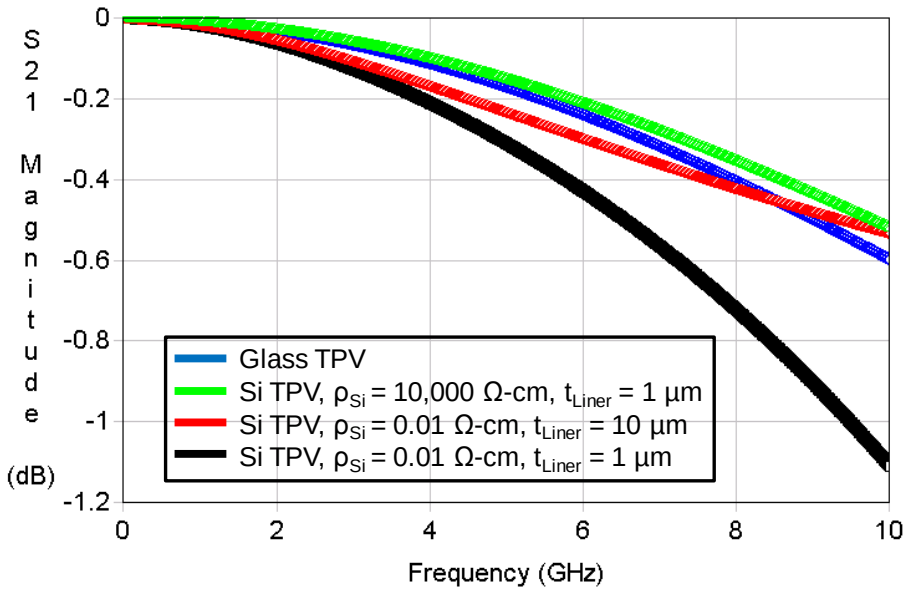


Figure 34. Insertion loss comparison between TPVs in glass and silicon interposers.

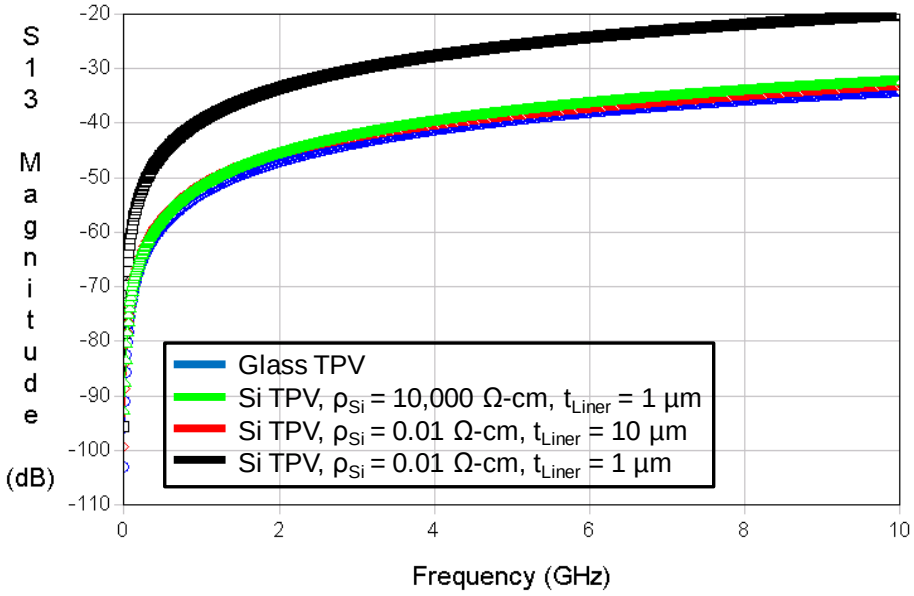


Figure 35. Near-end crosstalk comparison between TPVs in glass and silicon interposers.

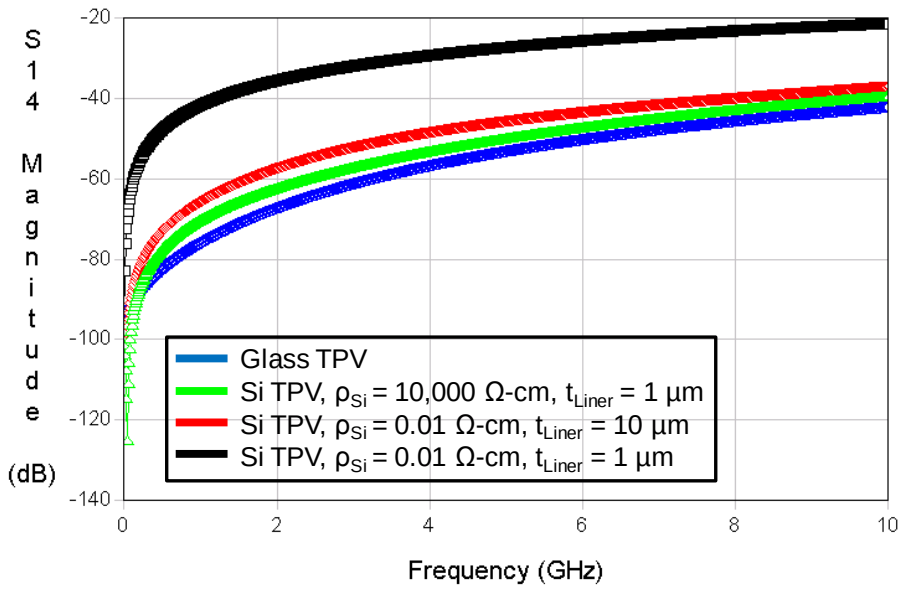


Figure 36. Far-end crosstalk comparison between TPVs in glass and silicon interposers.

From Figure 34, Figure 35, and Figure 36, it is observed that TPVs in low resistivity silicon interposer with a thin liner have much higher loss and crosstalk as compared with glass TPVs. This is primarily because of higher coupling and substrate loss in the low resistivity semiconducting silicon substrate. Glass, on the other hand, has very good insulating properties. This leads to lower loss and crosstalk in glass TPVs. The loss and crosstalk in silicon interposers can be reduced by using a thick side-wall liner in the TPV structures. The liner material has low loss. A thicker liner reduces the field penetration in the lossy silicon substrate, thereby reducing signal loss. The liner also reduces the substrate conductance between adjacent signal vias. This helps reduce the crosstalk.

The loss and crosstalk in Si TPVs can also be reduced by using a high resistivity silicon substrate as the interposer material. High resistivity silicon has lower doping concentrations and substrate loss as compared to low resistivity silicon.

3.1.2 Effect of TPV Diameter

The effect of the glass TPV diameter on the signal loss and crosstalk is studied in this section. The diameter of the glass TPV (as shown in Figure 33) was varied from 35 µm to 150 µm. Figure 37, and Figure 38 shows the insertion loss and far-end crosstalk variations in the TPVs as the diameter is varied. It is observed that the insertion loss varies inversely with the glass TPV diameter. The resistance and inductance of TPV decreases with increase in its diameter. This results in lower loss for the larger TPVs.

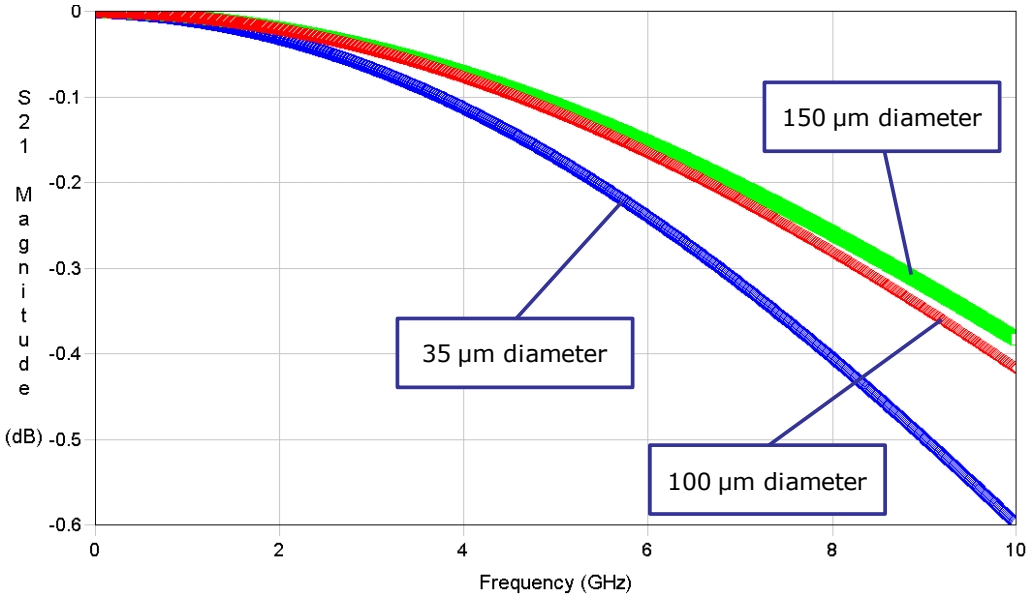


Figure 37. Insertion loss plots for glass TPVs of different diameters.

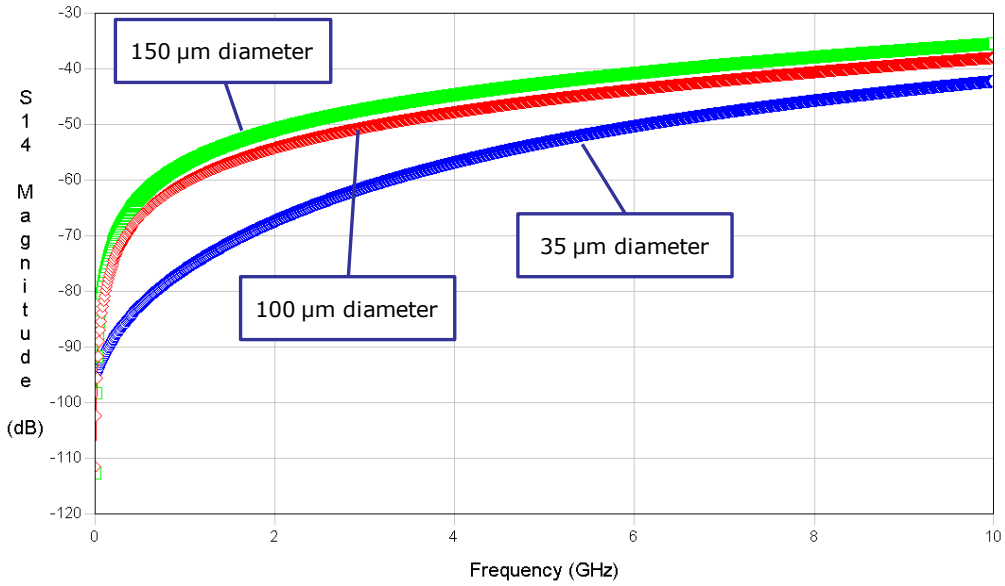


Figure 38. Far-end crosstalk plots for glass TPVs of different diameters.

In this study, the TPV pitch was kept constant while the TPV diameter was varied. Therefore, the spacing between the TPVs is larger for the design with smaller TPV diameter. This increased spacing between the smaller TPVs results in the reduced crosstalk as observed in Figure 38.

3.1.3 Effect of Glass and Polymer Choice

This section presents the effect of different glass and polymer materials on the insertion loss of the TPV. The conceptual TPV model is shown in Figure 33. The TPVs were 30 µm in diameter and 60 µm in pitch. The TPVs were modeled as completely filled with copper. Four types of glass interposers were simulated: (i) 180 µm thick ENA1 glass laminated with 20 µm thick RXP4 polymer, (ii) 180 µm thick ENA1 glass laminated with 17.5 µm thick ZIF polymer, (iii) 180 µm thick AS01 glass laminated with 20 µm thick RXP4 polymer, and (iv) 180 µm thick AS01 glass laminated with 17.5 µm thick ZIF polymer.

Figure 39 shows the insertion loss comparison for the TPVs in different glass and liner material combinations. It is seen that changing the glass or liner material has little effect on the TPV loss.

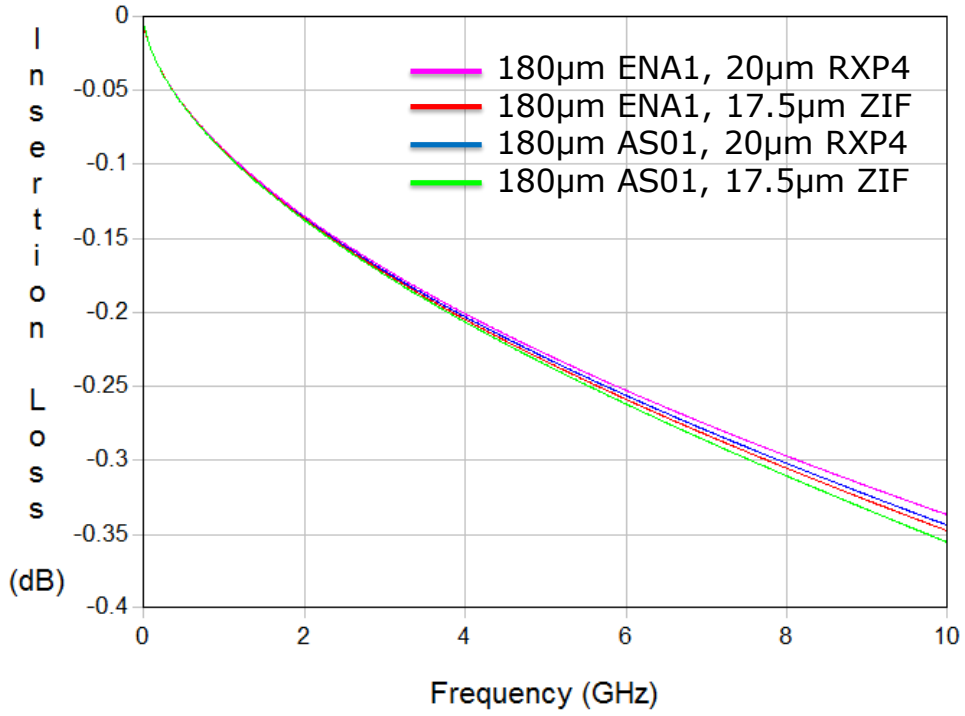


Figure 39. Insertion loss plots of TPVs in different glass interposers.

3.1.4 CPW Line to Glass TPV Transition

This section presents modeling and simulation of glass TPVs connected with re-distribution layer (RDL) wiring on the glass interposer. The RDL wiring was modeled as co-planar waveguide (CPW) lines on the top and bottom surfaces of the glass interposer. These lines were connected by glass TPVs as shown in Figure 40.

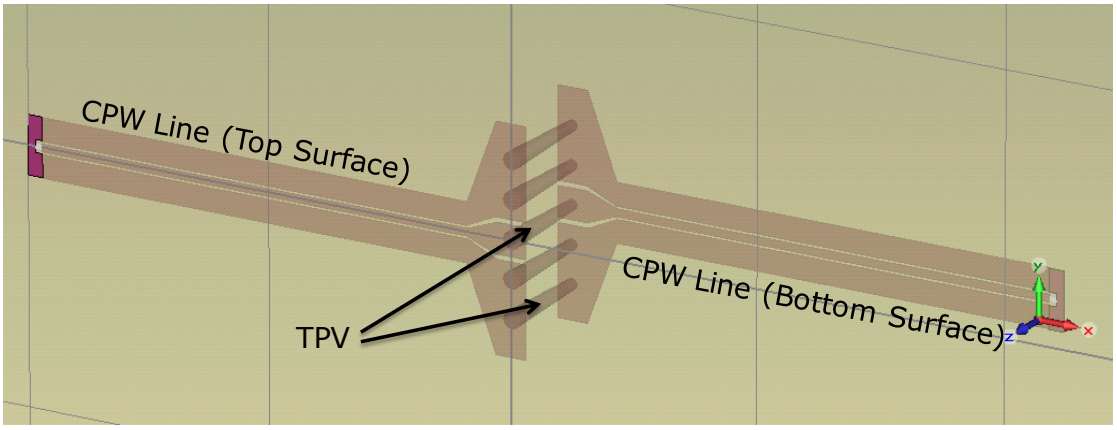
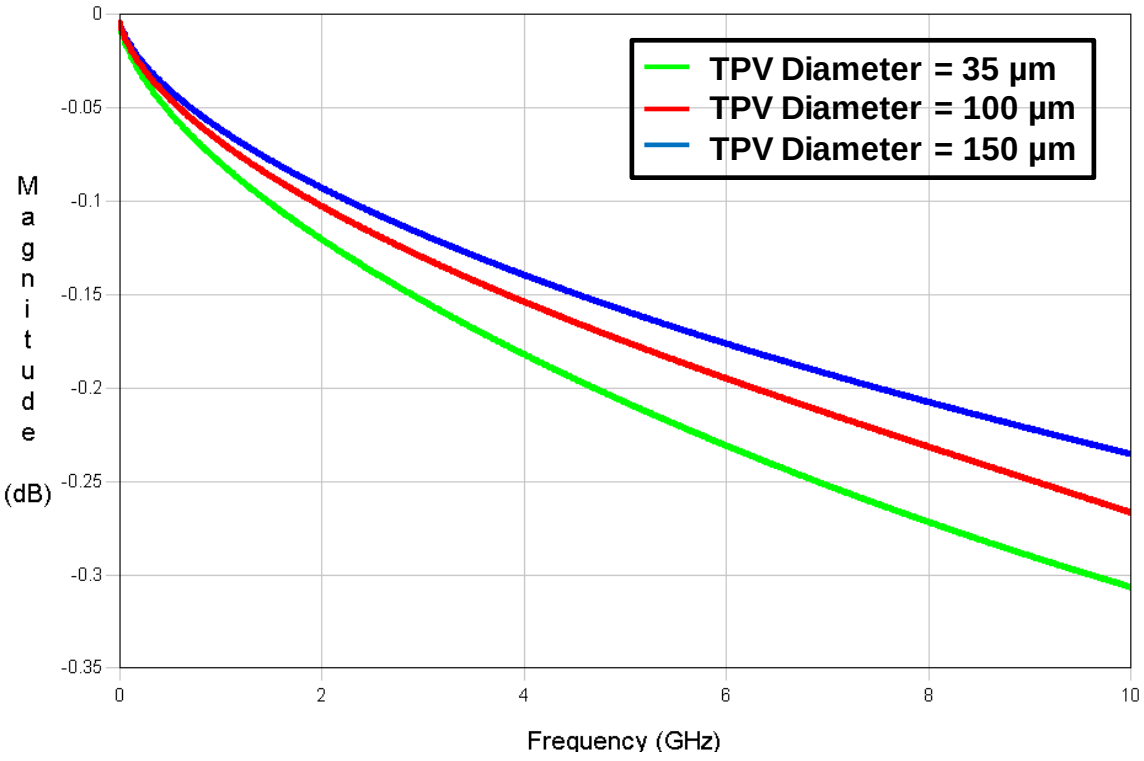
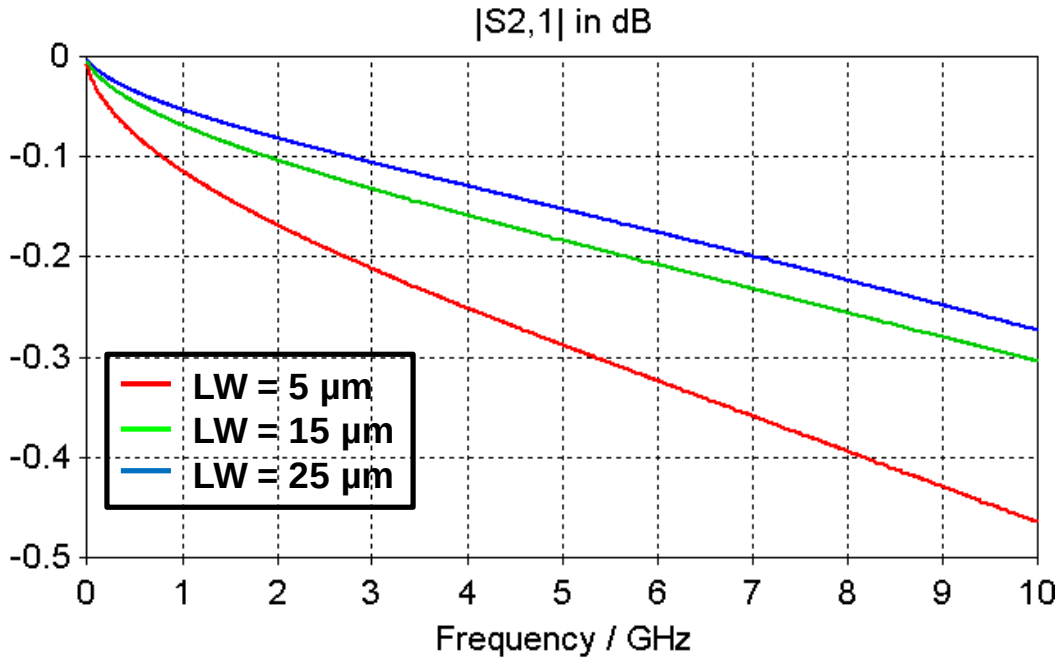


Figure 40. Model of co-planar waveguide (CPW) line to TPV to CPW line transition in CST Microwave Studio.

This model was excited by discrete (lumped) ports at the far ends of the CPW lines. The effect of varying the TPV diameter on the insertion loss is shown in Figure 41 (a). The CPW line width was fixed at 15 µm in this study. Reducing the TPV diameter increases the TPV resistance and inductance which results in higher insertion loss as seen in Figure 41 (a). Figure 41 (b) shows the effect of changing the CPW line width on the insertion loss. The TPV diameter was fixed at 35 µm in this study. The size of the TPV pad was 55 µm. As the CPW line width is reduced, the dimension mismatch between the line and the via pad increases. This results in increased losses at the line to via pad transition. The conductor loss also increases with decrease in line width. Due to these reasons, the insertion loss is higher for smaller line widths as seen in Figure 41 (b).



(a)



(b)

Figure 41. Insertion loss plots for CPW line to TPV to CPW line transition in glass interposers. (a) Effect of TPV diameter, (b) Effect of CPW line width (LW).

3.1.5 Microstrip Line to Glass TPV Transition

This section presents modeling and simulation of glass TPVs connected with re-distribution layer (RDL) wiring on the glass interposer. The RDL wiring was modeled as microstrip lines (MSL) on the top and bottom surfaces of the glass interposer. These lines were connected by glass TPVs as shown in Figure 42. The MSLs on the top surface of the glass interposer were excited in CST MWS by discrete (lumped) ports with respect to the ground (top) plane.

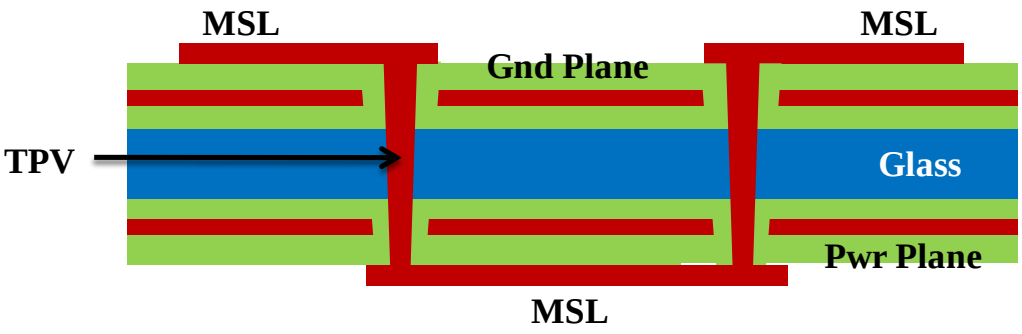


Figure 42. Schematic diagram of microstrip line (MSL) to TPV transitions in a four-metal-layer glass interposer.

Three types of glass interposers were modeled: (i) 180 µm thick AS01 glass, (ii) 180 µm thick ENA1 glass, and (iii) 75 µm thick O211 glass. ZIF polymer (10 µm thick) was used for laminating the glass surface (between the glass core and the metal plane), and also as a build-up layer (between the metal plane and the MSL). Every microstrip lines was 15 µm wide and 2 mm long. The TPVs were 30 µm in diameter. The MSLs, TPVs, and the planes were made of copper.

Figure 43 shows the insertion loss comparison of the signal path (shown in Figure 42) in different glass interposers. It is observed that all three types of glass interposers have several notches in their insertion loss plot. The notches occur due to power-ground plane resonances. The O211 glass interposer has the smallest notches. It has the smallest thickness which leads to increased capacitance and lower PDN impedance between the power and ground planes. The notches in the ENA1 glass interposer are the largest. The higher thickness (as compared to O211 glass) and lower permittivity (as compared to AS01 glass) of ENA1 glass leads to higher PDN impedance in ENA1 glass interposer.

The notches cause distortion and jitter in high-speed digital signals. The sharp notches in the insertion loss of the signal path lead to worsening of the signal eye diagram as shown and explained in [53]. Careful power delivery design in glass interposers using appropriate choice and location of decoupling capacitors will help in solving these issues.

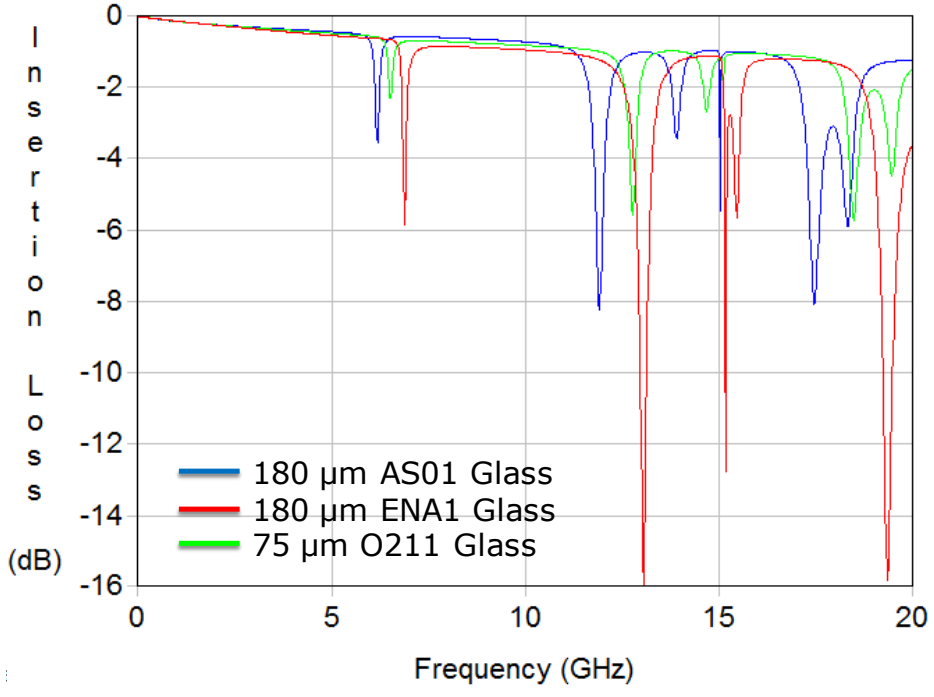


Figure 43. Insertion loss plots of MSL-TPV transitions in different glass interposers.

It is observed that in glass interposers, signal paths comprising of CPW lines and TPVs (Figure 41) have better electrical behavior than those comprising of MSLs and TPVs (Figure 43). The difference is mainly caused by the power-ground plane resonances in the latter scenario.

3.2 Parasitic Extraction of Glass TPVs

The electrical parasitics (resistance and inductance) of glass TPVs were extracted from simulation results. Figure 44 shows the top and side views of the structure used to extract the resistance and inductance of the TPV. The TPV in the center of this figure is the TPV under test. The metal pad on top of this TPV is excited at its either end (marked by 'S') with respect to the outer metal pad (marked by 'G'). Ground TPVs on either side of the TPV under test connect the outer metal pad to the bottom plane. All the TPVs are connected to each other by the bottom metal plane.

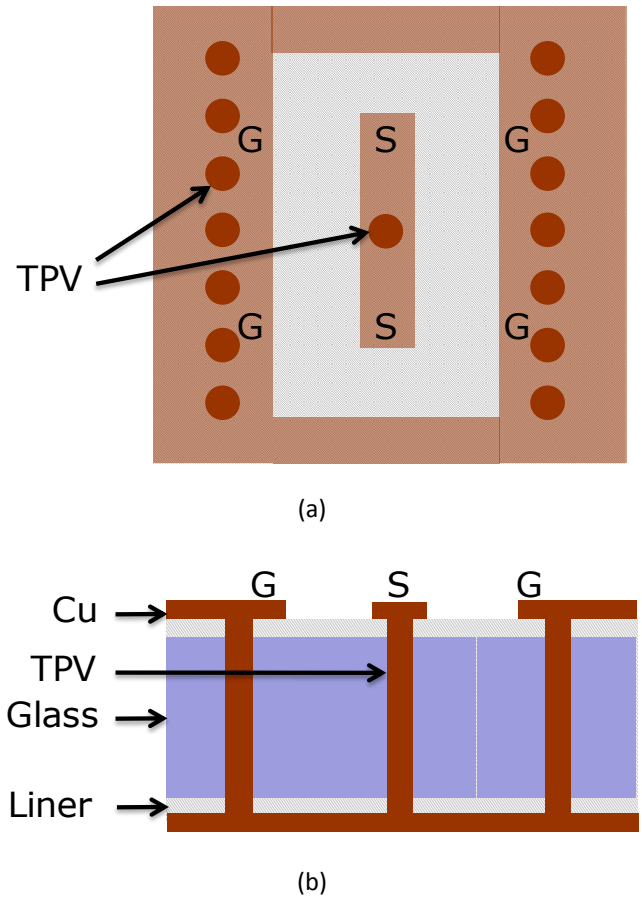


Figure 44. Structure for extracting resistance and inductance of TPV. (a) Top View, (b) Side view.

The structure shown in Figure 44 was excited with two discrete (lumped) ports on either end of the top signal metal pad. An equivalent T-model (as shown in Figure 45) was obtained from the simulated S-parameters. The component Z1 represent the signal test pad (from the probing point marked as 'S' to the top of the signal TPV as shown in Figure 44). The component Z2 represent the signal TPV under test. The real and imaginary parts of the component Z2 yields the resistance and inductance of the TPV, respectively.

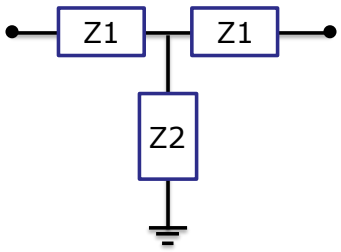


Figure 45. Equivalent T-model of the structure shown in Figure 44.

The extracted resistance and inductance of the TPVs are shown in Figure 46 and Figure 47, respectively. It is observed that the resistance and inductance of the smaller TPVs are higher than those of the bigger TPVs. The resistance of the TPV with 35 µm diameter is approximately three times that of the TPV with 150 µm diameter. The resistance increases with frequency because of skin effects.

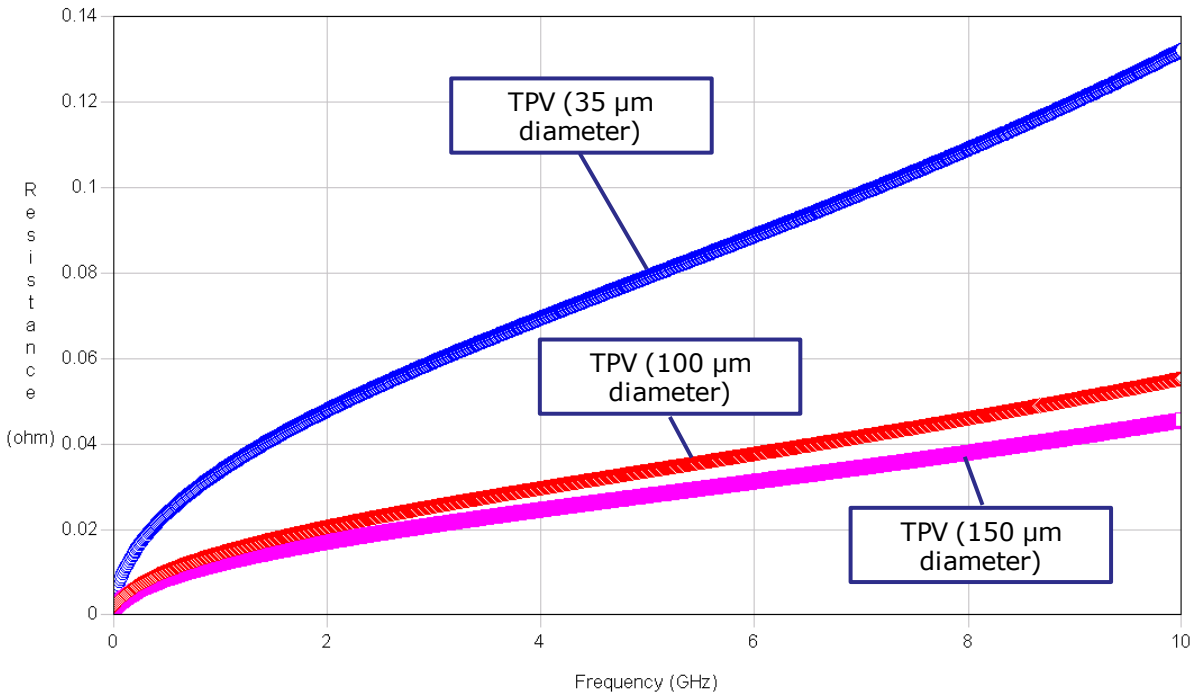


Figure 46. Resistance plots for glass TPVs with different diameters.

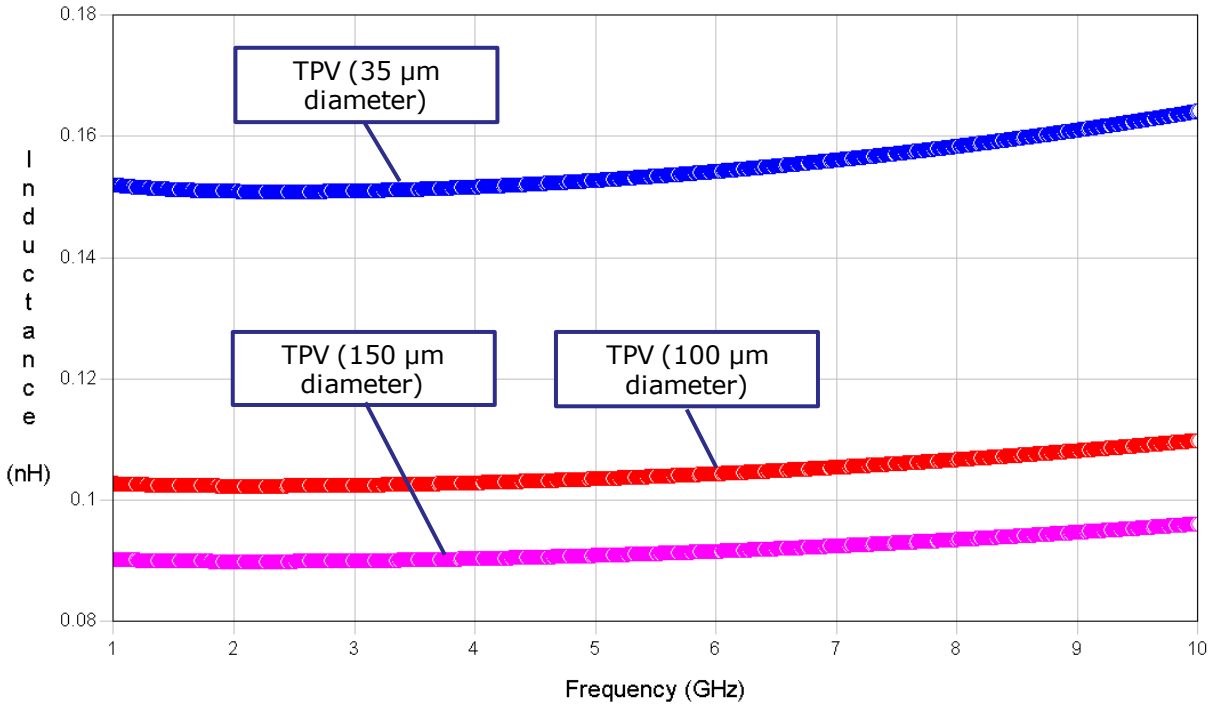


Figure 47. Inductance plots for glass TPVs with different diameters.

3.3 Current Density Simulation

Current density in the interconnections is an important parameter that needs to be carefully considered while designing electronic systems and modules. Copper interconnections begin to heat excessively when the current density increases beyond approximately 2×10^{6} A/m^{2}. Electromigration in copper begins when the current density in the copper interconnection is above 10^{10} A/m^{2} (approximately). In this section, the current density in the copper lines and vias are simulated and studied. The simulations are carried out in CST MWS [52]. The models used in these simulations are similar to that shown in Figure 40.

The glass interposer consisted of 180 µm thick ENA1 glass laminated with 20 µm thick RXP4 polymer. Similar results were seen with ZIF polymer and other glasses, as well. The Cu thickness (in the CPW lines) was 5 µm. The CPW lines were 1 mm long.

Table 3 shows the peak current densities in the CPW line at different frequencies. The width of the CPW line was varied in the simulations to study the effect of line width on peak current density. The TPV diameter was 30 µm on top and 20 µm on the bottom. The TPV pitch was 60 µm. It is observed that the peak current density in the CPW line increases as the line width is decreased. The current density increases with increase in excitation frequency due to skin effect. However, the maximum current density in the lines is well within the current carrying limits of copper traces.

Table 3: Current density in CPW lines.

Frequency (GHz)	**CPW line (5 µm wide)**	**CPW line (10 µm wide)**	**CPW line (15 µm wide)**
0	0.003 A/m^2	0.002 A/m^2	0.001 A/m^2
0.1	358 A/m^2	342 A/m^2	209 A/m^2
1	3616 A/m^2	3394 A/m^2	2081 A/m^2
5	18452 A/m^2	16702 A/m^2	10269 A/m^2
10	37090 A/m^2	32981 A/m^2	20337 A/m^2

Table 4 shows the peak current densities in the TPVs at different frequencies. The TPV diameter was varied in the simulations to study the effect of TPV diameter on peak current density. The CPW lines were 10 µm wide. It is observed that the peak current density in the TPVs increase as the diameter is decreased. The current density increases

with increase in excitation frequency due to skin effect. However, the maximum current density in the TPVs is well within the current carrying limits of copper traces.

Table 4: Current density in TPVs.

Frequency (GHz)	TPV (30 µm diameter, 60 µm pitch)	TPV (60 µm diameter, 120 µm pitch)	TPV (100 µm diameter, 200 µm pitch)
0	0.8 mA/m^2	0.2 mA/m^2	72 µA/m^2
0.1	94 A/m^2	50 A/m^2	30 A/m^2
1	941 A/m^2	502 A/m^2	333 A/m^2
5	4711 A/m^2	2516 A/m^2	1669 A/m^2
10	9438 A/m^2	5045 A/m^2	3347 A/m^2

To improve the thermo-mechanical reliability of the TPVs, a low-modulus metal (like palladium) can be used as a TPV side-wall liner, as shown in Figure 48. The diameter of the TPV (including the Cu and Pd) was 30 µm on the top and 20 µm on the bottom. The CPW lines were 10 µm wide.

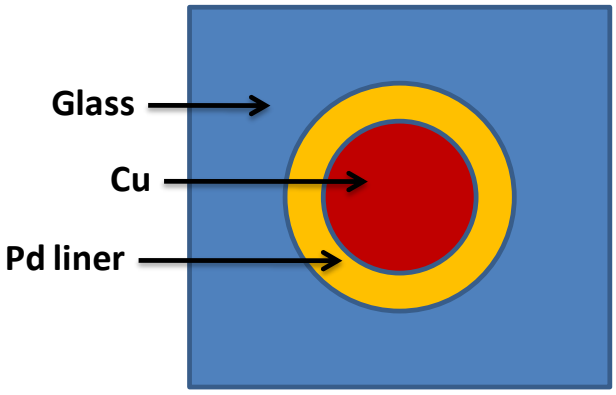


Figure 48. Cross-sectional schematic of a Pd-lined TPV in glass interposer.

Table 5 shows the peak current densities in the TPVs at different frequencies. The Pd liner thickness was varied in the simulations to study the effect of liner thickness on peak current density. The peak current density was observed in the Pd liner due to skin effect. It is observed that the peak current density in the TPVs increase as the liner thickness is decreased. The current density increases with increase in excitation frequency due to skin effect. However, the maximum current density in the TPVs is well within the current carrying limits of palladium.

Table 5: Current density in Pd-lined TPVs.

Frequency (GHz)	Pd-lined TPV (1 μm liner)	Pd-lined TPV (5 μm liner)
0	0.17 mA/m^2	0.26 mA/m^2
0.1	131 A/m^2	85 A/m^2
1	1314 A/m^2	845 A/m^2
5	6587 A/m^2	4230 A/m^2
10	13203 A/m^2	8476 A/m^2

Figure 49 compares the insertion loss plots of the Pd-lined TPVs and Cu-filled TPVs (without any Pd-liner). It is observed that the loss of the Pd-lined TPVs is slightly higher than that of the TPV without Pd-liner. The increase in loss can be attributed to the higher resistivity of Pd (approximately 105 nΩ-m) as compared to Cu (approximately 17 nΩ-m). There is almost no variation in the insertion loss with change in the Pd liner thickness.

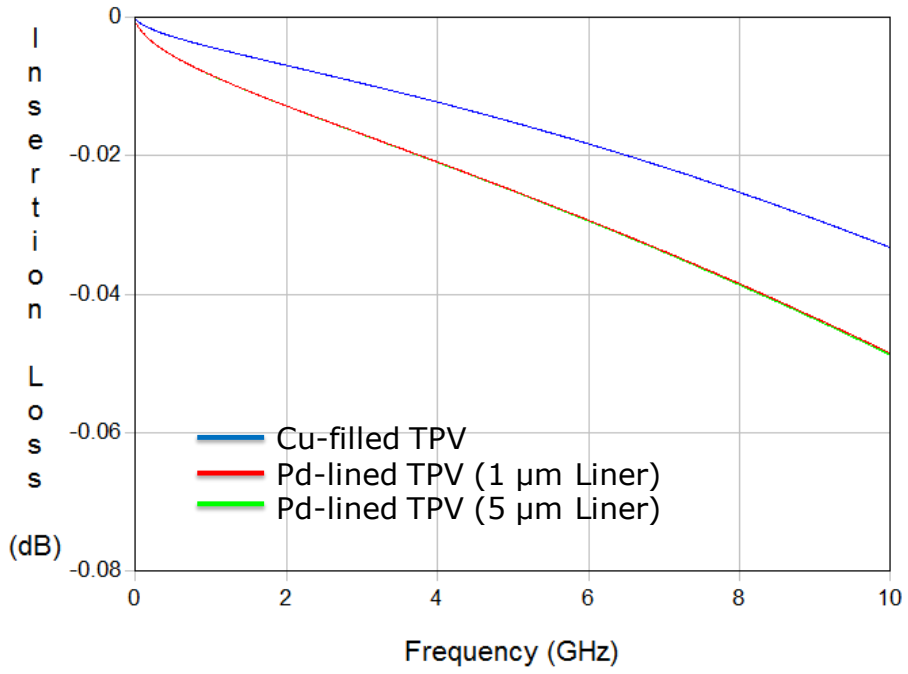


Figure 49. Effect of Pd-lining on the insertion loss of TPVs.

The thermo-mechanical reliability of TPVs in glass interposers can also be improved by using conformal metal filling (instead of completely filling the TPV). Figure 50 shows the cross-sectional schematic of a fully filled TPV and a conformally filled TPV. The conformal TPV was modeled with 5 µm thick Cu layer where the TPV outer diameter was 30 µm. The filled TPV was also 30 µm in diameter.

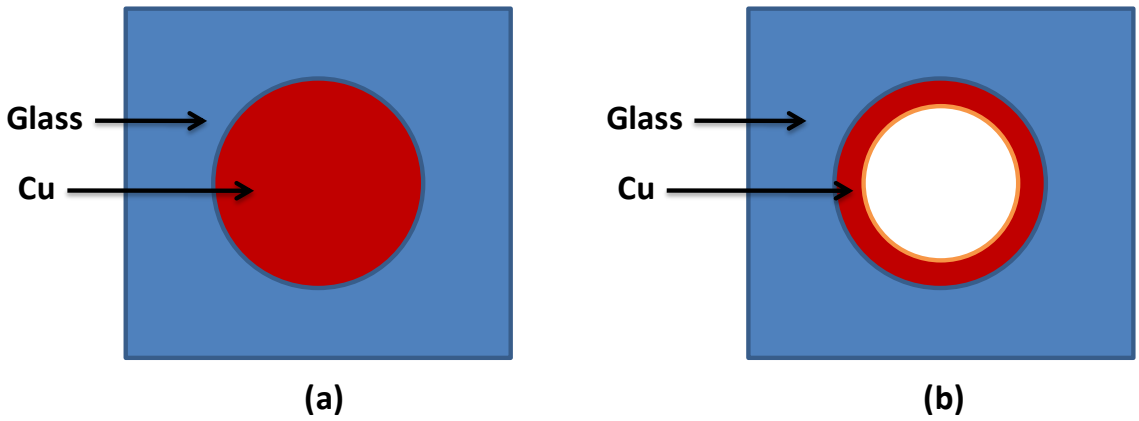


Figure 50. Cross-sectional schematic of TPV in glass interposer. (a) Filled TPV, (b) Conformal TPV.

Table 6 shows the peak current densities in the TPVs at different frequencies. The conformal TPV has higher peak current densities as compared to the filled TPV. The current density increases with increase in excitation frequency due to skin effect. However, the maximum current density in the TPVs is within the current carrying limits of copper.

Table 6: Current density in filled and conformal TPVs.

Frequency (GHz)	Filled TPV	Conformal TPV
0	0.8 mA/m^2	1.4 A/m^2
0.1	94 A/m^2	138 A/m^2
1	941 A/m^2	1476 A/m^2
5	4711 A/m^2	7209 A/m^2
10	9438 A/m^2	11873 A/m^2

Figure 51 compares the insertion loss plots of the filled TPV and the conformal TPV. It is observed that the loss of the conformal TPV is slightly higher than that of the filled TPV, although the difference is negligible. This is because most of the current is carried by the conductor surface (skin effect).

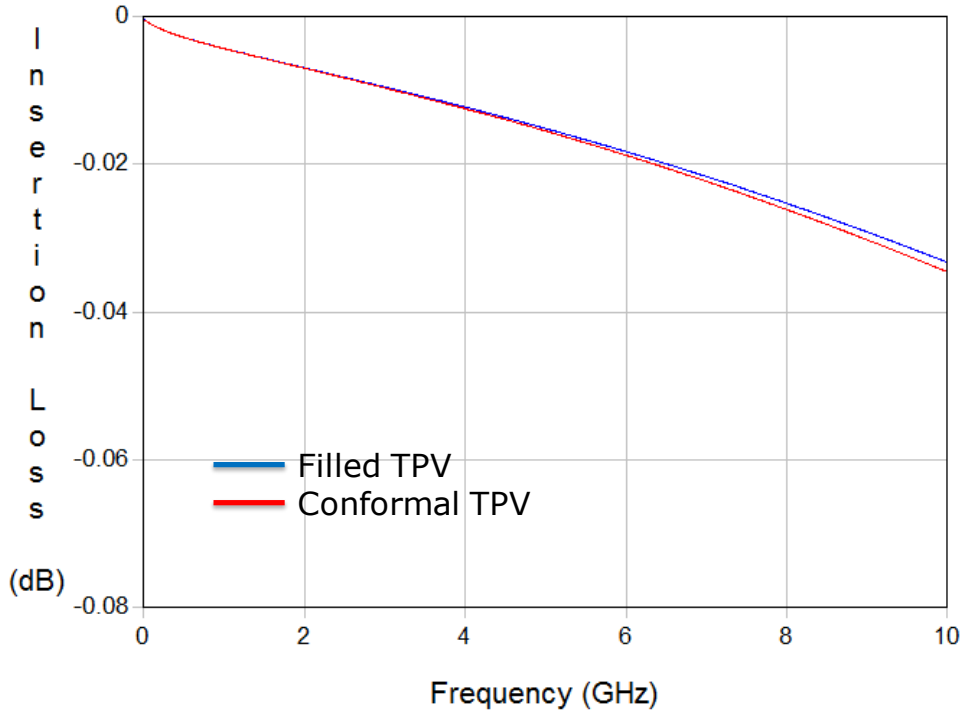


Figure 51. Effect of conformal via filling on its insertion loss.

3.4 Conclusion

TPVs in glass interposer have approximately 0.5 dB lower electrical signal loss and approximately 14 dB lower crosstalk as compared with TPVs in silicon interposer at 10 GHz. The insertion losses of smaller TPVs are higher than those of larger TPVs in glass interposers. The inductance and resistance of the TPVs increases with decrease in the TPV diameter.

Signal paths comprising of CPW lines and TPVs have better electrical behavior than those comprising of MSLs and TPVs in glass interposers. The signal path comprising of CPW lines and TPVs do not have return path discontinuities (RPDs). The MSL-TPV signal path has RPDs. The presence of RPDs and the power-ground plane resonances in glass interposers make the MSL-TPV signal path to suffer from worse eye diagram as compared to the CPW-TPV signal path. Careful power delivery design in glass interposers using appropriate choice and location of decoupling capacitors will help in solving the power-ground plane resonance issues and improve the eye diagram of the MSL-TPV signal path.

The current densities in the TPVs and interconnection lines are well within the current carrying limits of the interconnection material. The TPVs designed for better thermo-mechanical reliability (like Pd-lined TPVs and conformally filled TPVs) have almost similar electrical performance (loss and peak current density) as fully filled TPVs. The different glass and polymers that were considered had little effect on the insertion loss of the TPVs.

CHAPTER 4

POWER DELIVERY NETWORK DESIGN

Power integrity plays an important role in driving system performance. Therefore, it is essential to acquire an in-depth understanding of the issues that impact the power integrity of 3D interposers. To provide clean power, decoupling capacitors need to be placed close to the chips. This chapter studies the power-delivery network (PDN) in silicon and glass interposers. In silicon interposers, the MOS capacitance of Si TPVs is utilized for decoupling. A 3D power-delivery network (PDN) is simulated using the proposed Si TPV circuit-model (Section 2.2.3) to show the effect and importance of the voltage-dependent Si TPV MOS capacitance.

4.1 Power Delivery Network in Si Interposers

Modeling the voltage-dependent MOS capacitance is important for accurate electrical modeling of Si TPV, as discussed in Section 2.2. To study the effect of the Si TPV MOS capacitance in a practical application, the power-delivery network (PDN) in a 3D system is modeled and simulated in this section. Figure 52 shows the schematic view of the PDN that is studied.

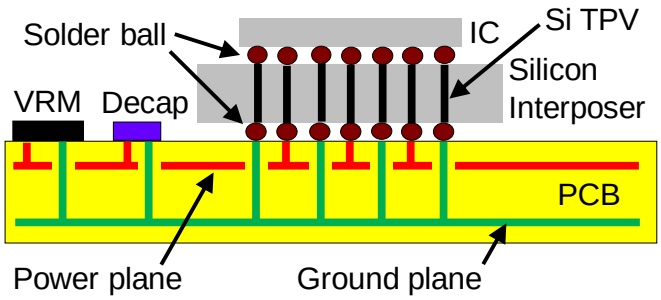


Figure 52. Schematic view of the power-delivery network of a 3D system with Si interposer.

Power is supplied from the Voltage Regulator Module (VRM) which is placed on the Printed Circuit Board (PCB). Multiple decoupling capacitors (Decap) are placed on the PCB. The parasitics of the decoupling capacitors on the PCB were 0.23 nF capacitance, 0.1 Ω resistance, and 0.2 nH inductance. These decaps were placed close to (within 4 mm) the interposer. The dielectric material between the PCB power and ground planes was modeled as 100 µm thick standard FR4. The Si TPVs in the silicon interposer supply power from the PCB to the IC. The IC is assembled on the interposer by solder ball connections. The interposer is assembled on the PCB with solder ball connections. Figure 53 shows the model of the PDN.

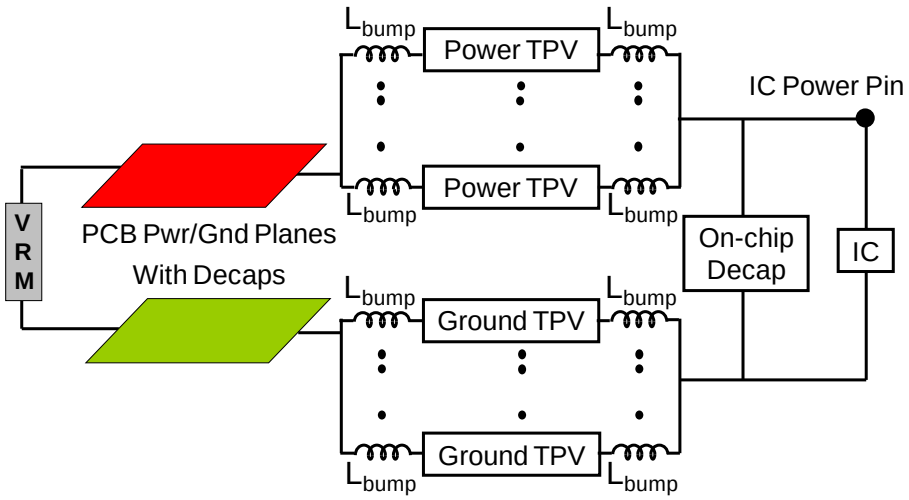


Figure 53. Conceptual model of power-delivery network of a 3D system.

The PCB power and ground planes along with the decoupling capacitors were simulated in Sphinx - a frequency-domain signal and power co-simulator [54]. The solder balls were represented by lumped inductances (L_{bump}). The equivalent circuit-model of the Si TPV, as shown in Figure 11 (b), was used to model the power and ground Si TPVs. The circuit was simulated in Agilent ADS [55].

The simulated Si TPVs were 30 µm in diameter and 100 µm in length. They were filled with copper and had 0.1 µm thick SiO_2 liner. The Si was doped p-type and its resistivity was 10 Ω-cm. The solder balls connecting the PCB and the interposer were modeled as 250 pH inductance. The solder balls connecting the interposer and the IC were modeled as 50 pH inductance. The on-chip decoupling capacitor was modeled by a series RLC circuit with 2 Ω resistance, 110 pH inductance and, 1 pF capacitance. The PCB power-ground planes were 10 cm by 10 cm in size.

Figure 54 shows the simulated impedance plots at the power pin of the IC. Three cases were simulated – (i) Si interposer biased with Si TPVs operating in the accumulation region, (ii) Si interposer biased with Si TPVs operating in the inversion region and, (iii) Si interposer floating. Small impedance is desirable to reduce the power supply noise in the system.

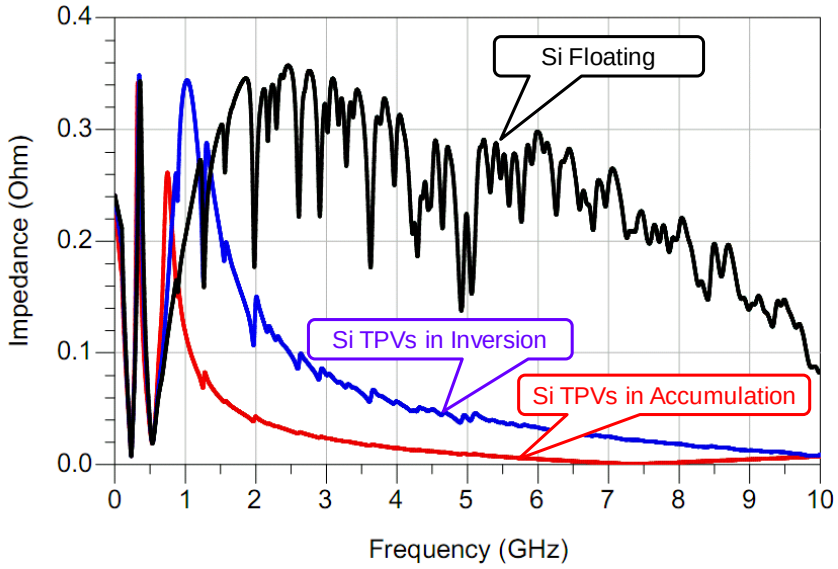


Figure 54. Simulated impedance plots at the IC power pin (as shown in Figure 53) of a 3D system.

It is observed from Figure 54 that the plots where the Si interposer is biased (i.e., Si TPVs in inversion and accumulation regions) have lower impedance than the plot where the Si interposer is floating. Si TPV MOS capacitance is absent when the Si interposer is floating. When the Si interposer is biased, the Si TPV MOS capacitance effect adds a decoupling capacitance to the power Si TPV. This helps in reducing the impedance. The MOS capacitance is higher in accumulation region than in the inversion region. This is the reason for the accumulation mode impedance being lower than that in the inversion mode.

For a Si interposer which is biased, if the MOS capacitance effect is neglected it is equivalent to modeling the PDN with the assumption that the Si is floating (black curve in Figure 54). This leads to overestimation of the impedance and can lead to inaccurate system performance prediction.

As discussed in Section 2.4.1, TPVs in the signal-delivery network (SDN) should have small capacitance to improve the signal integrity of high-speed digital signals. However, TPVs in the PDN need high capacitance to enhance its decoupling behavior. In a real situation, it is difficult to have different physical designs in the same interposer for TPVs in SDN and PDN. To understand the impact of different biasing conditions (i.e., different TPV MOS capacitance values) on its insertion loss, the Si TPV model was simulated. Figure 55 shows the insertion loss of Si TPVs under different biasing conditions. The dimensions of the TPVs were the same as mentioned earlier in this section.

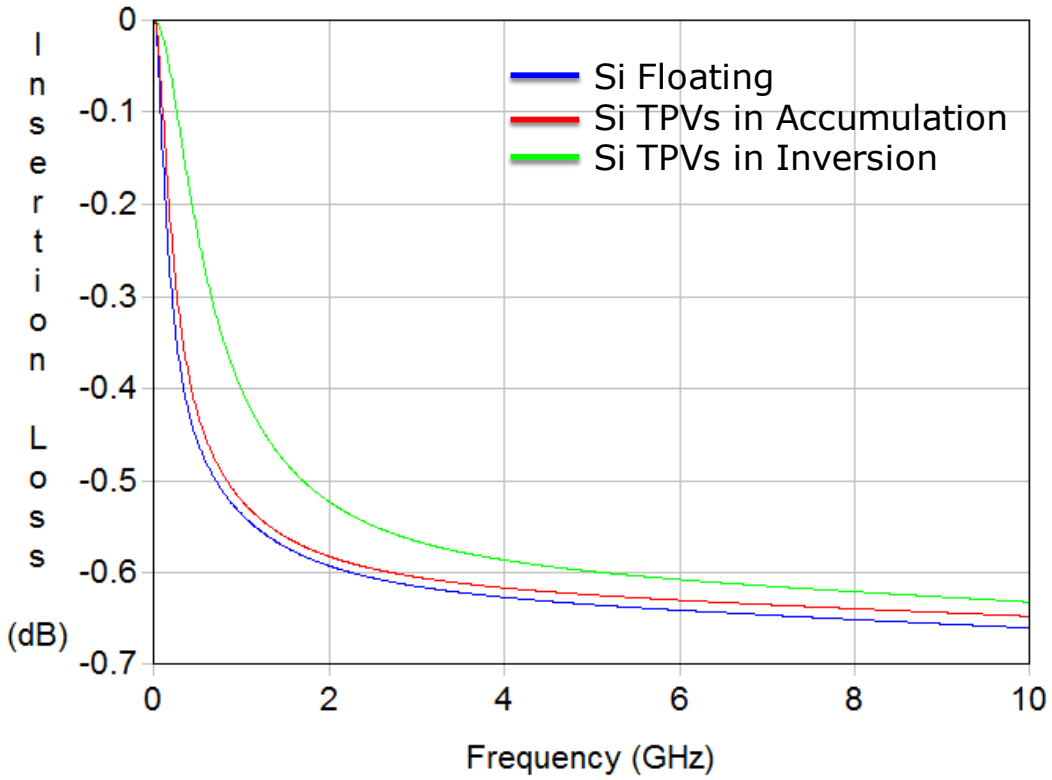


Figure 55. Insertion Loss of Si TPVs under different biasing conditions.

It is observed that the loss of the TPVs biased in accumulation and inversion regions is lower than that of the TPV with the Si substrate in floating condition (unbiased state). The loss of the TPV biased in inversion region is lower than that of the one in accumulation region because of lower capacitance of the former (smaller $C_{MOS}(V)$ in the circuit model of Figure 11 (b)). However, the difference in loss between these two cases is less than 0.1 dB in DC-10 GHz frequency range.

A signal path in Si interposer comprising of two CPW lines (each 15 µm wide and 2 mm long) connected by TPVs was also modeled and simulated. Figure 56 compares the insertion loss of this signal path under different biasing conditions. It is observed that the difference in loss is insignificant in the DC-10 GHz frequency range. The MOS

capacitance of the Si TPV in inversion and accumulation region is 3.2 pF and 1.04 pF, respectively. The signal path comprises of 4 mm of CPW line and 100 µm of Si TPV. The insertion loss of the signal path is dominated by the CPW lines, and the difference in Si TPV capacitance has a small role.

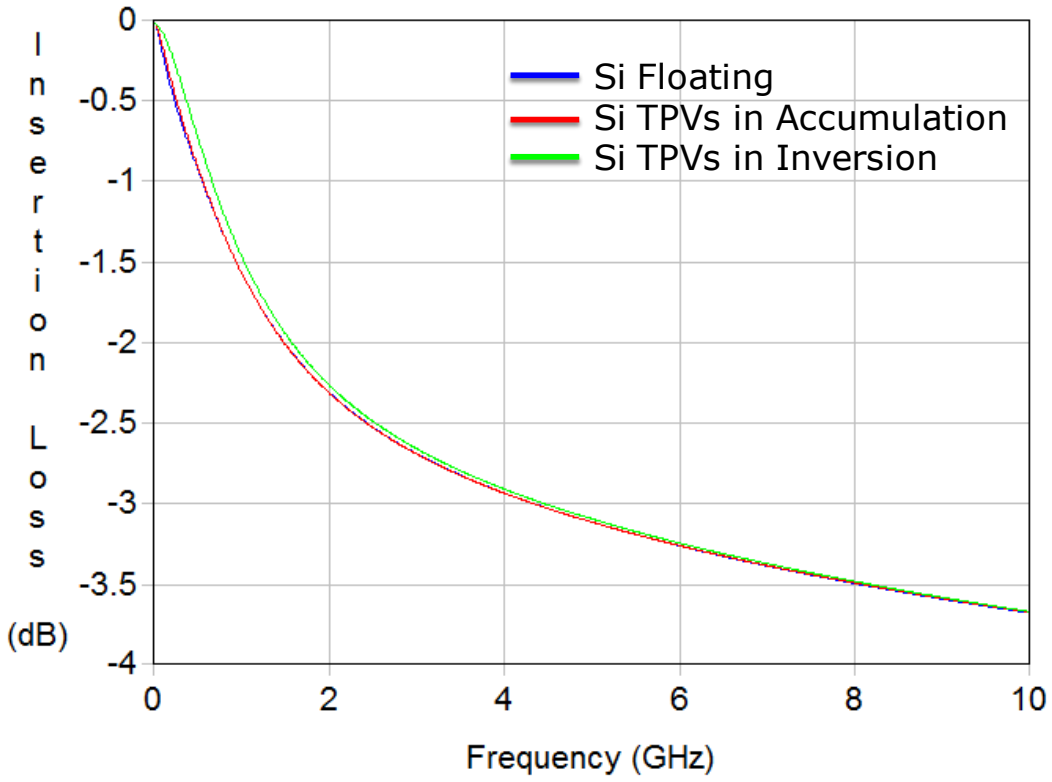


Figure 56. Insertion loss of CPW-TPV-CPW signal path in Si interposer under different biasing conditions.

From the above results, it can be concluded that the Si TPV capacitance has a more important role in the performance of the PDN as compared to the SDN of a Si interposer. To enhance the decoupling behavior of the Si TPVs, they should be biased in the accumulation region.

4.2 Power Delivery Network in Glass Interposers

The power-delivery network of a 3D system with glass interposer is modeled and simulated in this section. The results are compared with those of the Si interposer (Section 4.1). Figure 57 shows the schematic view of the PDN in a 3D system with glass interposer.

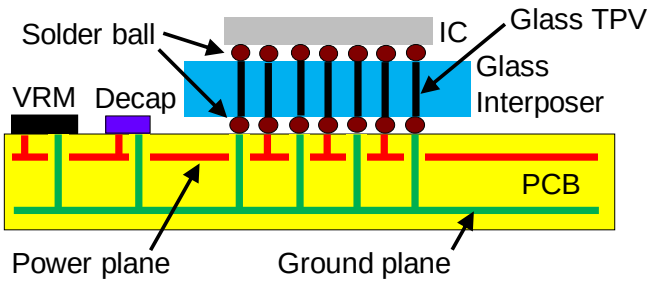


Figure 57. Schematic view of the power-delivery network of a 3D system with glass interposer.

Power is supplied from the voltage regulator module (VRM) which is placed on the printed circuit board (PCB). Multiple decoupling capacitors (Decap) are placed on the PCB. The TPVs in the glass interposer supply the power from the PCB to the IC. The IC is assembled on the interposer by solder ball connections. The interposer is assembled on the PCB with solder ball connections. The conceptual circuit model of the PDN is similar to that shown in Figure 53.

The PCB power and ground planes along with the decoupling capacitors were simulated in Sphinx - a frequency-domain signal and power co-simulator [54]. The solder balls were represented by lumped inductances (L_{bump}). The glass TPVs were modeled and simulated in CST Microwave Studio [52]. The complete PDN circuit was simulated in Agilent ADS [55].

The simulated TPVs were 30 µm in diameter. They were filled with copper. The glass interposer consisted of ENA1 glass laminated on both surfaces with ZIF polymer. The solder balls connecting the PCB and the interposer were modeled by 250 pH inductance. The solder balls connecting the interposer and the IC were modeled by 50 pH inductance. The on-chip decoupling capacitor was modeled by a series RLC circuit with 2 Ω resistance, 110 pH inductance and, 1 pF capacitance. The PCB power-ground planes were 10 cm by 10 cm in size.

Figure 58 shows the simulated impedance plots at the power pin of the IC. The glass interposer consisted of 576 power and 576 ground TPVs.

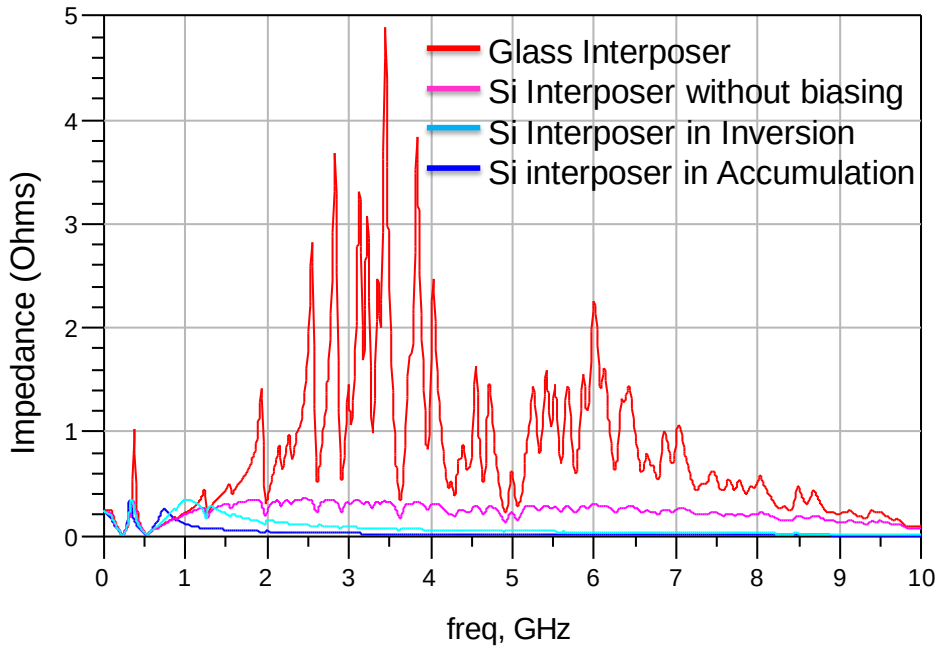


Figure 58. Simulated impedance plots at the IC power pin of a 3D system. The glass interposer PDN consists of 1 pF on-chip decoupling capacitor.

It is observed that the PDN impedance of the glass interposer is higher than that of the Si interposer. The PDN impedance plot of the glass interposer changed little when the number of power and ground TPVs was increased to 1000 each. The conductivity of silicon is much higher as compared to glass. Due to this reason, the equivalent dielectric constant of the Si interposer (consisting of SiO_2-Si-SiO_2 layers) is much higher as compared to that of glass interposer (consisting of polymer-glass-polymer layers). The high conductivity of Si helps in damping the power-ground plane resonances [53]. This leads to smaller impedance in double-sided Si interposers as compared to double-sided glass interposers.

The PDN of glass interposer with co-axial TPVs was also modeled and simulated. Figure 59 shows the schematic cross-section view of a co-axial TPV. Two types of co-axial TPVs were studied. The physical dimensions of these TPVs are outlined in Table 7.

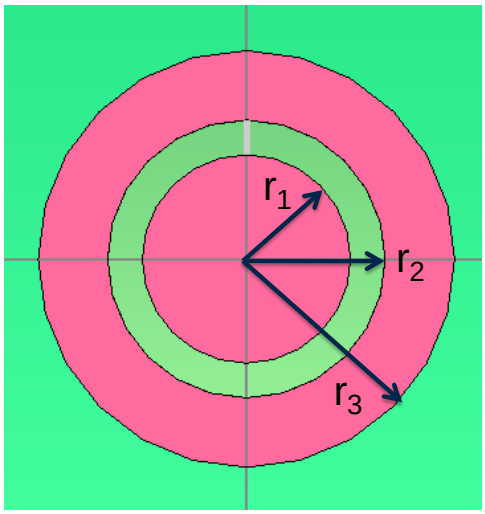
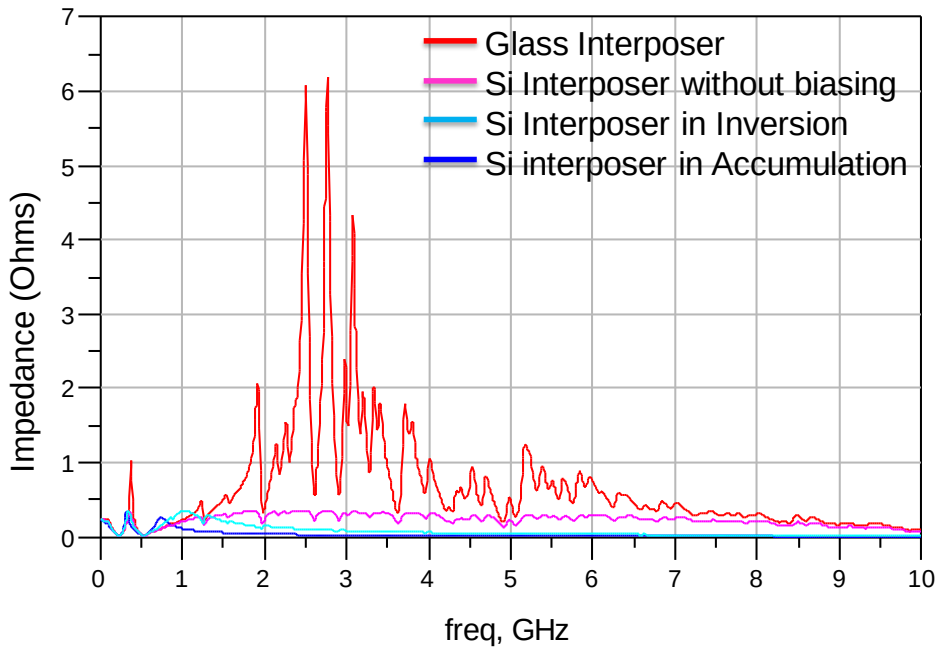


Figure 59. Schematic of a co-axial TPV.

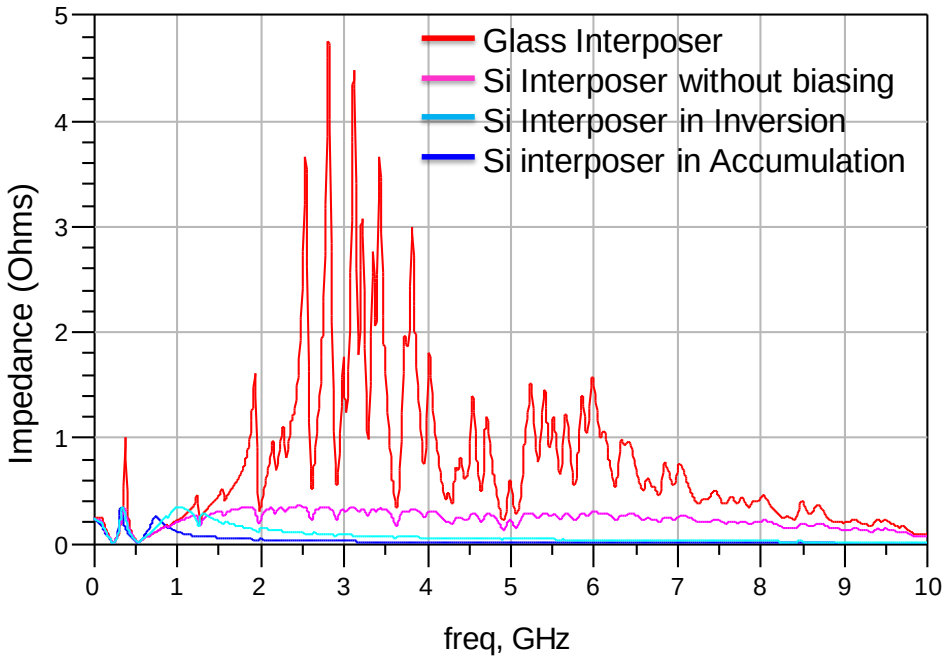
Table 7: Physical dimensions of co-axial TPVs in glass interposer.

Co-axial TPV	r_1 (µm)	r_2 (µm)	r_3 (µm)
TPV A	15	20	30
TPV B	5	10	15

The PDN impedance of the glass interposer with co-axial TPVs is shown in Figure 60 (a) and (b). It is observed that the impedance of the glass interposer with smaller TPVs (TPV B) is lower than that of the one with larger TPVs (TPV A). However, the impedance of the glass interposer with the co-axial TPVs is higher as compared to the Si interposer.



(a)



(b)

Figure 60. Simulated impedance plots at the IC power pin of a 3D system. The glass interposer PDN consists of co-axial TPVs and 1 pF on-chip decoupling capacitor. (a) Glass interposer with TPV A, (b) Glass interposer with TPV B.

To improve the PDN of glass interposers, the on-chip decoupling capacitance was increased from 1 pF to 100 pF. Figure 61 shows the PDN impedance plot of glass interposer with cylindrical TPVs and 100 pF on-chip decoupling capacitance. The Si interposer PDN impedance plots assume 1 pF on-chip decoupling capacitance. It is observed that the PDN impedance for the glass interposer is significantly reduced beyond 2.5 GHz (as compared to the glass interposer plot in Figure 58).

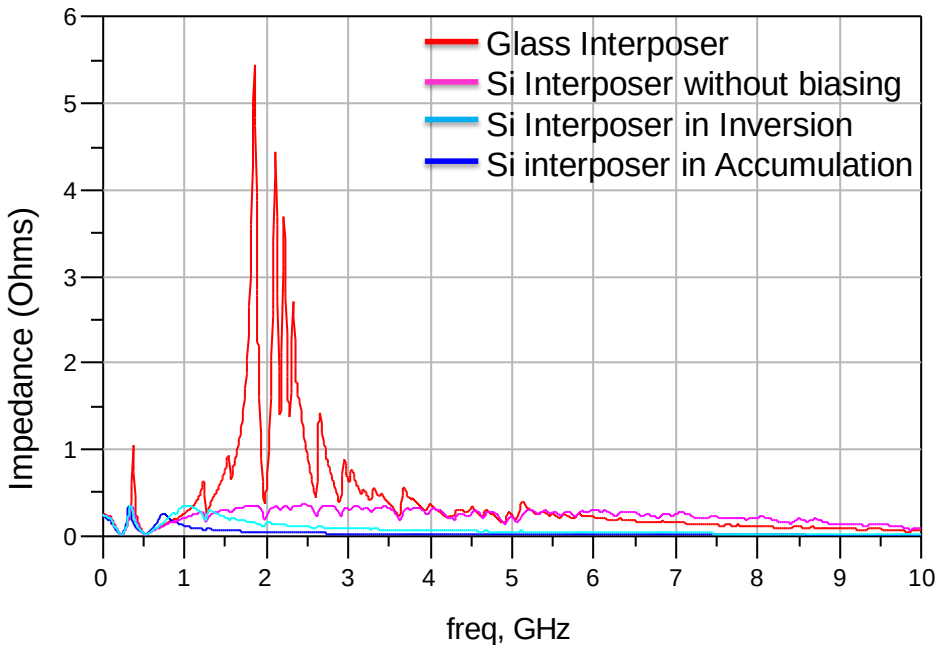


Figure 61. Simulated impedance plots at the IC power pin of a 3D system. The glass interposer PDN consists of 100 pF on-chip decoupling capacitor.

The PDN impedance of the glass interposer in Figure 61 is still high between 1 and 4 GHz. The on-chip decoupling capacitance was increased to 2 nF to bring the glass interposer PDN impedance to the levels of that of the Si interposer. Figure 62 shows the PDN impedance plot for glass interposer with 2 nF on-chip decoupling capacitance.

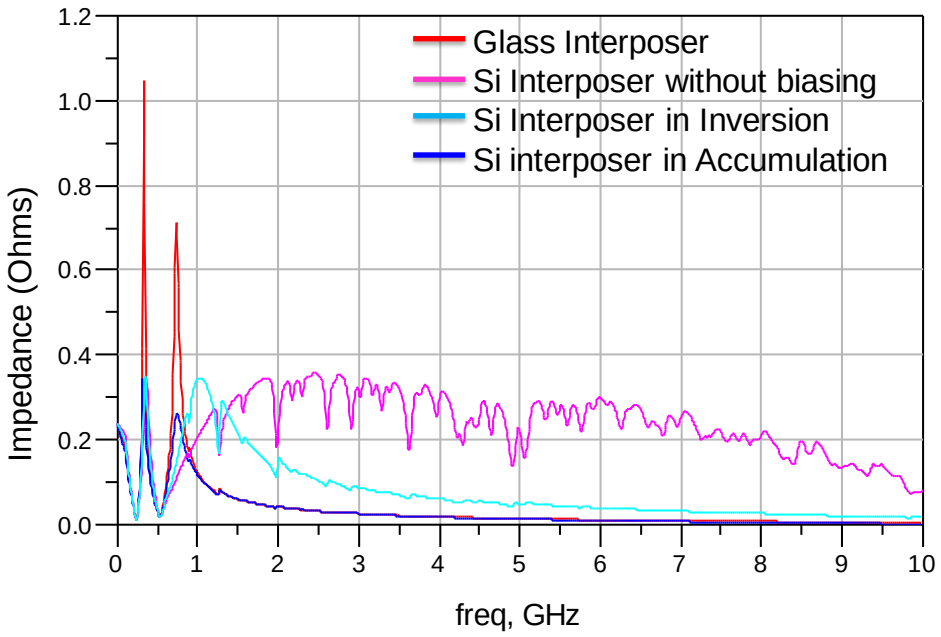


Figure 62. Simulated impedance plots at the IC power pin of a 3D system. The glass interposer PDN consists of 2 nF on-chip decoupling capacitor.

It is observed from Figure 62 that the PDN impedance of the glass interposer is similar to the PDN plot for the Si interposer with the Si TPVs biased in accumulation region. The impedance peaks below 1 GHz can be reduced by using discrete PCB decoupling capacitors.

4.3 Conclusion

In this chapter the PDN in 3D systems (with Si interposers and glass interposers) was modeled, simulated, and compared. It is important to model the MOS capacitance of Si TPVs for PDN simulations in 3D systems. The MOS capacitance of Si TPVs helps in decoupling the PDN. To achieve lower power noise, the Si substrate should be biased with the Si TPVs operating in the accumulation region.

TPVs in glass interposers lack the MOS capacitance of Si TPVs. The PDN impedance of glass interposers can be made similar to that of Si interposers by increasing the on-chip decoupling capacitance or by adding decoupling capacitors in the glass interposer.

To achieve the target PDN impedance for a particular system, the decoupling provided by only the MOS capacitance of the Si TPV may not be sufficient. In such scenarios, additional decoupling capacitors in the interposer are required to meet the performance standards. This chapter showed that while comparing silicon and glass interposers for PDN performance, the Si TPV biased in accumulation region provides additional useful decoupling capacitance. The difference in the available decoupling capacitance between Si and glass interposers was 2 nF for the studied via geometries (30 µm diameter, 120 µm pitch, and 100 µm height).

CHAPTER 5

ELECTRICAL CHARACTERIZATION

Fabrication and electrical measurements are important in validating the electrical models and simulations. This chapter presents electrical characterization results of the interconnections in silicon and glass interposers. The measured and simulated results are compared to establish confidence in the simulations. Several test vehicles were designed and fabricated for this purpose. Two-port vector network analyzer (VNA) measurements were performed using microprobes after short-open-load-through (SOLT) calibrations. The simulations were performed using CST Microwave Studio [52].

5.1 Si TPV MOS Capacitance

Measurement results of Si TPV MOS capacitance has been reported in [47], [56], [57], and [58]. High frequency Si TPV capacitance measurement has been presented in [56] and [57], while [47] has measured both - the high and low frequency Si TPV capacitance. The Si TPV C-V curves as obtained from the analysis in this research matches well with the trends in these measured results.

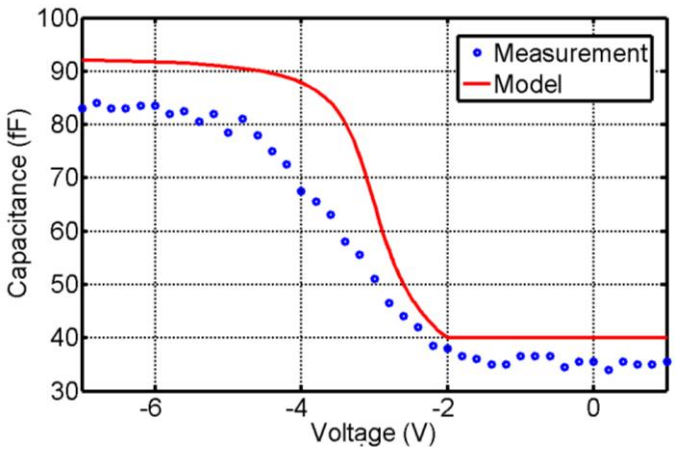


Figure 63. Model-to-Measurement correlation of the Si TPV capacitance based on measured data from [58].

Model-to-measurement correlation is performed with measured data from [58] and the result is shown in Figure 63. The Si TPV was 5 µm in diameter, 20 µm in length, and filled with copper. The thickness of the via side-wall SiO_2 liner was 118.2 nm. The doping concentration of the p-type Si substrate was $2x10^5$ cm^{-3}. It is observed that the modeling result matches closely with the measurement data. The difference is less than 5 fF in the inversion region and less than 10 fF in the accumulation region. The modeling result also correlate closely with the device simulation result presented in [58]. This validates the Si TPV capacitance modeling presented in Section 2.2.

5.2 Interconnection Wiring

Co-planar waveguide (CPW) lines were designed, fabricated, and measured in a SiO_2-coated Si interposer (Wafer-Si interposer). The CPW lines were 1 mm long and 125 µm wide. The gap between the signal and ground was 130 µm. The resistivity and thickness of the Si was 27 Ω-cm and 260 µm, respectively. The SiO_2 coating was 2 µm

thick. Figure 64 shows the insertion loss comparison between measurement and simulation for this CPW line. The simulated results match well with measured data.

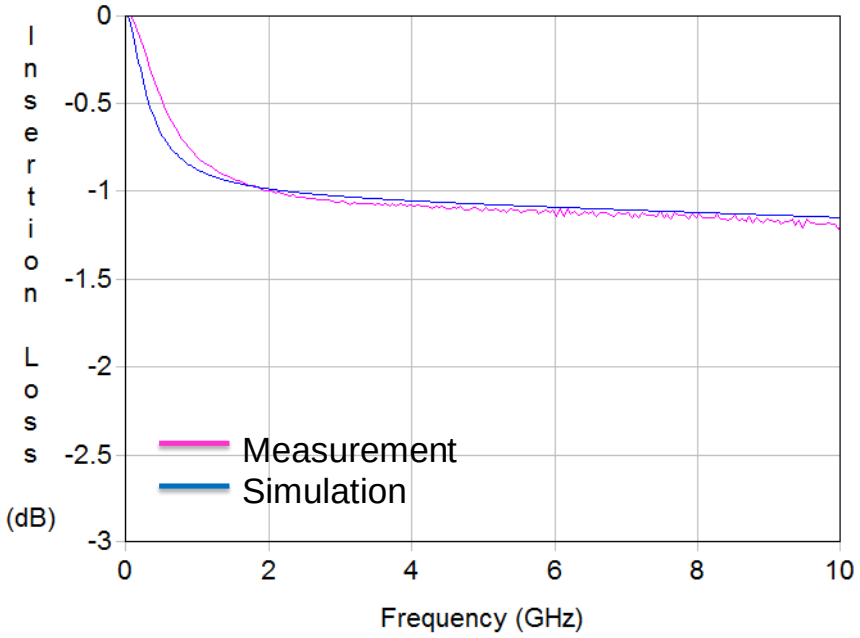


Figure 64. Insertion loss plot of a co-planar waveguide (CPW) line in SiO_2-coated, Si interposer (Wafer-Si interposer).

CPW lines were also designed and fabricated in a polymer-laminated, polycrystalline Si interposer (Panel-Si interposer). The fabricated CPW lines were 160 µm wide. The gap between the signal and ground was 36.5 µm. The resistivity of the Si was 0.15 Ω-cm. The thickness of the Si and the ZIF polymer coating was 220 µm and 40 µm, respectively. Figure 65 shows the insertion loss comparison between measurement and simulation. The simulated results match well with measured data.

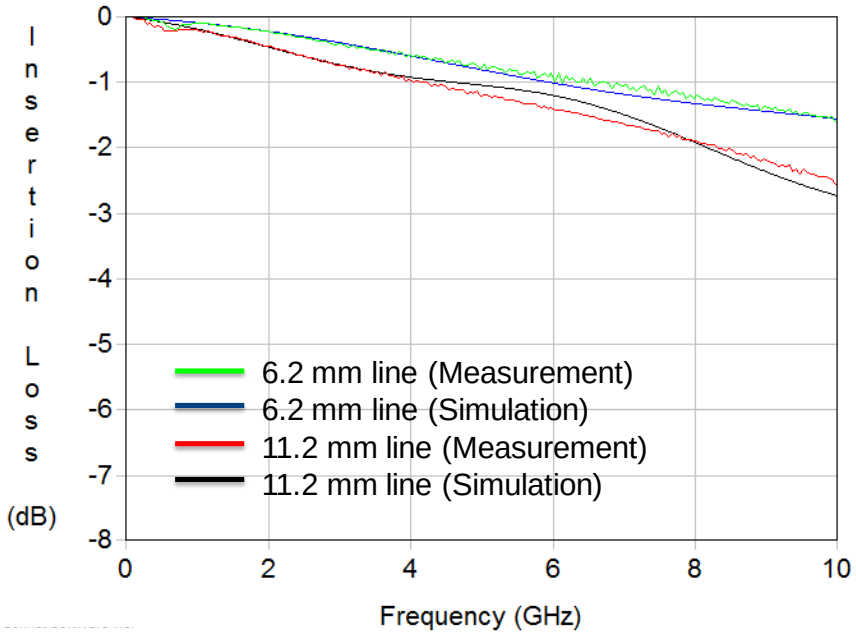


Figure 65. Insertion loss plots of CPW lines in polymer-laminated, polycrystalline Si interposer (Panel-Si interposer).

CPW lines were designed and fabricated in several polymer-laminated, glass interposers. Three types of glass interposer test vehicles were fabricated: (i) 180 µm thick ENA1 glass laminated with 20 µm thick RXP4 polymer, (ii) 180 µm thick ENA1 glass laminated with 17.5 µm thick ZIF polymer, and (iii) 75 µm thick O211 glass laminated with 20 µm thick RXP4 polymer. The CPW lines were 6.2 mm long and 160 µm wide. The gap between the signal and ground was 36.5 µm. Figure 66 shows the insertion loss comparison between measurement and simulation. The simulated results match well with measured data.

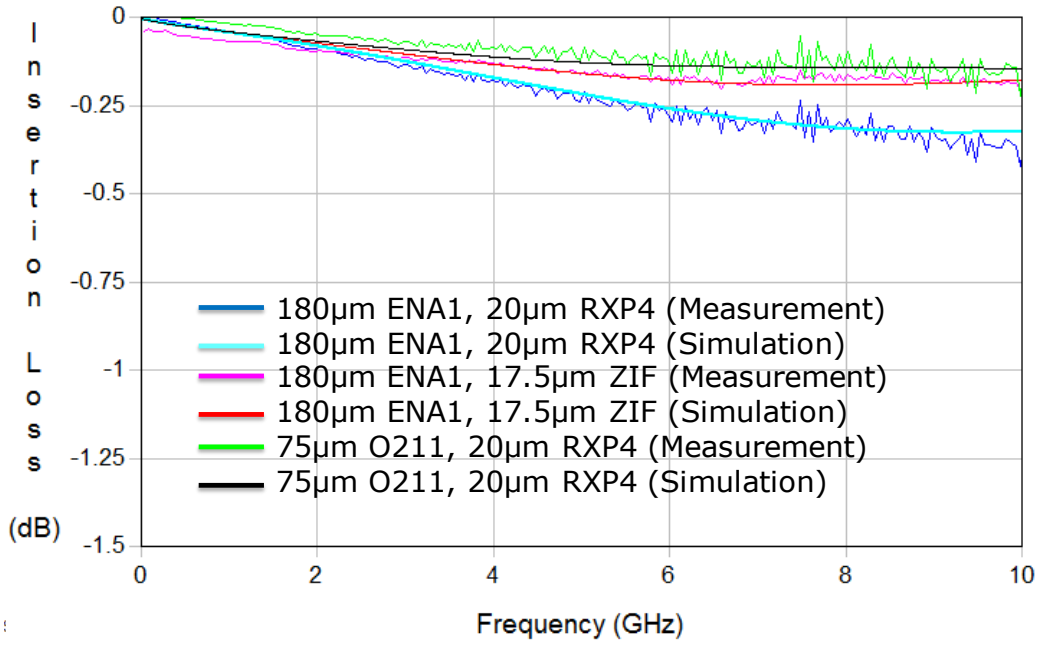


Figure 66. Insertion loss plots of 6.2 mm long CPW lines in glass interposers.

Figure 67 compares the measured insertion loss of CPW lines in glass, panel-Si, and wafer-Si interposers. The CPW line in glass interposer has the lowest loss (approximately 0.06 dB/mm at 10 GHz) because of the very high resistivity of glass, which leads to lower substrate loss as compared to silicon interposers. The CPW line insertion loss is higher (approximately 1.16 dB/mm at 10 GHz) in wafer-Si interposer as compared to that in panel-Si interposer (approximately 0.18 dB/mm at 10 GHz). The lower insertion loss in the panel-Si interposer is due to the thick polymer surface coating which reduces the substrate loss.

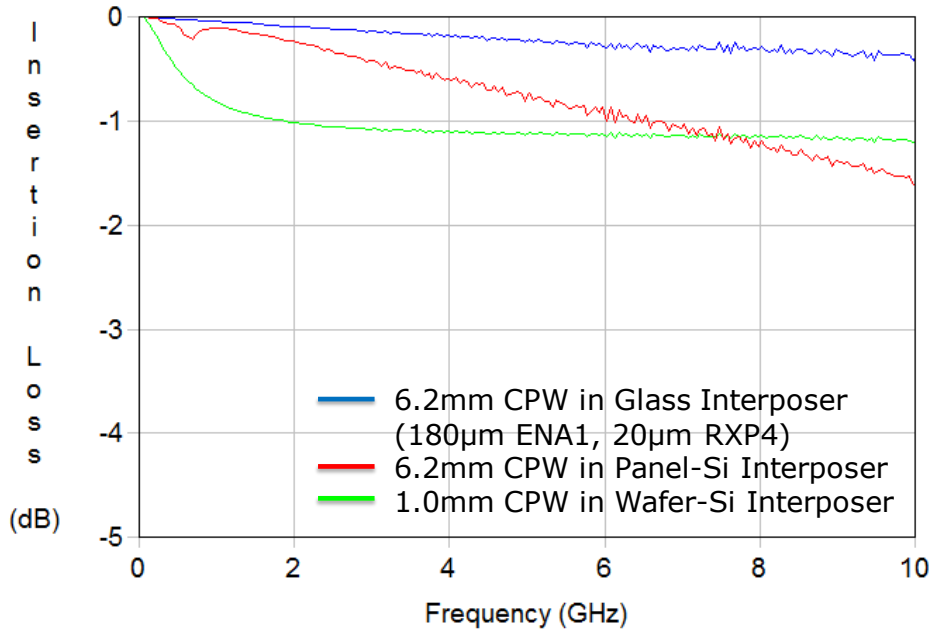


Figure 67. Comparison of measured insertion loss of CPW lines in glass, panel-Si, and wafer-Si interposers.

Figure 68, Figure 69, and Figure 70 show the eye diagram of a 1 mm long CPW line in wafer-Si interposer, panel-Si interposer, and ENA1 glass interposer (laminated with 20 µm thick RXP4 polymer), respectively. The lines were excited by 0-2.5 V, 5 Gbps pseudo-random bit streams (PRBS). Table 8 summarizes the eye diagram parameters.

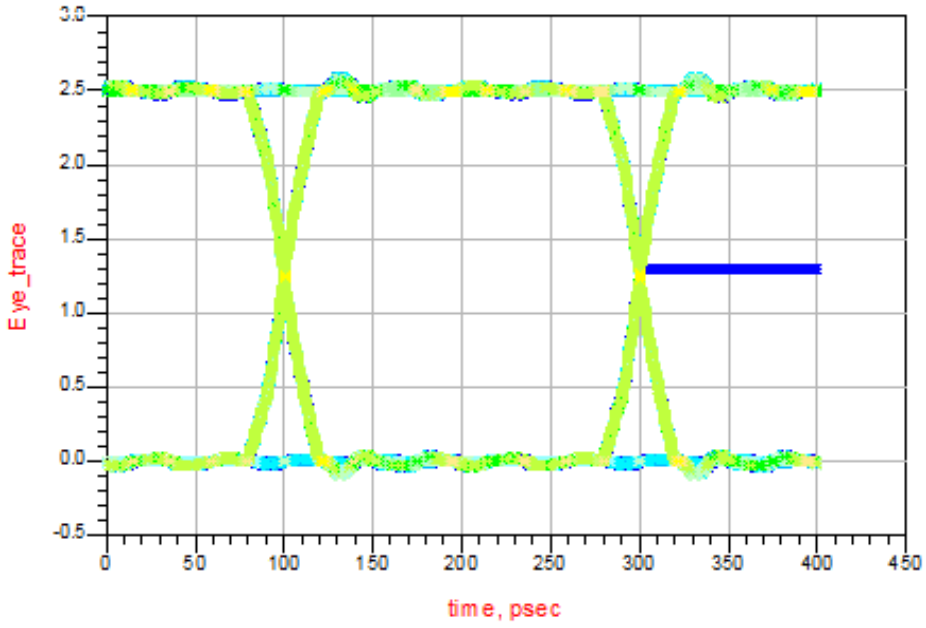


Figure 68. Eye diagram of CPW line (1 mm long) in wafer-Si interposer when excited by a 5 Gbps pseudo-random bit stream (PRBS).

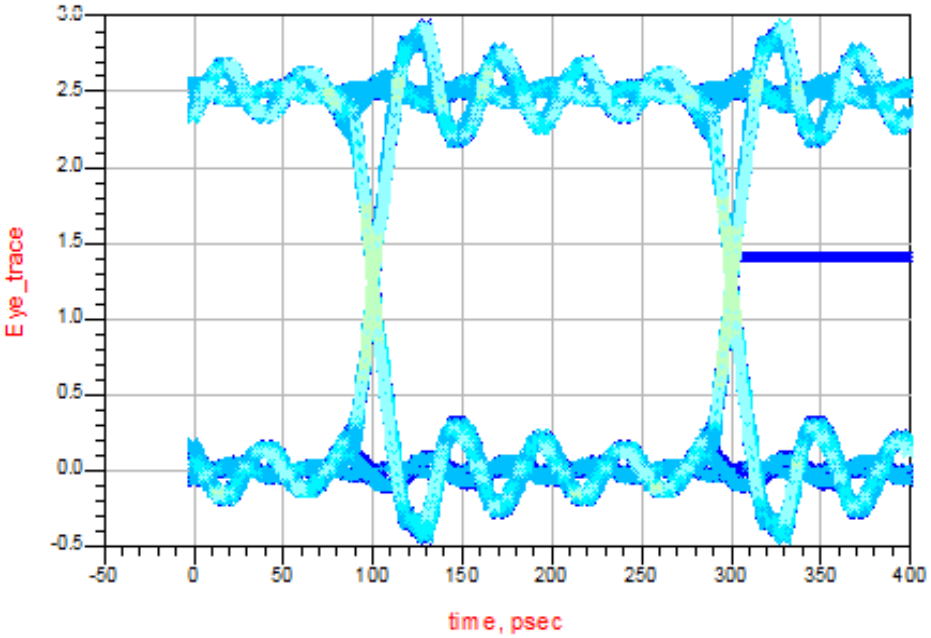


Figure 69. Eye diagram of CPW line (1 mm long) in panel-Si interposer when excited by 5 Gbps pseudo-random bit stream (PRBS).

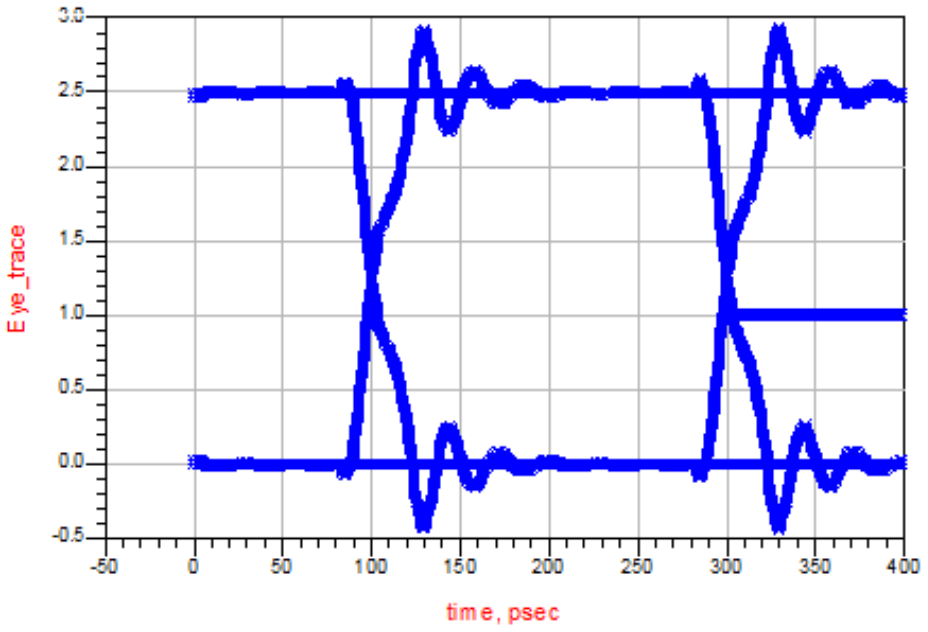


Figure 70. Eye diagram of CPW line (1 mm long) in ENA1 glass interposer when excited by 5 Gbps pseudo-random bit stream (PRBS).

Table 8: Eye diagram parameters of CPW lines.

Parameter	Glass Interposer	Wafer-Si Interposer	Panel-Si Interposer
Eye Height	2.317 V	2.303 V	1.897 V
Jitter (Peak-to-Peak)	0.887 ps	0.887 ps	1.47 ps

The eye diagrams are based on measured data from the fabricated transmission lines. The dimensions of the lines changed during fabrication from the designed values. This changed the characteristic impedance the transmission lines from the designed 50 ohm value. Due to this impedance mismatch, ringing is observed in the eye diagram for glass interposer line.

It is observed from Figure 68, Figure 69, Figure 70, and Table 8 that the glass interposer and the wafer-Si interposer exhibit better eye diagrams as compared to the panel-Si interposer. Although the wafer-Si interposer has higher loss, the insertion loss value changes little beyond 2 GHz. The insertion loss of the panel-Si interposer line increases continuously and almost linearly from DC to 10 GHz. Due to this nature of the insertion loss plot, high-frequency digital signals get more distorted while propagating through a CPW line in panel-Si interposer as compared to wafer-Si interposer.

The transmission line in wafer-Si interposer operates in the slow wave mode in low frequencies and in the dielectric quasi-TEM mode at high frequencies as described in [59]. The transmission line in panel-Si interposer operates in the slow wave mode from DC-10 GHz because of the lower resistivity of panel-Si interposer. The transition frequency between slow-wave and quasi-TEM modes increase with decrease in Si resistivity. Similar trend in the attenuation characteristics of transmission lines on different resistivity Si substrates was also reported in [59].

5.3 Through Package Via

Test structures were designed, fabricated, and measured to characterize the through package vias (TPVs) in silicon and glass interposers. Figure 71 shows the schematic of a typical test structure consisting of CPW lines on the top and bottom surfaces of the interposer connected by two sets of TPVs.

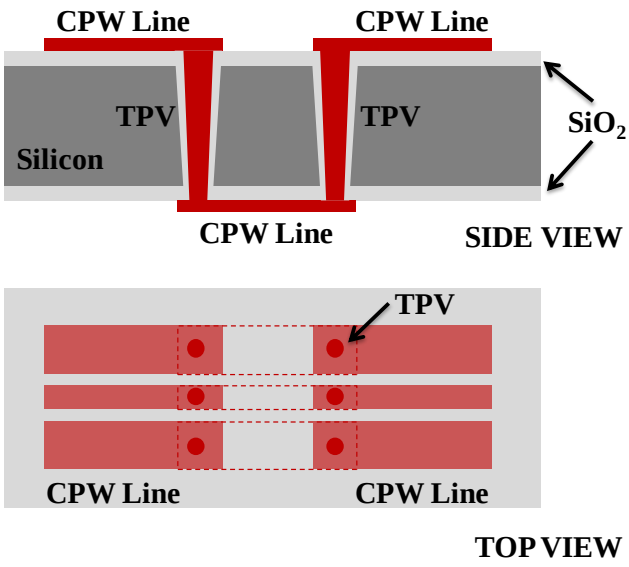
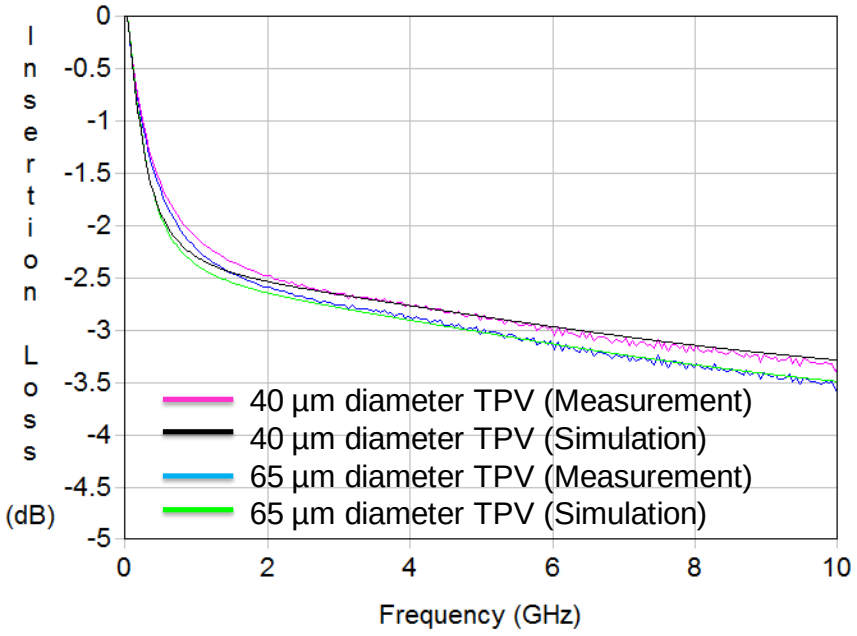
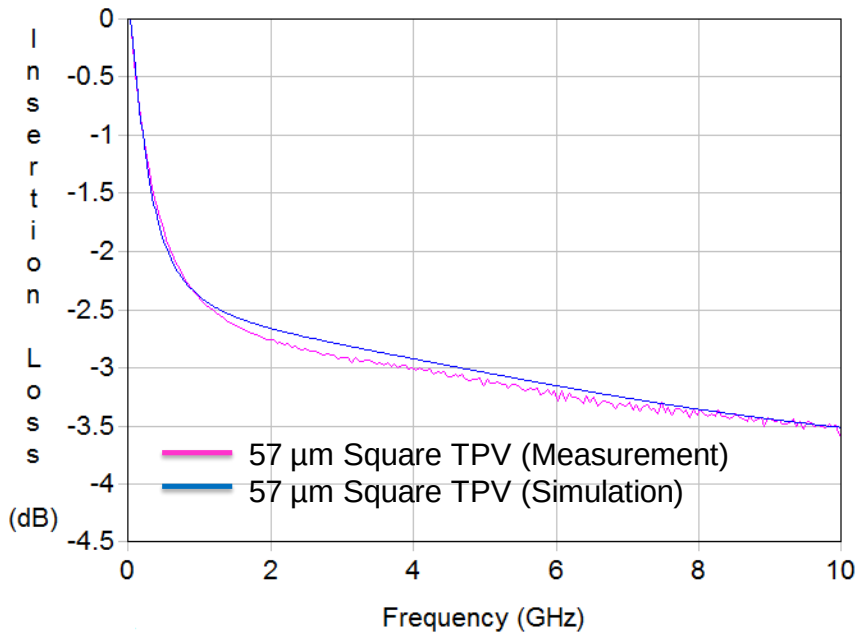


Figure 71. Schematic of a CPW-TPV test structure in Si interposer.



(a)



(b)

Figure 72. Insertion loss plots for CPW-TPV test structures in wafer-Si interposer. (a) TPV with circular cross-section. (b) TPV with square cross-section.

Figure 72 shows the insertion loss plots in wafer-Si interposer for TPVs with circular and square cross-sections. The CPW lines were 1 mm long and 125 µm wide. The gap between the signal and ground was 130 µm. The resistivity and thickness of the Si was 27 Ω-cm and 260 µm respectively. The thickness of the SiO_2 liner on the surface and the via side-wall was 2 µm.

The measured and simulated insertion loss plots match well as seen from Figure 72. Although the square TPV has similar loss as circular TPVs, the latter is preferable due to its better thermo-mechanical reliability. It is also observed that the smaller TPVs have lower loss as compared to the larger TPVs. This can be attributed to the smaller via side-wall capacitance and lower substrate conductance (between the TPVs) of the smaller TPVs. In order to reduce the signal loss it is preferred to have TPVs with small diameters in Si interposers.

CPW-TPV test structures were also designed, fabricated, and measured in panel-Si interposers. The TPVs were circular in cross-section with 50 µm diameter. The CPW lines were 125 µm wide. The gap between the signal and ground was 130 µm. The resistivity and thickness of the Si was 0.15 Ω-cm and 220 µm respectively. The thickness of the ZIF polymer liner on the surface and the via side-wall was 40 µm and 50 µm, respectively. Figure 73 shows the measurement and simulation results for these test structures.

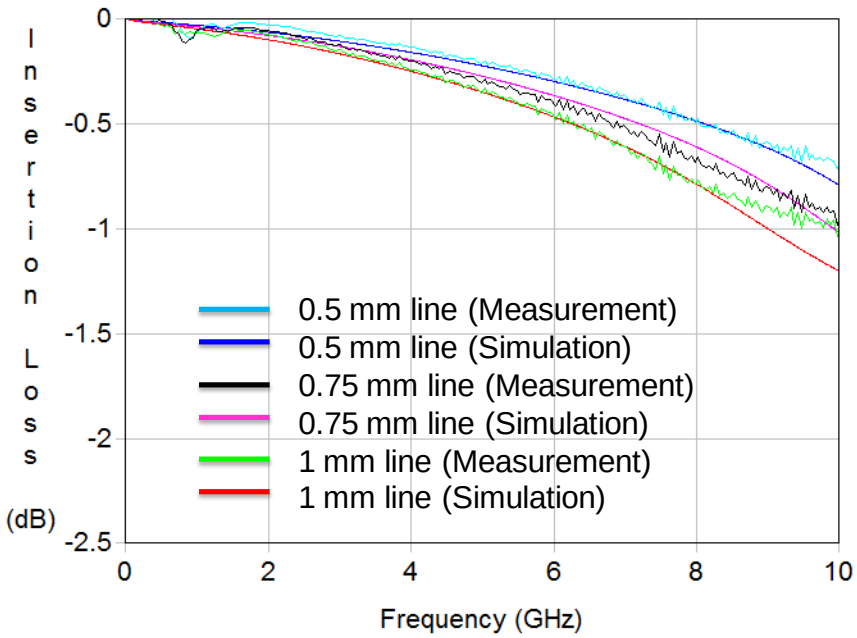


Figure 73. Insertion loss plots for CPW-TPV test structures in panel-Si interposer.

The measured and simulated insertion loss plots match well as seen from Figure 72. As expected, the loss in these test structures increase as the length of the CPW lines is increased from 0.5 mm to 1 mm. The insertion loss of the CPW-TPV structure with 0.5 mm long CPW lines is approximately 0.64 dB at 10 GHz. This test structure consists of two TPV transitions and a total of 1.5 mm of CPW line in the signal path. It is observed from Figure 67 that the loss in the CPW line is approximately 0.18 dB/mm. The loss in each TPV transition can be thus estimated to be 0.19 dB at 10 GHz.

CPW-TPV test structures were designed, fabricated, and measured in three different glass interposers. The first type of glass interposer used 180 µm thick ENA1 glass laminated with 20 µm thick RXP4 polymer. The TPVs were circular in cross-section with 60 µm diameter. The CPW lines were 160 µm wide. The gap between the signal and ground was 36.5 µm. There was no liner on the TPV side-wall.

Figure 74 shows the measurement and simulation results for these test structures. The measurement and simulation results agree well.

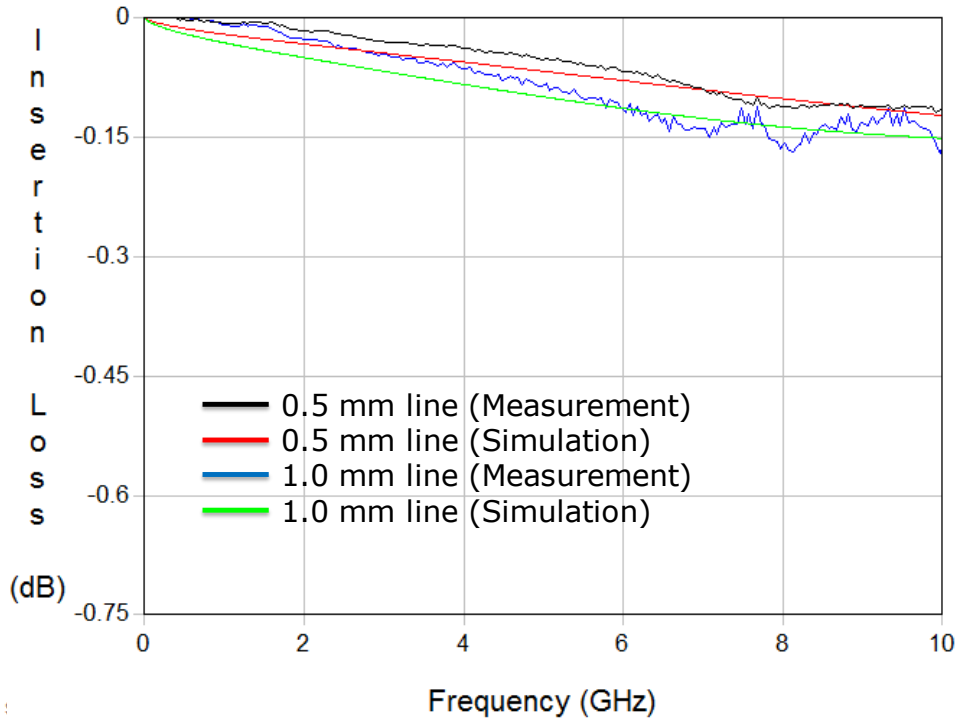


Figure 74. Insertion loss plots of CPW-TPV structures in ENA1 glass interposer with RXP4 polymer coating on surface.

The second type of glass interposer used 180 µm thick ENA1 glass laminated with 17.5 µm thick ZIF polymer. The TPVs were circular in cross-section with 100 µm top diameter and 72 µm bottom diameter. The CPW lines were 160 µm wide and 0.5 mm long. The gap between the signal and ground was 36.5 µm. There was no liner on the TPV side-wall. Figure 75 shows the measurement and simulation results for these test structures. The measurement and simulation results agree well.

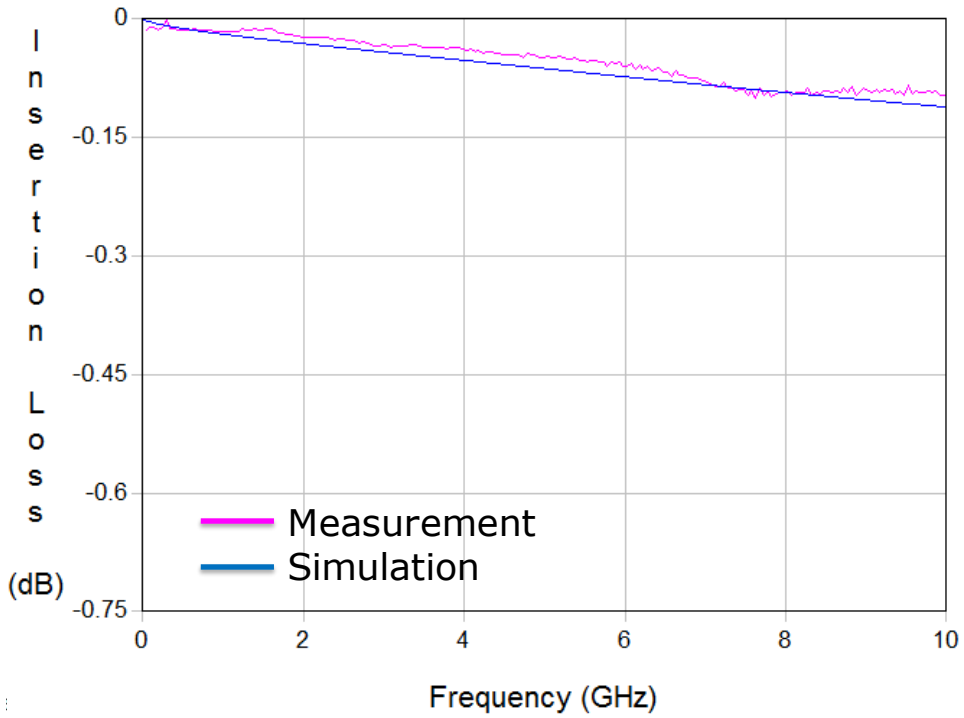


Figure 75. Insertion loss plot of CPW-TPV structure in ENA1 glass interposer with ZIF polymer coating on surface.

The third type of glass interposer used 75 µm thick O211 glass laminated with 20 µm thick RXP4 polymer. The TPVs were circular in cross-section with 40 µm diameter. The CPW lines were 160 µm wide and 1 mm long. The gap between the signal and ground was 36.5 µm. There was no liner on the TPV side-wall. Figure 76 shows the measurement and simulation results for these test structures. The measurement and simulation results agree well.

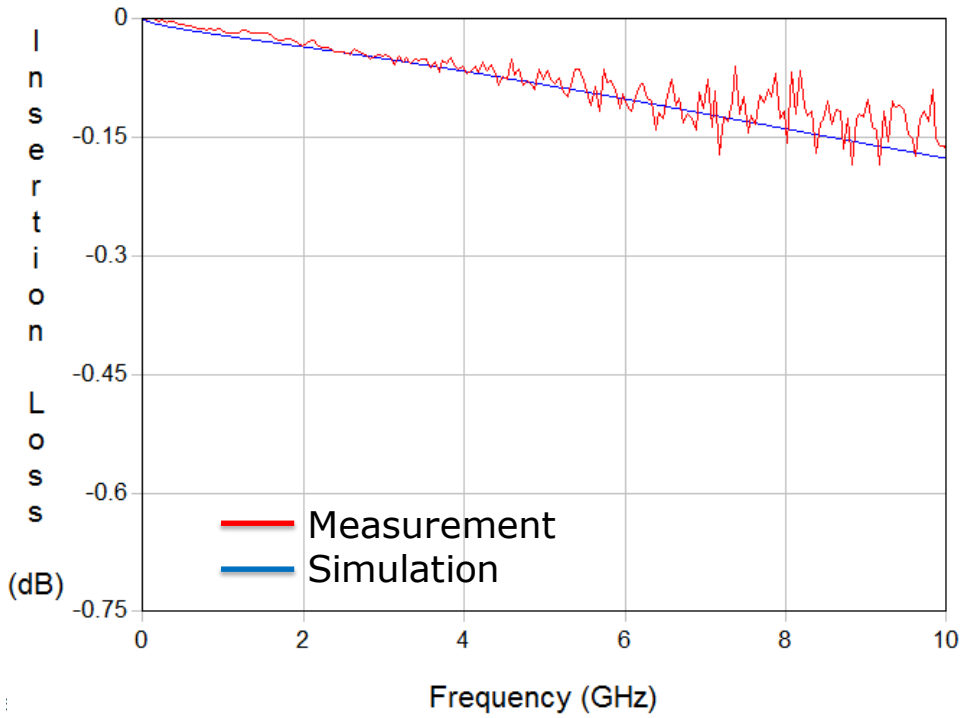


Figure 76. Insertion loss plot of CPW-TPV structure in O211 glass interposer with RXP4 polymer coating on surface.

The CPW-TPV interconnection structures in glass interposers (Figure 74, Figure 75, and Figure 76) have much lower insertion loss as compared to those in panel-Si and wafer-Si interposers (Figure 72 and Figure 73). This difference is due to the higher resistivity of glass as compared to silicon. It is observed from Figure 72 and Figure 73 that the insertion loss of the CPW-TPV structure in panel-Si interposer (1 mm CPW line) is smaller as compared with that in wafer-Si interposer. This can be attributed to the thick polymer liner in the panel-Si interposer.

5.4 Power and Ground Planes

Power and ground plane cavity structures were designed and fabricated in two-metal layer test vehicles in glass interposers and panel-Si interposers. The planes were 25 mm by 25 mm in dimension. The resistivity and thickness of the Si was 0.15 Ω-cm and 220 µm, respectively. The thickness of the ZIF polymer liner on the surface and the via side-wall was 40 µm and 50 µm, respectively. Three types of glass interposers, as described in Section 5.2 and Section 5.3 were used. Figure 77 plots the measured impedance curves of these cavity structures.

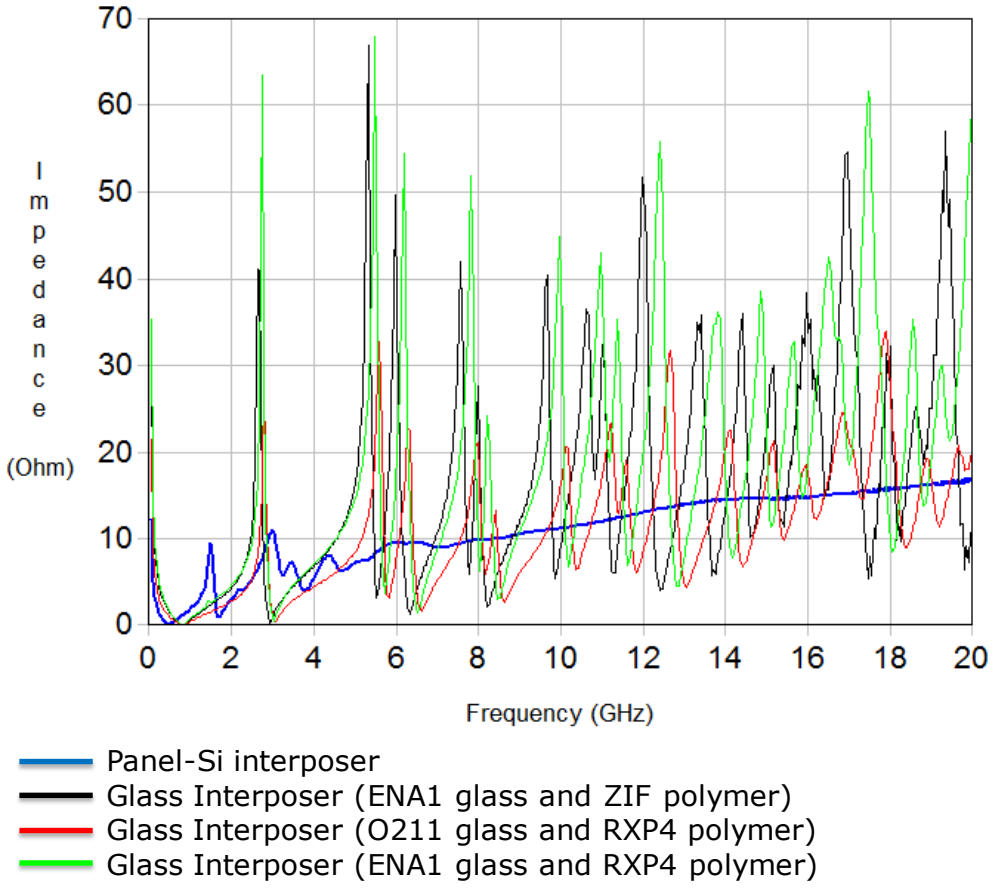


Figure 77. Measured impedance plots of glass interposers and panel-Si interposers.

It is observed that the panel-Si interposer has lower impedance as compared to the glass interposers. The Si interposer impedance curve is also mostly devoid of significant peaks which are present in the glass interposer plots. As explained in Section 4.2, this difference is due to the large difference in electrical conductivity between glass and Si. The thin glass interposer (75 µm thick O211 glass) has higher capacitance between the plane pairs. This leads to its lower impedance as compared to the other glass interposers.

5.5 Conclusion

This chapter presented measurement results of interconnection structures in wafer-Si interposers, panel-Si interposers, and glass interposers. The measurement results correlated well with simulation results thus validating the modeling and simulation work. The interconnection behavior was compared between the different interposers. Interconnections in glass interposers have good electrical performance. CPW lines in wafer-Si interposers are capable of handling high-speed digital signals with nominal distortion. The measured power-delivery network impedance in panel-Si interposers is lower than that in glass interposers.

CHAPTER 6

NANO-COPPER INTERCONNECTIONS

This chapter presents design and characterization of nano-structured copper-based (Nano-Cu) ultra-fine pitch chip-to-interposer interconnections for microwave frequencies. High-frequency performance of Nano-Cu interconnections (with dimension in the order of 15 to 0.5 µm) is studied for chip-on-interposer and chip-on-chip configurations (Figure 78 and Figure 79). Physical and material parametric studies (such as interconnection material, shape, dimension, and number of ground bumps) are performed on this interconnection by means of full-wave electromagnetic (EM) simulations. This chapter also presents important interconnection and package design guidelines (obtained from the parametric analysis) for the Nano-Cu interconnection.

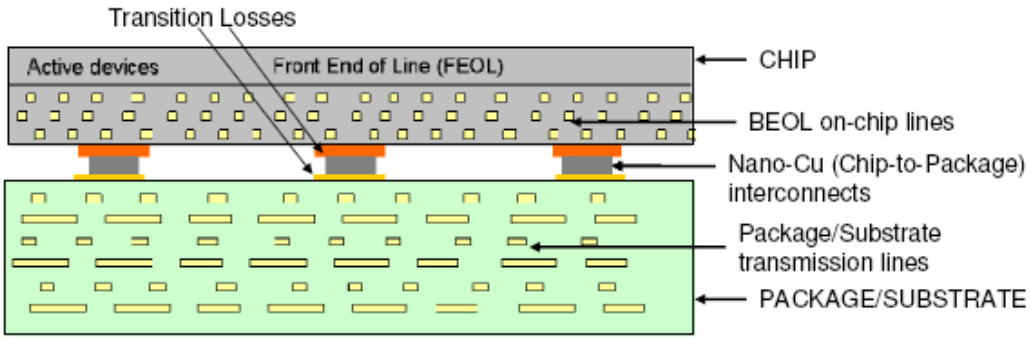


Figure 78. Cross-section view of a chip-on-interposer configuration with nano-copper interconnections.

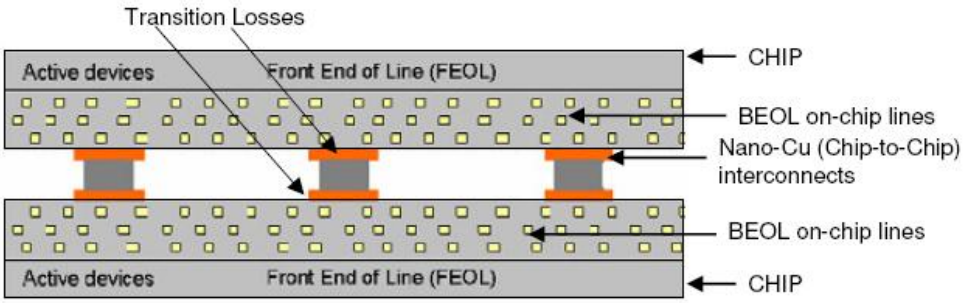


Figure 79. Cross-section view of a chip-on-chip configuration with nano-copper interconnections.

6.1 Modeling and Simulations

6.1.1 Electromagnetic Modeling

The interconnection wiring on the chip and interposer was modeled as microstrip lines. For the on-chip BEOL lines, the simulations were performed with the 65 nm node [60] BEOL line dimensions. Microstrip lines were modeled as lines in the last layer of metallization (M8 layer in Intel's 65 nm node). BCB (ε_r = 2.65) was used as a low-k interposer substrate material. Carbon-doped Oxide (ε_r = 2.6) was used as on-chip inter-metal layer dielectric material in the 65 nm node BEOL line models (Figure 80). Ansoft HFSS was used as a 3D full-wave EM simulator to study the system response.

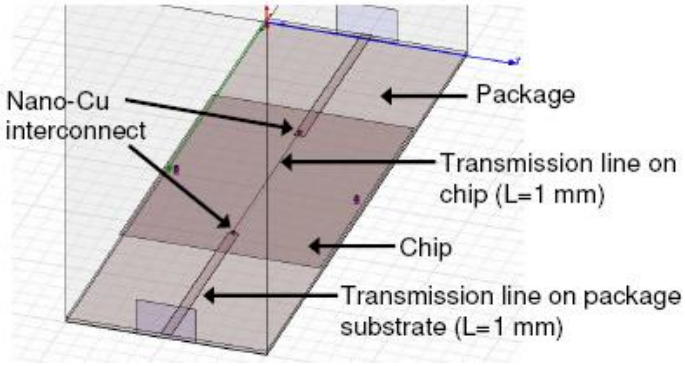


Figure 80. HFSS model for a chip-on-interposer configuration with nano-copper interconnection.

6.1.2 Comparison with Flip-chip Bumps

The Nano-Cu interconnection (15 µm diameter and height) was compared with traditional solder ball flip-chip bump as well as with gold-stud bumps for interfacing a 65 nm node chip to an organic interposer. Figure 81 shows the cross-sectional view, and Figure 82 shows the S-parameter system response of the structures. It is seen that the Nano-Cu interconnection offers approximately 0.4 dB lower insertion loss as compared to the other interconnections at 20 GHz.

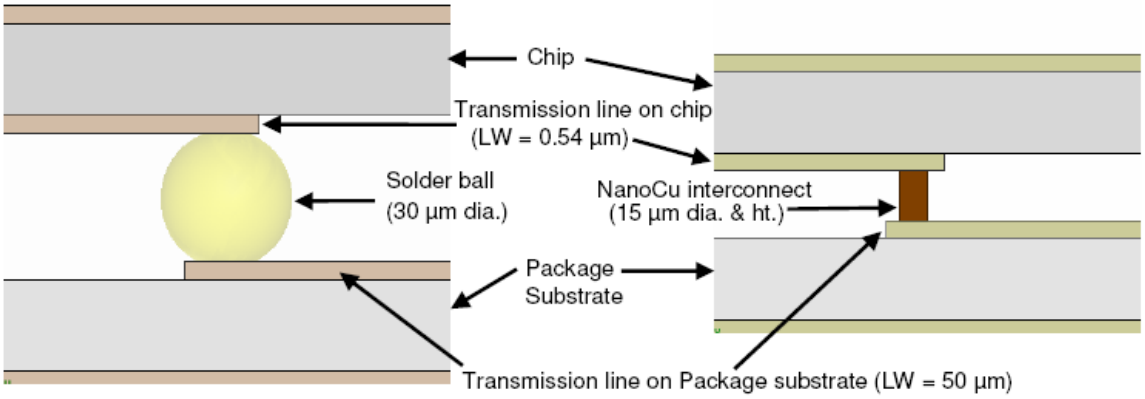


Figure 81. A comparison between traditional solder ball flip-chip and nano-copper interconnection.

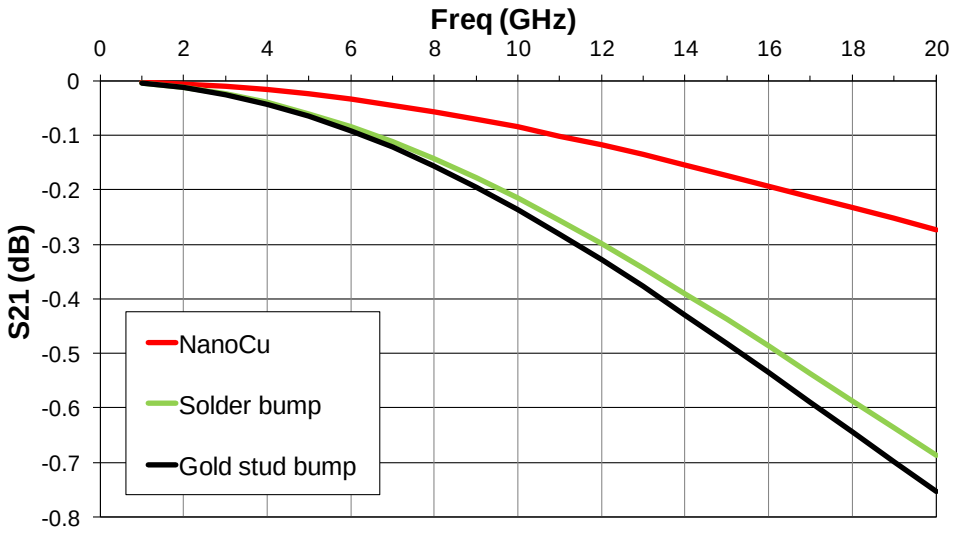


Figure 82. The effect of interconnection material on signal transmission.

6.2 Parametric Study

Different parametric studies were performed with Nano-Cu interconnection such as (i) Interconnection shape (cylindrical, conical, and spherical), (ii) Interconnection dimension (diameter and height – from 30 µm to 0.5 µm), and (iii) Number of ground bumps.

6.2.1 Interconnection Shape

Figure 83 shows the chip-on-interposer system response with on-chip and package microstrip lines connected by Nano-Cu interconnection of different shapes. The spherical Nano-Cu interconnections are seen to have approximately 0.1 dB lower insertion loss than the cylindrical and conical Nano-Cu interconnections.

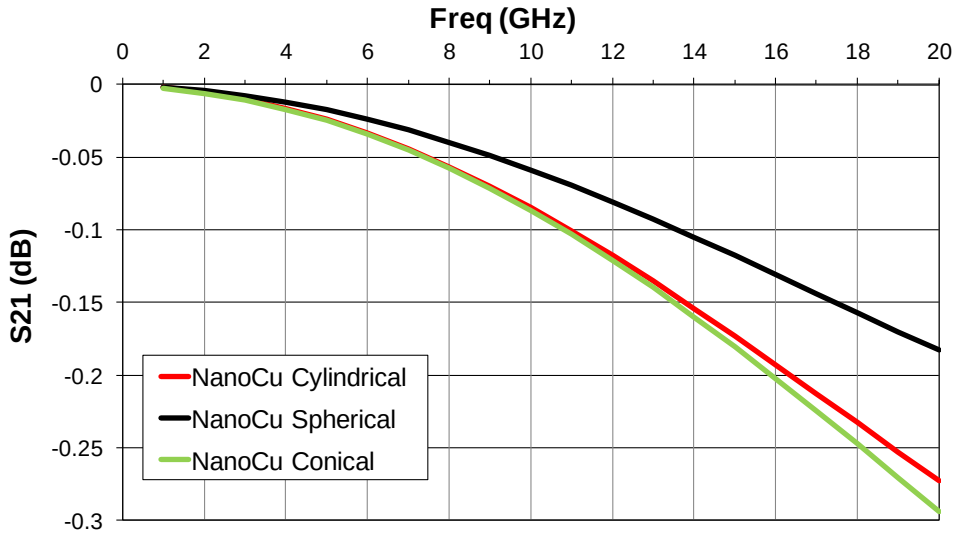


Figure 83. The effect of shape of nano-copper interconnections on system response in a chip-on-interposer configuration.

6.2.2 Interconnection Dimension

The parametric study on the interconnection dimension was carried out for both - chip-on-chip and chip-on-interposer configurations. The chip-on-chip structures (Figure 79) models the Nano-Cu interconnection performance in a 3D face-to-face chip stack as well as in silicon interposer applications. In this configuration, two 65 nm chips are connected face-to-face by the Nano-Cu interconnections. Nano-Cu interconnections of different dimensions from 0.5 μm to 15 μm (diameter and height) were studied along with a 30 μm diameter solder bump for these packaging configurations.

The best response for chip-on-interposer configuration is observed in the model with Nano-Cu bump of 5 µm diameter and height (Figure 84). There are two transitions to the bump in this structure. One is from the transmission line on chip (LW = 0.54 µm) to the bump, and the other one is from bump to the transmission line on package substrate (LW = 50 µm). As the dimension (diameter and height) of the bump is reduced from 30 µm to 0.5 µm, the dimensional mismatch between the on-chip transmission line and the bump decreases, but the mismatch between the interposer transmission line and the bump increases. So the signal scattering at the chip-to-bump interface decreases whereas the scattering at the interposer-to-bump interface increases.

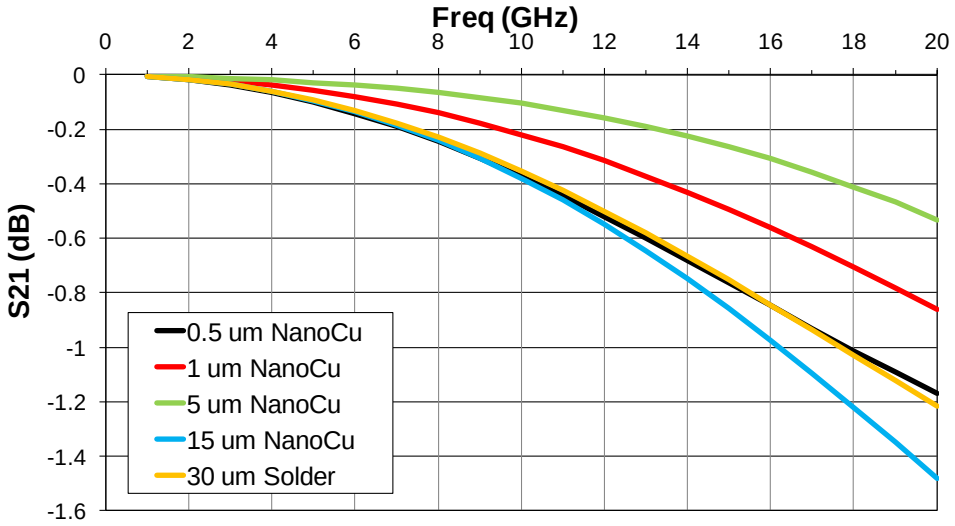


Figure 84. A parametric study on the dimensions (diameter and height) of the nano-copper interconnections in a chip-on-interposer configuration.

The transitions in a chip-on-chip system are from the transmission line on chip to the bump. As the dimension (diameter and height) of the bump is reduced from 30 µm to 0.5 µm, the dimensional mismatch between the line and the bump decreases. This leads to less signal scattering at the interface region. Therefore lower losses are observed in the simulations with smaller bumps, the best system response being the one with Nano-Cu interconnections of 0.5 µm diameter and height (Figure 85).

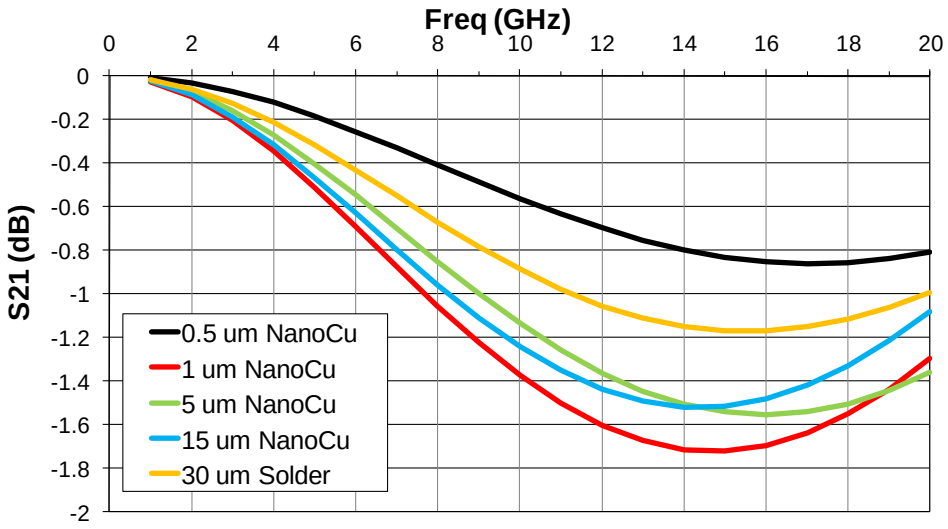


Figure 85. A parametric study on the dimensions (diameter and height) of the nano-copper interconnections in a chip-on-chip configuration.

The resonance observed in Figure 85 is caused due to the parasitic inductance of the chip-to-chip interconnection.

6.2.3 Number of Ground Connections

The number of ground vias/bumps connecting the chip and package ground planes (with transmission lines on interposer and chip modeled as microstrip lines) in a chip-on-interposer configuration was varied to observe its effect on the system response.

The chip-to-interposer interconnections used in this parametric study were Nano-Cu interconnections (15 µm diameter and height). It is observed from Figure 86 that the system response greatly improves by increasing the number of ground via/bump connections.

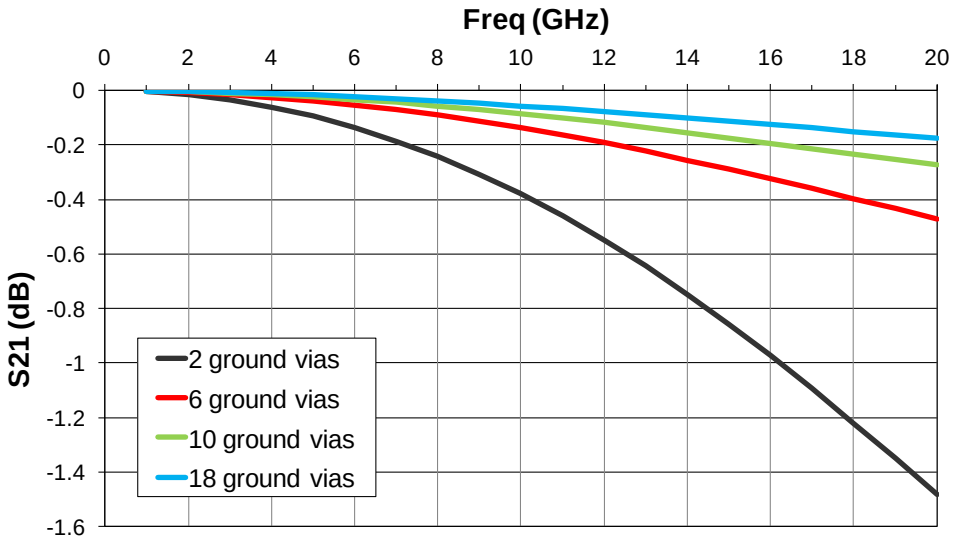
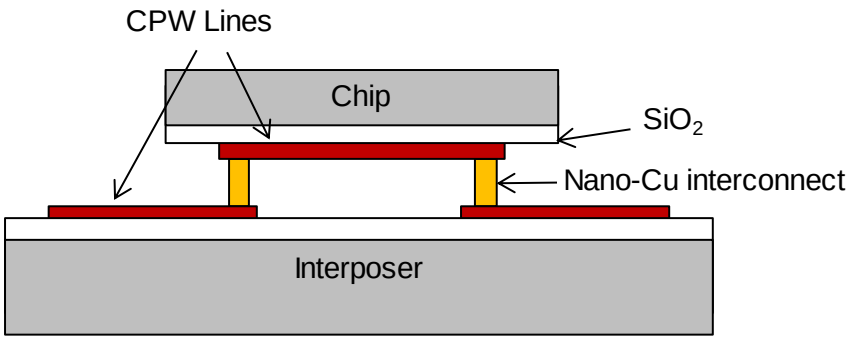


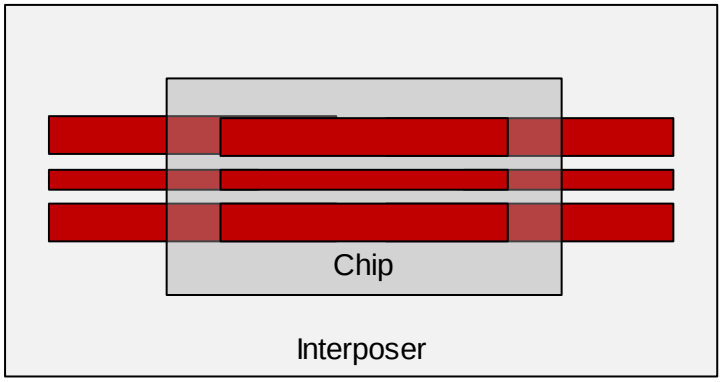
Figure 86. System response variations due difference in the number of ground bumps/vias connections in a chip-on-interposer configuration.

6.3 Test Vehicle Design and Measurement

A test vehicle was designed, fabricated, and measured to validate the simulation results by model-to-measurement correlation. The test vehicle consisted of a silicon test chip assembled on a silicon interposer using (15 µm diameter) Nano-Cu interconnections. The wiring on the chip and the silicon interposer consisted of 15 µm wide co-planar waveguide (CPW) lines. Figure 87 (a) and (b) shows the schematic view of the designed test vehicle.



(a)



(b)

Figure 87. Schematic view of Test Vehicle. (a) Side view, (b) Top view.

The Test Vehicle was fabricated and the models were validated by frequency-domain measurements till 20 GHz. The test vehicle measurements were performed using a two-port vector network analyzer (VNA) from Agilent Technologies. SOLT calibration was performed prior to measurements.

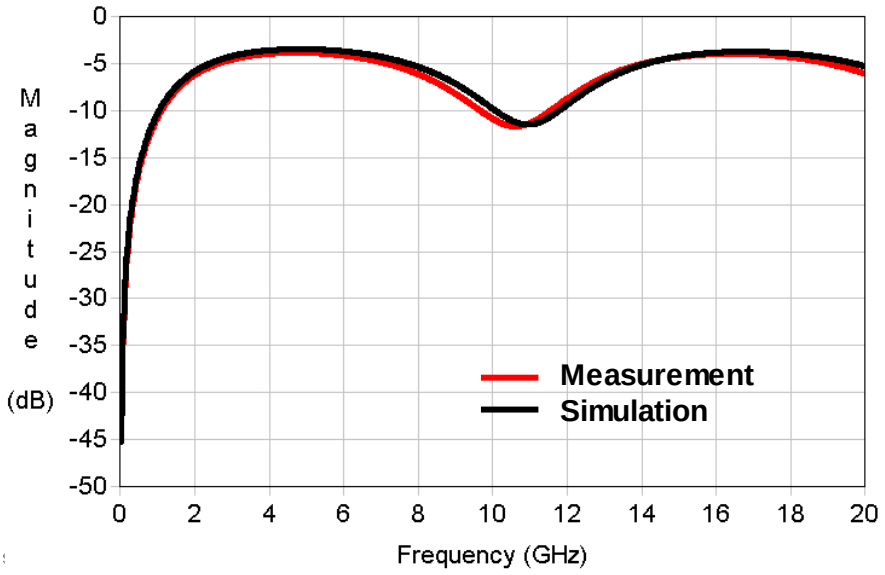


Figure 88. Return loss comparison between measurement and simulation results.

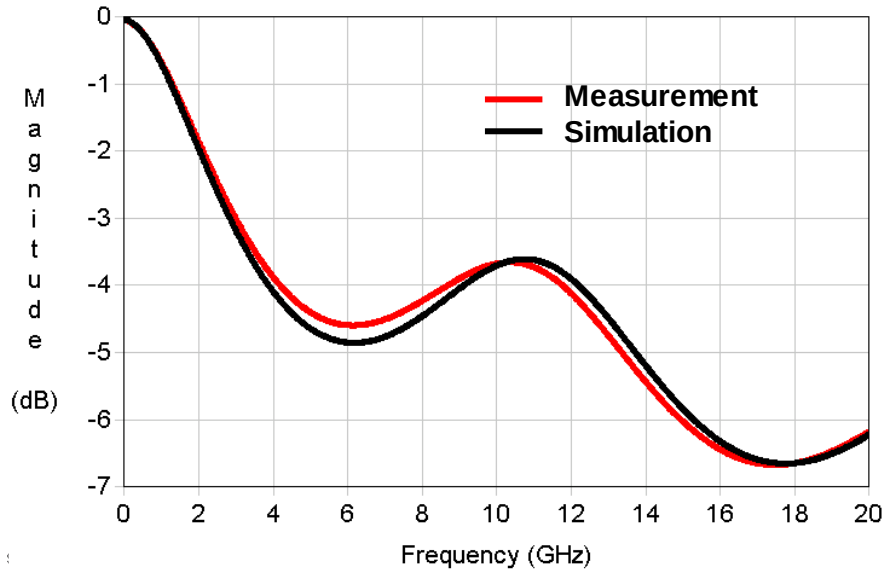


Figure 89. Insertion loss comparison between measurement and simulation results.

Figure 88 and Figure 89 show the correlation between simulation and measurement results. The close match between the measured and simulated results validates the modeling and simulation work presented in this chapter.

6.4 Conclusion

In this chapter, Nano-Cu chip-to-interposer interconnections were studied for their electrical performance, and compared with traditional chip-to-interposer interconnections. Nano-Cu interconnections exhibit much better high-frequency response as compared to conventional flip-chip bumps in chip-on-chip and chip-on-interposer configurations. Nano-Cu interconnections offer approximately 0.4 dB lower insertion loss, as compared to flip-chip solder bumps and Au-stud interconnections. Further, Nano-Cu interconnections exhibit 0.6 dB lower insertion losses in chip-on-interposer applications, and 0.2 dB lower insertion losses in chip-on-chip applications, as compared to solder bumps. The simulation results were validated by close measurement-to-model correlation.

CHAPTER 7

CONCLUSIONS

The main drivers for consumer electronics are miniaturization, enhanced functionality, and reduced cost. In the last few decades, this has been made possible by on-chip transistor scaling following Moore's Law. There are several barriers which are now being forecasted for transistor scaling beyond 22 nm. Some of these barriers are increased power requirements, limited performance enhancements, difficulty in integrating heterogeneous technologies, and expensive wafer fabrication facilities.

To mitigate some of these challenges, 3D ICs are being developed. There are several potential benefits of 3D ICs - low interconnection latency, low power consumption, increased bandwidth, reduced form factor, the ability to integrate heterogeneous technologies, and yield improvement (compared to system-on-chip). The 3D ICs are the active components of a system. Typically, the actives form a small part (about 10 %) of the electronic system [61]. There is an important need to develop 3D interposer technologies which are capable of supporting the interconnection requirements of 3D ICs and miniaturizing the size of the system.

In the last five chapters, this dissertation focused on the modeling, design, and characterization of the interconnections in 3D interposers. The power-delivery and signal-delivery networks in Si and glass interposers were also modeled and simulated. Design guidelines were presented based on the simulation and measurement results.

The extensive comparison between the performance of different types of silicon and glass interposers that was presented in this dissertation can be summarized as following:

(a) Co-planar waveguide (CPW) lines:

1. The insertion loss of CPW lines in glass interposers (0.06 dB/mm at 10 GHz) is less than that in Si interposers (Figure 67). The CPW line in panel-Si interposer has less loss (0.18 dB/mm at 10 GHz) as compared to that in wafer-Si interposer (1.16 dB/mm at 10 GHz).
2. The eye diagram is better for CPW lines in wafer-Si interposer as compared to that in panel-Si interposer because of the slope of its insertion loss plot (Table 8).

(b) Through package vias (TPVs):

1. Glass TPVs do not have the MOS capacitance which is observed in Si TPVs (with the Si biased). The MOS capacitance effect becomes less significant with increase in the via side-wall liner thickness. For a 30 μm diameter Si TPV, the MOS effect becomes negligible when the liner thickness becomes greater than 1 μm. The MOS capacitance is minimal for TPVs in panel-Si interposers for this reason.
2. The insertion loss of TPV in panel-Si interposer is less than that in wafer-Si interposer (approximately 1 dB lower loss at 10 GHz as shown in Figure 25). The insertion loss of TPV in glass interposer is less than that in panel-Si interposer (approximately 0.5 dB lower loss at 10 GHz as shown in Figure 34).

3. The crosstalk between TPVs in panel-Si interposer is less than that in wafer-Si interposer at low frequencies (below 8 GHz as shown in Figure 26). The crosstalk between TPVs in glass interposer is less than that in panel-Si interposer (approximately 20 dB less crosstalk at 10 GHz as shown in Figure 36).
4. The insertion loss in Si TPVs (both wafer-Si and panel-Si) decrease with decrease in via diameter (0.2 dB lower loss when diameter is changed from 60 µm to 30 µm as shown in Figure 29). The insertion loss in glass TPVs increase with decrease in via diameter (0.2 dB higher loss when diameter is changed from 100 µm to 35 µm as shown in Figure 37).
5. The crosstalk between TPVs (in Si and glass interposers) decreases with decrease in via diameter (when the TPV pitch is kept unchanged). The crosstalk reduces by approximately 10 dB at 10 GHz when the diameter of the TPV in panel-Si is reduced from 60 µm to 30 µm (Figure 30). The crosstalk reduces by approximately 5 dB at 10 GHz when the diameter of the TPV in glass interposer is reduced from 100 µm to 35 µm (Figure 38).
6. The insertion loss of Pd-lined Cu TPVs and conformal Cu TPVs are similar to those of filled Cu TPVs. The difference is less than 0.01 dB at 10 GHz (Figure 49 and Figure 51).

(c) CPW-TPV signal paths:

1. The measured insertion loss of CPW-TPV signal paths (Figure 71) is lower in glass interposers (typically < 0.2 dB at 10 GHz) as compared to wafer-Si interposers (approximately 3.5 dB at 10 GHz) and panel-Si interposers (approximately 1 dB at 10 GHz).
2. The measured insertion loss plot in wafer-Si interposers (Figure 72) has a smaller slope when compared with panel-Si interposers (Figure 73) beyond 2 GHz.

(d) Microstrip line (MSL) - TPV signal paths:

1. Signal paths in wafer-Si and panel-Si interposers comprising of MSL-TPV transitions (Figure 31) have a smooth insertion loss plot till 10 GHz without any plane resonance effects (Figure 32). The insertion loss plot of similar signal paths in glass interposers show significant plane resonance effects (Figure 43). These effects are comparatively less for glass interposers with smaller thickness and higher permittivity.
2. The insertion loss of MSL-TPV signal paths is higher (by approximately 6 dB at 10 GHz as shown in Figure 32) in wafer-Si interposer as compared to panel-Si interposer because of the difference in via side-wall liner thickness.

(e) Power delivery network (PDN):

1. The MOS capacitance of Si TPVs helps in reducing the PDN impedance in Si interposers with thin (<1 μm) side-wall liner (Figure 54), when the Si substrate is biased. This decoupling effect is not observed in unbiased Si interposers, Si

interposers with thick side-wall liner, and glass interposers. The additional decoupling capacitance provided by the MOS capacitance of Si TPVs (in the test case presented in Section 4.1) was estimated to be 2 nF.

2. Power-ground plane resonances are suppressed in Si interposers (Figure 77). In contrast, plane resonances are observed in glass interposers. The difference is because Si has much lower resistivity (approximately 0.1-100 Ω-cm) as compared to glass (approximately 10^{10} Ω-cm). Glass interposers with smaller thickness and higher permittivity have smaller resonance peaks in their PDN impedance plots.

The following section clarifies the contributions of this dissertation. Section 7.2 suggests possible extensions to this dissertation as future work. The final section presents a list of publications and awards received in the course of this dissertation research.

7.1 Contributions

7.1.1 Accurate Equivalent Circuit-Model of Si TPVs

Modeling the voltage-dependent MOS capacitance effect is important for accurate electrical modeling of Si TPV. This dissertation presented an in-depth study of the semiconducting and biasing effects in silicon interposers.

- The MOS capacitance of Si TPVs was accurately modeled for the first time by numerically solving Poisson's equation in cylindrical co-ordinates. An equivalent circuit-model of the Si TPV was developed. The results correlated well with measurement data to validate the model.

- Parametric studies demonstrated that the Si TPV capacitance can be tuned by varying different physical and material parameters. Design guidelines were proposed for designing Si TPVs in the signal and power-delivery networks as well as for Si TPVs in variable-capacitor applications.
- Low-loss Si TPVs were designed by utilizing the depletion region to reduce the dielectric loss in silicon.

7.1.2 Power Delivery Network Design in Silicon and Glass Interposers

The power-delivery network (PDN) in silicon and glass interposers was modeled, simulated, and compared in this dissertation. It is important to model the MOS capacitance of Si TPVs for PDN simulations in 3D systems.

- Si TPVs can be utilized as decoupling capacitors in 3D power-delivery networks by biasing the silicon substrate. The MOS capacitance of Si TPVs helps in decoupling the PDN.
- To achieve lower power noise, the Si substrate should be biased with the Si TPVs operating in the accumulation region.
- The PDN impedance of glass interposers can be made similar to that of Si interposers by increasing the on-chip decoupling capacitance or by adding appropriate decoupling capacitors in the glass interposer.

7.1.3 Modeling, Design, Characterization and, Signal Integrity Analysis of Glass and Silicon Interposers

This dissertation presented the signal integrity analysis of different types of glass and silicon interposers. The interconnections in the interposer were modeled, designed, and characterized. The measurement results correlated well with simulation results thus validating the modeling and simulation work.

- The performance of TPVs in panel-based polycrystalline Si (with thick polymer liner) is better as compared to that of wafer-based CMOS-grade Si (with thin SiO_2 liner).
- TPVs in glass interposer have lower electrical signal loss and crosstalk as compared with TPVs in silicon interposer. The electrical performance of glass TPVs can be improved by increasing its diameter. The electrical performance of the Si TPVs can be improved by decreasing its diameter and by increasing the sidewall liner thickness.
- The measured power-delivery network impedance in panel-Si interposers was lower than that in glass interposers. Power-ground plane resonances are suppressed in Si interposers because of high substrate conductivity. This causes a (mostly) smooth insertion loss curve for signal paths passing through microstrip lines and TPVs. A high-speed digital signal propagating through such paths is expected to have smaller distortion and jitter.
- CPW lines in wafer-Si interposers are capable of handling high-speed digital signals with nominal distortion.
- In glass interposers, signal paths comprising of CPW lines and TPVs have better electrical behavior than those comprising of MSLs and TPVs. The difference is mainly caused by the power-ground plane resonances in the latter scenario. Careful

power delivery design in glass interposers using appropriate choice and location of decoupling capacitors is required to solve the power-ground plane resonance issues.

- The choice of glass and polymer material has little effect on the electrical performance of glass TPVs. However, the power-ground plane resonances in glass interposers depend on the permittivity of the glass and polymer materials.
- Current density simulations indicate that the peak current densities in the TPVs and interconnection lines are well within the current carrying limits of the interconnection material.
- The electrical performance of TPVs designed for better thermo-mechanical reliability (like Pd-lined TPVs and conformally filled TPVs) was similar to the conventional, fully filled TPVs.

7.1.4 Modeling, Design, and Characterization of Nano-Cu Interconnections

This dissertation studied and compared the electrical performance of Nano-Cu chip-to-interposer interconnections with traditional chip-to-interposer interconnections.

- Nano-Cu interconnections offers approximately 0.4 dB lower insertion losses, as compared to flip-chip solder bumps and Au-stud interconnections.
- Nano-Cu interconnections exhibit 0.6 dB lower insertion losses in chip-on-interposer applications, and 0.2 dB lower insertion losses in chip-on-chip applications, as compared to solder bumps.
- The simulation results correlated well with measurement results.

7.2 Future Work

The research work presented in this dissertation can be extended in the future to complete the following tasks:

1. The MOS capacitance analysis of a non-uniformly doped Si substrate can be performed as a continuation of this research work.
2. The effect of generation-recombination on the C-V curve of a Si TPV can be studied in detail as part of a future work.
3. The effect of multi-point, multi-level biasing in Si interposers will be an interesting extension of the analysis presented in this dissertation.
4. Novel and useful tunable RF filters can be designed in Si interposers by using the MOS capacitance of Si TPVs.
5. Clock-delivery network can be designed to supply synchronized clock signal to the chips in a 3D IC stack by utilizing the voltage-dependent capacitance of Si TPVs.
6. The modeling, design, interconnection routing, and characterization of a complete, functional 3D interposer.
7. Test structures can be designed, fabricated, and measured to study the following:
    a. Loss in co-axial Si TPVs
    b. PDN impedance in wafer-Si interposer
    c. Current density in the interconnections
    d. Electrical performance of microstrip line to TPV transition in a four-metal-layer interposer.

7.3 Publications

7.3.1 Book Chapters

[1] R. Tummala and T. Bandyopadhyay, “Introduction to the System-on-Package (SOP) Technology”, in *Introduction to System-On-Package (SOP): Miniaturization of the Entire System*, Edited by Rao Tummala & Madhavan Swaminathan. 1st Edition (May 2008). McGraw-Hill Professional, New York.

[2] B-W. Lee, T. Bandyopadhyay, C.K. Yoon, R. Tummala & K.M. Brown, “Stacked ICs and Packages (SIP)”, in *Introduction to System-On-Package (SOP): Miniaturization of the Entire System*, Edited by Rao Tummala & Madhavan Swaminathan. 1st Edition (May 2008). McGraw-Hill Professional, New York.

7.3.2 Refereed Journal Articles

[1] T. Bandyopadhyay, K. J. Han, D. Chung, R. Chatterjee, M. Swaminathan, and R. Tummala, "Rigorous Electrical Modeling of Through Silicon Vias (TSV) with MOS Capacitance Effects," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 1, pp. 893-903, 2011.

[2] T. Bandyopadhyay, V. Sukumaran, V. Sundaram, M. Swaminathan, and R. Tummala, “Modeling and Characterization of Panel-based Glass and Silicon Interposers,” To be submitted to the *IEEE Transactions on Components, Packaging and Manufacturing Technology*.

[3] K. J. Han, M. Swaminathan, and T. Bandyopadhyay, "Electromagnetic Modeling of Through-Silicon Via (TSV) Interconnections Using Cylindrical Modal Basis Functions," *IEEE Transactions on Advanced Packaging,* vol. 33, pp. 804-817, 2010.

[4] V. Sridharan, M. Swaminathan, and T. Bandyopadhyay, “Enhancing Signal and Power Integrity using Double Sided Silicon Interposer,” Submitted to the *IEEE Microwave and Wireless Components Letters*.

[5] V. Sukumaran, T. Bandyopadhyay, V. Sundaram, and R. Tummala, “Low-cost, Ultra-thin and Ultra-high I/O Density Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of ICs and 3D ICs,” Submitted to the *IEEE Transactions on Components, Packaging and Manufacturing Technology*.

[6] Q. Chen, T. Bandyopadhyay, Y. Suzuki, F. Liu, V. Sundaram, R. Pucha, M. Swaminathan, and R. Tummala, “Modeling, Fabrication, and Characterization of Low-cost, Panel-based Polycrystalline Silicon Interposer with Through-Package-Vias (TPVs),” To be submitted to the *IEEE Transactions on Components, Packaging and Manufacturing Technology*.

[7] G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, S. Lim, and R. Tummala, "An Interposer approach with Ultra-high IO Density Glass and Silicon for High BW mobile applications,” To be submitted to the *IEEE Transactions on Components, Packaging and Manufacturing Technology*.

7.3.3 Conference Publications

[1] T. Bandyopadhyay, R. Chatterjee, D. Chung, M. Swaminathan, & R. Tummala, "Electrical modeling of annular and co-axial TSVs considering MOS capacitance effects," in *2009 IEEE 18th Conference on Electrical Performance of Electronic Packaging and Systems. EPEPS 2009, 19-21 Oct. 2009*, Portland, OR, USA, 2009, pp. 117-20.

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7.3.4 Awards

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