Development of III-Nitride Bipolar Devices: Avalanche Photodiodes, Laser Diodes, and Double-Heterojunction Bipolar Transistors

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Development of III-Nitride Bipolar Devices: Avalanche Photodiodes, Laser Diodes, and Double-Heterojunction Bipolar Transistors

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii

LIST OF TABLES vii

LIST OF FIGURES viii

NOMENCLATURE xiii

SUMMARY xvii

CHAPTER 1: INTRODUCTION TO III-NITRIDE MATERIALS AND DEVICES 1
- 1.1 Group III-Nitride Materials Properties and Applications 1
- 1.2 GaN Deep-Ultroviolet *p-i-n* Avalanche Photodiodes 4
- 1.3 InGaN/GaN-Based Laser Diodes 8
- 1.4 GaN/InGaN *npn* Double-Heterojunction Bipolar Transistors 12
- 1.5 Scope of this Dissertation 16

CHAPTER 2: DEVELOPMENT OF GAN ULTRAVIOLET AVALANCHE PHOTODIODES 17
- 2.1 Basic Device Physics 18
- 2.2 Epitaxial Material Layer Structure 20
- 2.3 Device Fabrication 21
  - 2.3.1 Fabrication Process Flow 21
  - 2.3.2 UV-assisted Wet-Etching Surface Treatment 22
  - 2.3.3 Ohmic Contact Study on *p*-GaN 28
  - 2.3.4 Ohmic Contact Study on *n*-GaN 29
- 2.4 Device Characterization 30
  - 2.4.1 Responsivity 30
  - 2.4.2 Photo Current Avalanche Gain 33
  - 2.4.3 Geiger-Mode Operation 35
  - 2.4.4 Effective Detectivity 38
- 2.5 Summary 42

CHAPTER 3: DEVELOPMENT OF INGAN-BASED LASER DIODES 43
- 3.1 Basic Device Physics 43
- 3.2 Device Fabrication 47
  - 3.2.1 Fabrication Process Flow 48
  - 3.2.2 Optimization of Ohmic Contact to *p*-GaN 49
- 3.3 Effects of a Step-Graded $Al_xGa_{1-x}N$ Electron Blocking Layer 50
  - 3.3.1 LD Structures and Simulations 52
  - 3.3.2 Threshold Current Density and Lasing Wavelength 56

3.3.3 Internal Quantum Efficiency 58
3.3.4 Temperature Dependence of Lasing Wavelength 59
3.3.5 Characteristic Temperature 61
3.4 CW-Mode 460-nm InGaN/GaN MQW Laser Diodes 62
3.4.1 LD Structures 63
3.4.2 Results and Discussions 63
3.5 Summary 66

CHAPTER 4: DEVELOPMENT OF GAN/INGAN DOUBLE-HETEROJUNCTION BIPOLAR TRANSISTORS 68
4.1 Basic Device Physics 69
4.2 Epitaxial Layer Structures 77
4.3 Device Layout Design 79
4.3.1 Device Layout Design for RF and Power HBTs 79
4.3.2 Process Control Monitors 82
4.4 Device Fabrication 84
4.4.1 Fabrication Process Flow 84
4.4.2 Ohmic Contact on Emitter, Collector, and Base 86
4.5 D.C. Characteristics 88
4.5.1 Common-Emitter *I-V* Characteristics of HBTs on Sapphire 88
4.5.2 Common-Emitter *I-V* Characteristics of HBTs on FS GaN 91
4.5.3 Analysis of Base Current Components 93
4.5.4 Breakdown Voltage 101
4.5.5 Degradation of the Common-Emitter Offset Voltage 105
4.6 RF Performance of DHBTs on Sapphire Substrates 108
4.7 Summary 113

CHAPTER 5: SUMMARY AND FUTURE WORK 115

REFERENCES 119

VITA 132

LIST OF TABLES

Table 1. Major material properties of binary III-N compound semiconductors and other important semiconductors at 300 K. 2

Table 2. Major recently reported III-N *p-i-n* APDs and photodiodes 6

Table 3. Recent development of InGaN/GaN-base LDs on *c*-plane GaN substrates. 10

Table 4. Recent development of InGaN/GaN-based LDs on semi-polar GaN substrates. 11

Table 5. Recent development of InGaN/GaN-based LDs on *m*-plane GaN substrates. 11

Table 6. Major reported III-N HBTs and their d.c. performance. 14

Table 7. The layer structure of the GaN homojunction *p-i-n* APD in this study. 20

Table 8. The experimental parameters in the DOE for the wet-etching surface treatment study. 24

Table 9. The DOE table in the wet-etching surface treatment study and the summary of the experiment response. 25

Table 10. The DOE table for the optimization of ohmic contact to *p*-GaN in InGaN-based LDs 50

Table 11. Compositions and thicknesses of the 420-nm LD structures. 53

Table 12. Compositions and thicknesses of the 460-nm LD structure. 64

Table 13. The characteristics of the RT CW-mode InGaN-based LDs at GT. 67

Table 14. The epitaxial layer structure of a published *npn* InGaP/GaAs HBT [193] 77

Table 15. The epitaxial layer structure of *npn* GaN/InGaN DHBTs in this study 78

Table 16. RF power HBT design variation. 81

Table 17. Characteristics of base current components 95

Table 18. Summary of A_E-related and P_E-related base current components at different J_C for GaN/InGaN DHBTs on a GaN substrate and a sapphire substrate. 96

Table 19. Breakdown characteristics of HBTs on the FS GaN substrate and the sapphire substrate 103

LIST OF FIGURES

Figure 1. Bandgap energy (eV) versus lattice constant (Å) for Würtzite III-N semiconductors at 300K. 3

Figure 2. Energy band diagram schematics of (a) a reverse-biased *p-i-n* photodiode, and (b) a *p-i-n* APD biased near the avalanche breakdown showing carrier multiplication by impact ionization. 19

Figure 3. (a) The fabrication process flow chart for GaN UV *p-i-n* APDs. (b) An SEM picture of a fabricated 76-µm-diameter (4536 μm^2) GaN UV *p-i-n* APD. 22

Figure 4. (a) The main effects of KOH concentration, $K_2S_2O_8$ concentration, and UV illumination power on the surface roughness improvement. (b) The interaction between each two of KOH concentration, $K_2S_2O_8$ concentration, and UV illumination power. 25

Figure 5. AFM images show the surface of a dry-etched *n*-type GaN sample (a) before and (b) after the optimized wet-etching surface treatment. 27

Figure 6. 3-dimentional AFM images show a dry-etched mesa sidewall (a) before and (b) after the optimized wet-etching surface treatment. 27

Figure 7. The comparison of reverse-biased I_{dark} of GaN *p-i-n* APDs. Sample A: without wet-etching surface treatment, Sample B: with the optimized wet-etching surface treatment. 28

Figure 8. The schematics of the spectral response measurement system. 31

Figure 9. (a) The bias-dependent R_λ of a 100-µm-diameter GaN *p-i-n* APD at RT. (b) The bias-dependent EQE of the same device. Wafer ID: 1-1206-1. 32

Figure 10. Reverse-biased *I-V* characteristics of a 76-µm-diameter GaN *p-i-n* APD with and without UV illumination and the corresponding photo current avalanche gain for the (a) 280-nm illumination and (b) 340-nm illumination. Wafer ID: 1-0907-5. 34

Figure 11. (a) A histogram showing photo current avalanche gains on 40 different-sized GaN *p-i-n* APDs measured on an 8×8 mm^2 sample. (b) Reverse-biased *I-V* characteristics of a 570-μm^2 GaN *p-i-n* APD with a record avalanche gain > 10^5 at λ=360 nm. Wafer ID: 1-0907-5. 35

Figure 12. The quenching circuit schematic of the Geiger-mode APD testing system in the University of Virginia [17]. 36

Figure 13. (a) SPDE and DCP of a 16-μm-diameter GaN DUV *p-i-n* APD. (b) Dark counts versus a.c. bias pulse repetition frequency in a time duration of 100 seconds, showing consistent dark count rates. Wafer ID: 2-1283-1. 38

Figure 14. (a) Reverse-biased *I-V* characteristics of an 80-μm-diameter GaN *p-i-n* APD without and with UV illumination at λ = 360 nm. (b) Curve-fitting of the measured dark current data from -25 V to -35 V to estimate R_V and I_{dark}. Wafer ID: 2-1283-6. 40

Figure 15. (a) Forward-biased *I-V* characteristics of different-sized GaN *p-i-n* APDs. (b) Current densities versus inverse of the device radii at a forward bias of 2.5 V. Wafer ID: 2-1283-6.. 41

Figure 16. Carrier transition mechanisms between the conduction band and valence band in semiconductors: (a) spontaneous recombination, (b) stimulated generation, (c) stimulated recombination, and (d) non-radiative recombination.................................... 44

Figure 17. Process flow chart of InGaN/GaN MQW vertical-current-injected edge-emitting LDs. 48

Figure 18. Designed band diagrams in the EBL and active regions for the abrupt-EBL LD and the step-graded-EBL LD. 53

Figure 19. The refractive index profiles and the corresponding optical-field distributions of LD Structures A and B. 54

Figure 20. Simulated energy band diagrams for (a) the abrupt-EBL LD and (b) the step-graded-EBL LD [86]. 55

Figure 21. Simulated carrier concentration distributions for (a) the abrupt-EBL LD and (b) the step-graded-EBL LD [86].. 55

Figure 22. (a) Pulsed-current *L-J* curves and (b) CW-mode *L-J-V* curves of the fabricated abrupt-EBL LD (Device ID: 2-1507-3-2-750-5-G2-4um) and step-graded-EBL LD (Device ID: 2-1518-3-3-750-2-G1-8um) at 293K. The device dimension is 8×750 μm^2. 57

Figure 23. CW-mode lasing spectra of (a) the abrupt-EBL LD (wafer ID: 2-1507-3-2) and (b) the step-graded-EBL LD (wafer ID: 2-1518-3-3) at P_{opt} of 30 mW. 58

Figure 24. The reciprocal differential quantum efficiency ($1/\eta_d$) versus cavity lengths (L) for Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3). 59

Figure 25. Temperature dependence of λ for the LD Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3) under pulsed-current operation from T = 20 C to T = 58 C.. 60

Figure 26. The peak photon emission wavelengths as a function of injection current for LD Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3) under pulsed-mode operation.. 61

Figure 27. Temperature dependence of the threshold currents for Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3) in the pulsed-current mode from T = 20 C to T = 58 C. 62

Figure 28. *L-J-V* curves of a 460-nm LD with $In_{0.03}Ga_{0.97}N$ waveguide layers under the pulsed-current operation. Device ID: 2-1508-4-3-F1000-G3-10um.......... 65

Figure 29. (a) Lasing spectra and (b) *L-J-V* curves of a 460-nm LD with $In_{0.03}Ga_{0.97}N$ waveguide layers under the CW-mode operation. Device ID: 2-1508-4-3-750-4a-G1-6um. Inset: the lasing far-field pattern of this device. 65

Figure 30. Temperature dependence of λ and I_{th} from T = 20 C to T = 58 C. Wafer ID: 2-1508-4-3.......... 66

Figure 31. Schematic diagram showing the locations of the four main base recombination currents in bipolar transistors: (1) surface recombination current in the exposed extrinsic base, (2) bulk recombination current in the neutral base region, (3) interface recombination current at the base contact, and (4) space-charge recombination current in the BE space-charge region. 70

Figure 32. The layout of an HBT with $A_E = 3 \times 10\ \mu m^2$. The device has three mesas: BE junction mesa, BC junction mesa, and device isolation mesa. The RF pad is only partially shown here. 80

Figure 33. The layout of an HBT with $A_E = 240 \times 4 \times 120\ \mu m^2$ designed for high power switches. 82

Figure 34. The design of a via-chain with 20 via holes for the collector metal. Similar via-chains also exist for the emitter metal and base metal.......... 83

Figure 35. TLM patterns for (from right to left) emitter contact, base contact, collector contact, on-wafer resistor, and device isolation. 83

Figure 36. The layout of an HBT with $A_E = 20 \times 20\ \mu m^2$ that can be measured as a “quick-test” device before the whole fabrication process is done. 84

Figure 37. Schematics of the direct-growth GaN/InGaN *npn* DHBT. 85

Figure 38. (a) An SEM picture of an $A_E = 4 \times 10\ \mu m^2$ HBT prior to the device passivation. (b) A microscope picture of a fully fabricated HBT device. The device is designed in G-S-G coplanar waveguide configuration for common-emitter RF measurement. 85

Figure 39. The emitter TLM results of Ti/Al/Ti/Au on *n*-GaN in GaN/InGaN *npn* HBTs: (a) *I-V* curves of $40 \times 80\ \mu m^2$ metal pads with different spaces, (b) linear fitting of measured resistances versus metal pads spaces. 86

Figure 40. The sub-collector TLM results of Ti/Al/Ti/Au on *n*-GaN in GaN/InGaN *npn* HBTs: (a) *I-V* curves of $40 \times 80\ \mu m^2$ metal pads with different spaces, (b) linear fitting of measured resistances versus metal pads spaces. 87

Figure 41. The base TLM results of Ni/Au on *p*-InGaN in GaN/InGaN *npn* HBTs: *I-V* curves of 40×80 μm^2 metal pads with different spaces. 87

Figure 42. (a) The common-emitter *I-V* family curves and (b) the Gummel plot of an A_E = 3×3 μm^2 GaN/InGaN *npn* HBT on a sapphire substrate. Device ID: 1-1785-1-G-B4-3x3CV. 88

Figure 43. (a) The common-emitter *I-V* family curves and (b) the common-emitter Gummel plot of an A_E = 3×5 μm^2 GaN/InGaN *npn* HBT. Device ID: 1-1785-1-E-B1-3x5GV. 89

Figure 44. (a) The common-emitter *I-V* family curves and (b) the common-emitter Gummel plot of an A_E = 20×20 μm^2 GaN/InGaN *npn* HBT. Device ID: 1-1777-6-E-2c-a2-20um. 90

Figure 45. (a) The microscope picture of a 24×6×60 μm^2 multi-finger GaN/InGaN *npn* HBT. (b) The common-emitter *I-V* family curves of this multi-finger HBT. Device ID: 1-1777-6-E-4c-fishbone24. 91

Figure 46. (a) The common-emitter *I-V* family curves and (b) Gummel plot of an A_E = 3×3 μm^2 GaN/InGaN *npn* HBT grown on a *c*-plane FS GaN substrate. Device ID: 1-1793-6-K-B4-3x3DV. 93

Figure 47. The common-emitter *I-V* family curves of an A_E = 3×3 μm^2 DHBT grown on a *c*-plane FS GaN substrate measured using 1-ms pulses at RT. Device ID: 1-1793-6-L-B2-3x3CV. 93

Figure 48. J_C/β versus P_E/A_E at J_C=100, 500, 1000 A/cm^2 for GaN/InGaN *npn* DHBTs on (a) a FS GaN substrate (Sample ID: 1-1793-6-M) and (b) a sapphire substrate (Sample ID: 1-1785-1-G). 96

Figure 49. J_C/β versus P_E/A_E at J_C=100 A/cm^2 for GaN/InGaN *npn* DHBTs large-area devices before and after the BCB passivation. Sample #: 1-1793-6-M. 97

Figure 50. Measured log-β-versus-log-I_C plots for the HBTs on the FS GaN substrate (Device ID: 1-1793-6-K-B4-3x3DV) and sapphire substrate (Device ID: 1-1785-1-G-B4-3x3CV), A_E = 3×3 μm^2. 99

Figure 51. (a) The I_{CBO} curves and (b) the I_{CEO} curves of GaN/InGaN *npn* HBTs with different A_E grown on the *c*-plane FS GaN substrate. Sample ID: 1-1793-6-M. 102

Figure 52. The I_{CBO} curve and I_{CEO} curve of an A_E = 3×3 μm^2 GaN/InGaN *npn* HBT on the sapphire substrate. Device ID: 1-1785-1-G-B2-3x3DV. 103

Figure 53. The forward- and reverse-biased *I-V* curves of the (a) BE diodes and (b) BC diodes of A_E = 3×3 μm^2 devices on the FS GaN substrate and sapphire substrate. . 104

Figure 54. The common-emitter *I-V* family curves of an A_E = 3×5 μm^2 GaN/InGaN *npn* DHBTs (a) when the V_{offset} degradation happens, and (b) 5 days after the V_{offset} degradation. Device ID: 1-1785-1-E-B1-3x5GV. 106

Figure 55. The Gummel plots of an A_E = 3×5 μm^2 GaN/InGaN *npn* DHBT on the sapphire substrate before and after the V_{offset} degradation. 107

Figure 56. The forward- and reverse-biased *I-V* curves of the (a) BC diodes and (b) BE diodes of two A_E = 3×5 μm^2 HBTs on the sapphire substrate. Device A has a low V_{offset} but Device B has a high V_{offset}. 107

Figure 57. The measured $|h_{21}|^2$ and MAG curves of an A_E = 3×5 μm^2 GaN/InGaN *npn* HBT on the sapphire substrate. Device ID: 1-1785-1-G-B12-3x5DV. 109

Figure 58. (a)The Gummel plot of an *npn* GaN/InGaN HBT with A_E = 4×20 μm^2 on a sapphire substrate, and (b) its common-emitter *I-V* family curves. Device ID: 1-1785-1-G-B4-4x20DV. 111

Figure 59. The measured $|h_{21}|^2$ and MAG of an A_E = 4×20μm^2 GaN/InGaN *npn* DHBT. Device ID: 1-1785-1-G-B4-4x20DV. 112

Figure 60. The f_T and f_{max} of an A_E = 4×20μm^2 GaN/InGaN *npn* DHBT at different J_C. Device ID: 1-1785-1-G-B4-4x20DV. 112

Figure 61. Current-gain-versus-J_C comparison chart for state-of-the-art III-N HBTs. Data points without substrate information shown in this plot are all from HBTs on sapphire substrates. 113

NOMENCLATURE

2DEG	two-dimensional electron gas
α	common-base current gain
α_i	internal loss
α_T	base transport factor
a.c.	alternating current
A_E	emitter area
AFM	atomic force microscope
ALD	atomic layer deposition
ANOVA	analysis of variables
APD	avalanche photodiode
β	common-emitter direct current current gain
BC	base-collector
BCB	Benzocyclobutene
BE	base-emitter
BJT	bipolar junction transistor
BV_CBO	open-emitter base-collector diode reverse-biased breakdown voltage
BV_CEO	open-base collector-emitter breakdown voltage
C_jc	base-collector junction capacitance
C_je	base-emitter junction capacitance
CPW	coplanar waveguide
CW	continuous-wave
D^*	effective detectivity
d.c.	direct current
DCP	dark count probability
DH	double-heterostructure
ΔE_c	conduction band energy difference
ΔE_g	bandgap difference
D_nB	minority electron diffusion coefficient in the base
DOE	design of experiment
D_pE	minority hole diffusion coefficient in the emitter
DUV	deep ultraviolet
DUT	device under test
E-gun	electron-gun
EBL	electron-blocking layer
E_g	bandgap energy

EHP	electron-hole pair
EQE	external quantum efficiency
f_{max}	maximum oscillation frequency
FS	free-standing
f_{T}	cut-off frequency
FWHM	full width at half maximum
$\mathit{\Gamma}$	optical confinement factor
γ	emitter injection efficiency
GPIB	general purpose interface bus
HBT	heterojunction bipolar transistor
HD	high-definition
h_{fe}	common-emitter small-signal current gain
HFET	hetero-junction field-effect transistor
I_{B}	base current
$I_{\mathrm{B,bulk}}$	recombination current in the neutral base region
$I_{\mathrm{B,cont}}$	recombination current at the base contact
I_{Bp}	hole back-injection current
$I_{\mathrm{B,scr}}$	recombination current in the BE space-charge region
$I_{\mathrm{B,surf}}$	surface recombination current in the exposed extrinsic base region
I_{C}	collector current
I_{CBO}	open-emitter BC diode reverse-biased leakage current
I_{CEO}	open-base collector-emitter leakage current
I_{Cn}	electron current in the overall collector current
I_{Cp}	hole current in the overall collector current
ICP	inductively coupled plasma
I_{dark}	dark current
I_{E}	emitter current
I_{En}	emitter electron current
III-N	III-Nitride
I_{p}	photo current
I_{s}	saturation current
I_{th}	threshold current
I-V	current-voltage
J_{C}	collector current density
J_{dark}	dark current density
J_{th}	threshold current density
λ	wavelength
L_{BE}	base metal to emitter mesa space
LED	light-emitting diode

LD	laser diode
L_{E}	emitter length
L-I	optical-output power versus current
L-I-V	optical-output-power versus current versus voltage
L-J	optical-output-power versus injection-current-density
L-J-V	optical-output-power versus current-density versus voltage
LPCVD	liquid phase chemical vapour deposition
M	avalanche multiplication coefficient
MBE	molecular beam epitaxy
MMIC	monolithic microwave integrated circuit
MOCVD	metal-organic chemical vapor deposition
η	ideality factor
η_{i}	internal efficiency
n	refraction index
N_{B}	base doping
N_{C}	collector doping
N_{E}	emitter doping
NEP	noise equivalent power
N_{ph}	photon density
P_{a}	avalanche probability
PCM	process control monitor
P_{E}	emitter perimeter
PEC	photo-enhanced chemical wet etching
PECVD	plasma-enhanced chemical vapor deposition
PMT	photomultiplier tube
P_{opt}	optical output power
QCSE	quantum-confined stark effect
QW	quantum well
ρ_{c}	specific contact resistances
R_{12}	stimulated generation rate
R_{21}	stimulated recombination rate
r_{B}	base resistance
r_{BE}	BE diode series resistance
r_{Bx}	extrinsic base resistance
r_{Bi}	intrinsic base resistance
r_{C}	collector resistance
r_{E}	emitter resistance
RF	radio frequency
RIE	reactive ion etching

RMS	root mean square
R_λ	responsivity
R_{nr}	non-radiative recombination rate
R_{sh}	sheet resistance
R_{sp}	spontaneous recombination rate
R_{st}	stimulated photon generation rate
RT	room temperature
RTA	rapid thermal annealing
SOLT	short-open-load-through
SPDE	single-photon detection efficiency
SPSL	short-period superlattice
SRH	Shockley-Read-Hall
τ_{b}	base transit time
τ_{c}	collector charging time
τ_{e}	emitter charging time
τ_{ec}	emitter-collector transit time
τ_{sc}	base-collector junction space-charge transit time
τ_{nB}	electron life time in the neutral base region
T_0	characteristic temperature
TLM	transmission line measurement
UID	unintentionally doped
UV	ultraviolet
V_{A}	early voltage
V_{BE}	base-emitter junction voltage
V_{CE}	collector-emitter voltage
V_{knee}	common-emitter knee voltage of V_{CE}
V_{offset}	common-emitter offset voltage of V_{CE}
V_{th}	threshold voltage
WBG	wide bandgap
W_{E}	emitter width
W_{eff}	effective emitter width
WPE	wall-plug efficiency
X_{B}	base thickness
X_{dep}	base-collector junction depletion width
X_{E}	emitter thickness

SUMMARY

This dissertation describes the development of III-nitride (III-N) bipolar devices for optoelectronic and electronic applications. Research mainly involves device design, fabrication process development, and device characterization for Geiger-mode gallium nitride (GaN) deep-UV (DUV) *p-i-n* avalanche photodiodes (APDs), indium gallium nitride (InGaN)/GaN-based violet/blue laser diodes (LDs), and GaN/InGaN-based *npn* radio-frequency (RF) double-heterojunction bipolar transistors (DHBTs). All the epitaxial materials of these devices were grown in the Advanced Materials and Devices Group (AMDG) led by Prof. Russell D. Dupuis at the Georgia Institute of Technology using the metalorganic chemical vapor deposition (MOCVD) technique.

Geiger-mode GaN *p-i-n* APDs have important applications in DUV and UV single-photon detections. In the fabrication of GaN *p-i-n* APDs, the major technical challenge is the sidewall leakage current. To address this issue, two surface leakage reduction schemes have been developed: a wet-etching surface treatment technique to remove the dry-etching-induced surface damage, and a ledged structure to form a surface depletion layer to partially passivate the sidewall. The first Geiger-mode DUV GaN *p-i-n* APD on a free-standing (FS) *c*-plane GaN substrate has been demonstrated.

InGaN/GaN-based violet/blue/green LDs are the coherent light sources for high-density optical storage systems and the next-generation full-color LD display systems. The design of InGaN/GaN-based LDs has several challenges, such as the quantum-confined stark effect (QCSE), the efficiency droop issue, and the optical confinement design optimization. In this dissertation, a step-graded electron-blocking layer (EBL) is

studied to address the efficiency droop issue. Enhanced internal quantum efficiency (η_i) has been observed on 420-nm InGaN/GaN-based LDs. Moreover, an InGaN waveguide design is implemented, and the continuous-wave (CW)-mode operation on 460-nm InGaN/GaN-based LDs is achieved at room temperature (RT).

III-N HBTs are promising devices for the next-generation RF and power electronics due to the advantages of high breakdown voltages, high power handling capability, and high-temperature and harsh-environment operation stability. One of the major technical challenges to fabricate high-performance RF III-N HBTs is to suppress the base surface recombination current on the extrinsic base region. The wet-etching surface treatment has also been employed to lower the surface recombination current. As a result, a record small-signal current gain (h_{fe}) > 100 is achieved on GaN/InGaN-based *npn* DHBTs on sapphire substrates. A cut-off frequency (f_T) > 5.3 GHz and a maximum oscillation frequency (f_{max}) > 1.3 GHz are also demonstrated for the first time. Furthermore, a FS *c*-plane GaN substrate with low epitaxial defect density and good thermal dissipation ability is used. Therefore, h_{fe} > 115, collector current density (J_C) > 141 kA/cm^2, and power density > 3.05 MW/cm^2 are achieved at RT, which are all the highest values reported ever on III-N HBTs.

CHAPTER 1

INTRODUCTION TO III-NITRIDE MATERIALS AND DEVICES

1.1 Group III-Nitride Materials Properties and Applications

With Column III elements, nitrogen atoms can form III-N compound semiconductors, such as GaN, aluminum nitride (AlN), indium nitride (InN), and their ternary and quaternary alloys. Major properties of binary III-N compound semiconductors are listed in Table 1 [1-8]. Compared to the other semiconductors in the table, Group III-N with the stable Würtzite lattice structure is the unique one that combines many interesting features: direct and wide bandgap (WBG), decent thermal conductivity, high electron saturation velocity, and bandgap engineering ability with wide bandgap energy (E_g) coverage. Therefore, III-N devices have attracted tremendous research attention and become of great commercial importance within the past ten years.

The direct bandgap makes III-N materials suitable for light emitters with high-efficient band-to-band electron-hole radiative recombination. As shown in Figure 1 [9], III-N materials cover a wide range of the electromagnetic spectrum from AlN (E_g = 6.2 eV, λ = 200 nm) in the DUV to InN (E_g = 0.7 eV, λ = 1772 nm) in the infrared, with GaN (E_g = 3.4 eV, λ = 364 nm) in between. In addition, the bandgap engineering ability allows the designs of the quantum well (QW) and EBL for high-performance light-emitting devices. Nowadays, III-N-based high-brightness light-emitting diodes (LEDs) have dominated the solid-state lighting market. III-N-based LDs in the violet and blue regions have been commercialized for high-density optical storage systems and laser pico-projectors and displays. On the other hand, because of their WBG nature, GaN- and

AlGaN-based photodiodes and APDs are prime candidates for filter-free UV and DUV photodetections, offering extremely low noise and high sensitivity.

Table 1. Major material properties of binary III-N compound semiconductors and other important semiconductors at 300 K.

	Binary III-N			Si	Ge	GaAs	InP	4H-SiC
	GaN	AlN	InN					
Lattice structure	W*	W*	W*	D*	D*	Z*	Z*	W*
Lattice constant *a* (Å)	3.189	3.11	2.544	5.431	5.646	5.653	5.869	3.073
Bandgap energy (eV)	3.44	6.2	0.7 ~ 1.0	1.12	0.66	1.42	1.35	3.26
Nature of bandgap	DI*	DI*	DI*	I*	I*	DI*	DI*	I*
Breakdown field (MV/cm)	2.5 ~ 5	1.2 ~ 1.8	--	0.25 ~ 0.8	0.1	0.3 ~ 0.9	0.5	3 ~ 5
Electron saturation velocity (10^7 cm/s)	2.5	1.9	3.4	1.0	3.1	0.7	3.9	1.9
Electron mobility (cm^2/Vs)	1000	300	3200	1450	3900	8000	5400	600
Hole mobility (cm^2/Vs)	400	14	--	500	1900	400	200	120
Thermal conductivity (W/cm K)	2.0 ~ 2.4	3.0 ~ 3.3	0.6 ~ 1.0	1.56	0.58	0.46	0.68	3.7

*W: Würtzite, D: diamond, Z: Zincblende, DI: direct bandgap, I: indirect bandgap

In electronic applications, III-N materials have been widely studied for high-voltage/high-power/high-temperature electronics because of their WBG, high material breakdown fields, and high thermal stability. The bandgap engineering enables the design of heterostructures for HBTs and hetero-junction field-effect transistors (HFETs). Furthermore, III-N materials have significant spontaneous- and piezoelectric-polarization effects, thereby providing more device design freedom. For instance, the channel of an

AlGaN/GaN HFET is formed by the spontaneous- and piezoelectric-polarization-induced two-dimensional electron gas (2DEG) at the AlGaN/GaN hetero-interface [10]. With the recent development of III-N material-growth technology, high electron saturation velocity has also been demonstrated in III-N materials. Therefore, III-N-based RF high-power transistors and high-speed power switches are believed to be important in the next-generation high-power wireless communication systems and high-efficiency power conversion systems.

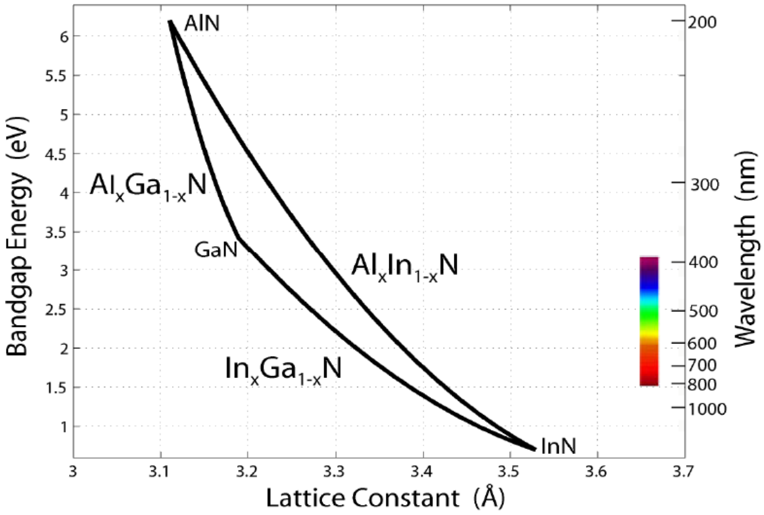


Figure 1. Bandgap energy (eV) versus lattice constant (Å) for Würtzite III-N semiconductors at 300K.

Because of the WBG and good heat dissipation ability, III-N devices are also attracting attention from areas such as geothermal, oil and gas industries where devices that can work at high temperature are highly desired. In addition, III-N devices exhibit superior radiation hardness compared to their narrow bandgap counterparts based on silicon (Si) or gallium arsenide (GaAs) technologies, allowing them to be deployed in many space applications.

1.2 GaN Deep-Ultroviolet *p-i-n* Avalanche Photodiodes

UV light is defined as electromagnetic radiation between violet and x-rays, in the wavelength range of 10 nm to 400 nm. There are three major spectral bands in the UV region: UVA (400 nm to 320 nm), UVB (320 nm to 280 nm), and UVC (280 nm to 100 nm). UV photodetectors with spectral response shorter than 400 nm do not collect signals from visible radiation, so they are named visible-blind UV detectors. Similarly solar-blind UV detectors are those only sensitive to the UVC band, because there is no UVC energy on the earth surface from the sun due to the high absorption in the ozone layer.

High-sensitive UV photodetectors are of great importance in numerous scientific, civilian, and defense applications such as biological agent detection [11], UV astronomy [12], flame detection [13], and covert communications [14]. Low dark current density (J_{dark}), high responsivity (R_{λ}), high optical gain, and the single-photon detection ability are desired for these applications. Photomultiplier tubes (PMTs) are widely used because they provide optical gains in the order of 10^6 with low dark current (I_{dark}). But PMTs have the disadvantages of low photocathode quantum efficiency for UV light, high operation voltage (> 1000 V), requirement of cooling systems, and extra filters for visible-blind and solar-blind detection. On the other hand, semiconductor APDs can offer large optical avalanche gains comparable to PMTs, combined with the benefits of small size, high reliability, high speed, low operation voltage, low power consumption, low cost, and all-solid-state integration. A UV-enhanced Si APD is one of the commercial UV semiconductor detectors. A typical J_{dark} of a commercial UV-enhanced Si APD (Hamamatsu® S9073) is 0.64 μA/cm^2 at an avalanche gain of 50 [15]. However, broad spectral response is an essential problem for Si APDs due to its narrow bandgap. Its spectral response is from 200 nm to 1000 nm with a peak at 620 nm, which is not blind to visible light without an external filter.

The WBG semiconductors, such as III-N and SiC materials, offer advantages for high-sensitive UV detection in terms of low I_{dark}, decent radiation hardness, and filter-free visible-blind or solar-blind (if $E_{\mathrm{g}} > 4.43$ eV) capabilities. In 2007, Prof. Joe C. Campbell's group at the University of Virginia demonstrated the first Geiger-mode SiC *p-i-n* APD with an avalanche gain $> 10^5$ at 265 nm [16,17]. Excellent performance on J_{dark} and device yield was also obtained. However, compared to the III-N materials, since SiC is a indirect bandgap material, the R_λ is not strong for a photon with energy just above E_{g}. Second, SiC's E_{g} is not large enough for intrinsic solar-blind UV detection. Also, SiC material system does not have the bandgap engineering flexibility.

III-N materials can provide high-effective band-to-band electron-hole-pair (EHP) generation because of the direct bandgap feather. In addition, wider bandgap III-N materials, such as AlGaN or InAlN, enable intrinsic filter-free solar-blind DUV photodetection as well as novel heterojunction designs. In 2001, the first Geiger-mode GaN *p-i-n* APD was demonstrated on a sapphire substrate at the MIT Lincoln Lab [18]. In the following years, many high-performance III-N *p-i-n* APDs have been reported. The recent development on III-N *p-i-n* APDs is summarized in Table 2.

To achieve high-performance Geiger-mode III-N *p-i-n* APDs for single-photon detection, technical issues mainly involve device layer structure design, material quality improvement, and fabrication process development especially the mesa sidewall treatment. First, the device layer structure needs optimization to enhance the impact ionization. The impact ionization process in GaN has been studied, and the ionization coefficient has been shown higher for holes than electrons [19]. Therefore, back-illuminated GaN *p-i-n* APDs and separated-absorption-and-multiplication (SAM) GaN APDs were proposed and fabricated, showing Geiger-mode operation ability [19-22]. However, the J_{dark} of those devices was still high [20] probably due to the high epitaxy defect density on sapphire substrates.

Table 2. Major recently reported III-N *p-i-n* APDs and photodiodes.

Research lab (year)	Substrate	J_{dark} (A/cm^2)	R_λ (mA/W)	Avalanche gain	SPDE*
GT [23] (2006)	GaN	7n @ -5V	-	1.0×10^3	-
NCU [24] (2006)	sapphire	-	110 @ 365 nm, 0 V	-	-
NWU [21,22] (2007)	sapphire	-	82 @ 361 nm, 0 V	5.7×10^3	20%
GT [25] (2007)	GaN	15 n @ -20 V	-	1.0×10^4	-
GT [26] (2007)	GaN	141 n @ -20 V	-	50	-
GT [27] (2008)	GaN	100 n @ -45 V	-	3.0×10^4	-
Bilkent [28] (2008)	sapphire	64 n @ -5 V	230 @ 356 nm, -5V	-	-
NWU [29] (2008)	sapphire	3.84 μ @ -40 V	94 @ 360 nm, -70 V	5.1×10^4	-
NWU [30] (2008)	sapphire	-	163 @ 352 nm, -20 V	5.0×10^3	-
NWU [20] (2008)	sapphire	8.89 μ @ -40 V	102 @ 364 nm, -40 V	4.1×10^4	-
GT [31,32] (2008)	GaN	5 n @ -10V	140 @ 360 nm, 0 V	1.0×10^3	1 %
CAS [33] (2009)	sapphire	159 n @ -20 V	-	57	-
GT [34] (2009)	GaN	40 p @ -20V	143 @ 364 nm, 0 V	-	-
NWU [35] (2010)	GaN	2.1 μ @ -70 V	-	1.4×10^4	24%
NWU [36] (2010)	*m*-plane GaN	3.6 μ @ -50 V	42 @ 364 nm, 0 V	8.0×10^3	-

*SPDE: single-photon detection efficiency

The lattice constant mismatch between sapphire substrates and GaN substrates is 14%, thereby resulting in a high epitaxy defect density in the $10^8 \sim 10^{10}$ cm^{-2} range. In *p-i-n* APDs, material defects lead to junction premature breakdown before the electric field becomes high enough for impact ionization to generate avalanche gains. The most effective way to improve the material quality is the use of lattice-matched FS GaN substrates, on which epitaxial GaN defect density less than 10^6 cm^{-2} has been achieved. Recently, GaN *p*-*i*-*n* APDs grown on FS *c*-plane GaN substrates have shown ultra-low J_{dark}, repeatable avalanche gains with high-yield $>10^4$, and Geiger-mode operation abilities [27,31,34,35]. Although the Geiger-mode GaN *p*-*i*-*n* APDs grown on sapphire substrates showed comparable SPDE to those on GaN substrates, their dark count probability (DCP) is higher than those grown on GaN substrates [35] because of the high I_{dark} induced by material defects.

In the fabrication of GaN *p*-*i*-*n* APDs, suppressing sidewall leakage current is the major technical challenge. Plasma dry-etching is conventionally used to form the III-N *p-i-n* diode mesa, but it creates damage on the etched mesa sidewall. Etching damages act as carrier trap centers that cause significant sidewall leakage current and premature sidewall breakdown. However, methods to reduce the process-induced sidewall leakage are less explored. A typical way is to deposit a surface passivation layer, such as SiO_2 or SiN_x using plasma-enhanced chemical vapor deposition (PECVD) [37] or atomic layer deposition (ALD). This method requires tight process control on the interface strain. The energetic plasma applied during the PECVD may induce additional surface damages.

In this dissertation, to address the sidewall leakage current issue in the device fabrication, two surface leakage reduction schemes have been developed: a wet-etching surface treatment technique to remove the dry-etching-induced surface damage [38], and a ledged structure to form a surface depletion layer to passivate the sidewall [39]. Because of these effective surface treatment methods as well as the high-quality GaN materials grown on FS *c*-plane GaN substrates, high-performance Geiger-mode GaN *p-i-n* APDs have been realized.

1.3 InGaN/GaN-Based Laser Diodes

III-N materials with the Würtzite crystal structure have direct WBG, so they are suitable for short-wavelength LEDs and LDs. By adding proper amount of indium to form $In_xGa_{1-x}N$ QWs in the active region, InGaN/GaN-based LEDs and LDs can effectively emit light between 400 nm and 550 nm, where three wavelength regions are of considerable commercial importance: 400 nm ~ 420 nm (violet), 450 nm ~ 470 nm (blue), and 520 nm ~ 540 nm (green).

Violet LDs are the key devices in high-density optical storage systems [40-42], high-resolution laser printers, and some biomedical applications. The short lasing wavelength allows a small diffraction-limited spot size, which enhances the data density of optical storage systems and the resolution of printers. On the other hand, blue and green LDs are required by the next-generation full-color laser pico-projectors. Compared to the lamp projectors, LDs provide high spectral purity, excellent color saturation, high resolution, high contrast ratio, and a practically unrestricted focus depth.

Although at present III-N materials dominate the solid-state lighting market, the first short-wavelength LDs were demonstrated on (Zn, Cd, Mg) (Se, S) II-VI materials in early 1990’s [43-46]. Research was first focused on II-VI compounds due to their same crystal structure and similar lattice constant to GaAs, which make the II-VI crystal growth with low defect density (10^3 ~ 10^4 cm^{-2}) on GaAs substrates straight forward. In 1998, II-VI LDs' lifetime was increased to 400 hours under the CW-mode operation with an optical power of 1 mW [47]. But shortly, researchers found that it was very difficult to further increase the lifetime and output power to a commercial level due to the unstable and fragile II-VI materials. On the other hand, studies on III-N materials were extremely difficult at the beginning, suffering from the lack of lattice-matched substrates and effective *p*-type doping techniques. Owing to the decent mechanical and chemical stabilities, III-N materials soon shown the ability to realize much more reliable LEDs and LDs despite the high epitaxy defect density (10^8 ~ 10^{10} cm^{-2}) grown on sapphire substrates.

As one of the top laser breakthroughs in the 1990s, the first InGaN/GaN MQW violet LD grown on sapphire substrates was demonstrated in 1995 by Nichia [48]. Toshiba [49], Cree [50], Fujitsu [51], and UCSB [52] followed in 1996 and 1997. In 1998, Nichia demonstrated CW-mode violet LDs with a lifetime longer than 10,000 hours [53], and then the violet InGaN-based QW LDs progressed to commercialization [54]. In 2000, the output power increased to 30 mW, which fulfilled the requirement of the high-density optical disk recording system [55]. In the following years, all the major consumer electronics companies, such as Sony, Toshiba, Samsung, LG, Philips, Sharp, etc., made great efforts to develop violet-LD-based high-density optical storage systems for high-definition (HD) videos and huge amount of data storage. In March 2006 Toshiba released the first consumer-based HD DVD player in Japan (sailing stopped in March 2008), and three months later the famous Blu-ray Disc™ players were released by Sony.

The full-color laser projection/display system is the next target application of InGaN-based LDs. After 10-year's development, InGaN-based blue LDs have been commercialized in 2006 [56-58]. However, the first lasing wavelength (λ) > 500 nm InGaN-based LDs were not demonstrated until 2009 [59]. After that, rapid progress has been achieved on the Indium-rich InGaN material growth techniques, and many groups have pushed λ to the true green region (λ > 520 nm) on (0001) *c*-plane, (20-21) and (11-22) semi-polar, and (1-100) non-polar *m*-plane GaN-substrates. Major InGaN/GaN LDs results reported recently on different substrates are listed in Table 3, Table 4, and Table 5.

Table 3. Recent development of InGaN/GaN-base LDs on *c*-plane GaN substrates.

Group (year)	λ (nm)	Cavity size (μm×μm)	Slope efficiency (W/A)	Optical power (mW)	J_{th} (kA/cm^2) *	Operation mode (lifetime)
Nichia [60] (2005)	482.1	2.5×675	-	7	6.2	CW (3000 hrs)
Nichia [58] (2006)	473	2.0×650	-	20	4.2	CW (10000 hrs)
Samsung [57] (2007)	448	2.5×650	0.7	300	1.85	CW (5000 hrs)
Osram [61] (2008)	441	1.5×600	1.0	60	2.78	-
Samsung [62] (2008)	485	2.0×650	0.12	10	7.16	CW
Nichia [63] (2008)	488	-	-	5	3.3	CW (10000 hrs)
Osram [59] (2009)	500	-	0.65	70	8.2	pulse
Nichia [64] (2009)	445	-	-	1000	-	CW (30000 hrs)
Nichia [65] (2009)	515	2.0×600	0.14	8	4.4	CW (5000 hrs)
Osram [66] (2009)	515.9	11×600	0.13	50	9.0	pulse
GT [67,68] (2009)	460	8×750	0.216	8.59	5.67	CW
Osram [69] (2010)	524	1.8×600	0.33	50	9.0	CW

*J_{th}: threshold current density

Table 4. Recent development of InGaN/GaN-based LDs on semi-polar GaN substrates.

Group (year)	λ (nm)	Cavity size (μm×μm)	Slope efficiency (W/A)	Optical power (mW)	J_{th} (kA/cm^2)	Operation mode (lifetime)
UCSB [70] (2008)	426.9	2.0×1200	0.14	20	12.8	pulse
Sumitomo [71] (2009)	531	10×600	-	-	15.4	pulse
Sumitomo [72] (2009)	520	2.0×600	0.1	2.5	7.9	CW
UCSB [73] (2009)	405.9	1.4×600	0.26	10	6.5	CW
UCSB [74] (2010)	506.4	3.0×1500	-	13	19	pulse

Table 5. Recent development of InGaN/GaN-based LDs on *m*-plane GaN substrates.

Group (year)	λ (nm)	Cavity size (μm×μm)	Slope efficiency (W/A)	Optical power (mW)	J_{th} (kA/cm^2)	Operation mode (lifetime)
UCSB [75] (2007)	404.3	1.9×600	-	25	6.8	CW (15 hrs)
ROHM [76] (2007)	451.8	1.5×600	-	20	22.3	pulse
ROHM [77] (2008)	459	2.0×400	0.37	5	5.0	CW
Sharp [78] (2008)	463	1.5×600	0.91	10	7.8	Pulse
ROHM [79] (2008)	481	2.5×400	0.49	20	6.1	CW
UCSB [80] (2009)	441.2	8.0×500	-	20	10.7	pulse
UCSB [81] (2009)	465	2.0×500	-	25	19	pulse
UCSB [82] (2009)	481	4.0×500	-	17	18	pulse
ROHM [83] (2009)	499.8	2.5×600	0.05	15	3.1	CW
UCSB [84] (2010)	461	4.0×500	0.3	5	4.1	CW
SORAA [85] (2010)	523	-	-	1.5	-	CW

Despite quite a few recent demonstrates of $\lambda > 500$ nm LDs the design and growth of high-quality Indium-rich InGaN/GaN QWs is still the major technical challenge for blue/green light-emitting devices due to the InGaN decomposition and segregation issue. For LDs, the design and growth of the cladding layers and waveguides are also challenges. A good optical confinement requires a large refractive index difference; however, it may result in large lattice mismatch and high dislocation/cracking densities.

In this study, LD structures are grown on *c*-plane FS GaN substrates. Compared to *m*-plane and semi-polar GaN substrates, the *c*-plane GaN substrate has the advantages of low cost and large wafer size, which are the keys for device mass production in the future. However, there are several issues for the III-N materials grown on polarized *c*-plane substrates, such as the quantum-confined stark effect (QCSE) and polarization-induced quantum efficiency droop. Based on Prof. P. Douglas Yoder's design [86], a step-graded EBL is introduced to address the polarization-induced quantum efficiency droop issue. A dramatically enhanced η_i has been demonstrated on 420-nm InGaN/GaN-based LDs [67,87]. Moreover, a novel InGaN waveguide design is successfully implemented for CW-mode 460-nm InGaN/GaN-based LDs [68,88].

1.4 GaN/InGaN *npn* Double-Heterojunction Bipolar Transistors

III-N transistors combine the advantages of high-power handling capability, high-temperature and harsh-environment operation stability, and high-frequency operation ability. Therefore, in the past decade, III-N HFETs and HBTs have been actively researched and developed for high-power switches and RF amplifiers that enable compact chip size with high output power density in many commercial and defense applications. Significant advancement has been achieved in III-N HFETs. Today, it is common to see III-N HFETs with f_T greater than 200 GHz [89-94] or ultra-high voltage operation in the kV-range [95-99]. On the other hand, when compared to HFETs, HBTs have the advantages of high power density, linear current gain, uniform device turn-on characteristics, and normally-off operation. However, the progress on III-N HBT development has been slow. A number of obstacles inhibit the development of III-N HBTs. For III-N *npn* HBTs, the major issue is the low-conductivity base layer, resulting from the difficulty of achieving high free-hole concentration, the plasma-induced dry-etching damage on the extrinsic base region, and the consequent type-conversion.

Shown in Table 6 are the major III-N HBTs reported since the first AlGaN/GaN *npn* HBTs using a selectively re-grown base layer and emitter layer [100,101]. Soon after, direct-grown AlGaN/GaN *npn* HBTs were reported with improved d.c. current gain (β) [102-104], but limited collector current (I_C) and collector current density (J_C) due to the low free-hole concentration in the *p*-type GaN base. In 2001, a *p*-type InGaN base was first reported in GaN/InGaN *npn* HBTs, showing higher base free-hole concentration, higher β and I_C than AlGaN/GaN *npn* HBTs with *p*-GaN base layers [105,106]. However, the etching-induced damage on the extrinsic base region is still inevitable. To minimize the etching damage and enhance the base conductivity, re-growth techniques were applied again on AlGaN/GaN *npn* HBTs with a re-grown emitter [107], and on GaN/InGaN *npn* HBTs grown on a SiC substrate with a re-grown extrinsic base [108]. However, in view of the process complexity and the cost for mass production, the re-growth approaches are not optimal choices.

Table 6. Major reported III-N HBTs and their d.c. performance.

Group (year)	Type	Base mate-rial	Re-growth	Substrate	β	I_C (mA)	A_E (μm×μm)	J_C (kA/cm^2)
UCSB [100] (1998)	*npn*	GaN	Base	sapphire	3	0.85	1×20	4.25
UCSB [101] (1999)	*npn*	GaN	Emitter	sapphire	1.5	-	17×50	-
UFL [102] (1999)	*npn*	GaN	None	sapphire	10	-	90 diameter	-
UFL [103] (1999)	*npn*	GaN	None	sapphire	2 ~ 5	-	50 diameter	-
UIUC [104] (1999)	*npn*	GaN	None	sapphire	4 ~ 10	1	60×60	0.028
NTT [106] (2001)	*npn*	InGaN	None	SiC	20	7.5	50×60	0.25
UCSB [107] (2003)	*npn*	GaN	Emitter	sapphire	18	9	20×50	1
NTT [108,109] (2003)	*npn*	InGaN	Base	SiC	400	80	50×30	6.7
NTT [110] (2005)	*pnp*	InGaN	None	sapphire	40	37	30×50	2.5
GT [111] (2006)	*npn*	InGaN	None	sapphire	13	10	25×25	1.6
UCSD [112] (2006)	*npn*	InGaN	None	sapphire	37	25	25×25	4
UIUC [113] (2007)	*npn*	InGaN	None	sapphire	49*	3	3×10	10
					17*	89	24×2×60	-
NTT [114] (2008)	*pnp*	InGaN	None	GaN	85	110	30×50	7.3
					47	1000	270×450	0.8
GT [115,116] (2009)	*npn*	InGaN	None	sapphire	42	21	20×20	5.2
GT [117,118] (2010)	*npn*	InGaN	None	sapphire	105*	27	20×20	6.5
GT [119] (2010)	*npn*	InGaN	None	sapphire	84	29	20×20	7.2
					30	200	24×6×60	1.6
GT [120] (2011)	*npn*	InGaN	None	sapphire	38*	1.75	3×3	19.4
GT [121] (2011)	*npn*	InGaN	None	sapphire	24	2.4	3×5	16
GT [122] (2011)	*npn*	InGaN	None	GaN	115*	17	3×3	141

* Current gains in the marked publications are the differential current gain h_{fe}.

After 2005, all the reported III-N HBTs used InGaN base layers and single-pass epitaxial growth schemes (no re-growth) as a result of the progress on the much refined MOCVD epitaxial material growth and device fabrication techniques. GaN/InGaN *pnp* HBTs were reported because a highly-doped *n*-type base layer can be easily obtained to achieve low base resistance [110,114]. To further improve the HBT performance, FS GaN substrates that provide low epitaxy dislocation density and high thermal conductivity were also used in GaN/InGaN *pnp* DHBTs [114]. Despite the decent power performance, *pnp* HBTs theoretically have inferior switching performance than *npn* HBTs as a result of the much slower hole mobility. On the other hand, more *npn* GaN/InGaN HBTs have been reported with good d.c. performance [111-113,123,124]. To further develop a viable III-N HBT technology for RF and power electronics, higher β, higher J_C, lower base resistance (r_B), lower collector-emitter offset voltage (V_{offset}) and knee voltage (V_{knee}) are highly desired.

In this dissertation, direct-grown GaN/InGaN *npn* HBTs are fabricated and tested. An optimized wet-etching surface treatment is applied to the devices to suppress the base surface recombination current. As a result, a record $h_{fe} > 100$ is demonstrated on devices grown on sapphire substrates. The metallization processes have also been carefully studied. Consequently, low-resistive metallization contacts are obtained on the emitter and collector. Low V_{offset}, low V_{knee}, $f_T > 5.3$ GHz and maximum oscillation frequency ($f_{\max}$) > 1.3 GHz are also demonstrated for the first time. Furthermore, on a *c*-plane FS GaN substrate, $h_{fe} > 115$, $J_C > 141$ kA/cm^2 and power density > 3.05 MW/cm^2 are achieved because of the low defect density and high substrate thermal conductivity.

These values are all the highest ones reported on III-N HBTs. Device results have been published in [115-122,125].

1.5 Scope of this Dissertation

The purpose of this study is developing advanced III-N bipolar devices, including Geiger-mode GaN DUV *p-i-n* APDs, InGaN/GaN-based blue/green LDs, and GaN/InGaN-based *npn* RF high-power HBTs. The research work is focused on device design, fabrication process development, and device characterization. The group III-N materials properties, the development status and technical challenges of these III-N devices have been introduced in this chapter.

Chapter 2 describes the fabrication process development and device characterization of the Geiger-mode GaN DUV *p-i-n* APDs grown on FS *c*-plane GaN substrates. In Chapter 3, the fabrication process has been developed for InGaN/GaN-based edge-emitting current-injection LDs. The effect of a step-graded EBL is investigated, showing dramatically enhanced η_i on 420-nm InGaN/GaN-based LDs. Furthermore, CW-mode operation is achieved on 460-nm InGaN/GaN-based LDs with a novel InGaN waveguide design. Chapter 4 covers the process development of direct-grown GaN/InGaN-based *npn* HBTs. An $h_{fe} > 100$ is achieved on devices grown on sapphire substrates. $f_T > 5.3$ GHz and $f_{max} > 1.3$ GHz are demonstrated for the first time. On a FS GaN substrate, record $h_{fe} > 115$, $J_C > 141$ kA/cm^2, and power density > 3.05 MW/cm^2 are obtained.

Finally, a summary of the completed work and discussion of possible schemes toward better device performance will be presented in Chapter 5.

CHAPTER 2

DEVELOPMENT OF GAN ULTRAVIOLET AVALANCHE PHOTODIODES

The objective of this research is to develop Geiger-mode GaN *p-i-n* APDs for UV single-photon detection. The research described in this chapter mainly focuses on the device fabrication process development and device characterization. The results have been published in [25,27,31,32,34,37,126,127]. A master thesis entitled *Fabrication and Characterization of GaN Visible-Blind Ultraviolet Avalanche Photodiodes* was submitted to the School of Electrical and Computer Engineering, Georgia Institute of Technology, in May 2009. The epitaxial structures were grown in the advanced materials and devices group (AMDG) led by Prof. Russell D. Dupuis at Georgia Tech. Epitaxial materials were grown on *c*-plane FS GaN substrates by low-pressure MOCVD using a Thomas Swan reactor system equipped with a close-coupled showerhead growth chamber.

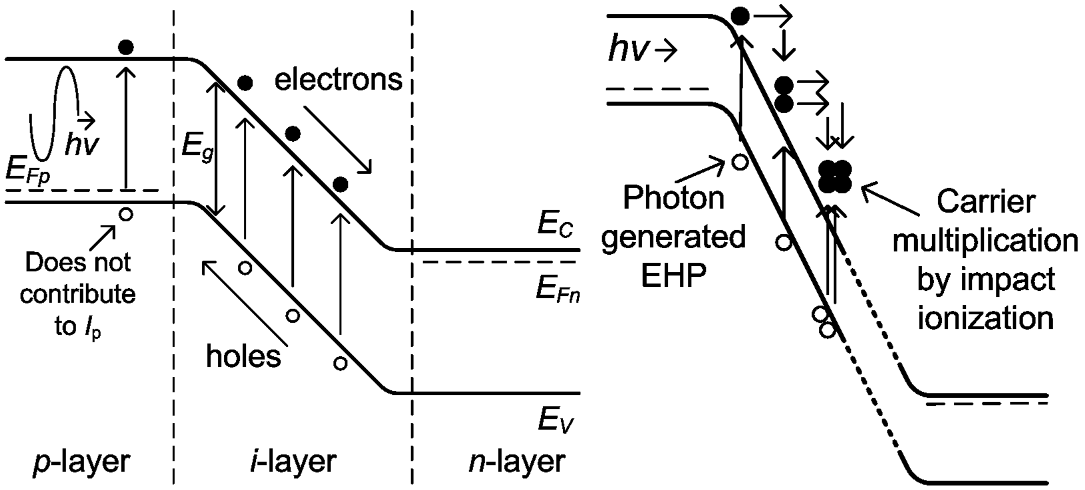
The first part of this chapter presents the device fabrication process. Mesa sidewall current leakage reduction methods have been developed to successfully achieve significant dark current suppression. The second part of this chapter shows the device characterization methods, setups, and results. The first Geiger-mode DUV GaN APD using a front-illuminated homojunction *p-i-n* diode structure is demonstrated on a FS GaN substrate with SPDE of 1.0 % and DCP of 0.03 at $\lambda = 265$ nm. A record photo current avalanche gain > 10^5 is also demonstrated at $\lambda = 360$ nm. When the APD is biased at -20 V and RT, the J_{dark} is lower than 40 pA/cm^2, and the R_λ is 140 mA/W at 360 nm. In addition, the noise equivalent power (NEP) is 4.27×10^{-17} W-Hz$^{-0.5}$, the D* is 1.66×10^{14} cm-Hz$^{0.5}$-W^{-1}, and the minimum detectable optical power is 100 fW. These values are all among the best ones reported to date for III-N *p-i-n* APDs.

2.1 Basic Device Physics

Semiconductors absorb photons by transition of electrons from the valence band to the conduction band, thereby generating EHPs. For band-to-band transitions, the required minimum photon energy equals to the E_g of the semiconductor. If an electric field exists in the semiconductors, then photon-generated EHPs can be swept away in accordance with the electric field direction and form photo current (I_p).

A *p-i-n* photodiode is one kind of important solid-state photodetectors. As shown in Figure 2 (a), in a well-designed *p-i-n* photodiode, most of incoming photons are absorbed in the *i*-region to generate EHPs, which are swept by the built-in or externally applied electric field in the depletion region and contribute to I_p. One figure of merit is the responsivity ($R_\lambda \equiv I_p$/incident optical power) with a unit of mA/W, which is a function of the illuminated photon wavelength (λ). The absorption of incident photons in the un-depleted *p*- or *n*-layer is undesirable because the EHPs excited there (electric field = 0) do not contribute to the I_p. Therefore, it is important to optimize the *p-i-n* layer structure to maximize the incident photons directly to the *i*-region. For example, the thickness of the bulk layer on the illumination side has to be thin to reduce the undesired photon absorption. Another design is based on heterostructures: if the *p*- and *n*-type regions are made of materials with wider bandgaps ($E_g > h\nu$), then they will be transparent to the photons absorbed in the *i*-layer ($E_g \leq h\nu$).

Besides the R_λ, another figure of merit of a photodetector is the I_{dark}, or the J_{dark}, which is the device leakage current without illumination. I_{d} is mainly induced by thermal generation within the depletion region and a few diffusion lengths on both sides of the depletion region. Typically the I_{dark} is quite low for WBG materials at room temperature (RT). Combining I_{dark}, R_λ, and the area of the device's optical window, there is an overall figure of merit named detectivity (D^*).



(a) (b)

Figure 2. Energy band diagram schematics of (a) a reverse-biased *p-i-n* photodiode, and (b) a *p-i-n* APD biased near the avalanche breakdown showing carrier multiplication by impact ionization.

A *p-i-n* APD is a highly sensitive *p-i-n* photodiode that operates in the avalanche regime to detect very weak optical signals. As shown in Figure 2 (b), when the APD is reverse-biased near the avalanche breakdown, one incident photon can create a number of EHPs through the impact ionization, thereby providing a very high R_λ. This carrier multiplication is known as the avalanche gain. To obtain a huge avalanche gain, a larger electrical field in the APDs' depletion region is preferred, so sometimes well-developed APDs have to be operated above the avalanche breakdown voltage. To protect the APDs from the large avalanche breakdown current, APDs are biased with short voltage pulses over the avalanche breakdown voltage and a current compliance is applied. This operation mode is called Geiger mode, which is particularly useful for single-photon detection. Single-photon detection efficiency (SPDE) and dark count probability (DCP) are two important figures of merit for the Geiger-mode operation. SPDE is the probability of detection of a single incident photon. DCP is the probability per pulse of error detection. The formulas and measurement methods for all the parameters mentioned above will be further discussed in Section 2.3.

2.2 Epitaxial Material Layer Structure

The GaN homojunction *p*-*i*-*n* APD layer structure is shown in Table 7. Detailed epitaxial material growth development and optimization have been reported earlier [23]. The substrates are *n*-type *c*-plane FS GaN substrates with electron concentrations of $\sim 1\times10^{18}$ cm^{-3}. The epitaxial growth starts from a 2.5-µm Si-doped GaN *n*-layer with a free-electron concentration of 5×10^{18} cm^{-3}, followed by a 280-nm unintentionally doped (UID) GaN *i*-layer with a background electron doping of 5×10^{16} cm^{-3}. The *p*-layer consists of a 100-nm Mg-doped GaN layer and a 20-nm highly Mg-doped GaN cap layer. The approximate free-hole concentration in the Mg-doped *p*-GaN layer is 1×10^{18} cm^{-3} based on previous growth calibrations [128].

Table 7. The layer structure of the GaN homojunction *p-i-n* APD in this study.

Layer	Material	Thickness (nm)	Free carrier concentration (cm^{-3})
p contact	GaN : Mg^{++}	20	$p = 2\times10^{20}$
p layer	GaN : Mg^{+}	100	$p = 1\times10^{18}$
i layer	GaN : UID	280	$n = 5\times10^{16}$
n layer	GaN : Si^{+}	2500	$n = 5\times10^{18}$
Substrate	*c*-plane FS GaN	-	$n \sim 1\times10^{18}$

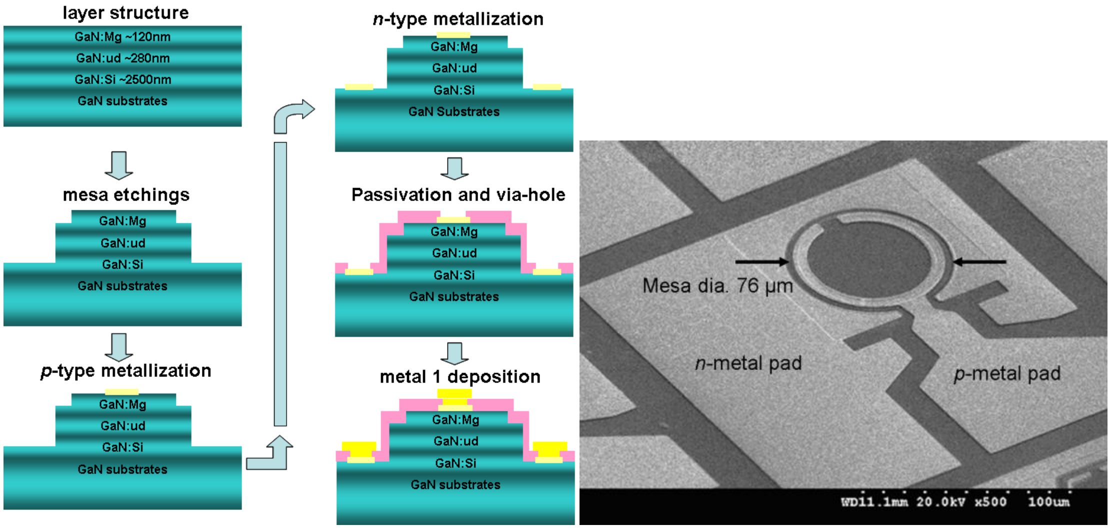
2.3 Device Fabrication

2.3.1 Fabrication Process Flow

The device fabrication process flow chart is shown in Figure 3 (a). An *i*-line contact aligner is used for the photolithography steps. The fabrication starts with two low-damage mesa etchings in an STS™ Multiplex inductively coupled plasma (ICP) etching system using Cl_2/He-based gas mixture. Electron-gun (e-gun) evaporated SiO_2 followed by a lift-off process serves as the etching mask. The first mesa etching keeps a thin *p*-layer (approximately 30 nm in thickness) on top of the *i*-layer to form a surface depletion region. The second mesa etching is a deep one to expose the *n*-layer. After that, a UV-assisted wet-etching surface treatment is applied to remove dry-etching-induced surface damages. The metal contact to *p*-type GaN uses an e-gun evaporated Ni/Ag/Ni/Au metal stack. The metal patterns are formed by lift-off process and annealed in a rapid thermal annealing (RTA) system for ohmic contact. Ti/Al/Ti/Au metal stack is deposited on the *n*-type GaN layer and the ohmic contact is achieved as deposit. The devices are then passivated with spin-on Benzocyclobutene (BCB) (3022-35, Dow Chemicals, Inc.). Another photolithography is applied to define the via hole patterns and an ICP etching is utilized to open these via holes on top of *p*- and *n*-metal with photoresist as the etching mask. Finally, a thick Ti/Au metal layer is evaporated to form wire-bonding pads. An SEM picture of a fully fabricated APD device is shown in Figure 3 (b).

The following sections will describe the development of several key fabrication processes. Two schemes have been developed to suppress the mesa sidewall leakage current. The first method is to recover the dry-etching-induced damages by using a UV-assisted wet-etching surface treatment technique. It removes the damaged surface materials by tenderly etching away several mono-layers of GaN atoms. The second method is a double-mesa structure (or a ledge structure) to form a surface depletion layer to reduce the electric field across the sidewall. As a consequence, the defects on the surface do not result in high leakage current.

Another issue for III-N bipolar device fabrication is the difficulty to achieve ohmic contact and low contact resistance on *p*-type III-N materials. The problem comes mainly from the difficulty of achieving high free-hole concentrations in III-N materials, and it also depends on the metallization process. Later in this chapter, the *p*-GaN metallization optimization aiming at a low contact resistance will be presented.


layer structure
GaN:Mg ~120nm
GaN:ud ~280nm
GaN:Si ~2500nm
GaN substrates
mesa etchings
GaN:Mg
GaN:ud
GaN:Si
GaN substrates
p-type metallization
GaN:Mg
GaN:ud
GaN:Si
GaN substrates
n-type metallization
GaN:Mg
GaN:ud
GaN:Si
GaN Substrates
Passivation and via-hole
GaN:Mg
GaN:ud
GaN:Si
GaN substrates
metal 1 deposition
GaN:Mg
GaN:ud
GaN:Si
GaN substrates
Mesa dia. 76 μm
n-metal pad
p-metal pad
WD11.1mm 20.0kV x500 100um

(a) (b)

Figure 3. (a) The fabrication process flow chart for GaN UV *p-i-n* APDs. (b) An SEM picture of a fabricated 76-μm-diameter (4536 μm^2) GaN UV *p-i-n* APD.

2.3.2 UV-assisted Wet-Etching Surface Treatment

Wet etching is widely used in the fabrication of semiconductor devices. Compared to dry etching, wet etching has the advantage of avoidance of plasma-induced surface damage. Because of the material inertness, UV illumination ($h\nu > E_g$) is required to generate EHPs for effective wet etching III-N materials. Several groups reported studies on KOH-based photo-enhanced chemical (PEC) wet etching [129-137] and KOH/$K_2S_2O_8$-based electrode-less UV-assisted wet etching [138-141] for III-N materials. Plenty of applications of the wet etching on III-N materials have been also reported, including rapid evaluation of defect density [142-144], LED surface roughening treatment [145], InGaN/GaN selective wet etching [146-148], and undercut structure formation [149-151].

Different from those applications, the goal here is to develop a post-dry-etching surface treatment using the wet-etching technique. This surface treatment is desired to remove dry-etching-induced damage by slightly wet etching several mono-layers of III-N atoms. The KOH/$K_2S_2O_8$-based electrode-less UV-assisted wet etching is chosen in this study because it does not need electrical contacts on the sample or an external electrode in the etchant to apply an electric bias. The chemical reaction equations have been given by [139]:

$$\mathrm{GaN} + \mathrm{photon} \rightarrow \mathrm{GaN} + \mathrm{e}^{-} + \mathrm{h}^{+} \tag{2.1}$$

$$\mathrm{GaN} + 3\mathrm{h}^{+} \rightarrow \mathrm{Ga}^{3+} + 1/2\mathrm{N}^{2} \tag{2.2}$$

$$\mathrm{S_2O_8}^{2-} + 2\mathrm{e}^{-} \rightarrow 2\mathrm{SO_4}^{2-} \tag{2.3}$$

$K_2S_2O_8$ works as an oxidant to consume electrons locally. Therefore, no electrode is needed and the etching rate is uniform. The wet etching condition needs to be carefully optimized for smooth surface morphology and low surface leakage, which is the key for the fabrication of high-performance III-N bipolar devices.

A 3-factor 2-level design of experiment (DOE) is conducted to determine the optimal wet-etching surface treatment recipe [38]. KOH concentration, $K_2S_2O_8$

concentration, and UV power are the three experimental variables with a two-level variation: high level (H) and low level (L). The detailed experiment parameters are listed in Table 8. An Oriel UV light source with a 1 kW mercury-xenon lamp is used to deliver the UV illumination. Eight samples are cut from a 2-inch *n*-type GaN wafer grown on a sapphire substrate. They are dry-etched in the STS™ Multiplex ICP system using the Cl_2/He-based gas mixture. The etching depth is 1000 Å. Each sample is randomly assigned to one etching condition. KOH and $K_2S_2O_8$ solutions are freshly prepared before each wet etching. All experiments are carried out at RT with a fixed etching time of 5 minutes.

Table 8. The experimental parameters in the DOE for the wet-etching surface treatment study.

	High level	Low level
KOH concentration	0.0005 M	0.00025 M
$K_2S_2O_8$ concentration	0.002 M	0.001 M
UV illumination power	900 W	600 W

The DOE output is the surface roughness improvement after the surface treatment. The surface root-mean-square (RMS) roughness is measured by atomic force microscope (AFM) before and after the surface treatment at the same locations on each sample. The surface RMS roughness improvement is defined in Equation 2.4. The full DOE table and results are summarized in Table 9.

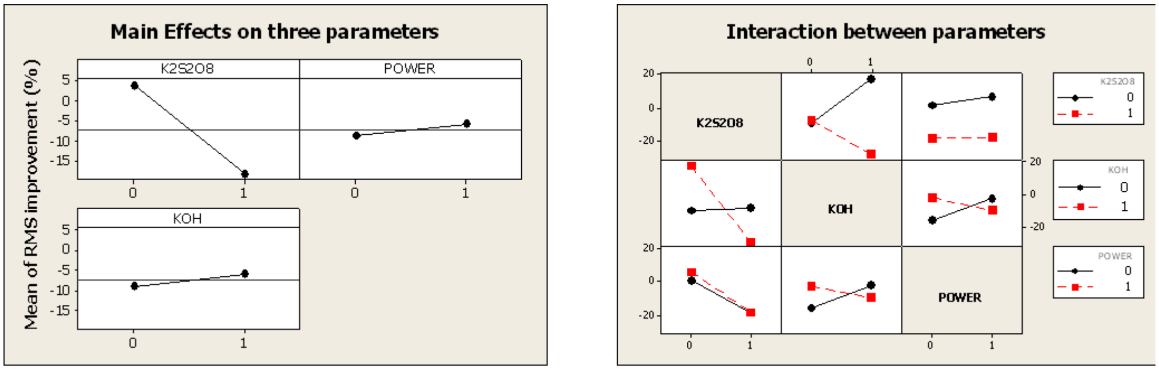
$$\Delta\mathrm{RMS}(\%) = \frac{\text{RMS before wet etching - RMS after wet etching}}{\text{RMS before wet etching}} \tag{2.4}$$

In Table 9, with proper choices of etching conditions, smooth surface can be achieved. However, some etching conditions result in worse surface roughness that corresponds to a negative ΔRMS, possibly because of aggressive etching on dislocation defects. To study the correlation between processing variables, analysis of variance

(ANOVA) is carried out using the Minitab® software. The main effects of KOH concentration, $K_2S_2O_8$ concentration, and UV lamp electrical power on the surface roughness improvement are plotted in Figure 4 (a). Their interactions with each other are plotted in Figure 4 (b).

Table 9. The DOE table in the wet-etching surface treatment study and the summary of the experiment response.

#	UV	KOH	$K_2S_2O_8$	RMS (nm) before wet etching	RMS (nm) after wet etching	ΔRMS (%)
1	H	L	L	0.390	0.378	3.07
2	H	H	L	0.385	0.348	9.61
3	H	L	H	0.315	0.340	-7.93
4	H	H	H	0.272	0.349	-28.3
5	L	L	L	0.281	0.344	-22.41
6	L	H	L	0.302	0.227	24.83
7	L	L	H	0.311	0.336	-8.03
8	L	H	H	0.266	0.333	-28.94



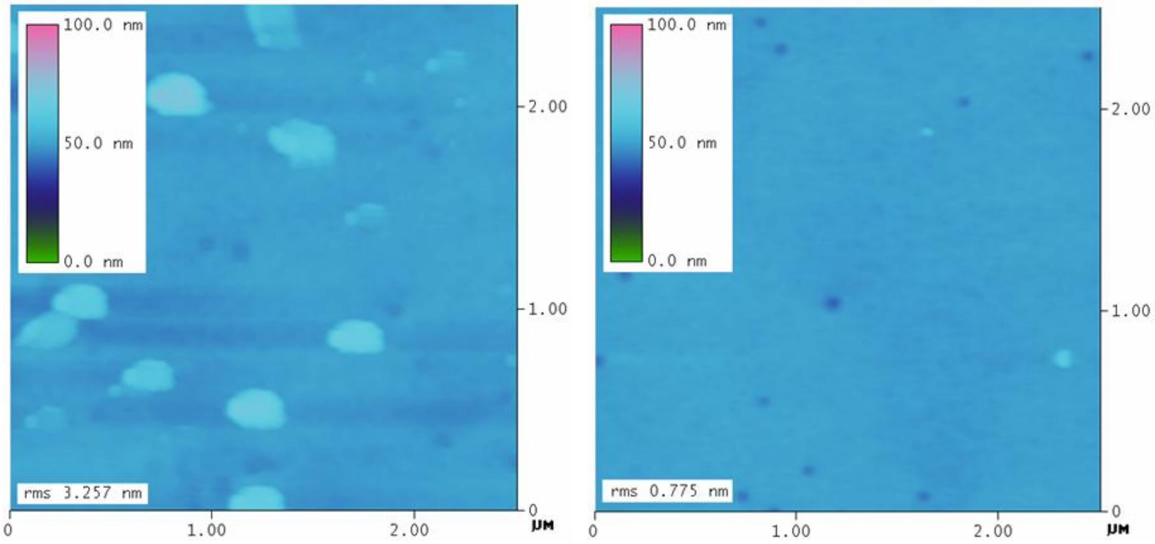
(a) **(b)**

Figure 4. (a) The main effects of KOH concentration, $K_2S_2O_8$ concentration, and UV illumination power on the surface roughness improvement. (b) The interaction between each two of KOH concentration, $K_2S_2O_8$ concentration, and UV illumination power.

In Figure 4 (a), “0” corresponds to the “L” level and “1” corresponds to the “H” level. The $K_2S_2O_8$ concentration has a significant effect: lowering the $K_2S_2O_8$ concentration can improve the surface smoothness. The other two variables, however, are not sensitive in this plot. Figure 4 (b) shows that $K_2S_2O_8$ and KOH have significant interaction. In etching conditions with a low $K_2S_2O_8$ concentration, a higher KOH concentration may yield smoother surface. On the other hand, if $K_2S_2O_8$ concentration is high, a higher KOH concentration produces a rougher surface. Based on this DOE, an effective wet-etching surface treatment can be achieved with a $K_2S_2O_8$ concentration in the vicinity of “L” level and a KOH concentration in the “H” level. The UV power however may not be a significant factor.

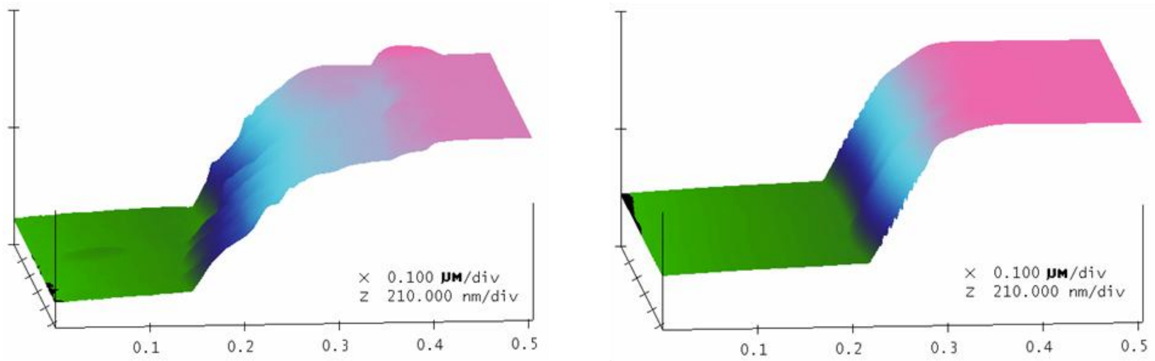
To evaluate the surface morphology modification effect of the wet-etching surface treatment, the optimized wet-etching recipe is applied on one dry-etched *n*-type GaN sample. AFM pictures before and after the surface treatment on the same location are shown in Figure 5 (a) and Figure 5 (b), respectively. In Figure 5 (a), some spikes are observed on the dry-etched surface probably due to the etching rate varies near the material dislocations. These spikes may act as surface leakage paths and greatly degrade the device performance. They are effectively removed by the wet-etching surface treatment, as shown in Figure 5 (b), and the surface roughness is improved by 75%. Figure 6 shows 3D AFM images of dry-etched mesa sidewall morphology from the same sample before and after the surface treatment. A smoother sidewall is obtained after the removal of several layers of dry-etching-damaged GaN atoms.

The effect of this wet-etching surface treatment on device electrical performance has been also studied. Two GaN *p-i-n* APD samples have been fabricated. They are from one wafer with the layer structure shown in Table 7 but on SiC substrates. The optimized wet-etching surface treatment is applied to Sample B, but not to Sample A. Their reverse-biased current-voltage (*I-V*) characteristics in dark condition are shown in Figure 7. They have similar I_{dark} when the reverse bias is lower than 15 V. Beyond 15 V, Sample A shows significantly increased I_{dark}.


100.0 nm
50.0 nm
0.0 nm
rms 3.257 nm
2.00
1.00
0
0
1.00
2.00
µm
100.0 nm
50.0 nm
0.0 nm
rms 0.775 nm
2.00
1.00
0
0
1.00
2.00
µm

(a) **(b)**

Figure 5. AFM images show the surface of a dry-etched *n*-type GaN sample (a) before and (b) after the optimized wet-etching surface treatment.


x 0.100 µm/div
z 210.000 nm/div
0.1
0.2
0.3
0.4
0.5
x 0.100 µm/div
z 210.000 nm/div
0.1
0.2
0.3
0.4
0.5

(a) **(b)**

Figure 6. 3-dimentional AFM images show a dry-etched mesa sidewall (a) before and (b) after the optimized wet-etching surface treatment.

On the other hand, with the proper wet-etching surface treatment condition, the I_{dark} of Sample B is reduced by at least one order of magnitude. In addition, Sample B’s avalanche breakdown voltage extends to a higher value. Clearly, this optimized wet-etching surface treatment technique is valuable for high-performance GaN *p*-*i*-*n* APDs.

This technique has been also applied to high-performance III-N-based HFETs [152] and HBTs [115]. A patent has been filed for this UV-assisted electrode-less wet-etching surface treatment technique [153].

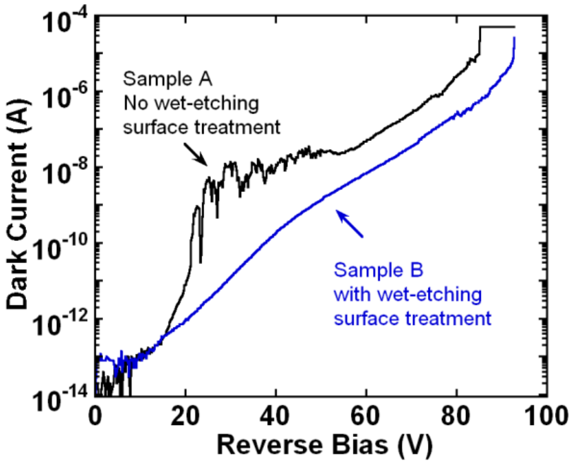


Figure 7. The comparison of reverse-biased I_{dark} of GaN *p-i-n* APDs. Sample A: without wet-etching surface treatment, Sample B: with the optimized wet-etching surface treatment.

2.3.3 Ohmic Contact Study on *p*-GaN

Low-resistance ohmic contacts are critical to high-performance semiconductor devices. However, achieving low-resistance ohmic contacts is a challenge for WBG materials, especially for *p*-type III-N materials due to the difficulty in *p*-type doping and the high dopant activation energy required. To obtain ohmic contact to *p*-GaN, metals with large work functions (> 5 V), such as Ni, Pd, or Pt are used as the direct contact layer to the III-N materials. In the development of InGaN-based LEDs in early 2000's, the widely used scheme to form the *p*-GaN ohmic contact is a thin Ni/Au metal stack annealed at 400 ~ 750 ℃ in air or O_2 ambient. Numerous papers have reported specific contact resistances (ρ_c) in 10^{-2} ~ 10^{-4} Ω cm^2 [154-164]. Most of these papers pointed out that the oxidized Ni/Au plays an important role in improving *p*-GaN metal contact quality. Another advantage of this thin Ni/Au scheme is that the film is highly transparent to the short wavelength light emitting from the InGaN-based LEDs, thereby not blocking the optical output from the LED top mesa.

Because of the development of the flip-chip bonding technique for high-brightness LED packaging, the high optical reflectance, instead of the high transparent, became a requirement for the *p*-metal. Since 2003, Ni/Ag-based metal stacks annealed in air or O_2 ambient for *p*-GaN ohmic contact have been widely reported, showing lower ρ_c [165-171] than the Ni/Au metallization. The Ag layer helps absorbing Ga from the *p*-GaN surface. As a result, Ga vacancies are generated near the *p*-GaN surface, thereby increasing the free-hole concentration at the metal-semiconductor interface and forming the tunneling contacts.

In this study, an e-gun evaporated Ni/Ag/Ni/Au metal stack is applied as the ohmic contact to *p*-GaN. The Au layer acts as a protection layer for smoother metal surface and better thermal stability. The Ni layer between Au and Ag is a diffusion blocking layer. The transmission line measurement (TLM) is used to estimate sheet resistance (R_{sh}) and ρ_c. *I*-*V* curves are measured across 40 μm×80 μm pads with 32, 16, 8, 4-μm spaces. By linear fitting, the typical *p*-GaN R_{sh} of the in the GaN *p*-*i*-*n* APDs is 100 KΩ/□, and the ρ_c is 2×10^{-3} Ω cm^2.

2.3.4 Ohmic Contact Study on *n*-GaN

Compared to *p*-type GaN, forming a low-resistance ohmic contact is much easier on *n*-type GaN because of the high free-electron concentration. Ti/Al-based contacts with ρ_c of 10^{-5} ~ 10^{-6} Ω cm^2 have been demonstrated on *n*-type GaN in 1990's [172,173]. In this Ti/Al-based metal contact scheme, N out-diffuses from the GaN lattice and forms

TiN with Ti. The accumulated N vacancies at the *n*-GaN surface act as donors, providing the heavy *n*-doped configuration that is required for tunneling contacts.

In this study, an e-gun evaporated Ti/Al/Ti/Au metal stack is applied as the ohmic contact layer to *n*-GaN. No annealing is needed since the ohmic contact is achieved as deposit. The typical *n*-GaN R_{sh} and ρ_c are 34 Ω/□ and 7×10^{-5} Ω cm^2, respectively. The ρ_c is overestimated here due to the cable resistance and probing resistance. A four-probe method can be used to eliminate these external resistances, which will be further discussed in Section 4.3.2.

2.4 Device Characterization

Fabricated GaN *p*-*i*-*n* APDs are characterized using an on-wafer d.c. probe station in a Faraday cage to reduce environmental noise. The d.c. *I*-*V* characterization is carried out using a Keithley 4200 semiconductor characterization system (SCS-4200) with low-current pre-amplifiers. The light source for the photo response testing is a Newport Apex Illuminator with a 150 W Oriel xenon lamp (ozone-free), providing illumination from 200 nm to 2400 nm with a stable optical output. A Newport Cornerstone 260 monochromator system is used to select single wavelengths. The optical signal is coupled into a 50-µm-diameter UV fiber and illuminated onto the device mesa from top.

2.4.1 Responsivity

Figure 8 shows the schematic drawing of the spectral responsivity measurement system. An HP VEE program is used to control the instruments and to acquire data through the general purpose interface bus (GPIB). An optical chopper is attached to the output window of the Newport Apex Illuminator to modulate the light with a 100 Hz signal, so the APD photo current is also 100-Hz modulated and can be picked up using a lock-in amplifier. The modulated illumination light enters a ¼-m Cornerstone™ 260 monochromator system (Newport 74100) for the single-wavelength selection. The 1200 l/mm holographic grating (Newport 74162) in the monochromator has a wavelength resolution of 0.10 nm with a primary wavelength region from 180 nm to 650 nm. After the single-wavelength selection, the optical beam is split by a 50/50 beam splitter. One beam is collected by a UV-enhanced Si photodetector (Hamamatsu Inc. S2281-04) for the optical power monitoring. The other one is coupled into a 50-µm-diameter UV fiber through a UV lens. The other end of the fiber is mounted on a micromanipulator and placed on top of the APD optical window. A Stanford Research DSP two-channel lock-in amplifier (SR 830) is used to pick up the photocurrent from the diode current, so the background noise can be filtered.

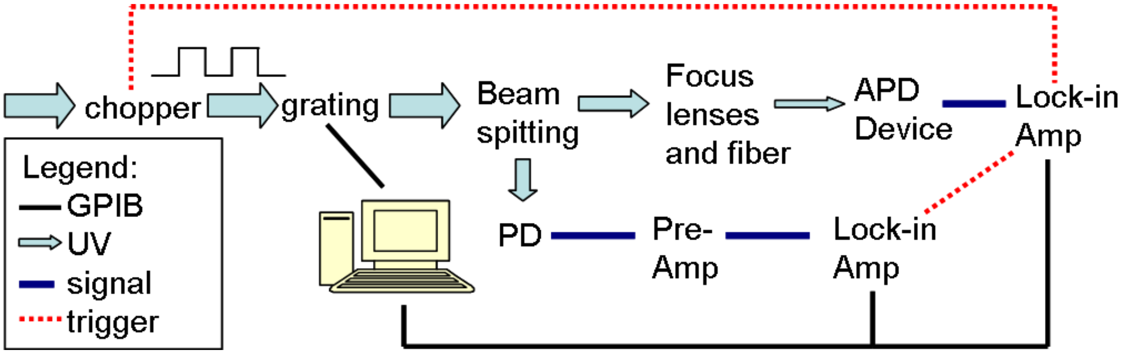
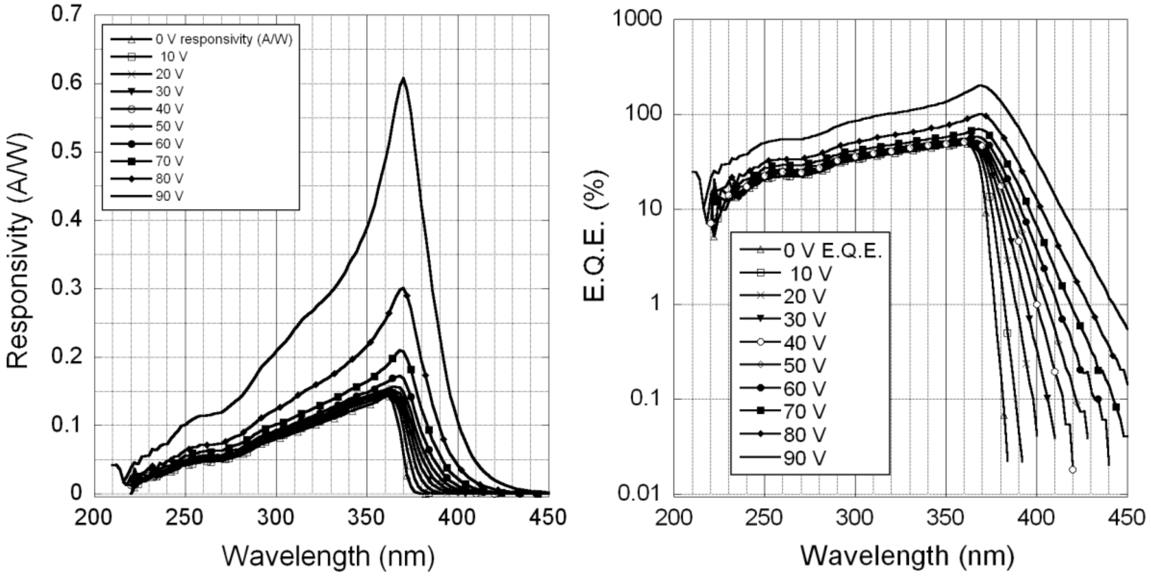


Figure 8. The schematics of the spectral response measurement system.

Figure 9 (a) shows the bias-dependent R_λ of a 100-µm-diameter GaN *p-i-n* APD (wafer ID: 1-1206-1) at RT [32]. This device has a breakdown voltage of -98 V without micro-plasma observed on the sidewall. At zero bias, R_λ of 143 mA/W peaks at λ = 364 nm with a cutoff wavelength at 380 nm, demonstrating the filter-free visible-blind UV detection. This zero-biased R_λ is higher than those of many other published III-N photodiodes [20-22,24,29,174-177]. An increased R_λ is expected if a thinner *p*-GaN layer is used, or, by a recessed optical-window approach during the device fabrication [28]. On the other hand, however, the *p*-GaN layer cannot be too thin, otherwise the tunneling effect will dramatically increase the I_d when the reverse bias is high [16].



(a) **(b)**

Figure 9. (a) The bias-dependent R_λ of a 100-µm-diameter GaN *p-i-n* APD at RT. (b) The bias-dependent EQE of the same device. Wafer ID: 1-1206-1.

In Figure 9 (a), with the increased reverse bias, the R_λ peak shifts slightly from 364 nm to 370 nm because of the Franz-Keldysh effect. Below -60 V, the magnitude of R_λ rises slowly with the reverse bias because the depletion region gradually expands into the *p*-GaN. Beyond -60 V, the increasing of the R_λ becomes steep because of the impact-ionization-induced carrier multiplication in the depletion region. Significant photo current gain is observed when the reverse bias is greater than -80 V. In addition, the absorption band shows significant broadening and red shifting at high reverse biases, indicating that the depletion region extends into the doped *p*-GaN [25]. This situation is different from most narrow bandgap *p*-*i*-*n* diodes whose the depletion region can be well-confined in the intrinsic layer due to the high *p*-type doping.

The bias-dependent external quantum efficiency (EQE) curves of the same device are shown in Figure 9 (b) [32]. Under a bias of -60 V, EQEs are 25.8%, 29.0%, and 55.9% at 265 nm, 280 nm, and 360 nm, respectively, and the peak EQE value is 57.6% at 364 nm.

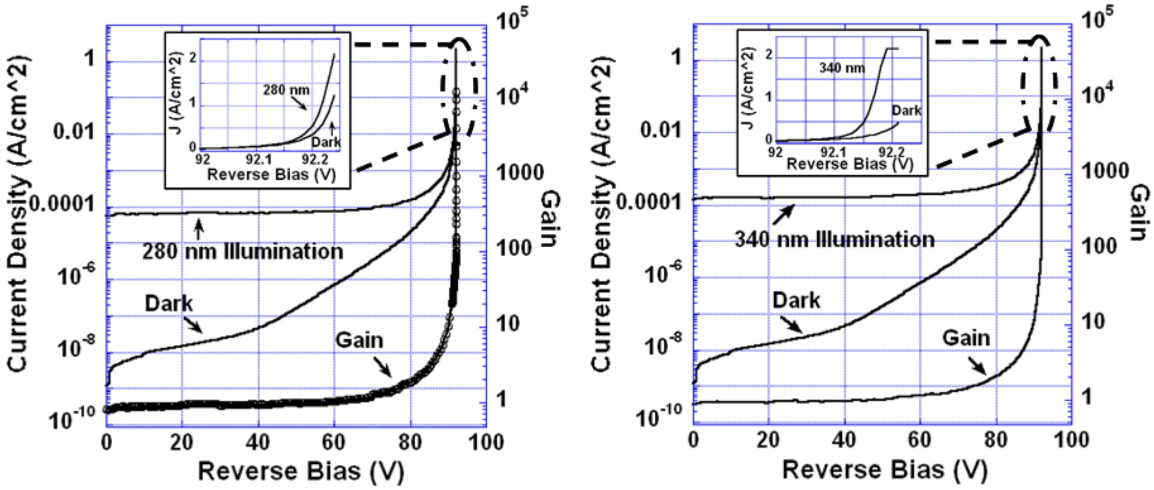
2.4.2 Photo Current Avalanche Gain

As shown in Figure 10, reverse-biased *I*-*V* characteristics of a 76-μm-diameter GaN *p*-*i*-*n* APD (wafer ID: 1-0907-5) are carried out from 0 V to the breakdown voltage for both I_{dark} and I_{p}. The breakdown voltage is -92.3 V, so the corresponding material breakdown field is 5.2 MV/cm if assuming that most of the voltage drops on the *i*-layer and the electric field has a triangle shape. I_{p} keeps approximately constant up to -60 V, at which bias the impact ionization starts to greatly amplify the photon-generated EHPs.

The photo current avalanche gain is defined as:

$$\text{Avalanche Gain} = \frac{\mathrm{I_p - I_{dark}}}{\mathrm{I_{p(unity)} - I_{dark(unity)}}} \tag{2.5}$$

Figure 10 (a) and (b) show photo current avalanche gains at 280-nm illumination and 340-nm illumination, respectively. Avalanche gains > 10^4 are achieved for both 280-nm illumination [25] and 340-nm illumination [27].

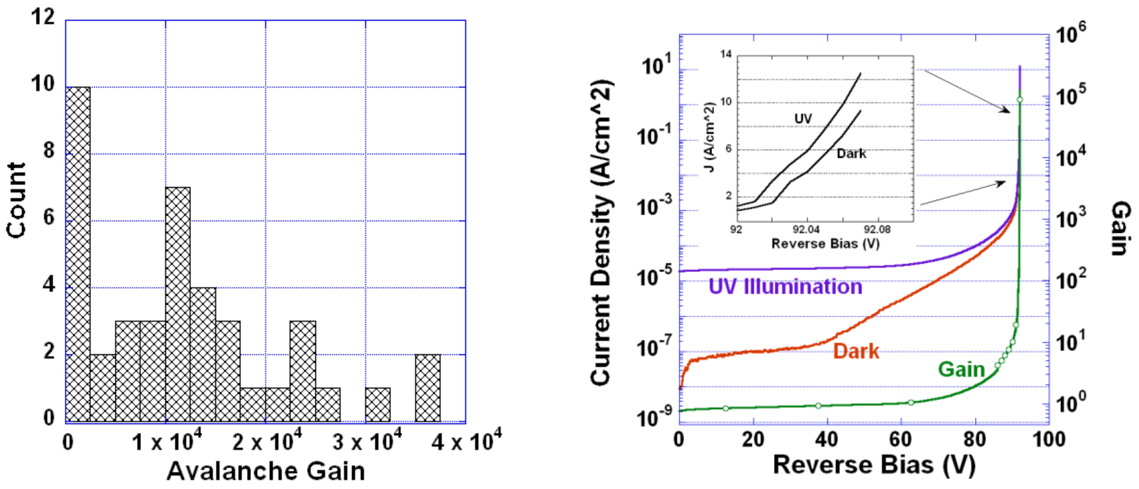


(a) (b)

Figure 10. Reverse-biased *I-V* characteristics of a 76-μm-diameter GaN *p-i-n* APD with and without UV illumination and the corresponding photo current avalanche gain for the (a) 280-nm illumination and (b) 340-nm illumination. Wafer ID: 1-0907-5.

Figure 11 (a) shows a histogram for the avalanche gains on 40 different-sized GaN *p-i-n* APDs measured on an 8×8 mm^2 sample (wafer ID: 1-0907-5) [27]. As shown in this graph, 75% devices under test (DUT) show avalanche gains > 2500 and 55% DUT show avalanche gains >10^4. The results also suggest that devices with smaller mesa areas have high possibility to achieve high avalanche gains. Therefore, reducing the material defects may play a critical role in further device performance improvement.

On the same sample, one 570 um^2 APD demonstrates an avalanche gain > 10^5 at λ = 360 nm. This value is among the highest photo current avalanche gains for III-N APDs reported to date. Reverse-biased *I-V* characteristics for I_p and I_{dark} as well as the corresponding avalanche gain of this device are shown in Figure 11 (b).



(a) (b)

Figure 11. (a) A histogram showing photo current avalanche gains on 40 different-sized GaN *p-i-n* APDs measured on an 8×8 mm^2 sample. (b) Reverse-biased *I-V* characteristics of a 570-μm^2 GaN *p-i-n* APD with a record avalanche gain > 10^5 at λ=360 nm. Wafer ID: 1-0907-5.

2.4.3 Geiger-Mode Operation

The DUV Geiger-mode operation of a 16-μm-diameter GaN visible-blind *p-i-n* APD (wafer ID: 2-1283-1 with recessed BCB on the optical window) has been demonstrated with the help from Prof. Joe Campbell's group at the University of Virginia. A gated quenching circuit is used and its schematic is shown in Figure 12. Detailed system setup can be found in [17]. During the Geiger-mode operation, the APD is reverse-biased by a d.c. voltage below the breakdown voltage, plus an alternating current (a.c.) pulse that makes the overall bias above the breakdown voltage, waiting for avalanche events. The effective a.c. pulse width is 1 nanosecond and its amplitude is 12 V, while the d.c. voltage varies for bias-dependent device performance. Avalanche events initiated by either UV photons or thermal carriers increase diode current up to a certain limit, which can be determined by the external circuit and registered to a counter. After that, the quenching circuit sets the d.c. bias a value to make the total bias below breakdown, thereby lowering the diode current to avoid device damage, and then the d.c.

bias is increased to the original value again, preparing the APD for the next photon detection pulse. In this study, the Geiger-mode testing is carried out at RT with the room lights turned off. A pulsed 265-nm UV laser with a repetition frequency of 7.2 kHz from a mode-locked tripled neodymium-doped yttrium aluminum garnet (Nd:YAG) laser is used as the light source. The estimated average number of photons per laser pulse is ~ 4.8.

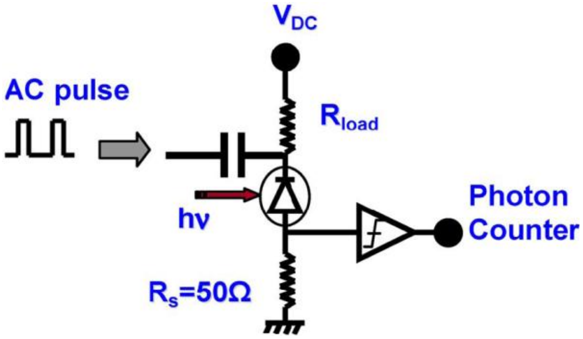


Figure 12. The quenching circuit schematic of the Geiger-mode APD testing system in the University of Virginia [17].

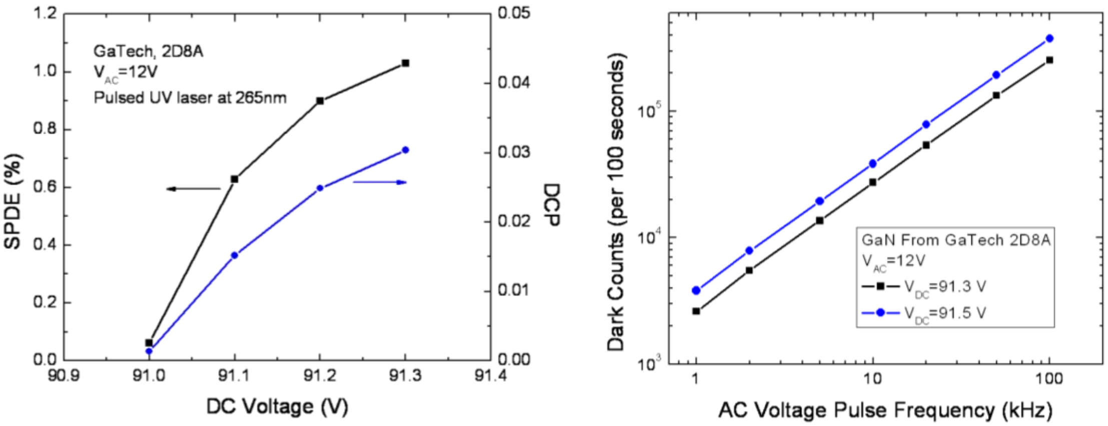
SPDE and DCP are the two most important figures of merit for the single photon detection. SPDE is the probability of detecting a single incident photon, and its expression is shown in Equation 2.6 [17], where η_{ex} is the EQE at the given wavelength, P_a (avalanche probability) is the probability that the photon-generated EHPs will initiate a detectable avalanche event, N_{light} and N_{dark} are the number of avalanche event counts per second with and without light illumination, f_{rep} is the laser repetition frequency, and ν is the number of photons per laser pulse. DCP is the probability of an error detection per laser pulse due to thermal-excited EHPs, and it is expressed in Equation 2.7 [17].

$$\text{SPDE} = \eta_{ex}P_a = -\ln\left(\frac{1-N_{light}/f_{rep}}{1-N_{dark}/f_{rep}}\right)/\nu \tag{2.6}$$

$$\text{DCP} = N_{dark}/f_{rep} \tag{2.7}$$

Both SPDE and DCP are strongly related to the excess voltage. Figure 13 (a) shows the SPDE and DCP as functions of the d.c. bias [31]. SPDE and DCP increase with the d.c. bias. The peak SPDE is 1.0% with a DCP of 0.03 under an overall bias of 103.3 V (d.c. bias of 91.3 V). This is the first demonstration of front-side-illuminated III-N Geiger-mode deep UV APD on *c*-plane FS GaN substrates. The EQE of this device at 265 nm is 22%, which is roughly twice that of a PMT at the same wavelength. An SPDE of 1.0% with an EQE of 22% indicates a P_a of 4.5% according to Equation 2.6.

Usually the SPDE and DCP are independent with the a.c. bias pulse repetition frequency. However, it is not true if there are many deep-level trap centers in the APD. If the a.c. bias pulse repetition period is too short (comparable to the trapped carrier's lifetime), the release of trapped carriers will trigger undesired avalanche events during the detection cycle, and an increase of the dark count rate (N_{dark} per a.c. bias pulse) over thermal carrier level will appear, which is the so-call after-pulsing effect. In this study, the after-pulsing effect is characterized by measuring the device dark count rates with different a.c. pulse repetition frequencies. Figure 13 (b) shows the dark counts versus the a.c. pulse repetition frequency in a time duration of 100 seconds with the d.c. biases of 91.3 and 91.5 V [31]. Up to 100 KHz, the dark counts increase linearly with the a.c. pulse frequency, suggesting no after-pulsing effect in this frequency range. Therefore, the DCP only depends on thermal-generated carriers, not the deep-level trapped centers. It means that the measured low P_a and relatively high DCP are not resulted from the material defects or process-induced surface states, but are primarily related to the device layer structure that needs to be further optimized toward better impact ionization process.



(a) **(b)**

Figure 13. (a) SPDE and DCP of a 16-μm-diameter GaN DUV *p-i-n* APD. (b) Dark counts versus a.c. bias pulse repetition frequency in a time duration of 100 seconds, showing consistent dark count rates. Wafer ID: 2-1283-1.

2.4.4 Effective Detectivity

This section describes the device performance when working as a low-noise UV photodiode at the zero-biased and low-reverse-biased regions, showing record-low J_{dark} and record-high D^*.

The reverse-biased *I-V* characteristics of an 80-μm-diameter GaN *p-i-n* APD (wafer ID: 2-1283-6) without and with different-power UV illuminations are shown in Figure 14 (a) [34]. The I_{dark} slightly decreases with the reverse bias from 0 V to -20 V until reaching the system noise floor. This trend is different from that of a typical diode whose I_{d} monotonically increases with the reverse bias. This phenomenon may be due to the double-mesa structure (the ledged *p*-layer) and can be explained as follows. I_{d} is mainly from the thermal-generated EHPs within the space-charge region and the surface leakage current on the plasma-etched mesa sidewall. Under the low-reverse-biased condition, the bulk leakage current may not be significant when compared to the surface leakage current. When the reverse bias increases, the ledged *p*-layer is more depleted. As a result, the surface leakage current goes down. When the ledged *p*-layer is fully depleted (at -20 V in this case) the surface leakage path will be effectively isolated, and the overall I_d will reach its minimum. If the reverse bias continuously increases, the thermal-generation dark current within the bulk space-charge region becomes significant and leads to a monotonic I_{dark} increase.

As shown in Figure 14 (a), the measured I_d less than 2 fA (or an equivalent J_{dark} of 40 pA/cm^2) is achieved at -10 V to -30 V. It is the lowest J_{dark} reported to date for III-N photodiodes. It also shows that the photodiode can clearly resolve an incident optical power as low as 100 fW at λ = 360 nm. The "sweet spot" for low-noise photodiodes could be achieved at -20 V, where the I_{dark} reaches its minimum. The two important figures of merit for noise performance are *NEP* and *D**. *NEP* is defined as the incident RMS optical power required to produce a signal-to-noise ratio of unity in a 1-Hz bandwidth [3]. *NEP* and *D** can be calculated according to Equation 2.8 and Equation 2.9, respectively [3].

$$NEP = \frac{\sqrt{2qI_{dark} + 4kT/R_V}}{R_\lambda} \ (\mathrm{WHz^{-0.5}}) \tag{2.8}$$

$$D^* = \frac{\sqrt{A}}{NEP} \ (\mathrm{cmHz^{0.5}W^{-1}}) \tag{2.9}$$

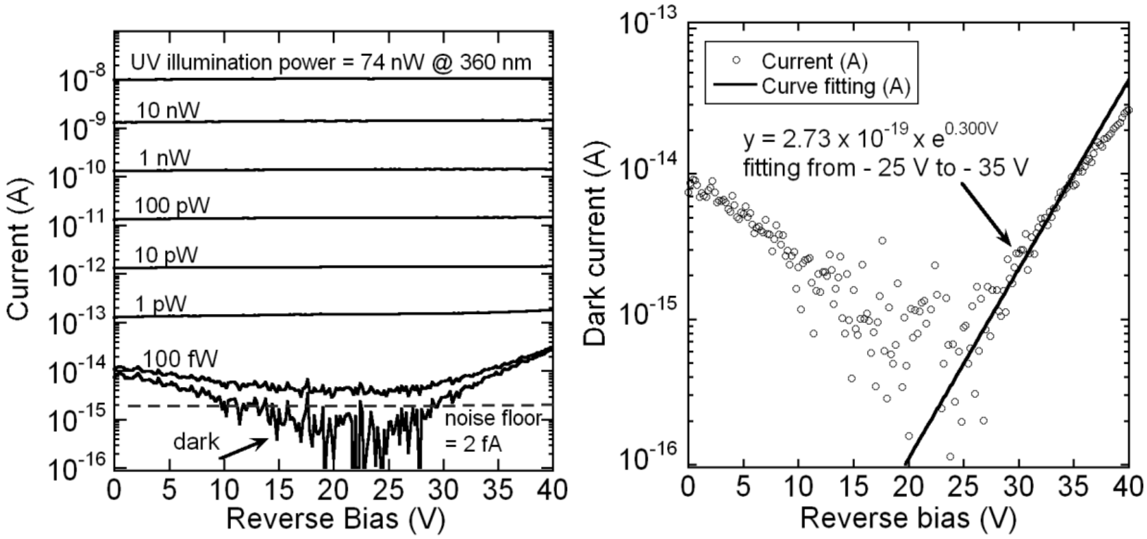
R_V is the device differential resistance and A is the mesa area. R_λ is the responsivity at the selected optical wavelength (140 mA/W @ λ = 360 nm in this case). As shown in Figure 14 (b), R_V and I_{dark} are extracted by curve fitting of the measured dark current curve from -25 V to -35 V.

The fitted *I-V* relationship is shown in Equation 2.10. At -20 V, $R_V = 3.03\times10^{16}\ \Omega$ is obtained by $(\partial I/\partial V)^{-1}$ as shown in Equation 2.11. The fitted I_{dark} is 1.10×10^{-16} A as shown in Equation 2.12. The corresponding RT (293K) *NEP* is 4.27×10^{-17} W-Hz$^{-0.5}$ and the D^* is 1.66 $\times 10^{14}$ cm-Hz$^{0.5}$-W^{-1} at λ = 360 nm. The *NEP* and D^* values are the best values reported to date for GaN visible-blind UV *p-i-n* photodiodes operating at reverse biases.

$$I = 2.73\times10^{-19}e^{0.300V}\,. \tag{2.10}$$

$$R_0\,|_{V=20} = (\partial I/\partial V)^{-1}\,|_{V=20} = 1/(2.73\times10^{-19}\times0.300\times\exp(0.300\times20)) = 3.03\times10^{16}\Omega \tag{2.11}$$

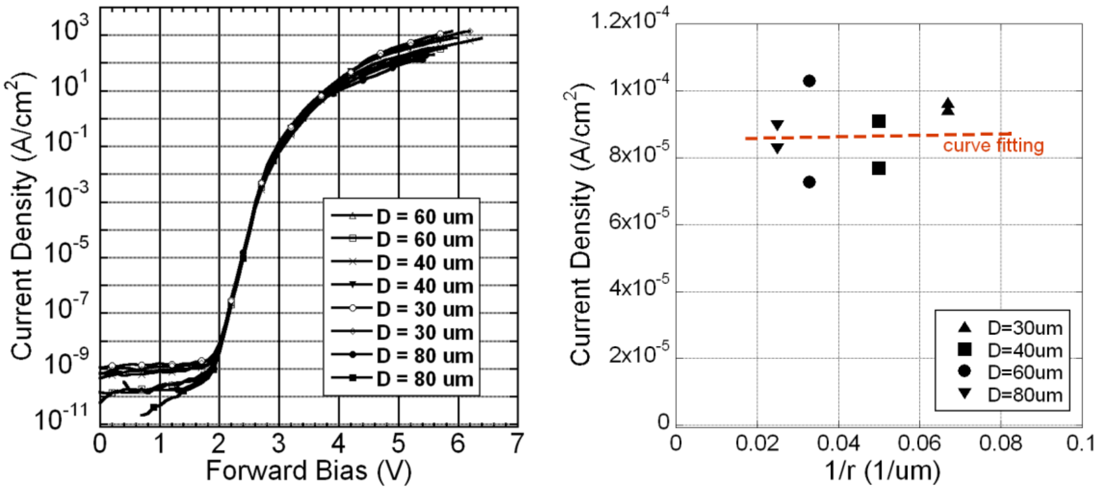
$$I(V=20) = 2.73\times10^{-19}e^{0.300*20} = 1.10\times10^{-16}(A) \tag{2.12}$$



(a) **(b)**

Figure 14. (a) Reverse-biased *I-V* characteristics of an 80-μm-diameter GaN *p-i-n* APD without and with UV illumination at λ = 360 nm. (b) Curve-fitting of the measured dark current data from -25 V to -35 V to estimate R_V and I_{dark}. Wafer ID: 2-1283-6.

Figure 15 (a) shows the forward-biased *I-V* characteristics of different-sized GaN *p-i-n* APDs (wafer ID: 2-1283-6). Eight devices with four different mesa diameters are taken randomly from a 1×1 cm^2 sample. These devices show very low current density (< 2 nA/cm^2) before junction turn-on, indicating high epitaxial quality and low surface leakage. Ideality factors have a mean value of 2.01 with a standard deviation of 0.01, suggesting that the space-charge recombination dominates the carrier transport. The increased current density deviation in the series-resistance region is possibly due to the non-uniform current distribution as the device diameter increases.



(a) **(b)**

Figure 15. (a) Forward-biased *I-V* characteristics of different-sized GaN *p-i-n* APDs. (b) Current densities versus inverse of the device radii at a forward bias of 2.5 V. Wafer ID: 2-1283-6.

To further study the locations of the space-charge carrier recombination, device forward-biased current can be expressed as Equation 2.13. Equation 2.14 is derived form Equation 2.13 by dividing the device mesa area on both sides. As shown in Figure 15 (b), forward-biased current densities of those eight devices at a bias of 2.5 V are plotted as a function of the inverse of device radius [178]. The trend of the curve fitting is flat, indicating that the recombination current density is not sensitive to the mesa sidewall. Therefore, clearly, the surface generation-recombination centers induced by the process have been effectively removed by the wet-etching surface treatment, or isolated by the ledge *p*-layer structure.

$$I = J_{bulk} \times area + J_{sidewall} \times perimeter \tag{2.13}$$

$$J = J_{bulk} + J_{sidewall} \times 2/radius \tag{2.14}$$

2.5 Summary

High-performance Geiger-mode GaN *p-i-n* DUV APDs grown on *c*-plane FS GaN substrates have been fabricated and characterized. Significant surface leakage current suppression is achieved through the use of an optimized wet-etching surface treatment as well as a ledged *p*-layer structure.

SPDE of 1.0 % and DCP of 0.03 at $\lambda = 265$ nm are demonstrated in the Geiger-mode operation on a 16-µm-diamter APD. This is the first Geiger-mode DUV GaN APD reported using a front-illuminated homojunction *p-i-n* structure grown on a FS GaN substrate. Furthermore, a 570 um^2 APD shows a photo current avalanche gain > 10^5 at $\lambda = 360$ nm, which is the highest avalanche gain for III-N APDs reported to date. At the DUV wavelength of 280 nm, a photo current avalanche gain greater than 10^4 is also achieved.

These APDs are also low-noise, high-sensitivity UV photodiodes under zero-bias and low-reverse-bias conditions. An 80-µm-diameter APD shows J_{dark} lower than 40 pA/cm^2 at -20 V and R_λ of 0.140 A/W at 360 nm. *NEP* of 4.27×10^{-17} W-Hz$^{-0.5}$ and record D^* of 1.66×10^{14} cm-Hz$^{0.5}$-W^{-1} are also obtained at RT.

CHAPTER 3

DEVELOPMENT OF INGAN-BASED LASER DIODES

The goal of this project is to develop InGaN/GaN MQW current-injected edge-emitting LDs with a lasing wavelength > 500 nm. The epitaxial structures were grown in the AMDG group supervised by Prof. Russell D. Dupuis at Georgia Tech. Materials were grown on *c*-plane FS GaN substrates by the low-pressure MOCVD technique using a Thomas Swan reactor system equipped with a close-coupled showerhead growth chamber. The research described in this chapter mainly focuses on the device fabrication and characterization. The research results have been published in [67,68,87,88].

The first part of this chapter presents the development of fabrication process of InGaN/GaN MQW LDs. In the second part, the CW-mode lasing at 420 nm is realized at RT. A step-graded $Al_xGa_{1-x}N$ EBL is studied and its efficacy on device performance is investigated with respect to stimulated emission properties, η_i, α_i, and temperature-dependent characteristics. In the third part, to achieve longer wavelength InGaN/GaN MQW LDs, LD structures with $In_{0.03}Ga_{0.97}N$ waveguides and a tapered $Al_xGa_{1-x}N$ EBL were grown. The CW-mode lasing at 460 nm is achieved at RT.

3.1 Basic Device Physics

In semiconductors, as shown in Figure 16, there are four basic electron-hole recombination/generation and photon emission/absorption mechanisms: (a) spontaneous recombination (photon emission), (b) stimulated generation (photon absorption), (c) stimulated recombination (coherent photon emission), and (d) non-radiative recombination (phonon generation) [179]. The spontaneous recombination is the primary mechanism within an LED, which is a semiconductor bipolar device that emits light under a forward bias. Electrons and holes are injected via *p*-type and *n*-type metal contacts, respectively, and recombine across the junction and releases energy in the form of light (photons). The photon's λ is determined by the E_g of the material where the spontaneous recombination happens.

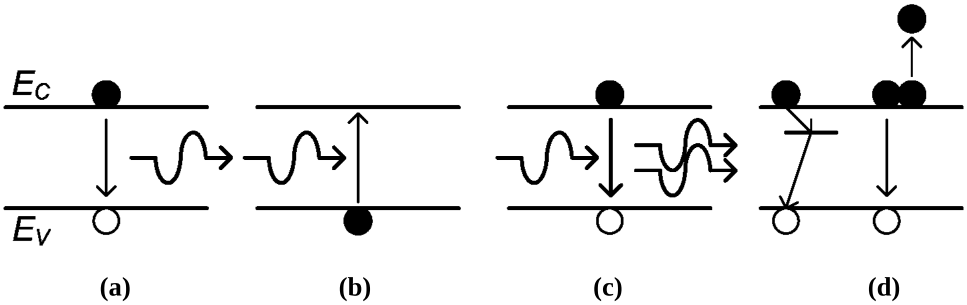


Figure 16. Carrier transition mechanisms between the conduction band and valence band in semiconductors: (a) spontaneous recombination, (b) stimulated generation, (c) stimulated recombination, and (d) non-radiative recombination.

In practice, indirect-bandgap semiconductors are not suitable for high-efficient light emitters because the major electron-hole recombination mechanism is non-radiative recombination that wastes much energy by heating the lattice. On the other hand, however, in direct bandgap semiconductors, non-radiative recombination still exists mainly in two mechanisms as shown in Figure 16 (d). The first mechanisms is the Shockley-Read-Hall (SRH) recombination involving material impurities that induce intermediate energy levels and act as non-radiative recombination centers. The second one is the Auger recombination.

To quantitatively describe the recombination process, R_{sp}, R_{12}, R_{21}, and R_{nr} are used to present the recombination rates for spontaneous recombination, stimulated generation, stimulated recombination, and non-radiative recombination, respectively. Clearly, to achieve high-efficient light emitters, the R_{sp} needs to be enhanced. The most important way to accomplish this is a double-heterostructure (DH), in which a narrow-bandgap material is sandwiched between two larger-bandgap materials. A potential well is then formed at the narrow-bandgap layer, where the electrons and holes are confined together, thereby increasing their recombination probability. The heterojunction idea and its implementation in LDs earned Herbert Kroemer and Zhores Alferov the 2000 Nobel Prize in physics. If the narrow-bandgap material in the DH structure is thin enough (typically a few nanometers), a QW is formed. It confines carriers more tightly than a bulk DH structure because of the quantum-confinement effect. The QW is one of the most important structures in modern LEDs and LDs. Furthermore, multiple quantum-well (MQW) structures are also commonly used today to provide more energy states in the active region.

Although the R_{sp} can be increased by using the QW structure, it has to be noticed that the R_{nr} may be increased as well. To reduce the R_{nr}, efforts have to be placed on reducing the material defect density and suppressing the Auger recombination.

R_{21} and R_{12} are not considered in the LEDs as less important factors. But the condition is different for LDs whose primary mechanism is the stimulated recombination. Simply speaking, a LD is a kind of LED that utilizes the spontaneous-recombination-generated photons to trigger the stimulated coherent photon emission, working in proper forward-biased conditions. A major advantage of the semiconductor LDs is that they can be driven directly by an electrical current, as opposed to many other gas or solid-state lasers that typically need external optical pumping.

In LDs, the stimulated recombination and stimulated generation are competing effects, and the net stimulated photon generation rate is given by [179]:

$$R_{st} \equiv R_{21} - R_{12} \tag{3.1}$$

A LD is functional only when the R_{st} is positive. This condition requires a forward bias across the active region greater than the semiconductor's E_{g} [179]. In this case, huge amounts of electrons and holes are injected into the active region, which is analogous to the population inversion condition in general lasers. So, different with LEDs, LDs work under a much higher current injection density. Another difference is that LDs demand good optical confinement around the active region, while LEDs not. R_{st} is proportional to photon density (N_{ph}) since R_{21} and R_{12} are proportional to the N_{ph}. Photons outside the active region cannot contribute to the optical gain. Therefore, the overlap of the active region and the optical field has to be maximized.

The optical confinement in the transverse directions is done in two ways. The first way is growing waveguides and cladding layers on both sides of the active region. The active region and waveguides must have higher refraction indices (n) than the cladding layers to confine the photons. The second way involves the LD device design and fabrication. The LD's mesa is usually designed to be a long rectangle shape with a long length and a narrow width, as opposed to typical LEDs with square mesas, thereby serving as an optical waveguide.

In edge-emitting LDs, the optical confinement in the longitudinal direction is required in hopes of that photons can pass through the LD cavity more times resulting in more stimulated emission. The longitudinal optical confinement is achieved by cleaving the emitting edges of the LDs. Sometimes, especially for narrow E_{g} materials, the difference in *n* at the air-semiconductor interface is sufficient to provide enough reflectance. But for WBG materials high-reflectance mirrors usually need to be deposited onto the cleaved facets to further enhance the reflection.

Important parameters of LDs include lasing wavelength (λ), threshold current (I_{th}), threshold current density (J_{th}), threshold voltage (V_{th}), slope efficiency, wall-plug efficiency (WPE), internal quantum efficiency (η_{i}), and internal loss (α_{i}). The characterization methods of these parameters will be further discussed in Section 3.3 and 3.4.

3.2 Device Fabrication

For the edge-emitting semiconductor LDs, there are two basic schemes for the lateral optical confinement and carrier confinement: the gain-guided structure and the ridge structure [179]. The gain-guided structure is easy in fabrication because of no mesa etching. The lateral carrier confinement is provided by the narrow metal strips. But the confinement is weak due to the carrier spreading. The optical confinement induced by the carrier injection is even weaker. Therefore, the device performance is limited with the gain-guided structure, which is rarely reported recently except for the Osram group [59,66,180]. On the other hand, the ridge structure provides better lateral optical confinement and carrier confinement, but the cost is the fabrication complexity. Narrow metal strips and via holes are difficult to be placed or opened on top of the narrow ridges (usually 1.4 μm ~ 10 μm wide). Furthermore, dry etchings for the via-hole opening bring plasma damages to the *p*-type III-N materials and the ohmic contact metal stack, resulting in contact resistance degradation.

3.2.1 Fabrication Process Flow

In this study, the ridge waveguide structure and vertical diode scheme are applied. The *p*-type GaN metal contact (anode) is on the top of the device, and the *n*-type GaN metal contact (cathode) is evaporated on the backside of the conductive *n*-type FS GaN substrate. The process flow chart is shown in Figure 17. The ridges are formed by an ICP etching using evaporated SiO_2 as the etching mask. An Al_2O_3 film is then deposited using an e-gun evaporator to serve as the insulating dielectric layer between the semiconductor and the *p*-GaN metal contact. After the Ni/Ag-based *p*-type ohmic contact is formed, substrates are lapped and polished to a thickness of 60 μm. A Ti/Al/Ti/Au contact metal stack is deposited on the backside surface.

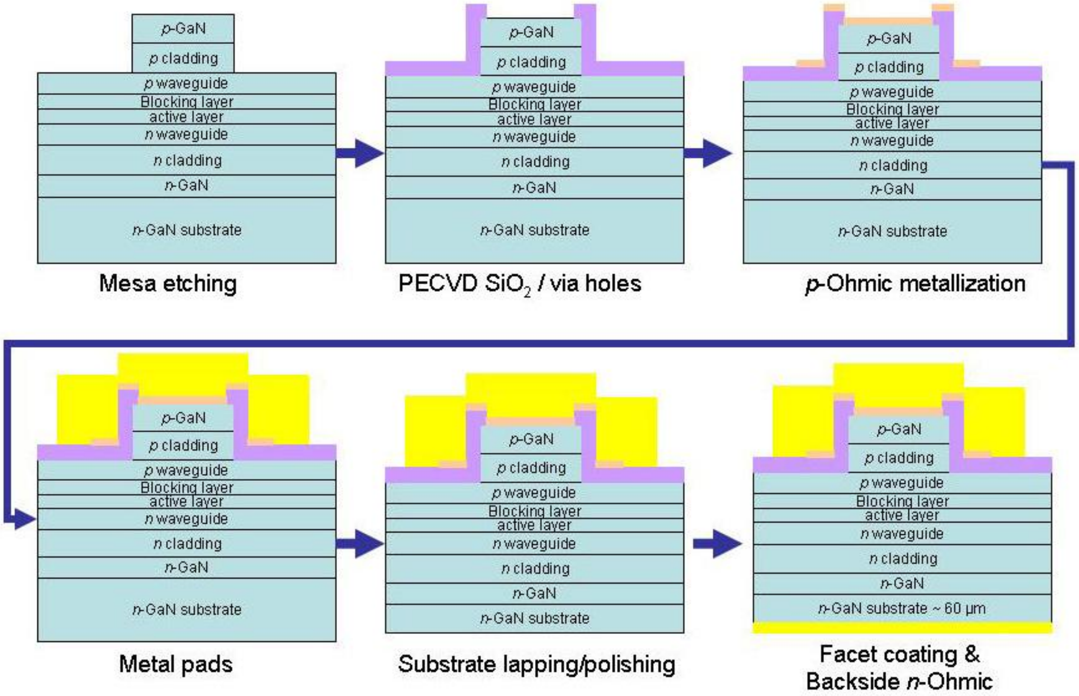

p-GaN
p cladding
p waveguide
Blocking layer
active layer
n waveguide
n cladding
n-GaN
n-GaN substrate
Mesa etching
PECVD SiO2 / via holes
p-Ohmic metallization
Metal pads
Substrate lapping/polishing
n-GaN substrate ~ 60 μm
Facet coating &
Backside n-Ohmic

Figure 17. Process flow chart of InGaN/GaN MQW vertical-current-injected edge-emitting LDs.

The end facets of the waveguide LDs are formed by cleaving along the *m*-plane of the sample followed by the deposition of distributed Bragg reflector (DBR) mirrors using alternating SiO_2 and HfO_2 (or TiO_2) layers. The reflectance of the rear DBR mirror is 99%, while that of the front DBR mirror varies for different design lasing wavelengths. The fabricated LD bars are placed *p*-side-up and attached to AlN submounts for testing. The temperature is controlled by a thermoelectric cooler and a temperature controller (ILX Lightwave Technology Inc., Model #: LDT-5948) during the device testing.

3.2.2 Optimization of Ohmic Contact to *p*-GaN

As forward-biased diodes working under the high current injection condition, LDs require low contact resistances. Based on the study in the GaN APD fabrication, the Ni/Ag/Ni/Au scheme is chosen for the process development at the beginning. However, one concern is that, at a high current injection level with a high junction temperature, the Ni barrier layer between Ag and Au may not be able to prevent the diffusion between Ag and Au. Therefore, a new metal stack, Ni/Ag/Pt, is studied for LD's *p*-type GaN ohmic contact. The DOE table for the *p*-type GaN ohmic contact study is shown in Table 10. There are two different metal stacks and five different RTA temperatures. The RTA time is fixed at 1 minute and the ambient is dry air for all the conditions. The O_2 descum treatment in a Plasma-Thermal reactive ion etching (RIE) machine is also included in this study. There are totally 20 experiment conditions in this DOE and the output is ρ_c.

Experiments are carried out on 20 LD samples grown on sapphire substrates. They have the same layer structure and epitaxial material growth condition with the LD samples on FS GaN substrates. The TLM is used for contact resistance analysis. For both

Ni/Ag/Ni/Au and Ni/Ag/Pt metal stacks, in the RTA temperature “sweet window”, ρ_c is stable and as low as 1.0×10^{-3} Ω cm^2. The advantage of the Ni/Ag/Pt scheme begins to be significant when the RTA temperature is high, where the ρ_c degradation rate is more severe on the Ni/Ag/Ni/Au metal stack. Therefore, the Ni/Ag/Pt has better thermal stability, which is important for the high-power LD operation.

Table 10. The DOE table for the optimization of ohmic contact to *p*-GaN in InGaN-based LDs.

#	Metal stack	O_2 descum	RTA Temp (C)	ρ_c (mΩ cm^2)
1	Ni/Ag/Ni/Au	Yes	400	5.10
2	Ni/Ag/Ni/Au	Yes	450	2.22
3	Ni/Ag/Ni/Au	Yes	500	3.76
4	Ni/Ag/Ni/Au	Yes	550	15.3
5	Ni/Ag/Ni/Au	Yes	600	98.9
6	Ni/Ag/Ni/Au	No	400	1.40
7	Ni/Ag/Ni/Au	No	450	1.06
8	Ni/Ag/Ni/Au	No	500	1.18
9	Ni/Ag/Ni/Au	No	550	4.08
10	Ni/Ag/Ni/Au	No	600	18.2
11	Ni/Ag/Pt	Yes	400	2.64
12	Ni/Ag/Pt	Yes	450	2.97
13	Ni/Ag/Pt	Yes	500	5.50
14	Ni/Ag/Pt	Yes	550	12.3
15	Ni/Ag/Pt	Yes	600	75.3
16	Ni/Ag/Pt	No	400	0.983
17	Ni/Ag/Pt	No	450	1.14
18	Ni/Ag/Pt	No	500	1.59
19	Ni/Ag/Pt	No	550	2.38
20	Ni/Ag/Pt	No	600	6.88

3.3 Effects of a Step-Graded $Al_xGa_{1-x}N$ Electron Blocking Layer

In addition to the quest of achieving longer-wavelength operations, reducing the J_{th} and improving the stimulated emission efficiency are also essential to achieve higher optical-output power, lower electric-power consumption, and longer life time in InGaN-based LDs. In semiconductor LD designs, an EBL is a widely-used approach to improve carrier confinement in the active region for higher η_i. Typical EBL in InGaN/GaN MQW diode lasers uses a single layer of $Al_xGa_{1-x}N$ with a constant aluminum content [48]. Other designs using AlGaN/GaN multiple-quantum-barrier EBL to achieve higher effective barrier height were also reported [181]. However, Piprek *et al.* reported that the hetero-interface between the $Al_xGa_{1-x}N$ EBL and the GaN top quantum barrier layer results in a large built-in polarization field and significant free electron accumulation. [182]. This free electron accumulation outside of the active region severely degrades η_i [179]. A similar problem was also observed on InGaN-based LEDs operating at high current densities, where LEDs without EBLs showed higher external quantum efficiency [183]. Therefore, the optimization of the EBL in III-N LD designs may be a key to further device performance improvement. To address this interface polarization charge issue, Chen *et al.* proposed a method of using an AlInGaN EBL, whose polarization can be tuned to match that of GaN [184]. However, due to the large mismatch in growth conditions (growth temperature, pressure, growth rate, etc.) between AlN/GaN and InN, it is difficult to achieve high quality quaternary AlInGaN epitaxial layers [185-188].

In this work, a three-layer step-graded $Al_xGa_{1-x}N$ EBL is studied in 420-nm InGaN/GaN MQW LDs to mitigate the built-in polarization field and the undesired electron accumulation at the $Al_xGa_{1-x}N$/GaN hetero-interface. This idea was first proposed by Prof. Paul D. Yoder at Georgia Tech [86]. With this simple structure modification, J_{th} is reduced from 4.6 kA/cm^2 to 2.5 kA/cm^2, and the corresponding slope efficiency is increased from 0.72 W/A to 1.03 W/A under the pulsed-current condition. The effects of the step-graded $Al_xGa_{1-x}N$ EBL on η_i, α_i, and temperature-dependent stimulated emission characteristics are also investigated. When compared to the single-layer abrupt $Al_{0.18}Ga_{0.82}N$ EBL design, η_i is dramatically increased from 0.60 to 0.92, while α_i keeps almost unchanged at 9 ~ 10 cm^{-1} in the step-graded $Al_xGa_{1-x}N$ EBL design. The results suggest that the improved stimulated emission performance is directly attributed to the enhancement of η_i with the insertion of the step-graded $Al_xGa_{1-x}N$ EBL. A temperature-dependent measurement of the peak stimulated emission wavelength also shows that the step-graded $Al_xGa_{1-x}N$ EBL can improve the temperature stability of λ from 0.05 nm/K to 0.034 nm/K.

3.3.1 LD Structures and Simulations

Two LD structures, Structure A for abrupt-EBL LD and Structure B for step-graded-EBL LD, were grown on *c*-plane FS GaN substrates. They have similar epitaxial layers except for the EBL design. The layer structures of Structures A and B are listed in Table 11. The epitaxial material growth starts from a 2000-nm-thick Si-doped *n*-type GaN buffer layer, followed by a Si-doped GaN/$Al_{0.16}Ga_{0.84}N$ short-period superlattice (SPSL) lower cladding layer and a 100-nm-thick Si-doped GaN lower waveguide. The active region consists of 4-pair $In_{0.1}Ga_{0.9}N$/GaN MQWs with 3.5-nm wells and 8.8-nm barriers, followed by the EBL. For *p*-type waveguide and cladding layers, both structures utilize a 100-nm-thick Mg-doped GaN layer and Mg-doped GaN/$Al_{0.17}Ga_{0.83}N$ SPSL. Atop of the *p*-cladding layer, a 30-nm-thick Mg-doped GaN cap layer and a 20-nm-thick highly Mg-doped GaN contact layer are grown for ohmic contact. Both Structures A and B have 20-nm-thick Mg-doped $Al_{0.18}Ga_{0.82}N$ EBLs. As shown in Figure 18, the major difference in the EBL design comes from the variation in the transition of the barrier layer to the $Al_{0.18}Ga_{0.82}N$ EBL. In Structure B, the step-graded EBL profile is formed by replacing the 8.8-nm-thick GaN top barrier layer, as seen in Structure A, with a 4.4-nm-thick $Al_{0.04}Ga_{0.96}N$ and another 4.4-nm-thick $Al_{0.09}Ga_{0.91}N$.

Table 11. Compositions and thicknesses of the 420-nm LD structures.

Layers	Abrupt-EBL LD		Step-graded-EBL LD	
	Matreial:doping	Thickness (nm)	Matreial:doping	Thickness (nm)
p-contact	GaN:Mg^{++}	20	GaN:Mg^{++}	20
p-injection	GaN:Mg	30	GaN:Mg	30
p-cladding super lattice 90 pairs	GaN/ $Al_{0.16}Ga_{0.84}N$:Mg	450	GaN/ $Al_{0.16}Ga_{0.84}N$:Mg	450
p-waveguide	GaN:Mg	100	GaN:Mg	100
EBL	$Al_{0.18}Ga_{0.82}N$:Mg	20	$Al_{0.18}Ga_{0.82}N$:Mg	20
	GaN barrier: undoped	8.8	$Al_{0.09}Ga_{0.91}N$:Mg	4.4
			$Al_{0.04}Ga_{0.96}N$:Mg	4.4
Active region MQWs 4 pairs	$In_{0.10}Ga_{0.90}N$/GaN: undoped	3.5/8.8	$In_{0.10}Ga_{0.90}N$/GaN: undoped	3.5/8.8
n-waveguide	GaN:Si	100	GaN:Si	100
n-cladding super lattice 150 pairs	GaN/ $Al_{0.16}Ga_{0.84}N$: Si	750	GaN/ $Al_{0.16}Ga_{0.84}N$: Si	750
Buffer	GaN:Si	2000	GaN:Si	2000
Substrate	*c*-plane GaN		*c*-plane GaN	

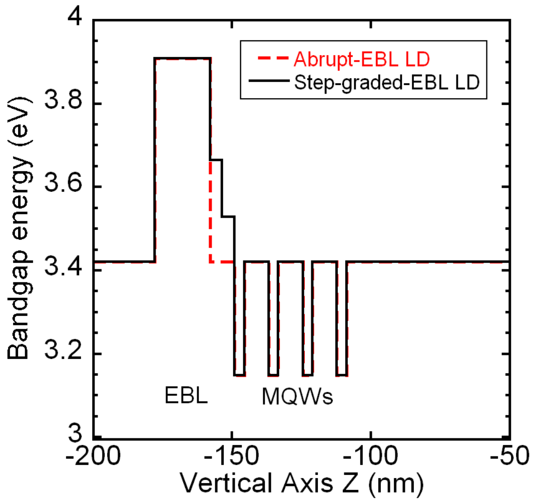


Figure 18. Designed band diagrams in the EBL and active regions for the abrupt-EBL LD and the step-graded-EBL LD.

Figure 19 shows the refractive index profiles and simulated optical field distributions of these LD structures. Both designs have nearly identical optical confinement factor (Γ) under the fundamental waveguide mode. The Γ is 0.5% for Structure A and 0.47% for Structure B.

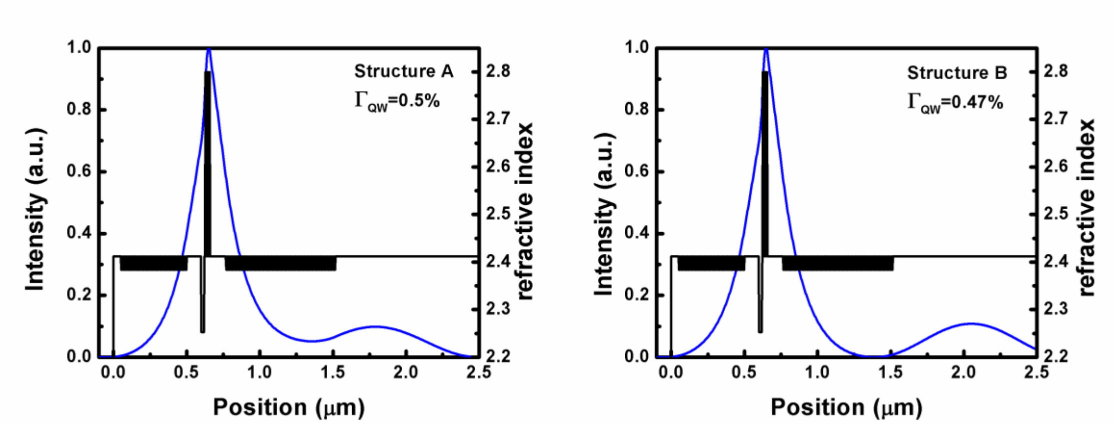
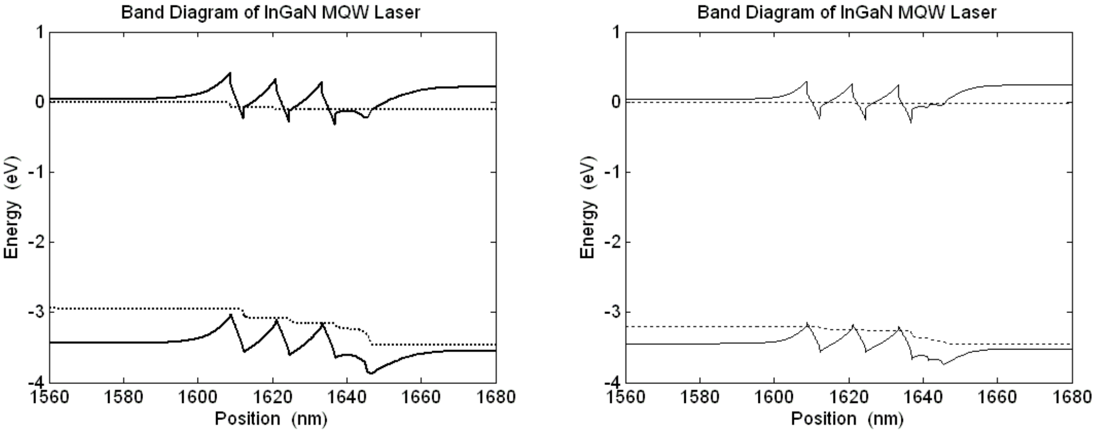


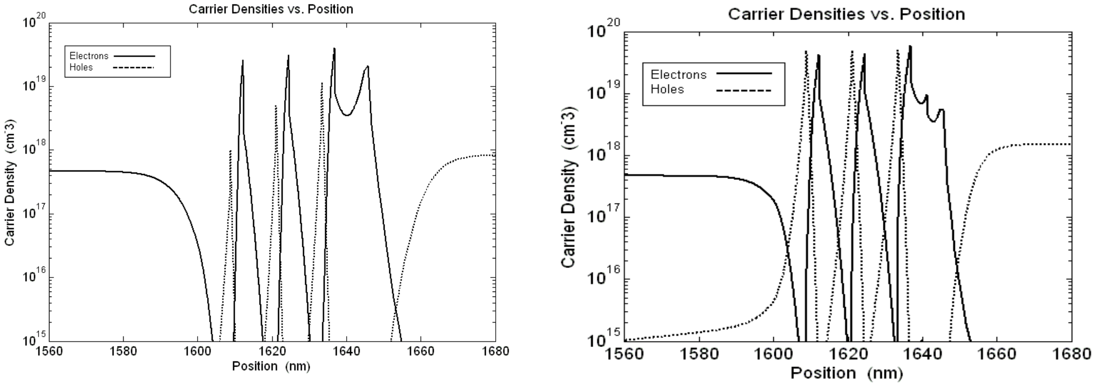
Figure 19. The refractive index profiles and the corresponding optical-field distributions of LD Structures A and B.

The band diagram and carrier distribution in the vicinity of the active region and the EBLs are simulated with spontaneous and piezoelectric polarization models included [86]. As shown in Figure 20 (a), at a forward bias of 3.6 V, the abrupt-EBL LD shows the formation of an electron potential notch at the EBL/barrier interface due to the piezoelectric field. This design is certainly not optimal because the injected electrons will be trapped at the EBL/barrier interface instead of the QW active region. On the other hand, in Figure 20 (b), the step-graded EBL design can remove the formation of the potential notch at the EBL/barrier interface at the same biasing condition. By plotting quasi-static electron and hole concentration distribution in this region, as shown in Figure 21 (a), a net polarization electron charge accumulation is observed at the $Al_{0.18}Ga_{0.82}N$/GaN barrier interface in the abrupt-EBL LD. It is expected that electrons accumulated at the EBL/barrier interface will not be effectively recombined with the injected hole for efficient optical energy emission under the forward biased condition.



(a) (b)

Figure 20. Simulated energy band diagrams for (a) the abrupt-EBL LD and (b) the step-graded-EBL LD [86].



(a) (b)

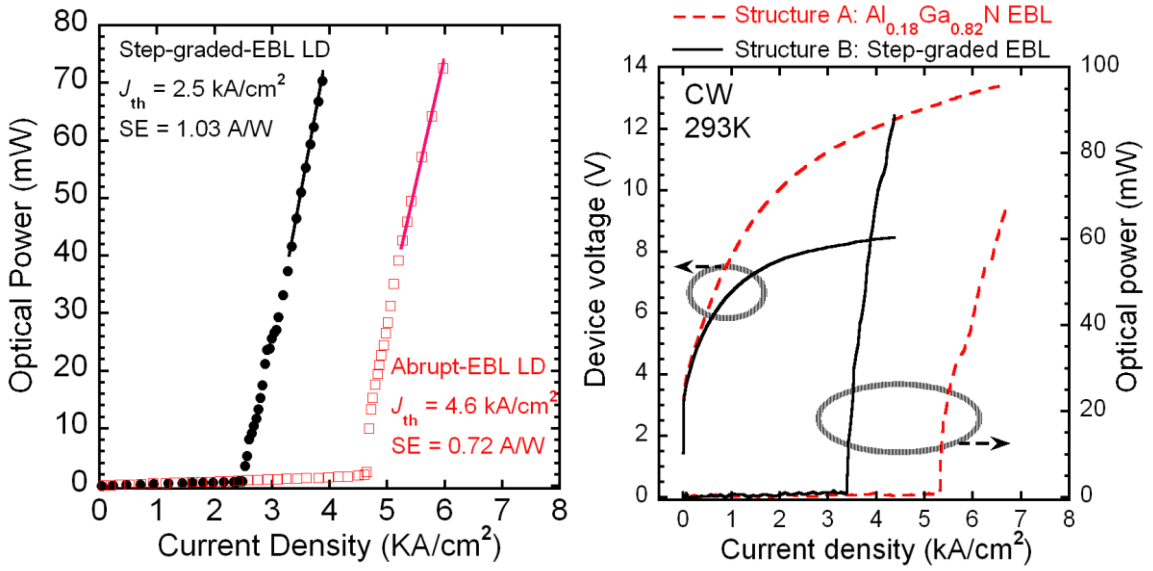
Figure 21. Simulated carrier concentration distributions for (a) the abrupt-EBL LD and (b) the step-graded-EBL LD [86].

In addition, Figure 21 (a) also demonstrates a substantially inhomogeneous population of holes among the QWs. Non-uniform hole distribution will make the transparency current density higher. On the other hand, the step-graded $Al_xGa_{1-x}N$ EBL design shown in Figure 21 (b) help "relocate" the injected electrons back to the QW active region with an enhanced uniform hole injection at the same biasing condition. As a result, the slight modification in the step-graded EBL design is supposed to offer tremendous LD performance enhancement in achieving a higher η_i, and hence higher slope efficiency and much lower J_{th}.

3.3.2 Threshold Current Density and Lasing Wavelength

The fabricated abrupt-EBL LD (wafer ID: 2-1507-3-2) and step-graded-EBL LD (wafer ID: 2-1518-3-3) are characterized by *L-I* measurement [67]. They are tested under pulsed-current operation at 293K to avoid the self-heating. The duty cycle of the pulsed current is 0.1% with a pulse width of 1 μs and a repetition rate of 1 KHz. The optical output power is measured from the front DBR mirror (R = 27%) using a calibrated silicon photodiode and a neutral density filter. For comparison, LDs with 8-μm-wide and 750-μm-long ridged waveguide designs from the abrupt-EBL LD and the step-graded-EBL LD are chosen and their pulsed-mode optical output power as a function of *L-J* curves are plotted in Figure 22 (a). J_{th} of the abrupt-EBL LD is 4.6 kA/cm^2, while that for the step-graded-EBL LD is 2.5 kA/cm^2. The slope efficiency for the step-graded-EBL LD is 1.03 W/A, and that for the abrupt-EBL LD is 0.72 W/A.

CW-mode operation is also achieved at 293K [67]. For comparison, the CW-mode optical-output-power versus current-density versus voltage (*L-J-V*) curves from the abrupt-EBL LD and the step-graded-EBL LD are plotted in Figure 22 (b). It is shown that J_{th} in the abrupt-EBL LD is 5.32 kA/cm^2, while that in the step-graded-EBL LD is 3.38 kA/cm^2. The slope efficiency for the step-graded-EBL LD is 1.35 W/A, and that for the abrupt-EBL LD is 0.82 W/A. The measured V_{th} and the series resistance also show lower values from the step-graded-EBL LD. V_{th}'s are 12.8 V and 8.2 V and the corresponding series resistances at the threshold lasing conditions are 10.8 Ω and 5.0 Ω, for the abrupt-EBL LD and step-graded-EBL LD, respectively.



(a) **(b)**

Figure 22. (a) Pulsed-current *L-J* curves and (b) CW-mode *L-J-V* curves of the fabricated abrupt-EBL LD (Device ID: 2-1507-3-2-750-5-G2-4um) and step-graded-EBL LD (Device ID: 2-1518-3-3-750-2-G1-8um) at 293K. The device dimension is 8×750 μm^2.

The CW-mode emission spectra are measured from the front DBR mirror using a SPEX® 1000M spectrometer with a scanning resolution of 0.01 nm. As shown in Figure 23, the stimulated radiation wavelengths are 423.18 nm and 420.34 nm at the optical output power (P_{opt}) of 30 mW for the abrupt-EBL LD and step-graded-EBL LD, respectively. The full width at half maximum (FWHM) is 0.03 nm in both designs. The calculated longitudinal cavity mode spacing ($\Delta\lambda = \lambda^2 / 2nL$) is 0.058 nm. The measured FWHM's ensured single longitudinal mode operation for both Structures.

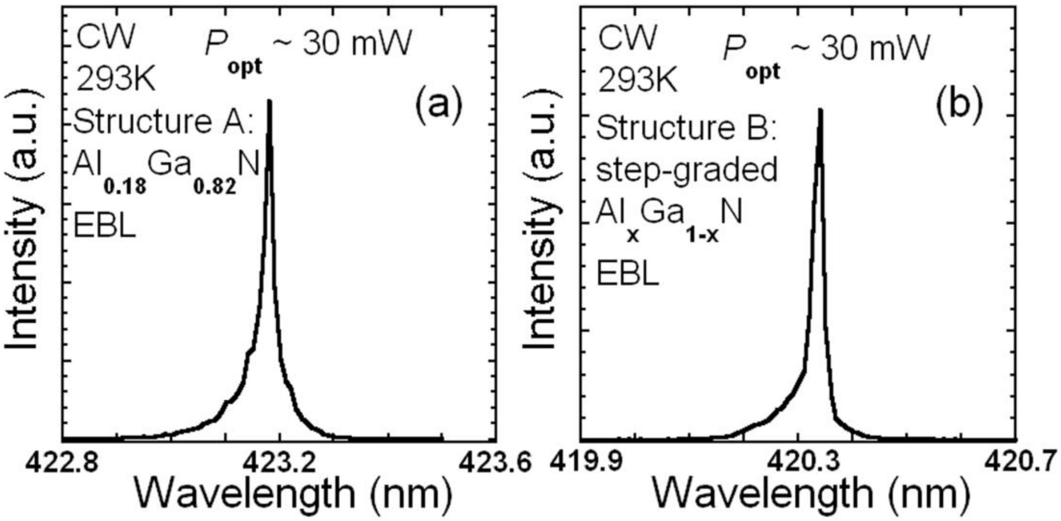


Figure 23. CW-mode lasing spectra of (a) the abrupt-EBL LD (wafer ID: 2-1507-3-2) and (b) the step-graded-EBL LD (wafer ID: 2-1518-3-3) at P_{opt} of 30 mW.

3.3.3 Internal Quantum Efficiency

The evaluation of η_i and α_i for fabricated LDs is obtained by measuring a set of cavity-length-dependent optical-output power versus current (*L-I*) curves [179,189]. In this study, devices under test have the same 8-μm cavity width but different cavity lengths (*L*) of 500 μm, 750 μm, and 1000 μm. The η_i and α_i can be determined by a linear fitting of the differential quantum efficiency (η_d) for LDs with different cavity lengths through the following equation [179]:

$$\frac{1}{\eta_d} = \frac{\alpha_i}{\eta_i \ln(1/\sqrt{R_1 R_2})} L + \frac{1}{\eta_i} \tag{3.2}$$

where R_1 and R_2 are end-facet mirror reflectance. η_d can be obtained by [179]:

$$\eta_d = \frac{1}{F} \frac{q\lambda}{hc} \frac{dP}{dI} \tag{3.3}$$

where *F* is the fraction of output power from the front mirror relative to the total output power and can be expressed as [179]:

$$F = \frac{1 - R_1}{(1 - R_1) + \sqrt{R_1 / R_2}\,(1 - R_2)} \tag{3.4}$$

As shown in Figure 24, η_i and α_i for Structure A are 0.6 and 10 cm^{-1}, respectively. In contrast, η_i of Structure B is 0.92 and α_i is 9 cm^{-1}. The significant enhancement of η_i confirms the consistency of the simulation results. Lower J_{th} and higher slope efficiency are achieved in the step-grade EBL design when compared to the abrupt EBL design. Similar values of α_i for Structures A and B are expected because they have similar layer structures and growth conditions except for the slight variation in the EBL design. The calculated α_i of 9 ~ 10 cm^{-1} is comparable to the values reported on other InGaN-based violet-blue LDs [189,190].

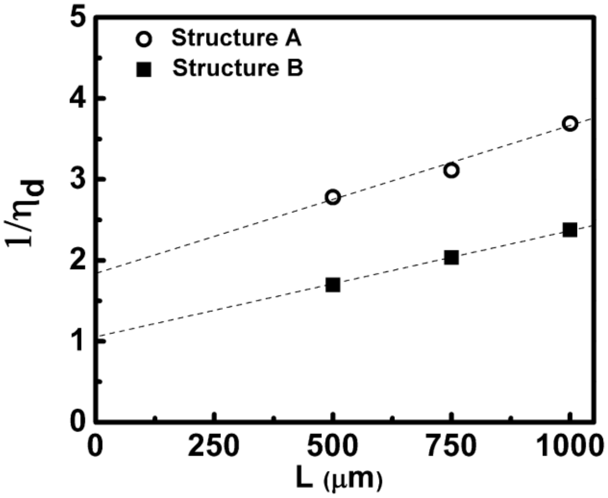


Figure 24. The reciprocal differential quantum efficiency (1/η_d) versus cavity lengths (*L*) for Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3).

3.3.4 Temperature Dependence of Lasing Wavelength

Figure 25 shows the temperature-dependent λ of Structure A and Structure B LDs at the P_{opt} of 10 mW. The dimension of the devices under test is 8×750 μm^2. The temperature of the LDs is controlled between 20 C and 58 C with a step of 2 C. Both structures show *λ* red-shift as the temperature increases, possibly due to the bandgap narrowing effect and the Joule heating. For Structure A, the *λ* red-shift shows a staircase pattern. It shifts slightly with a rate of 0.034 nm/K within a narrow temperature region (~ 10 C). At certain temperatures, a sudden increase of *λ* red-shift of 0.3 to 0.5 nm is observed. This mode-hopping phenomenon suggests that the stimulated emission switches from one longitudinal mode to another. The mode hopping persists across several higher-order longitudinal modes because the short longitudinal cavity mode spacing (0.058 nm). As a result, the overall λ red-shift rate increases to 0.05 nm/K for Structure A LDs. On the other hand, for Structure B LDs, the *λ* red-shift shows a smoother curve without any significant mode hopping and the overall rate of the red-shift is 0.034 nm/K. The results suggest that the step-graded EBL design may offer a better thermal stability in the lasing wavelength.

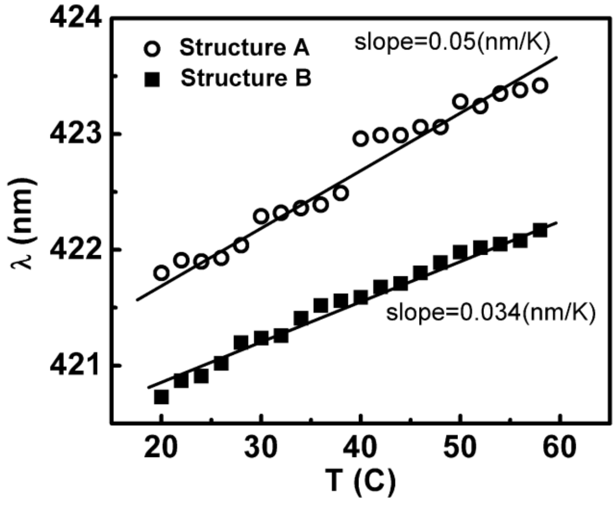


Figure 25. Temperature dependence of *λ* for the LD Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3) under pulsed-current operation from *T* = 20 C to *T* = 58 C.

Figure 26 shows the peak photon emission wavelength as a function of current for Structures A and B under pulsed-current operation. By increasing *I* from zero to I_{th}, the spontaneous emission peak wavelengths of Structures A and B LDs both show a blue-shift of 10 ~ 12 nm. The blue-shift is a result of combined band-filling effect and quantum-confined Stark effect as the injected carrier density increases. The inset of Figure 26 shows the trend of λ shifting beyond J_{th}. For Structure B LDs, λ stays approximately constant under the stimulated emission condition. On the other hand, several irregular mode hoppings (+/-~0.3 nm) are observed for Structure A as the current injection increases from 220 mA to 250 mA. The result demonstrates that the step-graded EBL design may be beneficial in suppressing the undesired mode hopping under high current injection and high optical-output power operations.

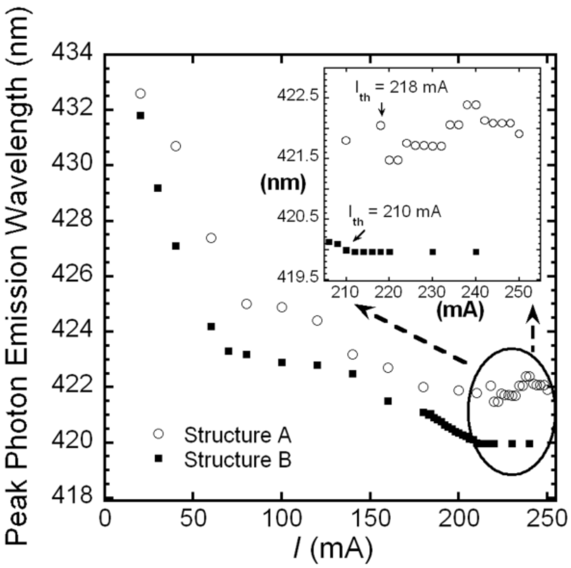


Figure 26. The peak photon emission wavelengths as a function of injection current for LD Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3) under pulsed-mode operation.

3.3.5 Characteristic Temperature

Figure 27 shows a comparison of the temperature-dependent characteristics of the I_{th} for both structures from T = 20 C to T = 58 C. Devices under test have the same dimension as mentioned in the previous sessions. The measurement is carried out in the pulsed-current mode to eliminate the self-heating effect. The extracted characteristic temperature (T_0) is estimated to be 210 K for Structure A, and 180 K for Structure B. It is noted that T_0 of 210 K on the abrupt EBL LDs is one of the highest values reported on InGaN-based violet-blue LDs. For the step-graded EBL LDs, T_0 of 180 K is also measured, which is comparable to typical values reported on other InGaN-based violet-blue LDs (140 K ~ 190 K) [57,58,189-191].

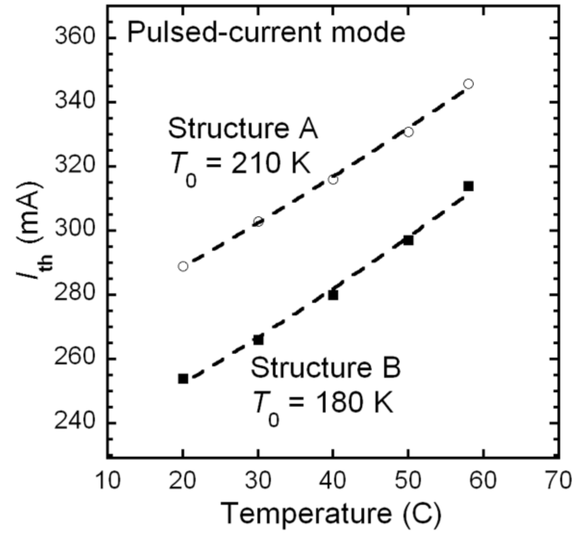


Figure 27. Temperature dependence of the threshold currents for Structures A (wafer ID: 2-1507-3-2) and B (wafer ID: 2-1518-3-3) in the pulsed-current mode from T = 20 C to T = 58 C.

3.4 CW-Mode 460-nm InGaN/GaN MQW Laser Diodes

Due to the smaller difference of refractive index between AlGaN and GaN materials as the propagation wavelength increases, optical confinement becomes weaker in longer-wavelength blue/green InGaN/GaN MQW LDs. Therefore, InGaN layers have been employed as waveguide layers in blue/green InGaN/GaN MQW LDs because of their larger refractive index compared to AlGaN and GaN. In addition to offering a better optical confinement, the InGaN waveguide layers also play roles in other aspects. Okamoto *et al*. reported that InGaN waveguide layers could reduce the strain in LD structures [83]. Lee *et al*. reported that InGaN waveguide layers could increase the η_i of the InGaN MQW active layer by reducing the indium composition fluctuation and the Mg diffusion into the active layer [192].

In this work, $In_{0.03}Ga_{0.97}N$ waveguide layers are introduced to 460-nm InGaN/GaN MQW LDs. A comparison study shows that $In_{0.03}Ga_{0.97}N$ waveguide layers significantly improve the emission efficiency of the active region in addition to offering a better optical confinement [68,88]. Consequently, 460-nm CW-mode lasing of InGaN/GaN MQW LDs at RT is achieved. When working in the CW-mode operation, the J_{th} is 5.67 kA/cm^2 and the V_{th} is 9.05 V. When operation under the pulsed-current mode, the J_{th} is 3.3 kA/cm^2 and the corresponding V_{th} is 5.9 V.

3.4.1 LD Structures

The epitaxial materials of the InGaN/GaN MQW 460-nm LDs were grown on *c*-plane FS GaN substrates. The detailed LD layer structure design is shown in Table 12 [88]. Different from the 420-nm LD structures in the previous section, the 460-nm LD structure employs composite waveguide layers consisting of $In_{0.03}Ga_{0.97}N$ and GaN.

3.4.2 Results and Discussions

The fabricated LDs with $In_{0.03}Ga_{0.97}N$ waveguides (wafer ID: 2-1508-4-3) are characterized by *L-I-V* measurement. They are tested under pulsed-current operation at 293K to avoid the self-heating. The duty cycle of the pulsed current is 0.1% with a pulse width of 1 μs and a repetition rate of 1 KHz. The optical output power is measured from the front DBR mirror (R = 93%) using a calibrated silicon photodiode and a neutral density filter. The *L-J-V* curves of one device with 12-μm-wide and 1020-μm-long ridged waveguide are plotted in Figure 28. The J_{th} is 3.3 kA/cm^2 and the threshold voltage is 5.9 V. The slope efficiency is 0.182 W/A.

Table 12. Compositions and thicknesses of the 460-nm LD structure.

Layer	Material	Thickness (nm)
p-contact	GaN:Mg^{++}	20
p-injection	GaN:Mg	30
p-cladding super lattice 90 pairs	GaN/ $Al_{0.16}Ga_{0.84}N$:Mg	450
p-waveguide	GaN:Mg	100
EBL	$Al_{0.18}Ga_{0.82}N$:Mg	20
p-waveguide	$In_{0.03}Ga_{0.97}N$: undoped	80
Spacer	GaN: undoped	8.8
Active region MQWs 2 pairs	$In_{0.18}Ga_{0.82}N$/GaN: undoped	2.8/8.8
n-waveguide	$In_{0.03}Ga_{0.97}N$: undoped	80
n-waveguide	GaN:Si	100
n-cladding super lattice 150 pairs	GaN/$Al_{0.16}Ga_{0.84}N$: Si	750
Buffer	GaN:Si	3000
Substrate	*c*-plane FS GaN	

After being bonded to AlN submounts, the CW-mode operation is achieved at 293 K, as shown in Figure 29. The ridge size of the LD device is 750 μm by 8 μm. The CW-mode *L-J-V* curves are plotted in Figure 29 (a). It is shown that J_{th} is 5.67 kA/cm^2 and V_{th} is 9.05 V. The slope efficiency is 0.216 W/A. The CW-mode emission spectra are measured from the front DBR mirror using the SPEX spectrometer with a scanning resolution of 0.01 nm. As shown in Figure 29 (b), the stimulated radiation wavelength is 460.2 nm and the FWHM is 0.02 nm. Since the calculated longitudinal cavity mode spacing is 0.058 nm, the measured FWHM ensures the single longitudinal mode operation. Shown in the inset of Figure 29 (b) is the lasing far-field pattern of this device operating in the CW mode, beam projecting on a piece of white paper. The distance between the LD facet and the paper is ~ 5 cm.

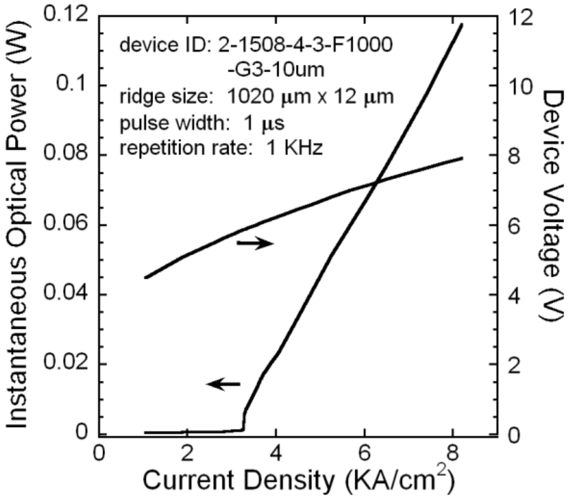
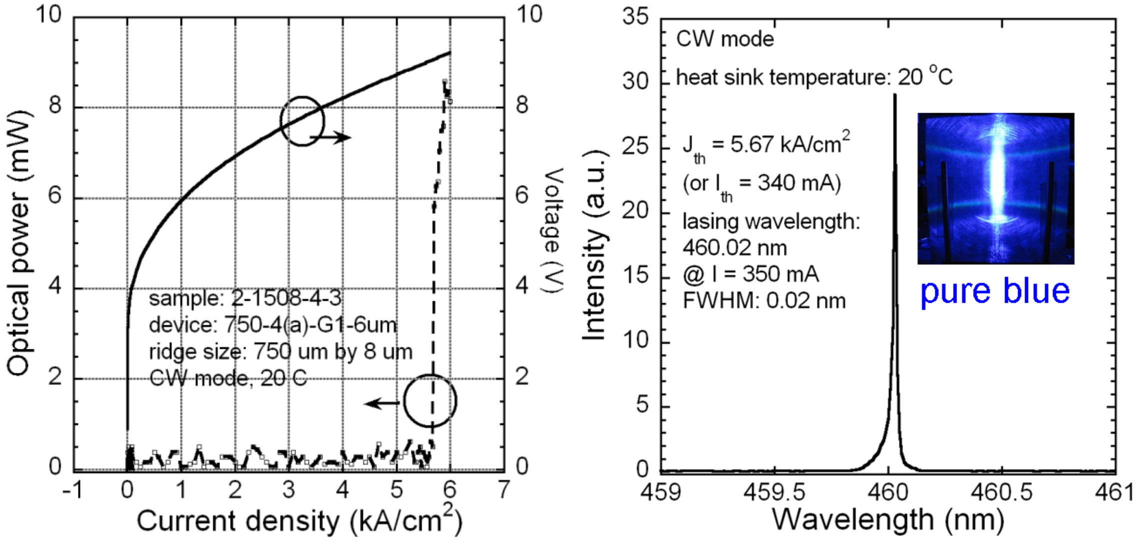


Figure 28. ***L-J-V*** **curves of a 460-nm LD with $In_{0.03}Ga_{0.97}N$ waveguide layers under the pulsed-current operation. Device ID: 2-1508-4-3-F1000-G3-10um.**



(a) **(b)**

Figure 29. (a) Lasing spectra and (b) ***L-J-V*** **curves of a 460-nm LD with $In_{0.03}Ga_{0.97}N$ waveguide layers under the CW-mode operation. Device ID: 2-1508-4-3-750-4a-G1-6um. Inset: the lasing far-field pattern of this device.**

Figure 30 shows the temperature dependence of λ and I_{th} from T = 20 C to T = 58 C. The test is carried out in the pulsed-current mode to eliminate the self-heating. The ridge size of the LD device is 750 μm by 8 μm. The λ red-shift rate is 0.052 nm/K, and the extracted T_0 is 140K.

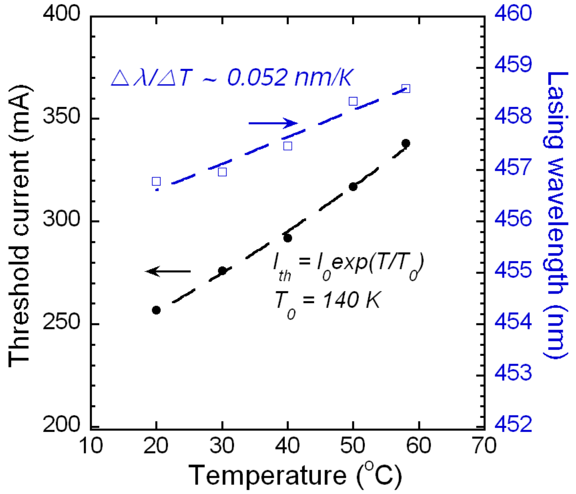


Figure 30. Temperature dependence of λ and I_{th} from T = 20 C to T = 58 C. Wafer ID: 2-1508-4-3.

3.5 Summary

The fabrication and characterization technologies for InGaN/GaN MQW current-injected edge-emitting LDs have been successfully developed at Georgia Tech. CW-mode operations of 420-nm and 460-nm InGaN-based LDs have been demonstrated at RT. Their characteristics are summarized in Table 13.

To achieve enhanced η_i and longer-wavelength lasing, EBL and waveguide have been carefully designed. The experimental results show that the step-graded $Al_xGa_{1-x}N$ EBL is better than the conventional abrupt $Al_xGa_{1-x}N$ EBL to enhance the LD performance. In addidtion, compared to GaN waveguide layers, the $In_{0.03}Ga_{0.97}N$ waveguide layers are desired in longer-wavelength blue/green InGaN-based LDs for better optical confinement.

Table 13. The characteristics of the RT CW-mode InGaN-based LDs at GT.

Parameter	460-nm CW LD	420-nm CW LD
Cavity length (mm)	0.750	0.650
Ridge width (μm)	8.0	8.0
I_{th} (A)	0.340	0.176
J_{th} (kA/cm^2)	5.67	3.38
V_{th} (V)	9.05	8.2
T_0 (K)	140	180 ~ 210
CW-operation lifetime (hour)	~ 1	~ 1
Max. optical power (mW)	8.59	88.7
Wall Plug Efficiency (%)	0.26 @ 8.59 mW	4.60 @ 88.7 mW
Slope efficiency (W/A)	0.216	1.35
Series resistance (Ω) (at I_{th})	7.8	5.0

CHAPTER 4

DEVELOPMENT OF GAN/INGAN DOUBLE-HETEROJUNCTION BIPOLAR TRANSISTORS

The objective of this research is to develop high-power RF GaN/InGaN *npn* HBTs. Epitaxial materials were grown in the AMDG group supervised by Prof. Russell D. Dupuis at Georgia Tech. The materials were grown on *c*-plane sapphire substrates and FS GaN substrates by MOCVD without base or emitter re-growth schemes.

This chapter mainly describes the GaN/InGaN *npn* HBT fabrication and d.c./RF characterization. The results have been reported in [115-122,125]. On sapphire substrates, the common-emitter *I-V* characteristics of a 3×3 μm^2 HBT show a J_C > 20 kA/cm^2 with a V_{offset} of 0.22 V and a V_{knee} of 2.1 V. The maximal h_{fe} of 38 is measured from the Gummel plot. The BV_{CBO} and BV_{CEO} are 126 V and 118 V, respectively. The f_T is 5.3 GHz and the $f_{\max}$ is 1.3 GHz at J_C = 4.7 kA/cm^2. To the best of our knowledge, this is the first RF performance demonstration on III-N HBTs with f_T > 5 GHz.

On FS GaN substrates, a large J_C of > 141 kA/cm^2 and a large d.c. power handling capability > 3 MW/cm^2 are achieved on a 3×3 μm^2 HBT. The measured BV_{CBO} and BV_{CEO} are 165 V and 152 V, respectively. These results represent the highest d.c. power handling capability ever reported in any III-N HBTs, demonstrating their great potential in power-transistor applications.

4.1 Basic Device Physics

A bipolar transistor is a three terminal device consisting of two back-to-back *pn* junctions. Different from a bipolar junction transistor (BJT) with homojunctions, the HBT has a wider-bandgap emitter than the base. If the collector also has a wider bandgap than the base, this HBT is named as a double-HBT (DHBT). In an *npn*-type BJT or HBT operating in the forward-active mode, the base-emitter (BE) junction is forward-biased, so the desired electron current from the emitter (I_{En}) is injected to the base and the back-injection of holes from the base (I_{Bp}) flows to the emitter. The total emitter current (I_{E}) is:

$$I_E = I_{En} + I_{Bp} \tag{4.1}$$

The *emitter injection efficiency* (γ) is defined as the ratio of the desired forward current component I_{En} to the overall I_{E}:

$$\gamma \equiv \frac{I_{En}}{I_E} \tag{4.2}$$

During I_{En} diffuses through the base to form the electron current in the collector (I_{Cn}), a fraction of the electrons are recombined in the base region, so I_{Cn} is always smaller than I_{En}. This recombination process needs the same amount of holes from the base to be recombined with the lost electrons. Define I_{Br} as the overall recombination hole currents, therefore:

$$I_{Br} = I_{En} - I_{Cn} \tag{4.3}$$

As shown in Figure 31, I_{Br} can be divided into four recombination components depending on different recombination locations [178]:

$$I_{Br} = I_{B,surf} + I_{B,bulk} + I_{B,cont} + I_{B,scr} \tag{4.4}$$

$I_{\mathrm{B,surf}}$ is the surface recombination current in the exposed extrinsic base region, $I_{\mathrm{B,bulk}}$ is the bulk recombination current in the neutral base region, $I_{\mathrm{B,cont}}$ is the interface recombination current at the base contact, and $I_{\mathrm{B,scr}}$ is the recombination current in the BE space-charge region.

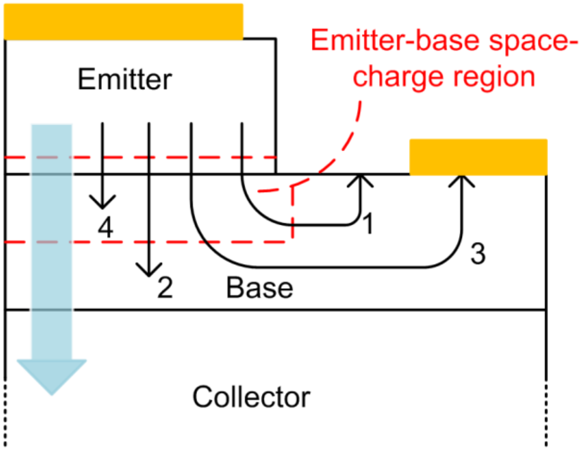


Figure 31. Schematic diagram showing the locations of the four main base recombination currents in bipolar transistors: (1) surface recombination current in the exposed extrinsic base, (2) bulk recombination current in the neutral base region, (3) interface recombination current at the base contact, and (4) space-charge recombination current in the BE space-charge region.

The *base transport factor* (α_{T}) characterizes the amount of electrons that survive after diffusion through the base region. It is defined as the ratio of I_{Cn} to I_{En}:

$$\alpha_T \equiv \frac{I_{Cn}}{I_{En}} \tag{4.5}$$

For a bipolar transistor in the forward-active mode, the base-collector (BC) junction is reverse-biased, so the electrons in I_{Cn} experience an electric field pointing to the base and are rapidly swept to the sub-collector. If the magnitude of this electric field exceeds a certain threshold, the crystal lattice impact ionization will become significant and the carriers will dramatically increase by the avalanche process, which has been introduced in Section 2.1 for APDs. The *avalanche multiplication coefficient* (*M*) is used to characterize the amount of carrier multiplication:

$$M \equiv \frac{I_C}{I_{Cn}} \tag{4.6}$$

where I_C is the total collector current consisting of I_{Cn} and the holes current I_{Cp}:

$$I_C = I_{Cn} + I_{Cp} \tag{4.7}$$

The *common-base current gain* (*α*), which is also known as the current gain transfer ratio, is defined as:

$$\alpha \equiv \frac{I_C}{I_E} \tag{4.8}$$

α should be the product of γ, α_T, and *M*:

$$\alpha = \gamma\alpha_T M = \frac{I_{En}}{I_E}\frac{I_{Cn}}{I_{En}}\frac{I_C}{I_{Cn}} = \frac{I_C}{I_E} \tag{4.9}$$

On the other hand, the *common-emitter current gain β*, which is the most important figure of merit in bipolar transistors, is defined as:

$$\beta \equiv \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C} \tag{4.10}$$

According to Eq. 4.9, *β* can be further expressed as:

$$\beta = \frac{1}{\frac{I_E}{I_C} - 1} = \frac{1}{\frac{1}{\alpha} - 1} = \frac{\alpha}{1-\alpha} = \frac{\gamma\alpha_T M}{1-\gamma\alpha_T M} \tag{4.11}$$

In a normal common-emitter operation of the GaN/InGaN *npn* HBTs, because of the material WBG and the relatively low BC junction reverse bias, the avalanche process is practically neglectable. By setting *M* to unity ($I_{Cp} \ll I_C$), the expression of *β* can be simplified as:

$$\beta = \frac{\gamma\alpha_T}{1-\gamma\alpha_T} \tag{4.12}$$

Apparently, to achieve a high β, γ and α_T must be as close to unity as possible, which is the basic rule of design a high-performance HBT.

As indicated in Equation 4.2, the key to increase γ close to 1 is the reduction of I_{Bp}. Without showing detailed derivation, the relationship between I_{Bp} and I_{En} at the BE junction is given as [178]:

$$\frac{I_{En}}{I_{Bp}} = \frac{D_{nB}X_E N_E}{D_{pE}X_B N_B}\exp(\frac{\Delta E_g}{kT}) \tag{4.13}$$

D_{nB} is the minority electron diffusion coefficient in the base, X_E is the emitter thickness, N_E is the emitter doping level, D_{pE} is the minority hole diffusion coefficient in the emitter, X_B is the base thickness, and N_B is the base doping level. ΔE_g (= $E_{g,\text{emitter}}$ - $E_{g,\text{base}}$) is the bandgap-energy difference between the emitter and base for an HBT with a graded BE junction. If the HBT has an abrupt BE junction, the conduction band energy difference (ΔE_c) will replace the ΔE_g in Equation 4.13. For a BJT with a BE homojunction, $\Delta E_g = 0$, so the exponential term is unity.

In BJTs, both I_{En} and I_{Bp} experience the same amount of energy barrier. N_E has to be much higher than N_B to keep γ close to 1. In contrast, the major advantage of an HBT is that the ΔE_g makes the back-injected holes experience a higher energy barrier, thereby preventing I_{Bp} and increasing γ. Even a small ΔE_g is able to significantly suppress the I_{Bp} due to the exponential control of the potential to the diode current. As a result, the designs of N_B and X_B are no longer limited by N_E and X_E. This is the reason why HBTs are preferred for high-frequency applications than BJTs. With the same γ as a BJT, an HBT allows a lower N_E and a higher N_B. A high N_B reduces the base resistance and enhances the power gain. A low N_E reduces the BE junction capacitance and decreases the emitter charging time.

Combining Equations 4.3, 4.4 and 4.5, the expression of α_T can be expanded as a function of each base recombination current component:

$$\alpha_T = 1 - \frac{I_{B,bulk}}{I_{En}} - \frac{I_{B,scr}}{I_{En}} - \frac{I_{B,surf}}{I_{En}} - \frac{I_{B,cont}}{I_{En}} \tag{4.14}$$

Therefore, all the base recombination current components need to be suppressed for maximum α_T. For the $I_{B,bulk}$ in the neutral base region, without detailed derivation [178]:

$$\frac{I_{B,bulk}}{I_{En}} = \frac{X_B^2}{2D_{nB}\tau_{nB}} \tag{4.15}$$

Equation 4.15 shows the reason why in an *npn* bipolar transistor, the base region thickness is designed to be much narrower than electron's diffusion length ($L_{nB} \equiv D_{nB}\tau_{nB}$) in the neutral base region. But the base region thickness cannot be too thin otherwise the base sheet resistance will be high. A typical value of the base thickness is between 50 nm to 100 nm. L_{nB} is a sensitive parameter to the material quality. If the material has a low defect density, the L_{nB} will be large and the $I_{B,bulk}$ will be very small compared to I_{En}.

The BE junction space-charge recombination current $I_{B,scr}$ can be written as [178]:

$$I_{B,scr} = I_0 \exp(\frac{qV_{BE}}{2kT}) \tag{4.16}$$

I_0 is a complex factor and depends on different materials and designs. Since I_{En} is proportional to $\exp(\frac{qV_{BE}}{kT})$, an approximated simplified expression of $I_{B,scr}$ / I_{En} is:

$$\frac{I_{B,scr}}{I_{En}} \propto \exp(-\frac{qV_{BE}}{2kT}) \tag{4.17}$$

Therefore, the influence of $I_{B,scr}$ to α_T is a function of BE junction forward bias V_{BE}. With increased V_{BE}, $\frac{I_{B,scr}}{I_{En}}$ decrease, thereby increasing α_T and β.

The $I_{B,surf}$ and $I_{B,cont}$ are proportional to $\exp(\frac{qV_{BE}}{\eta kT})$, but their ideality factors may have different values between 1 and 2 based on different materials, layer structures, and fabrication process technologies [178].

For the high-frequency performance, a good HBT should have a high cut-off frequency f_T and a high maximum oscillation frequency f_{max}. f_T is determined by the emitter-collector transit time (τ_{ec}):

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{4.18}$$

τ_{ec} is the time that an electron needs to move from the emitter contact to the collector contact, and it can be further expressed as [178]:

$$\tau_{ec} = \tau_e + \tau_b + \tau_{sc} + \tau_c \tag{4.19}$$

The first term τ_e is the emitter charging time [178]:

$$\tau_e = \frac{\eta kT}{qI_C}(C_{je} + C_{jc}) \tag{4.20}$$

Where η is the base current ideality factors, C_{je} and C_{jc} denote the junction capacitance of the BE and BC junctions, respectively. For a short τ_e, C_{je} and C_{jc} need to be reduced, usually by lowering the emitter doping level N_E and the collector doping level N_C for wider junction depletion regions. In the device layout design, smaller BE and BC diode areas are preferred for RF HBTs. In addition, τ_e inversely depends on the collector current I_C. So an RF HBT needs to be operated at high I_C levels.

The second term τ_b is the base transit time [178]:

$$\tau_b = \frac{X_B^2}{2D_{nB}} f(\kappa) \tag{4.21}$$

So the thin base thickness is not only for a high β but also for a short τ_b. κ is defined as the base electric field factor (unit-less) shown in Equation 4.22, and $f(\kappa)$ is directly given by Equation 4.23:

$$\kappa = \frac{q\varepsilon_B}{kT} X_B \tag{4.22}$$

$$f(\kappa) = \frac{2}{\kappa}(1 - \frac{1}{\kappa} + \frac{1}{\kappa} e^{-\kappa}) \tag{4.23}$$

If the base quasi-electric field (ε_B) is 0, which is the case that the base energy bandgap is constant, then κ = 0 and $f(\kappa) \rightarrow 1$. Otherwise, if the ε_B exists and points to the emitter, then κ > 0 and $f(\kappa)$ will be less than 1, therefore a smaller τ_b will be achieved.

The third term τ_{sc} is the BC junction space-charge transit time, which is the time required for an electron to drift through the BC depletion region [178]:

$$\tau_{sc} = \frac{X_{dep}}{2v_{sat}} \tag{4.24}$$

where X_{dep} is the BC junction depletion region thickness and v_{sat} is the electron saturation velocity. Since the low-doped collector is fully depleted, the collector thickness should not be too thick for a short τ_{sc}. On the other hand, the BC junction is usually revised-biased at a voltage that the v_{sat} is achieved. Furthermore, there are some BC junction layer structure designs so that the electron may travel at a velocity much higher than v_{sat}, which is the so-called velocity overshoot [178].

The last term τ_c is the collector charging time [178]:

$$\tau_c = (r_E + r_C)C_{jc} \tag{4.25}$$

Clearly, low emitter resistance r_E and collector resistance r_C are also important design concerns for a high f_T. For example, a high-doped sub-collector underneath the collector is a standard design to reduce the r_C while still keeping C_{jc} low. A high-doped emitter cap on top of the low-doped emitter is also applied to reduce the emitter contact resistance.

The maximum oscillation frequency f_{max} has the expression as:

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r_B C_{jc}}} \tag{4.26}$$

Therefore, in addition to a high f_T, a low base resistance r_B is also critical for a high f_{max}. This is the reason why a very high base doping N_B is usually applied in HBTs and the base thickness cannot be too thin.

Shown in Table 14 is the epitaxial layer structure of a high-performance InGaP/GaAs HBT reported in 1995 [193]. Nowadays the InGaP/GaAs HBT has been important commercial technology for many wireless communication applications. This HBT has $\beta > 48$, $f_T = 66$ GHz and $f_{max} = 109$, which is a convenient example to explain how these important design rules discussed above work in a real HBT: (1) The lattice-matched GaAs substrate, GaAs epi-layers, and $In_{0.49}Ga_{0.51}P$ emitter are for low defect density. (2) The large ΔE_c (0.3 eV) at the InGaP/GaAs BE junction provides a large γ even if the base doping is 100 times of the emitter doping. (3) The high base doping reduces the base resistance and is critical for the high f_{max}. (4) The moderate base thickness balances the requirement on the low base sheet resistance, low $I_{B,bulk}$, and short base transient time. (5) The low emitter doping reduces the BE junction capacitance and is good for high f_T and f_{max}. (6) The emitter cap and emitter contact layer use highly doped narrower bandgap materials for low emitter resistance, which decreases the τ_c. (7) High-doped sub-collector is also used to reduce the τ_c. (8) The collector doping is low and the collector thickness is moderate for both high-power and high-frequency operation.

The layer structure design of the GaN/InGaN *npn* DHBT in this study basically follow these design considerations. However, the epitaxy technology of the III-N materials is still not mature. As a result, the layer structure needs some modification and is different from the theoretically optimized design due to some epitaxy limitation, which will be discussed in the next section.

Table 14. The epitaxial layer structure of a published *npn* InGaP/GaAs HBT [193].

Layers	Material	Thickness (nm)	Free carrier concentration (cm^{-3})
Contact	$In_{0.50}Ga_{0.50}As$	30	$n = 1\times10^{18}$
Emitter grading	GaAs ~ $In_{0.50}Ga_{0.50}As$	30	$n = 1\times10^{18}$
Emitter cap	GaAs	130	$n = 6\times10^{18}$
Emitter	$In_{0.49}Ga_{0.51}P$	70	$n = 5\times10^{17}$
Base	GaAs	70	$p = 5\times10^{19}$
Collector	GaAs	500	$n = 3\times10^{16}$
Sub-collector	GaAs	500	$n = 6\times10^{18}$
Substrate	GaAs	-	Semi-insulating

4.2 Epitaxial Layer Structures

The GaN/InGaN *npn* DHBT layer structure is grown on 2-inch *c*-plane sapphire substrates or FS GaN substrates in a Thomas-Swan MOCVD system [125]. Detailed epitaxial material growth development and optimization have been reported earlier [111,194]. The layer structure is shown in Table 15. The free-electron and free-hole concentrations are calibrated in test samples prior to actual epitaxial material growth.

On sapphire substrates, the growth starts with a 2500-nm UID GaN buffer layer. On FS GaN substrates, because of the homo-epitaxial growth, a thinner 500-nm UID

GaN layer is enough as the buffer. The buffer layer is followed by a 1000-nm highly Si-doped n^+-GaN sub-collector and a 500-nm lightly Si-doped n-GaN collector. The free-electron concentration is 3×10^{18} cm^{-3} in the sub-collector and 1×10^{17} cm^{-3} in the collector. The base is a 100-nm Mg-doped p-$In_{0.03}Ga_{0.97}N$ layer with a free-hole concentration of 1×10^{18} cm^{-3}. Between the base and collector, a 30-nm n-$In_xGa_{1-x}N$ (x = 0 ~ 0.03) collector grading layer is included with a free-electron concentration of 1×10^{18} cm^{-3}. Between the base and emitter, a 30-nm n-$In_xGa_{1-x}N$ (x = 0.03 ~ 0) emitter grading layer is also included. Finally, a 70-nm highly-doped n^+-GaN emitter layer is grown to complete the DHBT growth. Both the emitter and emitter grading layers have high free-electron concentrations of 1×10^{19} cm^{-3}.

Table 15. The epitaxial layer structure of *npn* GaN/InGaN DHBTs in this study.

Layers	Material	Thickness (nm)	Free carrier concentration (cm^{-3})
Emitter	GaN	70	$n = 1\times10^{19}$
Emitter grading	GaN ~ $In_{0.03}Ga_{0.97}N$	30	$n = 1\times10^{19}$
Base	$In_{0.03}Ga_{0.97}N$	100	$p = 1\times10^{18}$
Collector grading	$In_{0.03}Ga_{0.97}N$ ~ GaN	30	$n = 1\times10^{18}$
Collector	GaN	500	$n = 1\times10^{17}$
Sub-collector	GaN	1000	$n = 3\times10^{18}$
Buffer	GaN	2500 (on sapphire substrates) 500 (on FS GaN substrates)	$n \approx 10^{16}$
Substrate	*c*-plane sapphire or FS GaN	-	-

Compared to the InGaP/GaAs HBT structure in Table 14, the GaN/InGaN DHBT structure in this work has several differences. A wider-bandgap collector is used to form the double-HBT structure for higher breakdown voltage, enhanced power handing capability, and lower offset voltage. To mitigate the conduction band discontinuity at the

BC hetero-junction and the consequent electron blocking effect, the collector grading layer is applied, which is highly-doped to reduce the Mg back-diffusion issue from the base. On the other hand, the emitter grading layer is to accommodate the strain at the BE hetero-interface for reduced “V-defect” density. Except for the high γ and low r_E, the major purpose of the heavily-doped emitter grading and emitter layers is to reduce the Mg-related memory effect.

4.3 Device Layout Design

4.3.1 Device Layout Design for RF and Power HBTs

The HBT device layout is drawn using Agilent ADS. HBT designs are mainly in two categories, the first one is for RF power amplifier applications with RF pads and relatively small emitter areas, and the second one is for power switching applications with multi-finger large-area emitters. Shown in Figure 32 is the device layout of an RF power HBT with $A_E = 3\times10\ \mu m^2$. There are many different device designs for the device scaling effect study. The design variation for part of devices is listed in Table 16. The emitter width is 3 μm or 4 μm, and the emitter length has different values from 3 um to 20 um. A larger emitter size reduces the BE junction resistance and increases the output power, but also increases the BE junction capacitance, so there is a trade-off in the emitter design. On the other hand, it is undoubted that the smaller BC mesa the better, which requires narrow base metal and tight space of the base metal to mesas. Due to the optical contact aligner in this study, the smallest feature is 1.2 μm for the width of the base metal finger, and the minimum alignment tolerance is 0.5 μm. It is the case for the device design in Figure 32. A base metal width of 1.5 μm and a base metal to mesas distance of 0.8 μm are also included in Table 16 for a higher process yield. Among different device designs, two design parameters are fixed: the distance from emitter metal to BE mesa edge is fixed at 0.5 μm, and the distance from collector metal to BC mesa edge is 1 μm

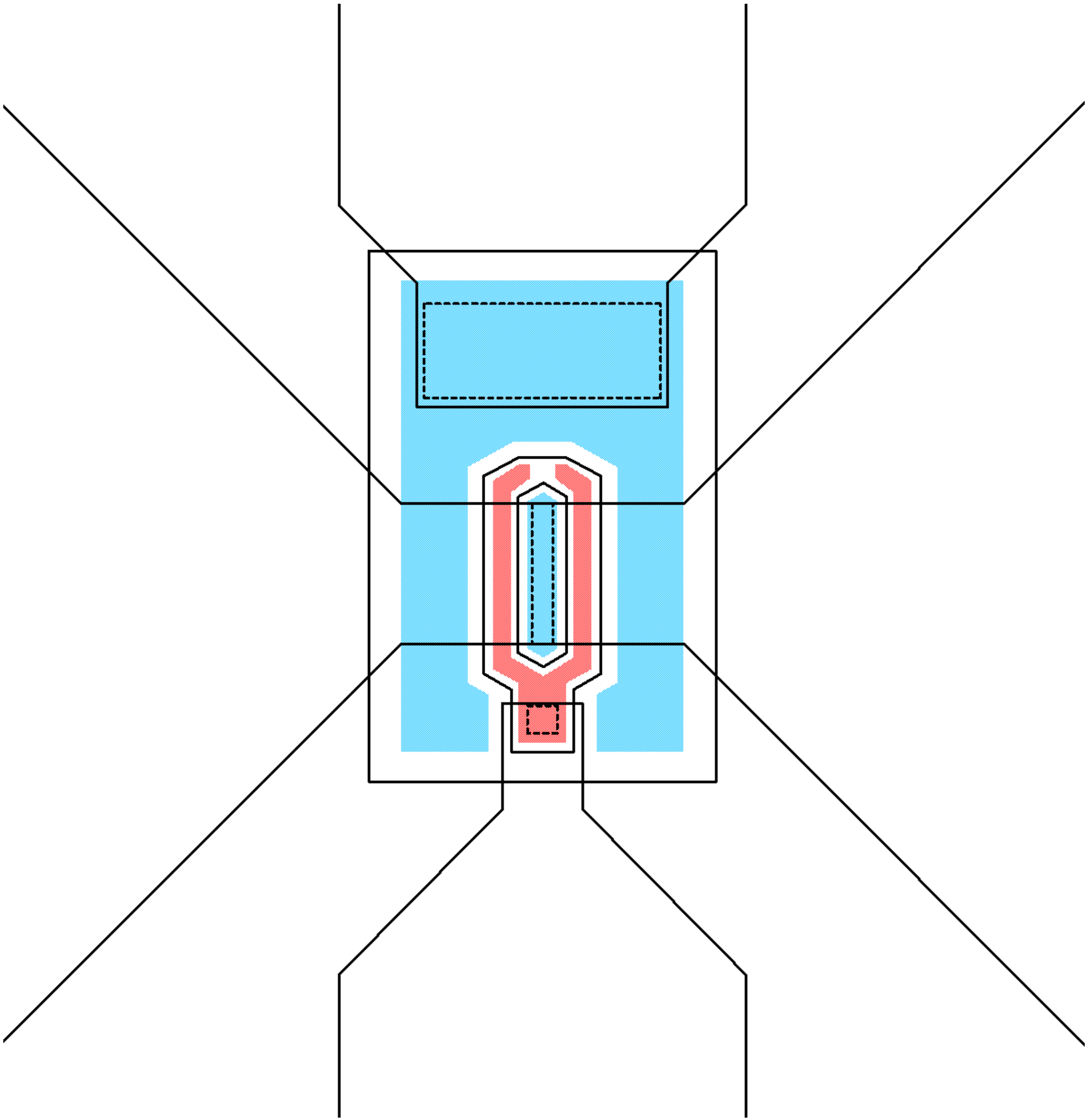


Figure 32. The layout of an HBT with $A_E = 3\times10\ \mu m^2$. The device has three mesas: BE junction mesa, BC junction mesa, and device isolation mesa. The RF pad is partially shown here.

Table 16. RF power HBT design variation.

Emitter Width (μm)	Emitter length (μm)	Base metal width (μm)	Base metal to BE mesa (μm)	Base metal to BC mesa (μm)
3	3	1.5	0.5	0.5
3	3	1.5	0.5	0.8
3	3	1.5	0.8	0.5
3	3	1.5	0.8	0.8
3	3	1.2	0.5	0.5
3	3	1.2	0.5	0.8
3	3	1.2	0.8	0.5
3	3	1.2	0.8	0.8
3	5	1.5	0.5	0.5
3	5	1.5	0.5	0.8
3	5	1.5	0.8	0.5
3	5	1.5	0.8	0.8
3	5	1.2	0.5	0.5
3	5	1.2	0.5	0.8
3	5	1.2	0.8	0.5
3	5	1.2	0.8	0.8
3	10	1.5	0.5	0.5
3	10	1.5	0.5	0.8
3	10	1.5	0.8	0.5
3	10	1.5	0.8	0.8
3	10	1.2	0.5	0.5
3	10	1.2	0.5	0.8
3	10	1.2	0.8	0.5
3	10	1.2	0.8	0.8
3	20	1.5	0.5	0.5
3	20	1.5	0.5	0.8
3	20	1.5	0.8	0.5
3	20	1.5	0.8	0.8
4	10	1.5	0.5	0.5
4	10	1.5	0.5	0.8
4	10	1.5	0.8	0.5
4	10	1.5	0.8	0.8
4	10	1.2	0.5	0.5
4	10	1.2	0.5	0.8
4	10	1.2	0.8	0.5
4	10	1.2	0.8	0.8
4	20	1.5	0.5	0.5
4	20	1.5	0.5	0.8
4	20	1.5	0.8	0.5
4	20	1.5	0.8	0.8

Shown in Figure 33 is the layout of an HBT with a multi-finger emitter of A_E = $240 \times 4 \times 120$ μm^2 designed for high power switches aiming at $I_C > 5$ A.

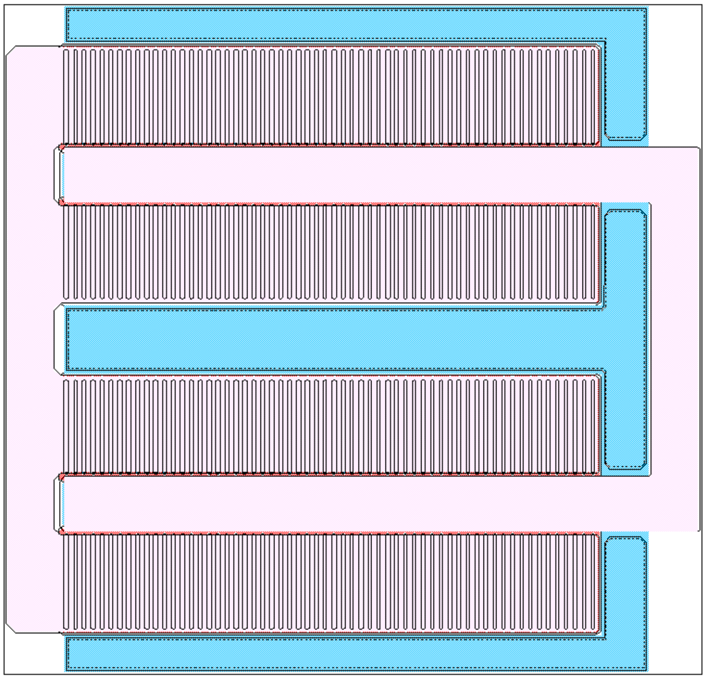


Figure 33. The layout of an HBT with A_E = $240 \times 4 \times 120$ μm^2 designed for high power switches.

4.3.2 Process Control Monitors

Several process control monitors (PCMs) are included in the photo-mask design. Figure 34 is the design of the collector metal via-chain. Similar via-chain designs also exist for emitter metal and base metal. After the via-hole opening and metal 1 deposition, discrete metal stripes connect with each other through the 20 via holes. The access resistance for each via-hole, which monitors the via-hole opening process, can be evaluated by measuring the resistance between these two contact pads.

Shown in Figure 35 are the TLM patterns for (from right to left) emitter contact, base contact, collector contact, on-wafer resistors (for example, NiCr), and device isolation. The via holes and metal 1 are also included in these TLM patterns, so TLM can be tested again after the surface passivation and via-hole etching to check if there is any process-induced contact resistance degradation.

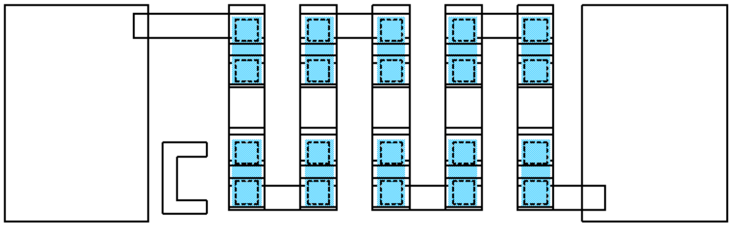


Figure 34. The design of a via-chain with 20 via holes for the collector metal. Similar via-chains exist for the emitter metal and base metal.

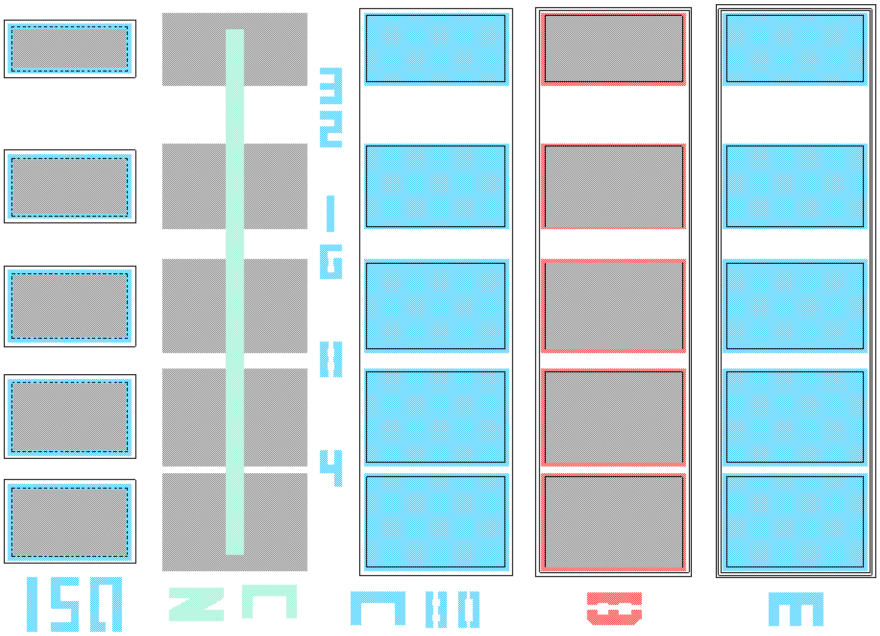


Figure 35. TLM patterns for (from right to left) emitter contact, base contact, collector contact, on-wafer resistors, and device isolation.

Figure 36 is the layout of an HBT with A_E = 20×20 μm^2 that can be measured before the surface passivation, via-hole etching, and metal 1 deposition. Therefore, these large-area square-emitter HBTs (with A_E = 20×20, 40×40, 60×60, and 100×100 μm^2) are useful as “quick-test” devices to provide a rapid feedback on the material and process quality before the whole fabrication process is completed.

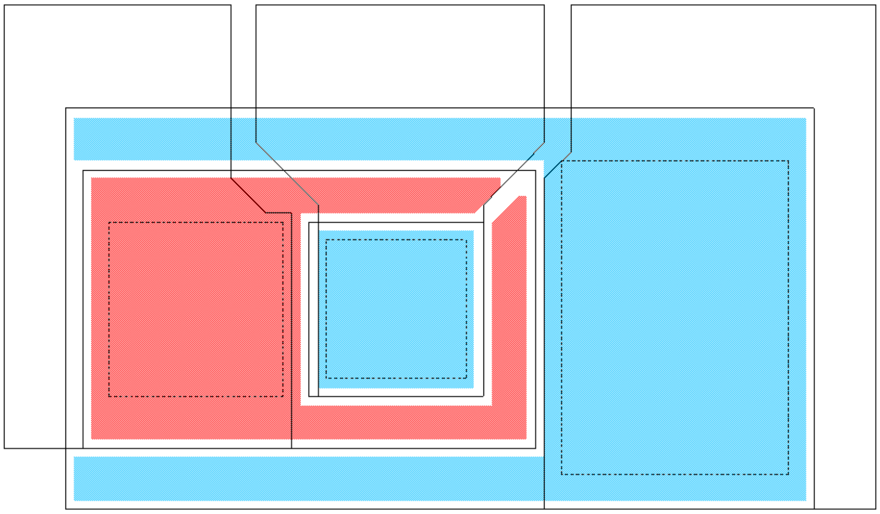


Figure 36. The layout of an HBT with A_E = 20×20 μm^2 that can be measured as a “quick-test” device before the whole fabrication process is done.

4.4 Device Fabrication

4.4.1 Fabrication Process Flow

The HBT fabrication processing flow is compatible with conventional GaAs-based HBT fabrication procedures. The device schematics is shown in Figure 37 [118]. Conventional vertical triple-mesa device scheme is applied without base or emitter re-growth. An *i*-line contact aligner is used for the photolithography steps. An STS™ ICP etching system is employed for the mesa etchings using a He/Cl_2-based gas mixture. E-gun evaporated SiO_2 layers are used as etching masks. The UV-assisted electrode-less wet-etching surface treatment is also applied to remove dry-etching-induced surface damages [38]. The Ti/Al/Ti/Au metal stack is deposited to form the ohmic contact on the *n*-type sub-collector and emitter layers. The *p*-type InGaN base contact uses a Ni/Au metal stack. However, the base contact is slightly Schottky due to the dry-etching-induced type-conversion on the extrinsic base surface and the relatively low free-hole concentration in the base. The post-device processing steps include BCB passivation, via-hole opening dry etching, NiCr resistor deposition, and finally, a thick E-gun evaporated Ti/Au layer to form the probing pads. Figure 38 (a) shows an SEM picture of a 4×10 µm^2 HBT prior to the post-device processing steps. Figure 38 (b) is a microscope picture of a fully fabricated HBT device with the RF measurement reference planes marked.

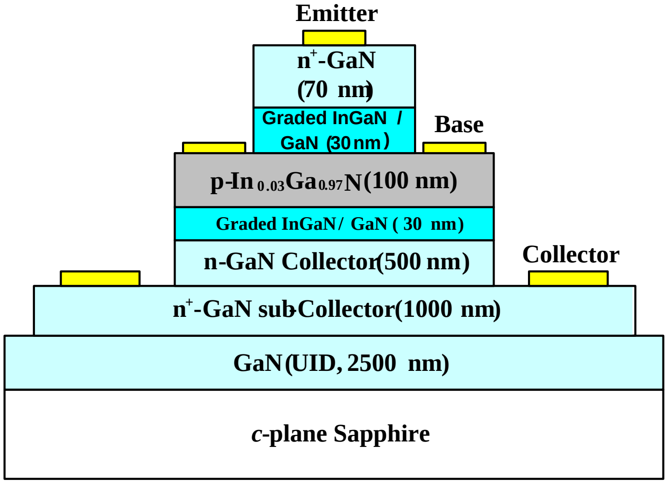
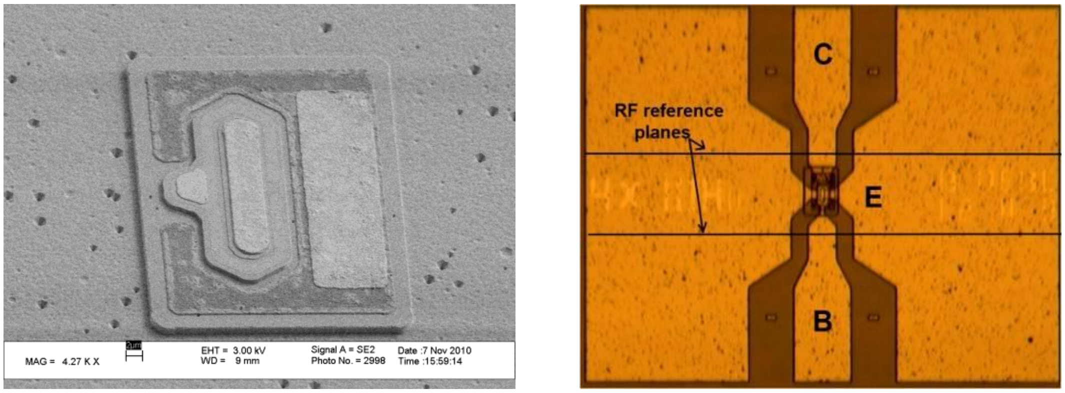

Emitter
n+-GaN (70 nm)
Graded InGaN / GaN (30 nm)
Base
p-In 0.03 Ga 0.97 N (100 nm)
Graded InGaN/ GaN (30 nm)
n-GaN Collector (500 nm)
Collector
n+-GaN sub-Collector (1000 nm)
GaN (UID, 2500 nm)
c-plane Sapphire

Figure 37. Schematics of the direct-growth GaN/InGaN *npn* DHBT.

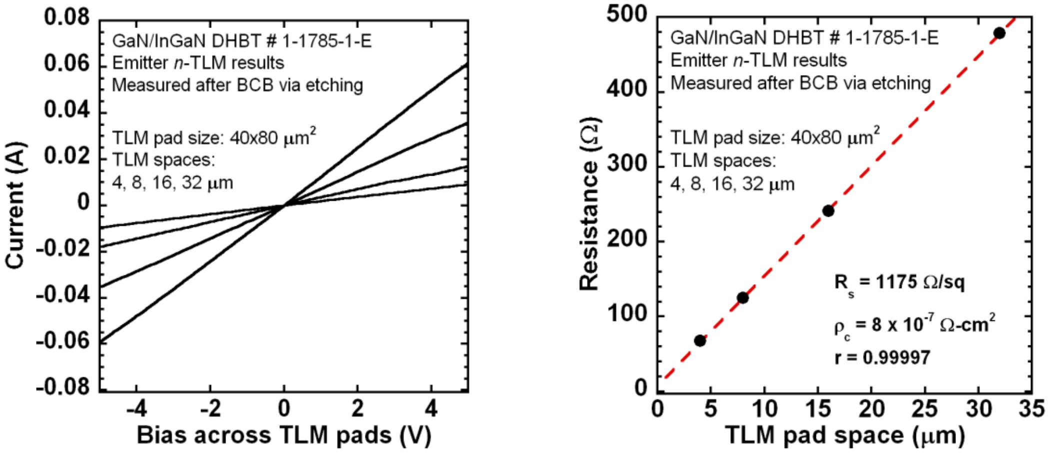

MAG = 4.27 K X
EHT = 3.00 kV
WD = 9 mm
Signal A = SE2
Photo No. = 2998
Date :7 Nov 2010
Time :15:59:14
C
RF reference planes
E
B

(a) (b)

Figure 38. (a) An SEM picture of an A_E = 4×10 µm^2 HBT prior to the device passivation. (b) A microscope picture of a fully fabricated HBT device. The device is designed in G-S-G coplanar waveguide configuration for common-emitter RF measurement.

4.4.2 Ohmic Contact on Emitter, Collector, and Base

E-gun evaporated Ti/Al/Ti/Au metal stacks (300/500/300/500 Å) are applied as the ohmic contact layer to *n*-type GaN. As shown in Figure 39 and Figure 40, ohmic contact is achieved on both emitter and sub-collector. Four-probe measurement method is applied to eliminate the cable resistance and probing resistance for an accurate evaluation of R_s and ρ_c. A typical R_{sh} for the emitter layer is 1000 ~ 1200 Ω/□ depending on different wafers and different positions on the wafer. ρ_c can be as low as 8×10^{-7} Ω cm^2 with a typical value lower than 3×10^{-6} Ω cm^2. For the sub-collector metal contact, typical R_{sh} and ρ_c are 80 Ω/□ and < 3.0×10^{-6} Ω cm^2, respectively. If the epitaxial layers are grown on GaN substrates, the sub-collector R_{sh} is typically < 2 Ω/□ because of the conductive *n*-type FS GaN substrate.

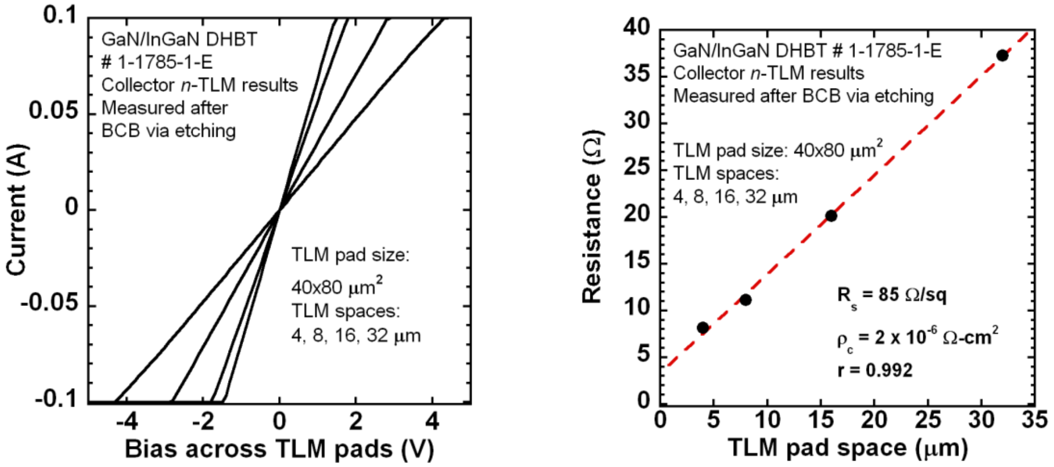


(a) (b)

Figure 39. The emitter TLM results of Ti/Al/Ti/Au on *n*-GaN in GaN/InGaN *npn* HBTs: (a) *I-V* curves of 40×80 μm^2 metal pads with different spaces, (b) linear fitting of measured resistances versus metal pads spaces.

An E-gun evaporated Ni/Au metal stack (50/50 Å) is used for the *p*-type InGaN contact. However, the base contact is non-ohmic. As shown in Figure 41, a 2.5-volt Schottky barrier exists and the *I-V* curves become linear only under a higher bias > 5 V.

The difficulty of forming ohmic contact on the base layer is due to the relatively low free-hole concentration in the *p*-InGaN base layer as well as the dry-etching-damaged surface and the consequent type-conversion [195]. In the previous work, methods to improve the base contact have been explored [118], and further improvement is still needed.



(a) (b)

Figure 40. The sub-collector TLM results of Ti/Al/Ti/Au on *n*-GaN in GaN/InGaN *npn* HBTs: (a) *I*-*V* curves of 40×80 μm^2 metal pads with different spaces, (b) linear fitting of measured resistances versus metal pads spaces.

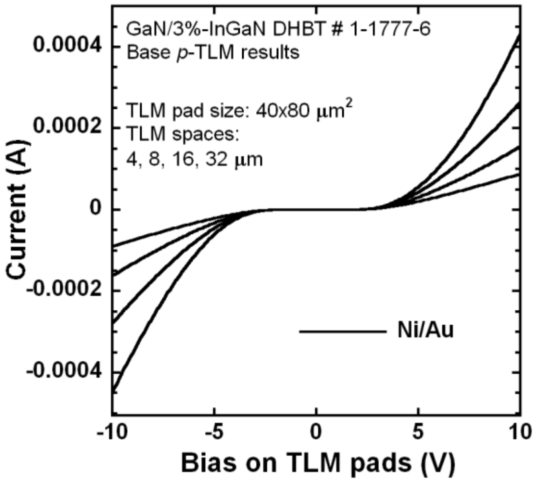
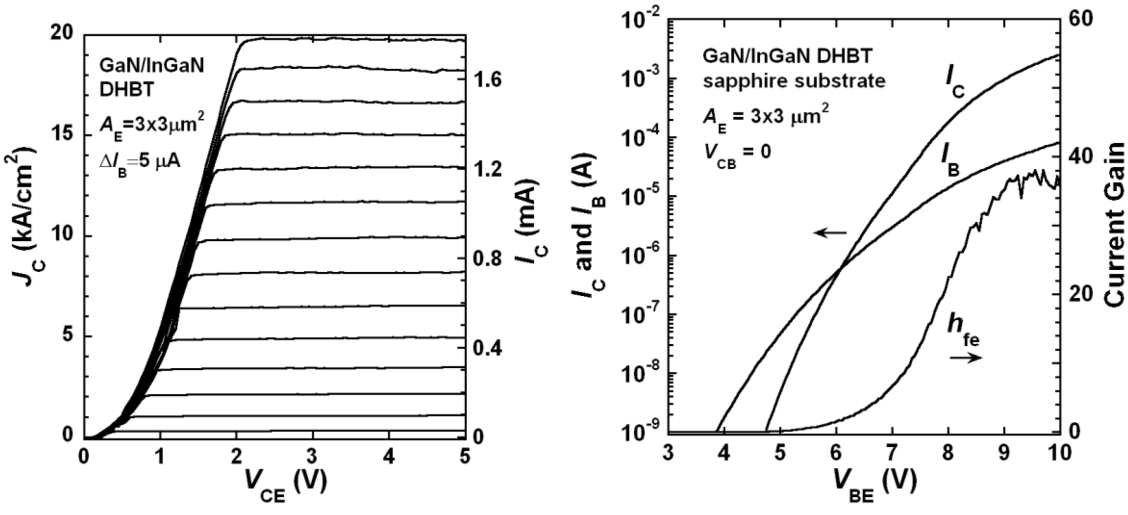


Figure 41. The base TLM results of Ni/Au on *p*-InGaN in GaN/InGaN *npn* HBTs: *I*-*V* curves of 40×80 μm^2 metal pads with different spaces.

4.5 D.C. Characteristics

4.5.1 Common-Emitter *I-V* Characteristics of HBTs on Sapphire

Fabricated *npn* GaN/$In_{0.03}Ga_{0.97}N$ HBTs are characterized using a Keithley SCS-4200 system at RT. Figure 42 (a) shows a set of common-emitter *I-V* family curves of an *npn* GaN/InGaN HBT with A_E = 3×3 μm^2 (Device ID: 1-1785-1-G-B4-3x3CV). The I_B increases from 5 μA to 70 μA with an increment of 5 μA per step. The collector voltage (V_{CE}) is swept from 0 to 5 V. At I_B = 70 μA, J_C reaches 19.8 kA/cm^2 (I_C = 1.78 mA) with a β of 25. The common-emitter V_{offset} is 0.22 V and the V_{knee} is 2.1 V.

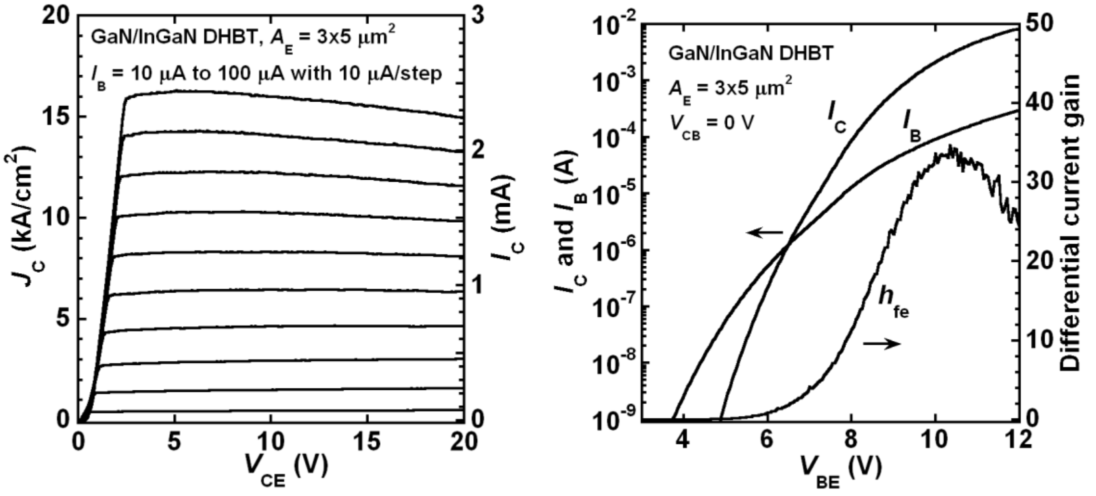


(a) (b)

Figure 42. (a) The common-emitter *I-V* family curves and (b) the Gummel plot of an A_E = 3×3 μm^2 GaN/InGaN *npn* HBT on a sapphire substrate. Device ID: 1-1785-1-G-B4-3x3CV.

Figure 42 (b) is the Gummel plot of the same A_E = 3×3 μm^2 HBT at V_{CB} = 0 V. At V_{BE} = 9.5 V and I_C = 1.75 mA (J_C = 19.4 kA/cm^2), a maximal h_{fe} of 38 is achieved. At V_{BE} = 10 V, I_C reaches 2.58 mA with a corresponding J_C of 28.6 kA/cm^2. However, one issue is that the V_{BE} in the Gummel plot for the peak h_{fe} is much larger than that in a typical III-V HBT. According to the I_B versus V_{BE} data in the Gummel plot, the BE diode series resistance (r_{BE}) is calculated to be 22.7 kΩ. Since the emitter resistance (r_E) is approximately 24 Ω based on the emitter TLM result and the emitter size, the overall base resistance (r_B) is larger than 22 kΩ, which dominates the r_{BE}. Therefore, the large V_{BE} issue is mainly due to the high base resistance.

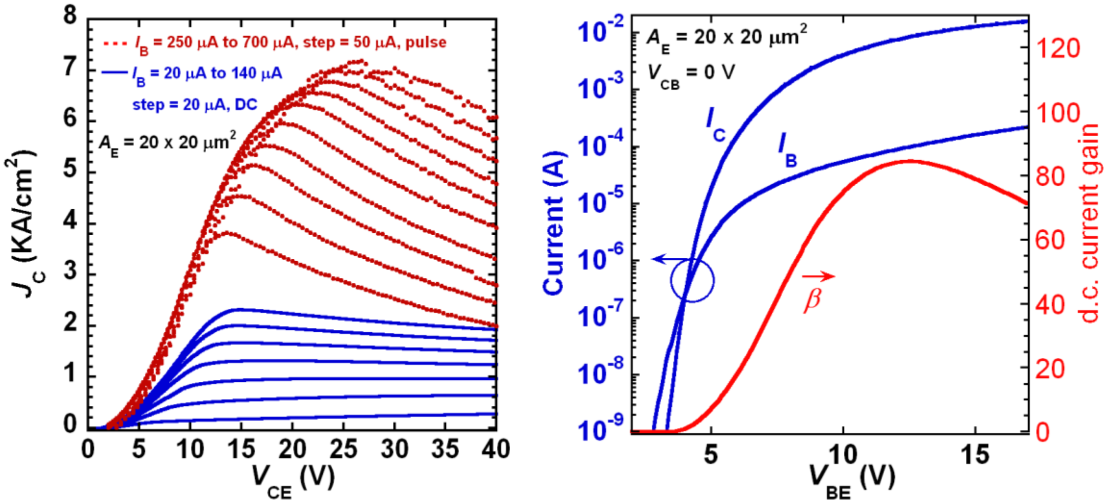
Figure 43 (a) illustrates a set of common-emitter *I-V* family curves of an $A_E = 3\times5$ μm^2 device from another sample fabricated in a different process batch (Device #: 1-1785-1-E-B1-3x5GV). Consistent device performance is achieved showing good fabrication process reliability. The I_B increases from 10 μA to 100 μA with an increment of 10 μA. The V_{CE} is swept from 0 to 20 V. The J_C peaks at 16.3 kA/cm^2 (I_C = 2.44 mA) with a β of 24. At higher V_{CE} and I_C, although J_C decreases because of the self-heating effect, a high power density of 300 kW/cm^2 is reached at V_{CE} = 20 V and J_C = 15.0 kA/cm^2. At I_B = 100 μA, the V_{offset} is 0.25 V and the V_{knee} is 2.4 V. Figure 43 (b) is the Gummel plot of this 3×5 μm^2 HBT at V_{CB} = 0. The maximal h_{fe} is 34 at V_{BE} = 10.5 V and I_C = 3.4 mA. At V_{BE} = 12 V, the I_C reaches 8.3 mA with a corresponding J_C of 55 kA/cm^2.



(a) (b)

Figure 43. (a) The common-emitter *I-V* family curves and (b) the common-emitter Gummel plot of an $A_E = 3\times5$ μm^2 GaN/InGaN *npn* HBT. Device ID: 1-1785-1-E-B1-3x5GV.

For medium-sized squared-emitter devices, Figure 44 (a) shows a set of common-emitter *I*-*V* family curves of an A_E = 20×20 μm^2 HBT (Device #: 1-1777-6-E-2c-a2-20um). The peak J_C is 7.2 kA/cm^2 at I_B = 700 μA and V_{CE} = 27 V. The V_{offset} is 1.8 V. The V_{knee} is 12.5 V at J_C = 2 kA/cm^2. Pulsed-mode measurement (pulse width = 500 μs, duty cycle = 5%) is applied when I_B > 250 μA using an Agilent B1505A high-power curve tracer. However, the self-heating is still severe due to the poor thermal conductivity of the sapphire substrate. As a result, a negative slope of I_C curve at high V_{CE} and high J_C is observed. The power density of > 240 kW/cm^2 is reached at V_{CE} > 38 V. Figure 44 (b) is the Gummel plot of this 20×20 μm^2 device at V_{CB} = 0 V. After the device BE junction burn-in stress testing, the maximum β reaches its peak value of 84 at V_{BE} = 12 V and I_C = 7.5 mA, and the maximum h_{fe} reaches 105 [117].

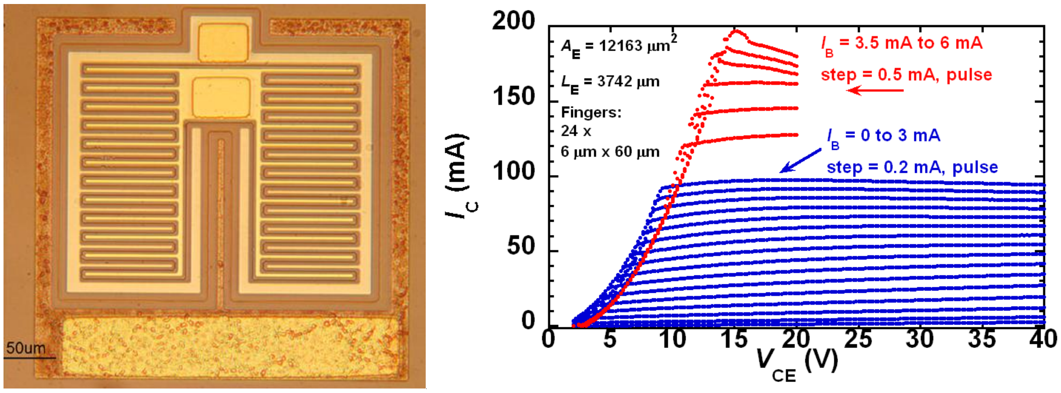


(a) (b)

Figure 44. (a) The common-emitter *I*-*V* family curves and (b) the common-emitter Gummel plot of an A_E = 20×20 μm^2 GaN/InGaN *npn* HBT. Device ID: 1-1777-6-E-2c-a2-20um.

Large-area multi-finger devices are also fabricated and tested. The multi-finger device has 24 emitter fingers (6×60 μm^2) with a total A_E = 12163 μm^2 including the contact area (Device ID: 1-1777-6-E-4c-fishbone24). Figure 45 (a) is a microscope picture of this multi-finger device. As shown in Figure 45 (b), I_C of 200 mA is achieved, which value is the highest one reported to date for III-N-based HBTs on sapphire substrates. It also shows a peak $\beta = 30$, a maximum $J_C = 1.62$ kA/cm^2 and maximum d.c. power = 3.76 W.

Compared to the $A_E = 20\times20$ μm^2 squared-emitter device, the β is lower for both the small-area HBT and the large-area multi-finger HBT, suggesting that the base current surface recombination is playing a significant role in these small-area or multi-finger devices with long emitter mesa perimeters. It is the so-called *emitter size effect* and will be further discussed in Section 4.4.3.



(a) **(b)**

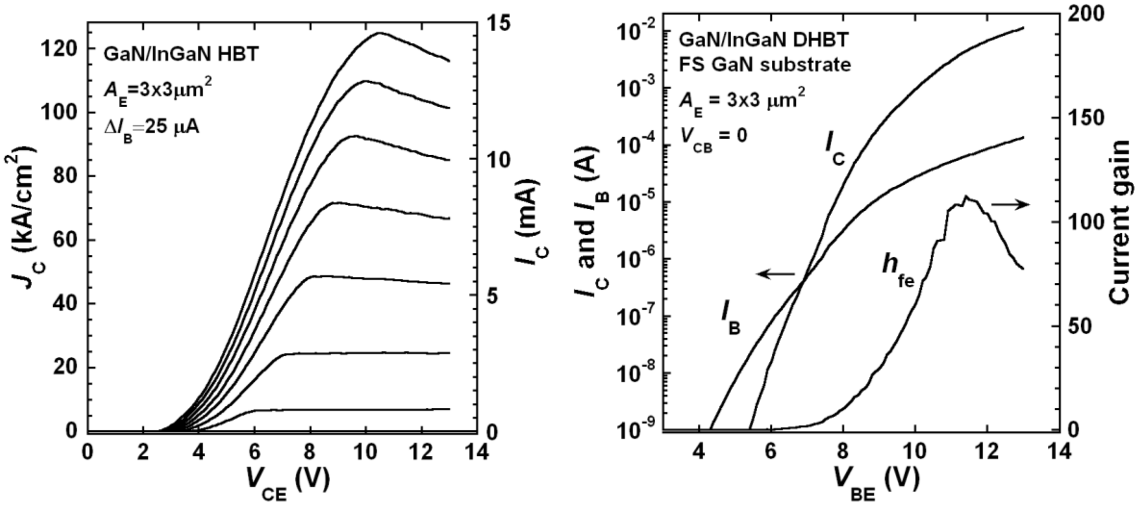
Figure 45. (a) The microscope picture of a 24×6×60 μm^2 multi-finger GaN/InGaN *npn* HBT. (b) The common-emitter *I-V* family curves of this multi-finger HBT. Device ID: 1-1777-6-E-4c-fishbone24.

4.5.2 Common-Emitter *I-V* Characteristics of HBTs on FS GaN

The widely used sapphire substrate is a foreign substrate for III-N materials with large lattice mismatch (14% to GaN), resulting in a high epitaxial material threading dislocation density on the order of 10^8~10^{10} cm^{-2}. These material defects act as carrier trap centers and leakage paths, which are serious problems especially for bipolar devices. Furthermore, the sapphire substrate has poor thermal conductivity, thereby limiting the device current and power handling abilities. To achieve higher current gains, higher J_C, higher power density, and higher breakdown voltages in III-N HBTs, the native FS GaN substrate is undoubtedly a better choice. Despite of its higher price than the sapphire substrate, a commercial 2-inch *c*-plane FS GaN substrate offers a relatively low threading dislocation density < 10^6 cm^{-2}. Kumakura *et al*. reported *pnp* AlGaN/GaN HBTs on FS GaN substrates with high I_C and high output power [114]. On the other hand, the *npn*-type III-N HBT on a FS GaN substrate, which is preferred for high-power RF applications, is reported for the first time in this study.

Figure 46 (a) illustrates the common-emitter *I-V* family curves of an A_E = 3×3 μm^2 GaN/InGaN *npn* HBT on a FS GaN substrate (Device ID: 1-1793-6-K-B4-3x3DV). Its I_B increases from 0 to 175 μA with an increment of 25 μA. The V_{CE} is swept from 0 to 13 V. A record J_C of 125 kA/cm^2 (I_C = 14.6 mA) is obtained at V_{CE} = 10.5 V. Although the I_C decreases with V_{CE} at the high J_C region as a result of the self-heating effect, a record power handling density of > 1.5 MW/cm^2 is achieved at V_{CE} = 13 V and I_C = 13.6 mA. Figure 46 (b) shows the common-emitter Gummel plot of this 3×3 μm^2 device at V_{CB} = 0. The maximal h_{fe} is 115 at V_{BE} = 12 V and I_C = 3.7 mA.

Using the Agilent B1505A high-power curve tracer, the quasi-static (1-ms pulse width with a 2-Hz repetition rate) common-emitter *I-V* family curves of an A_E = 3×3 μm^2 DHBT (Device #: 1-1793-6-L-B2-3x3CV) are measured and the results are shown in Figure 47. Because of the lesser heat accumulation in the pulsed-mode measurement, maximum J_C = 141 kA/cm^2 and power density = 3.05 MW/cm^2 are achieved at V_{CE} = 20.0 V and 22.5 V, respectively. The measured power density of 3.05 MW/cm^2 is 10 times higher than that of any reported GaN-based HBTs grown on GaN or SiC substrates [109,114], and 1.5 times higher than that of state-of-the-art submicron III-V HBTs [196].



(a) (b)

Figure 46. (a) The common-emitter *I-V* family curves and (b) Gummel plot of an A_E = 3×3 μm^2 GaN/InGaN *npn* HBT grown on a *c*-plane FS GaN substrate. Device ID: 1-1793-6-K-B4-3x3DV.

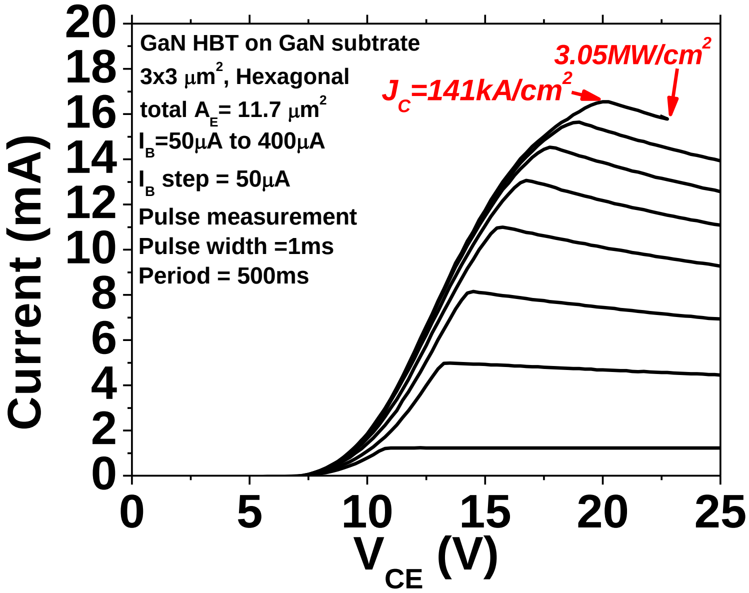


Figure 47. The common-emitter *I-V* family curves of an A_E = 3×3 μm^2 DHBT grown on a *c*-plane FS GaN substrate measured using 1-ms pulses at RT. Device ID: 1-1793-6-L-B2-3x3CV.

4.5.3 Analysis of Base Current Components

According to Equations 4.12, 4.13 and 4.14, the β of an HBT directly relates to the I_B that consists of I_{Bp} and four recombination components: $I_{B,bulk}$, $I_{B,scr}$, $I_{B,surf}$ and $I_{B,cont}$

according to different recombination locations. Therefore, an analysis on the I_B components is desired to understand the device performance and to propose β enhancement schemes. In the last section, the GaN/InGaN *npn* HBT on the FS GaN substrate has shown much higher β (and h_{fe}) at higher I_C than its counterpart on the sapphire substrate. The comparison between HBTs on sapphire and FS GaN substrates offers a convenient example to explore the I_B components.

Quantitively evaluating I_B components needs the knowledge on their characteristics, which are listed in Table 17 [178]. In general, $I_{B,scr}$, $I_{B,bulk}$ and I_{Bp} are proportional to the A_E and more relate to the material quality and layer structure design, while $I_{B,surf}$ and $I_{B,cont}$ are proportional to the P_E and more relate to the fabrication process. One method to distinguish these A_E-proportional components and P_E-proportional components is based on the measurement of the β of several HBTs with various P_E/A_E ratios. The idea of this method can be explained using the following equations [178]:

$$I_B = A_E(J_{B,bulk} + J_{B,scr} + J_{Bp}) + P_E(J_{B,surf} + J_{B,cont}) \tag{4.27}$$

$$\beta = I_C / I_B = J_C / J_B \tag{4.28}$$

$$\frac{J_C}{\beta} = (J_{B,bulk} + J_{B,scr} + J_{Bp}) + \frac{P_E}{A_E}(J_{B,surf} + J_{B,cont}) \tag{4.29}$$

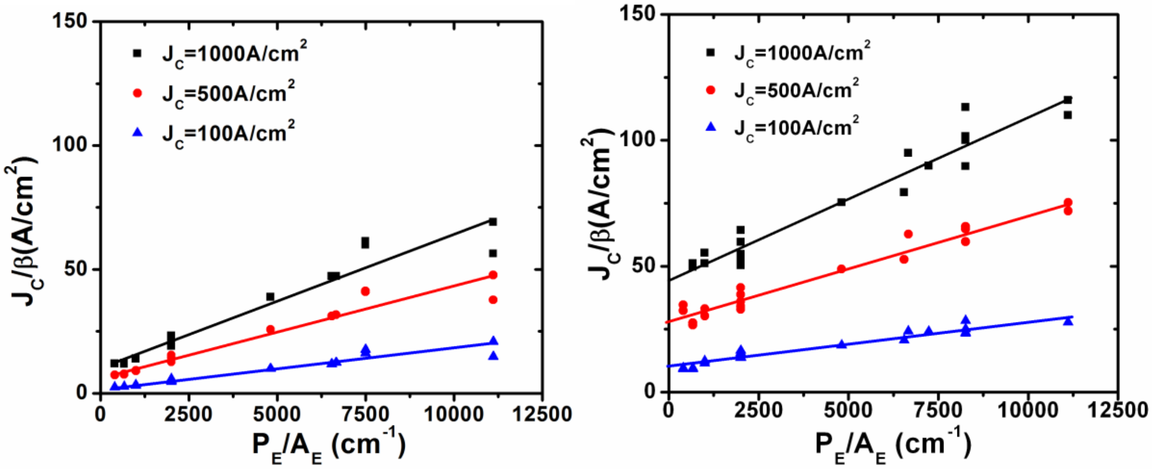
where $J_{B,bulk}$, $J_{B,scr}$ and J_{Bp} are normalized by A_E with the unit of A/cm^2; $J_{B,surf}$ and $J_{B,cont}$ are normalized by P_E with the unit of A/cm. Based on Equation 4.29, for HBTs with different P_E/A_E values, if plotting their J_C/β (in the y-axis) versus P_E/A_E at a given J_C, the linear-fitted y-intercept represents the sum of $J_{B,bulk}$, $J_{B,scr}$ and J_{Bp}, and the slope represents the sum of $J_{B,surf}$ and $J_{B,cont}$.

Table 17. Characteristics of base current components

Current component	Ideality factor (η)	Proportional to
$I_{B,scr}$	2	Area (A_E)
$I_{B,bulk}$	1	Area (A_E)
I_{Bp}	1	Area (A_E)
$I_{B,surf}$	2	Perimeter (P_E)
$I_{B,cont}$	1	Perimeter (P_E)

Figure 48 (a) and (b) show J_C/β versus P_E/A_E for HBTs on the FS GaN substrate (Sample ID: 1-1793-6-M) and on the sapphire substrate (Sample ID: 1-1785-1-G), respectively, at different J_C = 100, 500, and 1000 A/cm^2. The selected J_C values are relatively low to avoid the device self-heating issue and the emitter crowding issue. Large-area squared-emitter devices ($A_E = 20\times20$, 40×40, 60×60, and 100×100 μm^2) have smaller P_E/A_E values, while small-area devices have larger P_E/A_E values. These devices are measured after surface BCB passivation. The results of the statistical linear fitting for devices on different substrates at different J_C are listed in Table 18. At different J_C's, HBTs on the FS GaN substrate consistently show roughly 4.5 times lower $J_{B,bulk}+J_{B,scr}+J_{Bp}$ than those on the sapphire substrate. Since two samples have the same epitaxial layer structure, the reduction of $J_{B,bulk}+J_{B,scr}+J_{Bp}$ of devices on the FS GaN substrate should be mainly from the improved material quality.

On the other hand, in Figure 48, the slopes of the linear-fitting curves are not flat, meaning that the P_E-proportional $J_{B,surf}$ and $J_{B,cont}$ also play roles. It becomes a severe issue for small-area devices with large P_E/A_E ratios, which is the so-called *emitter size effect*. Although the wet-etching surface treatment has been applied, clearly, a more effective surface treatment or/and passivation technology is desired to suppress the process-induced base recombination current. Shown in Table 18, $J_{B,surf}+J_{B,cont}$ has similar values for the HBTs on the FS GaN substrate and sapphire substrate. It is expected because $J_{B,surf}+J_{B,cont}$ mainly depends on the process-induced surface recombination centers, and these samples are fabricated in the same processing batch.



(a) (b)

Figure 48. J_C/β versus P_E/A_E at J_C=100, 500, 1000 A/cm^2 for GaN/InGaN *npn* DHBTs on (a) a FS GaN substrate (Sample ID: 1-1793-6-M) and (b) a sapphire substrate (Sample ID: 1-1785-1-G).

Table 18. Summary of A_E-related and P_E-related base current components at different J_C for GaN/InGaN DHBTs on a GaN substrate and a sapphire substrate.

	$J_{B,bulk}+J_{B,scr}+J_{Bp}$ (A/cm^2)		$J_{B,surf}+J_{B,cont}$ (mA/cm)	
J_C (A/cm^2)	GaN substrate	Sapphire substrate	GaN substrate	Sapphire substrate
100	2.05	9.96	1.58	1.78
500	6.52	28.2	3.70	4.22
1000	10.5	45.2	5.39	6.40

Using the same analysis method, the effect of BCB passivation can be studied. Figure 49 shows J_C/β versus P_E/A_E at J_C = 100 A/cm^2 for HBTs on the FS GaN substrate (Sample ID: 1-1793-6-M) before and after BCB passivation. Only large-area devices are selected because small-area devices cannot be probed before passivation and metal 1 deposition. The statistical linear fitting shows that the value of $J_{B,bulk}+J_{B,scr}+J_{Bp}$ is 2.19 A/cm^2 and 1.57 A/cm^2 for devices before and after BCB, respectively, and the corresponding $J_{B,surf}+J_{B,cont}$ is 1.54 mA/cm and 1.81 mA/cm. Considering the statistical device variance, it is reasonable to say that the BCB passivation does not have significant effect on device performance. Because BCB is commonly used for monolithic microwave integrated circuit (MMIC), this result suggests that the III-N HBT fabrication process developed in this study with BCB passivation is compatible to the conventional MMIC fabrication technology.

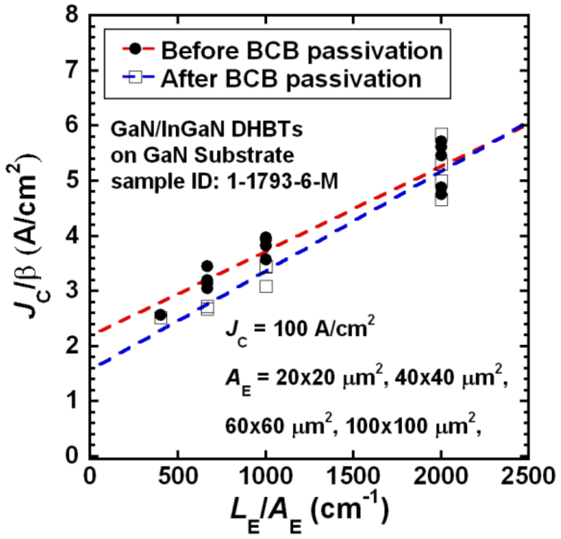


Figure 49. J_C/β versus P_E/A_E at J_C=100 A/cm^2 for GaN/InGaN *npn* DHBTs large-area devices before and after the BCB passivation. Sample #: 1-1793-6-M.

The above method is powerful to evaluate the $J_{B,surf}+J_{B,cont}$ and $J_{B,bulk}+J_{B,scr}+J_{Bp}$, but it cannot show which single I_B component has the dominant effect. The ideality factors η of these I_B components may help in further analysis. Equations 4.13 and 4.15 respectively show that I_{Bp} and $I_{B,bulk}$ are proportional to $\exp(\frac{qV_{BE}}{kT})$ because I_{En} is proportional to $\exp(\frac{qV_{BE}}{kT})$. So they have the ideality factors of 1 as listed in Table 17. While $I_{B,scr}$ has the η of 2 based on Equation 4.16. However, the ideality factors for $I_{B,surf}$

may have different values of 1 and 2 reported on different HBTs [178]. It is 2 in the GaN/InGaN HBTs in this study, which will be discussed later in this section.

Since β is defined as the ratio of I_C over I_B, it can be expressed as:

$$\begin{aligned}\beta &= \frac{I_C}{I_{Bp}+I_{B,bulk}+I_{B,scr}+I_{B,surf}+I_{B,cont}} \\ &= \frac{A\exp(\frac{qV_{BE}}{kT})}{B\exp(\frac{qV_{BE}}{kT})+C\exp(\frac{qV_{BE}}{kT})+D\exp(\frac{qV_{BE}}{2kT})+E\exp(\frac{qV_{BE}}{\eta_{surf}kT})+F\exp(\frac{qV_{BE}}{\eta_{cont}kT})} \quad (4.30) \\ &= \frac{1}{\frac{B+C}{A}+\frac{D}{A}\exp(-\frac{qV_{BE}}{2kT})+\frac{E}{A}\exp(\frac{1-\eta_{surf}}{\eta_{surf}}\frac{qV_{BE}}{kT})+\frac{F}{A}\exp(\frac{1-\eta_{cont}}{\eta_{cont}}\frac{qV_{BE}}{kT})}\end{aligned}$$

where A to F are linear-proportional factors, which can be seen as independent of β and V_{BE} for the first-order approximation. Use I_C to replace $A\exp(\frac{qV_{BE}}{kT})$:

$$\beta = \frac{1}{\frac{B+C}{A}+\frac{D}{A^2}I_C^{-0.5}+\frac{E}{A^2}\exp(\frac{1-\eta_{surf}}{\eta_{surf}})I_C+\frac{F}{A^2}\exp(\frac{1-\eta_{cont}}{\eta_{cont}})I_C} \quad (4.31)$$

Take log on both sides of Equation 4.31:

$$\log\beta = -\log(\frac{B+C}{A}+\frac{D}{A^2}I_C^{-0.5}+\frac{E}{A^2}\exp(\frac{1-\eta_{surf}}{\eta_{surf}})I_C+\frac{F}{A^2}\exp(\frac{1-\eta_{cont}}{\eta_{cont}})I_C) \quad (4.32)$$

Equation 4.32 reveals that if plotting log(β) versus log(I_C), the slope (n) of this curve and the base current ideality factor have the relationship of $\eta = \frac{1}{1-n}$. Therefore, this is one method to find out the dominant base current component by the ideality factor analysis. The advantage of this method is the direct relationship of β with I_C, so it can be applied to HBTs with non-ohmic base contact, which is the case in this study. Shown in Figure 50 are the log-β-versus-log-I_C curves for the $A_E = 3\times3\ \mu m^2$ HBTs on the FS GaN substrate and the sapphire substrate. Data is derived from Figure 46 (b) and Figure 42 (b), respectively. In the moderate I_C regions, the log-β-versus-log-I_C curve of the HBT on the FS GaN substrate has an n = 0.5, so its η is 2.0. While the log-β-versus-log-I_C curve of the HBT on the sapphire substrate has n = 0.44, so η is 1.8.

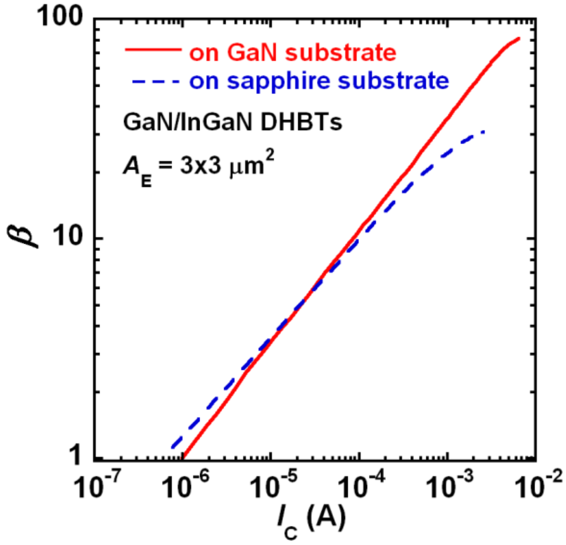


Figure 50. Measured log-β-versus-log-I_C plots for the HBTs on the FS GaN substrate (Device ID: 1-1793-6-K-B4-3x3DV) and sapphire substrate (Device ID: 1-1785-1-G-B4-3x3CV), A_E = 3×3 μm^2.

Therefore, the HBTs on the FS GaN substrate are dominated by base recombination current components with η = 2.0. According to Table 17, the $I_{B,scr}$ should be the major recombination mechanism in $J_{B,bulk}+J_{B,scr}+J_{Bp}$. It is because the base free-hole concentration is 10 times lower than the emitter free-electron concentration, so the BE depletion region is mainly in the base layer, where the carrier recombination rate is relatively high due to the narrower bandgap of InGaN. Furthermore, $J_{B,bulk}$ and J_{Bp} with η = 1 can be ignored because of the low-defect material and the hetero-barrier at the BE junction, respectively. In addition, Figure 48 (a) suggests that $J_{B,surf}+J_{B,cont}$ is also significant. So $J_{B,surf}$, the major factor in $J_{B,surf}+J_{B,cont}$, should have a η of 2.

η of 1.8 for the HBTs on the sapphire substrate means that some base current components with η = 1.0 cannot be ignored. Because the HBTs on different substrates have the same layer structure and fabrication process, I_{Bp} and $I_{\mathrm{B,cont}}$ may not be the cause. The major difference is from the material defect density, so the only possible I_{B} component that makes η lower than 2.0 is $I_{\mathrm{B,bulk}}$.

As shown in Figure 50, for the HBT on the FS GaN substrate, the slope of the log-β-versus-log-I_{C} curve starts to flatten when the I_{C} is higher than 3 mA. A similar phenomenon is observed in the HBT on the sapphire substrate, but it happens at a much lower I_{C} = 0.3 mA. The Kirk effect may not be the reason of the β flattening because both HBTs have the same epitaxial layer structure but show different J_{C} at the β turning points. Apparently some I_{B} components with η = 1 gradually dominate the I_{B} at the high I_{C} region.

The cause may be from the decreased γ at high temperature. In general, I_{Bp} can be ignored in HBTs due to the BE hetero-junction. However, this assumption is not true for HBTs working under a high temperature according to Equation 4.13. In addition, for *p*-type III-N materials, higher temperature will significantly enhance the dopant activation efficiency, thereby increasing the free-hole concentration in the base and lowering the γ. Because of the poor thermal conductivity of the sapphire substrate, the HBT grown on sapphire may have a higher junction temperature even the I_{C} is lower than that grown on the GaN substrate. Therefore, the β droop issue happens at a lower I_{C} level for the HBTs grown on sapphire substrates.

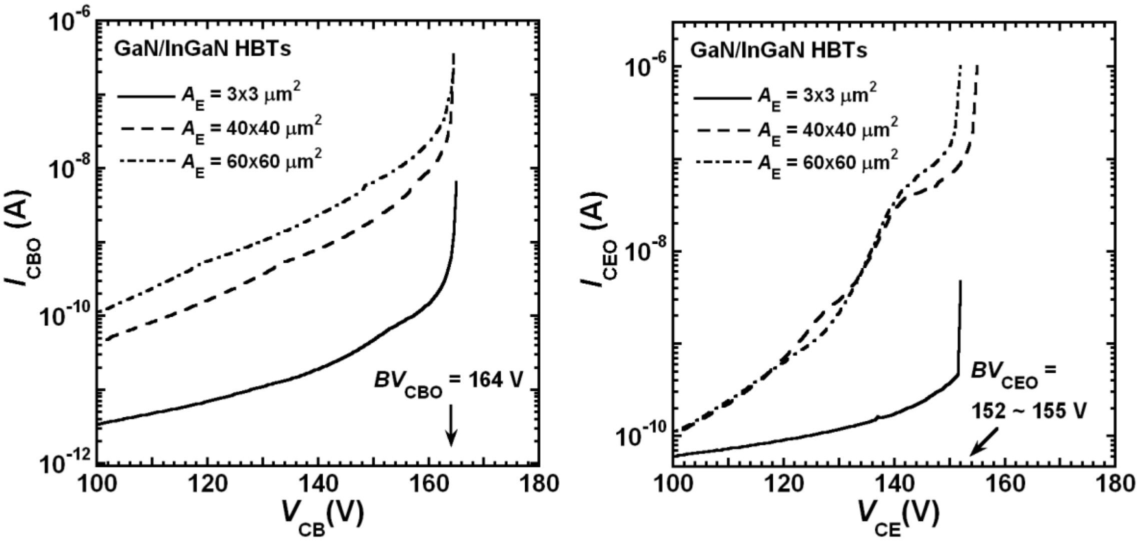
Another possible reason is $I_{\mathrm{B,bulk}}$ and the plausible explanation is the following. With the increase of V_{BE}, the thickness of the space-charge region reduces and the neutral base region expands. As a result, the $I_{B,bulk}$ becomes more important in the overall I_B, thereby lowering the η from 2 to 1. Because the HBT on the FS GaN substrate has a much lower $J_{B,bulk}+J_{B,scr}+J_{Bp}$ as shown in Table 18, this issue is not obvious until the device operates under a high I_C (or high V_{BE}) region.

It is also found that these β values shown in Figure 50 do not equal to those h_{fe} values in Figure 46 (b) and Figure 42 (b) at given I_C's. Based on the definitions of h_{fe} and β, their relationship can be expressed as $h_{fe} = \beta/(1\text{-}n) = \eta\beta$ [178]. Therefore, $h_{fe} = \beta$ only happens when the slope of the β-versus-I_C is zero, or in other words, the HBT has a constant current gain.

4.5.4 Breakdown Voltage

The characterization of leakage current and breakdown voltage is carried out on HBTs with different A_E of 3×3 μm^2, 40×40 μm^2, and 60×60 μm^2 grown on the FS GaN substrate (Sample ID: 1-1793-6-M). Figure 51 (a) shows open-emitter reverse-biased BC diode leakage current (I_{CBO}) curves and breakdown voltages (BV_{CBO}) of these devices. A consistent BV_{CBO} of 164 V is observed for different-sized devices. The corresponding material breakdown field is 6.4 MV/cm if assuming that most of the voltage drops on the 500-nm GaN collector layer and the electric field has a triangle shape. When biased below the avalanche breakdown voltage, different devices have I_{CBO} approximately proportional to the BC junction area. The 3×3 μm^2 device has the lowest I_{CBO} less than 4 pA at V_{CB} = 100 V. The low I_{CBO} is a direct proof of the low epitaxial material defect density grown on the FS GaN substrate.

Figure 51 (b) shows open-base collector-emitter leakage current (I_{CEO}) curves and breakdown voltages (BV_{CEO}) of these devices. Nearly identical BV_{CEO} between 152 V and 155 V are measured on different-sized devices. Consequently, the corresponding power switching figure of merit $BV_{\mathrm{CEO}} \times J_{\mathrm{C}}$ is calculated to be 21.4 MW/cm^2 for the 3×3 μm^2 device. When biased at a voltage close to BV_{CEO}, these devices show I_{CEO} roughly proportional to A_{E}. However, when devices are biased far below the BV_{CEO}, the I_{CEO} is no longer proportional to A_{E} for different-sized devices. The 3×3 μm^2 device shows higher I_{CEO} than that expected, which is caused by the electrically conductive FS GaN substrate, since the substrate leakage current cannot be ignored in the low I_{CEO} region and is not proportional to A_{E}. This conductive substrate may not be a severe issue for the d.c. characteristics but will lead to high-frequency substrate loss. This issue can be addressed by using semi-insulating substrates.



(a) **(b)**

Figure 51. (a) The I_{CBO} curves and (b) the I_{CEO} curves of GaN/InGaN *npn* HBTs with different A_{E} grown on the *c*-plane FS GaN substrate. Sample ID: 1-1793-6-M.

For HBTs grown on the sapphire substrate, the leakage current and breakdown voltage characterization is carried out on an $A_E = 3 \times 3\ \mu m^2$ device (Device ID: 1-1785-1-G-B2-3x3DV). Figure 52 shows I_{CBO} and I_{CEO} curves. The I_{CBO} is less than 3 pA until V_{CB} = 70 V, beyond which point, I_{CBO} increases exponentially with V_{CB}, and the BV_{CBO} is 126 V. Assuming that the total bias drops on the 500-nm GaN collector layer and the electric field has a triangle shape, the corresponding material breakdown field is calculated to be 5.0 MV/cm. The I_{CEO} curve shows that the BV_{CEO} is 118 V for this 3×3 μm^2 device on sapphire. The breakdown characteristics of HBTs on the FS GaN substrate and the sapphire substrate are summarized in Table 19.

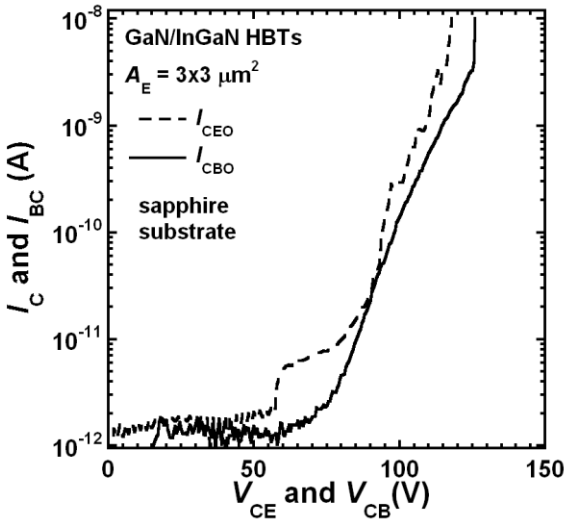
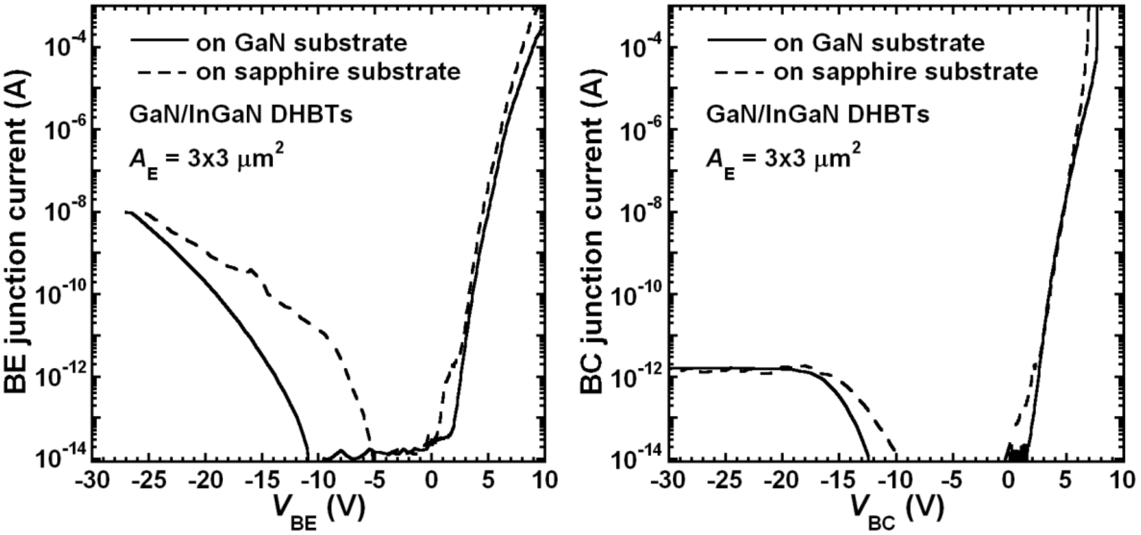


Figure 52. The I_{CBO} curve and I_{CEO} curve of an $A_E = 3 \times 3\ \mu m^2$ GaN/InGaN *npn* HBT on the sapphire substrate. Device ID: 1-1785-1-G-B2-3x3DV.

Table 19. Breakdown characteristics of HBTs on the FS GaN substrate and the sapphire substrate

	On FS GaN substrate	On sapphire substrate
BV_{CEO} (V)	152	118
BV_{CBO} (V)	164	126
GaN breakdown field (MV/cm)	6.4	5.0

The forward- and reverse-biased *I-V* curves of the BE diodes of the $A_E = 3\times3\ \mu m^2$ devices on the FS GaN substrate and sapphire substrate are plotted together in Figure 53 (a). When forward-biased prior to the diode turn-on, the BE diode on the sapphire substrate shows higher generation current, indicating more defect-induced generation-recombination centers in the epitaxial material. After the diode turns on, the BE junction on the sapphire substrate shows higher current at the same bias because of the higher saturation current (I_s). In the reverse-biased region, the BE diode on the sapphire substrate has higher leakage current because of more defects. The breakdown voltages (at a current compliance of 10 nA) of these two diodes are similar. Because the BE diode has high *n*- and *p*-type doping on both sides, so the breakdown characteristics is mostly determined by the high doping concentrations, not the material quality.



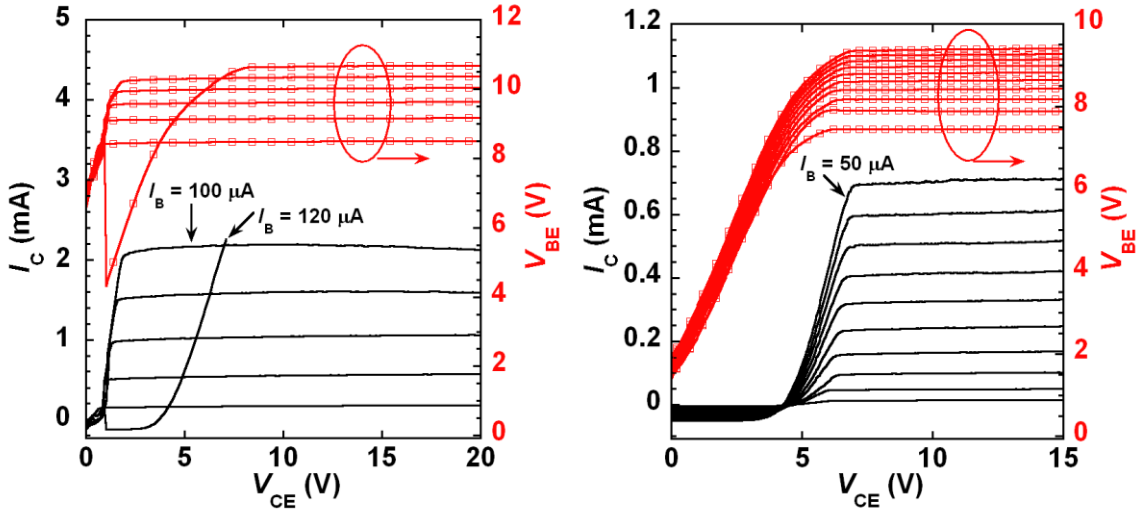
(a) (b)

Figure 53. The forward- and reverse-biased *I-V* curves of the (a) BE diodes and (b) BC diodes of $A_E = 3\times3\ \mu m^2$ devices on the FS GaN substrate and sapphire substrate.

The forward- and reverse-biased *I-V* curves of the BC diodes of the same $A_E = 3\times3\ \mu m^2$ devices are plotted together in Figure 53 (b). When forward-biased prior to the diode turn-on, the BC diode on the sapphire substrate also shows higher generation current, indicating more defect-induced generation-recombination centers in the epitaxial layer. After the diodes turn on, the *I*-*V* curves of the BC diodes overlap very well in the moderate current region.

4.5.5 Degradation of the Common-Emitter Offset Voltage

Compared to all the other III-N HBTs reported earlier, one important advantage of the GaN/InGaN *npn* DHBTs in this study is the low common-emitter V_{offset} and V_{knee} as shown in Figure 42 (a) and Figure 43 (a). The low V_{offset} and V_{knee} are due to the BC heterojunction design (the double-HBT design) and the laterally device down-scaling. However, devices show a reliability issue on the common-emitter V_{offset}, resulting in a sudden and permanent V_{offset} surge during high-I_B operation. Figure 54 (a) illustrates how this device failure happens during the measurement of common-emitter *I*-*V* family curves on one $A_E = 3\times5\ \mu\text{m}^2$ device (Device ID: 1-1785-1-E-B1-3x5GV) on the sapphire substrate. I_B increases from 20 to 120 μA with an increment of 20 μA. V_{CE} is swept from 0 to 20 V. At I_B = 100 μA, the V_{offset} is 0.25 V and V_{knee} is 2.4 V. But when the I_B is 120 μA and the device is still in the saturation region, the V_{BE} suddenly drops to a lower value and I_C becomes roughly -120 μA, meaning that most of the I_B flows to the collector. As a result, V_{offset} becomes larger than 4 V and the device needs a large V_{CE} to be driven into the saturation region again. Figure 54 (b) shows that this V_{offset} degradation is permanent: on the same device, the common-emitter *I*-*V* measurement performed again 5 days after the V_{offset} degradation happened. It still showed a V_{offset} of 4.3 V and a V_{knee} of 6.8 V at I_B = 50 μA.



(a) (b)

Figure 54. The common-emitter *I-V* family curves of an A_E = 3×5 μm^2 GaN/InGaN *npn* DHBTs (a) when the V_{offset} degradation happens, and (b) 5 days after the V_{offset} degradation. Device ID: 1-1785-1-E-B1-3x5GV.

Figure 55 shows the Gummel plots of the same device before and after the V_{offset} degradation. After the V_{offset} degradation happens, I_B slightly increases at the low- and moderate-current regions (< 10 μA), but slightly decreases at the high-current region. Assuming that the device has constant BE diode series resistance, I_B shows a higher saturation current (I_s) and a higher η. I_C also shows a similar trend. As a result, β degrades from 23 to 19 at V_{BE} = 10 V. Compared to the dramatically increased V_{offset}, the β degradation is relatively small, indicating that the device intrinsic part, especially the BE diode, is not obviously damaged.

The forward- and reverse-biased *I-V* curves of the BC diodes of this high-V_{offset} device (Devices B) and another device with a low V_{offset} (Device A) are plotted together in Figure 56 (a). For Device A, when reverse-biased, the BC diode leakage current is only several pA until -50 V. The leakage current hits the 10-nA compliance at 102 V without an avalanche breakdown, suggesting a BV_{CBO} of > 102 V. On the other hand, however, Device B shows a leaky BC diode. The reverse-biased leakage current is higher than 10 nA at only -1 V. Therefore, the V_{offset} degradation is most likely from the leaky external BC diode. The forward- and reverse-biased *I*-*V* curves of the BE diodes of Devices A and B are plotted together in Figure 56 (b). Because the BE diodes perform similarly, it is fair to say that the BE diodes do not play a critical role in this V_{offset} degradation issue.

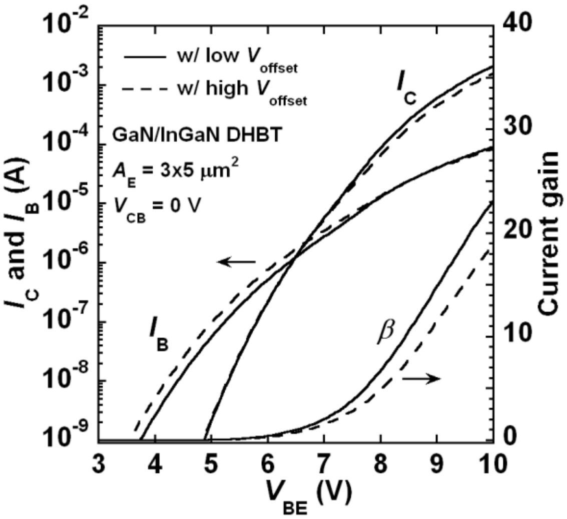
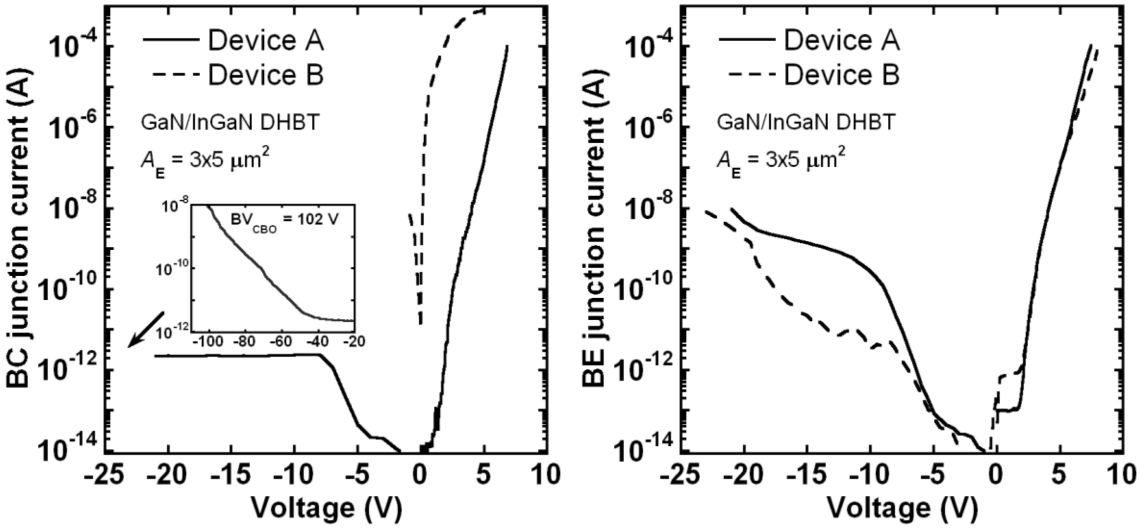


Figure 55. The Gummel plots of an A_E = 3×5 μm^2 GaN/InGaN *npn* DHBT on the sapphire substrate before and after the V_{offset} degradation.



(a) **(b)**

Figure 56. The forward- and reverse-biased *I*-*V* curves of the (a) BC diodes and (b) BE diodes of two A_E = 3×5 μm^2 HBTs on the sapphire substrate. Device A has a low V_{offset} but Device B has a high V_{offset}.

4.6 RF Performance of DHBTs on Sapphire Substrates

The S-parameters are measured by Mr. Yi-Che Lee using an Anritsu 37397D Vector Network Analyzer from 40 MHz to 20 GHz at RT. The devices are measured in the common-emitter coplanar waveguide (CPW) configuration. On-wafer short-open-load-through (SOLT) calibrations are used to move the RF reference planes to the lines indicated in Figure 38 (b).

As shown in Figure 57, the $|h_{21}|^2$ and MAG/MSG of an $A_E = 3\times5\ \mu m^2$ HBT (Device ID: 1-1785-1-G-B12-3x5DV) are measured at $V_{CE} = 6$ V and $J_C = 11.8$ kA/cm^2. The 20 dB/decade roll-off asymptotic line of the $|h_{21}|^2$ curve is used to obtain $f_T = 3.0$ GHz. A small-signal modeling shows that the high-frequency tailing of the $|h_{21}|^2$ curve is mainly due to the capacitive coupling between the emitter metal pad and the UID GaN buffer layer that is slightly *n*-doped. However, the measured f_{max} is only 950 MHz at MAG/MSG = 0 dB. This problem may be from the high base resistivity as well as the emitter design whose emitter length (L_E) over emitter width (W_E) ratio is small, which results in severe *emitter crowding effect* and large extrinsic base resistance (r_{Bx}) and intrinsic base resistance (r_{Bi}).

The GaN/InGaN *npn* HBTs in this study have vertical structures with I_B flowing horizontally from the base contacts to the center of the emitter region. The high base sheet resistance causes a large voltage drop as the I_B traverses through. Therefore, the effective BE junction voltage decreases from the BE mesa edge to the center. As a result, most of the current injection occurs near the edge of the emitter. This phenomenon is usually called the *emitter crowding effect*, which will be a serious problem for the HBT

RF performance if its base resistance is high: the central part of the transistor may cease contributing to the I_C, but still accounts for the r_E and RC delay.

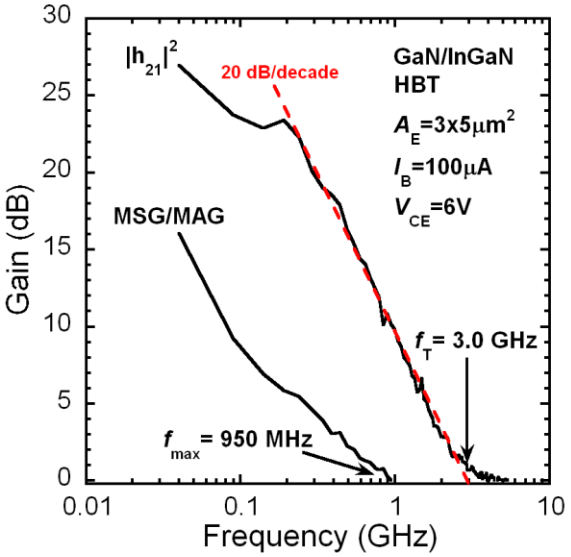


Figure 57. The measured $|h_{21}|^2$ and MAG curves of an $A_E = 3\times5$ μm^2 GaN/InGaN *npn* HBT on the sapphire substrate. Device ID: 1-1785-1-G-B12-3x5DV.

One figure of merit to quantify the emitter crowding effect is the effective emitter width (W_{eff}), which is defined as the emitter width that would result in the same current level if the current crowding was neglected and the J_C was uniform at its edge value. The W_{eff}/W_E ratio can be expressed as [178]:

$$\frac{W_{eff}}{W_E} = \frac{\sin c \cos c}{c} \tag{4.31}$$

$$c \tan c = \frac{q}{kT} \frac{I_E R_{sh,B} W_E}{4(\beta+1) L_E} \tag{4.32}$$

Therefore, the W_{eff} is determined by the base epitaxial material and the emitter geometry. Clearly, a “slim” emitter design with a large L_E/W_E value helps improving the emitter current uniformity and suppressing the emitter crowding effect. Furthermore, a large value of L_E/W_E is also beneficial in terms of r_{Bx} and r_{Bi} according to their expressions [178]:

$$r_{Bi} = \frac{r_{Bi(tvs)}}{4}\left[\frac{\tan c - c}{c\tan^2 c}\right] \tag{4.33}$$

$$r_{Bi(tvs)} = \frac{R_{sh,B}W_E}{L_E} \tag{4.34}$$

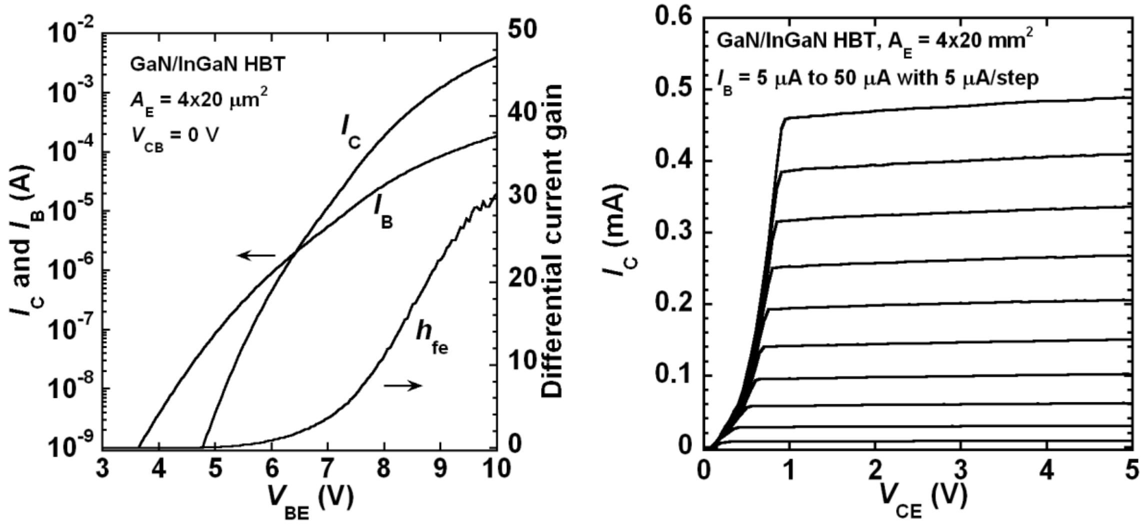
$$r_{Bx} = R_{sh,B}\frac{P_E}{L_{BE}} \tag{4.35}$$

where L_{BE} is the base metal to emitter mesa space. For this $A_E = 3\times5$ μm^2 HBT, based on the base TLM result ($R_{sh,B}$ = 300 kΩ/□) shown in Section 4.3.2, the calculated W_{eff} is 29.6%, r_{Bx} is 9.30 kΩ, and r_{Bi} is 8.02 kΩ. Apparently the too large base resistance will significantly limit the power current gain and f_{max}.

To achieve better f_{max} and f_T, one way is to design a device with a longer L_E and a thinner W_E. An HBT with $A_E = 4\times20$ μm^2 (Device ID: 1-1785-1-G-B4-4x20DV) is selected. Before the RF testing, its has been characterized for d.c. common-emitter performance and the results are shown in Figure 58. Figure 58 (a) shows that this device has $h_{fe} > 30$ at V_{BE} = 10 V and Figure 58 (b) shows that it has low V_{offset} and V_{knee}.

As shown in Figure 59, the frequency-dependent $|h_{21}|^2$ and MAG are measured at V_{CE} = 7 V and J_C = 4.7 kA/cm^2 for this $A_E = 4\times20$ μm^2 HBT. Compared to the $A_E = 3\times5$ μm^2 HBT, using the same evaluation method, the calculated W_{eff}/W_E is 41.3%, r_{Bx} is 1.70 kΩ, and r_{Bi} is 3.27 kΩ for this $A_E = 4\times20$ μm^2 DHBT. Due to the increased W_{eff}/W_E and reduced base resistances, f_T of 5.3 GHz is determined from the asymptotic 20 dB/decade line fitting on the measured $|h_{21}|^2$ curve. f_{max} of 1.3 GHz is also determined at MAG = 0 dB. This is the first demonstration of RF *npn* III-N HBTs showing a $f_T > 5.3$ GHz and a

f_{max} > 1.3 GHz. The device is unconditionally stable for frequencies up to 20 GHz. *MAG* does not show the 20 dB/decade roll-off characteristics as seen in typical HBTs. It is because the curve is still transitioning from the low-frequency gain region to the high-frequency roll-off region before it reaches the unit-gain frequency.



(a) (b)

Figure 58. (a)The Gummel plot of an *npn* GaN/InGaN HBT with $A_E = 4 \times 20$ μm^2 on a sapphire substrate, and (b) its common-emitter *I-V* family curves. Device ID: 1-1785-1-G-B4-4x20DV.

The J_C-dependent f_T and f_{max} values of this 4×20 μm^2 HBT are plotted in Figure 60. f_T increases monotonically with J_C and peaks at J_C > 5 kA/cm^2. A similar trend is found for f_{max}, which peaks at a value of 1.3 GHz for J_C > 3 kA/cm^2. When plotting τ_{ec} (= $1/(2\pi f_T)$) against $1/I_C$ (the inset of Figure 60), according to the Equations 4.19 and 4.20, the sum of the base transit time, BC space-charge transit time, and the collector charging time is estimated to be 26 ps when one linearly extrapolates the curve to $1/I_C = 0$. Possible RF performance improvements for GaN/InGaN HBTs include further reduction in the base resistance and growing these structures on substrates with better thermal conductivity for high-current operation.

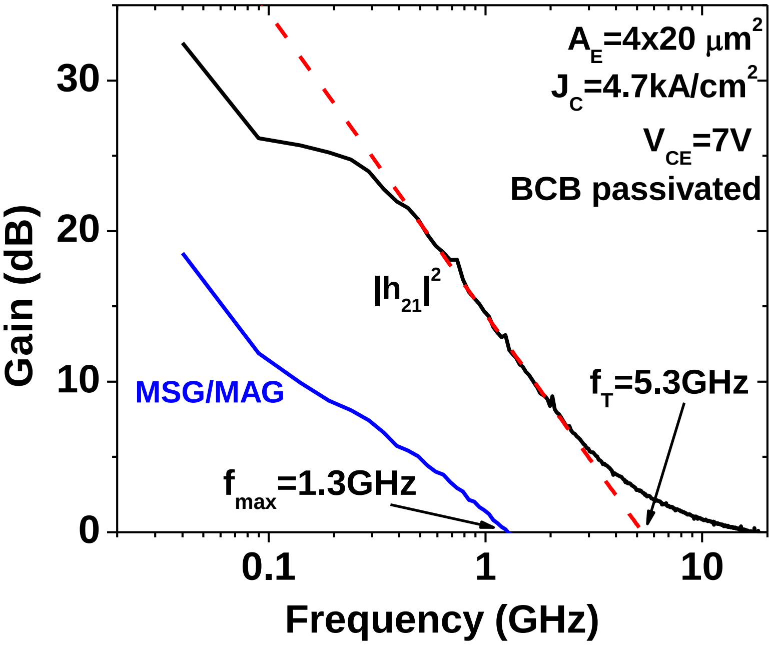


Figure 59. The measured $|h_{21}|^2$ and MAG of an A_E = 4×20μm^2 GaN/InGaN *npn* DHBT. Device ID: 1-1785-1-G-B4-4x20DV.

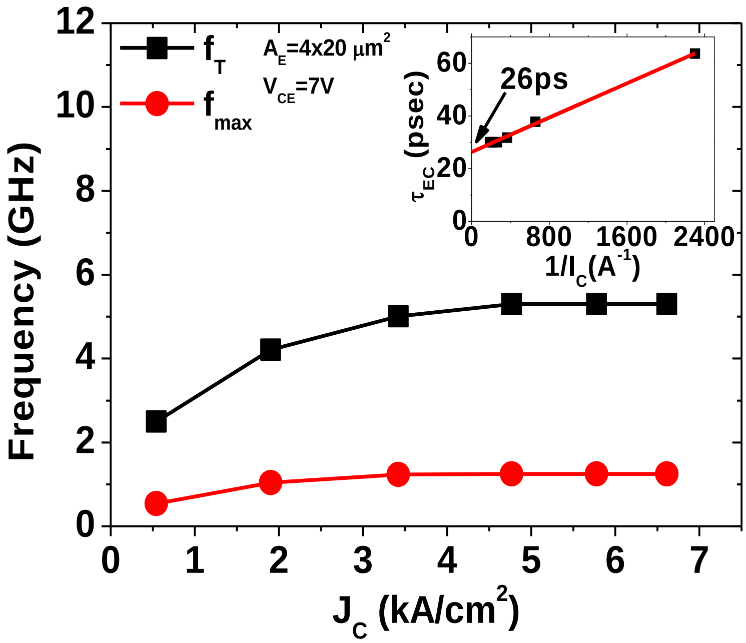


Figure 60. The f_T and f_{max} of an A_E = 4×20μm^2 GaN/InGaN *npn* DHBT at different J_C. Device ID: 1-1785-1-G-B4-4x20DV.

For those GaN/InGaN *npn* HBTs grown on FS GaN substrates presented in Section 4.5.2, the RF characterization cannot be correctly carried out as a result of the RF loss on the conductive GaN substrate. To address this substrate RF loss issue, semi-insulating GaN substrates or SiC substrates are possible substrate alternatives.

4.7 Summary

High-power RF GaN/InGaN *npn* DHBTs grown on *c*-plane sapphire substrates and FS GaN substrates have been successfully developed. As shown in the III-N HBT current-gain-versus-J_C comparison chart in Figure 61, the GaN/InGaN DHBTs in this study are among the best devices reported.

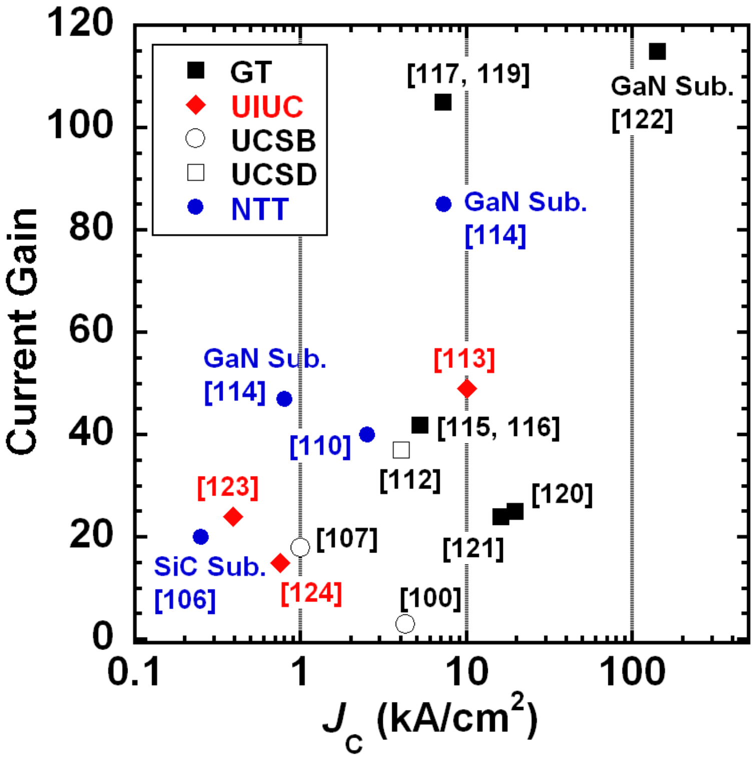


Figure 61. Current-gain-versus-J_C comparison chart for state-of-the-art III-N HBTs. Data points without substrate information shown in this plot are all from HBTs on sapphire substrates.

On sapphire substrates, the first RF performance on III-N HBTs with f_T > 5.3 GHz and f_{max} > 1.3 GHz has been demonstrated. The measured BV_{CBO} and BV_{CEO} are 126 V and 118 V, respectively.

On FS GaN substrates, a maximal h_{fe} of 115, a large J_{C} of 141 kA/cm^2 and a large d.c. power density of 3.05 MW/cm^2 are achieved. The measured BV_{CBO} and BV_{CEO} are 165 V and 152 V, respectively. These results represent the best d.c. performance reported in any III-N HBTs, suggesting that III-N HBTs are promising devices for the next-generation RF and power electronics.

CHAPTER 5

SUMMARY AND FUTURE WORK

III-N-based optoelectronic and electronic devices have been actively explored for more than 15 years. Nowadays, more and more III-N technologies are being transferred from research laboratories to foundries and become of great commercial importance, showing their potentials extending beyond the capabilities of the conventional III-V and Si technologies. As the biggest market of III-N devices, the high-brightness LED market reached annual global revenue of 10 billion US dollars in 2010. The RF and power electronics markets based on III-N HFET technology are also growing rapidly. On the other hand, as a relatively new field, the III-N technology is still not mature, and many promising devices are under development. The purpose of this study is to develop advanced fabrication technologies for III-N bipolar devices, particularly for GaN DUV *p-i-n* APDs, InGaN/GaN MQW LDs, and GaN/InGaN *npn* high-power RF HBTs.

Geiger-mode GaN *p-i-n* APDs have important applications in DUV and UV single-photon detections. Owing to their WBG nature, GaN- and AlGaN-based APDs offer extremely low noise, high sensitivity, and filter-free visible-blind or solar-blind detection ability. In the fabrication of GaN *p-i-n* APDs, the major technical challenge is the dry-etching-induced surface damage. To address this issue, a wet-etching surface treatment technique has been developed using DOE and ANOVA. The first Geiger-mode DUV GaN APD with a front-illuminated homojunction *p-i-n* diode structure is demonstrated on a FS GaN substrate with SPDE of 1.0 % and DCP of 0.03 at λ = 265 nm. A record photo current avalanche gain > 10^5 is also demonstrated at λ = 360 nm. When the APD is biased at -20 V, the J_{dark} is lower than 40 pA/cm^2, and the R_λ is 140 mA/W at 360 nm. In addition, the NEP is 4.27×10^{-17} W-Hz$^{-0.5}$, the D^* is 1.66×10^{14} cm-Hz$^{0.5}$-W^{-1}, and the minimum detectable optical power is 100 fW. These values are all among the best ones reported to date for III-N *p*-*i*-*n* APDs.

The future work for the GaN *p*-*i*-*n* APD research is to increase the SPDE. The major issue may be from the layer structure design. Due to the background doping the *i*-layer is slightly *n*-doped, resulting in a non-uniform (triangle shape) electrical field distribution. Therefore, the avalanche breakdown more easily happens near the *p*-region, and the impact ionization may not be strong enough to support high optical avalanche gain elsewhere in the whole depletion region. Further study will be on the novel device layer structure design for improved electrical-field uniformity in the the *i*-layer.

InGaN/GaN-based violet/blue/green LDs are the coherent light sources for high-density optical storage systems and the next-generation full-color LD display systems. In this study, the fabrication technology for InGaN/GaN MQW current-injection edge-emitting LDs has been successfully developed. 460-nm CW-mode lasing at RT is achieved with the J_{th} of 5.67 kA/cm^2 and the V_{th} is 9.05 V. When operation under the pulsed-current mode, the device has J_{th} of 3.3 kA/cm^2 and the corresponding V_{th} is 5.9 V.

A step-graded $\mathrm{Al_xGa_{1-x}N}$ EBL is introduced and enhanced η_{i} has been observed on 420-nm InGaN/GaN-based MQW LDs. When compared to the single-layer abrupt $\mathrm{Al_{0.18}Ga_{0.82}N}$ EBL design, η_{i} is dramatically increased from 0.60 to 0.92, while α_{i} keeps almost unchanged at 9 ~ 10 cm^{-1}. With this simple structure modification, J_{th} is reduced from 4.6 kA/cm^2 to 2.5 kA/cm^2, and the corresponding slope efficiency is increased from

0.72 W/A to 1.03 W/A under the pulsed-current condition. CW-mode operation is also achieved: the J_{th} is 3.38 kA/cm^2 and the slope efficiency is 1.35 W/A,

The next goal of the research on the InGaN/GaN MQW LDs is to achieve lasing $\lambda > 520$ nm. Future research will be mainly on the epitaxial material growth optimization on *c*-plane FS GaN substrates. It is a challenge to grow high-quality indium-rich InGaN/GaN QWs for green LDs. Furthermore, work can be further done on the novel LD structure design. For example, a new EBL structure consisting active-region-friendly and lattice-matched InAlN layer has been developed in the green LED structure showing dramatically enhanced quantum efficiency [197]. The InAlN EBL is expected to provide a more effective electron confinement than typical AlGaN EBLs without detrimental effects due to lattice mismatch and high growth temperatures.

III-N HBTs are promising devices for the next-generation RF and power electronics because of their advantages of high breakdown voltages, high power handling capability, high-temperature operation ability, and normally-off operation, etc. In this study, the wet-etching surface treatment has also been employed to reduce the surface recombination current on the extrinsic base region. Metallization processes have been carefully optimization on emitter, base, and sub-collector for low contact resistances. As a result, $h_{\text{fe}} > 100$ and power density > 0.3 MW/cm^2 are achieved on GaN/InGaN *npn* HBTs on sapphire substrates. $f_{\text{T}} > 5.3$ GHz and $f_{\text{max}} > 1.3$ GHz are also demonstrated for the first time. When this technology is transferred to the *c*-plane FS GaN substrate that has lower defect density and better thermal dissipation ability, a record $h_{\text{fe}} > 115$, $J_{\text{C}} >$ 141 kA/cm^2, and power density > 3.05 MW/cm^2 are obtained.

The next goal of the research on the GaN/InGaN *npn* HBTs is to demonstrate the first RF and power electronic circuits based on the III-N HBT technology developed at Georgia Tech. Despite those existing decent results on the GaN/InGaN HBTs presented in this thesis, the high base resistance and the Schottky barrier on the base metal contact prevent their applications in real circuits. To solve these problems, future work will be focused on the base layer design as well as fabrication process optimization. For the base layer design, first, the base layer thickness can be slightly increased for reduced base resistance. According to the analysis in Section 4.4.3, the $I_{B,scr}$ is the dominant base recombination mechanism, so the slightly increased base thickness, which only increases the $I_{B,bulk}$, will not significantly affect the β. Although the f_T may be decreased due to the longer base transit time, the f_{max} should be enhanced because of the reduced base resistance. In addition, several base layer designs utilizing the piezoelectric effect will be also studied to enhance the base free-hole concentration.

There are several issues need to be addressed in the fabrication process. First, proper dielectric passivation techniques are highly desired to suppress the base surface recombination current and the consequent emitter size effect. Second, the large Schottky barrier at the base metal contact is partly from the dry-etching-induced surface states, so methods to reduce the dry-etching damage are valuable. Possible solutions include an optimized low-damage dry etching technique and a wet-etching technique to expose the base region. Third, the base metallization recipe also needs further optimization to lower the Schottky barrier and reduce the contact resistance.

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