Fully-Integrated DLL/PLL-Based CMOS Frequency Synthesizers for Wireless Systems

A Dissertation
Presented to
The Academic Faculty

by

Jaehyouk Choi

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2010

Fully-Integrated DLL/PLL-Based CMOS Frequency Synthesizers for Wireless Systems

Approved by:

Dr. Emmanouil M. Tentzeris
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Chang-Ho Lee
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Jongman Kim
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Sung Ha Kang
School of Mathematics
Georgia Institute of Technology

Date Approved: July, 2010

ACKNOWLEDGEMENTS

First of all, I would like to acknowledge the enthusiastic supervision of my research advisor, Professor Emmanouil M. Tentzeris. Without his guidance and encouragement, my research work would not be completed.

I would also thank the defense committee members, Professor Saibal Mukhopadhyay, Professor Chang-Ho Lee, Professor Jongman Kim, and Professor Sung Ha Kang for their precious time, cooperation, suggestions.

I am grateful of Dr. Joy Laskar who guided and taught me with his endless energy and encouragement. I would like to thank Dr. Kyutae Lim and Dr. Woonyun Kim for their advice and support for my research.

I am greatly indebted to the members of the Microwave Applications Group (MAG) for their assistance and cooperation, especially to cognitive radio (CR) team members. I also owe special thanks to the senior engineers in Samsung Design Center for helpful discussion and encouragement.

To my parents, who have been shown great love and support in my life, I would like to express my deepest love and thank to them.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SUMMARY

A frequency synthesizer plays a critical role in defining the performance of wireless systems in terms of measures such as operating frequency range, settling time, phase noise and spur performance, and area/power consumption. As the trend in mobile system design has changed from single-standard systems to multi-standard/multi-application systems, the role of frequency synthesizers has become even more important.

As the most popular architecture, a phase-locked loop (PLL)-based frequency synthesizer has been researched over the last several decades; however, many unsolved problems related to the PLL-based synthesizer are still waiting for answers. This dissertation addresses key challenges related to fully integrated PLL-based frequency synthesizers, including the problem of large area consumption of passive components, the inherent reference-spur problem, and the problem of trade-offs between integer-N PLLs and fractional-N PLLs.

In this dissertation, new techniques and architectures are presented and developed to address those challenges. First, a low-phase-noise ring oscillator and a capacitor multiplier with a high-multiplication factor efficiently minimize the silicon area of sub-components, and a compact programmable delay-locked loop (DLL)-based frequency multiplier is developed to replace the PLL-based frequency synthesizer. Second, the charge-distribution mechanism for suppressing reference spurs is theoretically analyzed, and an edge interpolation technique for implementing the mechanism is developed. Finally, the concept and the architecture of sub-integer-N PLL is proposed and implemented to remove trade-offs between conventional integer-N PLLs and fractional-N PLLs.

CHAPTER 1

INTRODUCTION

1.1. Background

Over the last several decades, wireless communications have gained attention as the industry introduced affordable consumer products in order to expand the market. The industry has provided a variety of wireless applications, including cordless phones, cellular phones, global positioning systems (GPS), wireless local area networks (WLAN), and personal communication systems (PCS).

Almost all modern electronic systems, including wireless communication applications, require an appropriate reference clock to function. For example, analog-to-digital converters (ADCs) utilize a low jitter reference clock to achieve the targeted dynamic range. Clock-data-recoveries (CDRs) also require a reference signal in order to extract a clock from the incoming data streams and correct their timing. In microprocessors, a reference clock is also adopted to distribute clock signals to various parts of the chip.

Wireless communication systems also have to equip a reference clock with high phase noise performance to provide the system with a local oscillating clock. For wireless communication systems, which require a set of reference signals for target output frequency bands, frequency synthesizers that generate reference signals are particularly important because they determine system performance using such measures as frequency

range, settling time, phase noise and spur performance, power consumption, and silicon area.

While there are many frequency synthesizing architectures, a phase-locked loop (PLL)-based frequency synthesizer is the most popular choice for generating a reference clock. For the last decade, many topologies and circuit techniques of PLL-based frequency synthesizers have been researched to satisfy the requirements of various wireless applications. However, because of the great demands from the expanding market and emerging applications, challenges remain for frequency synthesizer designs.

This dissertation discusses the three key challenges of monolithic PLL-based frequency synthesizers and proposes new architectures and circuit techniques to address these challenges.

1.2. Organization

This dissertation consists of seven chapters.

Chapter 1 provides an introduction to trends in the wireless market, a review of the background of PLL-based frequency synthesizers, and an explanation of the motivation of this dissertation.

Chapter 2 presents the characteristics and key building blocks of PLL-based frequency synthesizers and describes the basic operation of PLL-based frequency synthesizers and DLL-based frequency multipliers.

Chapter 3 discusses three key challenges of fully integrated PLL-based frequency synthesizers: large area consumption of passive components, inherent reference spurious tones, and trade-offs between integer-N PLLs and fractional-N PLLs.

Chapter 4 presents techniques to address the problem of large area consumption of passive components in a PLL-based frequency multiplier. The chapter begins with a description of a compact ring oscillator that achieves both good phase noise performance and wide tuning range is described. Then a capacitor multiplier with a high multiplication factor for minimizing the area occupancy of the zero-making capacitor in the loop filter is presented. Finally, as an alternative to the PLL-based frequency synthesizer, a programmable delay-locked loop (DLL)-based frequency multiplier is introduced.

Chapter 5 introduces a new technique, the edge interpolation technique, for effectively suppressing spurious reference tones based on the charge distribution mechanism. The chapter details the charge distribution mechanism and implementation of the edge interpolator.

Chapter 6 presents a new PLL architecture to solve the trade-offs between integer-N PLLs and fractional-N PLLs. The sub-integer-N PLL realizes a high-frequency resolution using a single side-band (SSB) mixer and the mathematical concept of relatively prime without a fractional divider.

Chapter 7 concludes the dissertation.

CHAPTER 2

PLL-BASED FREQEUNCY SYNHESIZERS

2.1. Basic Characteristics

A PLL-based frequency synthesizer is one of the basic architectures for generating radio-frequency (RF) signals from a clean low-frequency clock. Figure 1 illustrates a general PLL architecture and its key building sub-blocks: a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LP), a voltage-controlled oscillator (VCO), and a programmable frequency divider. In a negative feedback system, the PFD in the loop detects differences in the phase frequency between the reference clock, f_{ref}, and the divided output signal from the VCO. The CP delivers this information to the VCO through the LF, and the VCO modulates the output signal, f_{out}, based on this information. Through repeated iterations of this operation, the difference in the phase/frequencies is sufficiently minimized. Finally, the PLL achieves the locked condition in steady-state, and the following equation holds:

$$f_{out} = \mathrm{N} \cdot f_{ref} . \tag{1}$$

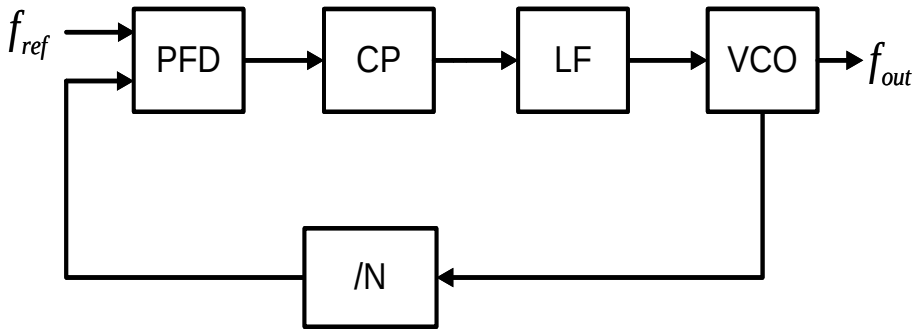


Figure 1. Block diagram of a basic PLL-based frequency synthesizer.

2.2. Key Building Blocks

2.2.1. Voltage-Controlled Oscillators

A VCO is one of the most essential parts of a PLL-based frequency synthesizer because it determines out-band phase noise performance and the frequency range of the overall system. However, the VCO creates a bottleneck that slows the system's ability to minimize the power and area consumption.

To modulate the output frequency, the VCO uses a frequency tuning circuit inside its positive feedback loop that amplifies the loop gain and sustains it as unity at the oscillating frequency. Despite the variety of configurations based on the frequency selection/tuning mechanism, oscillators can be simply classified into two categories: LC resonator oscillators and resonator-less oscillators. Because of the signal purity of LC resonators, they are the basis of many traditional VCOs. However, the difficulties in integrating on-chip inductors with LC resonators and their limited frequency-tuning range have raised problems in implementing a fully integrated PLL for wideband applications. By contrast, among several possible topologies of resonator-less oscillators, a ring oscillator is compact and has a wide frequency tuning range. Nevertheless, its poor phase noise performance compared to that of an LC oscillator has prevented its adoption in commercial products.

2.2.2. Phase Detector and Phase Frequency Detector

The basic function of a PD or a PFD is to detect the difference in the phase or the phase/frequency between two incoming signals—the reference clock and the divided VCO clock—and to deliver the information to the subsequent CP. PDs can be broadly classified into two topologies: the multiplier type and the sequential type. The multiplier-type PD

generates a DC error output as the average product of the reference clock and the divided VCO clock, which the sequential-type PD generates the output signal purely as a function of the time interval between two incoming clocks, so the sequential-type PD contains the memory of past transitions.

Among sequential-type PDs, the tri-state PFD is one of the most common topologies to be utilized with a CP, as in Figure 2. As its name implies, the tri-state PFD can take one of three states. When the phase and frequency differences between the reference clock and the divided VCO clock are detected, the tri-state PFD generates two output signals, the UP and the DN, to convey the information. By the rising edges of the reference clock, f_{ref}, and the divided VCO clock, f_{div}, the UP and the DN become 1 simultaneously.

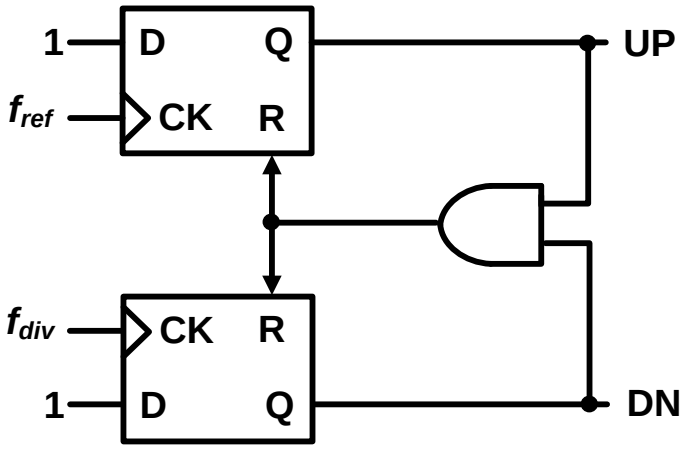


Figure 2. Block diagram of a tri-state PFD.

However, as soon as both the UP and the DN become 1, the AND gate resets both flip-flops, which causes the UP or the DN to obtain the phase/frequency difference information of the two input clocks, as shown in Figure 3.

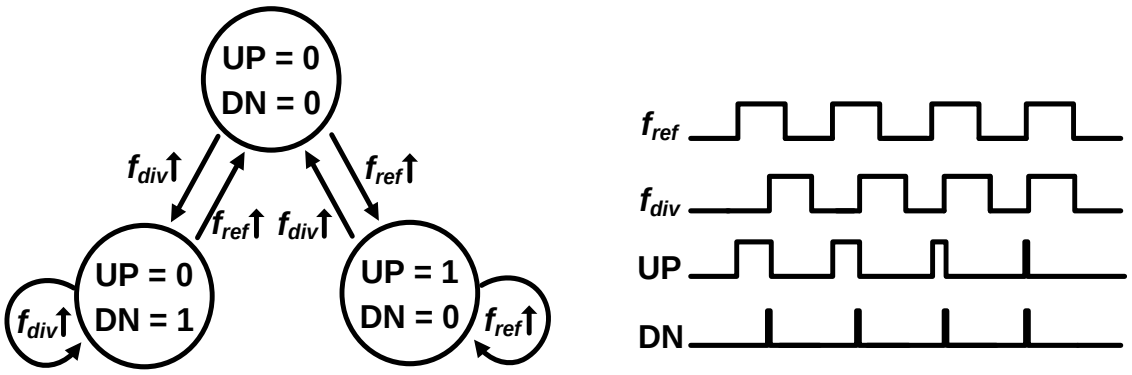


Figure 3. State machine and signal transitions of the tri-state PFD.

2.2.3. Charge Pump

The phase/frequency difference information conveyed in the pulse width of the output signals of the PFD should be converted into the form of DC voltage in order to modulate the output frequency of the VCO. Generally, this time-to-voltage conversion process takes place through the charge pump and the loop filter, as shown in Figure 4. First, the charge pump converts the pulse-modulated phase/frequency difference information into corresponding charges, and then these charges are translated to DC voltage by the loop filter.

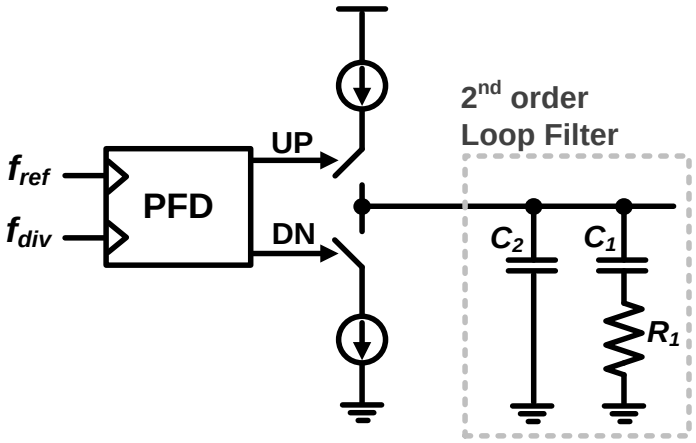


Figure 4. Block diagram of a charge-pump and 2nd-order loop filter.

Since functions of the tri-state PFD and the charge pump are closely coupled, an optimal design considers these two blocks as one unit. First, the dead-zone problem should be addressed so the in-band phase noise performance is not degraded. In the locked state, the phase error becomes almost zero, which makes the widths of the UP and the DN extremely narrow. When, in this situation, there is only a very small phase difference between the reference clock and the divided VCO clock, the PFD generates a very short pulse at the UP or the DN, but if this pulse is too short to open the charge-pump switch, the loop cannot track this small phase or frequency variation. This phenomenon leads to a small range in the input phase that is near the zero-phase error where the loop is inactive, which is called the dead zone. Fortunately, the dead-zone problem can be easily overcome by adding short delays to reset the signal paths and guarantee finite pulse widths of the UP and the DN so the charge pump can open even in the locked state. However, as these finite pulse widths become wider, other side effects caused by non-idealities of the charge pump become severe. The most critical problem is the reference spur. In the locked state, mismatched up/down currents of the charge pump flowing in this finite pulse duration evoke an unnecessary charging or discharging process in the loop filter that disturbs the control voltage of the VCO and increases the reference spur level in the VCO output signal.

2.2.4. Loop Filter

A loop filter establishes the desired PLL dynamics for the target application. The characteristics of the loop filter determine the performance of the PLL, such as the settling time, phase noise, and spur levels. To perform its basic function of decoding the information related to the amount of charge from the charge pump to the DC voltage level

of the VCO input, the loop filter must equip the shunt capacitor, C_1. However, with another pole at DC from the VCO itself, a loop filter that has only one shunt capacitor renders the PLL loop unstable. Therefore, to achieve loop stability, a practical loop filter involves one resistor, R_1, in series with the capacitor and, to suppress the levels of spurious tones, an additional parallel capacitor, C_2. The additional resistor and capacitor generate a lead-compensating zero, w_z, followed by another additional pole, w_p. The transfer function of a general second-order loop filter (Figure 5), which results in a third-order type-II PLL, can be expressed as

$$F(s) = \frac{1}{(C_1 + C_2) \cdot s} \cdot \frac{1 + s / w_z}{1 + s / w_p}, \qquad w_z = \frac{1}{R_1 C_1}, \; w_p = \frac{C_1 + C_2}{R_1 C_1 C_2}. \tag{2}$$

In some cases, one more RC stage can be added in series to suppress levels of spurious tones further; doing so increases the order of the loop filter and the PLL to third-order and fourth-order, respectively.

2.3. PLL-based Frequency Synthesizer Architectures

2.3.1. Integer-N PLL

Figure 1 shows the block diagram of an integer-N PLL synthesizer. The integer-N architecture is characterized by an integer modulus divider that remains constant during steady-state operation. Since the division ratio of the divider is restricted to an integer value, the frequency resolution of the frequency synthesizer is determined by the reference clock frequency, f_{ref}. Here, the trade-off between the frequency resolution and the settling time

increases. To guarantee stability, the loop bandwidth of the PLL should be less than one-tenth of f_{ref} [1]; this narrow loop bandwidth imposes a restriction on the settling time, which is inversely proportional to the loop bandwidth. In addition, to achieve a fine frequency resolution, f_{ref} should be extremely low. Thus, to generate the target RF frequency as a PLL output frequency, the division ratio must be relatively large, which degrades in-band phase noise performance. However, if requirements from the target application are not strict, the integer-N PLL architecture is typically the best solution because of its simplicity and the small number of spurious tones.

2.3.2. Fractional-N PLL

The beauty of fractional-N PLL architectures is that, by adopting a time-varying fractional divider, they eliminate the trade-off between the frequency resolution and the settling time of integer-N counterparts [2]. In this architecture, since the frequency resolution is not determined by f_{ref}, the loop bandwidth and f_{ref} can be increased arbitrarily, which accelerates the lock-acquisition process and reduces the settling time of the PLL. In addition, in-band phase noise performance can be enhanced since a high-frequency reference clock decreases the division ratio of the divider. The fractional division ratio is provided as a time-average value of several integer numbers. This operation can be implemented using a digital accumulator but, because of the periodic nature of toggling different integer numbers to generate the target fractional value, new spurious tones, called fractional spurs, are introduced at fractions of the reference clock frequency. Whereas in fractional-N PLL architectures the reference spur is far above the loop bandwidth,

fractional spurs fall well within the loop bandwidth, so they must be suppressed by compensation circuits or dithering techniques.

Among the various fractional-N PLL architectures for suppressing fractional spurs, the most successful so far is the ΔΣ fractional-N PLL, which adopts a ΔΣ modulator that randomizes the conventional periodic operation on fractional division (Figure 5).

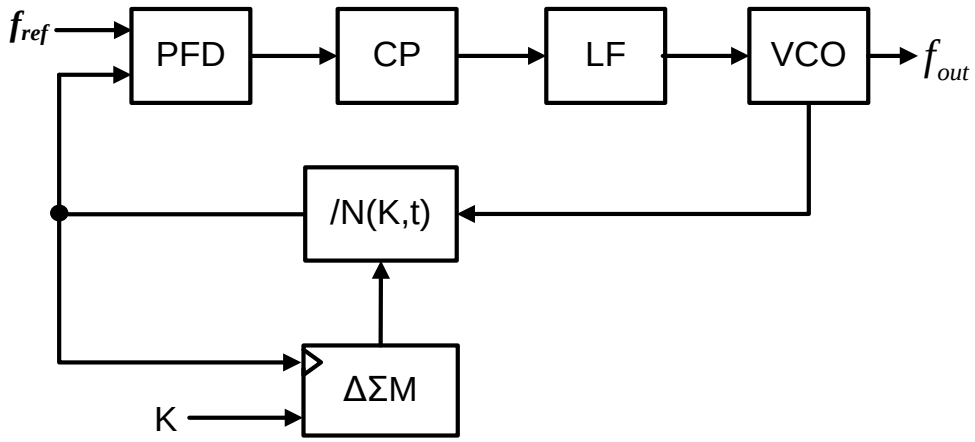


Figure 5. Block diagram of a ΔΣ fractional-N PLL.

The ΔΣ modulator provides a precise fractional part between 0 and 1, and its pseudo-random dithering nature pushes its quantization error or noise, which causes fractional spurs, far away from the PLL output frequency. The noise-shaping characteristics of the ΔΣ modulator are determined by the order and type of the modulator. The MASH-type modulator has been one of the most popular architectures because of its straightforward and unconditionally stable operation.

However, despite the popularity of fractional-N PLLs, fractional spurs and quantization errors from the modulator remain problematic. Limited cycles, inherent in the operation of the modulator, introduce fractional spurs when the fractional division ratio is a rational

fraction of the reference clock frequency [3]. In addition, the high-frequency quantization noise, shaped by the ΔΣ modulator, tends to be folded into the in-band range by nonlinearities of building blocks such as the PFD and the CP.

2.3.3. Offset-Frequency PLL

Another approach to eliminating the trade-off of an integer-N PLL is an offset-frequency PLL architecture, shown in Figure 6. Offset-frequency PLL architectures are implemented by mixing a signal with high operating frequency from the main PLL with a signal with a high-frequency resolution, or offset-frequency signal, f_{mix}.

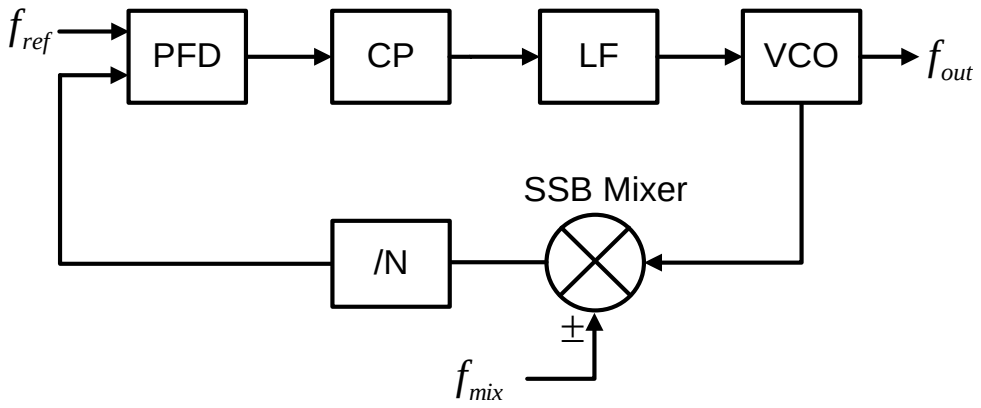


Figure 6. Block diagram of an offset-frequency PLL.

An offset-frequency PLL frequency synthesizer can be designed in various architectures according to how the high-frequency resolution signal is generated. A dual-loop PLL frequency synthesizer, one of the most popular architectures, adopts an additional PLL loop to generate the offset-frequency signal. Alternatively, in a hybrid PLL-direct digital

frequency synthesizer (DDFS) architecture, memory circuits such as a RAM and a ROM synthesize a high-resolution offset-frequency signal.

Despite its ability to remove the trade-off between the frequency resolution and the settling time of the integer-N PLL, each offset-frequency PLL architecture has disadvantages. Dual-loop architectures require multiple PLL loops and additional reference sources, which considerably increase power consumption, cost, and chip area [4]-[6]. In addition, they cannot reduce the overall settling time, which is defined by a narrower loop-PLL that determines the frequency resolution. For their part, the hybrid PLL-DFSS architectures of [7], [8] incur large power and area consumption because of their use of memory circuits in designing the DDFS.

2.4. DLL-based Frequency Multiplier

As a close relative of a PLL, a delay-locked loop (DLL) replaces the VCO of a PLL with a voltage-controlled delay line (VCDL) consisting of cascaded N-delay cell stages. When the periodic reference clock with the period of T_{ref} comes, the VCDL delays the incoming clock by one cycle, or T_{ref}. Then, the loop aligns the reference clock and the one-cycle delayed clock, which results in the locked state. In the locked state, each delay cell stage provides an evenly-spaced delay edge. The output signal, which has a multiplied output frequency, can be achieved by combining these edges from the cascaded N-delay cell stages.

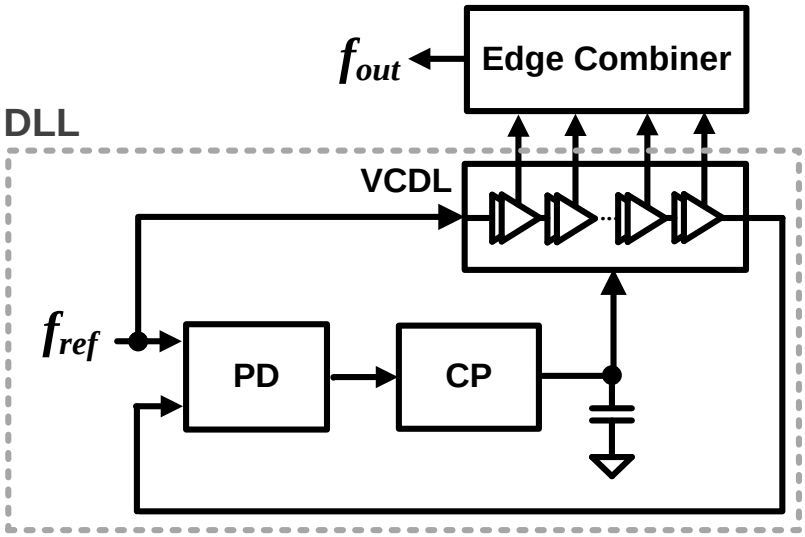


Figure 7. Diagram of the DLL-based frequency multiplier.

Compared to a PLL, the DLL-based frequency multiplier shown in Figure 7 has four strong advantages [9]-[12]. First, a VCDL typically introduces much less phase noise or jitter than an oscillator. As shown in Figure 8, while the oscillator keeps accumulating jitter in a PLL, an edge is refreshed from the reference clock at the end of the VCDL in a DLL.

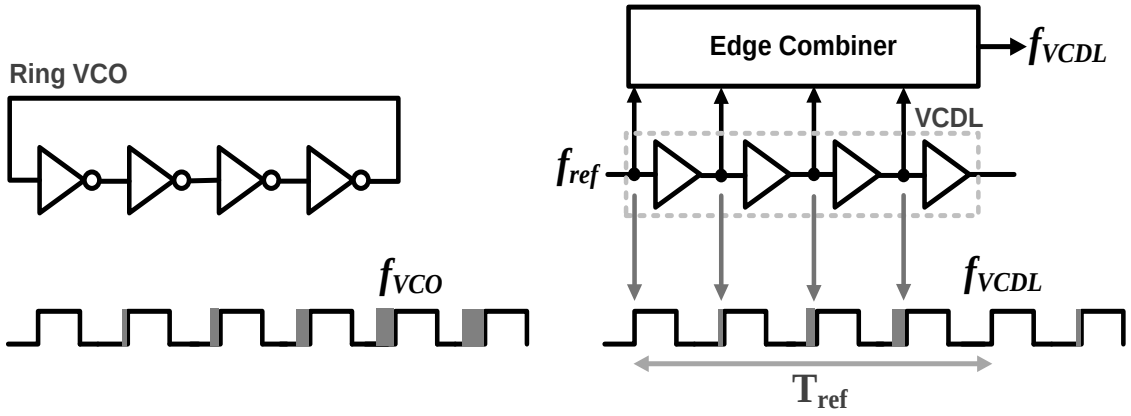


Figure 8. Comparison of the jitter, or phase noise performance of a PLL and a DLL-based frequency multiplier.

Thus, in a DLL, jitter is not accumulated from cycle to cycle. Second, since a DLL does not have an intrinsic pole from the oscillator of a PLL, just one shunt capacitor in the loop filter can achieve stability, so the loop filter becomes simple and compact. Third, because of its absolutely stable characteristics, there is no restriction on the capacitor in the loop filter, so using a relatively small capacitor allows the settling time to be decreased significantly. Finally, a general DLL occupies small chip area without an LC VCO or a bulky loop filter.

CHAPTER 3

CHALLENGES OF FULLY INTEGERATED PLL FREQUENCY SYNTHESIZERS

3.1. Large Area Consumption of Passive Components

A great deal of effort by academia, industry, and worldwide research organizations has brought in aggressive and steady technology scaling of CMOS technologies. This scaling trend was fueled by the demand for digital computation and memory, and the technology has primarily evolved to serve these markets.

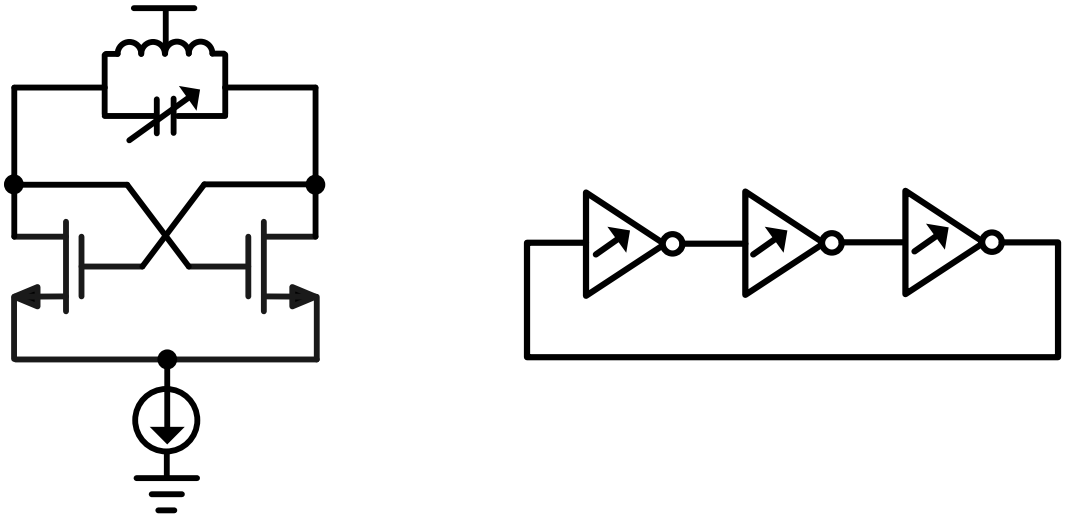
For area, cost, and power reductions, this trend, starting from the digital circuitry, strongly requires RF/analog circuitry to be integrated in a scaled-down CMOS technology toward the ultimate goal of full integration: both the complete transceiver system on a single chip and the RF/analog front-end and the digital modulator/demodulator on the same die.

Full integration of a frequency synthesizer is one bottleneck in this trend, since its large passive components do not have the advantages of the scaling-down of CMOS technologies [13]. General PLL architectures contain high-frequency building blocks, such as the voltage-controlled oscillator (VCO) and the prescaler, as well as low-frequency filters and other circuitry. Each block poses major design challenges and mostly requires external components. Although some of the presented transceivers incorporate the VCO active circuitry on the die, they all need an external inductance–capacitance (LC) tank to

achieve the required phase-noise specification. In addition, the large time constant required for the loop filter generally leads to the large zero-making capacitor.

3.1.1. LC VCO vs. Ring VCO

In general, VCOs can be classified into two types, as shown in Figure 9.



(a) **(b)**

Figure 9. Conceptual topologies of VCOs (a) LC VCO (b) Ring VCO.

Considering its small chip area consumption and scalability, a ring VCO is a good alternate to replace an LC VCO. Figure 10 compares the characteristics of an LC VCO and a ring VCO. Traditionally, because of the good phase noise performance, the LC VCO has overwhelmed its counterpart, a ring VCO, in commercial use [14]. However, to adopt an inductor with a high quality factor in the LC resonant tank, the large area consumption is inevitable. Furthermore, since the inductance value is related to a physical area of the

inductor, the LC VCO will take relatively more chip area in future deep-sub micron CMOS technologies.

	LC VCO	Ring VCO
Phase Noise	Good	Moderate
Tuning Range	Moderate	Wide
Chip Area	Large	Small
Scalability	Bad	Good
Multi. Phases	Additional ckt.	Available

Figure 10. Comparison of the characteristics of LC VCOs and ring VCOs.

By contrast, a ring VCO has a proper architecture to be integrated in deep-sub micron processes since it requires a smaller chip area as CMOS processes are scaled down.

Without compensation techniques, the tuning range of the LC-VCO is restricted to only 10% - 20 %, which is inappropriate for wideband applications as well as vulnerable to process variations. However, a ring VCO is capable of generating wide-range frequency signals for applications requiring wideband operation. Also, a ring VCO can naturally provide multiple phases to systems, while in a LC VCO, additional circuits such as I/Q generators make the circuit complicated [15]. Therefore, research on a ring VCO, equipped with both enhanced phase noise performance and wide-tuning capability, is one of the key challenges to implement a wideband fully-integrated PLL-based frequency synthesizer.

3.1.2. Large Capacitors in the Loop Filter

With the inductor in an LC-VCO, another obstacle to prevent full-integration of conventional PLL-based frequency synthesizers is a capacitor in the loop filter. Figure 11 shows two of the most popular passive loop filters utilized in the PLL, a 2nd order and a 3rd order. For more suppression of the reference spur, a 3rd order loop filter adopts one more pole using one more RC low pass stage consisting of R_2 and C_3.

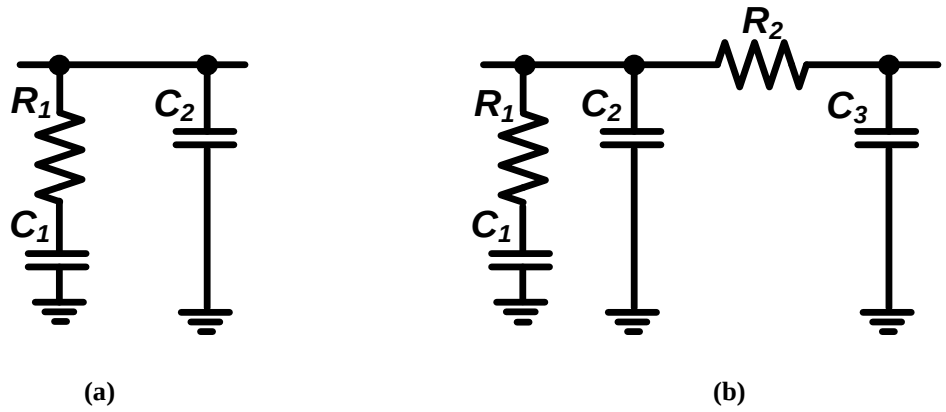


Figure 11. Passive loop filters in PLLs (a) 2nd order (b) 3rd order.

However, since $C_1 >> C_2$, C_3 and $R_1 >> R_2$, locations of the zero, the first pole, and the second pole are almost equal in two loop filters. Following are the locations of the zero and poles in loop filters.

$$w_{p1} = 0$$
$$w_{p2} = \frac{1}{R_1(C_2 + C_3)}$$
$$w_{p3} = \frac{C_2 + C_3}{R_3 C_2 C_3}$$
$$w_z = \frac{1}{R_1 C_1} \qquad (3)$$

The 3-dB loop bandwidth of the PLL, which is equal to its open-loop unity gain frequency, w_u, must be placed between w_z and w_{p2} to guarantee a reasonable phase margin for the loop stability. When assuming $w_u = \sqrt{w_{p2} \cdot w_z}$ and $w_{p3} >> w_{p2}$, the phase margin yields the following.

$$\phi_m \approx \arctan\left(\sqrt{\frac{w_{p2}}{w_z}}\right) - \arctan\left(\sqrt{\frac{w_z}{w_{p2}}}\right) \tag{4}$$

As discussed earlier, the 3-dB loop bandwidth of the PLL, w_u, should be ten-times less than the reference clock frequency for stability. In fractional-N architectures, this bandwidth limitation by the reference clock frequency is loosened compared to that in integer-N architectures. However, a reasonable level of phase noise and spurious tone suppression prevent a fractional-N PLL from arbitrarily expanding its loop bandwidth.

With this restricted bandwidth, values of passive components in the loop-filter become unbearably large [16]. In particular, capacitance of the zero-making capacitor, C_1, causes a practical problem. Figure 12 shows an example of the 2nd order loop-filter design. In the design, the zero-making capacitor has capacitance of 516.8 pF, which consumes a large area of silicon real-estate.

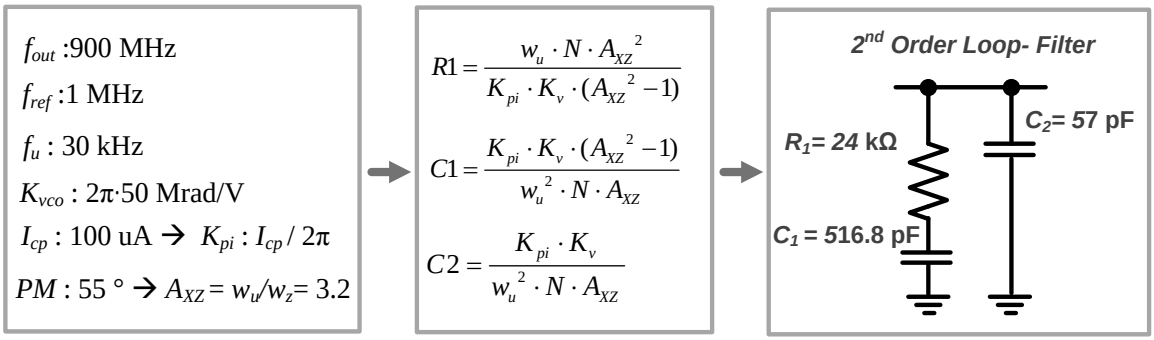


Figure 12. Design example of a 2nd order loop filter.

3.2. Reference Spurious Tones

In charge-pump PLL frequency synthesizers, the reference spur problem is an inherent and fundamental issue. As discussed earlier, in the locked state, non-idealities of a PFD and up/down current mismatch of a charge pump evoke periodic charging or discharging process as in the loop filter. As in Figure 13, this periodically disturbs the control voltage of the VCO, which results in the presence of the spurious tone at the reference clock frequency far from the VCO output frequency.

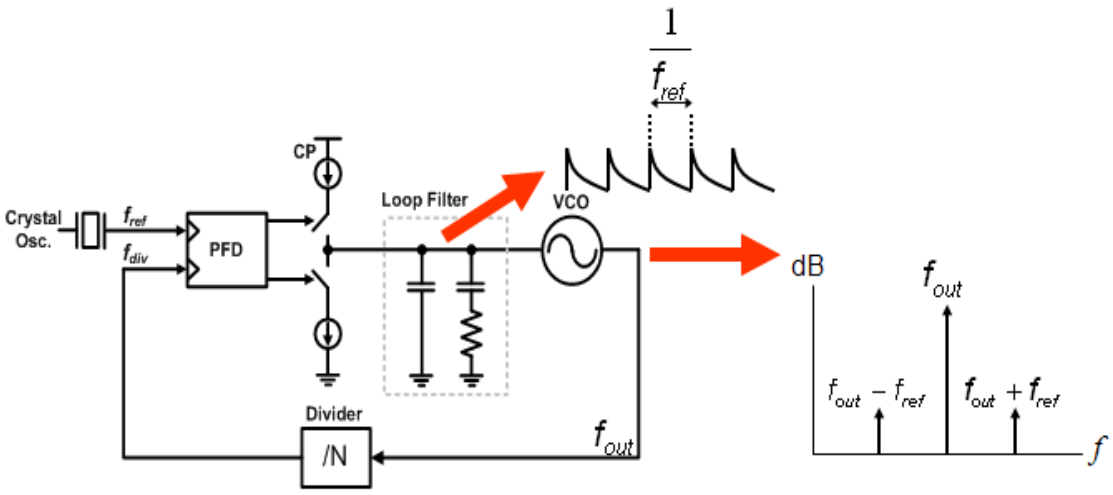


Figure 13. Spurious tone in PLL frequency synthesizers.

These large spurs and their harmonics are mixed with the signals from adjacent channels, degrading performance of wireless transceivers [17]. Moreover, recently, as wireless communication applications are required to cover wide frequency bands, the issue of reference spurs becomes more critical.

3.3. Trade-offs between Integer-N PLLs and Fractional-N PLLs

Obviously, trade-offs exist between integer-N PLLs and fractional-N PLLs [18], as shown in Figure 14. Integer-*N* PLLs have the advantages of their simple structures and ideally few spurs, but the large division factor impairs in-band phase noise performance for high-frequency resolution. In addition, since the loop bandwidth is limited to less than one tenth of the reference frequency for stability [1], phase noise from the voltage-controlled oscillator (VCO) cannot be suppressed enough by a loop filter, and the settling time increases. Fractional-*N* PLLs, by contrast, partially solve those problems of integer-*N* PLLs by removing the dependency on the reference frequency of the output frequency resolution, but fractional spur reduction or dithering techniques such as a delta- sigma (ΔΣ) modulation considerably increase system complexity.

	Integer-N	Fractional-N
Freq. Resolution	Low	High
Loop Bandwidth	Narrow	Wide
Settling Time	Slow	Fast
Spurious Tones	Good	Moderate
Complexity	Low	High

Figure 14. Comparison of the characteristics of integer-N PLLs and fractional-N PLLs.

For certain applications, the channel resolution is not so tight that a fractional-*N* PLL employing a ΔΣ modulation scheme is necessary. However, it is still desirable to achieve a

fractional frequency resolution while maintaining a wide loop bandwidth. To satisfy this requirement, research on a new architecture to take advantage of both conventional architectures is required.

CHAPTER 4

TECHNIQUES FOR MINIMIZING AREA OF FREQUENCY SYNTHESIZERS

4.1. A Low Phase Noise Ring VCO with Wide and Linear Tuning Characteristics

4.1.1. Introduction

In this research, a monolithic ring VCO is described. To improve the poor phase noise performance common in ring VCOs, a saturated-type delay cell was adopted [15, 19]. In [19], a ring VCO based on the saturated-type differential delay cell with a positive feedback path was introduced, whose phase noise performance is comparable to LC-VCOs. However, the oscillator of [19] has disadvantages due to its frequency-tuning mechanism, changing the strength of the latch in the positive feedback path. Since the strength of the latch is not proportional to the control voltage, the oscillator cannot have a linear frequency-voltage characteristic. Furthermore, the oscillator does not have a wide frequency-turning capability, especially in the relatively low frequency band, such as VHF TV bands covering from 30 MHz. Thus, to obtain a linear frequency-voltage characteristic with a wide tuning range, a transmission gate was utilized as a frequency-tuning method [20, 21]. In [20], the delay cell consists of three stacks of transistors, which is not suitable for the circuits operating under low supply voltage. In the proposed design, the headroom problem was overcome by moving a transmission gate to the node between two adjacent delay cells.

4.1.2. Low Phase Noise Design

To enhance the phase noise performance of a ring VCO, the proposed ring VCO adopts the saturated type delay cell of [19] with a cross-coupled latch. Thus, the delay cell eliminates the tail current source and has pseudo-differential configuration using a PMOS cross-coupled latch. As a saturated-type VCO, the delay cell allows a rail-to-rail output signal swing. In addition, the cross-coupled latch accelerates the signal and provides fast-switching edges. When the signal is injected, the latch operates in the direction of opposing the signal transition in the PMOSs. However, after a while, the function of the latch changes into a positive feedback and accelerates the signal transition. With the rail-to-rail swing signal with fast-switching transition, the proposed oscillator can enhance phase noise performance compared to conventional ones.

Qualitatively, the more time transistors are turned-on, the more thermal noise current is generated from those devices as in Figure 15.

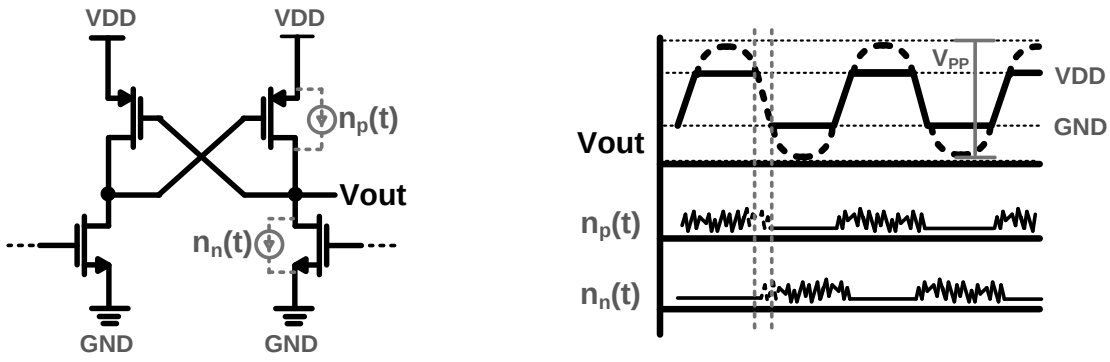


Figure 15. Effect of thermal noise on a saturated-type delay cell in a ring VCO.

The full-switching signal turns off either of PMOSs or NMOSs in the delay cell, as well as the fast-switching signal transition decreases the duration of both of PMOSs and

NMOSs are simultaneously turned on. Therefore, the fast-switching transition and the rail-to-rail swing imply shorter duration for transistors being turned-on, which intrinsically improves phase noise performance [15], [19], [20].

In addition, the elimination of the tail transistor reduces 1/f noise which is mainly contributed by bias devices, [22], [23]. This also can be explained by the phase noise analysis of ring oscillators [10]:

$$L(\Delta\omega) = \frac{512F \cdot kT \cdot R \cdot V_{DD}}{27\pi \cdot V_{PP}{}^3} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \quad , V_{PP} = 2\frac{SR_{\max}}{\omega_o}, \tag{5}$$

where F, $SR_{\max}$, $\Delta\omega$, ω_o, kT, V_{DD} and R are the excess noise factor, the maximum output slew rate, the angular frequency offset from the center frequency, the center frequency, the thermal energy, the power supply voltage and the equivalent output resistance of a delay cell, respectively. In (5), the increase of the maximum slew rate of the signal and V_{pp} due to the fast rail-to-rail signal transition of the proposed delay cell reduces phase noise. Therefore, (5) confirms that the adoption of a latch improves the phase noise performance of the delay cell even when utilized with a long delay-making mechanism.

4.1.3. Wide and Linear Frequency Tuning Design

One of the most important requirements of a VCO is the tuning range because it determines the operating frequency range of PLLs. Several conventional methods for achieving a wide range in ring VCOs are; changing the loading capacitor, the number of stages, or the driving capability. However, each technique has inherent disadvantages. First, when changing the loading capacitor, a large chip area is required to integrate multiple

capacitors. Second, the change of the number of delay cell stages takes much power consumption as well as large chip area. Last, changing the driving capability makes the VCO's frequency-voltage characteristic nonlinear. Hence, the approach to control the output resistance of the delay cell can be a good alternative. Figure 16 presents a simple small-signal model for the delay cell with a voltage-controlled resistor. Using this model, the oscillation frequency f_{osc} is represented as

$$f_{osc} = \frac{1}{2 \cdot N \cdot \tau} \approx \frac{1}{2 \cdot N \cdot C_1 \cdot (R + \frac{1}{G_m})}$$
$$\approx \frac{1}{2 \cdot N \cdot C_1 \cdot R} \quad (\textit{for } C_2 << C_1, \quad 1 << G_m \cdot R), \qquad (6)$$

where N is the number of stages, τ is the delay time in one stage, m G is trans- conductance of the delay cell, and R is voltage-controlled resistance. From (6), it is clear that linear and wide output frequency tuning is possible if a resistance change is large and inversely proportional to the control voltage change.

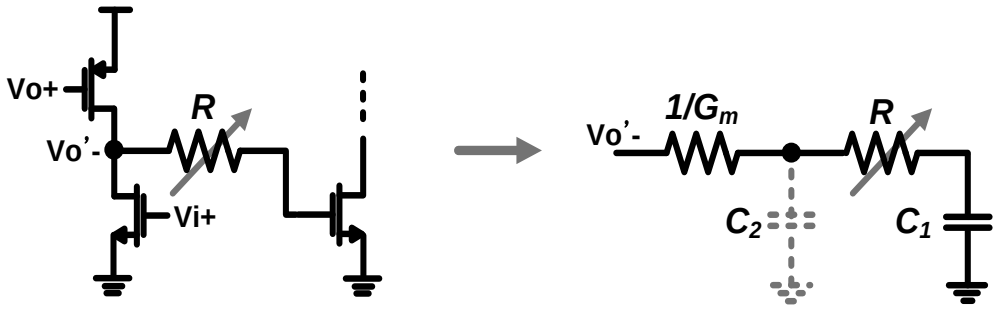


Figure 16. Simple small-signal model for the delay cell.

Recently, the transmission gate has gained attentions as the preferred implementation of a voltage-controllable resistor due to its wide resistance-tuning range. However, since

voltage transmission through the transmission gate is a nonlinear process, and its transistors operate in the saturation and triode regions periodically, it is not straightforward to determine its equivalent resistance. Therefore, to extract the equivalent resistance from this nonlinear operation, an indirect but simple method is adopted [20]. In Figure 17, if a steep rising unit step signal is injected into one end of the transmission gate, a time-delayed signal would appear at the other end, which is connected to a capacitor large enough compared to parasitic capacitance.

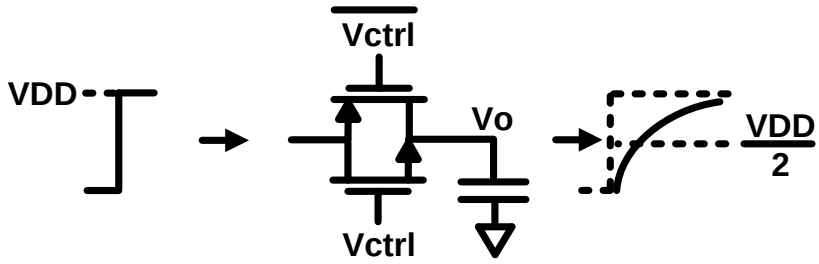


Figure 17. Model for effective resistance of the transmission gate.

Assuming this process has a first-order time constant model and measuring the delay time, t_d, for the output signal to reach half of the injected signal level, the effective resistance is obtained as

$$R_{eff} = \frac{t_d}{C_L \cdot \ln(2)} . \tag{7}$$

To understand the physical operation of the transmission gate, a mathematical analysis was performed. Since the square law model of the conventional Shockley device model cannot reproduce the voltage-current characteristics of contemporary short-channel MOSFETs, the alpha-power law was utilized, wherein the saturated drain current is

proportional to the alpha-power of the overdrive voltage (V_{GS}-V_T) [24]. The analytic effective resistance can be obtained based on the simple equation as

$$R_{eff} = \frac{1}{G_{eff}} = avg\left(\frac{V_{DD} - V_O}{I_D}\right). \quad (8)$$

where G_{eff} is the effective conductance of the transmission gate, and I_D is current flowing through the transmission gate. However, while the transmission gate is conducting, V_O and I_D keep changing. Thus, the effective resistance and the effective conductance should be calculated based on its probability distribution. First, if the control voltage, V_{ctrl} , is below threshold voltage, both transistors are turned off, and G_{eff} can be regarded as zero. In the above-threshold region, after a fast-rising unit step signal is injected into the transmission gate, the output voltage increases gradually from zero to V_{DD} . Within the output voltage transition, the operating point of the PMOS device moves from the saturation region to the triode region while the NMOS device stays in the saturation region until turned-off. When the sum of V_{ctrl} and V_{ctrl} is always equal to V_{DD} , an approximated value of the effective conductance can be obtained by averaging the conductance of each transistor at every moment as

$$\begin{aligned} G_{eff} &= avg\,(\,G\,(V_O)\,) \\ &= \frac{I_{D0}V_{DD}}{2}\left\{\ln 2\cdot\left(\frac{V_{ctrl}-V_{TH}}{V_{DD}-V_{TH}}\right)^{\alpha p} + \frac{\left((V_{ctrl}-V_{TH})+(V_{DD}-V_{ctrl}+V_{TH})\cdot\ln\left(1-\frac{V_{ctrl}-V_{TH}}{V_{DD}}\right)\right)}{(V_{DD}-V_{TH})^{\alpha n}}\right\}, \quad (9) \\ &(\ for\ V_{TH} < V_{ctrl} < V_{DD}) \end{aligned}$$

where I_{D0} is the current drivability index (the current at $|V_{GS}| = |V_{DS}| = V_{DD}$), and α^p and α^n are alpha-power coefficients for PMOS and NMOS, respectively.

If both α^p and α^n are set to unity, the V_{ctrl} - G_{eff} curve of (9) closely matches that of the effective resistance equation in [20]. For more accurate calculation, however, α value should be evaluated for specific process. The alpha-power coefficient depends on the channel length of a transistor, and α is given by the following equation [24];

$$\alpha = \frac{\log(I_{D1} / I_{D2})}{\log((V_{G1} - V_{TH}) / (V_{G2} - V_{TH}))}, \tag{10}$$

where (V_{G1}, I_{D1}) and (V_{G2}, I_{D2}) are two different points on the V_{GS} - I_D curve. According to (10), α^p and α^n are extracted as 1.45 and 1.2 for a gate length of 0.18μm. Figure 18 compares the effective resistance and the effective conductance.

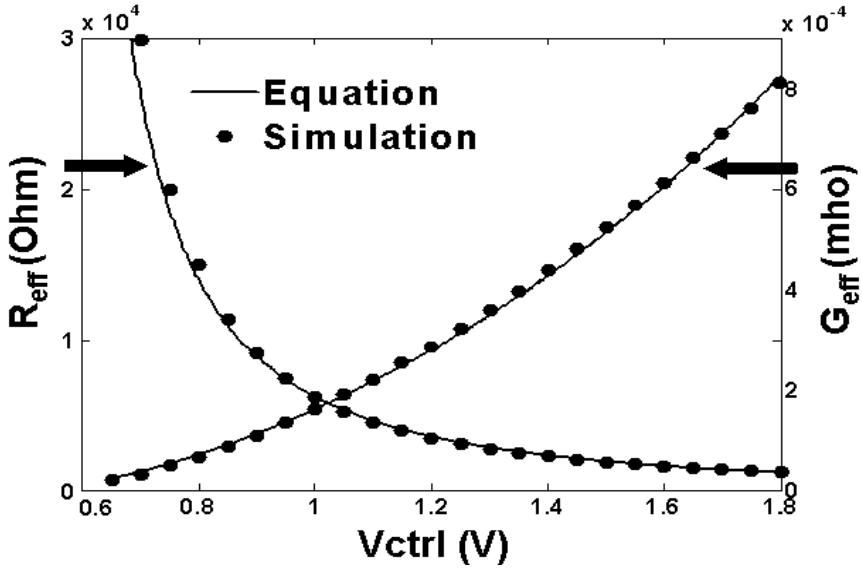


Figure 18. Effective resistance and conductance of the transmission gate from simulation and equation.

Effective resistance and conductance of the transmission gate from simulation and equation the above equation with those from a Spectre simulation. As shown, the conductance of the transmission gate changes linearly from an extremely small value to a large value proportional to the control voltage. This result confirms that the transmission gate is suitable for a delay cell in a VCO which requires wide and linear tuning characteristics. Furthermore, because the alpha-power coefficient decreases as the minimum channel length is reduced, G_{eff} becomes a more linear function of the control voltage in (9). Therefore, the transmission gate can be considered a more desirable candidate of voltage-controlled resistors for future CMOS process.

4.1.4. Schematics of the Ring VCO and the Delay Cell

The schematics of the proposed saturated-type delay cell adopting transmission gates and the 4-stage ring oscillator are shown in Figure 19.

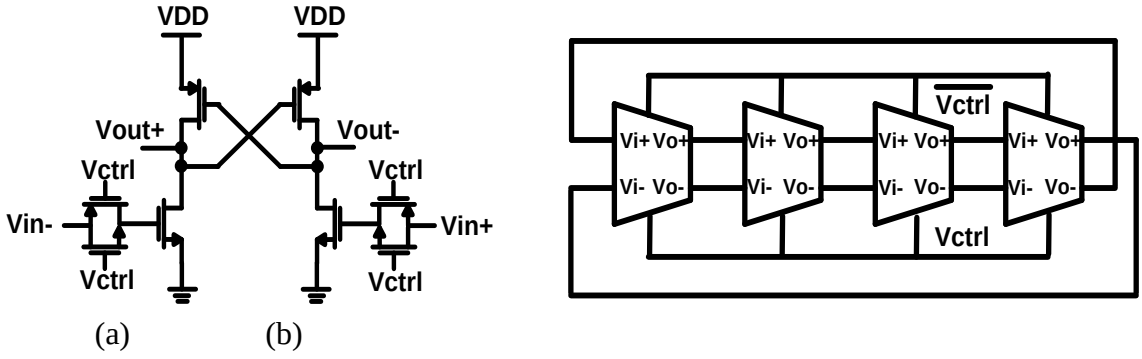


Figure 19. Schematics of (a) proposed delay cell (b) 4-stage ring oscillator.

Since the phase noise of the VCO is affected by the number of active devices, the delay cell was designed in a simple and straightforward manner. The delay cell consists of one NMOS input pair, one PMOS positive feedback pair and one transmission gate which

connects the output of one delay cell to the input of the next one. The whole ring oscillator is made of 4-stage delay cells considering the trade-off between the frequency tuning range, phase noise and power consumption. Thus, the VCO can provide eight different phases including quadrature signals.

4.1.5. Measurement Results

The stand-alone ring VCO was fabricated in a TSMC 0.18-μm CMOS process, and 2-V power supply voltage was used. By adopting a transmission gate for the saturated-type oscillator, a wide and linear frequency tuning range was achieved while maintaining good phase noise performance. In Figure 20, the fabricated ring oscillator exhibits a linear frequency-voltage characteristic with a wide tuning range from 20 MHz to 807 MHz, which closely matches the simulation results. Due to the linear tuning characteristic, the voltage gain of the oscillator is fairly constant. As discussed earlier, the effective conductance of the transmission gate is very small when the gate control voltage is near the threshold voltage and increases in proportion to the gate control voltage. Thus, output frequency linearly increases as the control voltage increases. The single sideband phase noise is shown in Figure 21. The measured phase noise is -113.5 dBc/Hz at 1-MHz offset from 800 MHz output frequency. In Figure 22, in-phase and quadrature-phase output signals are presented at different frequencies of 800, 600, 200 and 55 MHz, respectively. As an advantage inherent in thering-type topology, accurately matched quadrature output signals were obtained without an additional circuit.

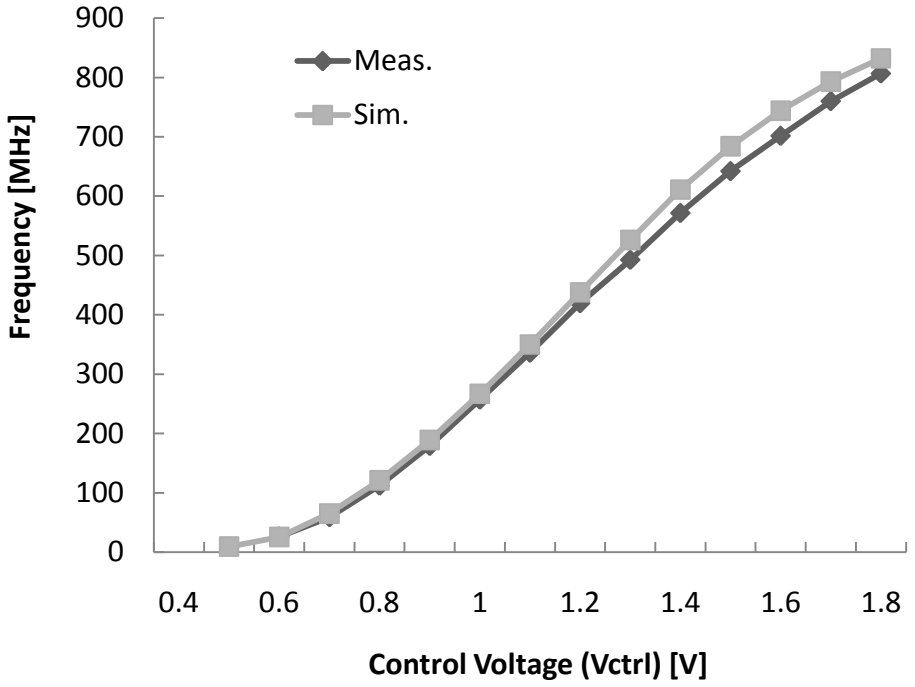


Figure 20. Frequency tuning range of the output signal

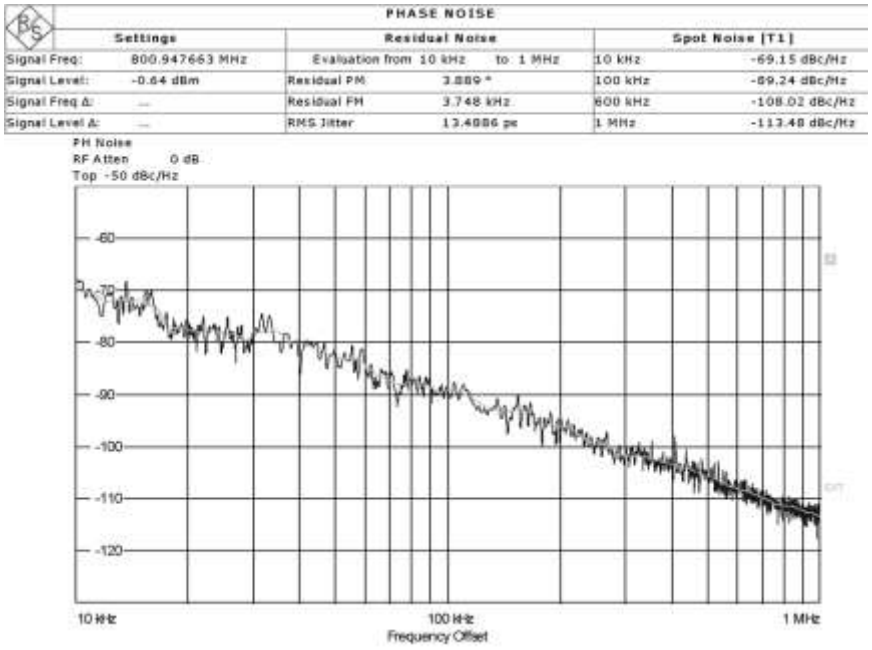


Figure 21. SSB phase noise performance when the 633 MHz output signal is generated

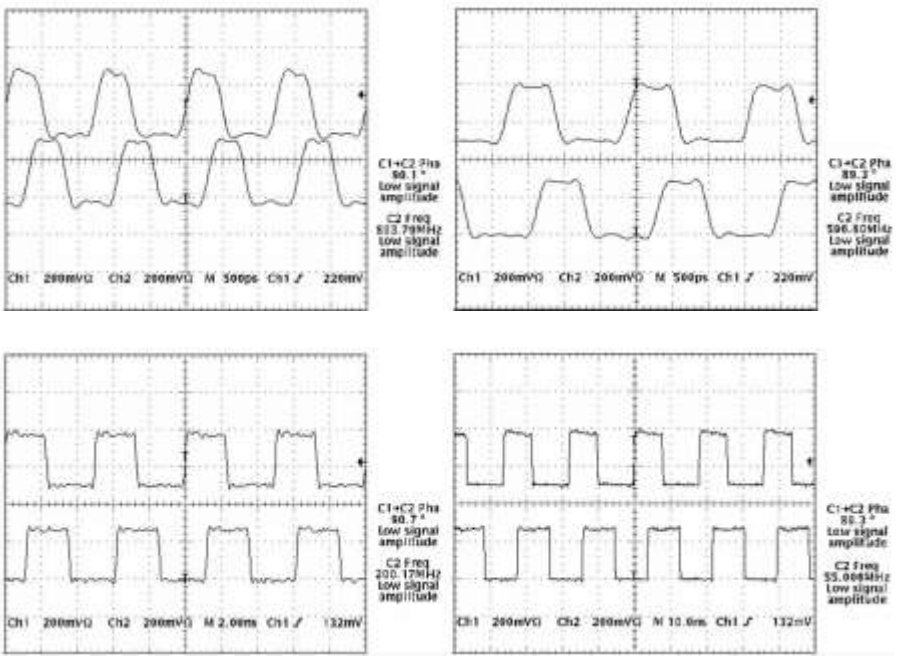


Figure 22. Waveforms of the output signal

Figure 23 shows the die photograph of the proposed ring VCO. The chip area is 60 μm × 51 μm for the core circuit and 167 μm × 124μm with output buffers.

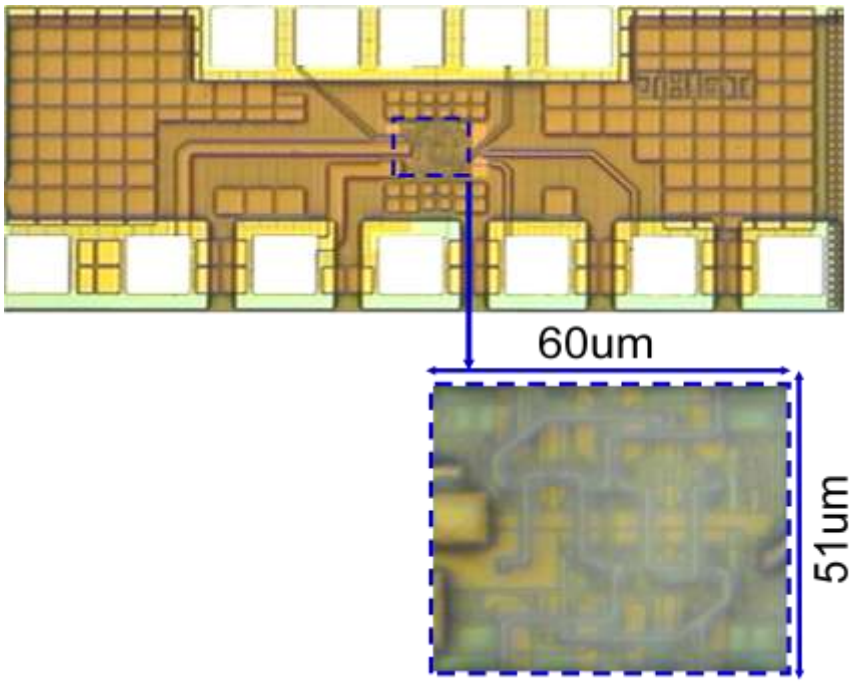


Figure 23. Die photograph of the proposed ring VCO

4.1.6. Conclusions

A novel saturated-type ring VCO based on a transmission gate was proposed, and the resistance tuning capability of the transmission gate was analyzed. By adopting the transmission gate for delay cells in a saturated-type oscillator, a wide and linear frequency tuning range was achieved while maintaining a fairly good phase noise performance. Figure 24 compare the performance of the frequency tuning range and phase noise of the proposed VCO with prior arts, which shows the proposed VCO achieves both a wide frequency tuning range and the good phase noise performance.

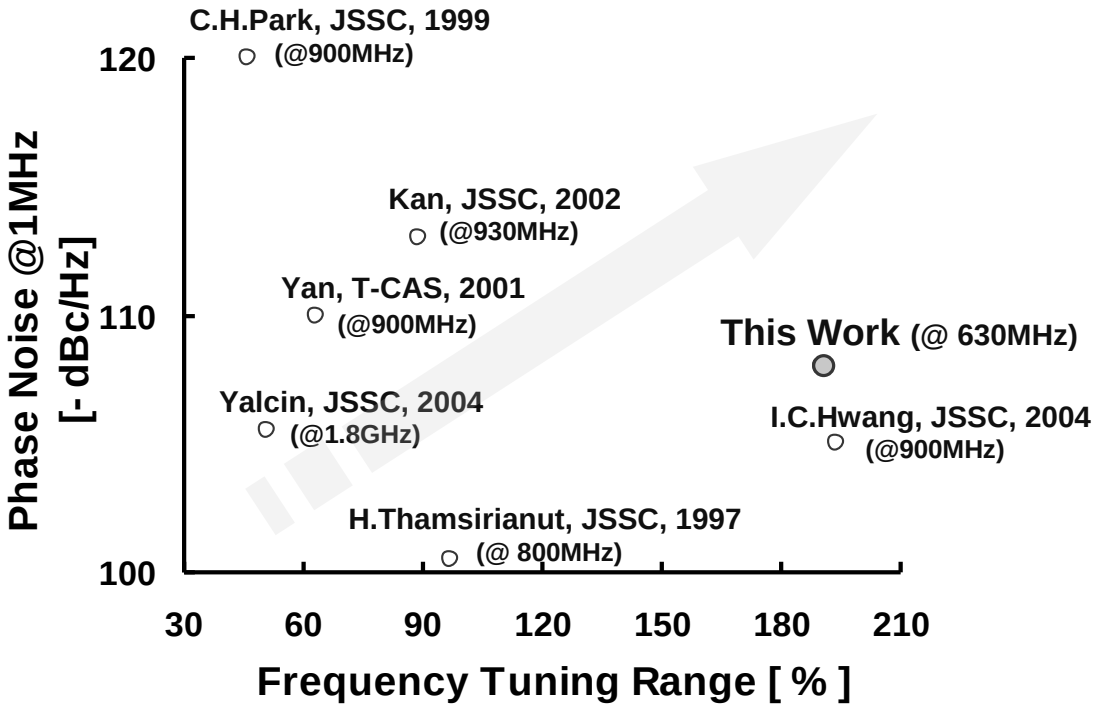


Figure 24. Comparison with prior arts on phase noise- frequency tuning range performance.

The use of this simple delay cell topology eliminated the need for current biasing and enables the VCO to operate under a low power supply voltage. In addition, essential

features for the system, such as a small chip area and accurate I/Q phase output signals, were obtained without additional circuits. The operating frequency range from 20 MHz to 807 MHz is wide enough to cover TV channel bands for the Cognitive Radio spectrum sensing system.

4.2. High Multiplication Factor Capacitor Multiplier for a Loop Filter

4.2.1. Introduction

Figure 25 shows a design example of an 3rd order integer-N PLL with a 1 MHz reference frequency. From the design parameters, the values of the passive components in the loop filter can be obtained. In this design, the problem is the zero-making capacitor of 516.8 pF, which takes more than 700 μm by 700 μm when using MIMCAP.

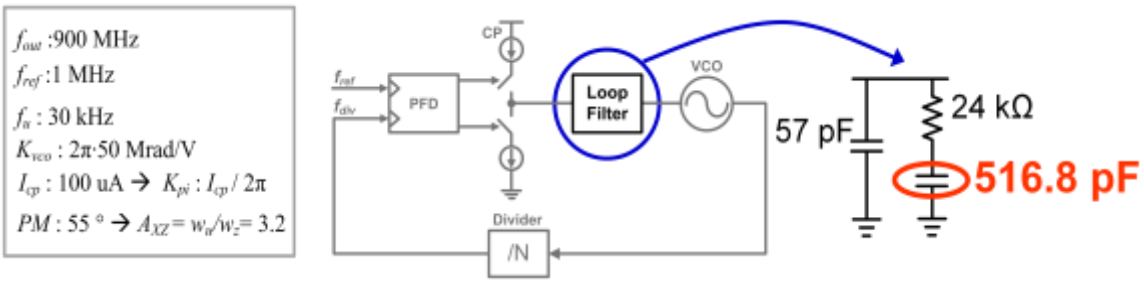


Figure 25. Design example of an 3rd order integer-N PLL with a 1 MHz reference frequency.

In order to minimize the physical area of an on-chip capacitor, various capacitor multiplication techniques have been introduced in voltage or current mode [25-28], as shown Figure 26. First, in the voltage mode topology using the Miller effect, the multiplication factor is practically limited to less than three [25]. Second, a current mode

topology, however, has demonstrated the possibility of achieving a higher multiplication factor [26-28].

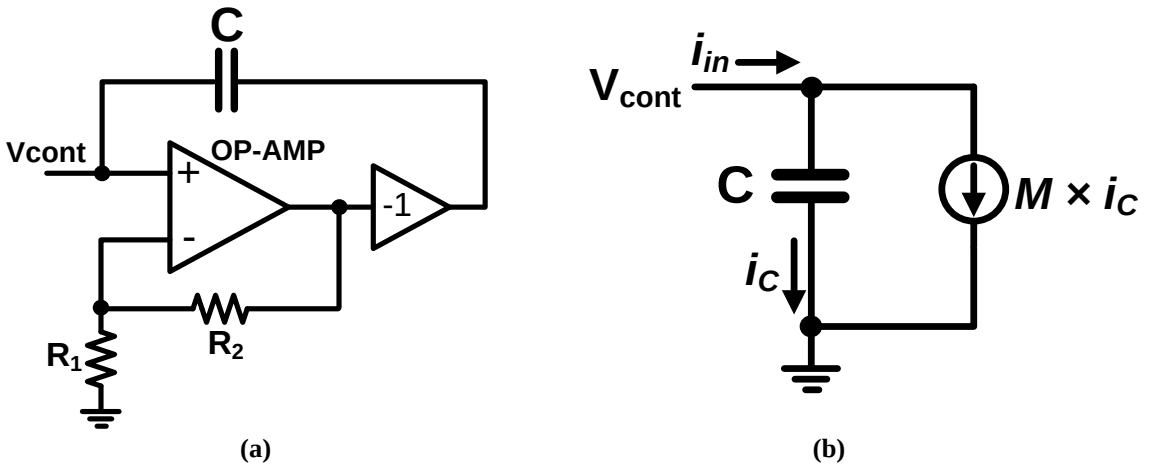


Figure 26. Conventional capacitor multipliers (a) voltage mode (b) current mode.

Nevertheless, each technique has limitations against being adopted in a PLL loop filter. In [26], the narrow input operating range due to the source follower configuration in the input stage prevents wide tuning of a voltage-controlled oscillator (VCO) in a PLL. In [27, 28], the capacitor multipliers adopted a simple current mirror whose mirroring ratio determines the multiplication factor. Thus, for a high multiplication factor, device sizes and power consumption have to be large, and a device mismatch in the current mirror impairs accuracy of the multiplication factor. This research proposes a multi-stage capacitor multiplier achieving a high multiplication factor without sacrificing power consumption.

4.2.2. Design of a High Multiplication Factor Capacitor Multiplier

Figure 27 shows the proposed capacitor multiplier consisting of three current mirror stages in cascade for the third order PLL loop filter.

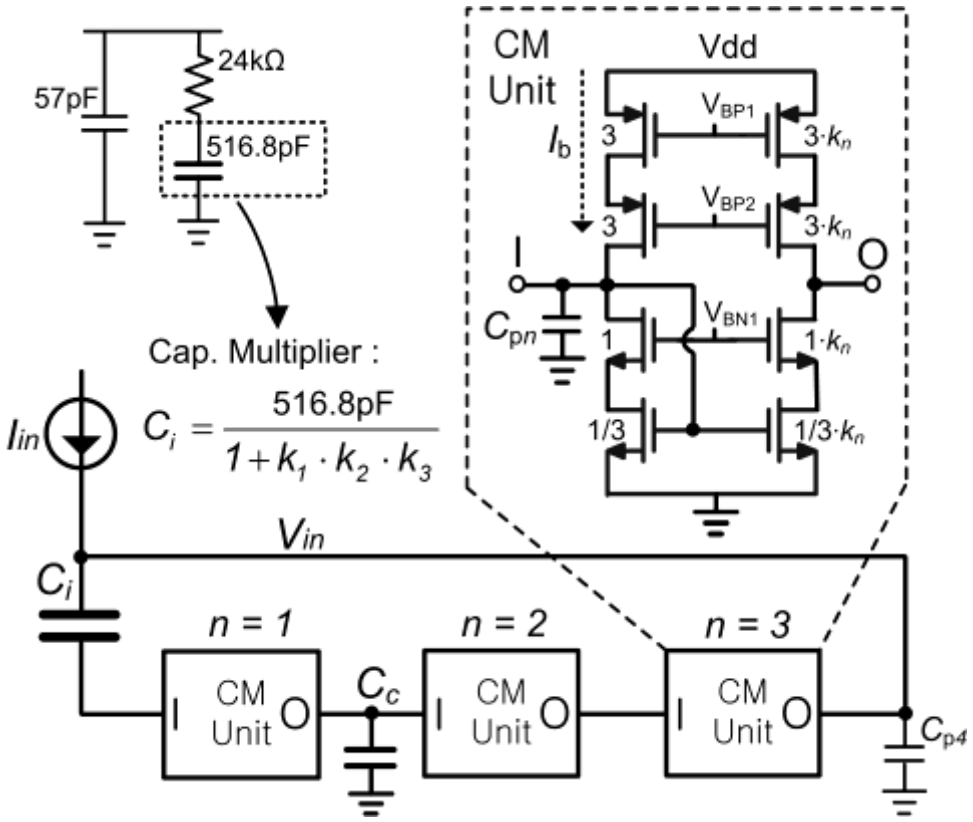


Figure 27. Proposed high multiplication factor capacitor multiplier.

Each stage has the same structure and input bias current, but can have a different mirroring ratio as k_1, k_2 and k_3, respectively. The equivalent small-signal admittance at the input node can be represented as follows.

$$y_{in} = g_{o3} + sC_{p4} + \frac{s^2 C_{p1} C_i + sC_i \cdot g_{m1} \cdot (1 + k_1 \cdot k_2 \cdot k_3 \cdot \frac{g_{m2}}{sC_{p2} + g_{o1} + g_{m2}} \cdot \frac{g_{m3}}{sC_{p3} + g_{o2} + g_{m3}})}{s(C_i + C_{p1}) + g_{m1}} \quad (10)$$

where C_{pn}, g_{mn} and g_{on} are the parasitic capacitance and input and output transconductances of the nth current mirror stage, respectively.

From the above equation, the proposed capacitor multiplier could have an ideal capacitance of $C_i(1+k_1k_2k_3)$ between the first pole of $g_{o3}/C_i(1+k_1k_2k_3)$ and the first zero of g_{m1}/C_i. Hence, if the first pole and the first zero are split far away, its operating frequency

range could be increased. Sometimes, in a multi-stage design, closely-located poles could evoke a stability problem. In Figure 27, a small compensation capacitor, C_c, was connected to ground between two consecutive stages to separate locations of the dominant pole and the second pole to solve the stability problem.

When the input bias current of a current mirror is set to I_b, the proposed capacitor multiplier consumes a current of $(3+k_1+k_2+k_3)I_b$, which is $(1+k_1k_2k_3)/(3+k_1+k_2+k_3)$ times less than those in previous works of [27, 28] with the same multiplication factor of $1+k_1k_2k_3$. Also, the physical chip area is reduced by the same ratio, since the device size and the bias current are proportional to each other. Therefore, for k_1, k_2 and k_3 equal to 10, more than 30 times current consumption and chip area can be saved. In addition, a low headroom bias circuit design allows the proposed capacitor multiplier to have a wide input operating range. Thus, the PLL is able to achieve a wide frequency tuning range with a small VCO voltage gain, which is required for the reference spur reduction. In the circuit implementation, the mirroring ratio of each stage is set to 4, which results in the overall multiplication factor of 65. Therefore, an effective capacitance of 516.8pF was implemented with only a capacitance of 7.95pF. Figure 28 shows the impedance of the capacitor multiplier, compared with that of an ideal capacitor. By using a cascade configuration with long channel transistors, each current mirror achieved an output impedance of 155dBΩ or 55MΩ near DC, which is large enough to make the current leakage negligible. The concern on the stability problem as a closed loop multi-stage topology was eliminated by adopting a small compensation capacitor between the first and the second stages, as mentioned. Figure 29 shows the variation on input impedance near DC as the input DC level, V_{in}, is swept. In the range between 0.4V and 1.5 V, the

impedance is larger than 145 dB and the location of the first pole is kept less than 10Hz. Thus, a wide range of 1.1V can be utilized to tune the frequency of a VCO.

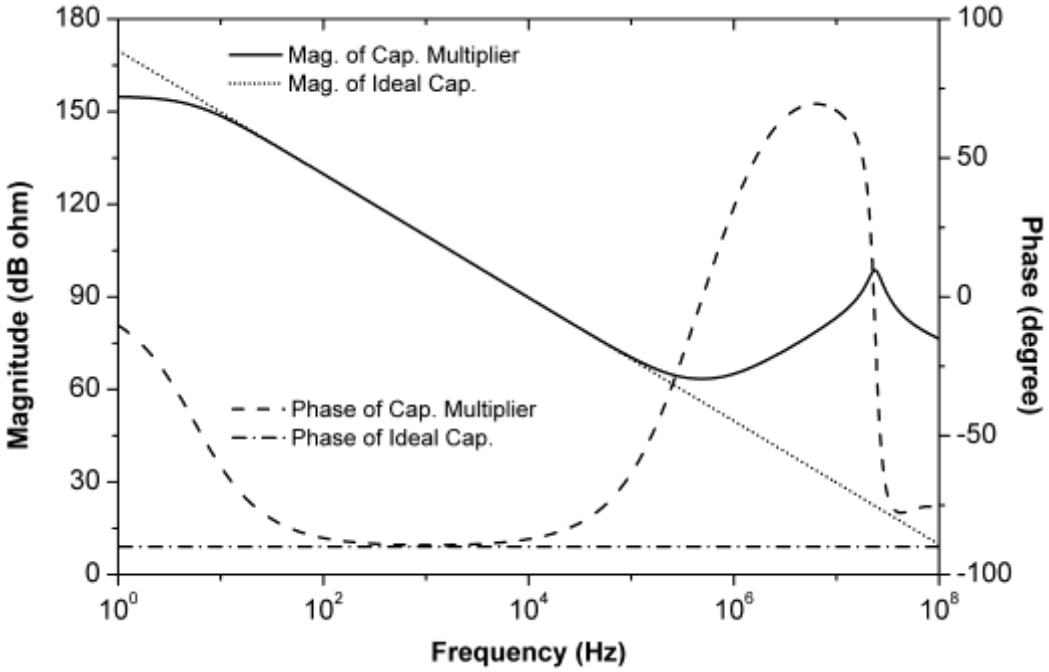


Figure 28. Frequency response of capacitor multiplier impedance.

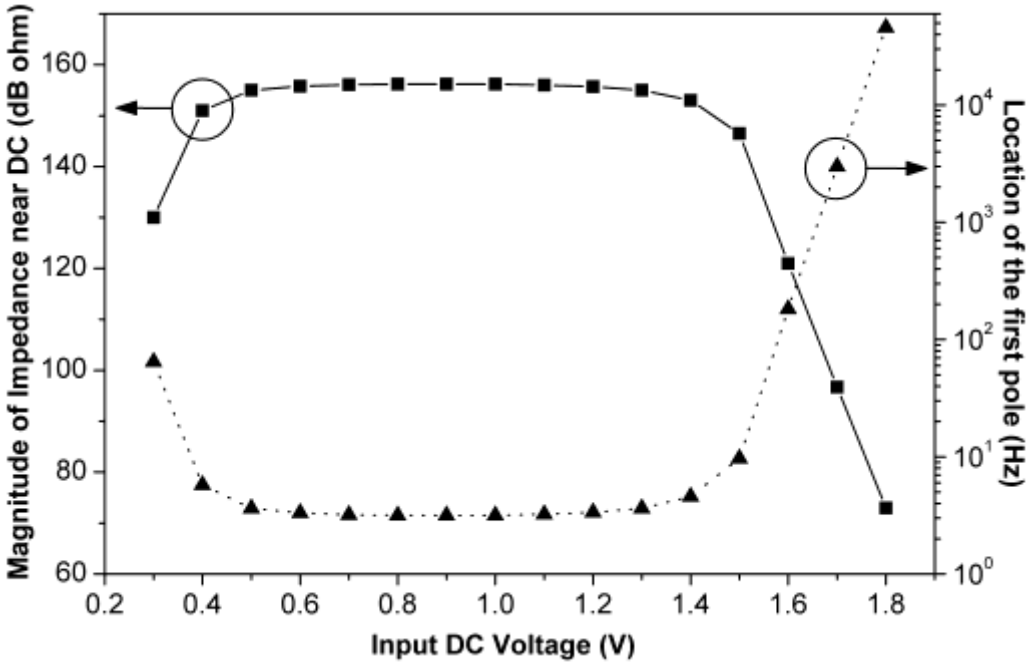


Figure 29. Impedance of the proposed capacitor multiplier with input DC voltage sweeping.

4.2.3. Measurement Results

In Figure 30, the measured phase noise spectrum shows the PLL has a loop bandwidth of 40 kHz, which verifies that the capacitor multiplier provides an accurate multiplication factor. Measured phase noise is -58 dBc/Hz and -111 dBc/Hz at 10 kHz and 600 kHz frequency offsets, respectively. Also, the wide input DC operating range of 1.1 V of the capacitor multiplier lends to the PLL having a wide frequency tuning range with small VCO voltage gain.

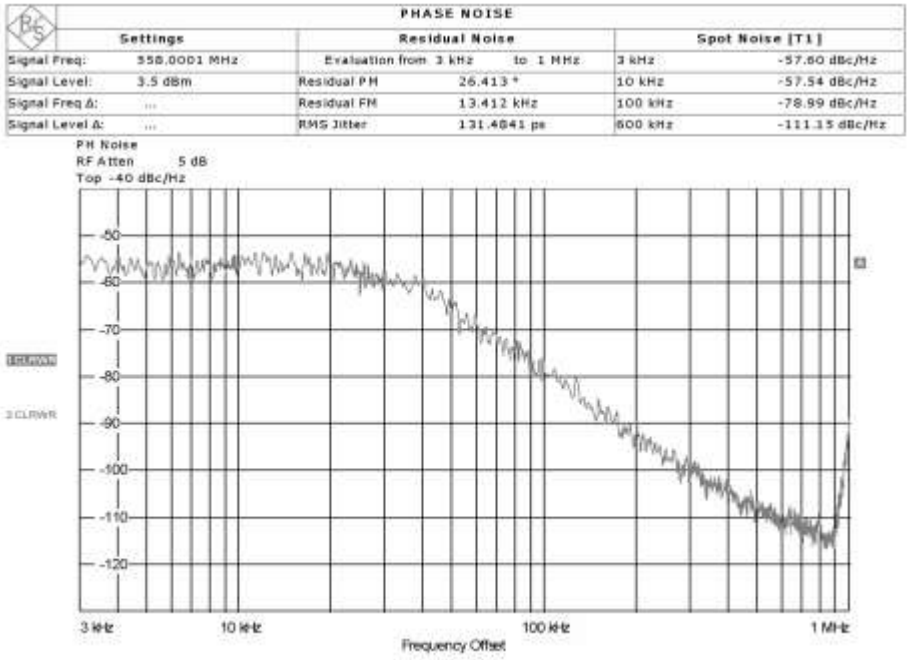


Figure 30. Phase noise spectrum of the PLL adopting a capacitor multiplier.

4.2.4. Conclusions

A monolithic Integer-N PLL with a 1MHz reference frequency has been fabricated in a 0.18 μm CMOS technology to employ a proposed capacitor multiplier. Using the proposed capacitor multiplier and the ring VCO [29], the PLL takes only 380μm×600μm active chip

area, as shown Figure 31. Considering 120 μA charge-pump current and 50 MHz/V VCO gain, parameters of 24 kΩ, 57 pF and 516.8 pF were used for implementing a third order loop filter with 40 kHz bandwidth.

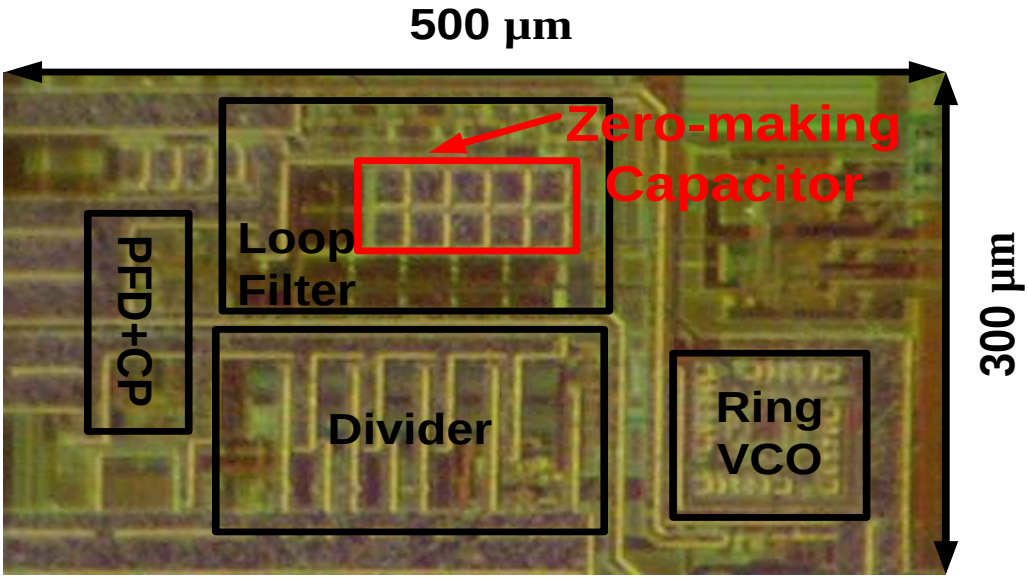


Figure 31. Die photograph of a prototype PLL adopting the high multiplication factor capacitor multiplier.

The proposed capacitor multiplier achieved a multiplication factor of 65 with a current consumption of 100 μA from a 1.8 V supply. Thus, the zero-making capacitor of 516.8 pF was implemented with an on-chip metal-insulator-metal (MIM) capacitor of only 7.95 pF, and the total area of the loop filter was dramatically minimized. If more area reduction is desired, the proposed technique can be adopted also to the other capacitor of 57 pF. Figure 32 compares performance of the proposed capacitor multiplier with conventional architectures.

	Tang, EL 2003	Shu, JSSC 2003	Hwang, EL 2006	**This Work, EL 2009**
Topology	Closed-loop Miller	Single-stage Current Mode	Single-stage Current Mode	Three-stage Current Mode
Technology	0.5 μm CMOS	0.35 μm CMOS	0.35 μm BiCMOS	0.18 μm CMOS
Multiplication Factor	× 3	× 16	× 16	× 65
Current Consumption	430 μA	100 μA	240 μA	100 μA

Figure 32. Performance comparison of the proposed high multiplication capacitor multiplier and conventional architectures.

4.3. A DLL-based Wide Range Programmable Frequency Multiplier

4.3.1. Introduction

Figure 33 compares properties of the DLL-based frequency multiplier and the PLL-based frequency synthesizer.

	PLL Freq. Synthesizer	DLL Freq. Multiplier
Freq. Resolution	Fine	Moderate
Phase Noise	Moderate	Good
Freq. Change	Moderate	Fast
Chip Area	Large	Compact
Scalability	Bad	Good

Figure 33. Property comparison of a DLL-based frequency multiplier and a PLL-based frequency synthesizer.

Different from the PLL-based architecture, in a DLL-based frequency multiplier, the VCDL generates evenly spaced delay edges when the DLL is locked. Then, by combining these edges, the multiplied output frequency is generated. Therefore, a frequency multiplier has a limitation on the frequency resolution. However, since jitter is not accumulated from cycle to cycle, it can achieve good phase noise performance. Also, frequency change takes just switching time of the edge combiner. Furthermore, since the DLL requires only one small capacitor in a loop-filter as a passive component, chip area becomes compact.

Thus, for minimizing area consumption, a PLL-based frequency synthesizer can be replaced with a programmable DLL-based frequency multiplier. In this research, a new simple frequency multiplier consisting of a DLL, a pulse generator and a pulse combiner is proposed. In the proposed architecture, each sub-pulse is generated from one corresponding unit delay cell. Therefore, a high multiplication factor and wide range of the output clock frequency can be obtained with a fewer number of delay cell stages. In addition, power dissipation is minimized because the pulse generator consists purely of D flip flops (DFFs) and inverters operating only when triggered in their turn. Also, since only the required sub-pulses are generated from the pulse generator for a target output signal frequency, an additional pulse selection process has been eliminated.

In the design of the VCDL, a saturated-type differential delay cell [15], [19] with a latch and transmission gates is adopted, which can easily provide a long time delay. Thus, the proposed frequency multiplier can be locked to a low-frequency reference clock without sacrificing physical area to integrate a large number of delay cells. Furthermore, owing to a saturated-type configuration adopting a latch, a sub-pulse has a fast and full switching

transition edge, which is essential for enhancing phase noise performance [15]. Finally, a power/area-efficient start-controlled circuit for preventing harmonic locking, which is critical in wide range DLL-based architectures, is proposed.

4.3.2. Design of the Wide Range Programmable Frequency Multiplier

The proposed frequency multiplier can take input reference frequencies from 30 MHz to 90 MHz, and the multiplication factor can be any common divisors of the number of delay cell stages, 24. Thus, wide range clock signals from 120 MHz to 2.16 GHz can be obtained from the proposed frequency multiplier. Figure 34 shows the overall block diagram of the proposed DLL based frequency multiplier consisting of a DLL, a pulse generator and a pulse combiner.

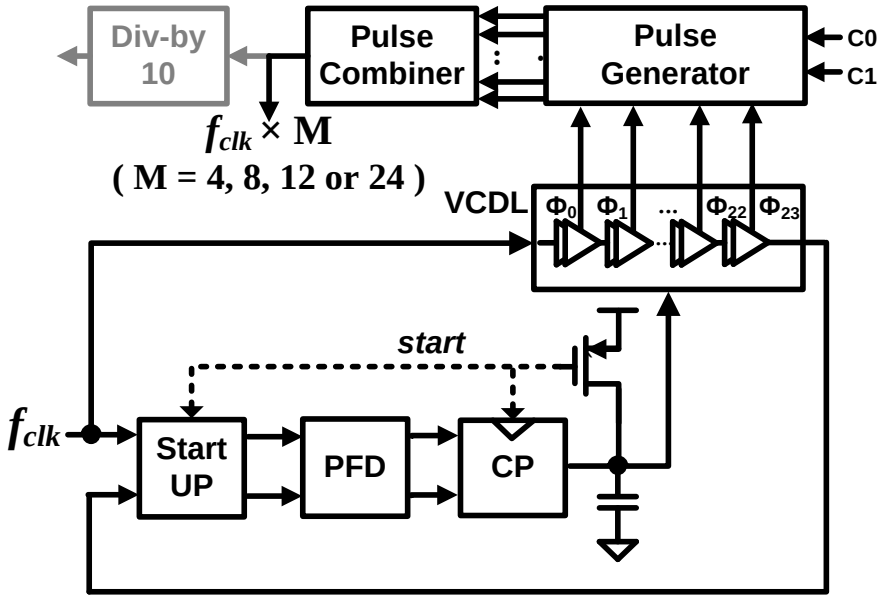


Figure 34. Proposed DLL-based frequency multiplier.

When the DLL, implemented with a phase detector, a charge pump, a loop filter and a VCDL, locks to the reference clock, the VCDL generates 24 uniformly-spaced differential phase-shifted signals. The pulse generator detects the rising edge of the selected phase-shifted signals among 24 streams according to the programmed 2-bit signals and creates a short pulse from each selected signal. Then, the pulse combiner collects these short pulses and provides a multiplied clock.

4.3.2.1. High Multiplication Factor Pulse Generator

Figure 35 details the operation of the proposed pulse generator and the pulse combiner, specifically, when M equals 12.

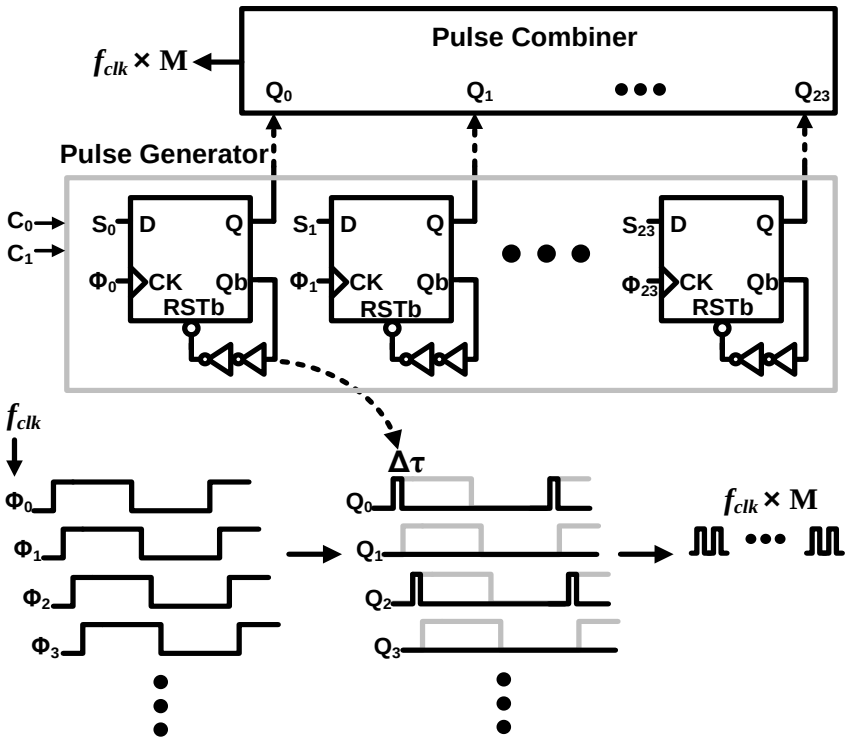


Figure 35. Detail operation of the proposed pulse generator and combiner when M equals 12.

When the phase shifted signal from the VCDL, Φ_k, enters to the corresponding *k*th DFF, Q_k goes high if the value in the D node, S_k, is set to 1. In the meanwhile, Qb_k goes low and resets Q_k by triggering the RSTb node. Since this reset process takes two-inverter delay time, a short pulse of duration, $\Delta\tau$, is generated at Q_k. Finally, the subsequent pulse combiner collects these pulses. In order to create only the required pulses, each S_k is set to either 0 or 1 according to the programmed 2-bit signals, C_0 and C_1. Thus, one of four multiplication factors - 4, 8, 12 and 24 - can be selected. In the proposed pulse generator, since each DFF generates one pulse from the corresponding delay cell, a high multiplication factor of up to 24 has been obtained with the same number of delay cells in VCDL. Also, power consumption is reduced because the DFFs and inverters are operating only when clocks are triggering them. Furthermore, since unnecessary pulses for the specific output clock are not generated, a separate phase selection process is not required.

The proposed frequency multiplier targets mobile communication systems using only rising edges. However, some digital applications using both of rising and falling edges require 50% duty cycle. In the proposed delay cell, the differential signals, Φ_k and $\Phi_k b$, are inherently generated from the differential-type architecture. Since another clock from $\Phi_k b$'s is supposed to have phase difference of π regarding the counterpart from Φ_k's, 50% duty cycle can be obtained by use of both clocks without sacrificing the maximum output frequency.

4.3.2.2. Delay Cell with Wide Delay Range and Good Phase Noise

In order to be utilized in a DLL, the delay from the VCDL should be long enough to lock to the input reference clock. Generally, a long delay can be generated in two ways. First,

utilizing a large number of delay cells with a relatively short unit delay can be considered. In this case, increase in area and power consumption is inevitable.

Conversely, if a small number of delay cells are used, each unit-delay cell should generate a considerably long delay. This prevents a signal from having a fast-switching transition edge; the slow-switching edges are more prone to degrade phase noise performance [15]. The phase noise performance of the unit delay cell is the important factor determining that of the overall DLL-based frequency multiplier [30]. This can be explained from the relation between the timing error variance of the unit delay cell, $E(\Delta d^2)$, and that of the overall VCDL, $E(\Delta t_{VCDL}^2)$ as

$$E(\Delta t_{VCDL}^2) = E\left(\Delta d^2\right) \cdot \frac{2N}{2 - \frac{I_{CP} K_d}{C_L}}, \tag{11}$$

where N, I_{CP} ,K_d and C_L denote the number of unit delay cell in the VCDL, the charge pump current, the gain of the delay cell, and the capacitance of the loop filter capacitor, respectively. Since the timing error variance can be directly translated to a jitter or a phase noise performance, (11) shows that a good phase noise performance of the delay cell is indispensable for achieving a good phase noise performance of the VCDL or the frequency multiplier.

Therefore, to create a long unit-delay with a fast-switching edge avoiding phase noise degradation, the architectural idea was adopted from the ring-type oscillator of [29]. Figure 36 (a) shows the proposed delay cell based on a pseudo-differential saturated-type configuration. In conventional delay cells, creating a long unit-delay inevitably results in slow signal transition, irrespective of a delay-making mechanism. However, in the

proposed delay cell, the signal regains fast-switching edges by the cross-coupled PMOS latch. When the signal is injected, the latch operates in the direction of opposing the signal transition in the PMOSs. However, after a while, the function of the latch changes into a positive feedback and accelerates the signal transition.

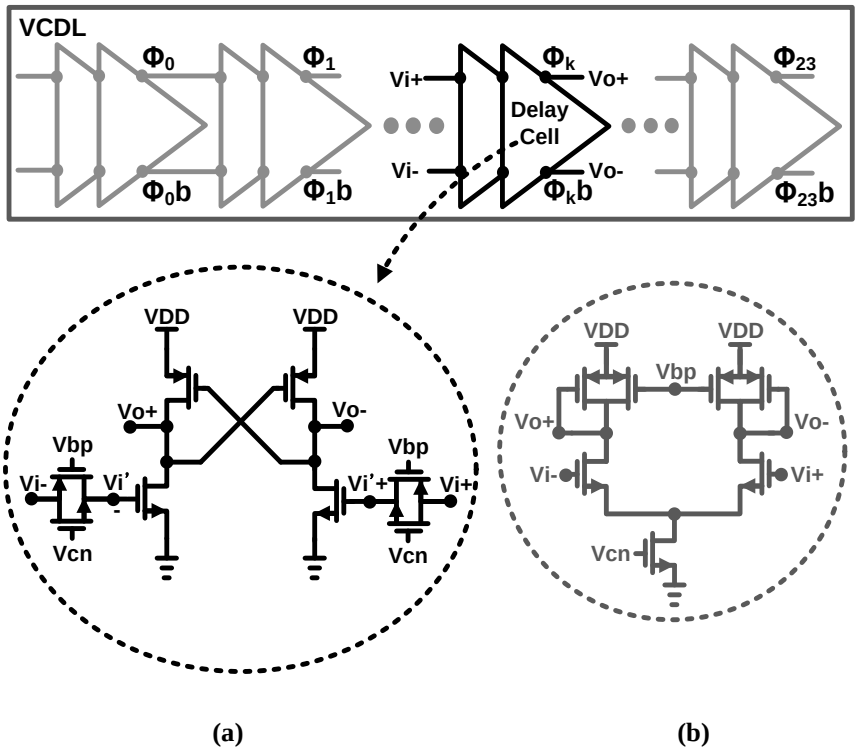


Figure 36. Delay cells adopted in the VCDL (a) proposed delay cell (b) conventional Maneatis load delay cell [31].

Figure 37 shows the signal transition characteristics of the proposed delay cell. When a 920 ps-delay is generated, the proposed delay cell makes a much steeper transition compared to the conventional Maneatis dealy cell in Figure 36 (b). Also, due to the saturated-type configuration eliminating the tail transistor, the proposed delay cell allows for rail-to-rail output swing.

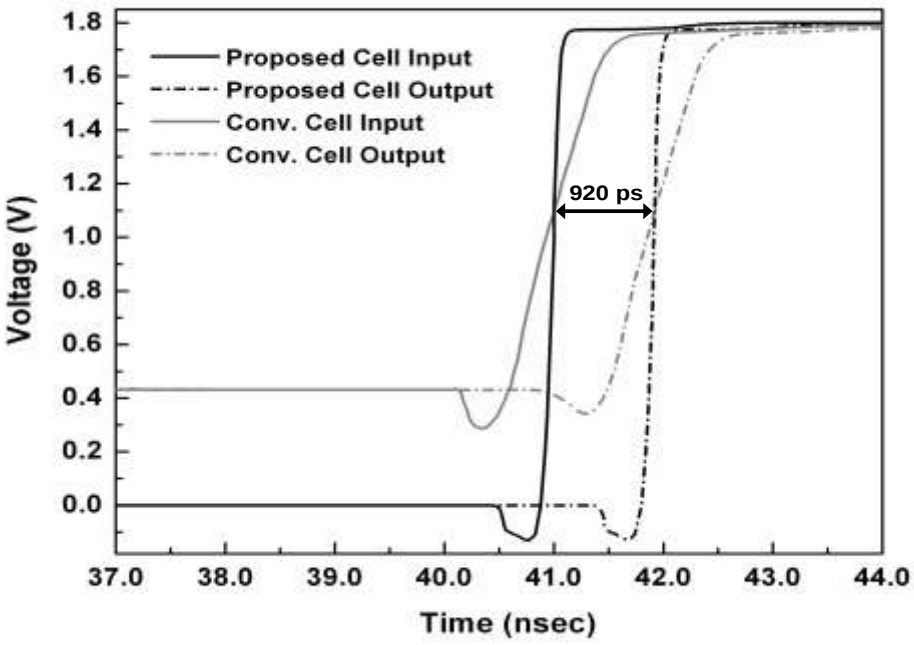


Figure 37. Time transient simulation on generating 920 ps time-delay of the proposed delay cell and the conventional delay cell with a Maneatis load.

Qualitatively, the more time transistors are turned-on, the more thermal noise current is generated from those devices. The fast-switching transition and the rail-to-rail swing imply shorter duration for transistors being turned-on, which intrinsically improves phase noise performance [15], [19], [20]. In addition, the elimination of the tail transistor reduces 1/f noise which is mainly contributed by bias devices, [22], [23]. This also can be explained by the phase noise analysis of ring oscillators [15]:

$$L(\Delta\omega) = \frac{512F \cdot kT \cdot R \cdot V_{DD}}{27\pi \cdot {V_{PP}}^3} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \quad , V_{PP} = 2\frac{SR_{\max}}{\omega_o}, \tag{12}$$

where F, $SR_{\max}$, $\Delta\omega$, ω_o, kT, V_{DD} and R are the excess noise factor, the maximum output slew rate, the angular frequency offset from the center frequency, the center frequency, the thermal energy, the power supply voltage and the equivalent output resistance of a delay

cell, respectively. In (12), the increase of the maximum slew rate of the signal and V_{pp} due to the fast rail-to-rail signal transition of the proposed delay cell reduces phase noise. Therefore, (12) confirms that the adoption of a latch improves the phase noise performance of the delay cell even when utilized with a long delay-making mechanism. By utilizing a transmission gate as a long delay-making method, the proposed delay cell can create a wide-range variable delay. Figure 38 shows the simulation result on a delay from one unit delay cell when sweeping the control voltage, V_{cn}. Since the delay changes in a linear fashion over a wide range, the proposed delay cell can be usefully adopted to a DLL for locking any widely varying input reference frequency by just changing the pre-selection voltage of V_{bp}.

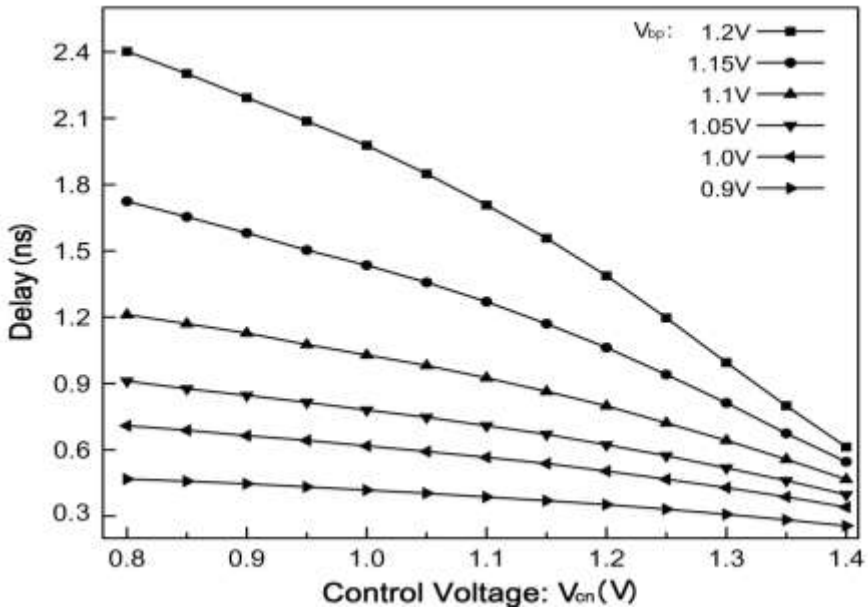
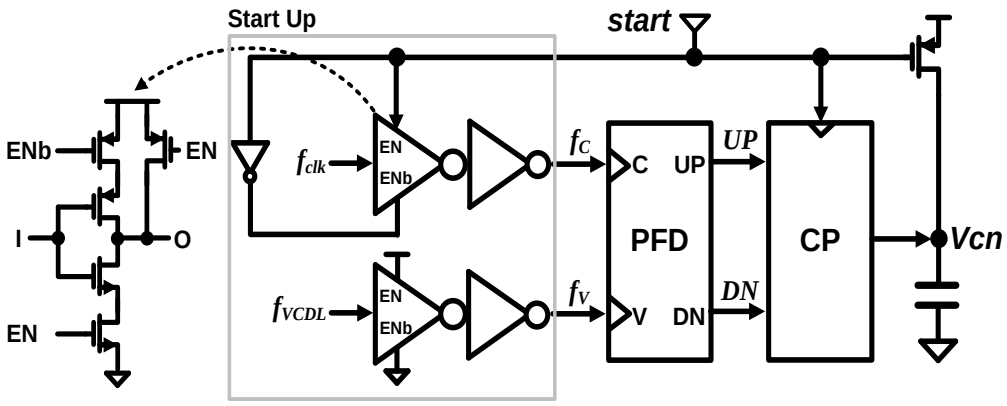


Figure 38. Delay time from the proposed unit delay cell according to the swept control voltage, V_{cn}, and the bias voltage, V_{bp}.

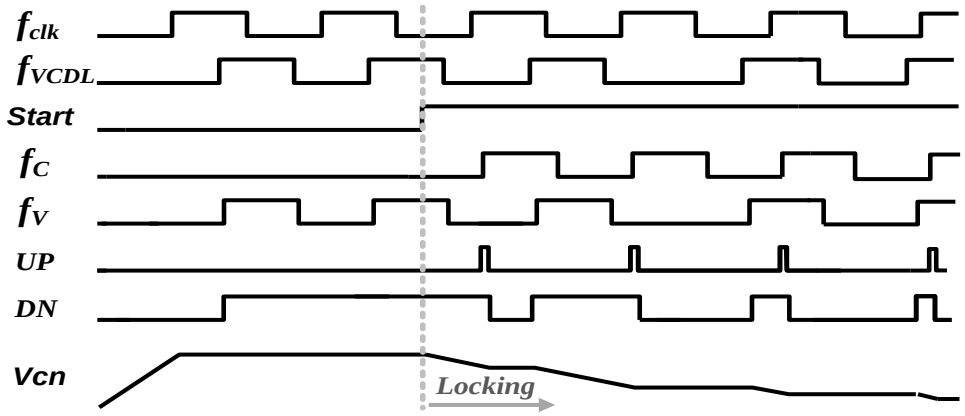
4.3.2.3. Simple and Robust Anti-harmonic Locking Technique

Generally, DLL-based architectures covering a wide range are vulnerable to harmonic locking. In previous research, several novel techniques have been reported. First, a single replica delay cell can be utilized to limit the range of the VCDL [32], [33]. Second, a harmonic locking detector block to monitor the harmonic lock can be adopted [34]. Third, a PFD combined with a start-up controlled circuit can solve the problem [35-37].

In this work, a power/area-efficient architecture based on the third concept is proposed as Figure 39 (a). Figure 39 (b) details the timing diagram explaining the sequential operation. In the beginning, the *start* signal is set to zero, and the capacitor in the loop filter is charged through the PMOS on the top of the capacitor instead of the disabled charge pump. Also, the *start* signal disables the inverter transferring the reference clock, f_{clk}, to the PFD. Thus, the signal into the port C of the PFD, f_c, is stuck to zero and the PFD detects only the signal into the V node, f_v, which makes *UP* and *DN* maintain their status as low and high, respectively. After a while, V_{cn} goes near VDD, and the delay from the VCDL is forced to set to the minimum. When the signal *start* goes high, the capacitor charging is controlled by the charge pump, and the signal of f_{clk} is transferred to the PFD, simultaneously. By the first rising edge of f_c, DN is reset to low, and the DLL starts the lock-acquisition process without concerns on the harmonic locking problem. The proposed start-controlled circuit is simple and power-efficient by requiring only three inverters and two inverter switches, additionally. Also, since this circuit is insensitive to the change timing of the *start* signal as long as the capacitor is pre-charged enough, it can successfully tackle the harmonic locking problem when adopted to DLL applications with a wide operating range.



(a)



(b)

Figure 39. Anti-harmonic Start-controlled circuit (a) schematic (b) timing diagram of the operation.

4.3.3. Measurement Results

The proposed programmable DLL-based frequency multiplier has been fabricated in a 0.18 μm CMOS technology. For the input reference frequency of 30 MHz to 90 MHz, SMU 200A has been used. Figure 40 shows the single-side band (SSB) phase noise of the output signal with a 1.2 GHz operating frequency when an input reference frequency of 50 MHz is multiplied 24 times.

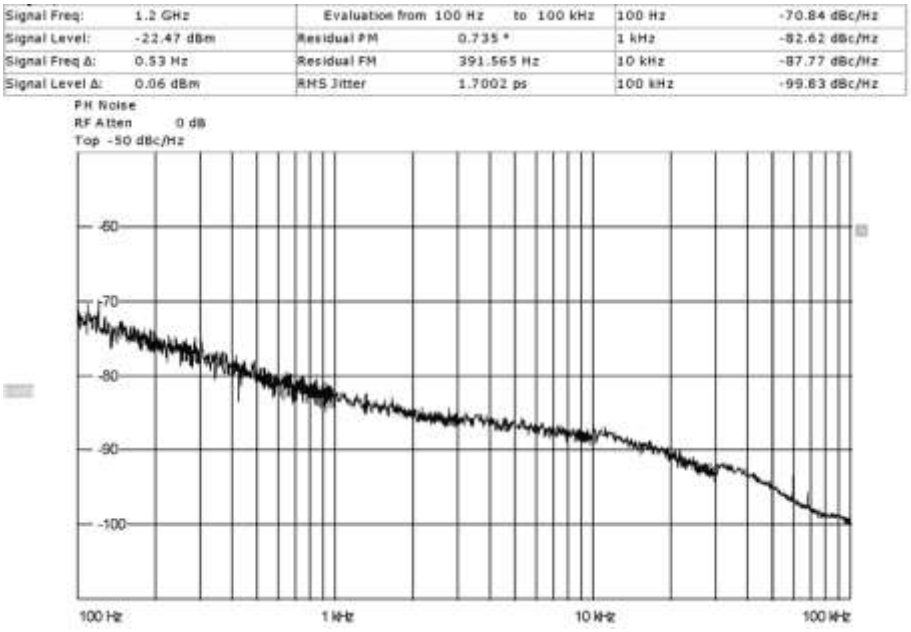
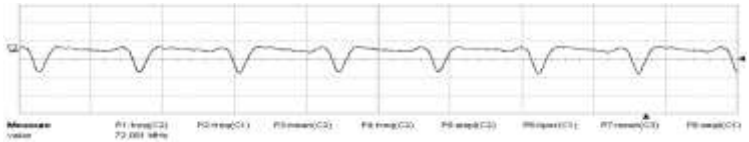


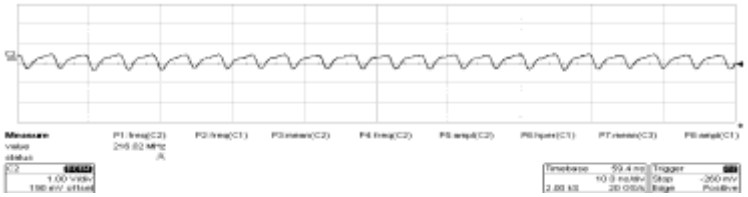
Figure 40. Measured SSB phase noise when a 50 MHz input reference clock is multiplied by 24, generating a 1.2 GHz output clock.

The phase noise performance is -88.7 dBc/Hz and -99.8 dBc/Hz at 10 kHz and 100 kHz offset frequencies, respectively, which can be translated into a 1.7 ps RMS jitter. Figure 41 shows the waveforms of the multiplied output clocks for multiplication factors of 8 and 24 when a 90 MHz input reference clock was injected. For time transient measurement, the output frequency was divided using the divide-by-10 frequency divider, as shown in Figure 32. Thus, the frequencies of 720 MHz and 2.16 GHz were measured as 72 MHz and 216 MHz, respectively. Uneven duty-cycle of the waveforms was due to frequency dividing operation of the divide-by-10 divider, and the limited output buffer bandwidth resulted in degradation on slew rate of waveforms. The proposed frequency multiplier can provide multiplied clock signals from the input clock with a reference frequency as low as 30 MHz. Figure 42 shows that a 30 MHz input reference clock is multiplied four times at the output.

Thus, from Figure 35 and Figure 36, the proposed frequency multiplier can provide the output clock frequency from 120 MHz to 2.16 GHz.



(a)



(b)

Figure 41. Measured waveforms of the output clock when 90 MHz of the input reference frequency is multiplied by M and divided by 10 (a) M=8 (b) M=24.

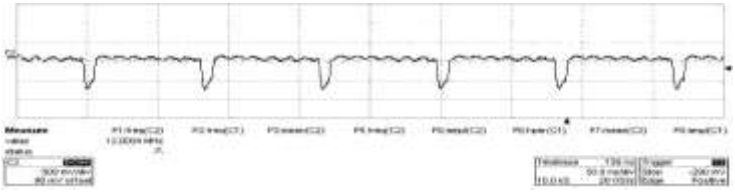


Figure 42. Measured waveforms of the output clock with the minimum operating frequency, 120 MHz, when a 30 MHz input reference frequency is multiplied by 4 and divided by 10.

The power consumption of the proposed frequency multiplier was 16.2 mW from a 1.8 V power supply for a 2.16 GHz output clock. Only 9 mW was consumed in the pulse generator, the pulse combiner and the VDCL combined. Figure 43 shows the micrograph of the prototype chip. The active chip area takes only 0.051 mm^2 despite its capability to generate the required long delay for a 30 MHz input clock.

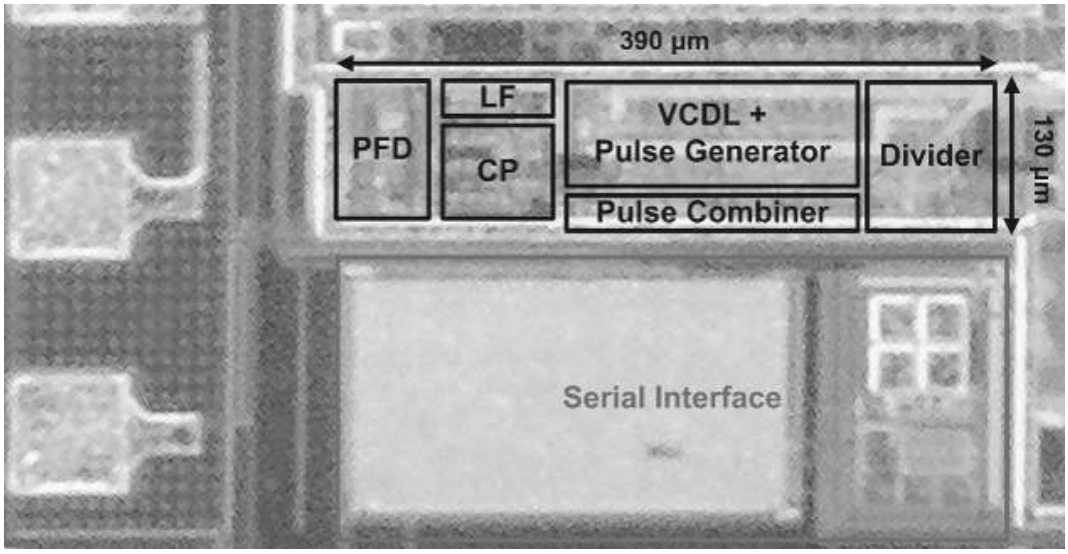


Figure 43. Micrograph of the proposed programmable DLL-based frequency multiplier.

4.3.4. Conclusions

Performance of the proposed frequency multiplier is summarized in Table 1. Table 2 summarizes the performance comparison of the proposed design with prior works. In this research, a programmable DLL-based frequency multiplier has been presented. Based on the proposed pulse generating scheme, the proposed frequency multiplier provides a high multiplication factor of up to 24 while consuming only 16.2 mW when generating a 2.16 GHz output clock. Also, since the proposed saturated-type unit delay cell is capable of providing a long time delay without sacrificing phase noise performance and chip area occupancy, the DLL can lock up an input reference frequency as low as 30 MHz. The phase noise performance is -88.7 dBc/Hz and -99.8 dBc/Hz at 10 kHz and 100 kHz offsets from the operating frequency of 1.2 GHz, respectively, which is equivalent to a 1.7 ps RMS jitter. Also, the proposed power/area-efficient start-up controlled circuit successfully tackled the harmonic locking problem. The active chip area is only 0.051 mm^2. The output clock frequency ranges from 120 MHz to 2.16 GHz.

Table 1. Performance summery of the proposed frequency multiplier

Supply Voltage		1.8 V
Process		0.18 μm CMOS 1P 6M
Multiplication Factor		× 4, × 8, × 12, × 24
Output Clock Frequency	Min	120 MHz (30MHz × 4)
	Max	2.16 GHz (90MHz × 24)
Phase Noise Performance	1.2 GHz	- 82.6 dBc/Hz @ 1kHz - 87.7 dBc/Hz @ 10kHz - 99.8 dBc/Hz @ 100kHz RMS jitter: 1.7 ps
Power Consumption	2.16 GHz	16.2 mW

Table 2. Performance comparison with frequency multipliers in prior works

	[4]	[8]	[9]	This Work
Process	0.35 μm	0.25 μm	0.13 μm	0.18 μm
Supply Voltage	3.3 V	2.5 V	1.2 V	1.8 V
Max. Multi. Factor	× 4	× 10	× 4	× 24
Min. Reference Freq.	240 MHz	120 MHz	240 MHz	30 MHz
Max. Output Clock Freq.	1 GHz	1.2 GHz	2 GHz	2.16 GHz
Power Consumption	42.9 mW @1GHz	52.2 mW @1.2 GHz	21 mW @2 GHz	16.2 mW @2.16GHz

CHAPTER 5

SPUR SUPPRESSION TECHNIQUE USING AN EDGE INTERPOLATOR

5.1. Introduction

In the charge pump (CP)-based phase locked loop (PLL), non-idealities in circuitry such as up-down current mismatches in the CP create a periodic disturbance of the control voltage of the voltage-controlled oscillator (VCO), which causes inevitable reference spurs in the PLL output spectrum [38]. These large spurs and their harmonics are mixed with signals from other channels, degrading the performance of wireless transceivers [17]. Moreover, recently, as wireless communication applications are required to cover wide frequency bands, the issue of reference spurs and the wide spur-free range becomes more important.

One of common approaches that reduce the spur level is to decrease a loop bandwidth. However, the narrow loop bandwidth increases the settling time, and restricts the data rate [39] if the frequency synthesizer is used as a direct modulator. A higher order loop-filter can also enhance the reference spur performance, but increase of the complexity and the instability of the loop filter is inevitable. Another approach is to reduce the VCO frequency-voltage gain, K_{VCO}, which alleviates a level of the undesirable phase modulation by a periodic disturbance of the VCO control voltage. However, when the K_{VCO} is reduced, to compensate the frequency-tuning range additional technique such as the switched capacitor (SC) [40] or the dual-path controlled VCO [41-44] is required. However, when

the SC technique is adopted, the reduction of K_{VCO} calls for complicated digital band selection algorithm for a wide tuning range. This complicated algorithm is likely to increase the frequency selection time even before a frequency synthesizer starts the frequency acquisition process. Besides, the adaptation of the dual-path-controlled VCO suffers from the tradeoff between phase noise and a frequency-tuning range [41], [42].

Recently, to suppress the reference spur, [45], [46] proposed techniques using multiple pairs of a distributed phase frequency detector (PFD)/CP in parallel, which shortens the period to update phase difference information. Thus, ideally, the new reference spur is pushed to a much higher frequency offset, and the spur-free frequency band can be extended. However, to eliminate high-order harmonics of the reference spur, the adoption of a large number of PFD/CP pairs is unavoidable. Hence, mismatches among these multiple PFDs and CPs restrict suppression of the reference spurs. In addition, uneven unit time-delay in front of PFD/CP pairs degrades the performance of spur suppression.

Instead of adopting the multiple PFD/CPs architecture vulnerable to mismatches, this paper proposes an architecture that adopts an edge interpolator that generates equally time-delayed edges, shortening the period to update phase difference information. Therefore, using the proposed edge interpolator with a high interpolation factor, even high-order harmonics of the reference spur as well as the fundamental reference spur can be dramatically eliminated.

5.2. Charge Distribution Mechanism for Spur Suppression

This research proposes an edge interpolator for CP-based PLLs that eliminates the reference spur and its harmonics illustrated in Figure 44. Initially, the edge interpolator

does not generate additional edges and just transfers the original edges from the reference clock and the signal from the divider to the PFD in the same way as conventional PLLs, which result in the f_{ref} and the f_{div} are equal f_{ref_int} and f_{div_int}, respectively.

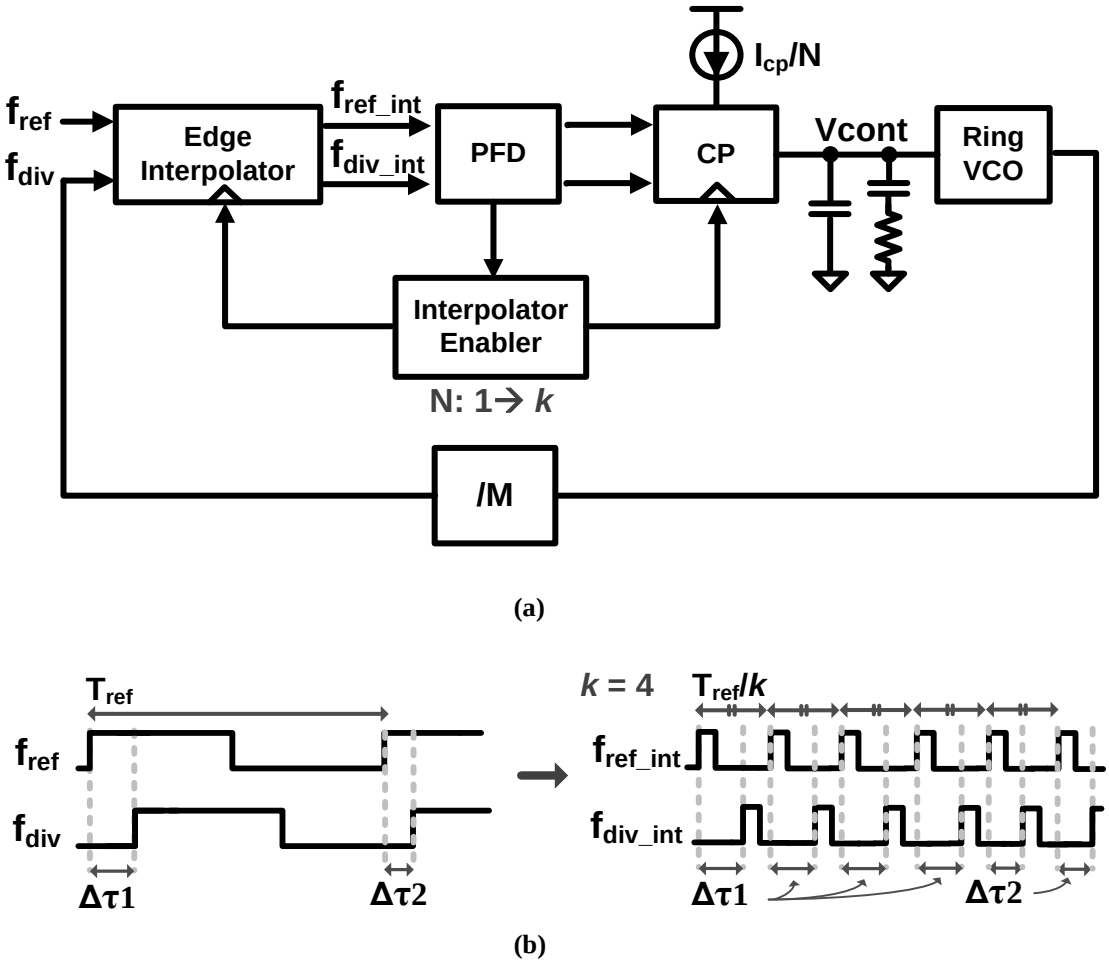


Figure 44. (a) Block diagram of the PLL with the proposed edge interpolator for spur elimination (b) illustration of edge interpolation when the edge interpolator is enabled with an interpolation factor, *k*.

After a while, when the phase difference between f_{ref} and f_{div} decreases less than $\Delta\tau 1$, the interpolator enabler generates an signal that triggers the edge interpolator to produce additional edges to be interpolated between original edges of the f_{ref} and the f_{div}. First,

between the two consecutive rising edges of the f_{ref}, the edge interpolator inserts additional *k*-1 edges that are equally time-spaced as T_{ref}/k, when T_{ref} denotes the period of the reference clock. Simultaneously, the interpolator also inserts *k*-1 edges after the rising edge of the f_{div} with maintaining time-delay of T_{ref}/k. Thus, in one reference period, T_{ref}, every corresponding pair of edges of f_{ref_int} and f_{div_int} maintains the same phase difference, $\Delta\tau 1$. In addition, since the CP current is scaled down *k*-time by the triggering of the interpolator enabler, the loop characteristic is preserved the same as when the interpolator is disabled.

In the PLL adopting the proposed edge interpolator, the process delivering the phase difference information between f_{ref} and f_{div} from the PFD/CP to the VCO is distributed into *k* consecutive times. Figure 45 (a) describes the fine lock-acquisition process after the edge interpolator catches the coarse lock. On the other hand, Figure 45 (b) illustrates the periodic disturbance on the control voltage of the VCO in the locked state. In the conventional case, N = 1, one strong disturbance occurs of the control voltage of the VCO during the every reference period. However, in the case of N = *k*, consecutive *k*-times small disturbance affects the VCO. From Fig. 45 (b), reference spur eliminations through this disturbance distribution mechanism by interpolated edges can be explained as

$$\frac{c_m}{m\cdot k}\cdot\left\{\begin{array}{l}\cos(2\pi f_{ref}t\cdot m)+\cos((2\pi f_{ref}t+\frac{2\pi}{k})\cdot m)+\cdots \\ \qquad\qquad +\cos((2\pi f_{ref}t+\frac{2\pi}{k}\cdot(k-1))\cdot m)\end{array}\right\}$$

$$=\frac{c_m}{m\cdot k}\cdot\sum_{r=0}^{k-1}\cos\left((2\pi f_{ref}t+\frac{2\pi}{k}\cdot r)\cdot m\right)=\begin{cases}0 & for\ m\neq p\cdot k\\ \frac{c_m}{m}\cdot\cos(2\pi m\cdot f_{ref}t) & for\ m=p\cdot k\end{cases} \qquad (14)$$

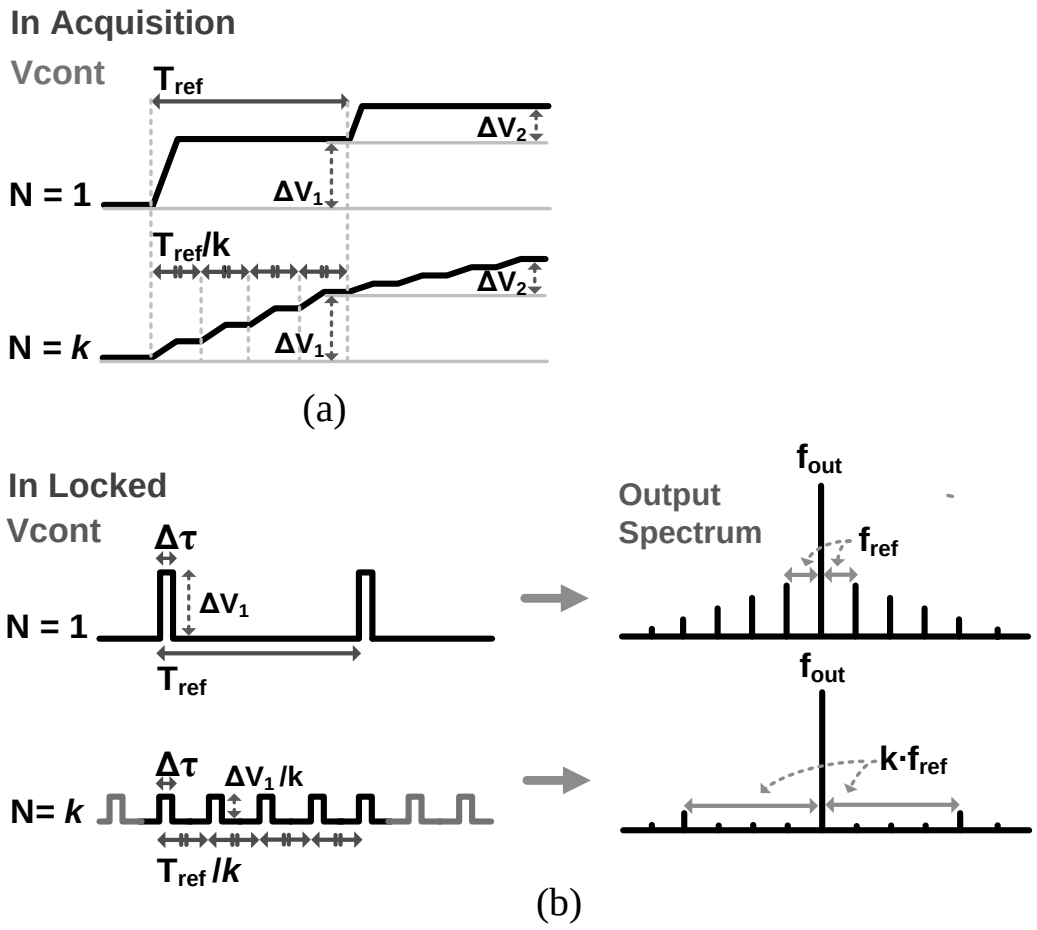


Figure 45. Diagrams of disturbance distribution of the control voltage (a) in the lock acquisition state (b) in the locked state.

where m, c_m, and p are the harmonic order of the reference spur, the amplitude coefficient of the mth harmonic, and any positive integers, respectively. Therefore, theoretically, if interpolated edges are perfectly placed evenly between the original edges, the disturbance distribution mechanism pushes away the fundamental reference spur into $k \cdot f_{ref}$, and all m-th harmonics of f_{ref} are eliminated when m is not any integer multiple of k.

5.3. Edge Interpolation Technique for Charge Distribution

For implementation, the proposed edge interpolator so that it properly functions as it does in theory, two critical issues have to be carefully considered. First, every new edge in f_{ref_int} should be placed at regular intervals of T_{ref}/k. Second, every corresponding pair of edges in f_{ref_int} and f_{div_int} has to maintain the same phase difference between itself as that between the original edges of f_{ref} and f_{div}, for delivering the accurate total phase difference information to the control voltage of the VCO through the PFD/CP.

When α is defined as an error of the interval of new edges in f_{ref_int}, the interval of consecutive edges can be represented as $T_{ref}\cdot(1+\alpha)/k$. Then, the equation, which estimates the practical spur suppression level of the proposed architecture including the effect of α, can be derived from (14). When specifying the focus only on the fundamental spur level, which refines *m* as 1, (14) can be represented as

$$\frac{c_1}{k}\cdot\sum_{r=0}^{k-1}\cos\left(2\pi f_{ref}t+\frac{2\pi(1+\alpha)}{k}\cdot r\right)$$
$$=\frac{c_1}{k}\cdot\left\{\cos(2\pi f_{ref}t)\sum_{r=0}^{k-1}\cos\left(\frac{2\pi(1+\alpha)}{k}\cdot r\right)+\sin(2\pi f_{ref}t)\sum_{r=0}^{k-1}\sin\left(\frac{2\pi(1+\alpha)}{k}\cdot r\right)\right\}. \quad (15)$$

From (15), the fundamental spur suppression respective to the spur level without the proposed technique, in which *k* equals 1, can be expressed as

$$20\log_{10}\left[\frac{1}{k}\cdot\left\{\left(\sum_{r=0}^{k-1}\cos\left(\frac{2\pi(1+\alpha)}{k}\cdot r\right)\right)^2+\left(\sum_{r=0}^{k-1}\sin\left(\frac{2\pi(1+\alpha)}{k}\cdot r\right)\right)^2\right\}^{1/2}\right] dB. \quad (16)$$

Finally, using trigonometric formulae, (16) can be reduced as

$$20\log_{10}\left\{\left|\frac{2}{k}\cdot\sum_{r=1}^{\lfloor k/2\rfloor}\cos\left(\frac{(2r-1)\pi}{k}\cdot(1+\alpha)\right)\right|\right\}\ dB. \tag{17}$$

Figure 46 shows fundamental spur suppression according to the various number of the interpolation factor, *k*, when the interval error, α, is swept from (17). As shown in Figure 46, errors between interpolated edges severely degrade the spur elimination capability of the proposed technique. Therefore, for the good performance of the proposed edge interpolator, a delay locked loop (DLL)-based architecture is the best choice, which can guarantee a regular interval between edges.

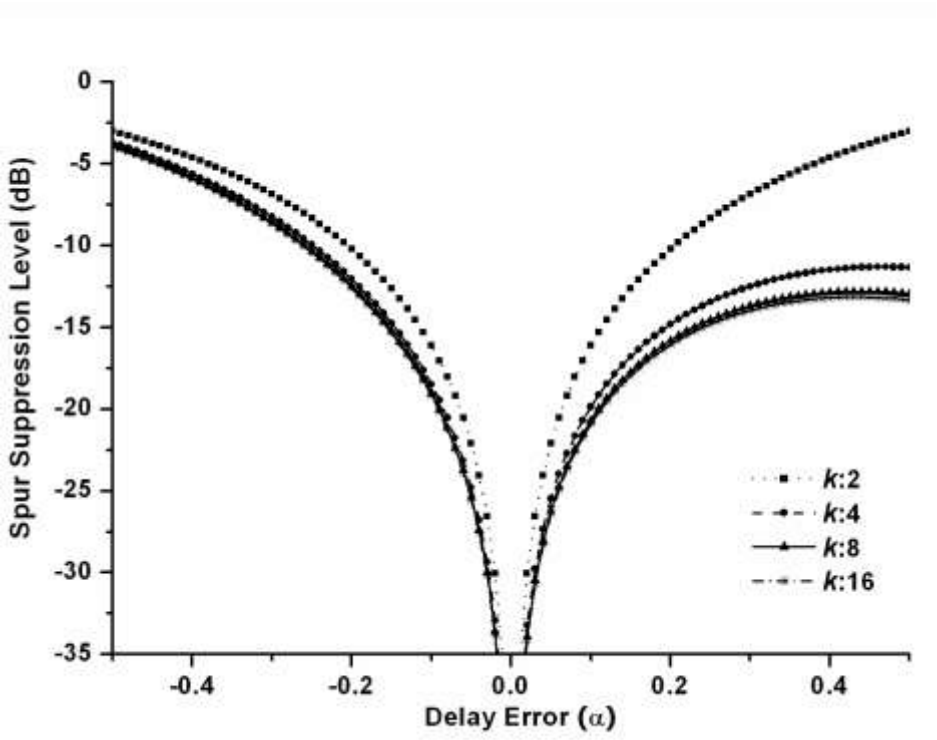


Figure 46. Fundamental spur suppression level according to delay error of α.

Figure 47 shows the proposed edge interpolator consisting of a DLL, a replica voltage-controlled delay line (VCDL), and edge generator/combiners. The reference clock

frequency, f_{ref}, was chosen as 13 MHz that is widely used in commercial products. The interpolation factor, *k*, was chosen as eight, above which the effect of the α on the spur suppression level is almost saturated as in Figure 43. In addition, using *k* as eight, resulting in eight delay cell stages in VCDLs, the new fundamental reference spur is pushed to the 104 MHz frequency offset, which is farther than receiver frequency bands of popular wireless communication standards, such as code division multiple access (CDMA), wideband CDMA (WCDMA), and global system for mobile communications (GSM).

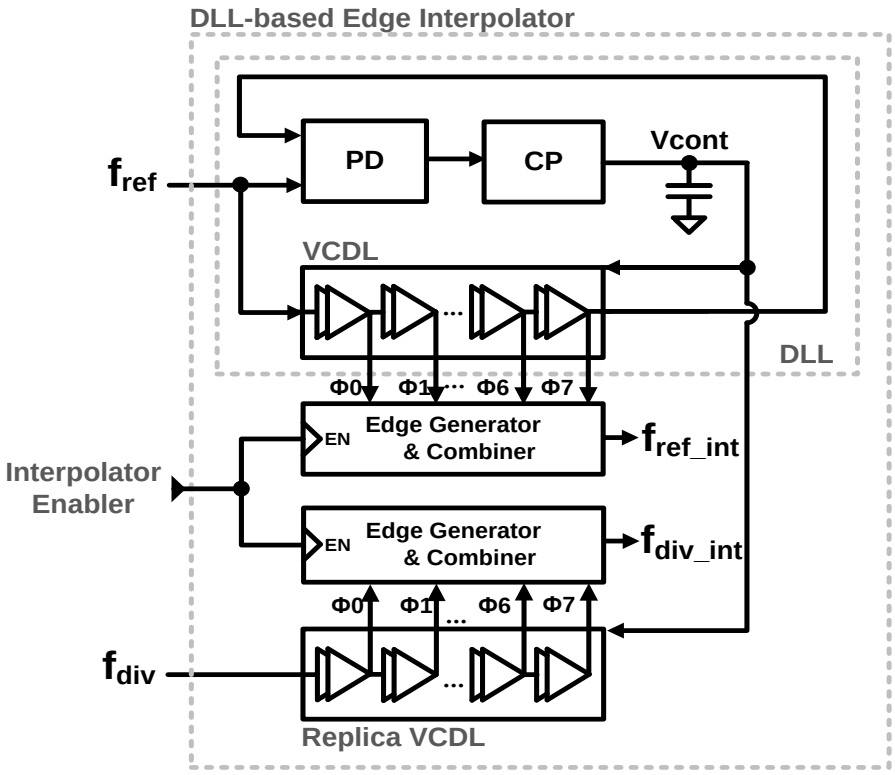
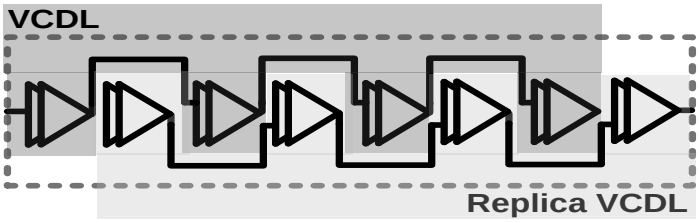


Figure 47. Block diagram of the proposed edge interpolator.

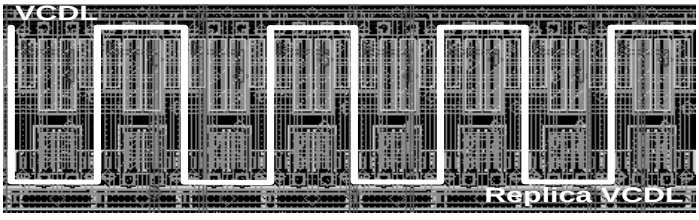
When the DLL locks to f_{ref}, the VCDL generates 8 consecutive signals with the accurate interval of $T_{ref}/8$. Then, the edge generator detects rising edges of these signals

and creates a short pulse from each edge. Finally, the edge combiner collects these short pulses and generates f_{ref_int}. At this time, the control voltage of the DLL keeps the information capable of restoring a $T_{ref}/8$ delay through one unit delay cell in the replica VCDL. Therefore, new edges maintaining intervals of $T_{ref}/8$ can be also created from f_{div} by introducing this control voltage to the replica VCDL, followed by another edge detector and edge combiner.

To maintain the phase difference between every corresponding pair of edges in f_{ref_int} and f_{div_int} precisely equals that between the original edges of f_{ref} and f_{div}, the VCDLs should be carefully laid out. Hence, to provide almost same environment to the two independent VCDLs, they were drawn as one group in the layout by interleaving delay cells one by one from two VCDLs, shown in Figure 48.



(a)



(b)

Figure 48. (a) Block diagram of connections of the VCDL and the replica VCDL in the layout (b) layout.

Figure 49 details the operation of the edge generator and the edge combiner. When the phase-shifted signal from the VCDL, Φ_l, enters the corresponding lth DFF, Q_l becomes high if the value in the D node is set on high. In the meantime, Qb_l becomes low and resets Q_l by triggering the RSTb node. Since this reset process takes two-inverter delay time, a pulse of short duration is generated at Q_l. Finally, the subsequent edge combiner collects these pulses.

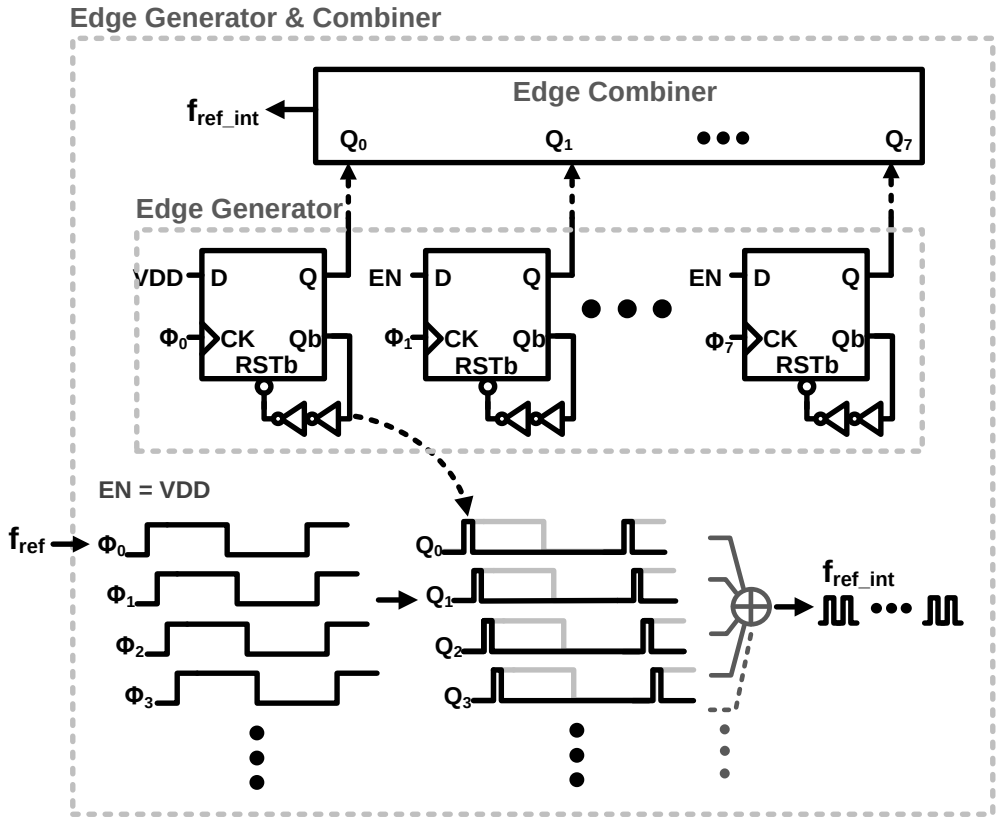


Figure 49. Block diagram of the edge generator and the edge combiner.

By adopting the DLL architecture, the edge interpolator can accurately control the identical interval between consecutively interpolated edges. Since the feedback system of the DLL precisely adjusts itself to internal or external variations, the same phase difference

information can be also well retained between every pair of corresponding edges in f_{ref_int} and f_{div_int}. In addition, after locking to the fixed f_{ref} when the circuit starts, the DLL continues to stay in the locked status even if the PLL changes the output frequency. Therefore, the proposed DLL-based edge interpolator does not affect the loop characteristics and the settling time of the PLL, which lends to the PLL maintaining the single-loop characteristics.

5.4. Measurement Results

The prototype PLL adopting the proposed spur elimination technique was fully integrated with an on-chip loop filter and a saturated-type ring VCO [29] in a 0.18 μm CMOS technology. Figure 50 shows output spectrum of the PLL when the 897 MHz output signal was generated. When the proposed edge interpolation technique was enabled, the fundamental reference spur at the 13 MHz frequency offset was reduced by 16 dB compared to the case when the technique was disabled. Furthermore, all the harmonics of the fundamental reference spur less than a 104 MHz frequency offset, the eighth harmonic, decreased noticeably. The remaining reference spurs at 13 MHz offset and its harmonics were caused by layout mismatches between delay cells in VCDLs as well as between two VCDLs. In addition, the direct substrate-coupling with the reference crystal oscillator could be another major reason why the measurement result was deviated from the theoretical analysis.

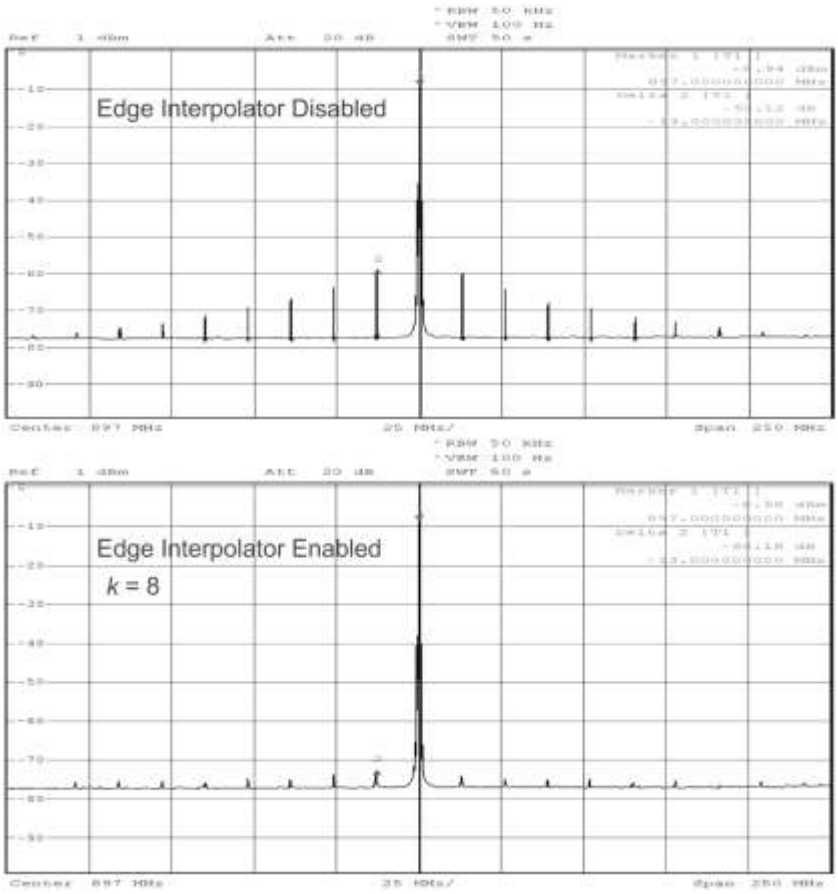


Figure 50. Measured output spectrum of the PLL (f_{out} = 897 MHz).

Figure 51 shows the micrograph of the PLL adopting the proposed DLL-based edge interpolation technique. The active area is 670 μm × 640 μm, and the current consumption is 16.5 mA from a 1.8 V supply. The edge interpolator consumes one-fifth of the total area and the power. When the proposed spur suppression technique was enabled, measured phase noise is -112 dBc/Hz at the 1 MHz offset from the 897 MHz output signal. Finally, Table 3 summarizes the performance of the PLL frequency synthesizer.

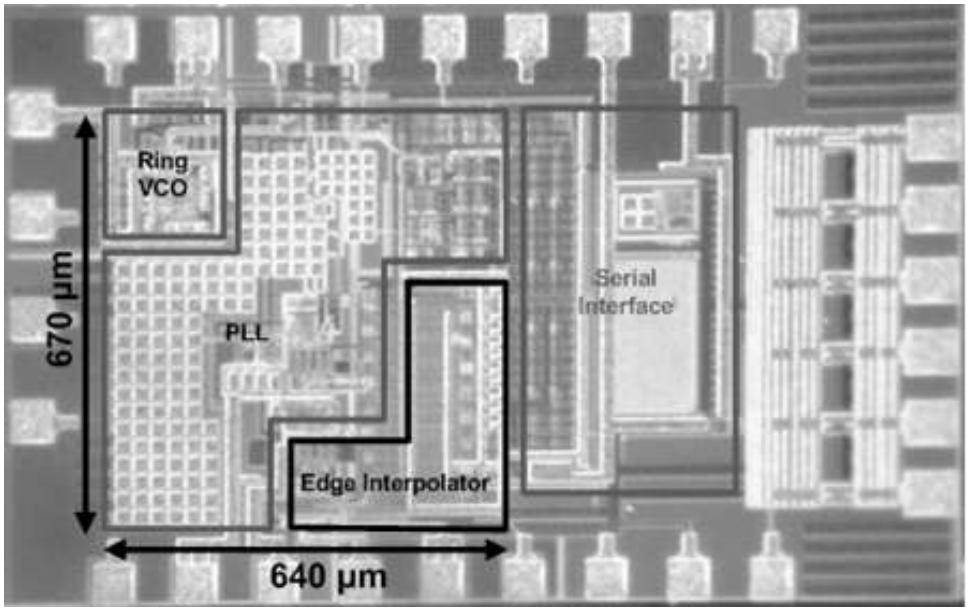


Figure 51. The die micrograph of the PLL with the proposed edge interpolator for spur elimination.

5.5. Conclusions

This research proposed a new reference spur suppression architecture for CP-PLLs based on the edge interpolation technique. Due to the disturbance distribution mechanism on the control voltage of the VCO, the proposed architecture is capable of suppressing the high-order harmonics of the reference spur as well as the fundamental reference spur according to the number of generated edges in the interpolator. In this work, the fundamental spur was suppressed more than 16 dB compared to the case when the interpolator was disabled. In addition, the level of all the harmonics of the reference spur less than the 104 MHz frequency offset were dramatically reduced. The additional circuits for the edge interpolator consume less than one-fifth of the total active chip area and the power. Table 3 summarizes performance of the PLL adopting the edge interpolation technique.

Table 3. Performance summary of the PLL with an edge interpolator

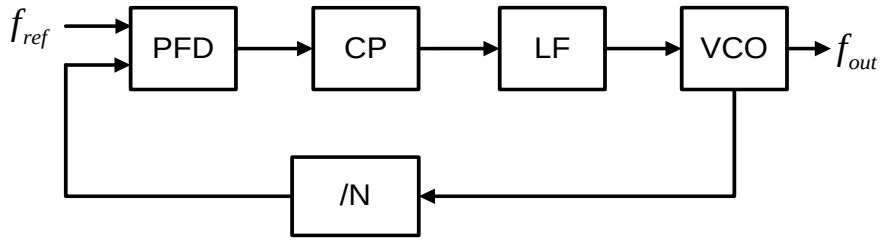
VCO Type	Ring VCO
Output Signal Frequency	700 ~ 1050 MHz
Reference Clock Frequency	13 MHz
Phase Noise at 1 MHz Offset @ 897 MHz	-112 dBc / Hz
Spur Level at 13 MHz Offset @ 897 MHz	
Edge Interpolator Disabled	-50 dBc
Edge Interpolator Enabled	-66 dBc
Supply Voltage	1.8 V
Current Consumption	16.5 mA
Edge Interpolator Only	3.2 mA
Active Chip Area	0.43 mm^2
Technology	0.18 μm CMOS

CHAPTER 6

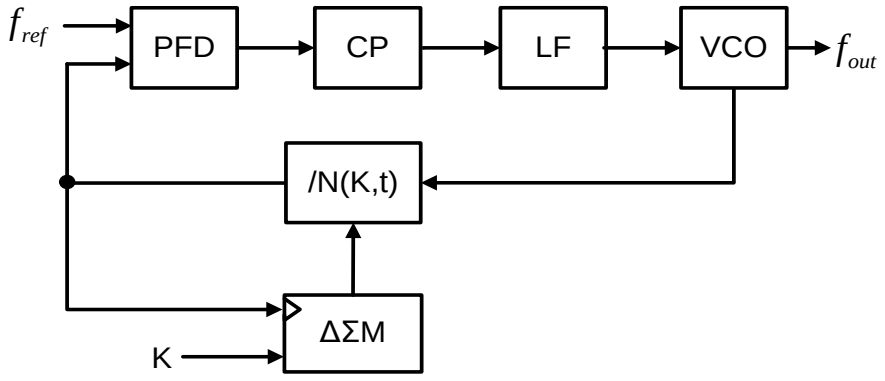
SUB-INTEGER-N PLL

6.1. Introduction

PLL-based frequency synthesizers are generally categorized into two configurations according to the relationship between the reference clock frequency and the output signal frequency: integer-*N* type and fractional-*N* type, as shown Figure 52. Basically, a frequency resolution of integer-*N* type PLLs is limited to the reference clock frequency. By contrast, fractional-*N* type PLLs can achieve a fine frequency resolution independent of the reference frequency by adopting a frequency divider with a time-varying modulus.



(a)



(b)

Figure 52. General PLL architectures of (a) integer-*N* type (b) fractional-*N* type.

Obviously, there exist tradeoffs between these two types of PLLs [18]. Integer-*N* PLLs have advantages on their simple structures and ideally few spurs, but the large division factor impairs in-band phase noise performance for high frequency resolution. In addition, since the loop bandwidth is limited less than one tenth of the reference frequency for stability [1], phase noise from a voltage-controlled oscillator (VCO) cannot be suppressed enough by a loop filter, and the settling time increases when a fine frequency resolution is required. By contrast, fractional-*N* PLLs partially solve those problems of integer-*N* PLLs by removing the dependency on the reference frequency of the output frequency resolution, but fractional spur reduction or dithering techniques such as a delta-sigma ($\Delta\Sigma$) modulation considerably increase the system complexity.

For certain applications, the channel resolution is not so tight that a fractional-*N* PLL employing a $\Delta\Sigma$ modulation scheme is necessary. However, to achieve a fractional frequency resolution while maintaining a wide loop bandwidth is still desirable. To satisfy this requirement, a concept of a sub-integer-*N* PLL has been suggested that utilizes a time-invariant divider providing a sub-integer division ratio [47].

In this research, a novel frequency synthesizer architecture realizing a high frequency resolution using a single side-band (SSB) mixer and a mathematical concept of relatively prime without a fractional-divider is investigated. Thus, the proposed PLL maintains simplicity of an integer-*N* type PLL while achieving a high frequency resolution. To fully integrate the proposed PLL in a compact chip area, a delay locked loop (DLL)-based frequency multiplier and a saturation-type ring VCO are proposed. In the frequency multiplier, each sub-pulse is generated from one corresponding unit delay cell, compared to other architectures using two consecutive delay cells for generating one sub-pulse [12],

[48], [49]. Therefore, various multiplication factors can be obtained with a small number of delay stages. In addition, power dissipation for generating pulses is reduced because the pulse generator consists of purely D flip flops (DFFs) and inverters operating only when triggered in their turn. Since only the required sub-pulses are generated from the pulse generator for a target output signal frequency, an additional pulse selection process in conventional frequency multipliers has been eliminated.

In the VCO design, a ring-type was adopted rather than LC-type considering system requirements: quadarature signal phases, a wide frequency tuning range, and a small chip area. Meanwhile, the utilization of a saturated-type delay cell and a latch configuration allowed for achieving the good phase noise performance.

6.2. Concept of the Sub-Integer-N PLL

To achieve high frequency resolution without a fractional divider, offset-frequency PLL architectures with a SSB mixer, which mixes a main PLL signal with a high resolution signal, have been suggested [4]-[8]. However, dual-loop architectures require multiple PLLs and additional reference sources, which considerably increase power consumption, cost, and chip area [4]-[6]. Furthermore, they are not able to reduce the overall settling time since it is defined by a narrower loop-PLL that determines the minimum frequency resolution. Architectures of [7], [8] require large power consumption and area because they involve a direct digital synthesizer (DDS).

The proposed frequency synthesizer adopts a single reference source for both the VCO outputs, f_{out}, and offset-frequency signals, f_{mix}. Each offset-frequency signal is generated from the frequency multiplier based on the DLL operating in the locked condition. When

the DLL is locked, the voltage controlled delay line (VCDL) in the DLL continuously provides evenly spaced edges. The change of f_{mix} takes just switching time of the edge selection process. Thus, the frequency multiplier does not limit the settling time of the overall system. In addition, the DLL-based frequency multiplier presents advantages on good phase noise performance, robustness under PVT variation, and a compact loop filter design over an additional PLL [50].

In the proposed frequency synthesizer, the frequency resolution is not determined by the resolution of f_{mix} as in conventional offset-frequency PLLs [4]-[8]. Instead, high frequency resolution is achieved by utilizing the mathematical relationship between the reference frequency, f_{ref}, and offset-frequency, f_{mix}. If a f_{ref} is selected in the form of $a + 0.1b$ when a and b denote the digits in the integer part and the fractional part of f_{ref}, respectively, the proposed frequency synthesizer can achieve the frequency resolution of $0.1b$, which is a fractional part of f_{ref}. Since the frequency resolution is not restricted by the offset-frequencies of f_{mix}, the proposed architecture could adopt high frequencies as f_{mix}. Thus, undesirable spurs from leakages and mismatches from the SSB mixer can be suppressed enough by the loop filter without any additional compensation techniques.

Figure 53 shows the concept of the proposed frequency synthesizer. The output frequency resolution of the proposed frequency synthesizer as a fractional part of the reference frequency can be verified as followings. When N_1 and N_2 are non-negative integers and especially N_1 is one-digit, the division number of N can be represented as $10N_2 + N_1$. Then, the output signal frequency, f_{out}, can be expressed as below.

$$f_{out} = f_{ref} \cdot N \pm f_{mix} \tag{18}$$

$$= (a + 0.1b) \cdot N \pm f_{mix} \tag{19}$$

$$= (a + 0.1b) \cdot (10N_2 + N_1) \pm f_{mix} \tag{20}$$

$$= (10a + \ b) \cdot N_2 + a \cdot N_1 + 0.1b \cdot N_1 \pm f_{mix}. \tag{21}$$

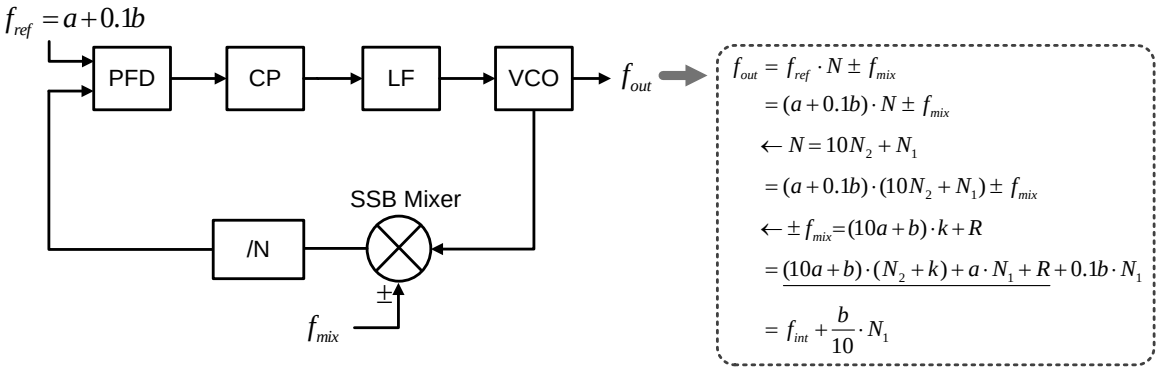


Figure 53. Conceptual architecture of the proposed frequency synthesizer.

Based on the Quotient-Remainder theorem [51], f_{mix} can be substitute with the form as (22) when k and R denote the quotient and the remainder. Subsequently, (21) can be restated as in (23).

$$\pm f_{mix} = (10a + b) \cdot k + R \tag{22}$$

$$f_{out} = \underline{(10a + b) \cdot (N_2 + k) + a \cdot N_1 + R} + 0.1b \cdot N_1 \tag{23}$$

Thus, if f_{mix} frequencies are chosen to have R covering every integer from 0 to $10a+b-1$ in (22), the integer part of the output frequency which is underlined can have any positive integer value with proper combination of k [52]. Finally, the output frequency, f_{out}, can be restated into (24) when the integer part is substituted with f_{int} representing any positive integer number.

$$f_{out} = f_{int} + \frac{b}{10} \cdot N_1 \tag{24}$$

As a result, the proposed frequency synthesizer can generate every output frequency with a resolution of $b/10$ by controlling the first digit number of the division factor, N_1.

6.3. Implementation of the Sub-Integer-N PLL

As shown in the derivation of the previous section, in order to allow the proposed frequency synthesizer for generating every output frequency with the frequency resolution of $b/10$, a set of f_{mix} should satisfy the condition that a corresponding set of R covers every integer from 0 to $10a+b-1$ in (23). Here, to generate a proper set of f_{mix}, the concept of relatively prime integers is introduced. Based on the theory of relatively prime ideals, following two propositions are observed [51]. First, if a set of f_{mix} consists of only relatively prime numbers of $10a+b$, and difference between any f_{mix} in the set is not multiple of $10a+b$, each f_{mix} provides unique remainder, R. Second, if one particular integer, f_{base}, is a relatively prime number of $10a+b$, all the multiples except $10a+b$ times of it are also relatively prime numbers of $10a+b$. Based on the first proposition, all the required R can be covered with minimum number of f_{mix} by selecting every f_{mix} as a relatively prime number of $10a+b$. Then, from the second proposition, this set of f_{mix} can be generated from one frequency multiplier having a reference frequency of f_{base} which is a relatively prime of $10a+b$. Therefore, $10a+b$ is set to 11, a prime number with a and b of 1, equally. When the frequency multiplier adopts f_{base} of 6 and multiplication factors, m, of 1,2,3,4 and 6 which are achievable from the only twelve delay cell stages in VCDL, (22) can be restated as

$$f_{mix} = f_{base} \cdot m = 6m = 11k + R \qquad (m = 0,1,2,3,4,6) \tag{25}$$

For *m* of zero, the frequency multiplier is disabled and provides no output signal. Figure 54 (a) shows all the required *R* from 0 to 10 can be obtained from this set of f_{mix} in (25) when f_{mix} is added to or subtracted from the VCO output frequency. After fixing the values of a and b, (23) can be reduced to

$$f_{out} = f_{ref} \cdot (N + 10k + R - \frac{R}{11}) \tag{26}$$

As a result, in (26), the proposed frequency synthesizer achieves the fractional resolution which is one eleventh of f_{ref}, since *R* can be changed from 0 to 10 in Figure 51 (a). Also, when all the frequency units are implemented in MHz, every output signal frequency with 0.1MHz frequency resolution can be generated despite adopting 1.1MHz reference frequency. Thus, using the proposed architecture, a PLL can have high frequency resolution without utilizing a fractional divider or mixing high resolution offset-frequency signals.

m	$+f_{mix}$	*k*	*R*	$-f_{mix}$	*k*	*R*
1	6	0	6	-6	-1	5
2	12	1	1	-12	-2	10
3	18	1	7	-18	-2	4
4	24	2	2	-24	-3	9
6	36	3	3	-36	-4	8
0	0	0	0	0	0	0

(a)

1. $f_{out}(MHz) = f_{int} + 0.1N_1$
2. $R = (f_{int} - N_1)\ \%\ 11$
3. f_{mix} *and k from fig.*3
4. $N_2 = \lfloor (f_{int} - N_1)\ \%\ 11 \rfloor - k$
5. $N = 10N_2 + N_1$
6. $f_{out}(MHz) = N \cdot f_{ref} \pm f_{mix}$

(b)

f_{out}(MHz)	*k*	*R*	N_2	N_1	*N*	f_{mix}(MHz)
561.0	0	0	51	0	510	0
561.1	-2	10	52	1	521	-12
561.2	-3	9	53	2	532	-24
561.3	-4	8	54	3	543	-36
561.4	1	7	49	4	494	+18
561.5	0	6	50	5	505	+6
561.6	-1	5	51	6	516	-6
561.7	-2	4	52	7	527	-18
561.8	3	3	47	8	478	+36
561.9	2	2	48	9	489	+24
562.0	1	1	50	0	500	+12

(c)

Figure 54. Formulae to obtain values for a target frequency, and examples to generate frequencies between 561.0MHz and 562.0MHz with the resolution of 0.1MHz when *ab* is set to 11.

Settings of N and f_{mix} for any given target frequency can be calculated from expressions in Figure 54 (b). For example, when the targeted output frequency, f_{out}, is 561.7MHz, the value of N and f_{mix}, can be obtained through following procedures:

$$1.\ f_{out}(MHz) = f_{int} + 0.1N_1$$
$$= 561.7 \ \Rightarrow\ f_{int} = 561,\ N_1 = 7$$

$$2.\ R = (f_{int} - N_1)\%11$$
$$= (561 - 7)\%11 = 4$$

$$3.\ f_{mix} = \underline{-18},\ k = -2$$

$$4.\ N_2 = \lfloor (f_{int} - N_1) \div 11 \rfloor - k$$
$$= \lfloor (561 - 7) \div 11 \rfloor + 2 = 52$$

$$5.\ N = 10 \cdot N_2 + N_1$$
$$= 10 \cdot 52 + 7 = \underline{527}$$

$$6.\ f_{out}(MHz) = N \cdot f_{ref} \pm f_{mix}$$
$$= \underline{527} \cdot 1.1\ \underline{-18}(MHz) = \underline{561.7}(MHz)$$

Thus, 561.7 MHz output frequency signal can be generated with the combination of the division number of 527 and f_{mix} of -18 MHz. Examples in the table of Figure 54 (c) show the generation of every frequency between 561.0MHz and 562.0MHz in this manner.

Figure 55 shows the implementation of the proposed architecture. In overall, the proposed sub-integer-N PLL consists of the integer-N third order type-II PLL, the frequency multiplier generating offset-frequencies and the SSB mixer to combine signals coming from former two blocks. The system adopts only one reference source. The

reference frequency for the main PLL loop is generated from the divider in front of the PFD, and all f_{mix} frequencies are obtained from the following frequency multiplier.

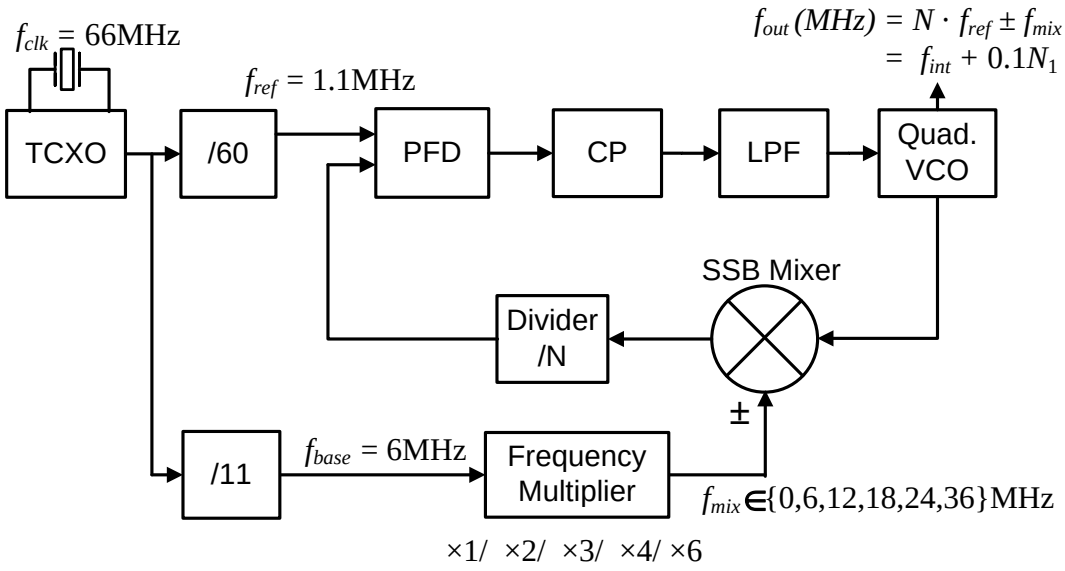


Figure 55. Block diagram of the proposed sub-integer-*N* PLL.

For frequency accuracy, a frequency multiplier was designed based on a DLL. The DLL is operating in locked condition and always provides 12 evenly spaced phases with a fixed frequency, f_{clk}. By combining phases selectively, any multiplication factor of 1, 2, 3, 4 or 6 can be obtained since 12 is a common multiple of these numbers. Since the selection of f_{mix} among six frequencies is performed only by the switching of the pulse collector, the system effectively maintains the single-loop characteristics.

6.4. Key Building Blocks

6.4.1. Implementation of the Sub-Integer-N PLL

Figure 56 shows the frequency multiplier consisting of a DLL, a pulse generator, and a pulse collector for generating required offset-frequency signals, f_{mix}. As shown, the proposed frequency multiplier is designed as a DLL-based configuration due to its strong advantages over conventional PLL-based counterparts: ; better phase noise performance, robustness on PVT variations, simple and compact loop filter, and fast settling time [50]. Since each f_{mix} is generated by selectively combining phases from the DLL in locked condition, the frequency change takes just a switching time, thus, impacts little on the overall settling time. Hence, the system can maintain single-loop system characteristics.

Generally, in conventional DLL-based frequency multipliers, two consecutive delay

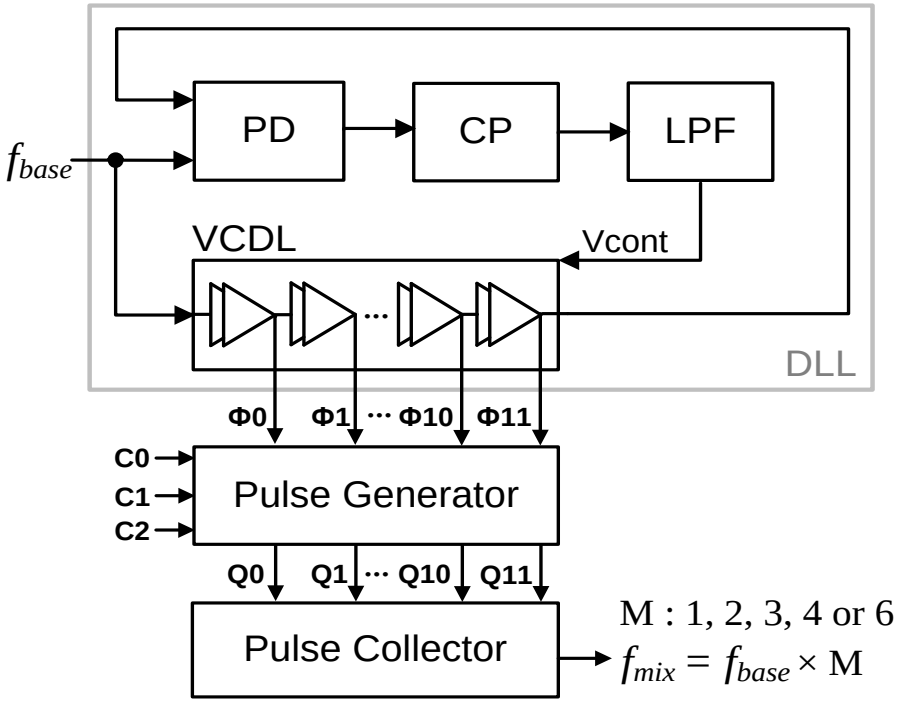


Figure 56. Block diagram of the frequency multiplier for generating offset- frequency signals, f_{mix}..

cells are utilized for generating one sub-pulse [11], [48], [49]. However, in the proposed architecture, each sub-pulse to be combined is generated from corresponding one unit delay cell. Therefore, a various multiplication factors can be obtained with the same number of delay cells in VCDL. In addition, power dissipation for generating pulses is minimized because the pulse generator consists of purely DFFs and inverters operating only when triggered in their turns. In addition, since only the required sub-pulses are generated from the pulse generator for a target output signal frequency, an additional pulse selection process in conventional frequency multipliers has been eliminated.

In Figure 56, when the DLL consisting of a phase detector, a charge pump VCDL, and a loop filter is locking to the reference signals, the VCDL generates uniformly-spaced 12 differential phase-shifted signals. Then, the pulse generator detects the rising edge of the only selected phase-shifted signals among 12 streams according to 3-bit control signals, C_0, C_1 and C_2, and creates a short pulse from each selected signal. Subsequently, the pulse collector combines these short pulses, and provides a clock with a multiplied frequency, f_{mix}. Figure 57 details these operations of the pulse generator and the pulse collector. When the phase shifted signal from the VCDL, Φ_k, enters to the corresponding k^{th} DFF, Q_k goes high if the value in the D node, S_k, is set to 1. In the meantime, Qb_k goes low and resets Q_k by triggering the RSTb node. Since this reset process takes two-inverter delay time, a short pulse of duration, $\Delta\tau$, is generated at Q_k. Finally, the subsequent pulse collector combines these pulses. In order to create only the required pulses, each S_k is set to either 0 or 1 according to the programmed 3-bit signals. Thus, five multiplication factors – 1,2,3,4, and 6 - can be selected by changing the combination of the programmed 3-bit signals.

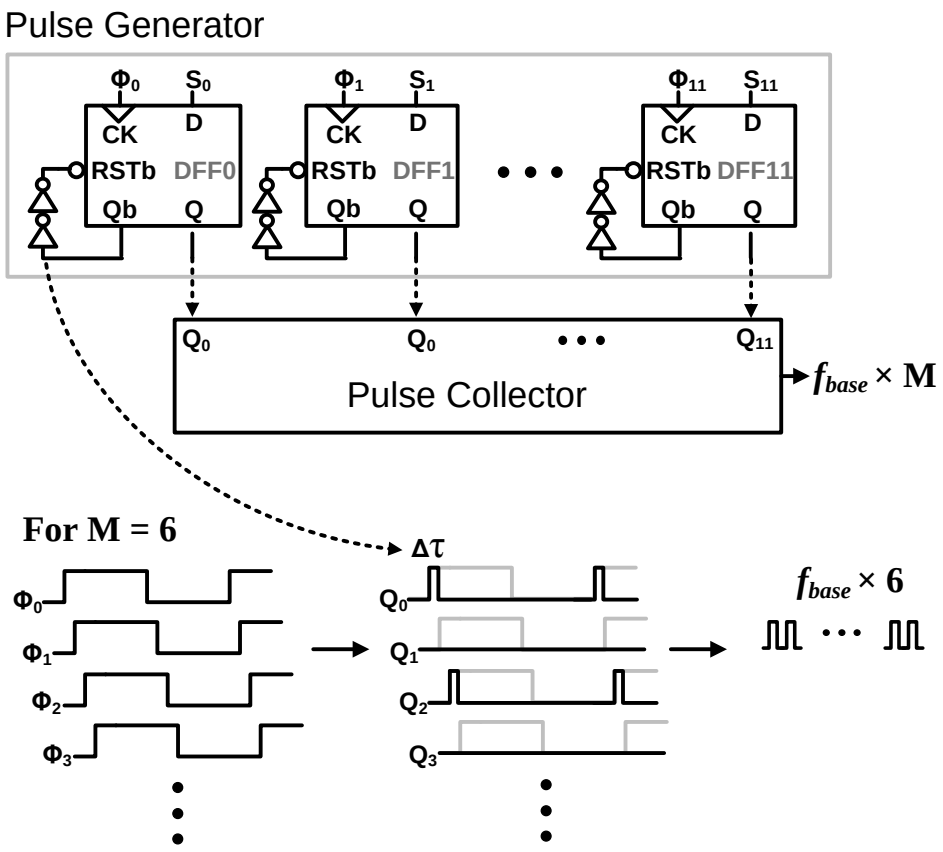


Figure 57. Operation of the frequency multiplier.

6.4.2. Ring VCO

Traditionally, LC-VCOs have been dominantly utilized for generating signals in PLLs due to their superiority on phase noise performance [14], [22]. However, the limited tuning range of the LC-VCO, usually less than 20%, makes itself vulnerable to process variations. In addition, adopting an inductor with a high quality factor considerably increases the chip area and cost considerably. Furthermore, in a system requiring multiple output phases, additional circuits, such as I/Q generators, increase the system complexity. By contrast, ring VCOs are capable of generating wide-range frequency signals with multiple output phases without any supplementary circuits. Most importantly, the ring VCOs without

inductors can be implemented in a small die area. Thus, in this work, a ring type oscillator has been considered in order to integrate a VCO generating quadarature output signals for the SSB mixer in compact chip area.

For improving the poor phase noise performance [15], [19], the proposed oscillator adopted a saturated-type delay cell with a latch configuration. The schematics of the proposed delay cell and the 4-stage ring oscillator are shown in Figure 58. The delay cell consists of an NMOS and a PMOS input pairs, a NMOS and a PMOS latches, and two NMOSs for changing the strength of the PMOS latch by the control voltage from the loop filter. In order to reduce the frequency gain (K_{VCO}) for enhancing the stability of the PLL system and suppressing the reference spur level, frequency bands were divided using MIM cap banks connected to the control voltage node.

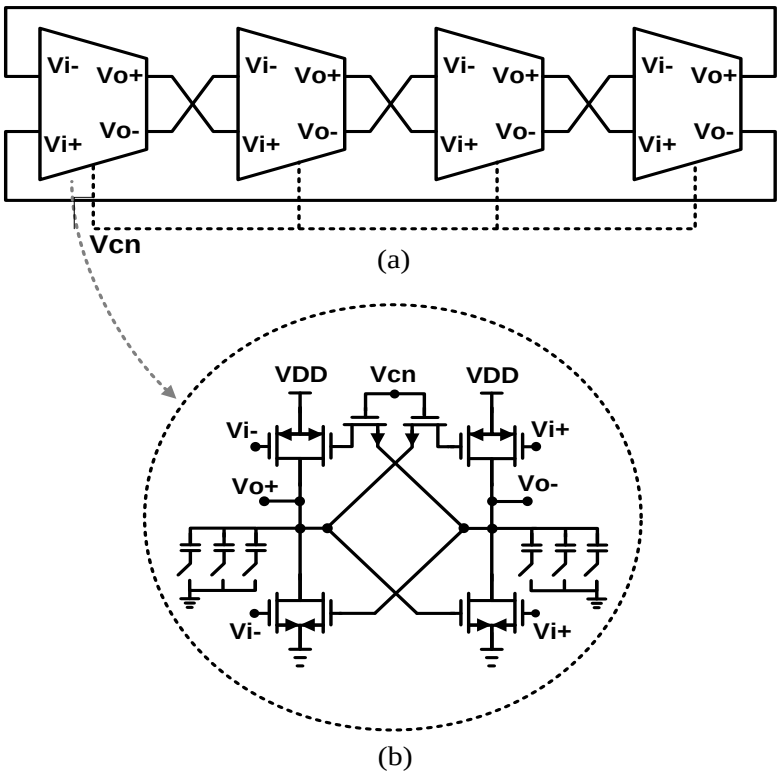


Figure 58. Proposed saturated-type ring oscillator (a) unit delay cell (b) 4-stage ring oscillator.

The whole ring oscillator was composed by 4-stage delay cells considering the trade-off between the frequency tuning range, phase noise, and power consumption. Thus, the VCO can provide evenly-spaced eight phases including quadrature signals required for providing quadarature LO signals for the subsequent SSB mixer.

In the proposed delay cell, the signal obtains fast-switching edges by the cross-coupled PMOS and NMOS latches. When the signal is injected, the latches operate in the direction of opposing the signal transition. However, after a while, the function of the latches changes into positive feedbacks and accelerates the signal transition. In addition, due to the saturated-type configuration eliminating the tail transistor, the proposed delay cell allows for rail-to-rail output swing.

Qualitatively, the fast-switching transition and the rail-to-rail swing imply shorter duration for transistors being turned-on. The more time transistors are turned-on, the more thermal noise current is generated from those devices. Hence, the fast rail-to-tail switching operation can intrinsically improve phase noise performance [23]. Phase noise performance of the proposed delay cell also can be explained based on the noise analysis equation of ring oscillators [15]:

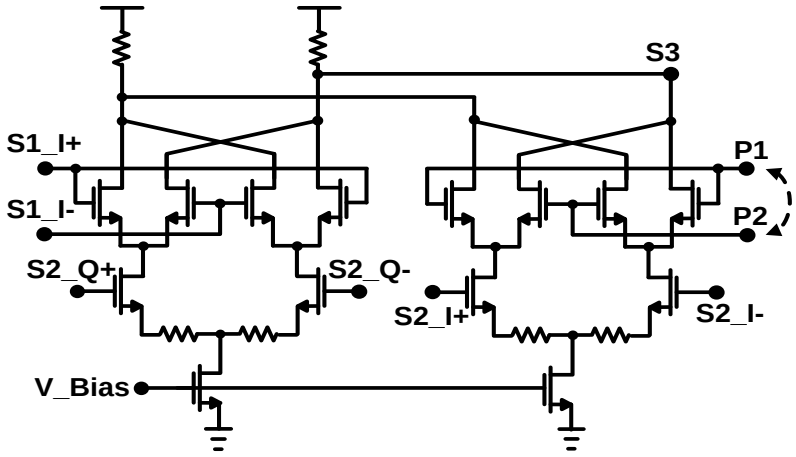
$$L(\Delta\omega) = \frac{512F \cdot kT \cdot R \cdot V_{DD}}{27\pi \cdot V_{PP}^{\ 3}} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \quad for \;\; V_{PP} >> V_{DD}$$
$$where\, V_{PP} = 2\frac{SR_{\max}}{\omega_o} \tag{27}$$

where F, $SR_{\max}$, $\Delta\omega$, ω_o, kT, V_{DD}, and R are the excess noise factor, the maximum output slew rate, the angular frequency offset from the center frequency, the center frequency, the thermal energy, the power supply voltage, and the equivalent output resistance of a delay cell, respectively. Because fast rail-to-rail signal transition increases the maximum slew

rate of the signal and V_{PP} , the proposed delay cell can achieve good phase noise performance according to (27). Furthermore, since 1/f noise is mainly contributed by bias devices, 1/f noise can be reduced by eliminating the tail transistor. Hence, the proposed ring VCO can achieve better phase noise performance compared to conventional ones.

6.4.3. SSB Mixer

In Figure 59, the SSB mixer consists of two cross-connected Gilbert cell mixers. In Fig.8, S1_I+, S1_I-, S1_Q+, and S1_Q- represent four quadarature signals from the VCO with operating frequency, f_{out}. S2_I+, S2_I-, S2_Q+, and S2_Q- are four quadarature signals from the frequency multiplier with operating frequency, f_{mix}.



	$f_{mixed} = f_{out} + f_{mix}$	$f_{mixed} = f_{out} - f_{mix}$
P1	S1_Q+	S1_Q-
P2	S1_Q-	S1_Q-

Figure 59. Structure of the SSB mixer changing the polarity for choosing lower side.

In the mixer, either of frequency addition or subtraction can be selected simply by exchanging the polarities of the signals applied to P1 and P2. Hence, for obtaining output signal with the frequency of f_{mixed} as a sum of f_{out} and f_{mix}, S1_Q+ and S1_Q- are put into P1 and P2, respectively. Conversely, output signal with the subtracted frequency can be achieved simply by reversing the connections between ports and signals.

In practice, signal leakages or the remaining image signal of the SSB mixer could result in spurs. However, levels of spurs are naturally suppressed because they occur far out of the loop bandwidth by adopting high offset-frequencies, f_{mix}. Thus, without any supplementary technique to reduce them, the proposed architecture is robust to those spurs mentioned above.

6.4.4. Loop Filter Design

For implementing third order type II PLL, a passive second order loop filter has been designed, which has a transfer function as below:

$$F(s) = \frac{1}{s(C_1 + C_2)} \cdot \frac{1 + sR_1C_1}{1 + sR_1C_k},\ C_k = \frac{C_1C_2}{C_1 + C_2} \tag{28}$$

Adopting this loop filter, the open loop transfer function of the main PLL can be expressed as followings:

$$\begin{aligned} GH(s) &= K_{pi} \cdot \frac{1}{s(C_1 + C_2)} \cdot \frac{1 + sR_1C_1}{1 + sR_1C_k} \cdot \frac{K_v}{s} \cdot \frac{1}{N} \\ &= \frac{K_{pi} \cdot K_v}{N(C_1 + C_2)s^2} \cdot \frac{\frac{s}{w_Z} + 1}{1 + \frac{s}{w_P}},\ w_z = \frac{1}{R_1C_1}, w_p = \frac{1}{R_1C_k} \end{aligned} \tag{29}$$

where K_{pi}, K_v, and N are the PFD/CP gain, the VCO gain, and the division factor of the PLL. When assuming the zero and the pole locate equally from unity gain frequency, w_x, by $A_{XZ,}$ from (12), w_x can be expressed as following equations.

$$Mag(GH) = \left| \frac{K_{pi} \cdot K_v}{N \cdot (C_1 + C_2) \cdot w^2{}_x} \cdot A_{XZ} \right| \rightarrow w_X = \sqrt{\frac{A_{XZ} \cdot K_{pi} \cdot K_v}{N \cdot (C_1 + C_2)}},$$

$$w_P = w_X \cdot A_{XZ}, \quad A_{XZ} = \frac{w_X}{w_Z} \tag{30}$$

In (13), the tradeoff between stability and settling time exists according to the value of A_{XZ}. Thus, if choosing a high value of or upper-side mixed frequency A_{XZ}, stability will be enhanced with the phase margin, but, settling time will be increased. Considering the tradeoff, A_{XZ} is set as 3.2 for the phase margin of 55 degree. Finally, based on the system parameters, each passive value in the loop filter can be obtained from following equations.

$$R1 = \frac{w_X \cdot N \cdot A_{XZ}{}^2}{K_{pi} \cdot K_v \cdot (A_{XZ}{}^2 - 1)} \tag{31}$$

$$C1 = \frac{K_{pi} \cdot K_v \cdot (A_{XZ}{}^2 - 1)}{w_X{}^2 \cdot N \cdot A_{XZ}} \tag{32}$$

$$C2 = \frac{K_{pi} \cdot K_v}{w_X{}^2 \cdot N \cdot A_{XZ}} \tag{33}$$

6.5. Measurement Results

The proposed frequency synthesizer was fully integrated with an on-chip loop filter and a ring VCO in a 0.18μm CMOS technology.

Figure 60 shows the waveforms of six offset frequencies, f_{mix}, – 6 MHz, 12 MHz, 18 MHz, 24MHz, and 36MHz. In Figure 57, each waveform has a triangular shape because they passed through the low-pass filter with a variable cutoff frequency for reducing harmonic levels before entering into the SSB mixer. These offset frequency signals are generated from the DLL-based frequency multiplier rather than PLL-based counterpart. Therefore, chip area and power consumption were dramatically saved while achieving good phase noise performance. The frequency multiplier takes only 350μm × 140μm and consumes less than 3 mA.

Figure 61 shows the SSB phase noise of 24 MHz offset frequency signal from the proposed DLL-based frequency multiplier. The phase noise performance is -113.5 dBc and -121.4 dBc at 10 kHz and 100 kHz offset, respectively.

Figure 62 presents the oscillating frequency of the proposed ring VCO. The proposed VCO achieved wide frequency tuning range from 420 MHz to 850 MHz with maintaining linear voltage-frequency characteristics. In addition, by adopting the MIM capacitor bank controlled by 3-bit signals, the VCO keeps the VCO gain low. Furthermore, by adopting the proposed saturated-type ring oscillator, the PLL achieved a good phase noise performance without sacrificing the chip area occupancy.

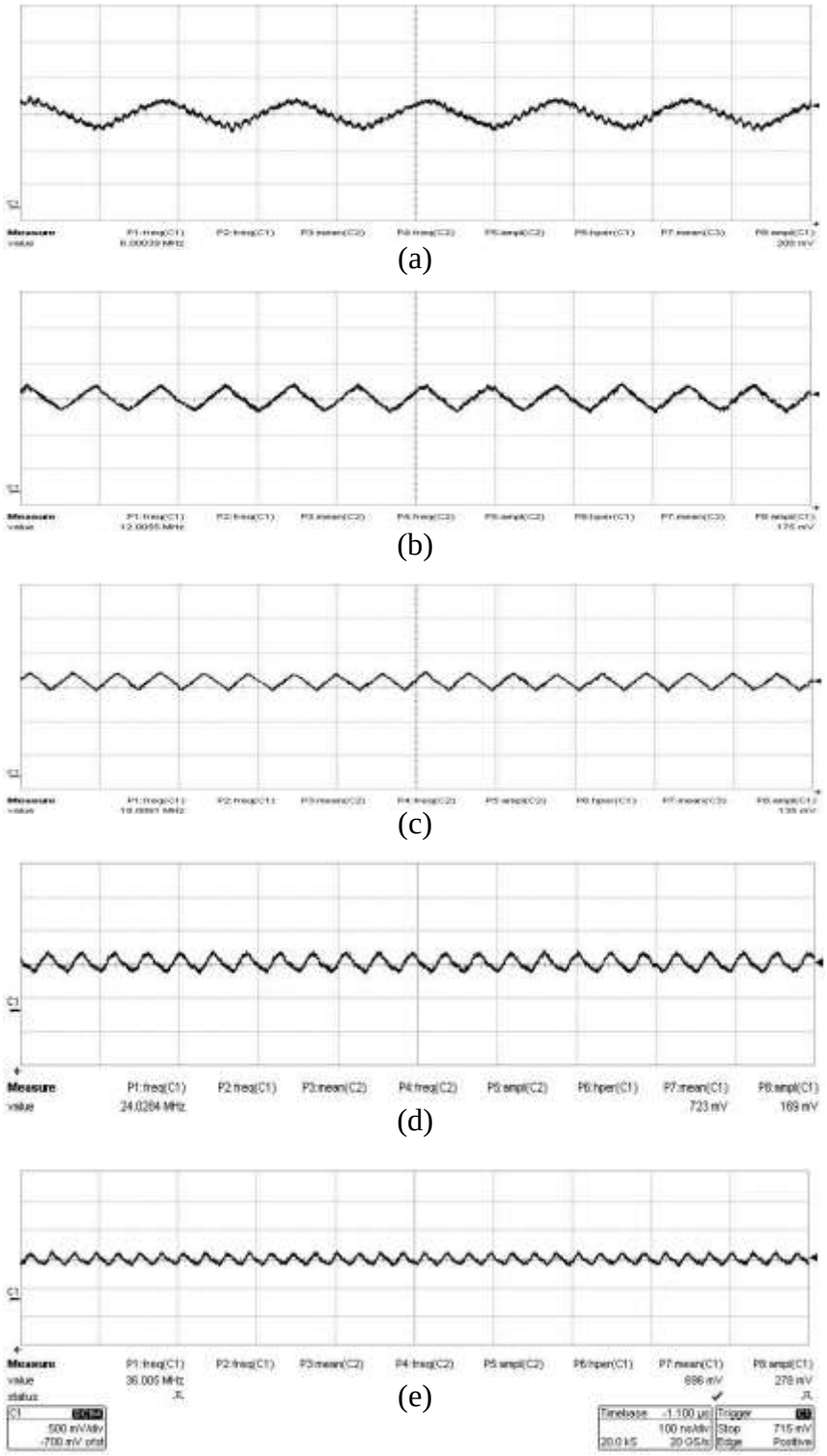


Figure 60. Measured waveforms of f_{mix} from the proposed frequency multiplier (a) 6 MHz (b) 12 MHz (c) 18 MHz (d) 24 MHz (e) 36 MHz.

Signal Freq:	24.000825 MHz	1 kHz	-101.96 dBc/Hz
Signal Level:	-9.21 dBm	10 kHz	-113.54 dBc/Hz
Signal Freq Δ:	-0.28 Hz	100 kHz	-121.41 dBc/Hz
Signal Level Δ:	-0.01 dBm	1 MHz	-128.52 dBc/Hz

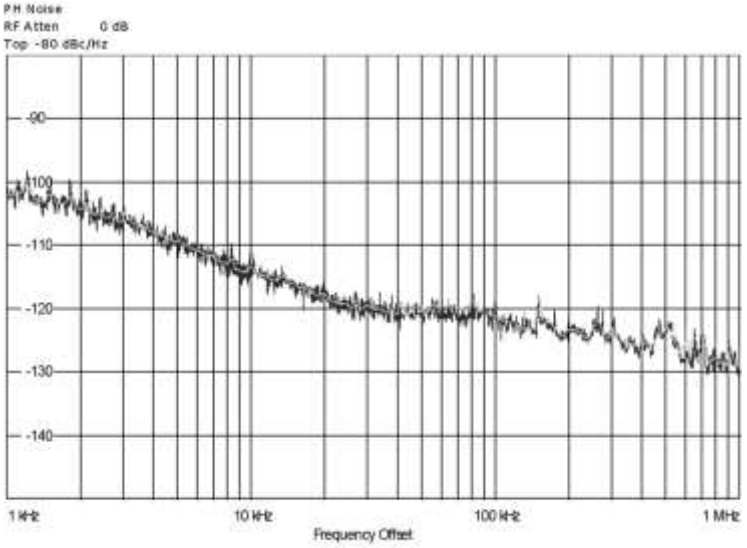


Figure 61. Measured SSB phase noise of the proposed frequency multiplier when f_{mix} = 24 MHz.

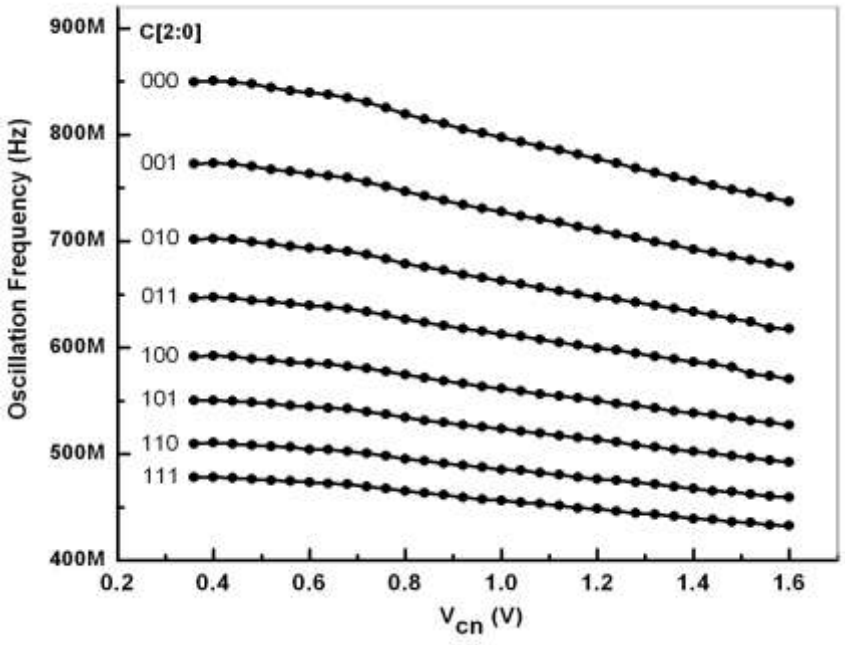


Figure 62. Measured frequency tuning range of proposed VCO.

Figure 63 presents the measured phase noise of the proposed frequency synthesizer when 599.5 MHz output signal is generated, which are -80.1 dBc/Hz and -112.2 dBc/Hz at 100 kHz and 1 MHz offset, respectively. Phase noise of the signal from the frequency multiplier is much less than that from the oscillator, which little affects the overall phase noise performance of the proposed PLL.

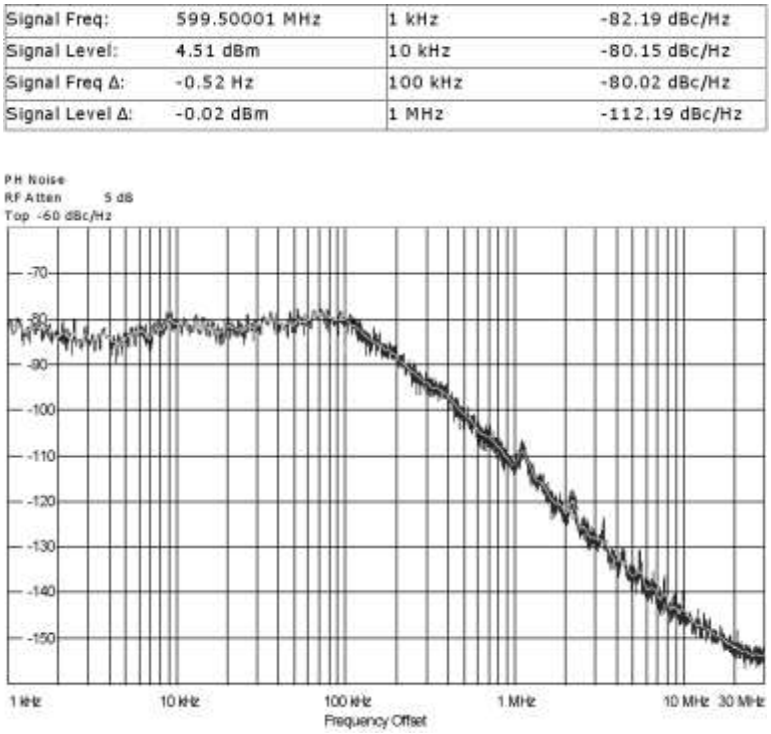


Figure 63. Measured SSB phase noise of the proposed frequency synthesizer when the output frequency is 599.5 MHz.

Figure 64 presents the frequency spectrum of the PLL output signal which shows -54 dBc reference-spur level locating 1.1 MHz offset. As shown in the die micrograph of Figure 65, the active area is 580μm × 500μm, and the current consumption is 15.7 mA from a 1.8V supply. Additional circuits for fractional-resolution including the divide-by-11 divider, the multiplier and the SSB mixer occupy just one fifth of the total area and consume less than 3 mA.

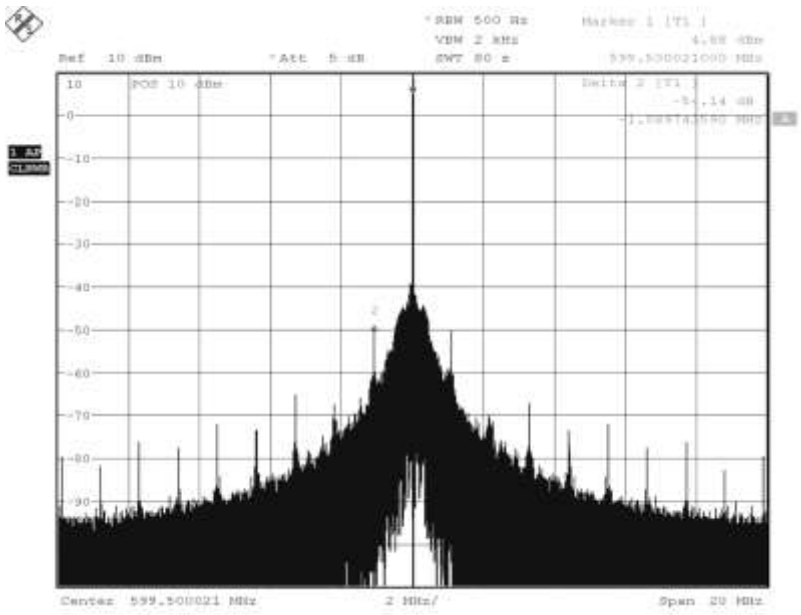


Figure 64. Measured frequency spectrum of the proposed frequency synthesizer when the output frequency is 599.5 MHz.

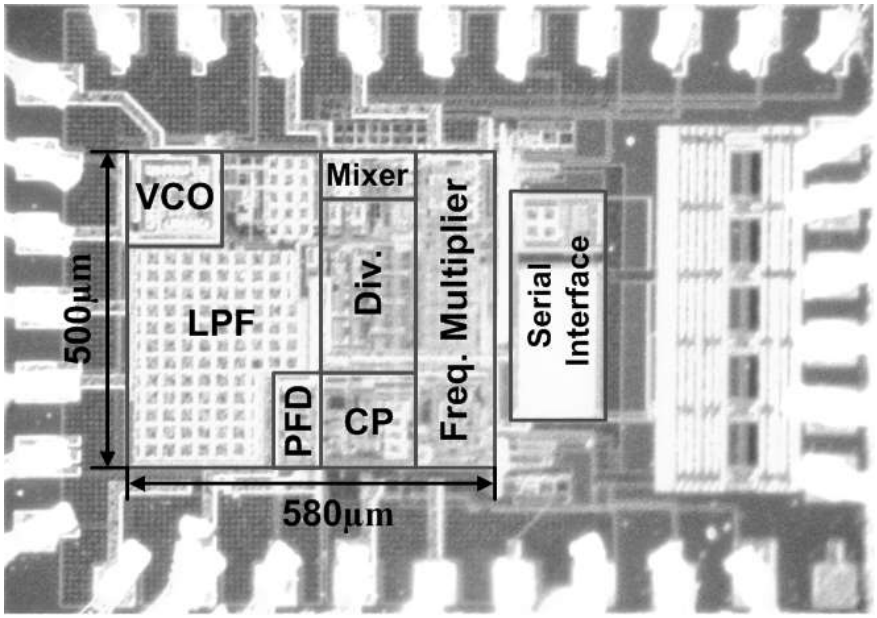


Figure 65. Micrograph of the proposed sub-integer-*N* frequency synthesizer.

Table 4 compares the performance of the proposed sub-integer-N PLL with those of previous dual-loop offset-frequency PLL architectures. Compared to previous works, the proposed architecture adopts only one loop and reference frequency source. Since offset frequency signals are generated from the multiplier rather than additional PLL loop, the bandwidth of the system was extended independent of the frequency resolution. The power consumption is also smaller than the prior works. In addition, due to the proposed low phase noise ring VCO and the DLL-based frequency multiplier, the core chip area was minimized dramatically with maintaining good phase noise performance.

Table 4. Performance comparison with offset-PLLs in prior works

	[7]	[8]	[9]	[11]	This Work
Architecture	Dual-Loop	Dual-Loop	Dual-Loop	DDFS-PLL	Sub-Integer-*N*
VCO Type	LC VCO	LC VCO/Ring VCO	Ring VCO	LC VCO	Ring VCO
No. of Clock Source	2	2	1	2	1
Clock Frequency	1.6 MHz / 205 MHz	800 kHz / 100 kHz	256 MHz	200 MHz / 74 MHz	66 MHz
Frequency Resolution	200 kHz	200 kHz	1 MHz	1 MHz	100 kHz
Loop Bandwidth	40 kHz / 27 kHz	120 kHz / 42 kHz	2 kHz / 4 MHz	1 MHz	120 kHz
Carrier Frequency	900 MHz	1.8 GHz	2.4 GHz	2.5 GHz	600 MHz
Active Chip Area	2.64 mm^2	2 mm^2	3.7 mm^2	5.12 mm^2	0.29 mm^2
Power Consumption	34 mW	95 mW	49.5 mW	*169 mW	28.3 mW
Phase Noise (@600 kHz)	-121.8 dBc/Hz	-112 dBc/Hz	-97 dBc/Hz	-103 dBc/Hz	-104 dBc/Hz
Process	0.5 μm CMOS	0.5 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Power Supply	2 V	2 V	3.3 V	3 V / 2 V	1.8 V

* Except the GFSK modulator

6.6. Conclusions

In this research, a sub-integer-*N* PLL realizing a high frequency resolution using a SSB mixer and a mathematical concept of relatively prime without a fractional-divider is presented. In implementation, the proposed frequency synthesizer achieved 0.1 MHz output frequency resolution while adopting 1.1 MHz reference frequency, which means 11 of the fractional factor. Therefore, compared to a conventional integer-*N* PLL targeting the

same output frequency resolution, the settling time was reduced by more than ten times due to the increased loop bandwidth. In addition, in-band phase noise performance was enhanced since the required division factor for the target frequency was lowered. Moreover, with another combination of a, b and, f_{mix}, the architecture can be extended to have an even higher fractional factor. When compared to conventional offset-frequency PLL architectures, the proposed architecture shows strong advantages on cost, chip area, and power consumption because it utilizes only one reference source, and offset-frequency signals are generated from the DLL-based frequency multiplier instead of an additional PLL or a DDS. Additional blocks for a fractional resolution including the frequency multiplier and the SSB mixer take only fifth of the total area and consume less than 3 mA. In addition, using the proposed ring VCO, the whole frequency synthesizer was fully-integrated in a very small chip area while maintaining good phase noise performance. The total active area occupies only 500 μm × 580 μm and consumes 15.7 mA from 1.8 V supply.

CHAPTER 7

CONCLUSIONS

As a key building block of a wireless transceiver, a frequency synthesizer plays important roles to define system performances, such as an operating frequency range, a settling time, phase noise and spur performance, and area/power consumption. Furthermore, the trend of integrating multi-standards mobile systems into one chip makes frequency synthesizer design more challenging. In particular, this dissertation focuses on three challenges, including the problem of large area consumption of passive components, the inherent reference-spur problem, and trade-offs between integer-N PLLs and fractional-N PLLs. This dissertation consists of three main contributions.

First, new techniques and design methodology are introduced for efficiently saving silicon real-estate occupied by passive components of a conventional PLL-based frequency synthesizer. A novel ring-oscillator, achieving both of good phase noise performance and a wide tuning-range, is introduced to replace an LC-VCO. By adopting the transmission gate for delay cells in a saturated-type oscillator, the VCO presents phase noise of -113 dBc/Hz at a 1 MHz offset from a 800 MHz output signal and 190 % tuning range. For minimizing the size of the zero-making capacitor in a loop filter, a new capacitor-multiplication technique is proposed. Based on a current-mode capacitor-multiplier topology, the proposed architecture achieved a multiplication factor of 65 with 100 μA current consumption. Thus, the zero-making capacitor of 516.8 pF was implemented with a 7.95 pF on-chip-MIM capacitor, and the total area of the loop filter was dramatically minimized. In addition, a programmable DLL-based frequency multiplier has been presented for

replacing a conventional PLL-based frequency synthesizer. Based on the proposed pulse generating scheme, the proposed frequency multiplier provides a high multiplication factor of up to 24 while consuming only 16.2 mW when generating a 2.16 GHz output signal. The phase noise performance is -88.7 dBc/Hz and -99.8 dBc/Hz at 10 kHz and 100 kHz offsets from the operating frequency of 1.2 GHz, respectively.

Second, the dissertation analyzes the charge distribution mechanism for suppressing reference spurs, and presents its practical implementation. The proposed architecture is based on the DLL-based edge interpolator. Due to the charge distribution mechanism on the control voltage of the VCO, the proposed architecture is capable of suppressing the high-order harmonics of the reference spur as well as the fundamental reference spur. In measurement, the fundamental spur was suppressed more than 16 dB compared to the case when the interpolator was disabled.

Third, a new architecture for removing tradeoffs between integer-N PLLs and fractional-N PLLs is investigated. Then, a sub-integer-*N* PLL realizing a high frequency resolution using a SSB mixer and a mathematical concept of relatively prime without a fractional-divider is presented. In implementation, the proposed frequency synthesizer achieved 0.1 MHz output frequency resolution while adopting 1.1 MHz reference frequency, which means 11 of the fractional factor. Therefore, compared to a conventional integer-*N* PLL targeting the same output frequency resolution, the settling time was reduced by more than ten times due to the increased loop bandwidth. In addition, in-band phase noise performance was enhanced since the required division factor for the target frequency was lowered. When compared to conventional offset-frequency PLL architectures, the proposed architecture shows strong advantages on cost, chip area, and

power consumption because it utilizes only one reference source, and offset-frequency signals are generated from the DLL-based frequency multiplier instead of an additional PLL or a DDS.

REFERENCES

[1] F. M. Gardner, “Charge-pump phase-lock loops,” *IEEE Transactions on Communication*, vol. COM-28, no. 11, pp. 1849-1858, Nov. 1980.

[2] T.A.D. Riley, M.A. Copeland, and T.A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE Journal of Solid-State Circuits*, vol.28, no.5, pp.553-559, May 1993.

[3] B. Miller and B. Conley, “A Multi-modulator Fractional Divider,” *in Annual Frequency Control Symposium*, vol. 44, pp. 559–567, 1990.

[4] W.S.T. Yan and H.C. Luong, "A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers," *IEEE Journal of Solid-State Circuits*, vol.36, no.2, pp.204-216, Feb. 2001.

[5] T. Kan, et al., “A 2-V 1.8-GHz Fully Integrated CMOS Dual-Loop Frequency Synthesizer,” *IEEE J. Solid State Circuits*, vol. 37, no.8, pp. 1012-1020, Aug. 2002.

[6] Zhinian Shu, Ka Lok Lee, and B.H. Leung, "A 2.4-GHz ring-oscillator-based CMOS frequency synthesizer with a fractional divider dual-PLL architecture," *IEEE Journal of Solid-State Circuits*, vol.39, no.3, pp. 452-462, Mar. 2004.

[7] A. Bonfanti, et al., "A DDS-based PLL for 2.4-GHz frequency synthesis," *IEEE Transactions on Circuits and Systems I*, vol.50, no.12, pp. 1007-1010, Dec. 2003.

[8] A. Bonfanti, et al., "A 2.5-GHz DDFS-PLL With 1.8-MHz Bandwidth in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol.43, no.6, pp.1403-1413, Jun. 2008.

[9] G. Chien and P. R. Gray, “A 900-MHz local oscillator using a DLL based frequency multiplier technique for PCS applications,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1996–1999, Dec. 2000.

[10] D.J. Foley and M.P. Flynn, "CMOS DLL-based 2-V 3.2-ps jitter 1-GHz clock synthesizer and temperature-compensated tunable oscillator, " *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp.417-423, Mar. 2001.

[11] R. Farjad-Rad, et al., “A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1804–1812, Dec. 2002.

[12] C. Kim, I. Hwang, and S.M. Kang, “A low-power small-area 7.28 ps jitter 1 GHz DLL-based clock generator,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1414–1420, Nov. 2002.

[13] J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer," *IEEE Journal of Solid-State Circuits*, vol.33, no.12, pp.2054-2065, Dec. 1998.

[14] J. Craninckx and M. Steyaert, “A 1.8GHz low-phase noise CMOS VCO using optimized hollo spiral inductors,” *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 736-744, May 1997.

[15] Liang Dai and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *IEEE Transactions on Circuits and Systems II*, vol.49, no.5, pp. 328-338, May 2002.

[16] K. Shu, et al., “A 2.4-GHz onolithic Fractional-N Frequency Synthesizer With Robust Phase-Switching Prescaler and Loop Capacitance Multiplier,” *IEEE Journal of Solid-State Circuits*, Vol. 38, no. 6, pp. 866–874, Jun. 2003.

[17] B. Razavi, “Challenges in the design of frequency synthesizers for wireless applications,” *IEEE Custom Integrated Circuits Conference*, pp. 395–402, May 1997.

[18] F. M. Gardner, Phaselock Techniques. Hoboken, NJ: Wiley, ch. 15. 2005.

[19] C. Park and B. Kim, “A Low-Noise 900MHz VCO in 0.6 m CMOS”, *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 586-591, May 1999.

[20] I. Hwang, C. Kim, S.M. Kang, “A CMOS self-regulating VCO with low supply sensitivity”, *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 42-48, Jan. 2004.

[21] Meng-Lieh Sheu, Ta-Wei Lin, and Wei-Hung Hsu, “Wide frequency range voltage controlled ring oscillators based on transmission gates”, *IEEE International Symposium on Circuits and Systems*, Vol. 3, pp. 2731- 2734, May 2005.

[22] B. Razavi, “A Study of Phase Noise in CMOS Oscillators,” *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 331-343, Mar. 1996.

[23] A. Abidi and S. Samadian, “Phase Noise in Inverter-Based and Differential CMOS Ring Oscillators,” *Proceedings of the IEEE Custom Integrated Circuits Conference*, Sep. 2005.

[24] T. Sakurai, et al., “Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas,” *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 1723-1732, Feb 1990.

[25] Y. Tang, M. Ismail, and S. Bibyk, "Adaptive Miller capacitor multiplier for compact on-chip PLL filter," *Electronics Letters* , vol. 39, no. 1, pp. 43-45, 9 Jan. 2003.

[26] S. Pennisi, "CMOS multiplier for grounded capacitors," *Electronics Letters*, vol. 38, no. 15, pp. 765-766, Jul. 2002.

[27] K. Shu, et al., "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier," *IEEE Journal of Solid-State Circuits*, vol.38, no.6, pp. 866-874, Jun. 2003.

[28] I. Hwang, "Area-efficient and self-biased capacitor multiplier for on-chip loop filter," *Electronics Letters*, vol. 42, no. 24, pp. 1392-1393, Nov. 2006

[29] J. Choi, K. Lim, and J. Laskar, "A ring VCO with wide and linear tuning characteristics for a cognitive radio system," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 395-398, Jun. 2008.

[30] Van de Beek, et al., "Low-jitter clock multiplication: a comparison between PLLs and DLLs," *IEEE Transactions on Circuits and Systems II*, vol.49, no.8, pp. 555-566, Aug. 2002.

[31] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1723-1732, Nov. 1996.

[32] Y. Moon, et al.,"An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 377-384, Mar. 2000.

[33] E. Song, et al., "A reset-free anti-harmonic delay-locked loop using a cycle period detector," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 2055-2061, Nov. 2004.

[34] J. Koo, S. Ok, and C. Kim, "A Low-Power Programmable DLL-Based Clock Generator With Wide-Range Antiharmonic Lock," *IEEE Transactions on Circuits and Systems II*, vol.56, no. 1, pp. 21-25, Jan. 2009.

[35] C.H. Kim, et al., "A 64-Mbit, 640-MByte/s bidirectional data strobed, double-data-rate SDRAM with a 40-mW DLL for a 256-MByte memory system," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 11, pp. 1703-1710, Nov. 1998.

[36] Hsiang-Hui Chang. et al., "A wide-range delay-locked loop with a fixed latency of one clock cycle," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1021-1027, Aug. 2002.

[37] R.C.-H. Chang, et al., "A Multiphase-Output Delay-Locked Loop With a Novel Start-Controlled Phase/Frequency Detector," *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 9, pp. 2483-2490, Oct. 2008.

[38] W. Rhee, "Design of high performance CMOS charge pumps in phase locked loop". *IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 545-548, Jul. 1999.

[39] D. Banerjee, PLL Performance, simulation and design, 4th ed. NJ: *Dog Ear Publishing*, 2006.

[40] A. Kral, F. Behbahani, and A. Abidi, "RF-CMOS oscillators with switched tuning," in *IEEE Custom Integrated Circuits Conference*, pp. 555–558, May 1998.

[41] F. Herzel, G. Fischer, and H. Gustat, "An integrated CMOS RF synthesizer for 802.11a wireless LAN," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1767–1770, Oct. 2003.

[42] F. Herzel, G. Fischer, H. Gustat, and P. Weger, “An integrated CMOS PLL for low-jitter applications,” *IEEE Transactions on Circuits and Systems II*, vol. 49, no. 6, pp. 427–429, Jun. 2002.

[43] H. Gustat and F. Herzel, “Integrated FSK demodulator with very high sensitivity,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 2, pp. 357–360, Feb. 2003.

[44] C. Kuo, J. Chang, and S. Liu, "A spur-reduction technique for a 5-GHz frequency synthesizer," *IEEE Transactions on Circuits and Systems I*, vol.53, no.3, pp.526-533, Mar. 2006.

[45] D.-K. Park and S. Mori, “Fast Acquisition Frequency Synthesizer with the Multiple Phase Detectors,” *IEEE PACRIM Conference on Communications*, vol. 2, pp. 665-668, May 1991.

[46] T. Lee and W. Lee, "A Spur Suppression Technique for Phase-Locked Frequency Synthesizers," *IEEE ISSCC Dig. Tech. Papers*, pp. 2432-2441, Feb. 2006.

[47] B. A. Floyd, "Sub-Integer Frequency Synthesis Using Phase Rotating Frequency Dividers," *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 7, pp. 1823-1833, Aug. 2008.

[48] J.-H. Kim, et al., “A 120-MHz–1.8-GHz CMOS DLL-based clock generator for dynamic frequency scaling,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2077–2082, Sep. 2006.

[49] C.-H. Lin and C.-T. Chiu, “A 2.24 GHz wide range low jitter DLL based frequency multiplier using pMOS active load for communication applications,” *IEEE International Symposium on Circuits and Systems*, pp. 3888–3891, 2007.

[50] B. Kim, T. C. Weigandt, and P. R. Gray, “PLL/DLL system noise analysis for low-jitter clock synthesizer design,” *International Symposium on Circuits and Systems*, London, U.K., Jun. 1994.

[51] B. Waerden, E. Artin, and E. Noether. Algebra. New York: *Springer*, 2003.

[52] N. Biggs. Discrete mathematics : *Oxford University Press*, 2002.

PUBLICATIONS

[1] S. Kim, **J. Choi**, S. Beck, T. Song, K. Lim, and J. Laskar, "Subthreshold Current Mode Matrix Determinant Computation for Analog Signal Processing," *IEEE International Symposium on Circuits and Systems*, June 2010.

[2] S. Kim, T. Song, **J. Choi**, F. Bien, K. Lim, and J. Laskar, "Semi-Active High-Efficient CMOS Rectifier for Wireless Power Transmission," *IEEE Radio Frequency Integrated Circuits Symposium*, May 2010.

[3] **J. Choi,** W. Kim, S. Kim, S. Beck, K. Lim, and J. Laskar "A Fully Integrated PLL with a Spur Elimination Technique using an Edge Interpolator," *IEEE Transactions on Circuits and Systems II*, May 2010, submitted.

[4] K. Kim, **J. Choi**, J. Laskar, "An All-Digital Out-Phasing Modulator with Digital Mismatch Compensation," *IEEE Transactions on Microwave Theory and Techniques*, February 2010, submitted.

[5] **J. Choi,** S. Kim, W. Kim, K. Kim, K. Lim, J. Laskar, "A Low Power and Wide Range Programmable Clock Generator with a High Multiplication Factor," *IEEE Transactions on Very Large Scale Integration (VLSI)*, October 2009, accepted.

[6] **J. Choi,** J. Park, K. Kim, K. Lim, and J. Laskar, "High Multiplication Factor Capacitor Multiplier for an On-chip PLL Loop Filter," *IET Electronic Letters*, February 2009.

[7] K. Kim, **J. Choi**, and, J. Laskar, "All-Digital Out-Phasing Transmitter", presented in the *ISSCC* 2009 Student Forum, February 2009.

[8] **J. Choi**, K. Lim, and, J. Laskar, "A ring VCO with wide and linear tuning characteristics for a cognitive radio system," *IEEE Radio Frequency Integrated Circuits Symposium*, pp.395-398, June 2008.

VITA

Jaehyouk Choi was born in Seoul, Korea, in 1980. He received the B.S. degree (*summa cum laude*) in electrical engineering from Seoul National University, Seoul, Korea, in 2003, and the M.S. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, in 2008. He is currently working toward the Ph.D. degree in electrical and computer engineering at Georgia Institute of Technology, Atlanta.

In the spring and the summer of 2010, he worked as an internship with Qualcomm, San Diego, where he designed advanced VCOs in TX PLLs. His current research interests include analog and RF circuit design, in particular, VCOs and PLL/DLL-based frequency synthesizers for wireless communication systems.