VersaQ, Inc.
75 Fifth Street NW
Suite 202
Atlanta, GA 30308

## Phase 1 Final Report

# LOW COST, HIGH PERFORMANCE TRANSMIT/RECEIVE INTEGRATED CIRCUIT ON A SINGLE CHIP

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Report developed under STTR contract for topic MDA09-T004. Under this contract, VersaQ is collaborating with Prof. John Cressler's group at Georgia Tech under sub-contractual agreement of the STTR award. In the proposed collaborative effort, we build upon and expand the scope of previous work performed at Georgia Tech with the goal to develop a fully operational X-band T/R module, one of the key-elements to building a phased array antenna.

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## Introduction

One of the key-elements to building a fully operational phased array antenna is the requisite RF electronics. Historically, radar transmit/receive (T/R) modules have been implemented as complex, multi-chip GaAs MMICs, resulting in very high cost per T/R module, high weight, and high power dissipation; all of these characteristics are clear disadvantages for compact vehicles. Recently, SiGe technology, with its low-cost, high yield, and high performance, has emerged as a viable path in defense radar system design and is rapidly gaining traction. While this low-cost, light-weight radar design paradigm was initially begun as a path forward for next-generation defense ground-based X-band tactical radars, this SiGe radar design methodology is clearly extendable to a variety systems, and will provide compelling advantages for many applications including defense radar systems with eventual commercial applications. In this project, VersaQ (a start-up Company) collaborated with Prof. John Cressler's group at Georgia Tech under sub-contractual agreement of the STTR award. In the proposed collaborative effort, we build upon and expand the scope of previous work performed at Georgia Tech with the goal to develop a fully operational X-band T/R module for a phased array antenna.

SiGe heterojunction bipolar transistor (HBT) technology, already well-entrenched as an integrated circuit design platform for a wide variety of high-speed, mixed-signal applications, is now rapidly gaining traction in the radar world. SiGe technology offers ultra-high-speed, very low-noise transistors at modest lithographic nodes (e.g., 200+ GHz as 130 nm), while maintaining low power dissipation, high levels of integration, unparalleled reliability, very high yield, and low cost. The high-speed SiGe HBT exhibits a unity-gain cutoff frequency ($f_T$) of 200 GHz and a maximum oscillation frequency ($f_{MAX}$) of 285 GHz. SiGe technology is also applied for the on die incorporation of 130 nm digital CMOS devices, along with microstrip transmission lines, low loss spiral inductors, and low loss MIM capacitors, enabling single-chip solutions with substantial embedded functionality.

X-band radar T/R modules historically incorporate a phase shifter, a low-noise amplifier (LNA), a power amplifier (PA), a single-pole double-throw (SPDT) switch, a circulator, and digital control circuitry, all based on various technologies and discrete components. The critical factors in producing a low power consumption phased array are component power consumption, efficiency and component loss. Losses indirectly drive power consumption by creating the need for additional amplification and therefore additional power consumption. Our proposed architecture utilizes a hybrid of integrated circuit technologies to select the best in terms of power consumption for each required phased array component.

Two versions of the T/R modules are described in this report. Both modules were optimized concurrently by leveraging our expertise from the previous collaborative efforts. The current spececifications and trade off analyses are also described for various performance optimization scenarios.

Two versions of power amplifiers viz., medium power and low power have been designed, built, and measured. The trade off analysis from the system perspective has been analyzed.

## 1. Phase 1 Technical Objectives

VersaQ has subcontracted Dr. Cressler's group at Georgia Tech to develop a low cost/ high yield/ high uniformity single chip TRIC. This SiGe T/R IC will include the T/R RF front-end, low loss switches, on-chip digital control, and digital compensation networks to ensure performance uniformity, along with control, at the element level, ultimately enabling a cost effective radar T/R platforms for future X-band radar needs.

The principal goal of Phase I is to conduct a trade study for the topology and outline specifications for building blocks of the single chip SiGe T/R IC, which could include: (1) LNA, (2) switches, (3) pre-amp driver, (4) PA, (5) phase shifter, (6) bias/control circuitry, (7) digital control, and (8) limiter. Part of the trade study will evaluate commercially available SiGe technology platforms for these designs, but initial work will focus on IBM 130 nm 8HP SiGe BiCMOS since many circuit building blocks exist in this platform.

A unique low-cost packaging technology, using organic liquid crystal polymer (LCP) and RXP materials from Rogers Corporation, will also be developed to support the integration of multiple T/R die for ultra-low-cost and small form-factor element arrays.

System-level performance specifications will be identified and a flow-down of RF block performance specifications will be determined. Trade studies in performance partitioning will be conducted (e.g., gain vs. noise figure). For a starting T/R architecture, we will build upon our previous MDA-sponsored X-band radar effort, since that targets already-defined future MDA spirals.

## 2. Phase 1 Work Plan

An outline of the proposed tasks is given below. The current status for each task is summarized in italics.

Task 1: Specify Radar Requirements and T/R Architecture

Teaming with the MDA, we will hold a kickoff meeting within 30 days of award. During this meeting, key issues regarding radar system specifications and defining MDA needs will be addressed. We will propose and obtain feedback on several candidate T/R architectures.

*A kick off meeting was conducted on June 23, 2010 where VersaQ and Georgia Tech capabilities and the current research status of various T/R modules were presented. Future efforts under the Phase 1 (and possible Phase II) award were discussed.*

Task 2: Perform T/R system architecture trade-off analysis

Based upon the selected T/R architecture(s), we will utilize an in-house radar specifications algorithm to develop flow-down performance specifications for individual RF building blocks (e.g., noise, gain, linearity, power, etc). Trade-offs of performance partitioning on both receive and transmit path will be applied, and then used to define circuit targets.

*These results are described in detail in Section 3.*

Task 3: Circuit Design and Simulations

The major Phase I task will be to perform block-level circuit simulations of the key T/R building blocks, and assess their performance capabilities, both at the block and system levels. These results will then be used to determine the projected overall receive path and transmit path performance. The important circuit blocks, together with the specifications to define and achieve are listed. (1) LNA (gain, noise, linearity, power), (2) switches (loss, power handling, robustness), (3) pre-amp driver (gain, power, output power), (4) PA (gain, achievable output power, power dissipation, stability, thermal constraints, efficiency), (5) phase shifter (number of bits, linearity, phase error, bandwidth, power), (6) bias/control circuitry (stability over P-V-T, robustness), (7) digital control (control functionality, robustness), and (8) limiter (loss, power handling).

*Results from these block level simulations and trade studies will be the basis for future Phase II work. Initial trade-study scenarios have been conducted and block level simulation based on performance of currently measured hardware is completed. A system level analysis with various trade options has been provided from the cost/ performance perspective.*

Task 4: LCP/RXP Packaging Technology

During this phase we will design optimized RF interconnects between the organic layers (LCP and RXP) and the SiGe circuits. We will pursue the wire bonding solution, as well as ball/bump bonding techniques and derive modeling circuits and design guidelines for various multilayer stack-ups in X-band. For higher frequencies, we will investigate embedding of the SiGe chips between two organic layers.

*Various efforts for incorporating SiGe circuits have been pursued. Design rules for processing LCP materials in large area have been established.*

Task 5: Optimized IC Designs Based on Actual Layouts

The trade studies and analysis performed at the end of Phase I will form the basis for actually laying out the requisite circuit blocks, extracting circuit node parasitics and assessing circuit performance sensitivity to parasitic. Further optimization of the circuits will be performed as needed.

*Optimized design and layout will be conducted upon starting Phase II after the appropriate designs trade-off analysis are completed in Phase I.*

Task 6: Control System Demonstration

In addition, the Phase I Option will be used to develop the logic by which the antenna array will be controlled. Simple control algorithms will be written and tested to allow for the array to control the beamsteering operation. This system will be demonstrated on the benchtop as a first generation test of the more sophisticated system which will be required by the end of Phase II.

*After the chip topology is selected, digital control will be designed and synthesized in Phase II to control these blocks.*

Task 7: BGA Reliability Testing

As a path to greater integration, ball grid array design will be pursued. However, the reliability of this method for connecting the RFICs with the microstrip connections, though studied, has not been proven in the case of LCP/RXP circuits. If LCP or RXP is chosen to be the package material, testing on BGA connections will be conducted. This step can lead to faster manufacturing and remove the need for cavities to be made for the ICs.

*Significant R and D efforts are in progress and various scenarios for embedding SiGe circuits within a viable commercial path have been studied. Conceptual paths for large format commercialization of embedded SiGe are provided. Reliability test procedures for various interconnection matrices will also be identified in Phase II.*

## 3. Phase 1 Accomplishments

Two T/R modules namely, MDA and NASA are described in this section. These are developed in collaboration with Prof. John Cressler's group and through the leverage of the past effort at Georgia Tech.

3.1.MDA T/R Module

The current X-band MDA T/R module was fabricated in IBM's commercially available SiGe 8HP BiCMOS process. Table 1 lists the desired performance specifications. Many design iterations and circuit block testing of this T/R module are present, with this report highlighting the simulation results of latest integrated design.

Table 1. Specifications for the T/R Module

| Category | Threshold | Objective |
|---|---|---|
| Operating frequency | 8.5-10.5 GHz | 8-12 GHz |
| Maximum pulse width | 10 ms | 10 ms |
| Duty cycle | 25%, max | 25%, max |
| Tx Input Power | 0 dBm | 0 dBm |
| Tx Output Power, peak | 0.5 W | 1 W |
| LNA Noise Figure | 2.0 dB | 1.5 dB |
| Chip noise figure * | $T_{sys}$ = 1000 K | $T_{sys}$ = 800 K |
| Chip gain * | $T_{sys}$ = 1000 K | $T_{sys}$ = 800 K |
| Input TOI | -10 dBm | -5 dBm |
| Switching speed | 1 usec | 100 nsec |
| Input VSWR | 2:1 | 1.5:1 |
| Phase shifter | 0-360°, 4 bits | 0-360°, 5 bits |
| Phase error (RMS) | <10° | <5° |
| Chip Efficiency | 15% | 25% |
| Total T/R chip area | < 35 $mm^2$ | < 20 $mm^2$ |

### *3.1.1. Design*

The topology for the T/R module is shown in Figure 1. The module contains two LNAs, which can take inputs from different radiators, bi-directional phase-shifter, SP3T duplexer switch, and a TX pre-amplifier. In addition, the phase-shifter is controlled by a digital serial-to-parallel converter, and biases are generated on-chip from 5 V (TX) and 3.5 V (RX) supplies. A digital interface was built into the RX and TX amplifiers allow them to be digitally turned into a low-power (off) mode. Lastly, the LNAs in the RX path are supplied by a band-gap reference (BGR) that should mitigate impacts from power supply noise and improve process variation.

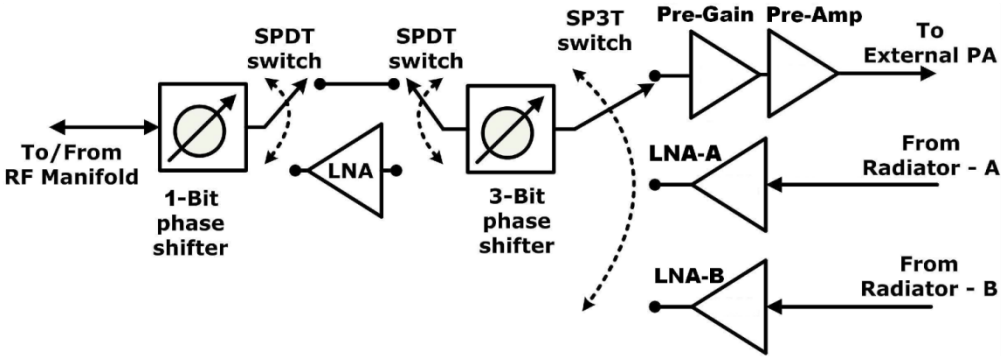



Figure 1. Topology for SiGe BiCMOS T/R module

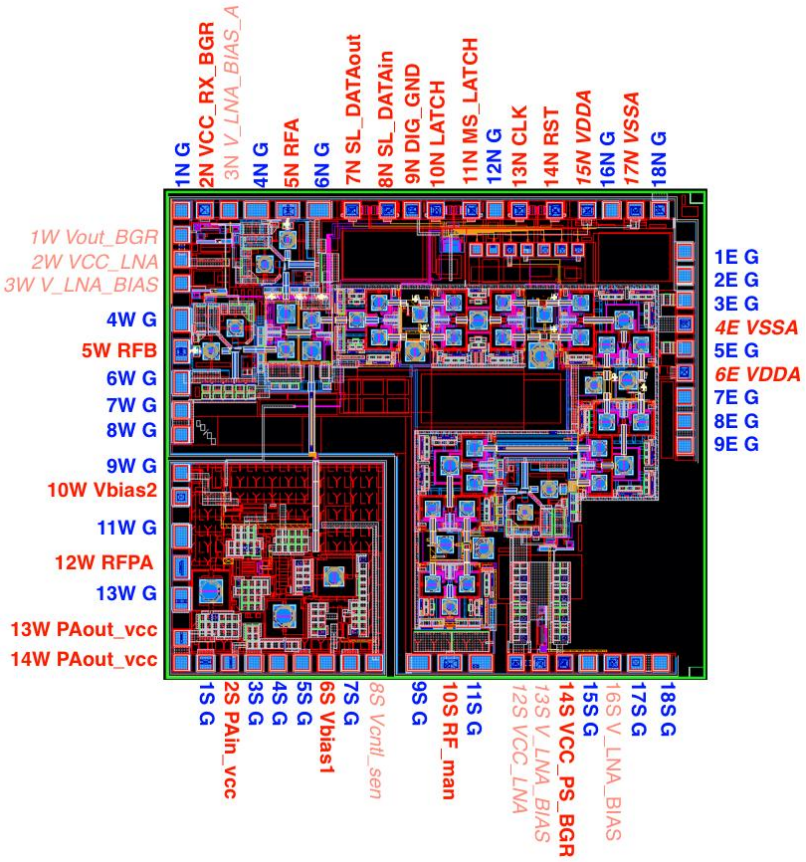



Figure 2. Layout of T/R module with I/O pads description

The entire chip dimensions are 3.4 x 3.8 $mm^2$, with both TX and RX amplifiers internally matched. Figure 2 depicts the layout and I/O pins for the T/R module.

### 3.1.2. RX simulation results

DC and RF monte carlo simulations were performed on the RX path to determine process and temperature stability. Fig 3 shows the monte carlo results from 200 samples of the bias currents for the LNAs at 25° C. The standard deviation is approximately 1-2 mA. Table 2 presents the results of all relevant bias currents for the RX path.

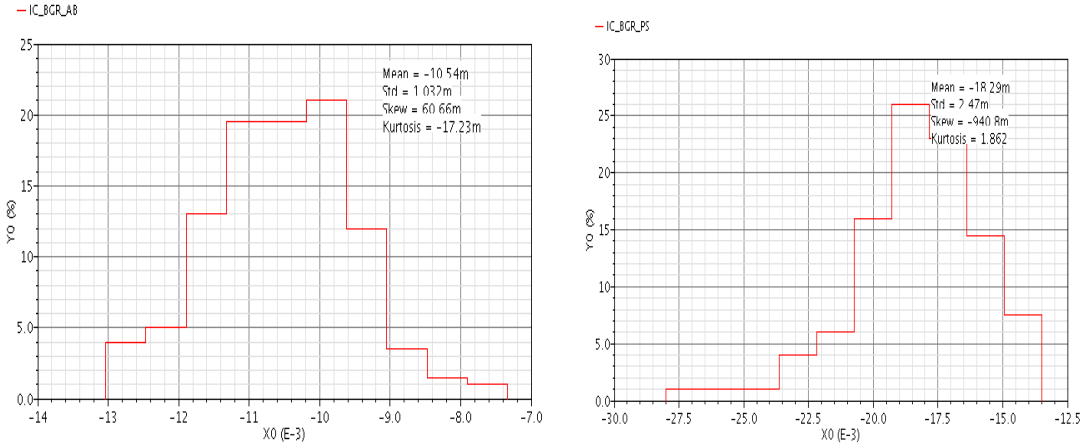



Figure 3. LNA bias currents for RX path

Table 2. *DC* results from monte carlo simulation of RX path.

| Bias name | mean | + std | - std |
|---|---|---|---|
| Vout_BGR_AB | 2.558 V | 2.605 V | 2.512 V |
| Vout_BGR_PS | 2.557 V | 2.601 V | 2.513 V |
| IC_BGR_AB | 10.54 mA | 11.57 mA | 9.505 mA |
| IC_BGR_PS | 18.29 mA | 20.76 mA | 15.82 mA |
| LNA_PS_IC | 16.56 mA | 18.97 mA | 14.15 mA |
| LNA_B_IC | 8.562 mA | 9.537 mA | 7.588 mA |

S-parameters and noise figure of the RX path were also simulated using the same setup and the results are presented below for 8.5 – 10.5 GHz. The gain / NF standard deviation was approximately 1 / 0.2 dB, respectively (Figure 4). Figure 5 shows plots of these performances over X-band.

In addition, high-temperature operation was simulated (+125° C) and shown in Figure 6. The gain was reduced by approximately 5 dB, while the NF was increased by 1 dB. The source of these variations can be attributed to changes in the bias currents and RF performance of the devices.

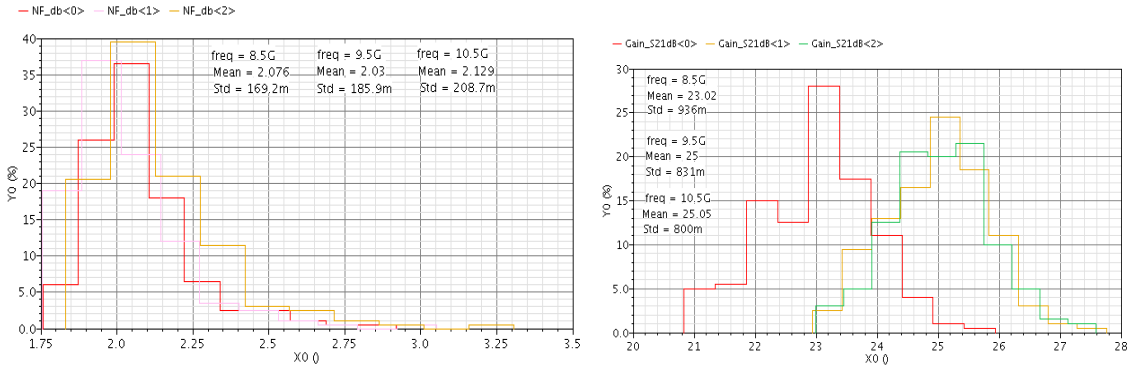



Figure 4. Monte Carlo results of NF and Gain of RX path

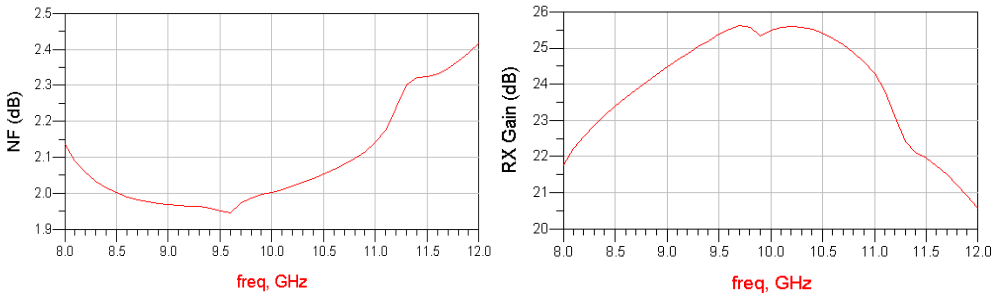



Figure 5. NF and Gain of RX path from 8 - 12 GHz

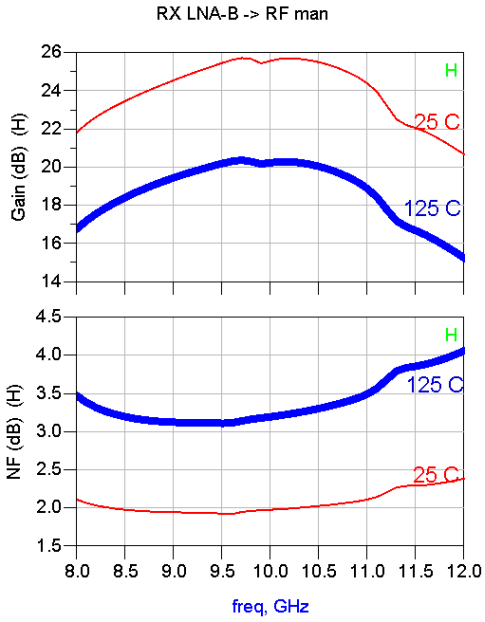



Figure 6. RX path performance simulated at 125 C

### 3.1.3. TX Simulation results

The transmit path of the full T/R module was also simulated at 25° C and 125° C, which included the pre-amp PA and phase shifter. The output 3 dB compression point at 25° C was simulated to be over 21 dBm at 9.5 GHz as shown in Figure 7. The peak PAE was simulated to be over 28 % as shown in Figure 8. The small-signal S-parameters are shown in Figure 9 with over 20 dB of gain for the entire TX path.

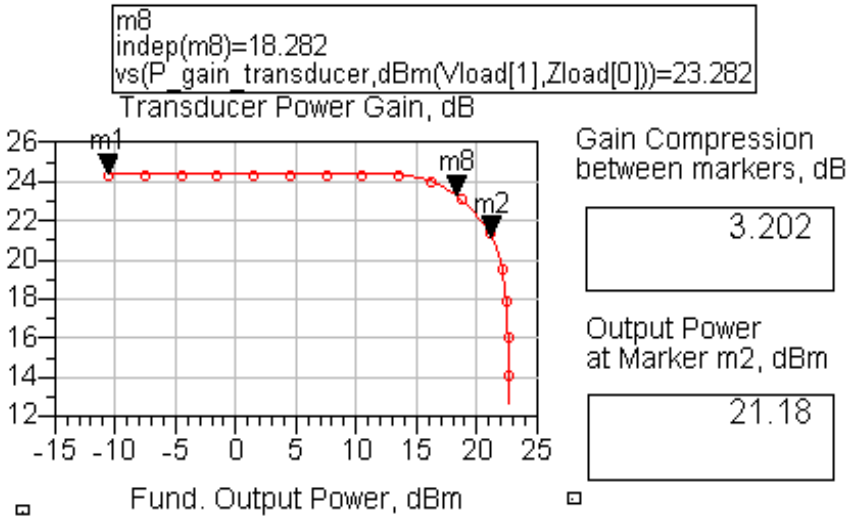



Figure 7. Output power of TX path of T/R module at 9.5 GHz

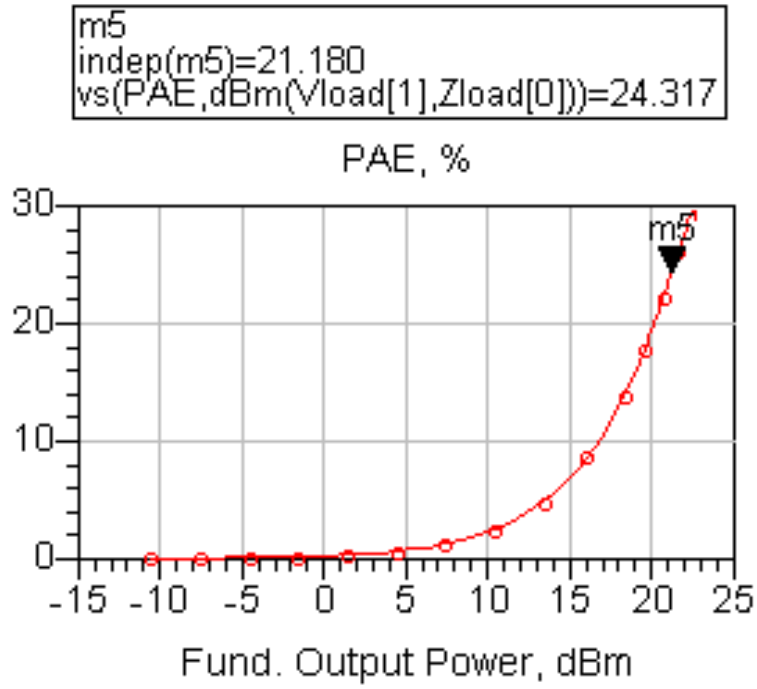



Figure 8. PAE as function of ouput power for T/R module

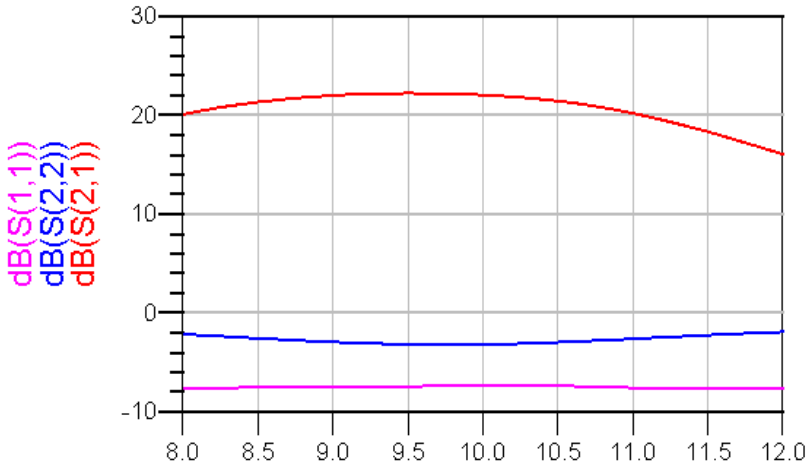



Figure 9. Small-Signal S-parameters of TX path of T/R module

The performance at 125° C is similar with slightly degraded gain and output power; bias currents are tuned to the designed values to compensate for changes over temperature (Figures 10 and 11).

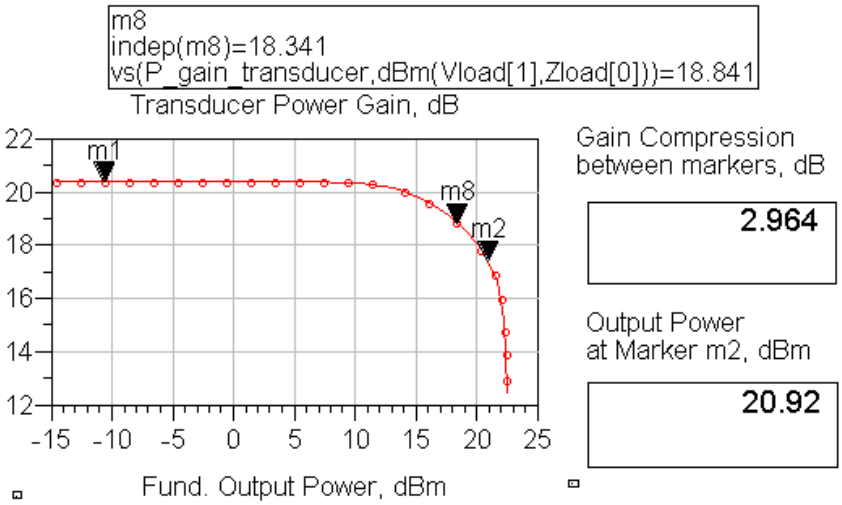



Figure 10. Output power at 125 C of TX path of T/R module

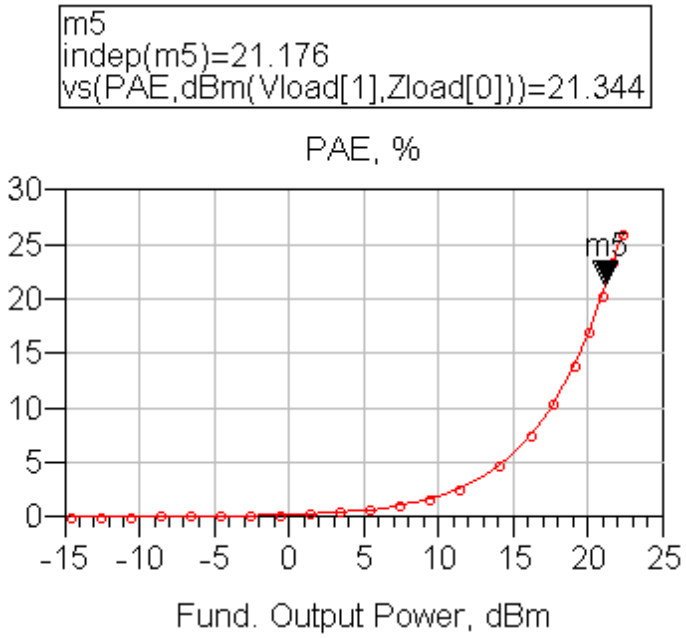



Figure 11. PAE of T/R module at 125 C

### 3.1.4. Digital Serial – to – parallel converter simulation results

The T/R module also includes a VHDL generated digital serial-to-parallel converter block that controls the phase shifter and T/R setting. The inputs to the digital block are as follows:

- SLDATAin - serial data for T/R module (5 … 0)

| Bit | Purpose | 0 | 1 |
|---|---|---|---|
| 0 | T/R select | RX | TX |
| 1 | LNA A/B Select | LNA_B | LNA_A |
| 2 | V180 | 0 deg | 180 deg |
| 3 | V90 | 0 deg | 90 deg |
| 4 | V45 | 0 deg | 45 deg |
| 5 | V22 | 0 deg | 22.5 deg |

- LATCH - Latches in data into registers once all serial data has been sent, set high one clock cycle at end of serial SLDATAin data stream.
- MSLATCH – applies serial data to parallel pins, data is applied at rising edge of MSLATCH asynchronous with clock, set high after LATCH.
- RST – resets spc, should be done when chip is turned on.

Data is read at rising edge of clock, for our simulations, the data is applied 1.5 ns (for 100MHz CLK) before the clock goes high. Simulation results are shown in Figure 12.

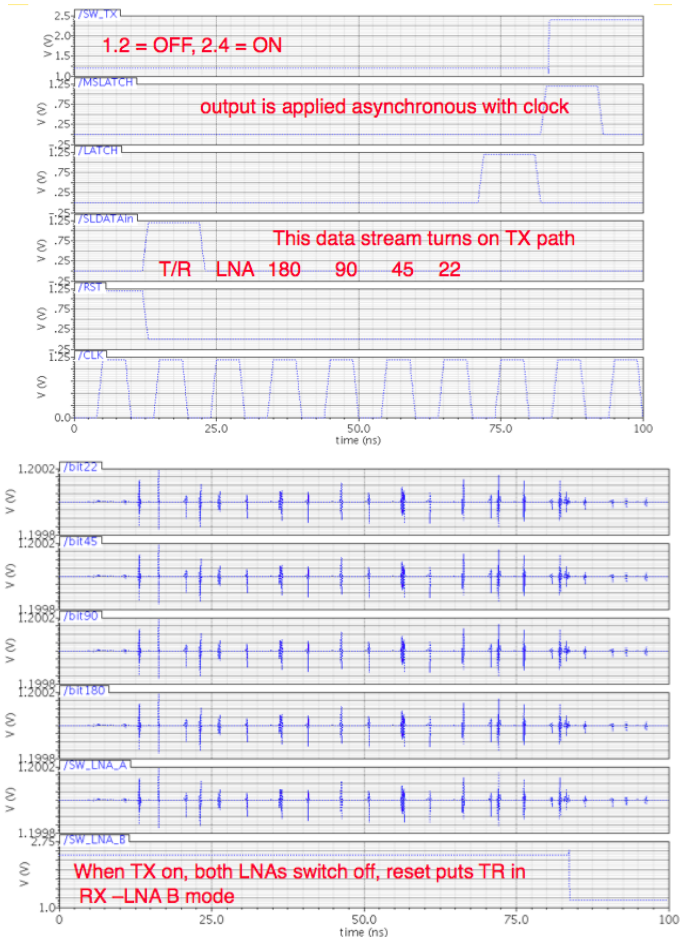



Figure 12. Results of SPC digital block simulation

Simulated results for an X-band SiGe BiCMOS T/R module for low-power density phased-array antenna systems are presented. The T/R module was designed to be easily packaged and includes self-biased receive and transmit paths and digital control. The performance specifications simulated meets the system objectives for this T/R module. The T/R module was biased and matches the simulated *dc* results, indicating the T/R module is functional. The measured results will be available at the conclusion of Phase 1 with board design allowing RF performance. Previous designs confirm that the measured results match the simulation.

## 3.2. NASA T/R Module

### 3.2.1. T/R Chip design and Layout

Several T/R module iterations were undertaken within the domain of collaborative work with Prof. John Cressler's group at Georgia Tech under the NASA award. A topology for the NASA T/R module is shown in Figure 13. Simulations were performed for the full RX path and are presented in Figures 14 and 15. The simulated gain is over 10 dB at 9.5 GHz with the corresponding NF less than 2 dB. Figure 16 shows the stand-alone PA results with the ability to shut the PA on/off during TX/RX mode. The small signal gain of the PA was determined to be approximately 40 dB, while saturated output power was over 20 dBm. The T/R module also includes a digital serial-to-parallel converter and bias generation circuits for all the circuit blocks.

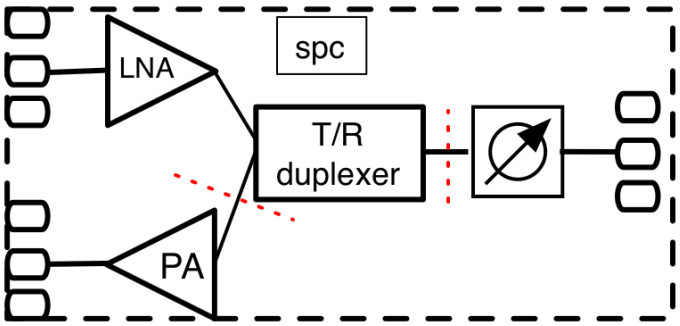



Figure 13. Topology of T/R module

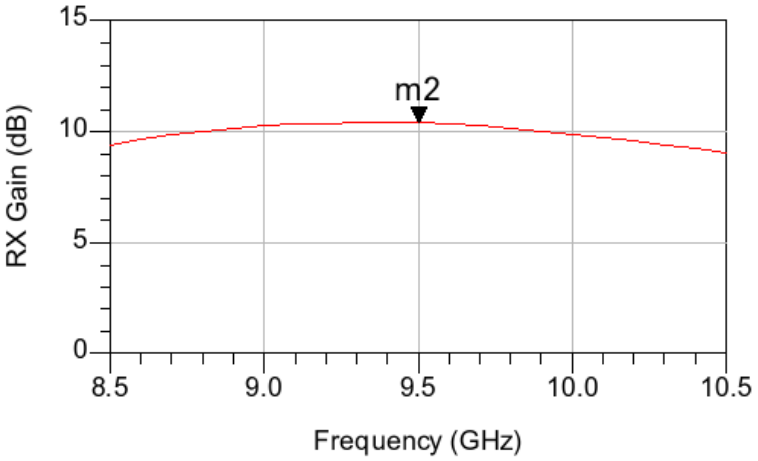



Figure 14. Simulated Gain of full RX path

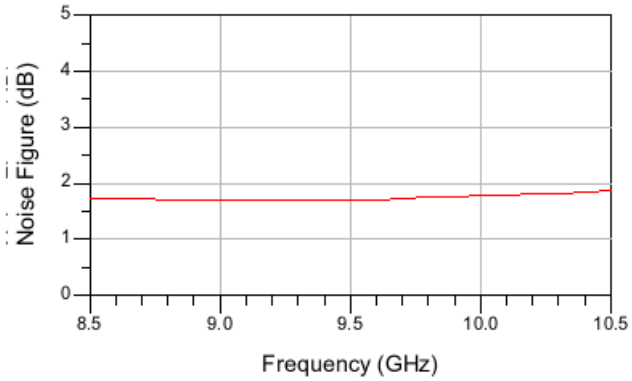
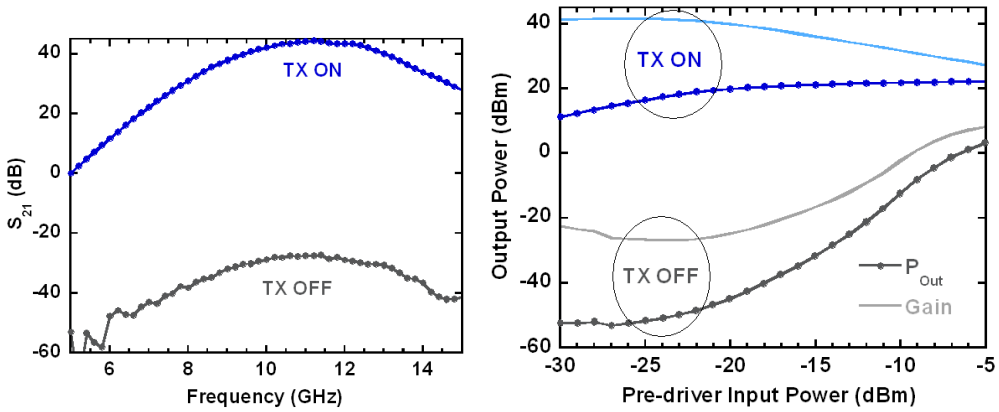


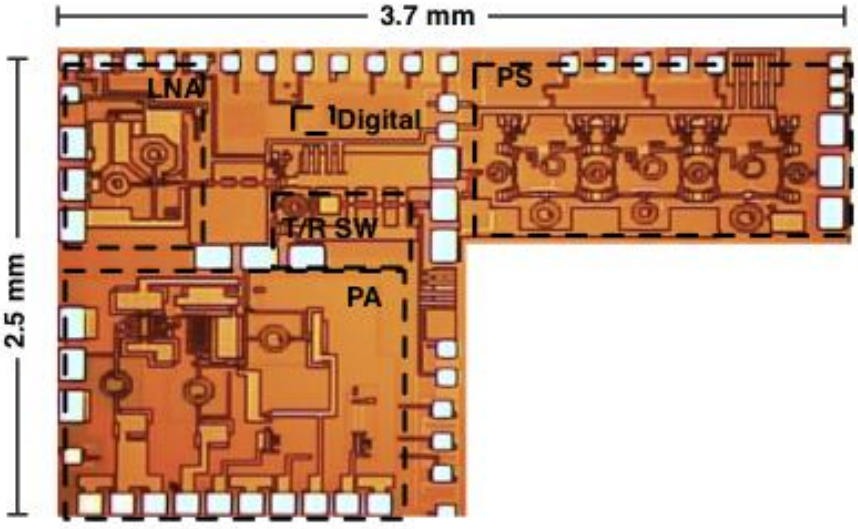

Figure 15. Simulated Noise Figure of RX path



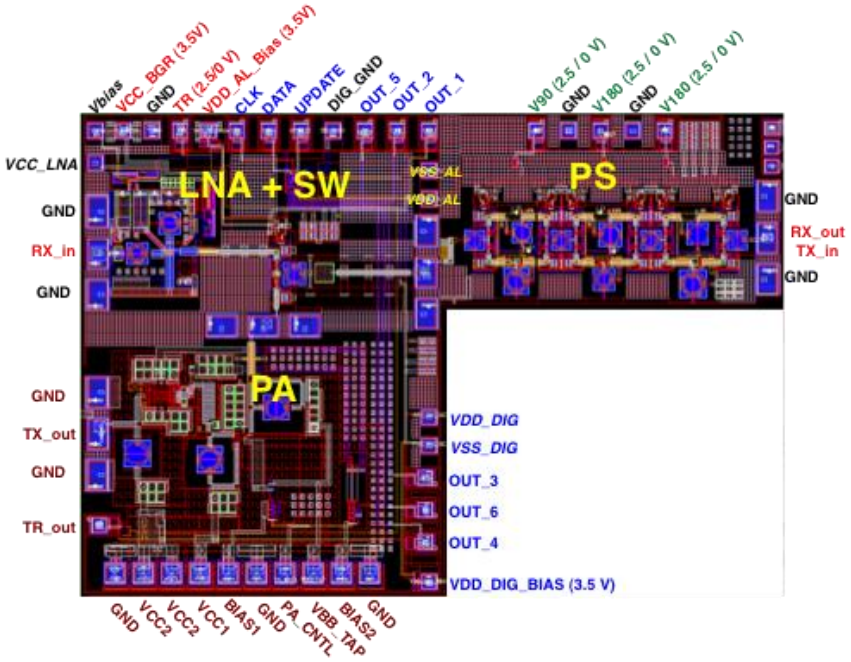

(a) Small Signal Gain (b) Output Power at 9.5 GHz

Figure 16. Measured PA results

The transmit and receive paths were tested independently to verify the performance of both paths of the integrated module. The layout with the I/O pins is shown in Figure 17.




(a)




(b)

Figure 17. (a) Photo and (b) Layout of T/R chip with I/O pins

### 3.2.2. RX path Measurement

The RX path was measured from the LNA, T/R switch, and phase shifter. The measurement was conducted on an on-wafer integrated S-parameter, load-pull, and noise figure test setup. S-parameters for each phase state and noise figure and linearity at the 0 state were measured. To control the phase-shifter and T/R switch, a switchboard was fabricated to control the digital I/O. A picture of the measurement system and switchboard are shown in Figure 18.

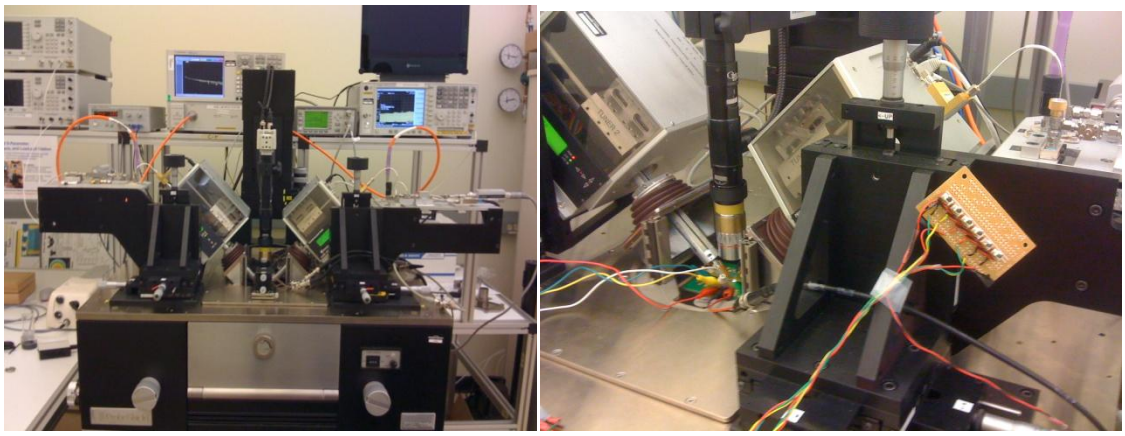


Figure 18. On-wafer measurement system and digital I/O control setup *[Dr. John Cressler's Group, Georgia Tech Equipment]*.

For biasing the RX path, only a single 3.5 V supply is necessary from which all-internal biases are generated, and draws under 10 mA of current, yielding a total dissipated power of 35 mW for the RX path. For controlling the phase shifter and T/R bit, 2.5 V logic levels are used.

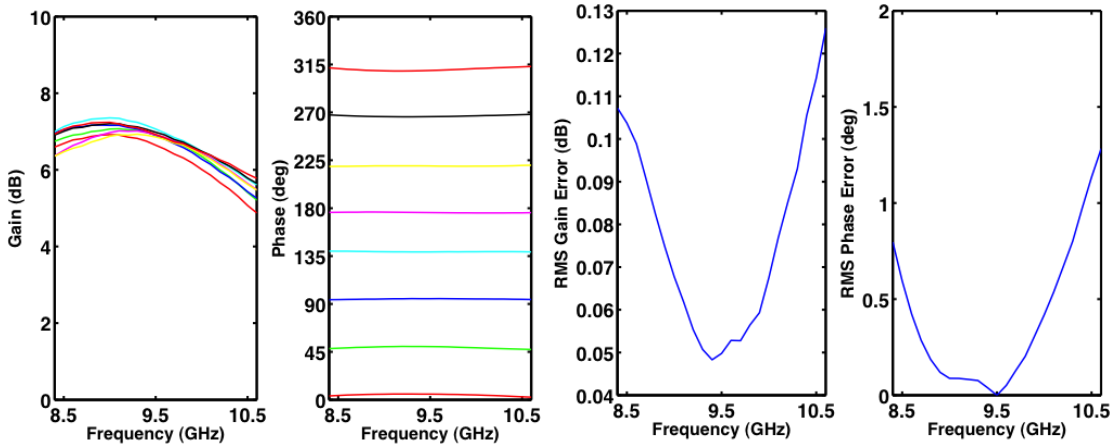



Figure 19. Gain and phase for RX path of SiGe T/R module

The RX path was measured to be fully functional with approximately 7 dB of gain for the full path at 9.5 GHz. In addition, the phase states showed a good response as shown in Figure 19.

The noise figure of the T/R was measured to be less than 2.5 dB at 9.5 GHz, with a close match to the minimum noise figure. In addition, the two-tone linearity showed an OIP3 of 7.8 dBm, as shown in Figure 20.

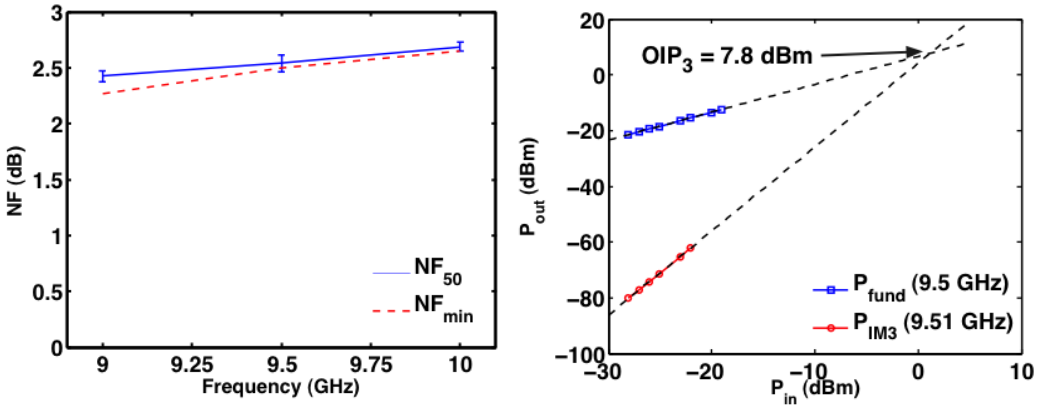



Figure 20. Noise figure and 3rd order linearity of SiGe T/R Module

### 3.2.3. TX Path Measurement

The TX path was measured from the phase shifter to the output of the PA on the same integrated system used to characterize the RX path. Load-pull and swept power measurements were conducted on the TX path to determine maximum output power. A photograph of the setup is shown in Figure 21.

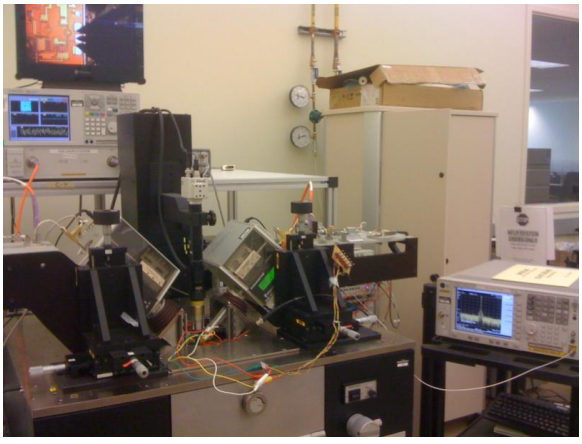


Figure 21. Photograph of TX measurement setup. Spectrum analyzer is shown with output signal from PA. *[Dr. John Cressler's Group, Georgia Tech Equipment*]

The TX biasing requires multiple bias points including an upper supply voltage of 5 V and two tuned voltages to achieve optimal performance. In addition, the T/R bit, operating from 5V logic, is also required. The two-stage PA draws 60 mA of current in steady state operation and increases to 90 mA during compression.

The 3dB compression point was determined to be above 18 dBm with a gain of above 24 dB as shown in Figure 22. With tuning bias voltages, the output power can be improved to near 20 dBm.

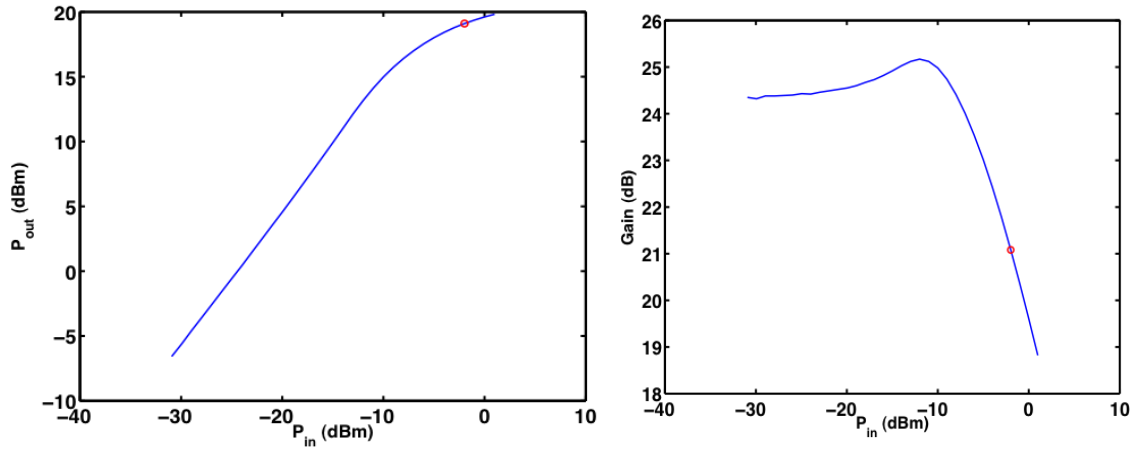



Figure 22. Pout vs Pin and Gain vs Pin for TX path

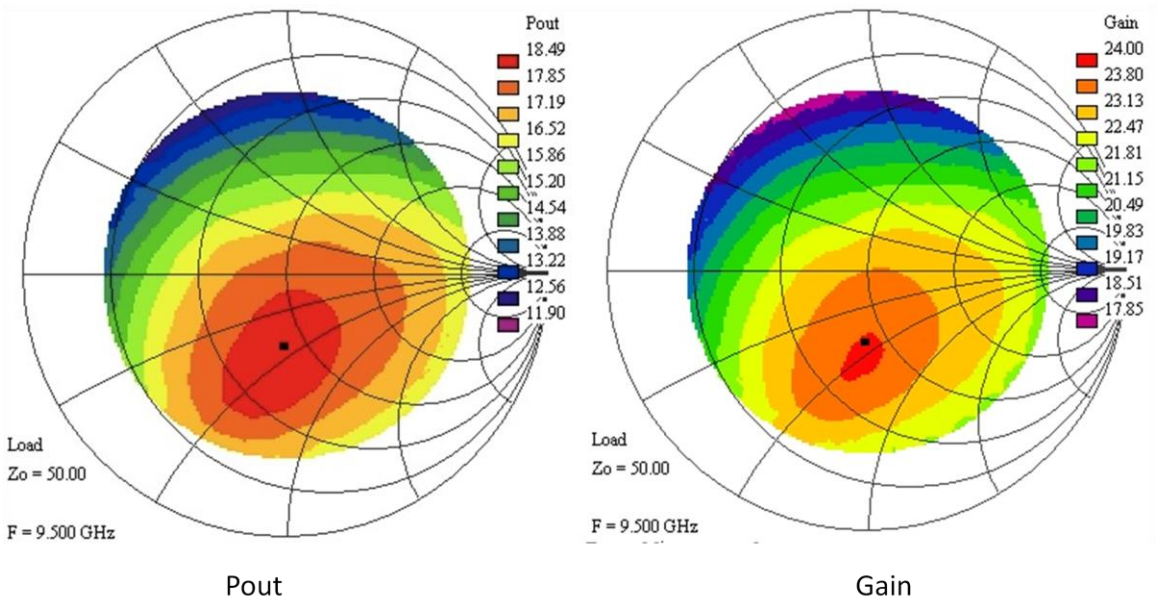



Figure 23. Load-pull contours for Pout and Gain for TX path

In addition, load-pull was performed on the TX path at 9.5 GHz demonstrating the maximum power for the PA. The maximum output power of above 18 dBm (Figure 23) was achieved near 50 Ω. Further testing is necessary to tune the PA bias to achieve maximum output power. In addition, optimized RF probes will be used to measure the PA, and should yield improved results.

Both RX and TX paths are functional with the RX path achieving over 7 dB of gain, and TX path having over 18 dBm of output power.

## 3.3. Trade Studies

### 3.3.1. RX Trade Study

Based on the current SiGe T/R module designs, three different design scenarios are highlighted in Tables 3 and 4. The first scenario aims to target the lowest possible system noise figure by providing a large gain and very low noise figure by trading off linearity with moderate *dc* power consumption. Scenario 2 targets ultra-low *dc* power but yields lower gain, higher noise figure, and moderate linearity, by consuming 14x less power. Scenario 3 makes use of a high-dynamic range LNA that can provide high gain, moderately low-noise figure, and high linearity, but consumes considerably more power.

The figure of merit (FOM) in Tables 3 and 4 is defined by

$$FOM[dBm] = -NF[dB] + ITOI[dBm] + G[dB] + 10\log\left(\frac{P1dB[mW]}{P_{dc}[mW]}\right) + 20\log\left(\frac{f_o[GHz]}{1GHz}\right)$$

Table 3. RX Trade Study Options for T/R modules

| | Current MDA T/R module | NASA T/R module |
|---|---|---|
| RX gain (dB) | 15 | 7 |
| RX NF (dB) | 4 | 2.5 |
| RX ITOI (dBm) | -7 | 0 |
| RX Pdc (mW) | 70 | 35 |
| FOM (dBm) | 3.5 | 6.0 |

Table 4. RX Trade Study Options for different scenarios

| | Scenario 1: target NF | Scenario 2: Low Power | Scenario 3: Balanced |
|---|---|---|---|
| RX gain (dB) | 22 | 9.5 | 19.5 |
| RX NF (dB) | 1.9 | 2.4 | 2.2 |
| RX ITOI (dBm) | -16 | -8.8 | -2.7 |
| RX Pdc (mW) | 70 | 4 | 285 |
| FOM (dBm) | 1.6 | 2.9 | 16.8 |

### 3.3.2. TX Trade Studies

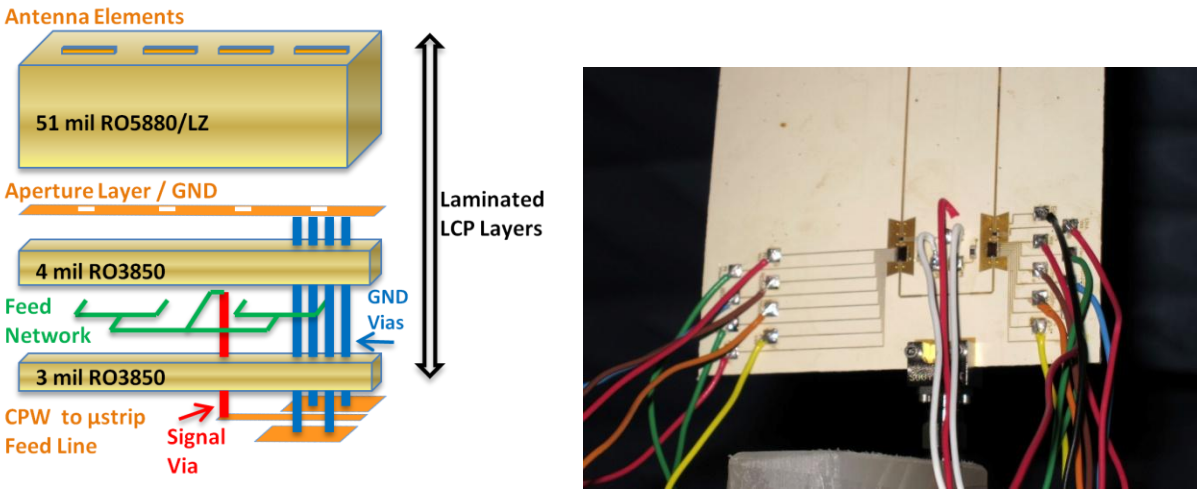
Based on current hardware, much of the TX trade studies will focus on achieving higher output power, on a chip that is self-bias and robust, that can be used for large scale radar applications (Table 5). The first scenario will aim for 0.5 W of output power by using a two stage PA, with both on and off-chip matching. The second scenario will focus on 100 mW PA, targeting a PAE of greater than 30%. Analysis will be conducted to determine if the matching networks for this PA can be done on or off-chip.

Table 5. TX Trade Study Options

| | Current MDA T/R module | NASA T/R module | Scenario 1: higher power | Scenario 2: higher PAE |
|---|---|---|---|---|
| TX Output Power (dBm) | 20 | 20 | 27 | 20 |
| TX gain (dB) | 18 | 20 | 30 | 20 |
| TX PAE (%) | 28 | 28 | 20 | 30 |

## 4. Packaging with SiGe Electronics

An X-band antenna array with integrated silicon germanium low noise amplifiers (LNA) and 3-bit phase shifters (PS) has been extensively investigated in collaboration with Prof. John Cressler at Georgia Tech. SiGe LNAs and SiGe PSs were successfully integrated onto an 8x2 lightweight antenna utilizing a multilayer liquid crystal polymer (LCP) feed substrate laminated with a Duroid antenna layer. A baseline passive 8x2 antenna is measured along with a SiGe integrated 8x2 antenna for evaluation of results. Successful comparisons of the measured and simulated results verify a working phased array with a return loss better than 10 dB across the frequency band of 9.25 GHz - 9.75 GHz. A comparison of radiation patterns for the 8x2 baseline antenna and the 8x2 SiGe integrated antenna show a 25 dB increase in gain. The nulls and peaks of both antennas are closely matched with that in simulation. The SiGe integrated antenna demonstrated a predictable beam steering capability of ±41°. A stack up of the multi-layer antenna array is shown in Figure 24. The packaged LNA and Phase Shifters are shown in Figure 24.




(a) (b)

Figure 24. (a) A Multi-layer Stack up of antenna array, (b) Packaged LNA and phase shifter

## 5. *PA designs for TX path*

Two preliminary PAs have been designed for the TX path: a medium power PA and a robust, lower power PA. The fabricated samples were received in September, 2010.

*Medium Power PA*

The medium power PA was designed using a cascode topology, with simulation results yielding a gain of over 20 dB, Pout of 18 dBm, and a PAE of 30%. The topology and a photograph of the chip are shown in Figure 25.

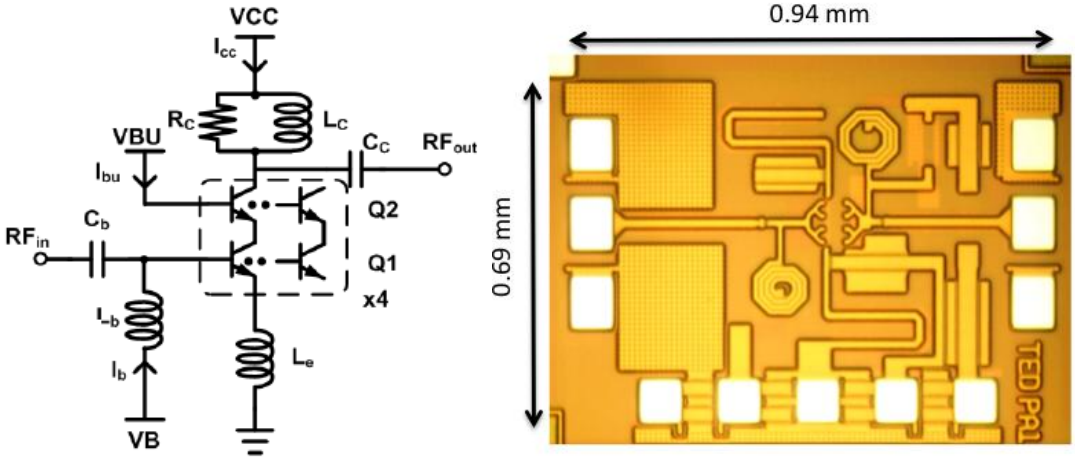



Figure 25. Medium power PA topology and chip

The measured and simulated small-signal S-parameters are shown in Figure 26. There is a significant reduction in gain (over 5 dB) due to problems with both the input and output return loss. These discrepancies will reduce the overall PAE of the PA. Figure 27 shows the large-signal characteristics, with the ability to still achieve the desired 18 dBm of output power.

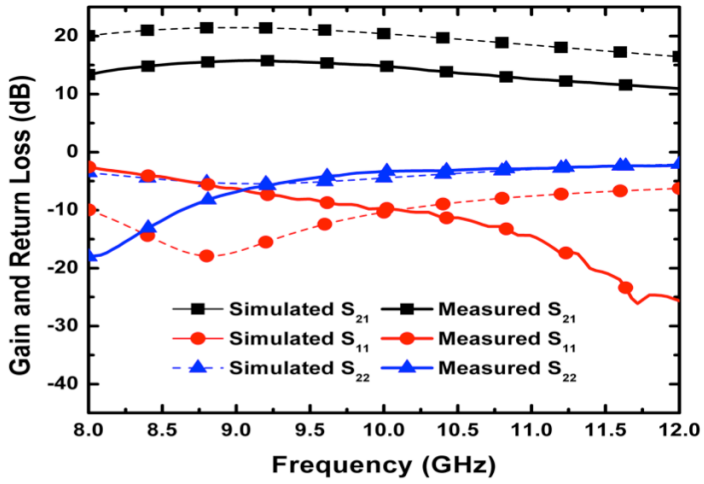



Figure 26. Measured and simulated small-signal S-parameters of medium power PA

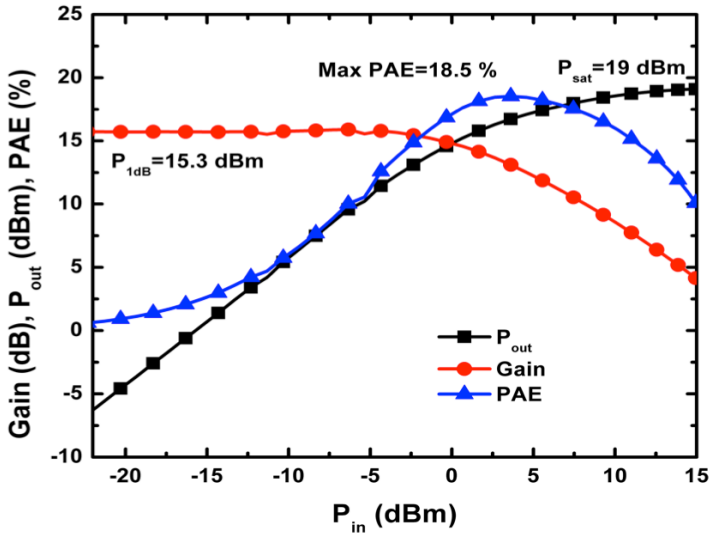



Figure 27. Large-signal measured results of medium power PA

Closer examination of the matching networks as in Figure 28 shows that the passive elements are modeled well within the design kit, therefore, the source of these errors are most probably unaccounted for parasitics around the core transistors and feed networks.

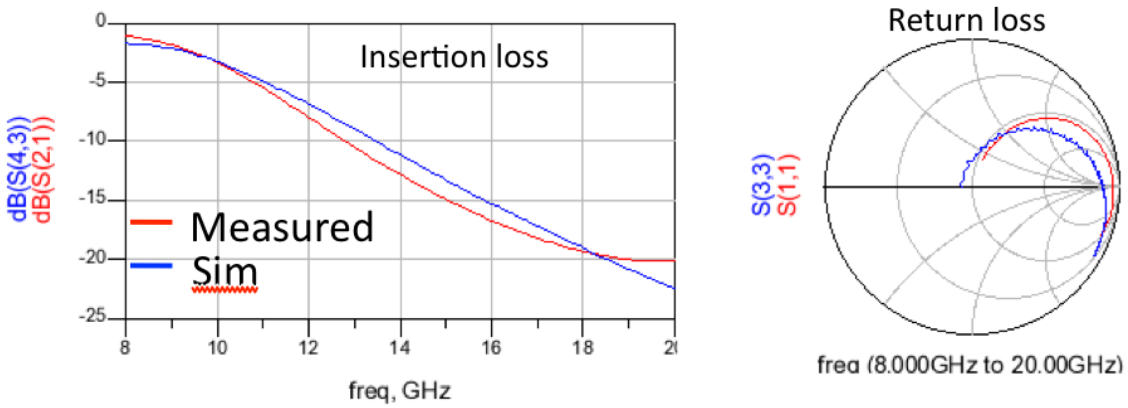



Figure 28. Simulated and measured comparison of matching network in PA

***Robust, lower power PA***

The robust, lower power PA was designed to operate from a self-bias network, which allows robust operation, crucial when implementing these designs in a large array. The topology and photograph of the chip is shown in Figure 29.

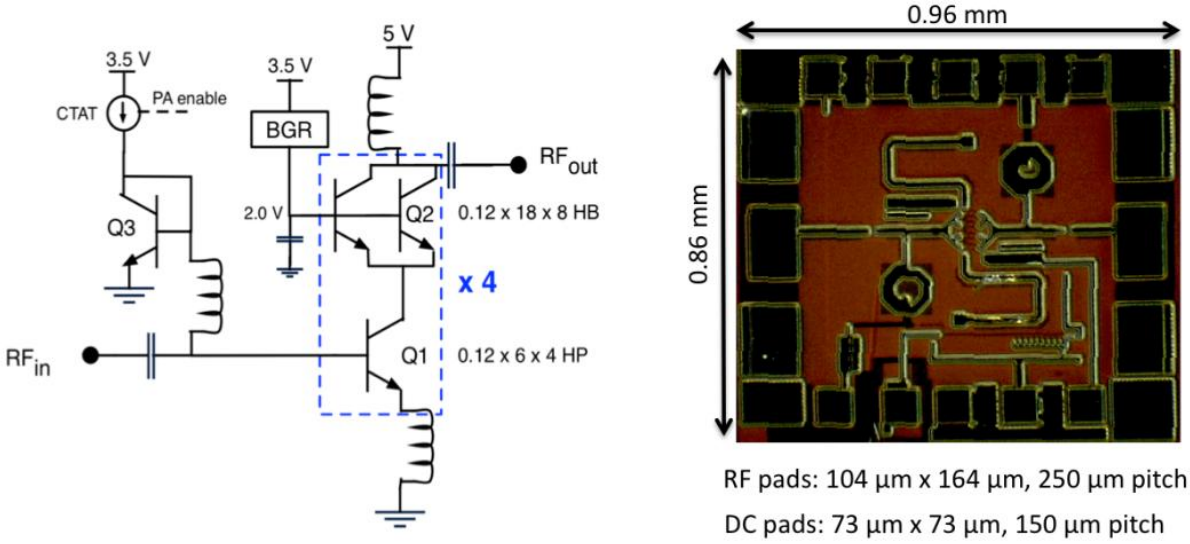



Figure 29. Robust PA topology and die photograph

Similar issues with the matching as found in the medium power PA, and future versions will be redesigned to improve performance. By source matching the input, the gain and output power were improved and are shown in Figure 30.

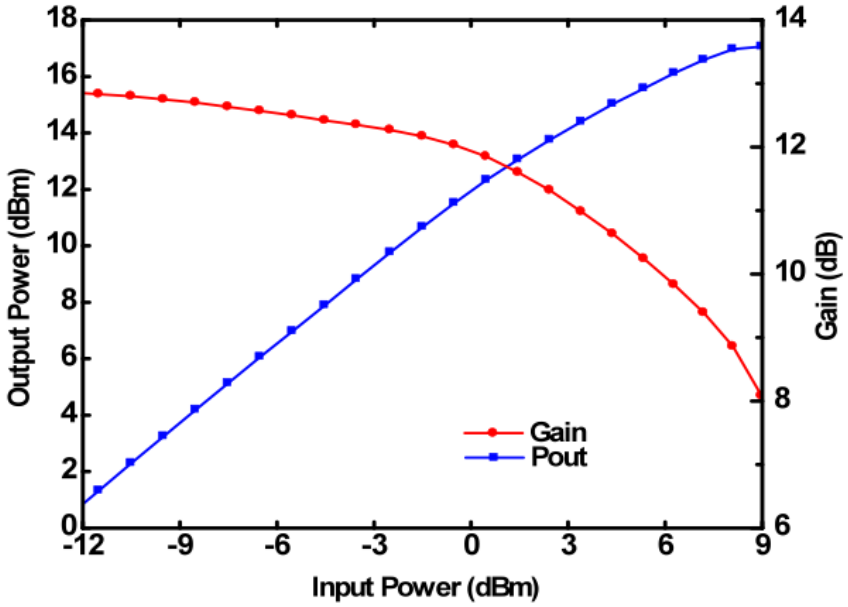



Figure 30. Large signal gain and output power of robust PA

***Upcoming PA Efforts***

The discrepancies between the measured data and the simulation results for each PA are currently being investigated, and the matching issues should be resolved in future design cycles. Once these discrepancies are resolved a robust, medium power PA will be developed. After this PA has been perfected, it will be used as the first stage in a two-stage PA that will push to higher output powers (27+ dBm). While the robust medium power PA is being developed, high power PA design will be explored in the IBM 5PAe process. This SiGe BiCMOS process is targeted for PA applications. Features of 5PAe include high-breakdown devices ($BV_{ceo}$ = 6.3 V, 8.3 V) and through-silicon vias, which are crucial for packaging and stability. Preliminary loadpull measurements have been performed on 5PAe cores, and a board for PA testing has been designed and submitted.

## 6. New Packaging Concepts

We are currently pursuing various options for embedding chips (SiGe, GaN, or GaAs) within the core of the organic package. Feasible paths have been indentified including efficient die cooling particularly applicable for GaN chips. In order to embed the active RF circuits we have already studied wire bonding and via interconnect. Preliminary results on these approaches are summarized below.

### 6.1. Wire Bonding

In the wire bonded approach, the chips will be recessed in a micromachined cavity within the organic package. Figure 31 shows the wire bonded version of a packaged oscillator [1]. The mm-wave SiGe oscillator has been successfully packaged using an LCP organic material while maintaining a high performance profile as shown in Figure 31. This work was done in collaboration with Prof. Cressler's Group at Georgia Tech.

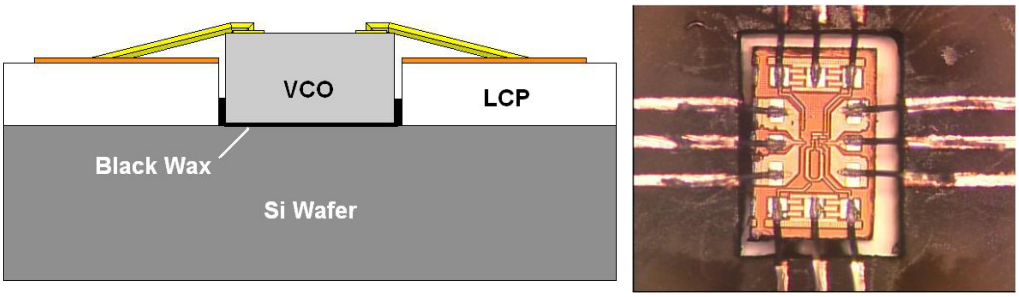
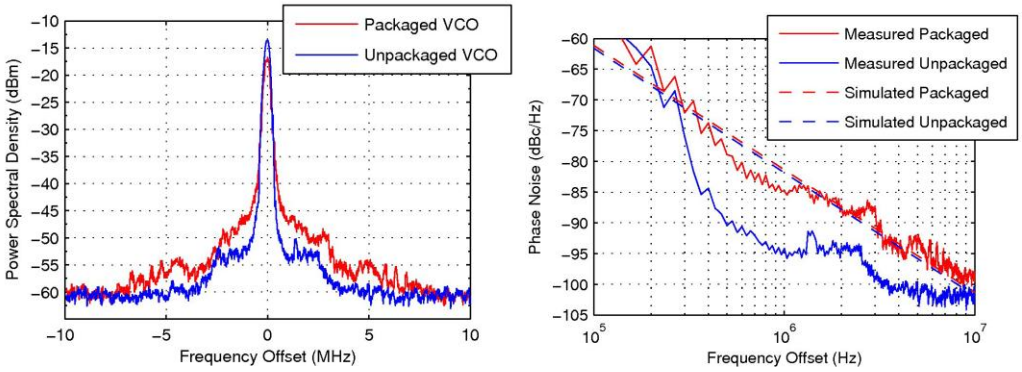



Figure 31. Wire Bonded oscillator on a Silicon carrier wafer [1].

Measurements after packaging (Figure 32) showed a figure of merit 13 dB down from the on chip measurements. Much of this degradation in oscillator performance was expected due to the wire bond connections. This can be improved by decreasing the length of wire bonds.

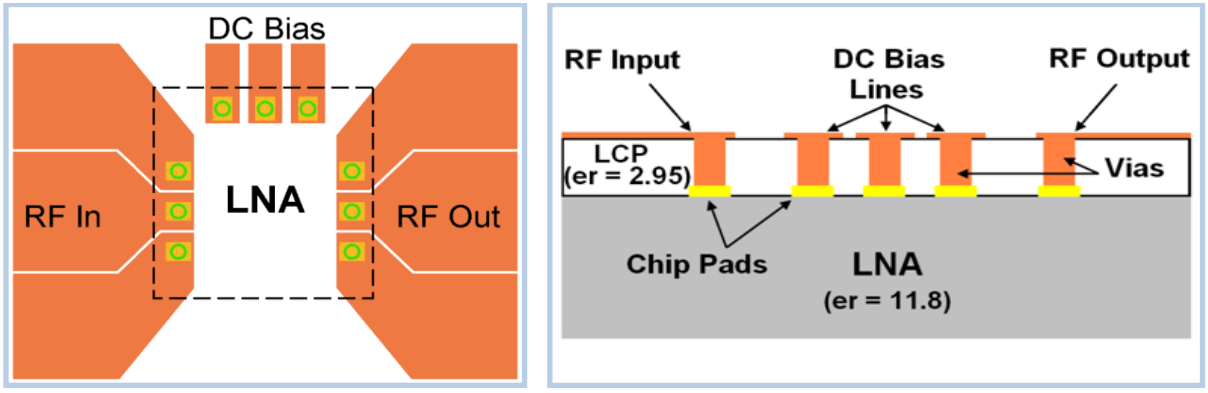



(a) (b)

Figure 32. (a) Output spectrum of the packaged and unpackaged VCO, (b) Phase noise of the packaged and unpackaged VCO [1]

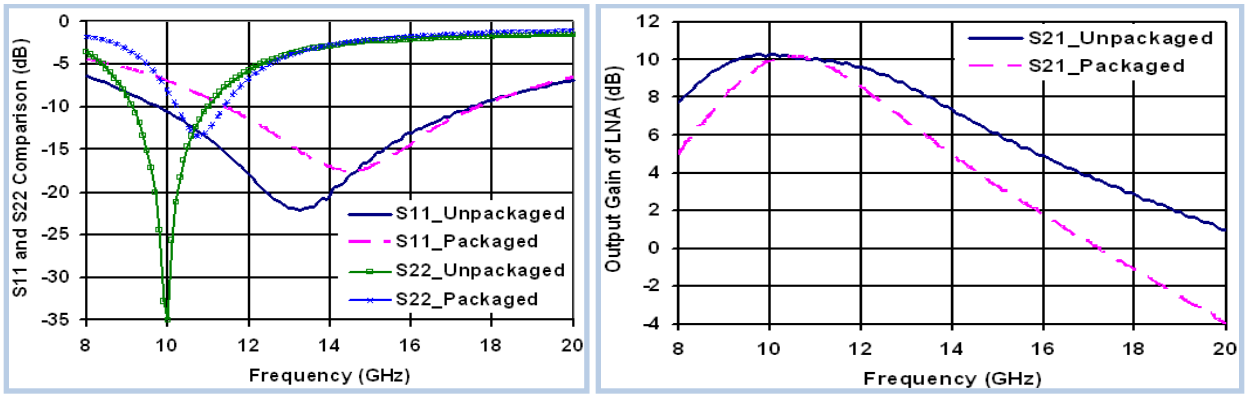
### 6.2. Via Interconnect

In this approach, the chips are fully embedded within the core layers and the interconnections to the pads of the chip will be done through via holes on the organic layer laminated on top of the SiGe (or GaN) chip. An X-band SiGe LNA has been successfully packaged while maintaining a high performance profile. The fabrication of the optimized package design is to laminate a layer of 2 mil LCP onto the LNA, then expose the chip pads by drilling 50 µm diameter via-holes through the LCP using an excimer laser (Figure 33). Measurements after packaging showed only a 0.1 dB of loss in the output gain and a 0.1 dB increase in noise figure (Figure 34).




(a) (b)

Figure 33. (a) Top view of the LNA package where LNA pads are connected through vias on LCP, (b) Cross-sectional view of the via interconnection build up




(a) (b)

Figure 34. (a) Comparison of S11 and S22 before and after packaging, (b) comparison of S21 before and after packaging [2]

### 6.3. Flip chip bonding

In this proposed process (Figure 35), the SiGe chip will be first flip chip bonded to the multilayer LCP pre-formed with vias and interconnects (Laminate 1). A second thick LCP layer will be recessed (by laser formed cavity) to fit the additional chip height and bonded with Laminate 1 using a bond ply material in between. The proposed concept will exert less stress to the die and is potentially a high volume manufacturing option. Figure 36 shows the process flow for achieving embedded chip package. A modified version of this embed chip concept is being implemented under the current NASA effort in collaboration with Prof. Cressler's group at Georgia Tech.

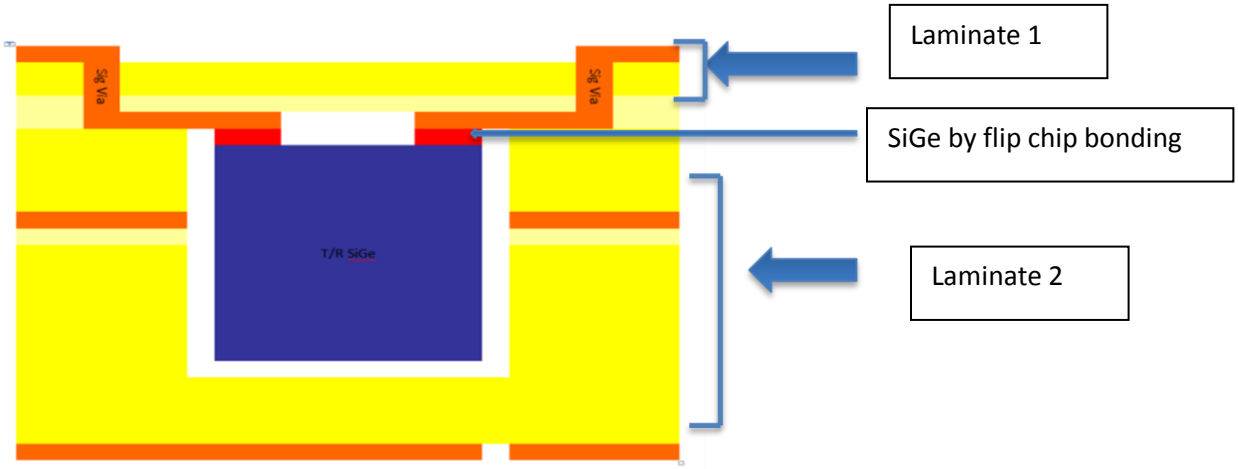



Figure 35. Flip chip bonded embedded SiGe chips in an LCP package

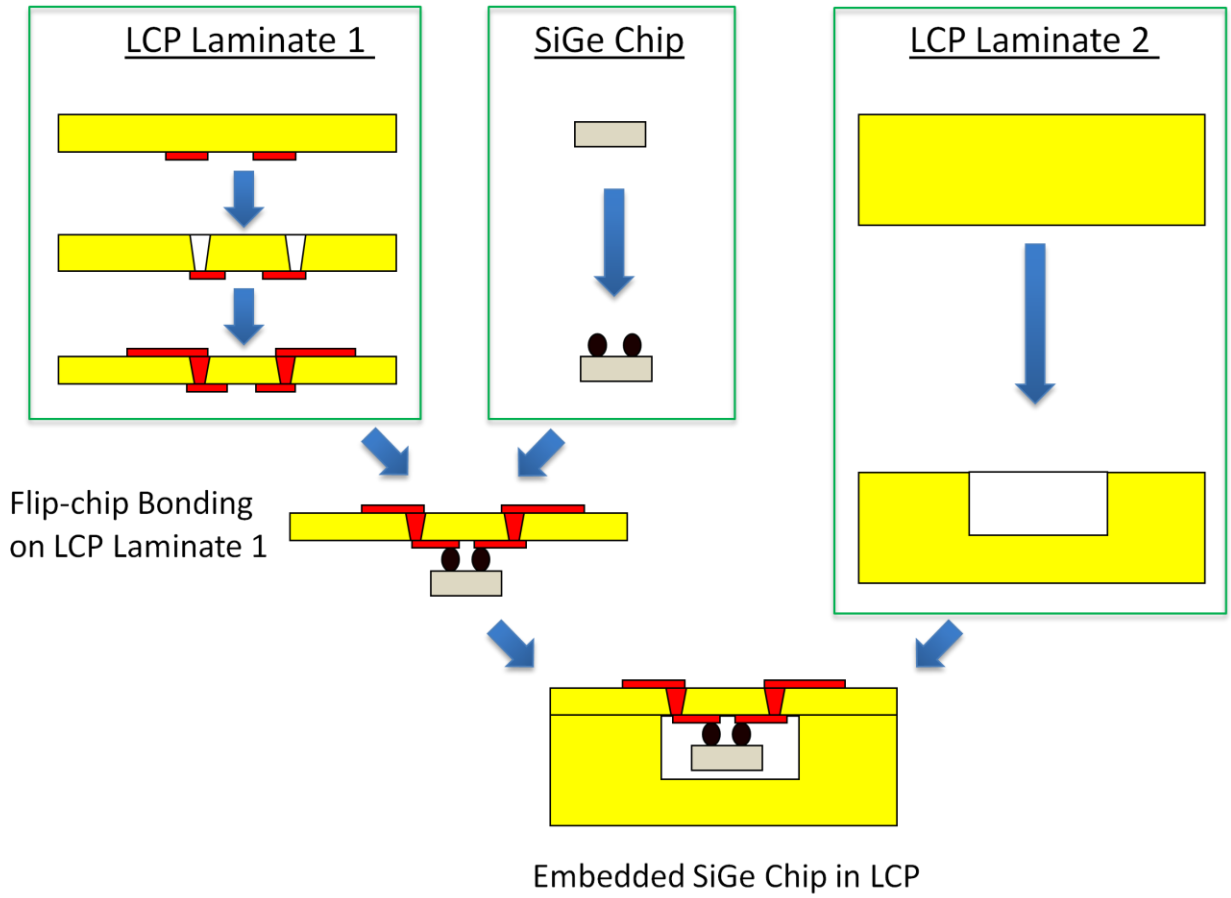



Figure 36. Process flow for the flip chip bonding and embedded chip construction

### 6.4. Modeling of Transmission Lines

Transmission lines for flip chip bonding shown in Figure 35 were modeled with three different configurations. The simulation results are presented in Figures 37 through 40.

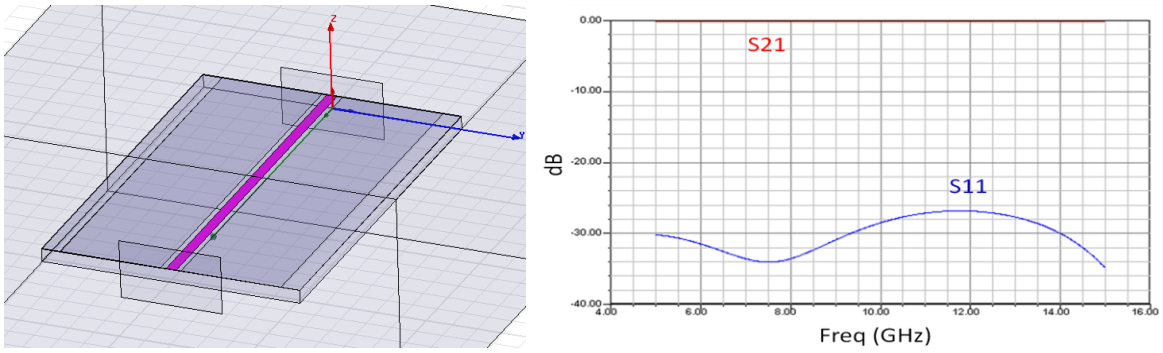



Figure 37. Modeled transmission line on SiGe stack up, 50 ohms CPW line on $SiO_2$/Si wafer, 275 micron thick wafer with 10 micron oxide layer.

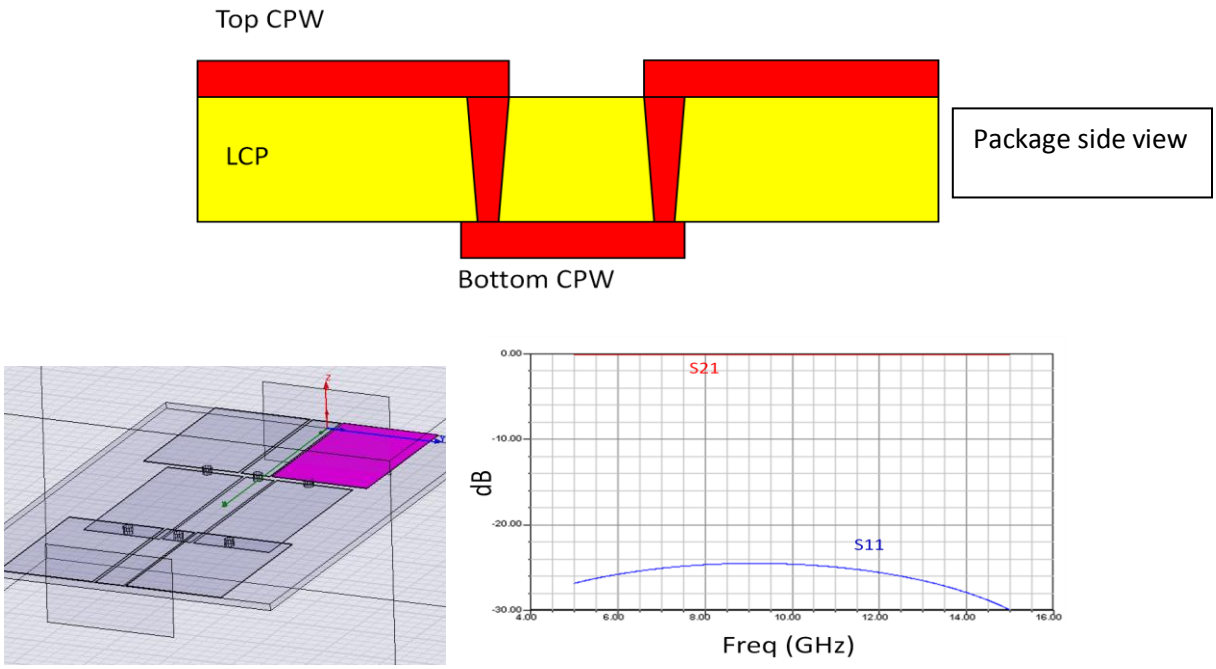



Figure 38. Modeled CPW 3-D transition on 4 mil thick LCP

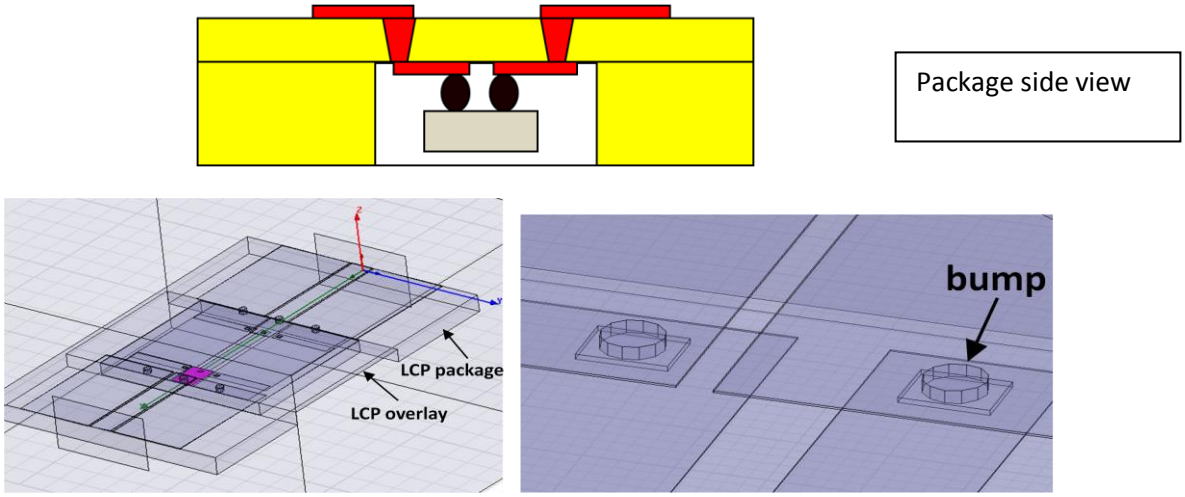
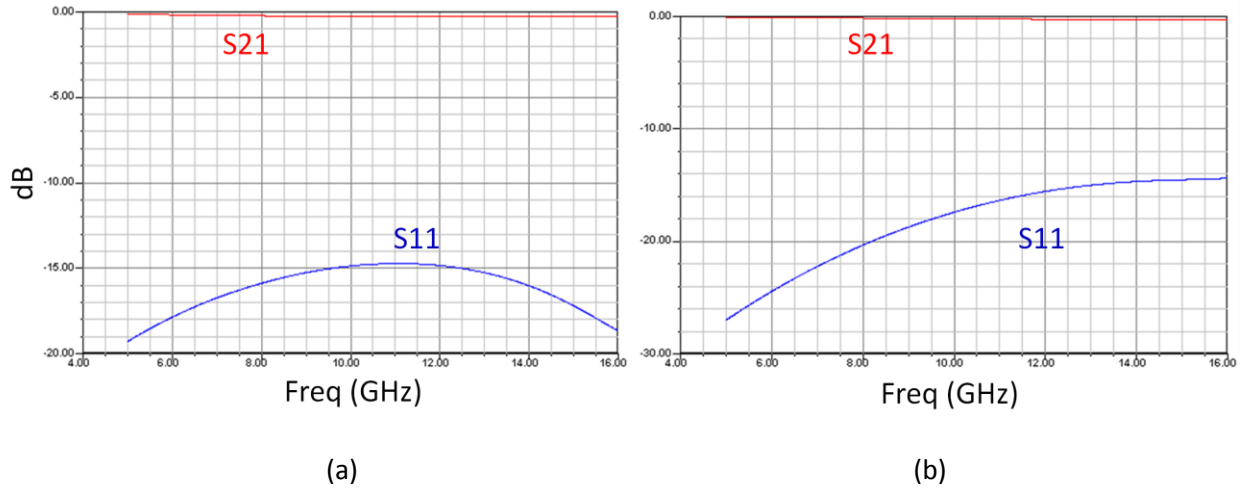



Figure 39. Flip chip LCP packaged Si. SiGe chip: 275 µm thick, LCP package: 11 mils, LCP overlay: 4 mils thick Total LCP: 15 mils.




(a) (b)

Figure 40. Simulated flip chip packaged Si chip (a) 7 micron bump height (b) 20 micron bump height.

## 7. System Trade Study

In order to better determine the trade-offs involved with a large integrated antenna array platform, a system trade analysis can be performed to analyze components design decision choices. In this example, impact of system performance of PA output power is analyzed with respect to radar SNR performance, cost, and dc power, with a radar FOM presented to help compare design choices.

### Example system design

The example system chosen for this trade study was developed as part of a NASA radar application to detect snow and ice from a UAV. The analysis presented is intended for a comparison between two different scenarios and not reflective of absolute radar performance for any specific application.

The phased array panel is an 8x8 element array where two different scenarios are proposed. The first scenario (Figure 41) has 1 T/R module per column (8 T/R) while the second has 1 T/R per element (64 T/R). The first scenario is based on a higher-power density array while the second is focused on a low-power density approach. The receive elements are constant between each scenario, with the appropriate losses being taken into consideration.

**Scenario 1 analysis: higher-power density**

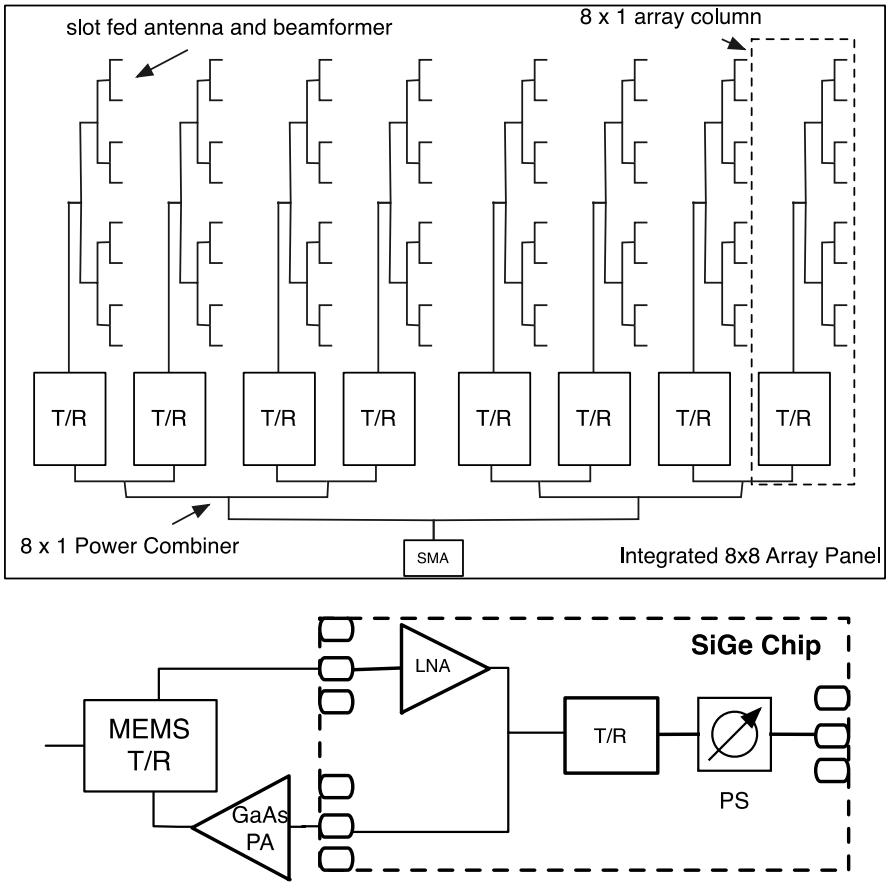



Figure 41. An 8x8 array with one T/R per column

For this scenario, an external GaAs PA is used in conjunction with a MEMS T/R switch (to be able to handle the high power) and SiGe T/R module, which contains an LNA and phase shifter. The PA is assumed to have 1.4 W output power, 25% PAE. The MEMS T/R has 0.5 dB of loss, and the RX path has 10 dB of gain and 2.5 dB noise figure. The beamformer has 4 dB of loss. Given this scenario and assuming an 8 km range, pulse integration, an appropriate RCS, the total received signal power is -78 dBW. The total noise power is -110 dBW. This yields a total SNR of 32 dB for scenario 1. The component cost totals $600 (MEMs T/R $30, PA $35, and SiGe T/R is $12). The dc power is approximately 45 W, mostly consumed by the PA. Results are summarized in Table 6.

Table 6. Trade study with 1 T/R module per column

| | | |
|---|---|---|
| PA power (1.4 W) | 1.46 | dBW |
| # PAs (8) | 9.03 | dB |
| switch loss | -0.50 | dB |
| feed losses | -4.00 | dB |
| Antenna Gain | 25.50 | dBi |
| Space Losses (tx) | -90.24 | dB |
| RCS + Integration | 31.00 | dB |
| Space Losses (rx) | -90.24 | dB |
| Antenna Gain | 25.50 | dBi |
| Feed losses | -4.00 | dB |
| switch loss | -0.50 | dB |
| # LNAs (8) | 9.03 | dB |
| LNA gain | 10.00 | dB |
| **RX signal power** | -77.95 | dBW |

| **Noise** | | |
|---|---|---|
| Feed losses | 4.50 | dB |
| RX noise figure | 2.50 | dB |
| kTB | -117.00 | dBWs |
| **Noise power** | -110.00 | dBW |

**Scenario 2: low-power density**

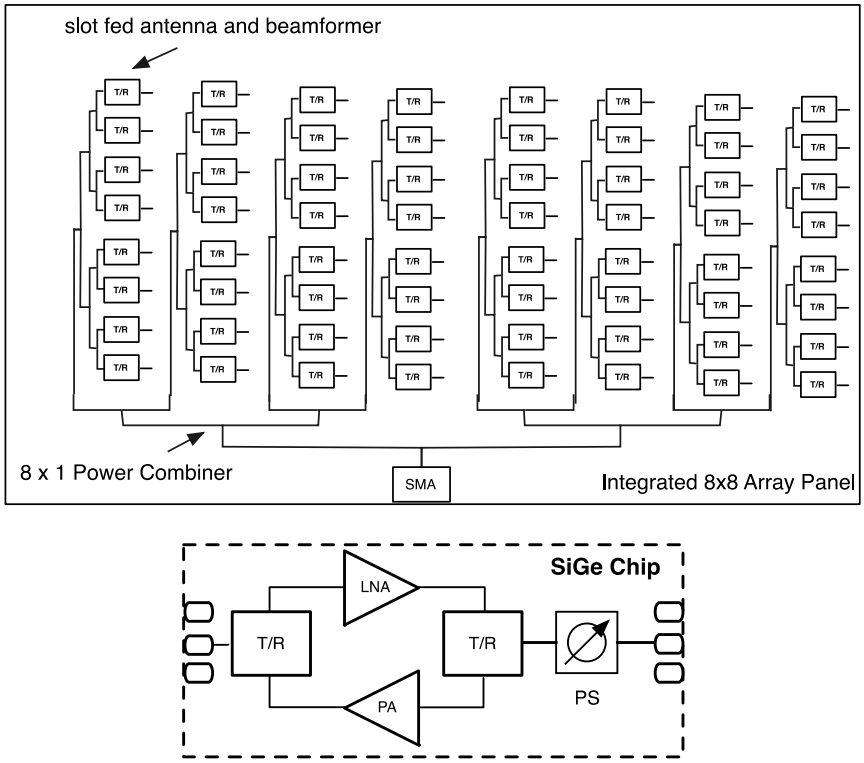



Figure 42. An 8x8 array with 1 T/R module per element

In scenario 2, a low-power, 15 dBm SiGe PA and CMOS output T/R switch (2 dB insertion loss) is integrated directly into the SiGe chip. The PA is limited to 15 dBm due to the compression point of the CMOS T/R switch. For this design, each antenna element will contain 1 T/R with a total of 64 T/Rs for the 8x8 array (Figure 42). Even though each element has 1 T/R, the total chip count only increases by 60% since each T/R block contains 1 chip instead of 3 as in scenario 1. In addition, since the T/R is directly connected to each element, the feed line losses will be minimal as compared to scenario 1.

Table 7. Trade study with 1 T/R module per element

| | | |
|---|---|---|
| PA pwr | -15.09 | dBW |
| # Pas | 18.06 | dB |
| switch loss | -2.00 | dB |
| feed losses | 0.00 | dB |
| Antenna Gain | 25.50 | dBi |
| Space Losses (tx) | -90.24 | dB |
| RCS + Integration | 31.00 | dB |
| Space Losses (tx) | -90.24 | dB |
| Antenna Gain | 25.50 | dBi |
| Feed losses | -4.00 | dB |
| switch losses | -2.00 | dB |
| # LNAs | 18.06 | dB |
| LNA gain | 10.00 | dB |
| **RX signal power** | -75.44 | dBW |

| **Noise** | | |
|---|---|---|
| Feed losses | 2.00 | dB |
| RX noise figure | 2.50 | dB |
| kTB | -117.00 | dBWs |
| **Noise power** | -112.50 | dBW |

Even though the PA output power is significantly lower, the total received signal power is almost the same as in scenario 1. This is due to the increased number of elements and reduction in feed

line losses on the transmit path. In addition, the RX noise will be improved, since the feed line losses will come after the LNA and is shown below.

For scenario 2, the SNR was computed to be approximately 37 dB, with total component cost of $768, with the T/R module costing $12 per chip. The total TX dc power assuming 30% PAE for the PA, is 6.6 W and receive power of 2.24 W, with a total power of 8.8 W.

**Analysis and Comparison**

In order to present an accurate comparison between these two scenarios, a FOM was created to allow comparison of radar SNR, *dc* power consumption, and cost.

---

The FOM are computed and comparison is shown in the Table 8.

Table 8. Results from FOM analysis

| | Scenario 1 | Scenario 2 | Delta (2-1) |
|---|---|---|---|
| **SNR [dB]** | 33.6 | **37** | 3.4 |
| **dc power [W]** | 45.0 | **8.9** | -31.4 |
| **Cost [$]** | **616** | 768 | -152 |
| **FOM ($/dB)** | 39.7 | **27.8** | -11.89 |

The FOM for the low power density array is approximately 12 $/dB better than the higher power density array.

In addition, other factors that are not taken into account include:

1) Assembly costs: if using integrated embedded SiGe T/R packaging technique, only small added costs for packaging additional elements, while for higher power density approach, packaging multiple chip types
2) Thermal management with higher power PA (active cooling, etc)

3) SiGe chip costs based on estimate of scale quantity, costs for a limited number of chips could be much higher.
4) Required real estate for packaging multiple chips versus a single chip.

## 8. Conclusions

Two T/R modules have been presented based on the previous work at Georgia Tech and its extension under the current Phase 1 award. Medium and lower power PAs were designed and their component level performance were measured. A system level trade study was conducted to discuss various options to meet the cost target and the performance goals which we expect to investigate further in Phase II.

## References


1. C. Patterson, S. Horst, S. K. Bhattacharya, J. Papapolymerou, J. Cressler, "Low cost organic packaging for silicon based mm-wave wireless systems", IEEE European Microwave Conference, Amsterdam, October, 2008, pp 1242-1245.

2. C. Patterson, T. Thrivikraman, S. K. Bhattacharya, J. Poh, J. Papapolymerou, J. Cressler "Organic wafer scale packaging of X-band SiGe low noise amplifier" IEEE European microwave Conference, Rome, October, 2009, pp 141-144.