FINAL REPORT:

DEVELOPMENT OF HIGH-VOLTAGE GAN-BASED DC-DC CONVERTER FOR RADIO ISOTOPE MICRO-POWER SYSTEMS

SPONSOR:

TRACE PHOTONICS INC., CHARLESTON, IL

SUBMITTED BY

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SUMMARY:

In this RIMS, major tasks for the Georgia Tech (GT) team is to develop a high-voltage gallium nitride (GaN)-based transistor technology that is customized for the DC-DC converter design for radio isotope micro-power systems. We worked closely with engineers at the Trace Photonics and developed high-voltage and low-leakage III-N transistors that may be suitable for high-efficiency trickle charging circuits in this project. During the project period, the fabricated devices are scalable beyond 500 V (up to 1 kV) and low leakage current (<100 nA @ > 500 V) of these transistors switches was achieved, which suggests tremendous reduction in energy loss to the switching element in a dc-dc converter when compared to silicon-based components. Several processing module to further reduce the leakage current in GaN transistors such as insulating-gate structure were also under development. It is expected that this transistor technology developed in the project may provide feasible solutions to the realization of inherently radiation-hard, high-temperature tolerant, high-voltage, and low-loss DC-DC converts for the innovative radioactive isotope micro power cells in a wide variety of harsh environment applications.

1 DC-DC Converter circuit development summary

In the design of a dc-to-dc converter for this project, the need for the GaN-based switching element in the pulse width modulation (PWM) circuits are highlighted in Figure 1. Since the off-the-shelf commercial PWM chips have standby power consumption (~ mW), this level of power consumption is not suitable for the RIMS cell implementation. As the energy resources becomes scarce in the RIMS batteries, GaN-based transistor switches that can operate at high-voltage (> 2 kV) and very low leakage current (< 10 nA), in additional to their high-temperature and high radiation hard nature, has emerged as an ideal choice of the dc-dc converter circuits in this project. In the initial development, the GT team worked with Ms. Doris Chan of Trace Photonics to investigate the rail to rail operational amplifier (Op-amp) comparators to generate the positive and negative dc source to power up the PWM circuit. The rationale is that the typical D-mode transistor switch would need both positive and negative d.c. power supplies for proper device operation. However, this requirement can be lifted by PWM control circuits were initially designed in the Advanced Design System (ADS) software and optimized on printed circuit board (PCB) using a off-the-shelf silicon components for circuit implementation while the new GaN transistors were developed in parallel. In the initial study, 500-V dc-dc converter was first designed and implemented. The PWM circuit has frequency range from 30 kHz to 105 kHz with duty ratio range from 5% to 95%. Initial Buck converter is designed with ideal PWM circuit and efficiency 92% to 63% depend on high side switch control signal. Low voltage Buck converter is also prototyped and tested efficiency is approximately 42% from calculation. High voltage 500 V to 5 V Buck's converter need to design and optimized for high side to low side switching circuits and efficiency. Alternative approach for low side switching converter and Flyback converter were designed and simulated by Trace Photonics. The research objectives were that the switching element of the dc-dc converters can be replaced by the GaN transistor switcher through a direct drop-and-replace system upgrade as the project moved along.

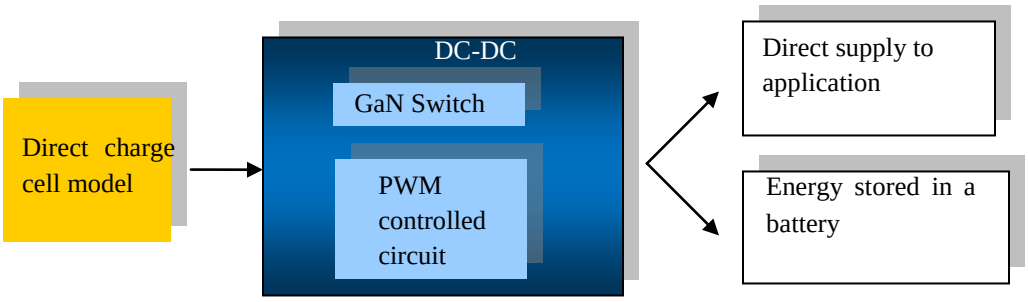
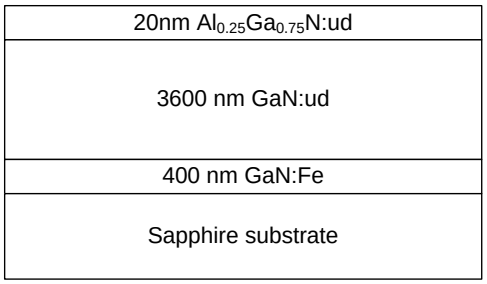


Figure 1. A schematic block diagram of the DC-DC power converter architecture used in the RIMS direct charge cell (Source: Trace Photonics, Inc., Charleston, IL)

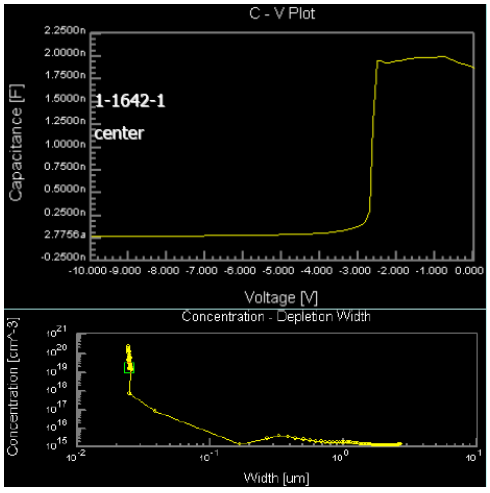
2 GaN HEMT development

2.1 GaN HEMT design and growth

A standard AlGaN/GaN HEMT was grown with a structure shown in Figure 2. The sheet charge resistance is around 700 Ω/square. The C-V measurement shows that the interface charge at the buffer and the substrate is not observable and the threshold voltage of this device is -3V. Based on our earlier device result, such layer structure may have a zero-gate-bias current density (I_{dss}) of 0.25 A/mm and will be verified in the new batch device fabrication. We have begun the device fabrication on this wafer batch and will expect to complete the first iteration device evaluation by the end of September to provide the measured I-V characteristics for circuit simulation.



(a)



(b)

Figure 2 (a) Standard GaN HEMT structure for the first iteration high-voltage HEMT switch development and (b) the corresponding C-V measurement

To extend the GaN HEMT measurement capability beyond 200 V in this project, we acquired a high-voltage digital curve trace from Agilent (Model B1505A) tha was delivered in Oct. 2009. The system is capable of measuring bare die and packaged high-voltage transistor switch up to 3 kV and be capable of storing high-voltage data digitally. The system is up and running for high power GaN HEMT evaluation. Due to the high substrate cost, we have used the GaN/AlGaN HFET grown on sapphire substrate in the first few months of the program to seek for proper device processing methodology. The fabricated GaN HFETs on sapphire have higher dislocation defect density due to poorer substrate quality and large lattice mismatch. These issues may contribute to the leakage current at ultra-high-voltage operation in our current fabricated devices. With the demonstration of high-voltage GaN HFET on sapphire substrate, we will extend the work to grow the GaN HFET structures on silicon carbide (SiC) platform in the coming months.

Based on our high-voltage leakage current assessment, we have ruled out several layer structures and will focus on the device structure as shown in Figure 3. In this layer structure design, the GaN HFET will be grown on a semi-insulating (S.I.) silicon carbide (SiC) substrate. A high-temperature aluminum nitride (AlN) buffer layer will be grown to obtain a smooth surface morphology for the subsequent GaN/AlGaN hetero-structure growth. The GaN/AlGaN heterstructure will be formed by incorporating 22 to 23% of the aluminum in the AlGaN layer to enhance the on-state resistance as well as to reduce the gate leakage current at high-voltage region. An AlN binary barrier will also be inserted in between the GaN and the AlGaN layer to further enhance the gate current blocking and the piezoelectric-induced 2-dimensional electron gas sheet charge density.

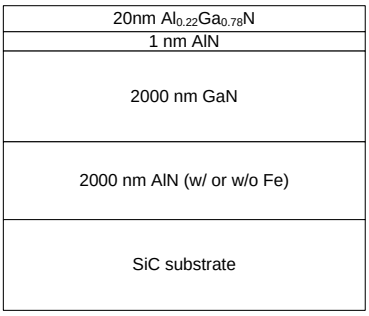


Figure 3 A GaN/AlGaN HFET layer structure design for the next-phase GaN switch development

It is believed that the residual silicon at the SiC/AlN interface may induce unnecessary parasitic conduction paths in the GaN/AlGaN HFETs. However, this issue was not studied in more detail in our prior GaN/AlGaN HFET growth on SiC substrates. To eliminate the problematic silicon-doping problem at the AlN buffer layer, the iron (Fe) doped in the AlN layer was proposed to help the Fermi-level pinning for the highly resistive buffer layer formation. For comparative study, we design in a series of GaN HFET growth variation in terms of the AlN buffer layer with and without the Fe doping, should the unexpected epitaxial layer quality degrade due to non-optimized growth conditions. The tasks are formulated as follows: 1) growth of the new layer structure on sapphire substrate to verify the effectiveness of the leakage reduction; (2) growth of the new layer structure on a quarter of a 2" SiC substrate with undoped AlN buffer layer; and (3) growth of the new layer structure on a 2" SiC substrate with Fe-doped AlN buffer layer. We hope to use this designed experiments to verify the effectiveness of the use of SiC substrate as well as a suitable AlN buffer layer design to further reduce the leakage current near device breakdown voltage.

2.2 Device Fabrication development

The processing development goals were set to explore the fundamental fabrication and material growth limitation of the GaN HFET devices under high electric field stressing conditions. It is clear that the gate leakage current may need to be reduced further in our current devices. We worked on the following items in a hope to achieve this goal: 1) the use of SiC substrate to achieve a lower dislocation density for reduced gate leakage current, 2) the use of an insulating gate structure for suppressed gate leakage path, and 3) the investigation of the impacts of the surface passivation methods and their effectiveness to further reduce the surface leakage path. We have used bisbenzocyclobutene (BCB) passivation in our current wafer runs (on sapphire substrates) and have achieved sub-micro-ampere leakage on selected devices up to kV

ranges. To further exploit ultimate surface passivation for such devices at high-voltage regime in the future, a thin layer of aluminum oxide (Al_2O_3) by atomic layer deposition can be applied for possible device passivation and for a metal-insulator-semiconductor (MIS) gate structure for further gate leakage current reduction. We also worked on the device singulation and the packaging of the current fabricated devices into a TO-220 high-voltage discrete transistor package for circuit integration.

In fabrication processing development, we have been focusing on further reduction in the device leakage current. Major research task is to rectify the source of leakage path in the GaN HEMTs grown on sapphire substrates. The first task is to reduce the surface-induced leakage path on the GaN devices. The photoresist residue and surface states usually contribute to the premature device breakdown at high voltage operation through the arcing. As shown in Figure 4, using a set of designed experiment, we have successfully removed the origin of the photoresist residue issue and have obtained a clean surface, which enabled us to further exploit high voltage characteristics of the transistors.

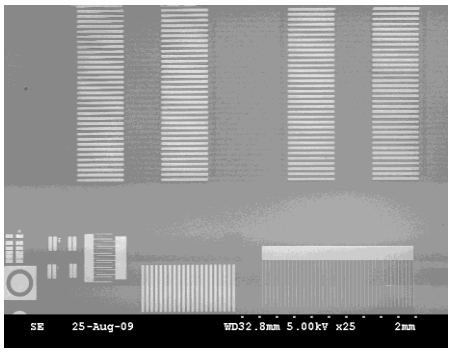


Figure 4 SEM photographs showing a clean surface of fabricated HEMT devices with improved processing steps to eliminate the residual photoresist deposition after metal lift-off step.

The evaluation of leakage paths were conducted through the I-V measurement between etched mesas and etched surfaces. The distance of two electrodes on isolated areas (on etched surface) was set at 32 microns and the leakage current was measured up to +/- 200 V. With cleaned surface that is free from the photoresist residue, the best leakage current between the electrodes on the undoped GaN layer can be in the sub-nA range at 200 V, indicating the leakage through the isolation layer may be well controlled. However, the isolation leakage current is not uniform across a two-inch wafer, suggesting the non-uniform buffer leakage may still exist across the wafer. Nevertheless, the epi-wafer quality is reasonably acceptable for the first iteration high-voltage device performance evaluation.

In our baseline fabrication processing, we used the BCB as a standard passivation material. This material has shown stability in reproducing low device leakage up to 200 V. However, as the operating voltage increases, we recently observed abnormal material dissolution phenomena at high-voltage operation. It is hypothesized that the BCB films we used may not be fully cured and may suffer from processing variation due to accidental exposure of oxygen during the curing process. We are looking in to this issue closely by curing the samples in different vacuum ovens with extended nitrogen purging cycles, in a hope to retain processing control in this critical step. On the other hand, a new passivation was sought in an atomic layer deposition (ALD) system. We have gained access to an ALD system in the Georgia that is capable of depositing nanoscaled aluminum oxide with monolayer precision. Based on recently

research, ALD-grown Al_2O_3 may be used to passivate GaN HFETs and possibly be used as a gate dielectric layer for the formation of the metal-insulator-semiconductor (MIS) FETs. The MISFET will be able to provide a leakage current of less than 1 nA at voltage as high as > 1kV.

2.3 Device characterization

Due to the delayed equipment delivery of the high-voltage curve tracer, we were not be able to complete the precision high-voltage measurement setup in this month. However, we managed to setup an interim measurement system with two 6-1/2 digital multimeter (HP 34410A) for current sensing, one low-voltage power supply (up to 40 V), and one high-voltage power supply (Stanford Research PS350, up to 5 kV) for preliminary high-voltage device performance study. Shown in Figure 5 is a schematic drawing for the high-voltage transistor measurement setup.

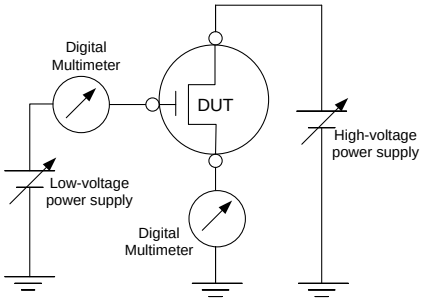


Figure 5 A schematic system setup for a preliminary high-voltage GaN transistor measurement.

The minimal detectable current is 10 nA for the digital multimeters used in this measurement. The drain leakage current is assessed as the sum of the gate leakage current and the source leakage current. As shown in Figure 6, the low-voltage current-voltage characteristics of a GaN HFET with a drain-to-gate distance (L_{dg}) = 100 μm shows that the device has a pinch-off voltage of ~ -1.5 V and an on-state resistance of 340 Ω at V_{GS} = 0 V was achieved. The leakage current at 200 V is < 20 nA (not shown here) was measured using a high-precision semiconductor characterization system (Keithley SCS 4200). It is also identified that major leakage current component comes from the gate leakage current at low voltage regime, meaning that the buffer leakage of GaN HFETs grown on sapphire substrates may be well controlled.

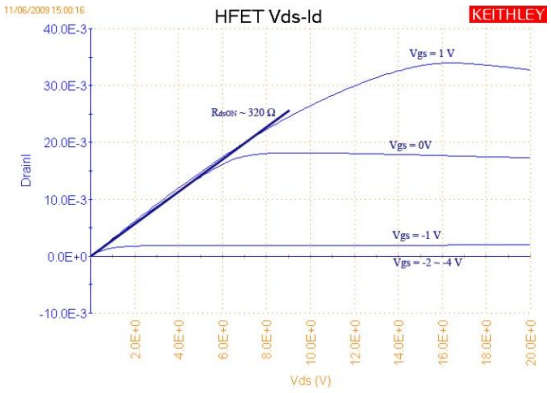


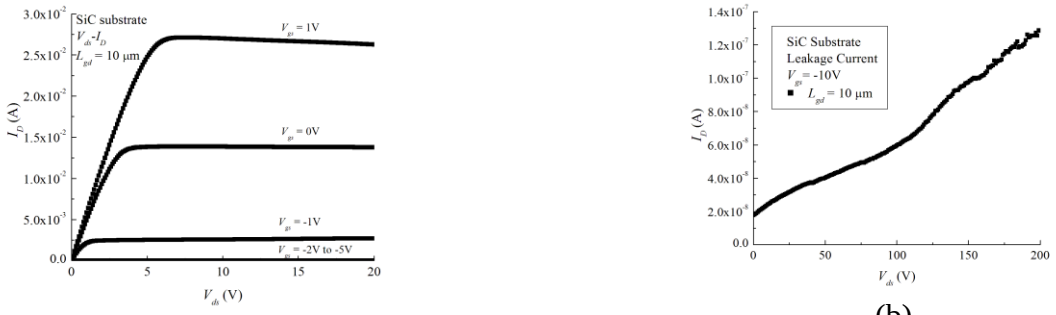
Figure 6. A common-source I-V characteristic of a fabricated GaN HFET (wafer ID: 1-1639-4, block: E3) with the L_{dg} = 100 μm, L_g = 3 μm, and W_g = 0.3 mm. At V_{GS} = 0 V, the $R_{ds(ON)}$ is ~ 320 Ω.

Shown in Figure 9 is a set of high-voltage measurement results that utilize the interim measurement setup shown in Figure 5 for the same device. As shown in the pictures, the GaN HFET is biased at a gate bias voltage of -5 V and the V_{DS} is biased at 500 and 1 kV, respectively. As shown in Figure 9 (a), the gate current (I_G) is 210 nA and the source leakage current (I_S) is < 10 nA (not detectable by the measurement system). The resulting drain leakage current (I_D) is ~

210 nA at V_{DS} = 500 V. As V_{DS} increases to 1 kV (Figure 9 (b)), I_G = 330 nA and I_S = 370 nA (, or I_D = 700 nA) are measured. This particular device can operate up to 1.1 kV before the leakage current hits the 1 μA mark. We are also in the process to collect more device data on different device designs to explore possible $R_{ds(ON)}$ and breakdown voltage (*BV*) design trade-offs in this batch of devices for better understanding of the device scaling issues in higher blocking voltage designs.

To achieve low leakage current GaN HEMT for operation at 500 V and beyond, our October report identified that the gate leakage current component may need further study. To reduce the channel leakage, the dislocation density and the mismatch in the substrate may play roles in the device performance improvement. We have acquired the GaN HFET on SiC substrates from Prof. Dupuis' group this month. In task (1), two GaN HEMT layer structures were grown on semi-insulating (S.I.) silicon carbide (SiC) substrates. Due to different growth schemes, the high-temperature (HT) AlN buffer layer is inserted, when compared to typical GaN HEMTs growth on sapphire substrates. Standard AlGaN/GaN heterojunction without a GaN cap layer were grown on these wafers with undoped and Fe-doped HT-AlN buffer layer designs to explore possible reduction in the channel leakage arising .

Shown in Figure 7 is the preliminary device obtained after the Schottky gate metal formation without any surface passivation. The fabricated GaN HFETs (wafer ID: 1-1740-6) has a gate width of 150 μm and the gate-to-drain distance (L_{gd}) is 10 μm. In Figure 7(a), the HFETs shows I_{dss} = 12 mA at V_{gs} = 0 V. The corresponding on-state resistance is about 200 Ω at V_{gs} = 0 V and the pinch-off voltage is < -3V. At V_{gs} = -10 V, the drain leakage current is 120 nA at V_{ds} = 200 V (Figure 7(b).) For comparison, the leakage current measured in test devices grown on sapphire substrates typically exceed 200 nA at such biasing conditions. It is expected that further reduction in off-state leakage can be reduced with lateral device scaling and surface passivation.



(a) (b)

Figure 7. Device results of a fabricated un-passivated GaN HFET. Note that the device performance is evaluated on a processing control monitoring (PCM) devices for processing control purpose. This device has a relatively short L_{dg} design (L_{dg} =10 μm) and the leakage current corresponds to the leakage at the electric field of 200 kV/cm. It is expected that the leakage current for wider Ldg will be less than the PCM devices.

As expected, we found that the leakage current is mostly dominated by the gate leakage current, even at a relatively low voltage stress (< 200 V). A proper device passivation step will

be desired. In this part of study, we continued using the GaN HFETs grown on the sapphire wafers to investigate possible ways to get a lower leakage current at high voltage regime with focuses on operating voltage of 500 V and beyond. Three tracks of the study were conducted. The first approach is to study different passivation schemes in our currently fabricated HFETs

We studied GaN HFETs passivation using the ALD-grown Al_2O_3 layer. For valid evaluation, the measurement was extended to 500 V to exploit the leakage performance in such region. The devices under evaluation have L_{gd} of 50 μm and 100 μm, respectively, because they are the devices intended for >1-kV DC-DC converter implementation. As shown in Figure 8, the devices with L_{gd} = 50 μm showed leakage current of < 150 nA, which is similar to that obtained in devices using BCB passivation (in terms of the order of magnitude). However, the devices with L_{gd} = 100 μm showed higher leakage current. The result is not consistent with the expected device scaling and this discrepancy may indicate that the Al_2O_3 passivation processing is not optimal and annealing of ALD aluminum oxide may be required. Detailed study will need to be explored.

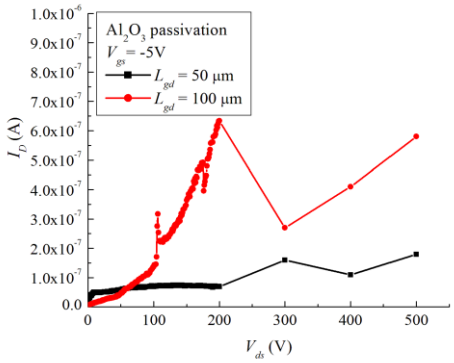
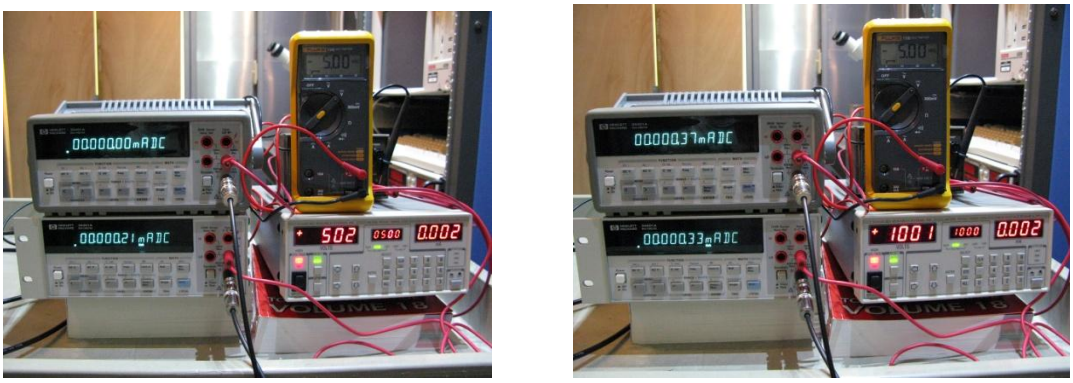


Figure 8 Evaluation of the drain leakage current for device passivation using ALD-grown Al_2O_3 layer (sample ID: 1-1643-2-2-4).

Another approach to extend the device breakdown is to use the lateral device scaling. Using the BCB passivation scheme, we studied the leakage current performance for devices with different L_{gd}. As shown in Figure 9, the leakage current on devices measured across the fabricated sample (wafer ID: 1-1639-4). It is shown that the leakage current stays in the few hundred nano-ampere ranges for devices having L_{gd} varied from 25 to 100 μm. The results also indicated that a wider L_{gd} may not offer advantages in lowering the drain leakage current but at the cost of higher on-state resistances for 500-V application. It is also an indication that the leakage current component may not come from the intrinsic channel property but from extrinsic part of the device such as dielectric passivation or sidewall leakage paths that are somehow connected to the gate electrode. Further study on the leakage current identification will continue throughout this program. Based on current device available, we will use devices with L_{gd} =25 μm for the 500-V DC-DC converter demonstration. It should be noted, however, that the current results may also include possible leakage paths in this measurement system. The actual leakage current for the fabricated high-voltage GaN HFETs may be much smaller than the reported values. In summary, the fabricated devices can be incorporated into the 500-V GaN switch modeling and circuit implementation for a quick 500-V-to-5-V dc-dc converter demonstration in the future.



(a) (b)

Figure 9 High-voltage measurement results of the same device shown in Figure 6 at (a) V_{DS} = 500 V and (b) V_{DS} = 1,000 V, respectively. The values shown on the right (from top to bottom) are V_{GS} and V_{DS}, respectively. The values shown on the left instruments (from top to bottom) are I_S and I_G, respectively, at the transistor switch-off state. Note that the least significant digit of the digital multimeters corresponds to 10 nA in the display.