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A 2×6b 8GS/s 17–24GHz I/Q RF-DAC based Transmitter in 22nm FDSOI CMOS

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Abstract—We describe a 2×6 bit Cartesian RF IQ-modulator, implemented on 0.15 mm² in a 22 nm FDSOI CMOS technology. Measurements show a 3 dB bandwidth of 17–24 GHz and a saturated output power of 10.4 dBm with a peak drain efficiency of 15.6 %. The IQ-modulator has been verified up to 8 GS/s. To the best of our knowledge, this is the highest-frequency CMOS RF IQ-modulator using sub-50 %-duty-cycle LO signals, and the highest sample rate reported for >3 bit fully integrated Cartesian IQ-modulators.

Index Terms—IQ-modulator, RF-DAC, SOI CMOS

I. INTRODUCTION

THE continuing demand for higher data rates drives the need for increased spectral resources at higher carrier frequencies. High data rates and small antenna separation at mm-wave frequencies necessitate high integration. CMOS implementation of mm-wave transmitters enables tight integration of high-efficiency digital circuits with analog front ends at modest power levels suitable for array antennas [1].

RF-DACs are a promising alternative for CMOS mm-wave transmitter realizations [2]. They have been demonstrated for frequencies from a few GHz to beyond 60 GHz [2]–[8]. For complex modulation formats, RF-DACs can be used in a polar or a Cartesian configuration. The polar IQ-modulator applies amplitude and phase in two separate steps, requiring these signals to be time-aligned with sub-sample precision [5], which is very challenging for wideband signals. The Cartesian IQ-modulator uses two RF-DACs with a 90° phase offset to generate I- and Q-components; but combining these without losses and impairments is complex. Direct summation of the RF components causes cross-modulation distortion; this may be addressed with 2D digital predistortion (DPD) [2], which is however considered unrealistic for high-bandwidth systems [1]. A proper combiner can avoid such distortion, at costs in loss and area. Alternatively, the use of sub-50 %-duty-cycle LO signals has shown good results for low-GHz RF-DACs in CMOS [3], and at higher frequencies in BiCMOS [9].

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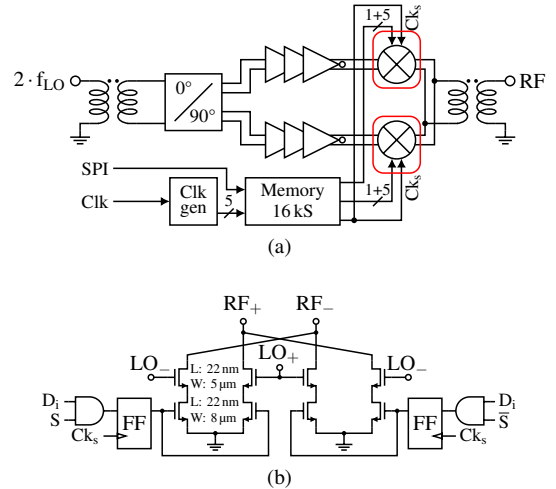


Fig. 1. (a) IQ-modulator block diagram with full RF path and on-chip supporting circuitry. RF-DACs are marked in red. (b) Unit-cell schematic, excluding biasing, including flip-flops (FFs) used for data timing alignment between branches. The data-bit D_i and sign-bit S determine the output level.

Here, we present a 22nm-CMOS, 8 GS/s, 2×6 bit Cartesian IQ-modulator operating at 17–24 GHz using sub-50 %-duty-cycle LO signals. In addition to the high carrier frequency, we have focused on maximizing the sample rate, and thus the achievable bandwidth and/or oversampling ratio.

II. RF IQ-MODULATOR DESIGN

A block diagram of the modulator is shown in Fig. 1a. An LO at twice the RF frequency is used to generate four sub-50 %-duty-cycle, 0° and 90° LO signals, which drive the RF IQ-modulator through inverter-chain buffers. The digital baseband (BB) signals are fed from an on-chip memory.

A. Unit cell, DAC cores, and modulator

The unit cell topology greatly affects the performance of the RF-DAC. The RF-DAC output levels can either be generated through bitwise cancellation, keeping all unit cells constantly active [4], [10], or through deactivation of the unit cell by cutting its bias using the data switch [2], [11]. A top-placed data switch brings some LO leakage suppression, which can be further improved by gating the LO signal with the data signal [2], however potentially at the cost of peak performance.

Our unit cell topology (Fig. 1b) combines sign generation and LO leakage neutralization, while allowing unused unit cells to be deactivated, which reduces the power consumption.

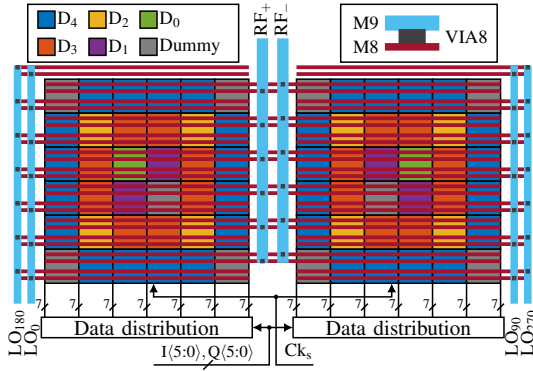


Fig. 2. Floor plan of the RF IQ-modulator core, including LO, RF and BB routing and color coded unit cell placement according to their binary grouping.

Two balanced mixers with top-placed LO switches generate the three signed output levels [-1, 0, 1]. The dual mixers provide symmetrical leakage paths from both LO signals to each RF output, bringing inherent LO leakage neutralization. In-cell flip-flops (FFs) reduce data-switching skew.

The floor plan of the RF IQ-modulator is shown in Fig. 2, which highlights the common-centroid placement scheme [12] used for the unit cells. To ensure equal delays from LO input to RF output for all unit cells, the distribution and collection of the LO and RF signals are done through two mirrored differential ‘F’-shaped nets. The signed unit cells allow for digital suppression of DAC-level LO leakage within ± 0.5 LSB per DAC. An H-tree (not shown) is used for distributing the clock within each DAC core.

B. Quadrature LO generation

Two cross-coupled current mode logic (CML) latches divide a double-frequency LO into sub-50% duty cycle, 0° and 90° LOs. Four 17-stage inverter buffer-chains increase the drive strength sufficiently to switch all the DAC LO transistors. DC-block capacitors located at both the input and output of the buffer chains allow for free tuning of the RF-DACs LO input bias level and also for adjustments of the duty cycle. The duty-cycle control uses the longer rise- and fall-times at the divider output in combination with DC bias level at the input of the buffer chain to tune the duty-cycle. The LO generation was designed to enable studies of the benefits of non-overlapping LO signals rather than to achieve the highest system efficiency.

C. High-speed on-chip memory

To evaluate the design, a variety of digital BB I/Q waveforms must be sent to the modulator at a high sample rate. A 16 kS, 8 GS/s SRAM is used to generate these signals within the chip, thus avoiding the challenge of off-chip interconnects. A low-speed serial interface is used to program the memory.

D. Input and output matching

The RF IQ-modulator was designed to operate at 28–31.5 GHz. Both input and output matching were implemented with EM-simulated interleaved baluns, using the

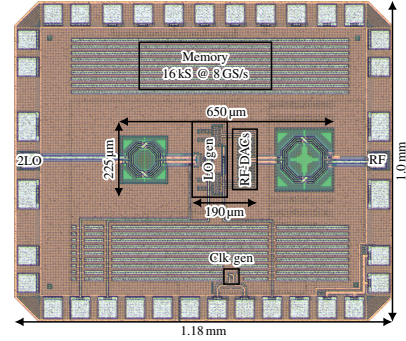


Fig. 3. Chip photo of the 17–24 GHz RF IQ-modulator. Core area is dominated by the input and output baluns. Total chip area is pad-limited.

two topmost metal layers, and shunt MOM capacitors to tune in the desired band. The divider-based LO generation required the LO input to be tuned for twice the operation frequency.

III. EXPERIMENTAL RESULTS

The RF IQ-modulator was implemented and fabricated using a 22 nm FDSOI process. A chip photo is shown in Fig. 3. The entire design measures 1.0 mm \times 1.18 mm, of which the core uses 225 μ m \times 650 μ m (225 μ m \times 190 μ m without baluns).

The design was evaluated up to the full memory speed of 8 GS/s using the coplanar 2LO and RF pads as the calibrated reference planes. The clock and data distribution within the DAC cores consume a maximum of 18.5 mW.

A. Continuous-wave measurements

The static properties of the RF IQ-modulator were evaluated with a Keysight PNA-X vector network analyzer. The analog bandwidth and peak RF power of Fig. 4a have been measured with all cells active in both RF-DACs. This figure also shows the DC power consumption for the divider and LO buffers, and for the output stage excluding its digital circuits. The measured 3 dB CW bandwidth is 17–24 GHz; IQ phase imbalance grows rapidly at lower frequencies. At each frequency point, the input bias on the inverter buffers was adjusted for a minimum I/Q imbalance and to yield a 3dB increase when both I and Q branches are active as opposed to one branch only. The peak saturated output power is 10.4 dBm, while the output stage consumes 70 mW, resulting in a drain efficiency of 15.6%. LO generation and distribution power is 330mW at 21 GHz.

The CW frequency range was lower than expected. An observed 15% reduction in the output match center frequency is referred to unaccounted-for inductance in the RF-DAC routing. Also, an undersized supply net for one LO buffer stage further reduces the measured CW frequency range compared with the target. It also reduces the duty cycle tuning range, which limited our possibilities to fully investigate the benefits of non-overlapping LO signals.

The vector output signal for all code-word combinations are shown in Fig. 4b. A small I/Q output level difference and a small phase rotation can be noticed. The curtain-like phase drift patterns change with the code-word sweep direction and is expected to originate from the test setup.

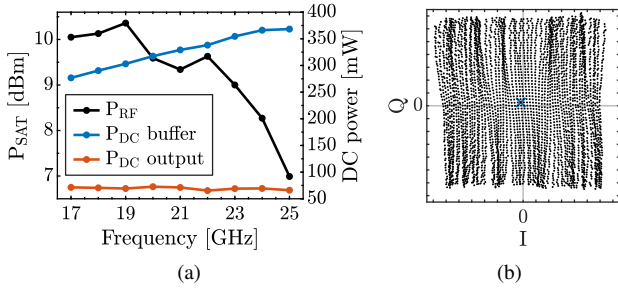


Fig. 4. Measured CW characteristics. (a) RF and DC power at maximum DAC settings. (b) Static RF behaviour measured for all different digital code words. The blue cross marks when both RF-DACs are off, showing a LO leakage corresponding to around one LSB.

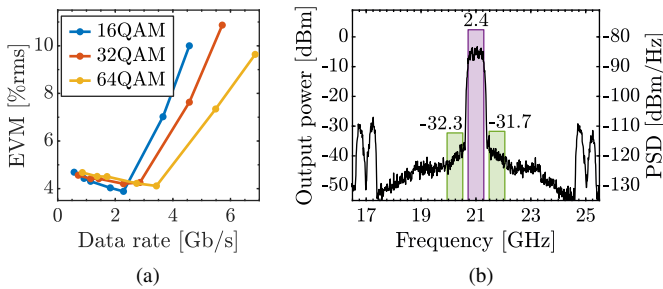


Fig. 5. (a) EVM for various data rates and modulation formats with static errors compensated for. EVM for an ideal 2×6 bit IQ-modulator is 0.8%. (b) Output spectrum for constellation shown in Fig. 6c. Purple bar shows the total signal power; green bars show leakage power in the neighbouring channels.

The true performance of the LO leakage neutralization provided by the symmetrical unit cells has not been possible to verify with measurements. A LO leakage of -29.3 dBc was measured with all unit cells disabled, as shown in Fig. 4b. Post-fabrication simulations reveal DAC-level routing as the probable cause of this leakage. With digital compensation, a minimum leakage of -39.7 dBc was achieved.

B. Wideband modulated measurements

Dynamic performance was evaluated with 16-, 32-, and 64QAM single-carrier signals at 21 GHz. Signals were $7 \times$ oversampled and RRC-filtered (factor 0.35) in the digital domain. At each configuration, I/Q-gain and phase imbalance and LO leakage were compensated for through digital I/Q offset and scaling; no 2D DPD was used. Biases were chosen for best performance at high rates and kept unchanged for lower rates. The RF output signal was captured using a Keysight PNA-X vector network analyser operated in spectrum analyser mode. Measured EVM for various data rates are presented in Fig. 5a; a representative spectrum is shown in Fig. 5b. Fig. 6 shows constellations for some of the datasets. The reduced power spectral density at higher bitrates limit EVM and ACPR while compression artifacts remain very small, indicating that performance is limited by switching noise and clock jitter rather than by cross-modulation. The slight EVM degradation at low bitrates is not reflected in ACPR, indicating noise rather than a nonlinear origin.

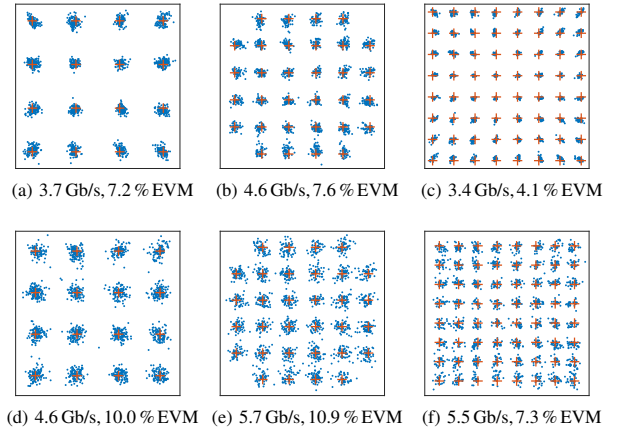


Fig. 6. Measured constellation diagrams at 21 GHz and 7 samples per symbol for various modulation formats and data rates. The results include a static digital compensation of I/Q gain and phase imbalance.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART.

	This work	[2]	[4]
Technology	22 nm SOI	28 nm	45 nm SOI
Resolution [b]	2×6	2×10	2×6
Sample Rate [GS/s]	8	2	6.5
Frequency (3 dB BW) [GHz]	17–25* (17–24)*	20–32 (–)	15–32 (18–32)
Supply voltage [V]	0.9	1	4.5–6
Peak Psat [dBm]	10.4	19.0	19.9
Drain eff. [%]	15.6	34.4	15.6
Peak energy eff. [pJ/b]	24.6	48.7	80.0
Modulation format, Data rate [Gb/s], Oversampling ratio, EVM [%rms], ACPR [dBc]	16QAM, 4.6, 7, 10.0, -23.3 ; 32QAM, 4.6, 7, 7.6, -24.6 ; 64QAM, 3.4, 7, 4.1, -34.1	64QAM, 3, 4, 3.6, -33.6 ; 256QAM, 1, 16, 2.8, -32.4	16QAM, 26, 1, 7.9, $-$; 32QAM, 30, 1, 6.9, $-$; 64QAM, 12, 1, 4, $-$
Area (core) [mm ²]	1.18 (0.15)	1.6 (0.2)	2.42 (–)

* Working range limited by IQ phase imbalance

RF IQ-modulator performance is compared with other implementations in Table I. For 64QAM, we achieve an EVM of 4.1% at 3.4 Gb/s. At the full sample rate of 8 GS/s, 16QAM is still viable with an EVM of 10% [7]. The peak CW power is 10.4 dBm; the higher power in [4] is achieved with cascodes while [2] uses a significantly larger total transistor area. The average power for 64QAM is 2.4 dBm, while the output stage consumes 25.9 mW, for an average drain efficiency of 6.7%.

IV. CONCLUSION

We have presented a 2×6 bit, 8 GS/s, 17–24 GHz RF IQ-modulator implemented in a commercial 22 nm fully depleted SOI CMOS process. The design demonstrates the feasibility of using sub-50%-duty-cycle LO signals for CMOS RF DACs at tens of GHz. As far as we know, this is the highest-frequency CMOS RF IQ-modulator using this principle, and the clock rate is also the highest reported for a >3 bit fully integrated Cartesian modulator.

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