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Analytical Conduction Loss Calculation of a MOSFET Three-Phase Inverter Accounting for the Reverse Conduction and the Blanking Time

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***Abstract*—The reverse conduction capability of MOSFETs is beneficial for the efficiency of a three-phase inverter. In this paper analytical expressions in closed form are presented which allow to quickly evaluate the conduction losses, considering the effect of the reverse conduction and blanking time for both sinusoidal PWM operation with and without third harmonic injection. The losses of a three-phase SiC MOSFET inverter suitable for traction applications are estimated with the proposed method and show good agreement of about 98.5 % with measurements, performed with a calorimetric setup.**

***Index Terms*—Analytical models, calorimetry, power MOSFET, pulse width modulated inverters, traction motor drives.**

I. Introduction

The thermal capability and the low switching losses of silicon carbide (SiC) MOSFETs can be beneficial in comparison to classical silicon (Si) IGBTs when used in a three-phase converter [1]–[4]. Available comparisons between SiC MOSFET and Si IGBT based converters show that SiC MOSFETs can achieve a more compact inverter design, while improving the system efficiency [1], [2]. Especially at high switching frequencies and high junction temperatures, the converter efficiency can be increased using SiC MOSFETs [2]–[6]. Furthermore, MOSFET based converters, as described in [7]–[11], have also reduced conduction losses at partial load operation. In [12]–[16], extensive work has been done to derive analytical switching-loss models.

However, the available comparisons in [1]–[9] are mainly based on analytical conduction-loss models in the literature [17]–[20] or provided by semiconductor manufacturers' application manuals [21], [22] for different IGBT and MOSFET converter topologies. These models do not include the effect of the reverse conduction in the MOSFET inverter, also referred to as third quadrant characteristic [23]–[25]. MOSFET devices typically have a body diode that allows for reverse conduction. Additionally, when a negative drain-source voltage is present, the MOSFET channel's conduction can also be controlled by applying a gate-source voltage above the threshold voltage level [26]. In a three-phase inverter this results in parallel conduction of the diode and MOSFET when output voltage and current differ in sign.

The conventional way of controlling a two-level three-phase inverter is to send a PWM signal to the top switch of the inverter leg and the inverted PWM signal to the bottom one with a blanking time in between to prevent a short circuit of the leg [27]. This means that, typically, all MOSFET converters use the reverse conduction capability. An analytical conduction loss model for three-phase SiC MOSFET inverters, which includes the reverse conduction, was first presented in [28]. However, this model is limited to an output PWM signal using a pure sinusoidal reference and the effect of the blanking time is not included. In [29] models are presented for different modulation strategies, however, they do not accurately consider the effect of the current split between the diode and the MOSFET. In [30] the authors have presented analytical expressions to quickly evaluate the conduction losses, taking into account the effect of the reverse conduction and the blanking time. Both sinusoidal PWM operation with and without third harmonic injection, which can also be used for space vector modulation with small error, are derived in a closed form. Further, these analytical expressions have been validated with numerical simulations and it was shown that the loss reduction due to the reverse conduction is significant over a driving cycle [30]. However, all presented models [29]–[31] are lacking experimental validation, which is quite challenging. Because of the high efficiency, and hence low losses, the simple subtraction of output power from input power involves a small relative difference between these quantities, and is therefore prone to large errors and low accuracy. Calorimetry is a recognized means for the direct measurement of losses in power electronics inverters, which can be used to overcome these difficulties [32]–[35].

The contribution of this article is to experimentally verify theoretically derived expressions regarding the impact of the reverse conduction on the conduction losses of a MOSFET three-phase inverter. Therefore, this paper derives and presents

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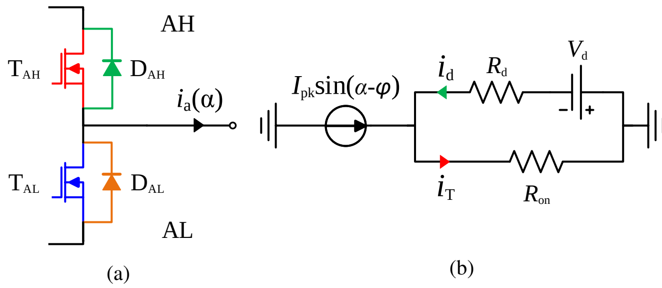

Fig. 1: (a) Single inverter leg (half-bridge) of a three-phase inverter. (b) Equivalent circuit of parallel conduction of diode and MOSFET channel in reverse direction [26]. During the reverse conduction $i_{\mathrm{T}} < 0$, and, thus, the MOSFET current flows in opposite direction of the red current arrow.

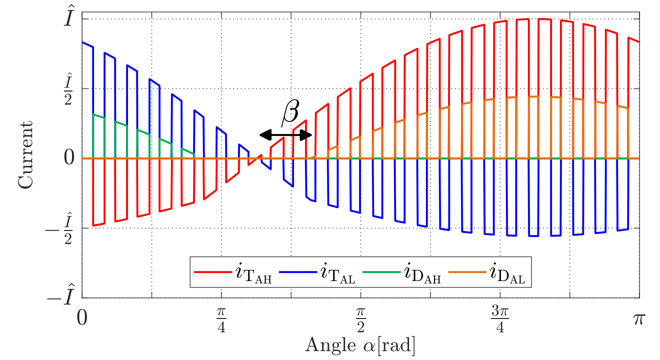

Fig. 2: Parallel conduction of diode and MOSFET channel, starting at angle β relative to the zero current crossing.

simplified analytical expressions, based on [30], to quickly evaluate the conduction losses in a three-phase MOSFET converter, including the effect of the reverse conduction and the blanking time. A SiC MOSFET three-phase inverter is tested in different operating conditions using a double jacketed calorimeter with a water cooled circuit, resulting in high accuracy of the loss measurements. Thus, the presented loss models are experimentally validated.

II. Conduction Losses considering Reverse Conduction of MOSFET Channel

The steady state conduction losses of a three-phase voltage source inverter, utilizing MOSFETs, are evaluated in this paper. It is assumed that all three-phase output currents are sinusoidal and balanced. Under this assumption it is sufficient to calculate the losses for a single inverter leg as shown in Fig. 1(a). Consequently, the result can be extended to the other two legs. The average MOSFET conduction losses can be calculated, approximating the drain source characteristic to an on-state resistance R_{on}, as

$$P_{\mathrm{c,T}} = \frac{1}{2\pi}\int_0^{2\pi} D(\alpha) R_{\mathrm{on}} i_{\mathrm{T}}^2(\alpha) d\alpha \quad , \tag{1}$$

where $\alpha = \frac{2\pi}{T}t$ and D is the duty cycle. Similarly, the diode conduction losses can be obtained, approximating the forward characteristic to mimic an on-state resistance R_{d} and a constant voltage drop V_{d}, as

$$P_{\mathrm{c,d}} = \frac{1}{2\pi}\int_0^{2\pi} D(\alpha)(R_{\mathrm{d}} i_{\mathrm{d}}^2(\alpha) + V_{\mathrm{d}} i_{\mathrm{d}}(\alpha)) d\alpha \quad . \tag{2}$$

Assuming a naturally sampled PWM sine-triangle modulation, the duty cycle as a function of α can be defined as

$$D(\alpha) = \frac{1}{2}(1 + M\sin(\alpha)) \quad , \tag{3}$$

where M is the modulation index [17]. When current and voltage in one leg are discordant, either the upper or the lower diode is forward biased. If the corresponding MOSFET gate-source voltage is above the threshold voltage level, the MOSFET channel conducts in parallel with the diode. Due to the constant voltage drop, the diode will only be forward biased, if the device current times the on-state resistance R_{on} is above the diode's threshold voltage V_{d}. Thus, it is convenient to define the parallel conduction angle β as

$$\sin(\beta) = \frac{V_{\mathrm{d}}}{R_{\mathrm{on}}\hat{I}} \quad , \tag{4}$$

shown in Fig. 2. For example, when the load current is positive and MOSFET T_{AH} in Fig. 1 is provided with a positive gate-source voltage, the phase to neutral voltage will be positive and T_{AH} will conduct the current

$$i_{\mathrm{T},1}(\alpha) = \hat{I}\sin(\alpha - \varphi) \quad \text{for} \quad -\beta \le \alpha - \varphi \le \beta + \pi \quad , \tag{5}$$

where φ is the angle of displacement power factor and $\hat{I}$ is the peak value of the phase current. On the other hand, when MOSFET T_{AH} is off, diode D_{AL} will conduct in parallel with MOSFET T_{AL}. Therefore, the diode and MOSFET currents during the parallel conduction of T_{AH} and D_{AH}, as schematically shown in Fig. 1(b), are calculated as

$$i_{\mathrm{T},2}(\alpha) = \frac{R_{\mathrm{d}}\hat{I}\sin(\alpha - \varphi) - V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} \quad \text{for} \quad \pi + \beta \le \alpha - \varphi \le 2\pi - \beta \tag{6}$$

and

$$i_{\mathrm{d}}(\alpha) = -\frac{R_{\mathrm{on}}\hat{I}\sin(\alpha - \varphi) + V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}} \quad \text{for} \quad \pi + \beta \le \alpha - \varphi \le 2\pi - \beta \, . \tag{7}$$

The integral in (1) can be calculated for the different intervals by defining $\vartheta = \alpha - \varphi$ as

$$P_{\mathrm{c,T}} = \frac{R_{\mathrm{on}}}{4\pi}\left(\int_{-\beta}^{\pi+\beta}(1 + M\sin(\vartheta + \varphi)) i_{\mathrm{T},1}^2(\alpha) d\vartheta + \int_{\pi+\beta}^{2\pi-\beta}(1 + M\sin(\vartheta + \varphi)) i_{\mathrm{T},2}^2(\alpha) d\vartheta\right) \quad . \tag{8}$$

Inserting (5) and (6) in (8), the conduction losses can be expressed as

$$P_{\mathrm{c,T}} = \frac{R_{\mathrm{on}}}{4\pi}\left(\int_{-\beta}^{\pi+\beta}(1 + M\sin(\vartheta + \varphi))\hat{I}^2\sin^2(\vartheta) d\vartheta + \int_{\pi+\beta}^{2\pi-\beta}(1 + M\sin(\vartheta + \varphi))\left(\frac{R_{\mathrm{d}}\hat{I}\sin(\vartheta) - V_{\mathrm{d}}}{R_{\mathrm{d}} + R_{\mathrm{on}}}\right)^2 d\vartheta\right) \quad . \tag{9}$$

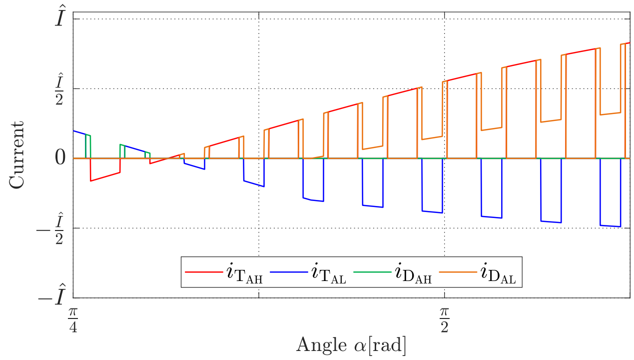

Fig. 3: Effect of the blanking time on the diode and MOSFET current.

Similarly, the integral in (2) can be expressed as

$$P_{\mathrm{c,d}} = \frac{1}{4\pi}\int_{\pi+\beta}^{2\pi-\beta}(1+M\sin(\vartheta+\varphi))(R_{\mathrm{d}}i_{\mathrm{d}}^2(\alpha)+V_{\mathrm{d}}i_{\mathrm{d}}(\alpha))d\vartheta. \tag{10}$$

Inserting (7) in (10) yields

$$\begin{aligned} P_{\mathrm{c,d}} = &\frac{1}{4\pi}\int_{\pi+\beta}^{2\pi-\beta}(1+M\sin(\vartheta+\varphi))\cdot \\ &\left[R_{\mathrm{d}}\left(\frac{R_{\mathrm{on}}\hat{I}\sin(\alpha-\varphi)+V_{\mathrm{d}}}{R_{\mathrm{d}}+R_{\mathrm{on}}}\right)^2 - \right. \\ &\left. V_{\mathrm{d}}\left(\frac{R_{\mathrm{on}}\hat{I}\sin(\alpha-\varphi)+V_{\mathrm{d}}}{R_{\mathrm{d}}+R_{\mathrm{on}}}\right)\right]d\vartheta \quad . \end{aligned} \tag{11}$$

A third harmonic can be added to the reference voltage in order to achieve a higher value of the fundamental output voltage. Typically, the optimal value is $1/6$ of M, allowing the output voltage to be increased by up to $15\,\%$ without reaching the over-modulation region. The duty cycle expression in the integral to calculate the losses when a third harmonic is added to the reference is

$$D(\alpha) = \frac{1}{2}(1+M\sin(\alpha)+\frac{1}{6}M\sin(3\alpha)) \quad . \tag{12}$$

The complete expressions with the integrals in (8), (11) and considering the third harmonic injection (12) are reported in the Appendix.

A. Effect of the Blanking Time

Because of the finite turn-on and turn-off times, associated with any type of semiconductor switch, a delay time, often referred to as blanking time, t_{bl}, between the conduction of the upper and lower switch of the same inverter leg must be implemented in order to avoid a shoot-through. During the blanking time only the diode is conducting the current. The effect of the blanking time is shown in Fig. 3. Its effect on the MOSFET conduction loss calculation can be accounted for by defining an equivalent duty cycle

$$D_{\mathrm{eq}}(\alpha) = \mathrm{D}(\alpha) - t_{\mathrm{bl}}f_{\mathrm{sw}} = \frac{1}{2}(1-2t_{\mathrm{bl}}f_{\mathrm{sw}}+M\sin(\alpha)) \ , \tag{13}$$

where f_{sw} is the switching frequency). Negative duty cycle values are not to be considered, so the condition

$$1-2t_{\mathrm{bl}}f_{\mathrm{sw}}+M\sin(\alpha) > 0 \tag{14}$$

must be verified in the case of a sinusoidal reference voltage. In the case with 1/6 third harmonic injection the condition to fulfill is

$$1-2t_{\mathrm{bl}}f_{\mathrm{sw}}+M\sin(\alpha)+1/6M\sin(3\alpha) > 0 \quad . \tag{15}$$

For values of M close to the boundary of the over-modulation region, the method of using an equivalent duty cycle should be applied carefully. Negative duty cycle values are to be avoided. Since the diode is conducting the whole current during the blanking time, the average conduction losses in (11) must be extended by the addition of

$$\frac{1}{2\pi}\int_{\pi}^{2\pi}2t_{\mathrm{bl}}f_{\mathrm{sw}}\left(R_{\mathrm{d}}\hat{I}^2\sin^2(\vartheta)-\hat{I}\sin(\vartheta)V_{\mathrm{d}}\right)d\vartheta \quad , \tag{16}$$

which results in

$$t_{\mathrm{bl}}f_{\mathrm{sw}}\hat{I}\left(\frac{1}{2}\hat{I}R_{\mathrm{d}}+\frac{2}{\pi}V_{\mathrm{d}}\right) \quad . \tag{17}$$

While (9) and (11) have been derived without introducing any approximation, the formulas including the blanking time have some degree of approximation. Using an equivalent duty cycle as in (13) means a reduction of the current conduction interval with two times the blanking time. However, the blanking time intervals are not specifically placed at the beginning or the end of the reverse conduction, but are considered averaged over the whole electrical period, introducing a small error. Nevertheless, the entity of this error is still negligible and the equivalent duty cycle is very accurate in estimating the losses including the effect of blanking time as shown in [30].

Again the complete analytical expressions of the conduction losses, including the effect of the blanking time, are reported in the Appendix.

B. Switching Losses

In order to evaluate the overall efficiency of the three-phase inverter, the switching losses need to be considered as well. The device's data sheet usually provides the switching losses as a function of the device current for certain voltage levels. Thus, the switching losses for one semiconductor switch can be calculated, taking every switching event into account, by a look-up table approach, as

$$P_{\mathrm{sw}} = \frac{\sum_{j=1}^{n=T_1f_{\mathrm{sw}}}(E_{\mathrm{on},j}(i_{\mathrm{T}}(t))+E_{\mathrm{off},j}(i_{\mathrm{T}}(t))+E_{\mathrm{rr},j})}{T_1} \quad , \tag{18}$$

where T_1 is the fundamental period of the output voltage and E_{rr} is the reverse recovery loss. The switching losses, $E_{\mathrm{on}}(i_{\mathrm{T}})$ and $E_{\mathrm{off}}(i_{\mathrm{T}})$, can be scaled according to the DC link voltage as

$$E_{\mathrm{on/off}}(i_{\mathrm{T}}) = \left(\frac{V_{\mathrm{DS}}}{V_{\mathrm{DC,ref}}}\right)^{K_{\mathrm{v,on/off}}} \quad . \tag{19}$$

The value of $K_{\mathrm{v,on/off}}$ is typically about 1.4 [36] and can be obtained from the supplier's data sheet through interpolation. According to [22], the switching loss calculation can be simplified by expressing the AC current through an equivalent DC current as

$$I_{\mathrm{DC}} = \frac{\hat{I}}{\pi} = i_{\mathrm{T}} \quad . \tag{20}$$

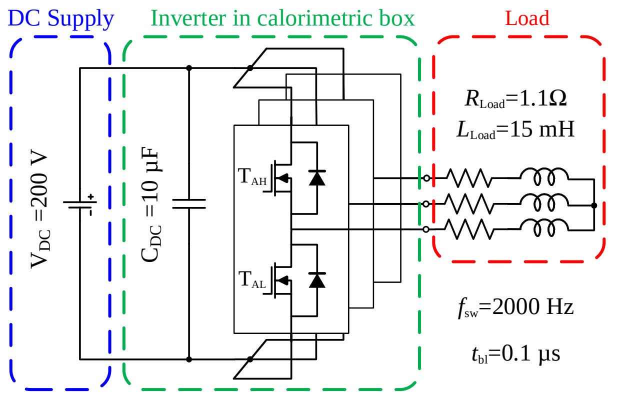

Fig. 4: Schematic operation of the inverter setup, using an RL-load. The low switching frequency and the low DC-link voltages reduce the switching losses.

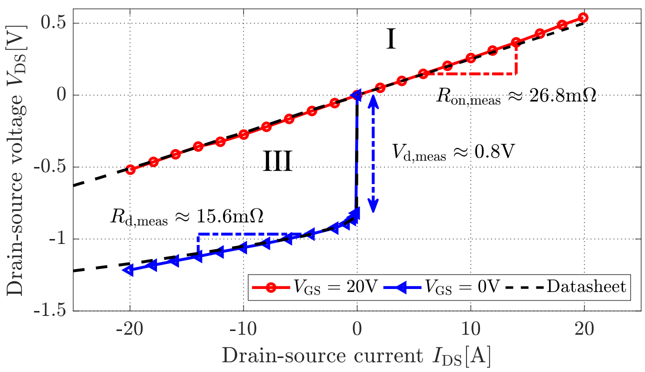

Fig. 5: Measured MOSFET and diode characteristic of the chosen SiC MOSFET inverter. Reverse conduction is also shown.

Thus, the switching losses can be estimated as

$$P_{sw} = f_{sw}(E_{on}(I_{DC}) + E_{off}(I_{DC}) + E_{rr}) \quad . \tag{21}$$

Having the MOSFET turning on and off during reverse conduction would in theory increase the switching losses. However, due to the fact that the diode is conducting in parallel or is conducting during the blanking time, the voltage across the MOSFET is forced to $V_d + R_d \hat{I}$ during the beginning of the switching transient, achieving quasi zero-voltage-switching (ZVS) [12], [37]. Therefore, the switching losses of the MOSFET during reverse conduction are negligible.

III. Experimental validation

To experimentally validate the conduction-loss models derived in Section II, a SiC MOSFET inverter was operated with and without reverse conduction using a calorimetric box, as schematically shown in Fig. 4. In this section the experimental setup is described and the loss measurements are presented and compared with the analytical models.

TABLE I: Equipment list

Device	Manufacturer	Model
SiC module 1.2 kV/50 A	Wolfspeed	CCS050M12CM2 [38]
SiC gate driver board	Wolfspeed	CGD15FB45P1 [39]
2 DC link capacitors 5 μF	Vishay	MKP386M550125YT4
4W-PT100	RS PRO	25mm x 4mm Probe
Acquisition unit	Fluke	Hydra 2620A
Pump	Shenchen	LabN6

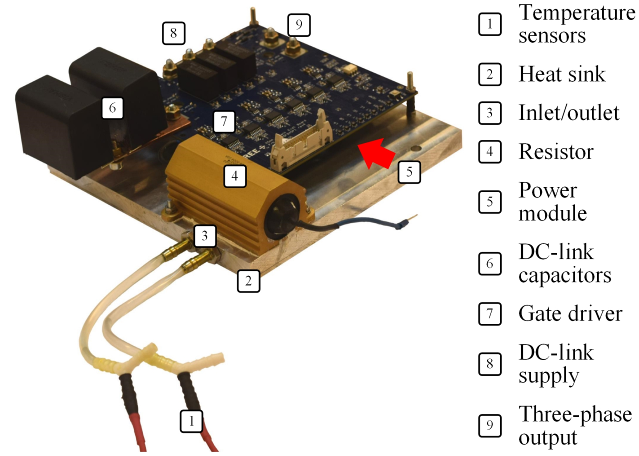

Fig. 6: Three-phase inverter prototype and calibration resistor mounted on the water cooled heatsink.

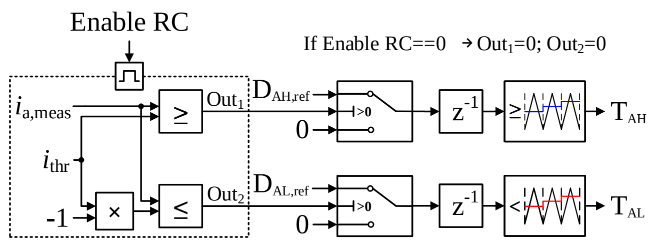

Fig. 7: Schematic description to disable the reverse conduction by keeping the gate switched off, if the phase current exceeds the threshold value i_{thr}.

A. Case Study and Setup Description

A SiC MOSFET inverter was built using one of Cree's six-pack three-phase modules, including the custom gate driver board, listed in Table I. The MOSFETs' and diodes' voltage drop, including the effect of the reverse conduction, were experimentally characterized at ambient temperature for different drain-source current levels, as can be seen in Fig. 5. The module, together with a 220 Ω calibration resistor with a maximum power dissipation of 100 W, was mounted on a water cooled heat sink as shown in Fig. 6. The PWM signals were generated using a DSpace DS1006 processor board and DS5202 FPGA Base Board. A program was implemented to be able to enable the reverse conduction, With Reverse Conduction (W-RC), and disable the reverse conduction, With-Out Reverse Conduction (WO-RC), by either providing a high or a low gate signal to the corresponding SiC MOSFET when voltage and current are of opposite sign. A schematic description of the program is presented in Fig. 7. The complete laboratory setup is shown in Fig. 8. The double jacketed calorimetric box, as described

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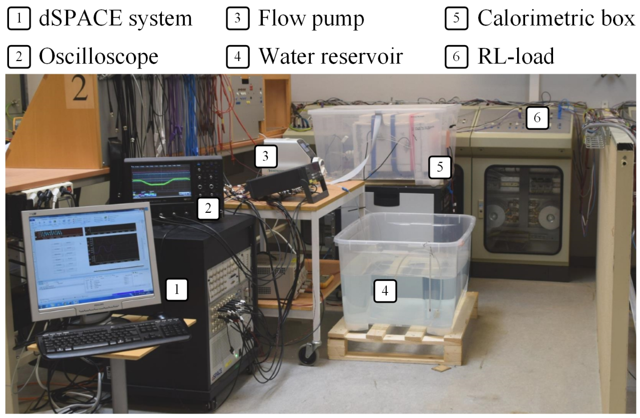

Fig. 8: Actual test setup environment with calorimetric box, water reservoir, data acquisition and control unit.

in [40], has an inner and an outer air chamber. Having two chambers reduces the leakage heat through the box walls. The inverter and heatsink were fitted inside the calorimetric box with high resolution temperature sensors (4-wire PT100) at the water inlet and outlet. The pump used in the setup is a medical grade pump, see Table I, able to operate with a high accuracy at very low flow rates. A low flow rate of $200\,\mathrm{mL\,min^{-1}}$ was chosen in order to increase the outlet to inlet water temperature difference and have a good reading accuracy of the temperature sensors. This is necessary when measuring losses in the range of 10-30 W. The inverter's losses were measured using the thermal Steady Flow Energy Equation (SFEE)

$$P_{\mathrm{loss}}(1-\sigma_{\mathrm{th}}) = c_{\mathrm{p}}\dot{V}\rho\Delta T \quad , \tag{22}$$

where σ_{th} is the calorimetric box's leakage factor, c_{p} is the heat capacity at constant pressure, $\dot{V}$ is the volumetric flow rate, ρ is the volumetric mass density and ΔT is the temperature difference between the inlet and the outlet. To determine the heat leakage conducted through the cables and the walls, a specific loss was injected, using the calibration resistor, and compared with the measured losses, derived from the cooling circuit. Fig. 9 shows the calibration measurements using an injected power dissipation in the resistor of about 25 W. After an initial transient, the absolute temperatures inside the box were rising with a constant slope due to the fact that the inlet water temperature comes from a water reservoir, which was slowly warming up with time. Regardless, the coolant outlet to inlet temperature difference becomes constant after the first transient, which can be be considered as a quasi steady state for the loss evaluation. The calibration results for different levels of injected power dissipation are depicted in Fig. 10. The leakage factor is fairly constant within the chosen dissipated power range, thus the average value was applied to the measurements on the inverter.

B. Loss Measurements

The setup, as presented in Figs. 4 and 8, was used to evaluate the conduction losses for both cases, W-RC and WO-RC. The switching frequency of 2 kHz and the DC-link

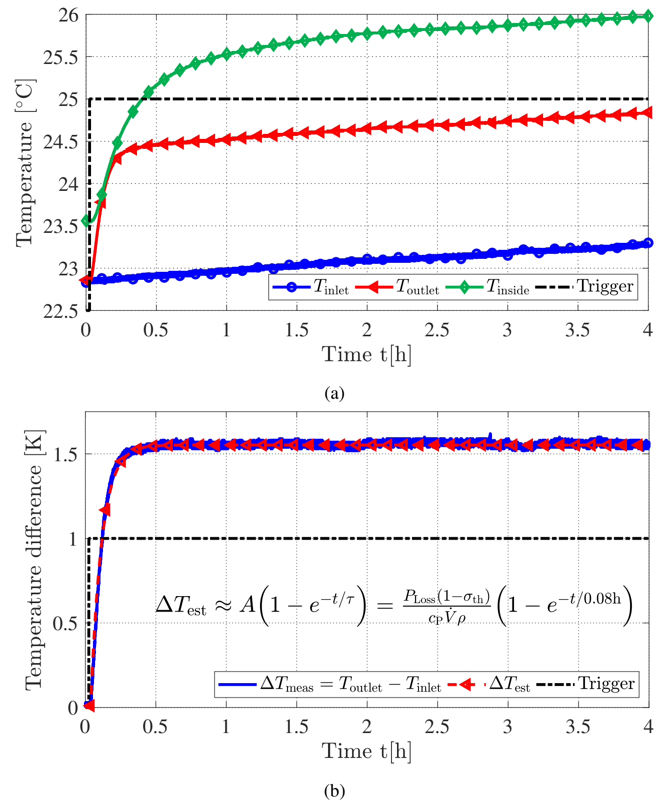

Fig. 9: Transient temperature profiles using a flow rate of $200\,\mathrm{mL\,min^{-1}}$ for about 25 W of injected power. (a) Temperature profiles of the water inlet, water outlet and the air inside the box. (b) Water temperature difference between the outlet and the inlet, both measured and estimated.

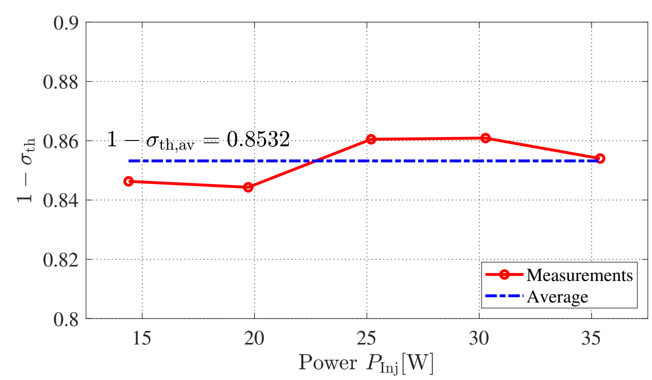

Fig. 10: Calorimetric box's leakage factor measured for different power levels of injected DC power using the calibration resistor.

voltage of 200 V were selected in order to focus on the conduction losses by keeping the switching losses low, as the conduction losses are not dependent on the DC-link voltage as shown in (9) and (11). Furthermore, using a switching frequency of 2 kHz and considering the proper modulation of the injected third harmonic component, output fundamental frequencies up to 66.67 Hz can be synthesized [27], while generating some audible noise. In an actual application, it is beneficial to use a switching frequency of at least 20 kHz,

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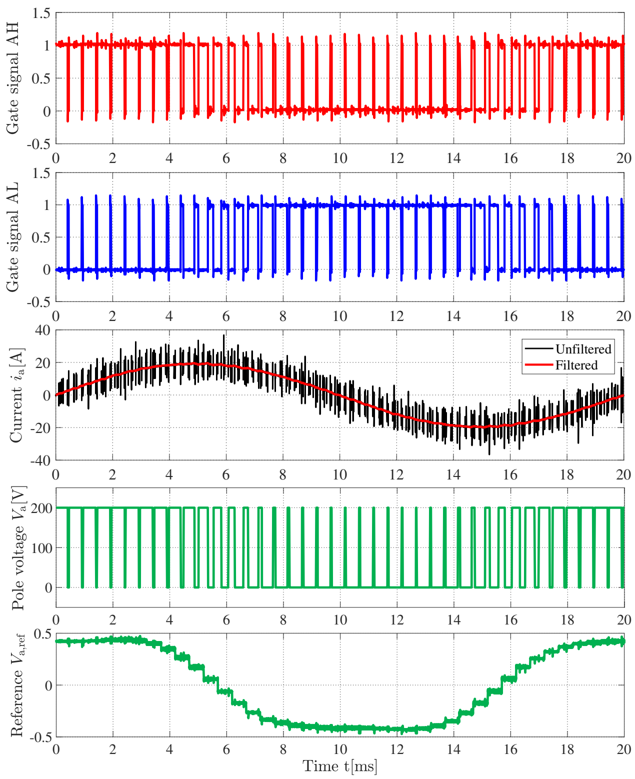

Fig. 11: Gate signals, output current, pole voltage and reference voltage with enabled reverse conduction (W-RC) for one of the three phases (pole voltage signal is simulated, all other signals are measured).

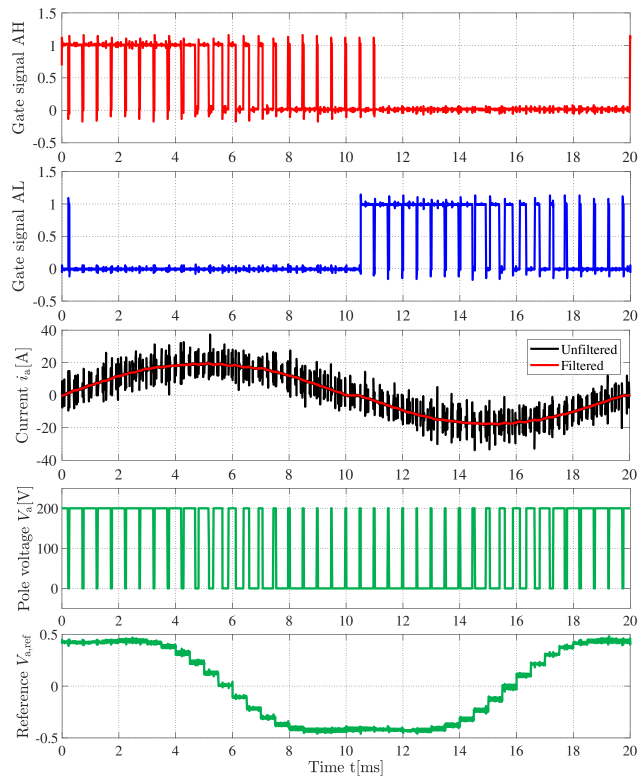

Fig. 12: Gate signals, output current, pole voltage and reference voltage with disabled reverse (WO-RC) conduction for one of the three phases (pole voltage signal is simulated, all other signals are measured).

to avoid the audible noise. A fixed RL-load was applied on the output and the power factor was varied by changing the fundamental frequency. To adjust the three-phase output current's amplitude, a current controller using loop shaping, as described in [27], [41], was implemented. The gate driver board inside the calorimetric box was generating additional losses, which were accounted by the measured supply power.

At first, the inverter's output current amplitude was controlled to about $20\,\mathrm{A}$ at a frequency of $50\,\mathrm{Hz}$. The high side and the low side gate signals together with the output current and the voltage reference of the measurements for one of the three phases are presented in Fig. 11 for the W-RC case and in Fig. 12 for the WO-RC case. The corresponding temperature difference between the outlet and the inlet of the calorimetric box can be seen in Fig. 13. In time intervals of about $1\,\mathrm{h}$, the inverter was alternately operated with and without reverse conduction. It can be noted that the effect of the reverse conduction has a significant impact on the inverter losses. The loss comparison between both cases, W-RC and WO-RC, at thermal steady state are presented in Fig. 14. The measured auxiliary losses of approximately ($2.8\,\mathrm{W}$) are from the gate driver board. Theoretically, these are dependent on the switching frequency ($\Delta P_{\mathrm{Aux}} \approx 33\,\mathrm{\mu W\,Hz^{-1}}$ [39]). The difference of the effective gate driver switching frequency between the cases W-RC and WO-RC was about $1\,\mathrm{kHz}$, which should result in a theoretical, auxiliary loss difference of about $33\,\mathrm{mW}$. In practice, however, there was

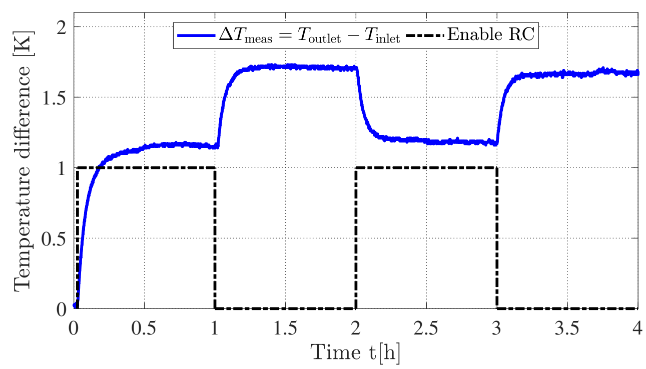

Fig. 13: Measured water temperature difference between the outlet and the inlet with alternately enabled and disabled reverse conduction for a current amplitude of $20\,\mathrm{A}$ at $50\,\mathrm{Hz}$.

no difference in the measured auxiliary power. The switching losses were quantified to be approximately $0.2\,\mathrm{W}$, for both W-RC and WO-RC. The switching and the auxiliary losses are added to the conduction losses calculated with the analytical model and compared with the total losses from the calorimetric measurement showing a very good agreement. Considering the case with enabled reverse conduction, the presented analytical expressions show an agreement of approximately $98.5\,\%$ in comparison to the measured losses. Even when using a $1200\,\mathrm{V}$ device with a high on-state resistance, R_{on}, and an anti-parallel Schottky diode with a low forward drop, V_{d}, there is

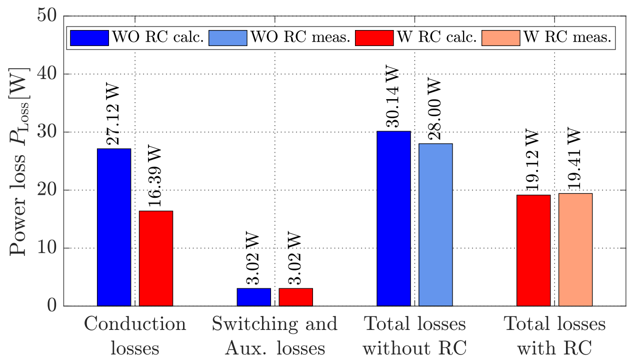

Fig. 14: Comparison of estimated losses, using the analytical models, and measured losses for a current amplitude of 20 A at 50 Hz.

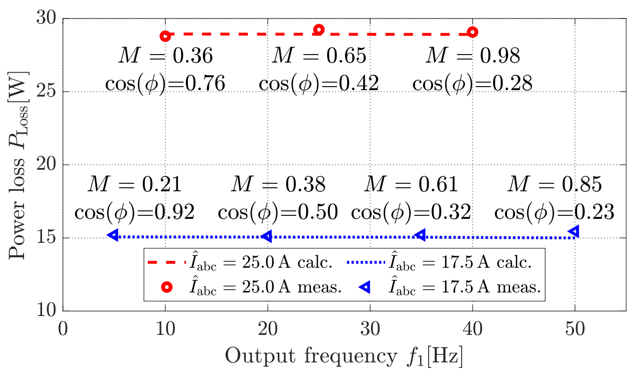

Fig. 15: Comparison of estimated losses, using the analytical model, and measured losses for different operating points with enabled reverse conduction.

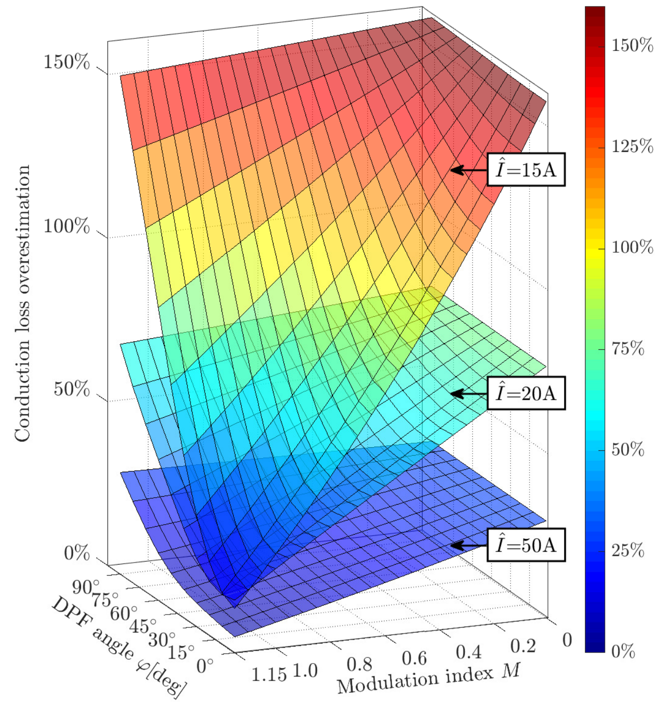

Fig. 16: Overestimation of the conduction losses when using the method described in Semikron's application manual [21] in comparison to the presented method for the SiC MOSFET three-phase inverter of Cree [38].

a significant difference between the cases W-RC and WO-RC at partial load operation.

The same procedure was repeated for several operating points (all W-RC), varying the frequency of the fundamental (and consequently the power factor) and the amplitude of the output current. The results are presented in Fig. 15. Similarly as before, the losses measured with the calorimetric method match very well with the ones estimated using the analytical models presented in this paper.

IV. Comparison of the Proposed Method

As experimentally shown, the conduction-loss models described in [17]–[20] and the semiconductor manufacturers' applications manuals [21], [22] overestimate the conduction losses of a three-phase inverter when using Si and SiC MOSFETs instead of IGBTs. Figure 16 depicts the overestimation of the conduction losses proposed in [21] in comparison to the model presented in equations (23) to (30) relative to the modulation index M and the displacement power factor (DPF) angle φ for different output current amplitudes. For the calculations, the parameters of the SiC MOSFET power module [38], determined from the measured characteristic in section II, are used. As can be seen, the relative differences become smaller for larger current amplitudes. For a fixed current amplitude, the overestimation becomes the highest at low modulation index and pure inductive DPF and the lowest at a high modulation index and unity DPF. For the depicted current amplitudes of 15 A and 50 A, the relative overestimation varies from 13.5 % to 159.3 % and 4.9 % to 29.8 %, respectively.

A. Practical Selection of MOSFETs for Three-Phase inverters used for Drive Applications

When choosing a MOSFET for a drive application, its rated blocking voltage should be sufficiently higher than the voltage at which it will be actually used in order to withstand the overvoltages caused by each switching event [5], [42]. For example in electric vehicles (EVs), typical DC-link voltages are either 400 V or even 800 V, which leads to a blocking voltage selection of 600 V to 650 V or 1200 V, respectively [43], [44]. This corresponds to a design factor of about 1.5 ($V_{\mathrm{Block}}/V_{\mathrm{DC}}$). Including a safety margin, the MOSFET's maximum drain current should comply with the maximum operating current [5]. The switching frequency should be selected in accordance with the application and design optimization. For example, to ensure a proper current control it is reasonable to select a switching frequency, which is at least ten times higher than the maximum fundamental frequency [27]. For an EV, the electric motor is typically operated at fundamental frequencies up to about 1 kHz and, thus, a switching frequency of 10 kHz is often selected [41]. If the audible noise needs to be reduced as well, the switching frequency could be increased above 20 kHz [45], [46]. For example, when dealing with grid connected inverters, it might be more beneficial for the overall system design to choose an even higher switching frequency ($f_{\mathrm{sw}} >> 20\,\mathrm{kHz}$) to reduce passive components, as for example the grid filter [5], [47]. This in turn would result in a higher portion of the switching losses in relation to the total losses. Subsequently, when considering different MOSFETs, it must be ensured that the sum of the switching and conduction losses does not exceed the maximum permissible power dissipation of the MOSFET and the temperature rise due to the heating should be kept within the specified temperature boundaries, including the application of necessary cooling [42], [48]. The switching losses can be estimated by (18) to (21) using a lookup-table approach with data-sheet values or measurement values obtained from double-pulse tests [49]. The conduction losses can be estimated using (23) to (30). Simple thermal models can be used to estimate the junction temperature of the MOSFET [42], [48].

Since the rated operating point is usually used for the MOSFET selection and circuit design, the difference between the estimated conduction losses, exemplified in comparison to [21] corresponds only to a few percent, as can be seen in Fig. 16. However, the effect of the presented conduction loss estimation becomes more beneficial when considering also the actual operating range throughout the inverter's lifetime, as variable speed drives, e.g. pumps or air compressors, are often operated at partial load [50]. In such cases, the properties of the body (or the anti-parallel) diode are of less importance as the MOSFET channel is mainly conducting the current in reverse conduction mode. Hence, it might be beneficial to motivate a higher investment cost for a SiC MOSFET inverter with a low on-state resistance R_{on} in comparison to a cheap IGBT inverter [5], [7], considering that the increased energy cost savings throughout the lifetime and that the total energy and acquisition costs typically correspond to about $80\,\%$ and $9\,\%$ of the total costs, respectively [50].

V. Conclusion

This paper has presented analytical models to quickly evaluate the conduction losses of a three-phase MOSFET inverter including the effect of the reverse conduction. These models can be used as a quick and accurate tool during the inverter design process to evaluate the inverter efficiency and to perform thermal evaluations.

The proposed equations have been experimentally validated. A SiC MOSFET inverter for traction applications has been tested for different operating conditions and the losses were measured using a calorimetric setup. The measured losses have been compared with the proposed analytical models showing good agreement. A calculated comparison of the presented method with [21] shows that the available methods for IGBT inverters overestimate the conduction losses when used for MOSFET inverters, especially at partial load operation.

This allows the conclusion that the negligence of the reverse conduction can lead to significant errors in the conduction loss estimation, which might result in an overdimensioned cooling system.

Appendix

$$A = \begin{cases} 1 & \text{for } t_{\mathrm{bl}} = 0 \\ 1 - 2t_{\mathrm{bl}}f_{\mathrm{sw}} & \text{for } t_{\mathrm{bl}} > 0 \end{cases} \tag{23}$$

$$B = \frac{\pi}{2} + \beta - \frac{\sin(2\beta)}{2} \tag{24}$$

$$C = \cos(\beta) - \frac{\cos^3(\beta)}{3} \tag{25}$$

$$D = 2M\cos(\varphi) \tag{26}$$

Average MOSFET conduction losses (one switch), using sinusoidal voltage reference:

$$\begin{aligned} P_{\mathrm{c,T}} = &\frac{R_{\mathrm{on}}\hat{I}^2}{4\pi}(AB+CD) + \\ &\frac{R_{\mathrm{on}}}{4\pi(R_{\mathrm{on}}+R_{\mathrm{d}})^2}\Big(\hat{I}^2R_{\mathrm{d}}^2(A(\pi-B)-CD) + \\ &V_{\mathrm{d}}^2((\pi-2\beta)A - D\cos(\beta)) + \hat{I}R_{\mathrm{d}}V_{\mathrm{d}}(4A\cos(\beta)-(\pi-B)D)\Big) \end{aligned} \tag{27}$$

Average Diode conduction losses (one diode), using sinusoidal voltage reference:

$$\begin{aligned} P_{\mathrm{c,d}} = &\frac{R_{\mathrm{d}}}{4\pi(R_{\mathrm{on}}+R_{\mathrm{d}})^2}\Big(R_{\mathrm{on}}^2\hat{I}^2(\pi-B-CD) + \\ &V_{\mathrm{d}}^2(\pi-2\beta-D\cos(\beta)) - R_{\mathrm{on}}\hat{I}V_{\mathrm{d}}(4\cos(\beta)-(\pi-B)D)\Big) - \\ &\frac{V_{\mathrm{d}}}{4\pi(R_{\mathrm{on}}+R_{\mathrm{d}})}\Big(\frac{1}{2}R_{\mathrm{on}}\hat{I}(\pi-B)D + 2R_{\mathrm{on}}\hat{I}\cos(\beta) - \\ &V_{\mathrm{d}}(\pi-2\beta) + V_{\mathrm{d}}D\cos(\beta)\Big) + t_{\mathrm{bl}}f_{\mathrm{sw}}\hat{I}\Big(\frac{1}{2}\hat{I}R_{\mathrm{d}} + \frac{2}{\pi}V_{\mathrm{d}}\Big) \end{aligned} \tag{28}$$

Additional average MOSFET conduction losses (one switch), using 1/6 third harmonic injection (to be added to (27)):

$$\begin{aligned} &\frac{MR_{\mathrm{on}}\hat{I}^2}{60\pi}\cos(3\varphi)(4\sin^4(\beta)\cos(\beta)+C)\Big(\frac{R_{\mathrm{d}}^2}{(R_{\mathrm{on}}+R_{\mathrm{d}})^2} - 1\Big) - \\ &\frac{MV_{\mathrm{d}}^2}{36\pi(R_{\mathrm{on}}+R_{\mathrm{d}})}\cos(3\varphi)\cos(3\beta)\Big(\frac{R_{\mathrm{on}}}{(R_{\mathrm{on}}+R_{\mathrm{d}})}\Big) - \\ &\frac{MR_{\mathrm{on}}\hat{I}R_{\mathrm{d}}V_{\mathrm{d}}}{24\pi(R_{\mathrm{on}}+R_{\mathrm{d}})^2}\cos(3\varphi)\Big(\frac{\sin(4\beta)}{2} - \sin(2\beta)\Big) \end{aligned} \tag{29}$$

Additional average Diode conduction losses (one diode), using 1/6 third harmonic injection (to be added to (28)):

$$\begin{aligned} &\frac{M\hat{I}^2R_{\mathrm{d}}}{60\pi}\cos(3\varphi)(4\sin^4(\beta)\cos(\beta)+C)\Big(\frac{R_{\mathrm{on}}^2}{(R_{\mathrm{on}}+R_{\mathrm{d}})^2}\Big) - \\ &\frac{MR_{\mathrm{on}}\hat{I}V_{\mathrm{d}}}{48\pi(R_{\mathrm{on}}+R_{\mathrm{d}})}\Big(\cos(\varphi)\Big[\sin(2\varphi)\cos(2\beta) - \frac{\sin(4\varphi)\cos(4\beta)}{2}\Big] - \\ &\sin(\varphi)\Big[\sin(2\varphi)\cos(2\beta) - \frac{\cos(4\varphi)\cos(4\beta)}{2}\Big]\Big) + \\ &\frac{MV_{\mathrm{d}}^2}{36\pi(R_{\mathrm{on}}+R_{\mathrm{d}})}\cos(3\varphi)\cos(3\beta)\Big(1 - \frac{R_{\mathrm{d}}}{(R_{\mathrm{on}}+R_{\mathrm{d}})}\Big) + \\ &\frac{MR_{\mathrm{on}}\hat{I}R_{\mathrm{d}}V_{\mathrm{d}}}{24\pi(R_{\mathrm{on}}+R_{\mathrm{d}})^2}\cos(3\varphi)\Big(\frac{\sin(4\beta)}{2} - \sin(2\beta)\Big) \end{aligned} \tag{30}$$

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