

# Plasma-Enhanced Atomic Layer Deposition of Al<sub>2</sub>O<sub>3</sub> on Graphene Using Monolayer hBN as Interfacial Layer

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The deposition of dielectric materials on graphene is one of the bottlenecks for unlocking the potential of graphene in electronic applications. The plasma enhanced atomic layer deposition of 10 nm thin high quality aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) on graphene is demonstrated using a monolayer of hexagonal boron nitride (hBN) as protection layer. Raman spectroscopy is performed to analyze possible structural changes of the graphene lattice caused by the plasma deposition. The results show that a monolayer of hBN in combination with an optimized deposition process can effectively protect graphene from damage, while significant damage is observed without an hBN layer. Electrical characterization of double gated graphene field effect devices confirms that the graphene does not degrade during the plasma deposition of Al<sub>2</sub>O<sub>3</sub>. The leakage current densities are consistently below 1 pA μm<sup>-2</sup> for electric fields across the insulators of up to 8 MV cm<sup>-1</sup>, with irreversible breakdown happening above. Such breakdown electric fields are typical for Al<sub>2</sub>O<sub>3</sub> and can be seen as an indicator for high quality dielectric films.

## 1. Introduction

Graphene has remarkable properties that make this material interesting for science and applications.<sup>[1]</sup> Especially in electronics, graphene has attracted significant attention because of its excellent electronic and photonic properties including high carrier mobility and broadband optical response.<sup>[2–10]</sup> One of the essential steps in manufacturing graphene based electronic and photonic devices is to deposit a dielectric on top of this material, either for encapsulation or for electrical gating.<sup>[11,12]</sup> Specifically, electro-optical modulators for data communication require the deposition of thin dielectrics with high breakdown field and low leakage current on top of graphene, without reducing the quality of the graphene.<sup>[13–14]</sup> Substantial

efforts have been put into the deposition of high-k dielectrics on graphene for different device applications. Atomic layer deposition (ALD) is considered the most appropriate technique, in particular for thin layers as it provides precision control of the uniformity, composition control and film thickness.<sup>[15–17]</sup> However, ALD growth requires the chemical adsorption of the precursors on the substrate surface, so the chemical inertness of graphene makes the growth of dielectrics by ALD difficult. There are different types of ALD processes for the deposition of oxides like Al<sub>2</sub>O<sub>3</sub>, where water, ozone, or oxygen plasma is used as an oxygen source together with an Al precursor, typically trimethylaluminum (TMA). Direct growth of high-quality and thin dielectrics on graphene by a thermal, water-based ALD process is not possible without process adaptations due to the lack of available nucleation sites on graphene. For a total surface coverage and a high oxide uniformity, the presence of seed layers on the graphene or other pretreatments that facilitate the initial growth of a closed layer of dielectric on its surface is required.<sup>[16,18–23]</sup> A seed layer may be deposited prior to ALD to promote the growth of a closed film of dielectric, for example e-beam evaporation of aluminum (Al) before depositing Al<sub>2</sub>O<sub>3</sub> by water-based ALD.<sup>[18,19]</sup> Another possibility is a modification of the deposition process during the ALD deposition,<sup>[16,21–24]</sup> which has been achieved by increased water absorption at lower temperatures just before the actual water-based ALD process at higher temperatures<sup>[16,21]</sup> or by deposition of a TMA-based functionalization layer either by NO<sub>2</sub>-TMA deposition at room


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temperature,<sup>[22]</sup> by omitting the purging steps after TMA and H<sub>2</sub>O pulses for the first several cycles of ALD<sup>[23]</sup> or by increasing the residence time of the precursors in the deposition chamber.<sup>[24]</sup> However, these methods require additional steps in the fabrication and the majority of these processes also introduce defects in graphene that can be seen by Raman spectroscopy.<sup>[19,21,23]</sup>

The deposition of Al<sub>2</sub>O<sub>3</sub> on graphene before transfer, i.e., on the substrate where graphene was grown is another alternative. Strong interaction between the growth substrate and graphene can enhance the nucleation of Al<sub>2</sub>O<sub>3</sub> deposited by thermal ALD. In the case of monolayer graphene on native metallic substrates like copper the presence of polar traps at the interface (graphene/metal) can increase the adsorption of water molecules onto graphene in the thermal process using water as precursor.<sup>[25–27]</sup> In the case of graphene grown on SiC substrates, the adsorption energy for water molecules can be enhanced by the high n-type doping of the graphene induced by the underlying buffer layer.<sup>[28,29]</sup> However, if the oxide/graphene stack needs to be transferred to a different substrate, the handling and bending of the film during transfer introduces strain in the graphene and damage to the oxide and graphene films. The bending can induce cracks that may lead to significant reduction of film quality.<sup>[26]</sup> Plasma-enhanced atomic layer deposition (PEALD), on the other hand, has significant advantages over the thermal-based process: shorter process times and higher quality oxides are possible, enabling thinner gate oxides with higher breakdown fields.<sup>[30]</sup> However, the oxygen plasma process can cause significant surface damage especially to sensitive materials like graphene. The interface between the 2D crystal graphene and the 3D amorphous Al<sub>2</sub>O<sub>3</sub> is also critical for the electrical properties of graphene.<sup>[31]</sup> Graphene's intrinsic exceptional electrical properties are best preserved when there are only van der Waals interactions with the surrounding dielectrics, while Al<sub>2</sub>O<sub>3</sub> tends to form covalent bonds to the underlying layer. This leads to non-perfect interfaces, reducing the mobility in graphene, increasing 1/f noise and introducing reliability problems of graphene-based devices.<sup>[31]</sup> Single-crystal multilayer hexagonal boron nitride (hBN) has been shown to improve the electronic performance of graphene immensely, leading to higher mobilities at room temperature due to weak interlayer van der Waals forces in both graphene and hBN and the small lattice mismatch between hBN and graphite (less than 2%<sup>[32]</sup>). While scalable chemical vapor deposition (CVD) processes for hBN have not yet reached a maturity comparable to graphene, poly-crystalline hBN films are widely available, with mono-layer hBN being most well controlled in terms of domain size (mm size demonstrated) and homogeneity. Such CVD monolayer hBN has recently been used as interfacial layer on single crystalline graphene flakes to enable encapsulation with 17 nm silicon nitrate (SiN) as dielectric deposited by using plasma-enhanced CVD.<sup>[33]</sup> Recently, thin films of hBN (1.6 nm) have been used as a protective buffer layer to protect graphene from damage during PEALD of Al<sub>2</sub>O<sub>3</sub>.<sup>[34]</sup> For very thin dielectrics, where the higher quality of dielectrics deposited by PEALD becomes important, a 1.6 nm buffer layer may be too thick and despite the thickness of the hBN there was still some damage to the graphene. These works demonstrate an increased interest in being able to protect graphene from plasma damage.<sup>[34]</sup>

In this work we demonstrate that even a monolayer of hBN on top of graphene can act as an effective protective and interfacial layer for the graphene when PEALD with a very short plasma duration is used, enabling PEALD deposition of high quality and 10 nm thin Al<sub>2</sub>O<sub>3</sub>. Similar to graphene, hBN also has no dangling bonds, which can prevent proper nucleation in a thermal ALD process. However, also the hBN is expected to receive damage due to the plasma exposure, which can promote nucleation for the Al<sub>2</sub>O<sub>3</sub> growth process. Therefore, no additional seeding layers or pretreatments are needed for the PEALD process on hBN. For this study, we have intentionally chosen monolayer hBN grown by CVD, because it is available in wafer-scale (15 cm) areas and, due to the thin body of atomic monolayer thickness, it only gives a small contribution to the total dielectric thickness.

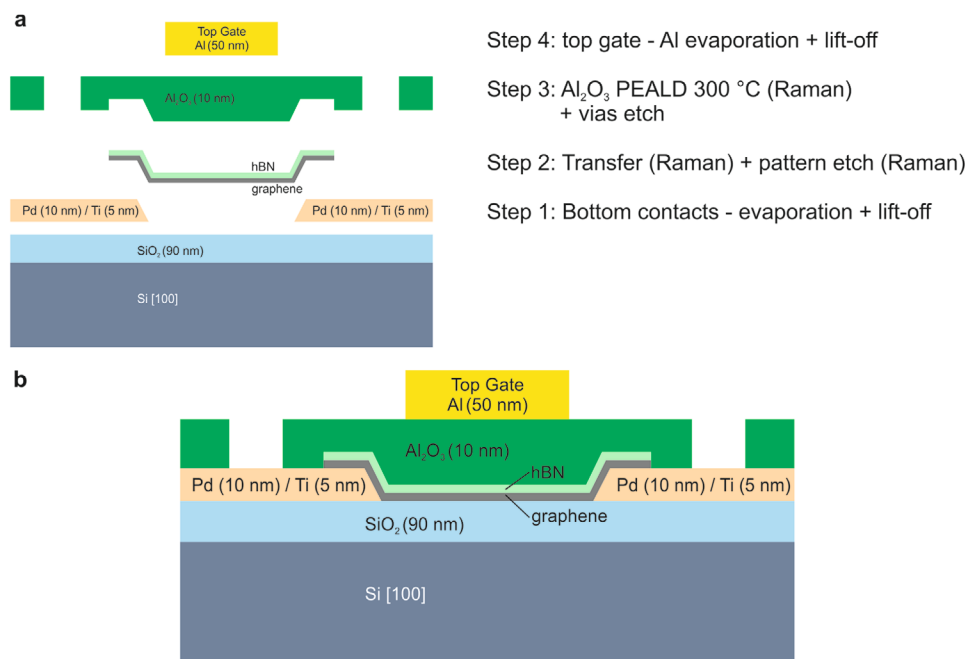
All experiments were conducted with monolayer graphene and monolayer hBN grown by CVD on metal foils. The hBN/graphene stacks were prepared by sequential etching and transfer steps and transferred to a 6 in. Si wafer covered by 90 nm thermally grown SiO<sub>2</sub> (see the Experimental Section for details). In the reference samples only graphene was transferred without hBN. After the transfer, the samples were encapsulated by PEALD with 10 nm of Al<sub>2</sub>O<sub>3</sub> in an Oxford Instruments Atomfab ALD system using TMA and oxygen plasma as precursors. It is important to point out that the plasma time was only 0.1 s per cycle. A reference sample was prepared and covered by 20 nm of Al<sub>2</sub>O<sub>3</sub> using a thermal (i.e., plasma free) ALD process with TMA and H<sub>2</sub>O. The reason for the difference of the Al<sub>2</sub>O<sub>3</sub> thickness in this reference sample is that less than 20 nm Al<sub>2</sub>O<sub>3</sub> did not provide closed layers suitable for electrical gating, consistent with what has been typically reported. Raman spectroscopy was performed before and after the deposition to monitor the structural parameters like defects and strain variations.

Double-gated graphene transistors (graphene field-effect transistors, GFET) were fabricated for measuring the electrical parameters of the graphene and the dielectrics. The process flow for device fabrication is shown in **Figure 1a**. Bottom contacts were made of palladium/titanium (Pd/Ti) by e-beam evaporation on the substrate being Si covered by thermally grown SiO<sub>2</sub> (90 nm). The Si substrate acted as a global back gate. The graphene/hBN stack was then transferred and patterned by reactive ion etching. Afterward 10 nm Al<sub>2</sub>O<sub>3</sub> was deposited by PEALD as described above. Vias were etched by reactive ion etching to access the contact pads. Finally, the top-gate was fabricated by optical lithography, metal deposition (50 nm Al by e-beam) and lift-off. A drawing of the final device is shown in **Figure 1b**. All electrical measurements were performed at room temperature under ambient conditions. In addition, Raman spectroscopy was performed at the different stages of fabrication.

## 2. Results and Discussion

### 2.1. Damage Analysis between Al<sub>2</sub>O<sub>3</sub> Deposited by H<sub>2</sub>O and Plasma Process ALD

Raman spectroscopy and electrical characterization was performed to analyze the PEALD deposition of the Al<sub>2</sub>O<sub>3</sub> on hBN/graphene. **Figure 2** summarizes the results of the Raman spectroscopy measurements for a wafer with hBN/graphene

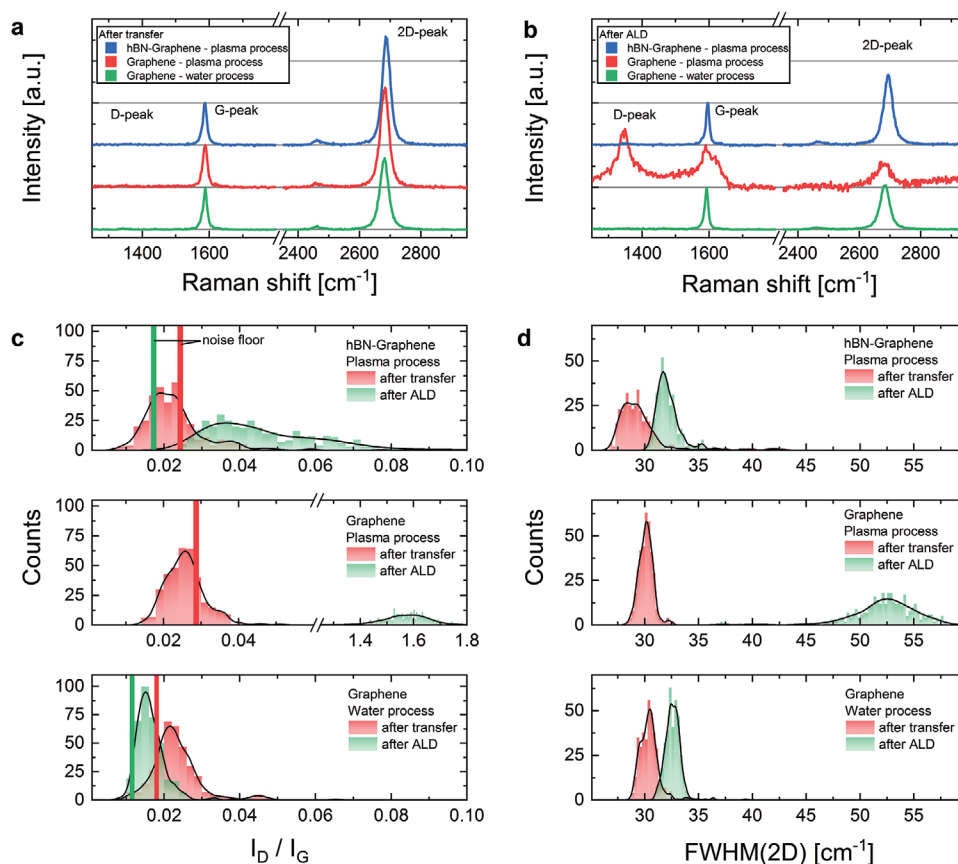


**Figure 1.** Process flow schematic for the GFET device fabrication. a) Individual building blocks and steps, b) final device.

encapsulated by PEALD, a wafer with only graphene encapsulated by PEALD and a reference wafer with only graphene encapsulated by thermal ALD. Typical Raman spectra (i.e., the spectra with the median value of  $I_D/I_G$  for each respective map) are shown in the Figure 2a recorded directly after transfer and Figure 2b after encapsulation with  $\text{Al}_2\text{O}_3$ . For graphene the intensity of the D peak located at around  $1350\text{ cm}^{-1}$  provides information on the defect density of the crystal lattice.<sup>[35]</sup> After transfer, no D-peak is visible indicating high graphene quality for all three wafers. After encapsulation a clear D-peak becomes prominent for the sample encapsulated by PEALD without hBN on top of graphene, which demonstrates that the PEALD process significantly damages unprotected graphene. For the sample encapsulated by PEALD with hBN on top of graphene, the D-peak is close to the noise floor, which demonstrates an efficient protection of the graphene layer. Actually, the whole spectrum (blue curve) of this sample looks similar to the sample encapsulated by the reference process with thermal ALD (green curve). The deposition of  $\text{Al}_2\text{O}_3$  also causes a decrease in the intensity ratio  $I_{2D}/I_G$  and a shift in the positions of the G and 2D peaks. The  $I_{2D}/I_G$  in monolayer graphene depends on the doping level,<sup>[36]</sup> with higher doping leading to a lower  $I_{2D}/I_G$  ratio. In addition the optical interference pattern provided by the dielectric environment of the graphene also can have a significant effect on the  $I_{2D}/I_G$  ratio.<sup>[37]</sup> In our samples both the doping level and the dielectric interference pattern of the substrate are changed by the deposition of  $\text{Al}_2\text{O}_3$ . Therefore the  $I_{2D}/I_G$  ratio is not a well suited parameter to monitor the doping level in the graphene. The 2D-peak position versus the G-peak position for all spectra of the Raman mappings is shown in Section S1 in the Supporting Information.

In order to investigate the structural change due to the encapsulation in more detail, histograms of key parameters have been extracted from the mapping of the Raman spectra. Figure 2c

shows the  $I_D/I_G$  intensity ratio before (red) and after (green) encapsulation. Again, the sample encapsulated by PEALD without hBN shows a significant increase in the  $I_D/I_G$  from 0.03 to 1.6, while the sample with hBN only shows a slight increase of the  $I_D/I_G$  from 0.02 to 0.04, confirming that a single layer of hBN is efficient in protecting the graphene against plasma damage during encapsulation. The reference sample encapsulated by thermal ALD even shows a reduction of the  $I_D/I_G$  ratio. However, one needs to point out that the  $I_D$  in this sample is close to the noise floor and that the peak intensities of the Raman spectra do not only depend on the crystalline structure of graphene, but also on the optical interference pattern of the substrate, which changes by the deposition of the  $\text{Al}_2\text{O}_3$ . The noise level is shown in the histogram of Figure 2c as solid perpendicular lines, and  $I_D/I_{\text{Noise}}$  is shown in Section S2 in the Supporting Information. The reduction of  $I_D/I_G$  must therefore be attributed to a reduction of the noise level due to a change in interference pattern and not to a reduction of defects. Another important parameter of the Raman spectrum of graphene is the full-width-at-half-maximum (FWHM) of the 2D peak, which mainly depends on nanoscale strain variations: A low FWHM(2D) corresponds to small strain variations,<sup>[38–40]</sup> which ultimately enables high carrier mobilities.<sup>[38–40]</sup> These variations depend on not only the quality of the graphene, but also the smoothness of the substrate as well as the interactions of the graphene with the substrate and the encapsulation.<sup>[41,42]</sup> For example, graphene encapsulated by single crystal, multilayer hBN has a very small FWHM(2D) (less than  $20\text{ cm}^{-1}$ )<sup>[42]</sup> whereas encapsulation by amorphous oxides typically increases the FWHM(2D). Figure 2d shows the histograms of FWHM(2D) of the samples before and after deposition. The sample without hBN and encapsulated by PEALD shows a significant increase of the FWHM(2D) from 28 to  $52\text{ cm}^{-1}$ . This is mainly due to the damage to the graphene caused by the plasma exposure. In contrast, the other two samples show only a moderate increase



**Figure 2.** Raman analysis for Gr/SiO<sub>2</sub>/Si and hBN/Gr/SiO<sub>2</sub>/Si before and after Al<sub>2</sub>O<sub>3</sub> deposition. a) Raman spectra for Gr/SiO<sub>2</sub>/Si and hBN/Gr/SiO<sub>2</sub>/Si after transfer. b) Raman spectra for Gr/SiO<sub>2</sub>/Si and hBN/Gr/SiO<sub>2</sub>/Si after Al<sub>2</sub>O<sub>3</sub> deposited by PEALD and TMA-H<sub>2</sub>O ALD. c) Histogram of I<sub>D</sub>/I<sub>G</sub> for Gr/SiO<sub>2</sub>/Si and hBN/Gr/SiO<sub>2</sub>/Si before and after Al<sub>2</sub>O<sub>3</sub> deposition by PEALD and thermal ALD. The solid vertical lines indicate the average noise level of the acquired mappings (green before and red after encapsulation). d) Histogram of FWHM(2D) for Gr/SiO<sub>2</sub>/Si and hBN/Gr/SiO<sub>2</sub>/Si before and after Al<sub>2</sub>O<sub>3</sub> deposition by PEALD and thermal ALD.

from around 29 to 32 (plasma ALD) or 33 cm<sup>-1</sup> (thermal ALD). This means that the PEALD encapsulation of the hBN/graphene sample delivers similar levels of local strain variations as the thermal ALD process. Note that a FWHM(2D) of 32 cm<sup>-1</sup> is state-of-the-art for CVD graphene encapsulated by a scalable method, even when compared to single crystalline CVD grown graphene flakes indicating homogeneity of the hBN monolayer transfer as otherwise holes therein would lead to local graphene damage.<sup>[43]</sup> Another parameter having an impact on the damage of the graphene is the plasma time for each cycle in the ALD process. In Section S3 in the Supporting Information we compare the Raman spectra of Al<sub>2</sub>O<sub>3</sub> deposited by PEALD on graphene with and without protection by hBN with short plasma time (0.1 s) and with longer plasma time (2 s). For the longer plasma time significant damage can be observed even with an hBN monolayer on top of the graphene, demonstrating that the deposition process also has an impact on the damage to the graphene.

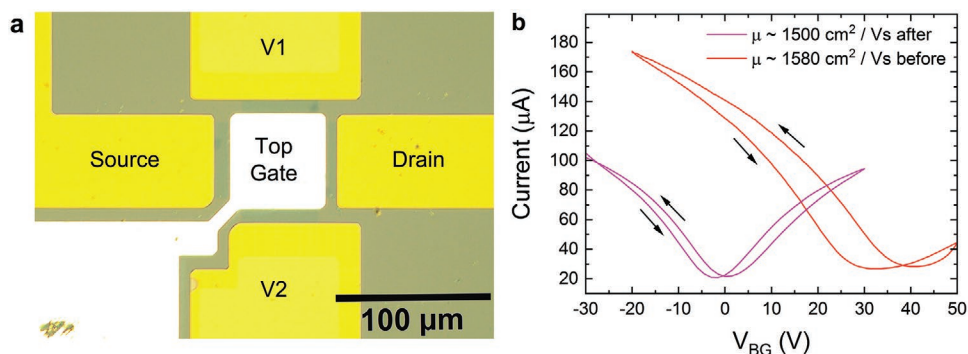
Double gate field effect devices were fabricated and Raman analysis was performed for all steps of the device fabrication (Section S4, Supporting Information). While overall the spectra are very similar and consistent with the ones shown in Figure 2, small differences are observed between the position of the D-peak and the G peak. This can be fitted as a broad peak

that we attribute to amorphous carbon (a-C).<sup>[44]</sup> In our samples source of this carbon is resist residue remaining after optical lithography, which leads to a higher peak.

## 2.2. Electrical Characterization of Devices

The electrical properties of the graphene were assessed through back-gate mode and top-gate mode drain current versus gate voltage measurements (transfer characteristics) at different stages of sample fabrication. **Figure 3a** shows an optical microscope image of one double gated device. Figure 3b shows the back-gate transfer characteristic for the same device before and after encapsulation (here with grounded top-gate) measured under ambient conditions. The two-probe field effect mobility, which includes the contact resistance, is approximately  $\mu = 1500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  before and after the Al<sub>2</sub>O<sub>3</sub> deposition, demonstrating that the PEALD process does not reduce this figure of merit. The hysteresis after the Al<sub>2</sub>O<sub>3</sub> deposition is 2.7 V, which is quite low, given that measurements were conducted at room temperature and in ambient air, and also compared with the measurement before the Al<sub>2</sub>O<sub>3</sub> deposition (8 V, note that the sweep voltages are different before and after the Al<sub>2</sub>O<sub>3</sub>



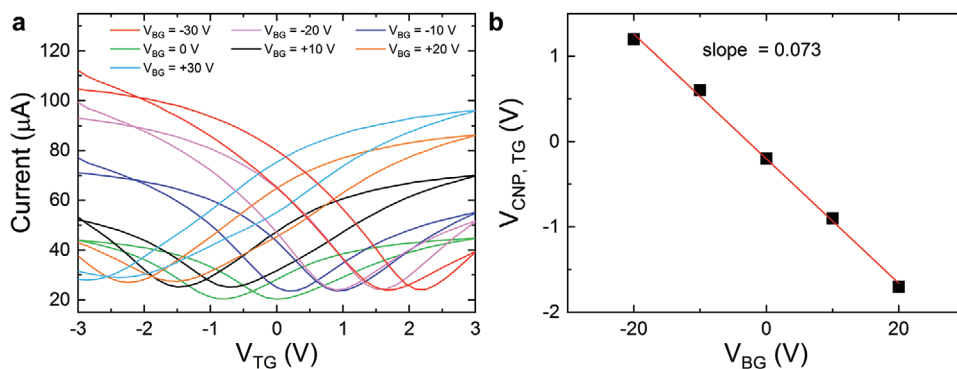


**Figure 3.** Device characterization. a) Optical microscope image of one device after top-gate fabrication. b) Transfer curves of back-gate measurements for one device before and after the Al<sub>2</sub>O<sub>3</sub> deposition and top-gate fabrication.

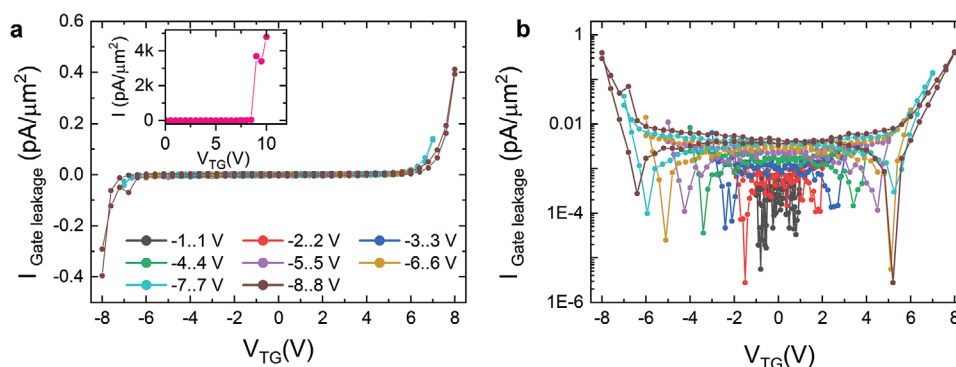
deposition). In addition, the doping level is lower after encapsulation and is close to zero. Here, doping refers to doping by charge transfer rather than substitutional doping. Similarly, low doping levels and hysteresis were observed in graphene encapsulated with Al<sub>2</sub>O<sub>3</sub> using thermal ALD.<sup>[19]</sup> For the double gate measurements, the back-gate was kept constant and the top-gate was swept. The top-gate transfer curves for seven different back-gates for one device can be seen in **Figure 4a**. The sweep range for the top gate voltage is from  $-3$  to  $3$  V and the back-gate voltages were  $0$ ,  $+10$ ,  $-10$ ,  $+20$ ,  $-20$ ,  $+30$ ,  $-30$  V. The two-probe field effect mobility is approximately  $\mu = 500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which is lower compared to the back-gate curves. The reason for this difference is that a large area of the graphene between the contact pads and the top gate is not gated by the local top gate, which results in a large series access resistance. Subtracting this access resistance would significantly increase the extracted mobility value,<sup>[45]</sup> but as this will not lead to new insights with respect to this work, such a subtraction is not performed here. The hysteresis for the top-gate sweeps is larger compared to back-gate measurements of this device (area of the top gate), although similar to other results obtained on top-gated GFETs measured at comparable electric fields.<sup>[46]</sup> From the curves in **Figure 4a** we extracted the dielectric constant  $\epsilon_r$  of the Al<sub>2</sub>O<sub>3</sub> by plotting the top gate voltage at the charge neutrality point (CNP) as a function of the applied back-gate voltage (Figure 4b). The slope of a linear fit in this plot is equal to the

ratio of the capacitance of the back gate ( $90 \text{ nm SiO}_2$ ) to the top gate capacitance ( $10 \text{ nm Al}_2\text{O}_3$ ), so  $\epsilon_r$  can be calculated. The slope is  $0.073$ , which corresponds to a top-gate equivalent oxide thickness (EOT) of  $6.6 \text{ nm}$ , assuming  $\epsilon_r = 3.9$  for SiO<sub>2</sub>. This results in a dielectric constant of  $5.9$  for the  $10 \text{ nm Al}_2\text{O}_3$  layer. This value of  $\epsilon_r$  is similar to the ones reported in literature, e.g., for thermal ALD with TMA and H<sub>2</sub>O precursors,  $4.9$ – $9.1$  is reported in literature depending on the deposition process and conditions of the measurements.<sup>[16,18,21,46]</sup> Note that only  $10 \text{ nm Al}_2\text{O}_3$  have been assumed as top-gate dielectric. The monolayer hBN and possible interfacial contamination were not included in the estimation of the dielectric constant of the Al<sub>2</sub>O<sub>3</sub>. Considering such effects, the dielectric constant of Al<sub>2</sub>O<sub>3</sub> will become slightly larger. However, for device applications only the total capacitance or the EOT of the top-gate are important.

**Figure 5** shows the top-gate leakage current for different sweeping ranges in linear (a) and log-scale (b). The gate dielectric is stable for sweeping ranges from  $-8$  to  $8$  V with leakage current densities below  $1 \text{ pA } \mu\text{m}^{-2}$ . Above  $8$  V irreversible breakdown happens in this device (see inset **Figure 5a**). Overall, in  $50$  devices the breakdown voltage was measured on different wafers with values between  $7.5$  and  $9.8$  V.  $8$  V correspond to an electric field strength of about  $8 \text{ MV cm}^{-1}$ , which is very high for dielectrics deposited on graphene, especially keeping in mind the rather large area of the gate electrode ( $50 \times 50 \mu\text{m}^2$ ). These values match those in reference structures without



**Figure 4.** Transfer curves of top-gate measurements with the back-gate voltage kept constant for both sweeping directions. a) Sweep range:  $-3$  to  $3$  V, each curve (different color) was at a different constant back-gate voltage from  $-30$  to  $30$  V ( $10$  V steps). b) Top gate voltage at the charge neutrality point (CNP) as a function of the applied back-gate voltage.



**Figure 5.** Electrical behavior of one device. a) Leakage current as a function of the gate voltage for eight different sweep ranges from 2 V (–1 to 1 V) to 16 V (–8 to 8 V). The behavior is stable for several sweeps. Inset: Sweep range of 20 V plotted from 0 to 10 V. Irreversible breakdown of the device occurs at 8 V. b) The same leakage currents of (a) plotted on a log-scale.

graphene for the Al<sub>2</sub>O<sub>3</sub> ALD process.<sup>[30]</sup> Therefore, we conclude that the dielectric is not only pinhole-free, but also that the quality of the dielectric is not reduced due to the growth on top of a 2D material heterostructure.

### 3. Conclusion

The present study investigates the deposition of Al<sub>2</sub>O<sub>3</sub> on graphene by PEALD with and without hBN as an interfacial layer. Monolayer CVD hBN acts as an efficient protection layer against direct plasma damage, while the direct plasma process on graphene without protection caused significant damage. The dielectric properties of the PEALD Al<sub>2</sub>O<sub>3</sub> are excellent with an EOT of 6.6 nm and a high breakdown electric field strength and gate leakage currents below 1 pA μm<sup>-2</sup> at gate fields up to 8 MV cm<sup>-1</sup>.

### 4. Experimental Section

**CVD of Graphene and hBN:** CVD grown monolayer graphene and monolayer hBN were used from in-house sources and commercially available on 15 cm Cu foils (Grolltex, San Diego, USA). The in-house growth was performed as follows: Continuous monolayer graphene films consisting of mm-sized domains were grown by CVD on Cu foils.<sup>[47]</sup> Briefly, Cu foils (99.9%) were oxidized in air at 250 °C for 5 min, followed by annealing in Ar (50 mbar, 30 min), and subsequently by H<sub>2</sub> annealing (12 mbar H<sub>2</sub>, 38 mbar Ar, 60 min) at around 1075 °C. Graphene was grown by introducing a CH<sub>4</sub>/H<sub>2</sub>/Ar mixture (1.2 × 10<sup>-2</sup>, 9, and 41 mbar, respectively) for 6 h. Monolayer hBN was grown by CVD on Fe foils as described in prior work.<sup>[47–49]</sup> Briefly, 0.1 mm Fe foils (99.8% purity) were oxidized in air at 350 °C for 5 min, followed by annealing in 1 × 10<sup>-2</sup> mbar Ar at 980 °C for 20 min to remove localized impurities in the foil and create a minute oxygen reservoir. A brief reducing treatment of 3 × 10<sup>-3</sup> mbar acetylene was applied for 5 min, followed by a 20 min dose of ammonia at 1 × 10<sup>-2</sup> mbar. Borazine was added together with ammonia with partial pressure of 8 × 10<sup>-4</sup> mbar for 90 min to grow a continuous monolayer hBN film consisting of domains of hundreds of micrometers.

**Wet Transfer Using PMMA and Cu Etching:** Some experiments were conducted with monolayer graphene and monolayer hBN grown by CVD on metal foils commercially available on 15 cm Cu foils (Grolltex, San Diego, USA). The hBN/graphene stack was prepared by a sequential wet chemical transfer of the layers from the growth substrate (Cu) using PMMA as supporting layer.<sup>[50]</sup> First, the hBN was released by etching the

copper foil, rinsed in water, and transferred to graphene on copper foil. Subsequently, the hBN/graphene stack (between 1 × 1 and 4 × 4 cm<sup>2</sup>) was released by again etching the copper foil and, after rinsing in water, transferred to a 6-inch Si wafer covered by 90 nm thermally grown SiO<sub>2</sub>. In the reference samples only graphene was transferred without hBN.

**Wet Transfer Using PC and Electrochemical Delamination:** For the graphene and hBN that were grown in-house, the following transfer method was used: After controlled humidity oxidation of the hBN/Fe interface, and coating with a support polymer (poly-bisphenol-A-carbonate, PC), the PC/hBN stack was detached via electrochemical delamination.<sup>[51]</sup> This was directly transferred to graphene/Cu and after drying and curing (160 °C, 5 min), the PC/hBN/graphene structure was detached from Cu via electrochemical delamination. Finally, the stack was transferred onto the target pre-patterned wafer and PC was dissolved in chloroform. This material and transfer were just used for device fabrication.

**Al<sub>2</sub>O<sub>3</sub> ALD Deposition:** After the transfer, the samples were encapsulated by PEALD with 10 nm of Al<sub>2</sub>O<sub>3</sub> in the Oxford Instruments Atomfab ALD and FlexAL system using TMA and oxygen plasma as precursors. For the Atomfab ALD system the deposition temperature was 300 °C, the plasma time was 0.1 s and the total cycle time was 0.9 s. Reference samples were prepared and covered by 20 nm of Al<sub>2</sub>O<sub>3</sub> using a thermal (i.e., plasma free) ALD process with TMA and H<sub>2</sub>O (10 s cycle time) in a FlexAL ALD at 150 °C.

**Raman Characterization:** A Horiba XPlora Raman Spectrometer with a 100× microscope objective was used for Raman measurements. The excitation wavelength was 532 nm. Raman spectroscopy was performed before and after the deposition to monitor the structural parameters like defects and strain variation. 10 × 10 μm<sup>2</sup> areas with 121 spectra each were measured at several locations for each sample. The peaks of each spectrum were fitted by a Lorentzian function. From the fits the ratio between the D and G peak intensities as well as the FWHM of the 2D peak was determined and histograms were created for each sample.

**Device Fabrication:** GFET were fabricated according to the work flow depicted in Figure 1a. Bottom contacts were made of Pd/Ti by e-beam evaporation on the substrate, i.e., Si covered by thermally grown SiO<sub>2</sub> (90 nm). The Si substrate acted as a global back gate. Afterward the graphene/hBN stack was transferred (as described above) and patterned by reactive ion etching. Afterward 10 nm Al<sub>2</sub>O<sub>3</sub> was deposited by PEALD in an Oxford Instruments Atomfab ALD system as described above. Vias were etched by reactive ion etching to access the contact pads. Finally, the top-gate was fabricated by optical lithography, metal deposition (50 nm Al by e-beam evaporation) and lift-off. A drawing of a final device is shown in the Figure 1b. It was confirmed in previous works using Raman spectroscopy, X-ray photoelectron spectroscopy, and transmission electron microscopy that these films are monolayer films of hexagonal boron nitride.<sup>[48,49,52]</sup>

**Electrical Measurements:** The electrical properties of the graphene film and of the dielectric were measured in double-gated graphene

transistors, having a global back-gate and a local top-gate electrode. The back-gate transfer curves were performed to compare the mobility before and after encapsulation. The breakdown voltage and leakage current were extracted from the top-gate measurements and the dielectric constant was extracted from double-gate measurements. The Si substrate acted as global back gate. All electrical measurements were performed at room temperature under ambient conditions.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

Research data are not shared.

## Keywords

Al<sub>2</sub>O<sub>3</sub> thin film, ALD, breakdown field, double-gate-transistors, GFET, graphene, hexagonal boron nitride

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