

Development of arsenic doped Cd(Se,Te) absorbers by MOCVD for thin film solar cells

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Abstract

Recent developments in CdTe solar cell technology have included the incorporation of ternary alloy Cd(Se,Te) in the devices. CdTe absorber band gap grading due to Se alloying contributes to current density enhancement and can result in device performance improvement. Here we report Cd(Se,Te) polycrystalline thin films grown by a chamberless inline atmospheric pressure metal organic chemical vapour deposition technique, with subsequent incorporation in CdTe solar cells. The compositional dependence of the crystal structure and optical properties of Cd(Se,Te) are examined. Selenium graded Cd(Se,Te)/CdTe absorber structure in devices are demonstrated using either a single CdSe layer or CdSe/Cd(Se,Te) bilayer (with or without As doping in the Cd(Se,Te) layer). Cross-sectional TEM/EDS, photoluminescence spectra and secondary ion mass spectroscopy analysis confirmed the formation of a graded Se profile toward the back contact with a diffusion length of $\sim 1.5 \mu\text{m}$ and revealed back-diffusion of Group V (As) dopants from the CdTe layer into Cd(Se,Te) grains. Due to the strong Se/Te interdiffusion, CdSe in the Se bilayer configuration was unable to form an n-type emitter layer in processed devices. In situ As doping of the Cd(Se,Te) layer benefited the device junction quality with current density reaching 28.3 mA/cm^2 . The results provide useful insights for the optimisation of Cd(Se,Te)/CdTe solar cells.

Keywords: CdTe; CdSe; Cd(Se,Te); thin film; As doping; MOCVD; solar cells; photovoltaics

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1. Introduction

Recent advances in CdTe thin film solar cells have shown improved device performance, with a record efficiency of 22.1% [1, 2]. One of the main developments has been the modification of the absorber layer with Se alloying [3 – 5]. CdTe absorber band gap is graded via this approach (from 1.5 eV to ~1.4 eV) toward the front interface of the device, due to the band bowing property of Cd(Se,Te) [6 - 8]. As a result, current collection can be improved in the infrared region of the spectrum. In addition, it is also possible to avoid the use of traditional window layers (with characteristic parasitic blue/near UV absorption), and improve short wavelength response, therefore making it possible to achieve maximum J_{SC} in record devices [9]. According to theoretical analysis based on ideal values for J_{SC} , V_{OC} , FF and efficiency with CdTe band gap changes [10], a projected J_{SC} increase due to band gap reduction from 1.5 to 1.38 eV will more than compensate for V_{OC} and FF reduction, resulting in overall efficiency increase. Further benefits of introducing Se into a CdTe absorber include increased minority carrier lifetimes and grain boundary passivation [11, 12].

Initially, Paudel and Yan replaced the CdS window layer in the classical “CdS/CdTe” superstrate device structure with sputtered CdSe and showed an enhanced spectral response with J_{SC} approaching 27 mA/cm² [13]. Munshi and co-workers [14] achieved confirmed cell efficiency of 19.1%, by incorporating selenium into the CdTe absorber as well as introducing other advances, such as replacement of CdS with MgZnO and insertion of Te layer prior to the back contact. Recently, Ablekim and co-workers [9] reported 19% efficient solar cells using thermally evaporated CdSe and CdTe in a similar device structure. In both cases, CdSe layers provided a reservoir of Se for diffusion into, and alloying with, the CdTe absorber, resulting in a graded bandgap. This diffusion is driven by the CdCl₂ heat treatment (CHT), which is still indispensable for passivation of the device. However, this approach is not always straightforward, as it may leave a residual (non-consumed) CdSe layer at the front of the device, which could contribute to poor device performance through the formation of non-uniform band gaps below that of CdTe. To this end, direct alloy growth of Cd(Se,Te) has also been reported by co-sublimation [15]. Producing high quality and uniform films via this process was, however, found to be challenging. Recently, Li and co-workers [16] reported highly efficient Cd(Se,Te)/CdTe solar cells, where the Cd(Se,Te) layer was grown by vacuum co-evaporation.

To the best of our knowledge, there has been no reports on Cd(Se,Te)/CdTe device fabrication by metalorganic chemical vapour deposition (MOCVD). MOCVD offers a non-vacuum processing alternative, in addition to ease of alloying and doping, with promising PV performance (~15%) [17]. In this paper, it is reported for the first time, results of direct Cd(Se,Te) alloy film growth and in combination with separate binary CdSe as an n-type emitter layer, displaying excellent composition

control and *in-situ* p-type doping using arsenic, with subsequent incorporation into CdTe solar cells. Results of the PV performance of Cd(Se,Te)/CdTe thin film solar cells will also be presented to illustrate the potential role of CdSe as an emitter layer.

2. Experimental details

Cd(Se,Te) thin films were first deposited onto a 10 x 10 cm² transparent conducting oxide (TCO) coated substrate in our in-house developed inline chamberless MOCVD system [18, 19] at a substrate temperature of 480°C. The commercial TCO consisted of 450 nm thick SnO₂:F (FTO) layer with sheet resistance of 10 Ω/sq and 10 nm of undoped SnO₂ buffer layer, deposited on a 3 mm thick soda lime glass (NSG Pilkington). In this system, a nitrogen stream surrounding the deposition area provides the isolation necessary for the chemical reaction with the surrounding ambient. Metalorganic precursors used include Dimethylcadmium (DMCd), Diisopropyltelluride (DiPTe) and Diethylselenide (DESe) for cadmium, tellurium and selenium, respectively. The DESe/(DESe+DiPTe) ratio was varied between 0 to 1 for different layers to adjust the film composition. Total flow rate of the precursor gases plus the nitrogen carrier/dilution gas through the injector nozzle was about 2.0 l/min. Translation speed of the heated substrate under the coating head was set to 1.8 – 5.4 cm/min, for an optimum coating quality in terms of composition and thickness uniformity. Four coupons of 5 × 5 cm² could be obtained from the TCO/Cd(Se,Te) substrate and used for subsequent fabrication of solar cell devices.

To fabricate the Cd(Se,Te)/CdTe devices, the TCO/Cd(Se,Te) substrate (cleaved to 5 x 5 cm²) was transferred onto a horizontal MOCVD reactor, where a CdTe absorber layer was grown at 390°C. The CdTe absorber comprised of 3 μm thick 1 × 10¹⁸ /cm³ As doped p-CdTe layer terminated with a more heavily arsenic incorporated (>1 × 10¹⁹ /cm³) 0.3 μm cap layer to form a low resistance back contact. The precursor for As doping was tris(dimethylamino)arsenic. Further experimental details on device processing can be found elsewhere [19]. Grain boundary passivation was performed by CHT. This entailed depositing a thick layer (~1 μm) of CdCl₂ at 200°C, then annealing for 10 minutes at 420°C in a hydrogen ambient. Tertiarybutylchloride (tBuCl) was used as the Cl precursor. Following cool down, the device stack was rinsed with deionised water to dissolve the excess CdCl₂, dried with N₂ gas and subsequently subjected to a low temperature (170°C) anneal for 90 mins in air [17]. Device fabrication was completed by thermal evaporation of gold (Au) contact pads of 0.5 × 0.5 cm² across the CdTe surface.

Compositional analysis of the Cd(Se,Te) films was carried out using a Hitachi TM3000 table-top scanning electron microscope (SEM) equipped with an energy dispersive X-ray spectroscopy (EDS) detector (Oxford Instruments), whilst high resolution plan-view images were obtained using an HS-4800 SEM. Se composition (x) is defined as $x = \text{Se}/(\text{Se} + \text{Te})$, whereby Se at.%, Te at.% were determined

by EDS. Micro-PL measurements were performed at room temperature with a Renishaw InVia confocal Raman microscope (Renishaw plc., Wotton-Under-Edge, UK) in backscattering configuration using a 532 nm green laser operated at a maximum power of 30 mW with a 50× objective (numerical aperture = 0.50, beam diameter $\approx 1 \mu\text{m}$). X-ray diffraction (XRD) measurements were obtained using a D8 Discover instrument (Bruker, Karlsruhe, Germany) diffractometer in the Θ - 2Θ configuration with a Cu-K α source ($\lambda = 0.15418 \text{ nm}$) operated at 40 kV and 40 mA.

Sample cross sections for Scanning Transmission Electron Microscopy (STEM) were prepared using a gallium focused ion beam (FIB) with a dual beam FEI Nova 600 Nanolab. A standard in situ lift out method was used to prepare cross-sectional samples through the coating into the glass substrate. A platinum over-layer was deposited to define the surface and homogenize the final thinning of the samples down to $\sim 100 \text{ nm}$. Transmission Electron Microscopy (TEM) was undertaken using a Tecnai F20 operating at 200 kV to investigate the detailed microstructures of the cell cross sections. The system was equipped with an Oxford instruments X-max N80 TLE SDD EDX detector and this was used in STEM mode to collect elemental distribution maps. Details of the procedures followed are available elsewhere [20].

Elemental (As, Se, etc.) depth profiling was performed via secondary-ion mass spectroscopy (SIMS) using a Cameca IMS-4f instrument with Cs⁺ ion source operating at 10 keV energy and 20 nA current (LSA Ltd). Samples for SIMS were prepared by peeling off the entire absorber stack from the growth substrate (FTO/SnO₂) using the lift-off method described in Perkins *et al.*, [21], which involves bonding the sample with an epoxy adhesive to a flat transfer substrate and dipping the assembly in liquid nitrogen. Peeling of the device stack and starting the SIMS measurement from this surface allowed us to profile a smooth surface beginning at the absorber/oxide interface which provides better resolution at the front interface. This enabled the measurement to start close to the front interface, which reduced the depth resolution lost during sputter removal, and avoids the roughness from the back.

AM 1.5 current density - voltage (*J-V*) measurements obtained with a Keithley 2400 source meter were performed using an Abet Technologies Ltd. solar Sun 2000 solar simulator (Class A) with the light power density calibrated using a GaAs reference cell. The capacitance - voltage (*C-V*) characteristics were measured using a Solartron Impedance Analyzer. External quantum efficiency (*EQE*) measurements were carried out using a Bentham PV300 spectrometer, with system response calibrated with a certified c-Si reference detector.

3. Results and discussion

3.1. Growth and characterisation of Cd(Se,Te) thin films

Cd(Se,Te) thin films of 380 nm thickness and with different Se composition were successfully grown by inline MOCVD at a minimum substrate surface temperature of 480°C. No film growth below this temperature was attributed to the relatively high thermal stability of Se precursor (DESe). A plot of Se composition (x) versus the precursor partial pressure ratio $\text{DESe}/(\text{DESe} + \text{DiPTe})$ is shown in Fig. 1, whereby the value of x was determined by EDS measurements. It can be seen that a linear compositional control of Se content can be achieved by varying the $\text{DESe}/(\text{DESe} + \text{DiPTe})$ ratio using chamberless inline MOCVD technique.

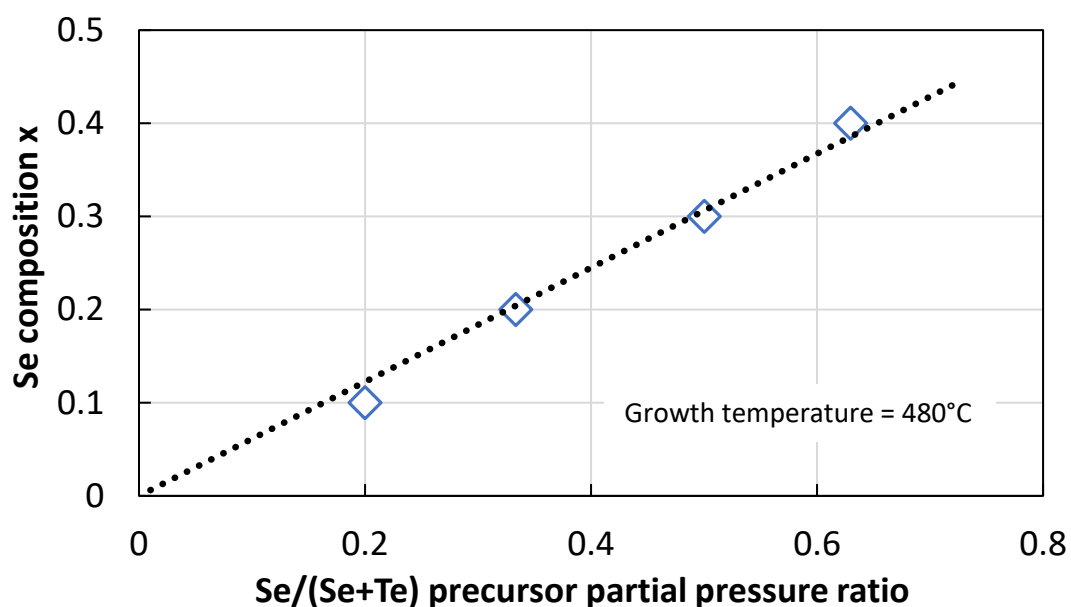


Figure 1: Measured Se composition (x) as a function of the $\text{Se}/(\text{Se} + \text{Te})$ precursor partial pressure ratio

The morphology of Cd(Se,Te) films with Se composition, $x = 0.1, 0.2, 0.3$ and 1.0 were analysed and are shown in Fig. 2. As x increases from 0.1 to 0.3, surface crystalites become more faceted. However, in the case of the binary CdSe thin film, grains appear to coalesce, losing the faceted appearance, accompanied with the formation of voids. Similar observations have been reported on the morphology of Cd(Se,Te) films by co-sublimation [15].

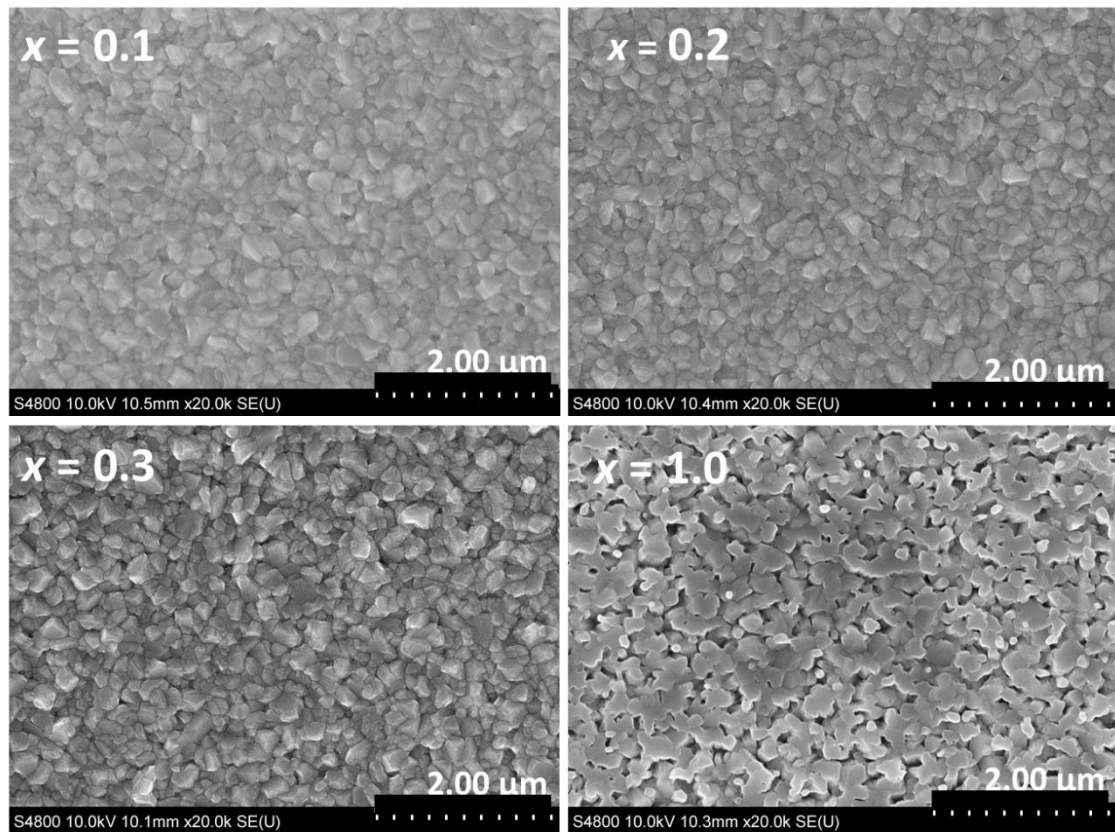


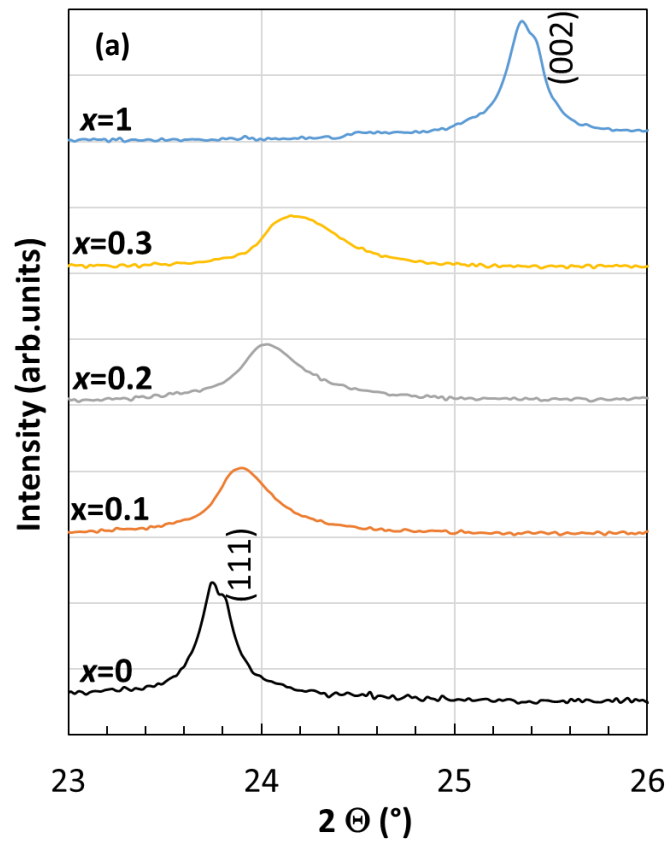
Figure 2: Plan-view (SEM) of selected Cd(Se,Te) thin films (380 nm thick)

The Cd(Se,Te) films were found to exhibit polycrystalline characteristics from XRD measurements and showed compositional-dependent crystallinity. The expanded view around the preferential orientations for the grown films is displayed in Fig. 3 (a). The (111) peak of the cubic (zinc-blende) structure for CdTe is positioned at $2\Theta = 23.74^\circ$, consistent with literature [22]. As the Se content increases from $x = 0.1$ to 0.3, the (111) peak shifts to higher 2Θ values. For Se rich films and CdSe, the 111 texture with cubic structure is replaced with a hexagonal (wurtzite) structure with (002) preferential orientation [23]. Both cubic and hexagonal phases were found to coexist in hot wall deposited Cd(Se,Te) with $x = 0.4$ and 0.6 [24], which suggests a cubic-hexagonal transition region in the range $0.4 \leq x \leq 0.6$. Interestingly zinc blende structures have also been reported for CdSe, via other synthesis processes, such as electron beam deposition [8] and dip-coating method [25], suggesting that the choice of processing technique and conditions are crucial to the resulting film's crystalline properties. The (111) peak of the Cd(Se,Te) ternary films are noted to be relatively wider than CdTe (Fig. 3a). This can be attributed to local compositional inhomogeneity and crystal disorder [22]. The lattice parameter for the cubic films (a) was calculated using Equation 1, and those of the hexagonal films (a, c) via Equation 2 [26].

$$\sin^2\theta = \frac{\lambda^2}{4a^2} (h^2 + k^2 + l^2) \quad [1]$$

$$\sin^2\theta = \frac{\lambda^2}{4} \left[\frac{4}{3} \left(\frac{h^2+hk+k^2}{a^2} \right) + \frac{l^2}{c^2} \right] \quad [2]$$

Fig. 3 (b) gives a plot of the lattice parameter vs composition for the cubic films in the $x = 0 - 0.3$ range. A linear variation of the lattice parameter with composition (x) is observed, in accord with Vegard's law. The summary of the XRD parameters for all films measured are presented in Table 1. In calculating the lattice parameters for hexagonal structured CdSe with equation 2, the reflection of the Miller indices of the type $hk0$ was used, in this case (210) reflection at 51.5° 2θ diffraction angle (see Fig. S1 for the wide range XRD spectra), consequently reducing the second factor of equation 2 to zero, allowing for the determination of parameter a first. Using (002) reflection reduces the first factor of Equation 2 to zero (since $h = k = 0$), which allowed straightforward calculation of parameter c . These values are seen to be in good agreement with previous reports [8, 24, 15, 27].



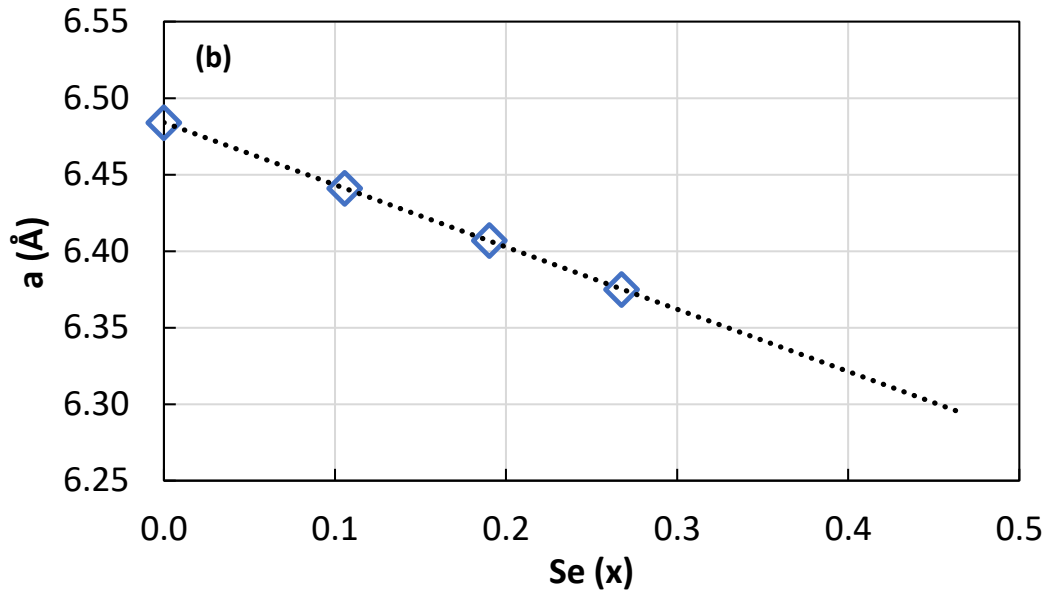


Figure 3: (a) XRD spectrum of selected Cd(Se,Te) thin films (expanded view around the dominant (111) and (002) peaks for cubic and hexagonal phases, respectively). (b) Variation of the lattice constant with Se content for cubic films ($0 \leq x \leq 0.3$)

Table 1: XRD parameters determined using the dominant (111) and (002) peaks shown in Fig. 3 (a). Se composition (x) calculated using the lattice constant is in good agreement with EDS results. Crystallite size was estimated using the Scherrer equation.

Sample	(111) 2 θ (°)	(002) 2 θ (°)	a (Å)	c (Å)	x (from XRD)	x (from EDS)	FWHM (111) (°)	FWHM (002) (°)	Crystallite size (nm)
CdTe	23.74	-	6.48	-	0.00	0.00	0.116	-	69.91
CdSe _{0.1} Te _{0.9}	23.90	-	6.44	-	0.11	0.10	0.245	-	33.12
CdSe _{0.2} Te _{0.8}	24.03	-	6.41	-	0.19	0.20	0.307	-	26.47
CdSe _{0.3} Te _{0.7}	24.15	-	6.38	-	0.27	0.30	0.380	-	21.37
CdSe	-	25.35	4.69	7.02	1.00	1.00	-	0.124	65.68

It is important to note the resulting phase of the Cd(Se,Te) layer in the final solar cell structure is also very crucial to photovoltaic performance, as Poplawsky and co-workers [28] have indicated the wurtzite phase is photo-inactive, thus not beneficial for high performance PV.

The room temperature micro-PL spectra of the Cd(Se,Te) films, collected with 0.3 – 1.5 mW power, beam diameter $\sim 1 \mu\text{m}$, and acquisition time of 5 s, are displayed in Fig. 4a.

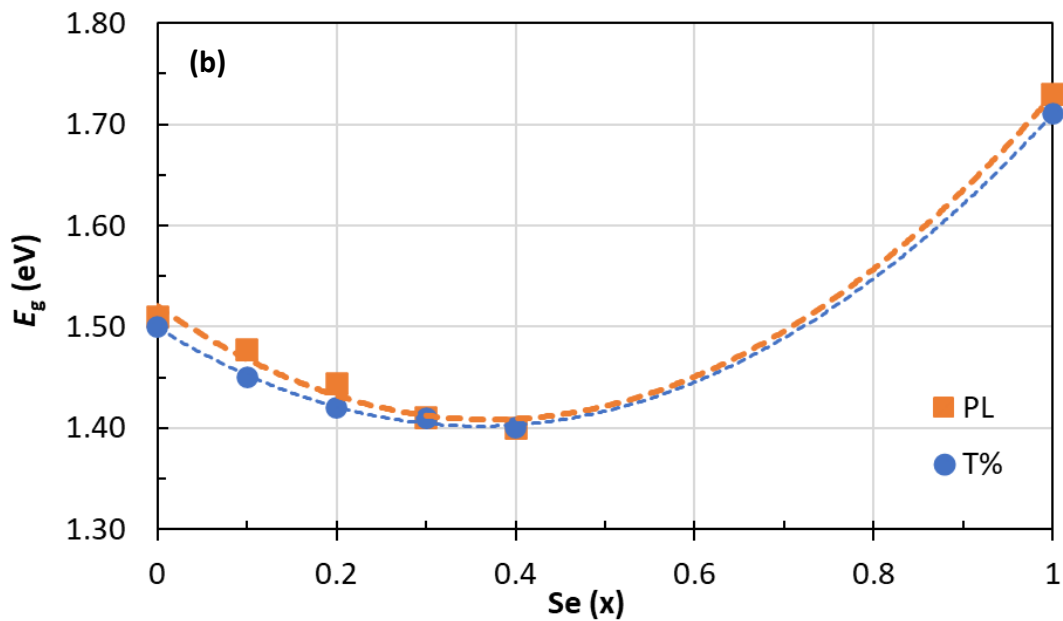
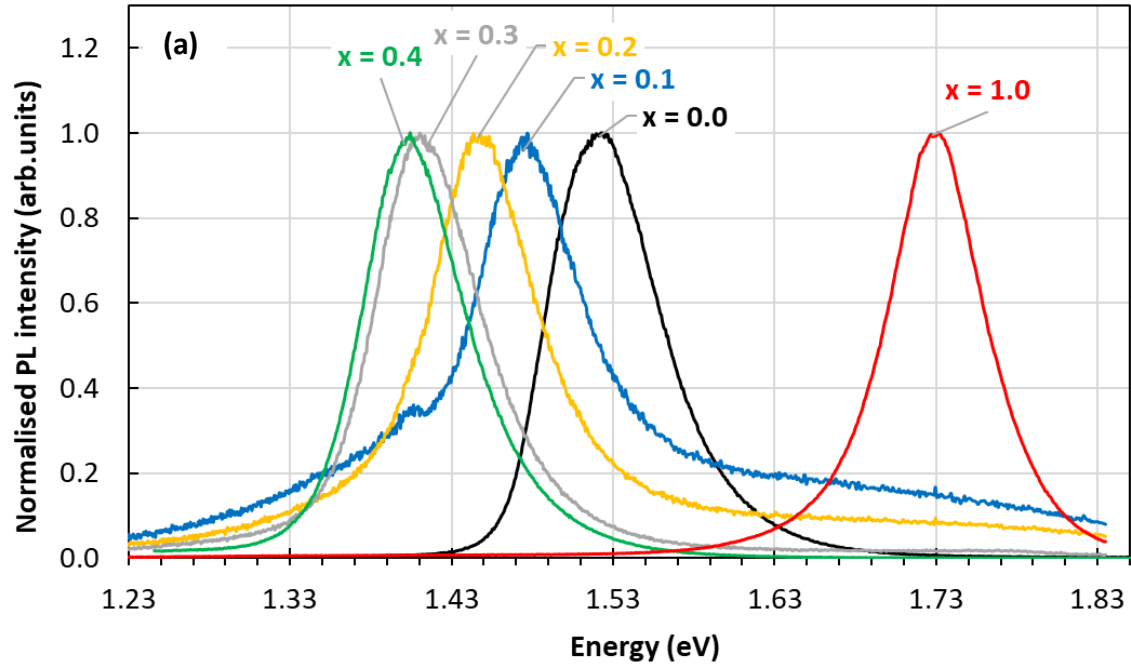


Figure 4: (a) Micro-PL spectrum of Cd(Se,Te) thin films with $x = 0$ (CdTe), 0.1, 0.2, 0.3, 0.4 and 1 (CdSe), and (b) E_g (from Tauc plots and PL spectrum) vs. composition (x). The broken lines are polynomial fits.

The PL peak of CdTe is centered on 1.52 eV, which shifts to lower energies as x is increased from 0.1 to 0.4 and then increases to 1.73 eV for CdSe, displaying a bowing effect (Fig. 4b). The optical bandgaps, E_g , measured from transmission spectra (Tauc plots) of these films (shown in Fig. S2) are shown in Fig. 4b and can be seen to compare well with the results from PL spectrum analysis. The orange broken line in Fig. 4b is a second-order polynomial fit, from which the following relationship for the compositional dependence of E_g (PL) of Cd(Se,Te) thin films was extracted:

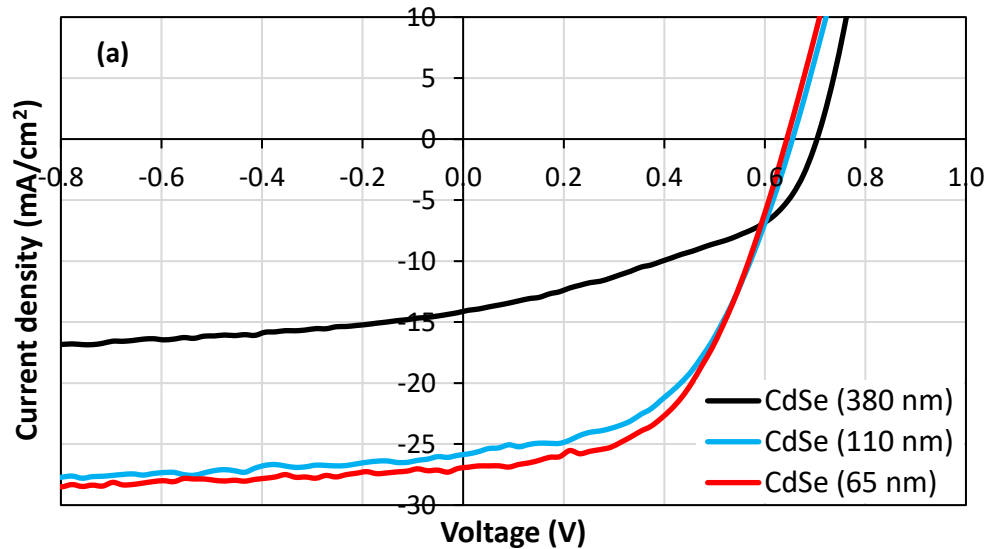
$$E_g(x) = 1.73x + 1.52(1-x) - bx(1-x) \quad (3)$$

where $b = 0.81$ is the bowing parameter.

Similarly, a bowing parameter of 0.75 was deduced with the transmission spectra measurement. The values 0.81 and 0.75 are within the range of reported bowing parameters estimated by different measurement techniques for bulk and thin film Cd(Se,Te) fabricated by different methods [29]. A similar quadratic variation of bandgap with composition have been reported, for example, for Cd(Se,Te) alloys by the Bridgeman method [7], e-beam evaporation [8] and co-evaporation [27]. Equation 3 can therefore be used to calculate the bandgap of a given composition of Cd(Se,Te). Further, the $E_g(\text{PL})$ vs x curve (Fig. 4b) exhibits a minimum between $x = 0.3 - 0.4$. Feng *et al.* [7] reported similar values of x for minimum E_g from their combined PL and theoretical studies on Bridgeman grown Cd(Se,Te). Fig. 4b indicates that the minimum E_g attainable in the current work, that is for a graded CdTe absorber via Se alloying, is ~ 1.40 eV, corresponding to a Se content of 35-40%.

3.2. Cd(Se,Te)/CdTe thin film solar cells

Firstly, undoped CdSe layers of 380, 110 and 65 nm thickness were investigated in the device structure FTO/SnO₂/CdSe/CdTe:As. Figure 5 shows the illuminated J-V curves and EQE spectra of these devices. Box plots of the J-V data (reference CdSe-free device included) are shown in Fig. 6 with the respective PV parameters summarised in Table S1.



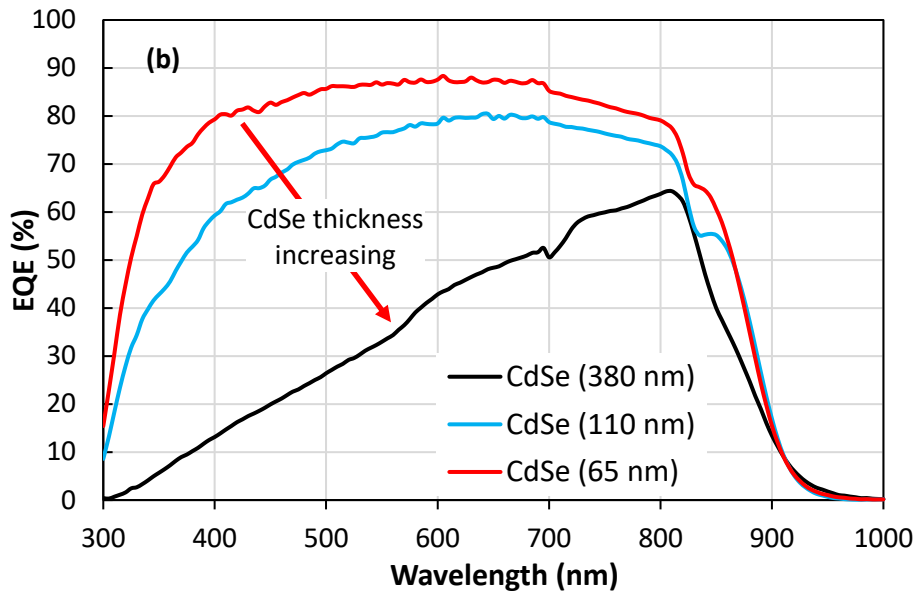


Figure 5: Under illumination J-V curves (a) and EQE spectra (b) of FTO/SnO₂/CdSe/CdTe:As devices

Devices without a CdSe layer performed poorly, mainly due to very low V_{oc} (see Table S1). With the incorporation of a CdSe buffer, all PV parameters improve, which indicates the important role of CdSe introduction. The role of CdSe buffer in this case is believed to be akin to the traditional CdS window layer which provides favourable interface to the front contact, minimizing interfacial recombination. Device performance improvement was observed with reducing CdSe layer thickness, and the best PCE of 9.2% was measured in a cell with 65 nm CdSe. This is mainly due to a significant enhancement in J_{sc} which is consistent with the EQE response in the 300 – 800 nm region. Some contribution, albeit small, is also from the FF, as it slightly improves with the thinning CdSe layers. A high J_{sc} of 26.9 mA/cm² is obtained in the cell with 65 nm CdSe. J_{sc} decreased sharply to 14.1 mA/cm² when the CdSe layer thickness was increased to 380 nm, with its EQE showing a buried junction effect. The slightly better V_{oc} of the 380 nm CdSe device can be attributed to the relatively higher apparent carrier density (N_A) measured in the absorber layer of this sample (see Fig. S3). Similar observations of J_{sc} decrease and emergence of a buried junction effect were also reported by [13], where the CdSe layer thickness was varied from 0 to 350 nm. They speculated that the consumption of the CdSe layer during CdCl₂ treatment could be incomplete in the case of thicker CdSe (≥ 350 nm), leaving a remnant CdSe binary layer at the front of the device causing significant parasitic absorption. However, the presence of any remnant CdSe was not observed here, even in the case of 380 nm CdSe.

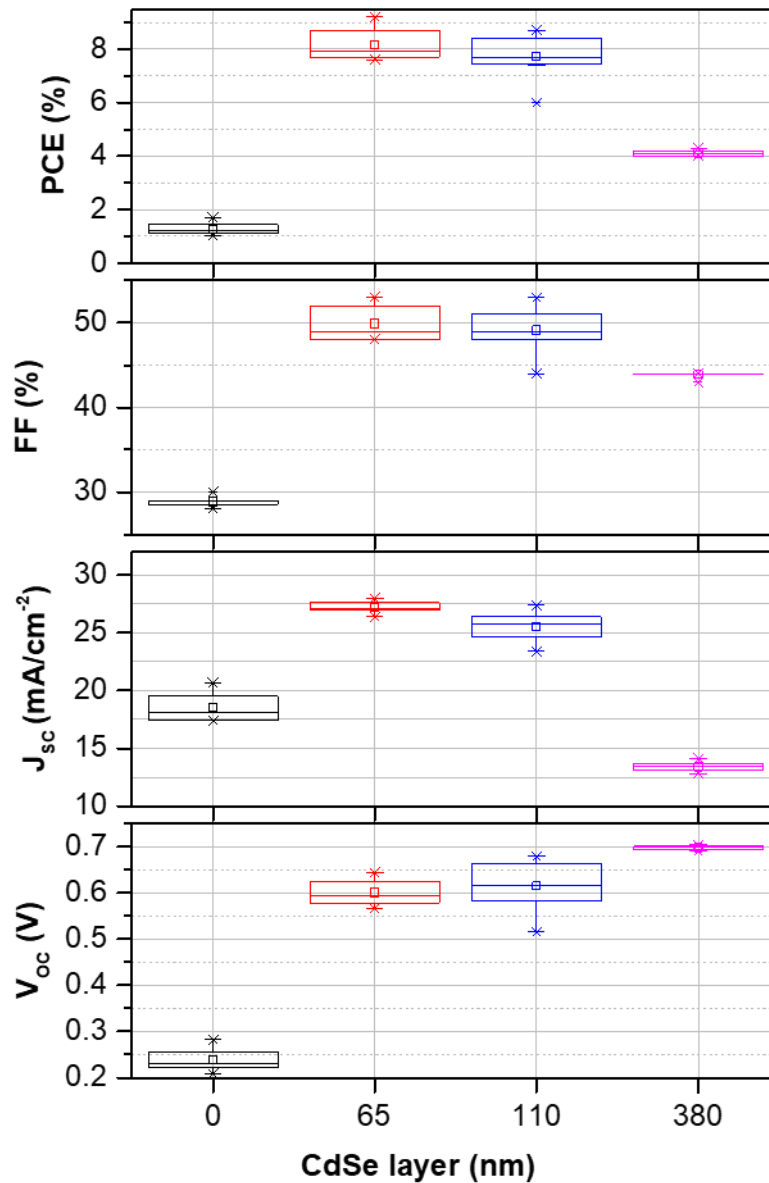
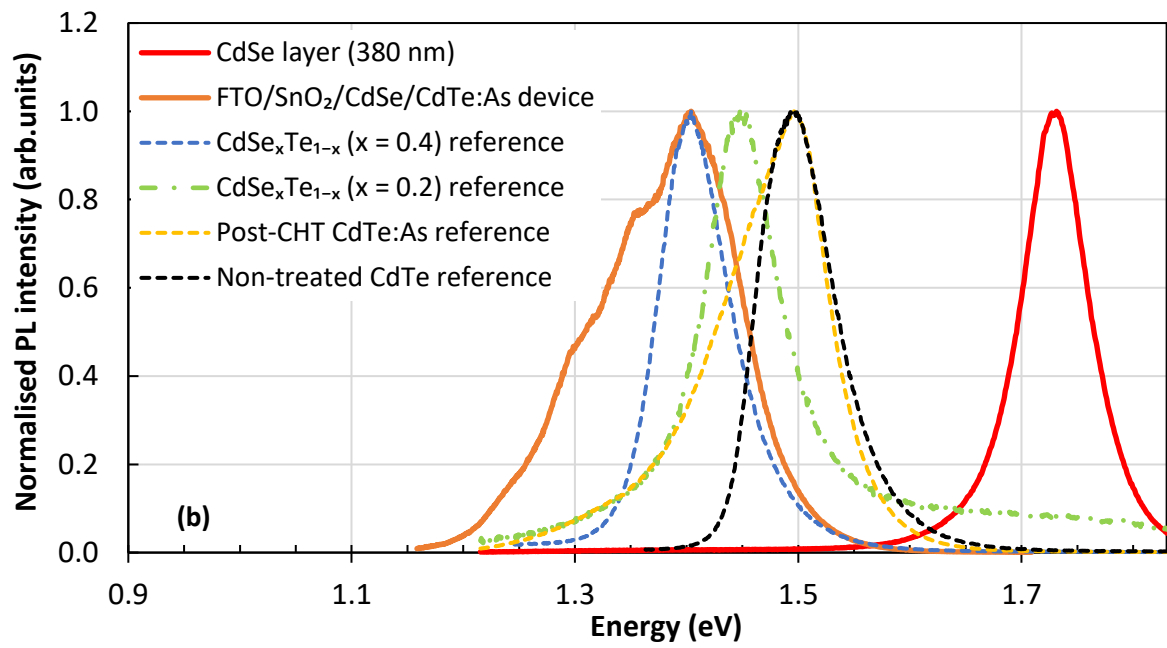
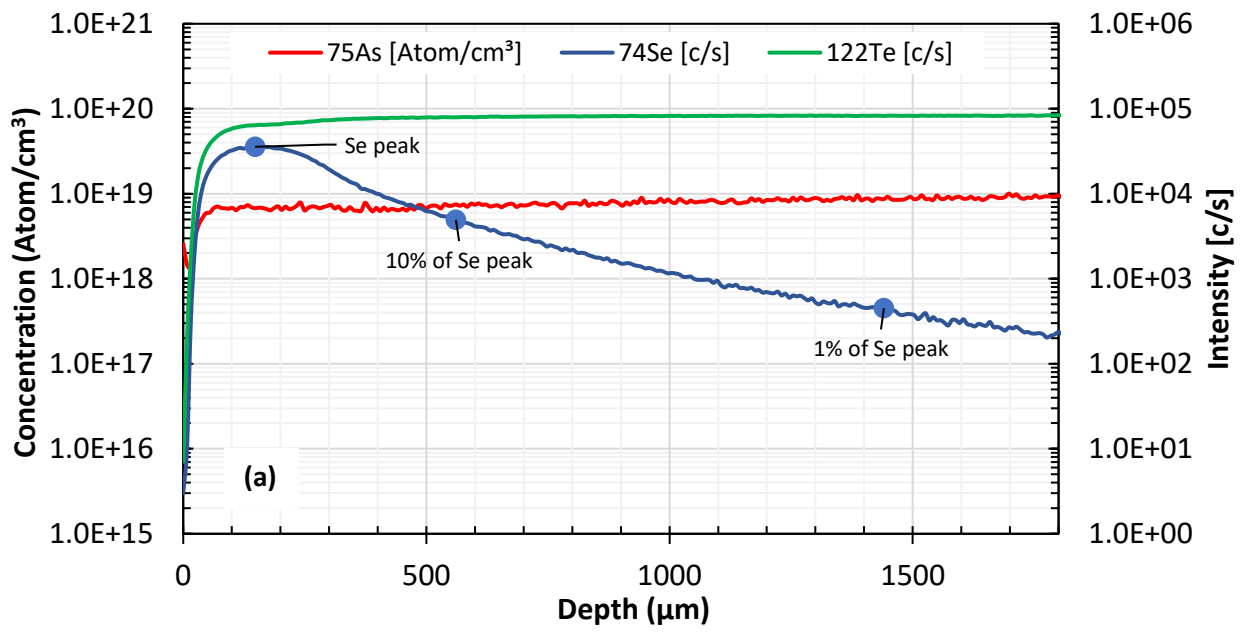


Figure 6: Box plot comparison of J-V parameters of FTO/SnO₂/CdSe/CdTe:As devices (8 cells per device) with varying thickness of CdSe.

As can be seen from the Se SIMS profile in Fig. 7a, there is a single Se peak but not a two-step Se profile, meaning CdSe is completely interdiffused into the CdTe absorber forming a Cd(Se,Te) ternary alloy. The Se diffusion length (Se_{DL}), defined here as the distance over which the Se signal drops to 1% of the peak value, is $\sim 1.5 \mu\text{m}$ from the front interface. In addition, the PL taken from the front interface in Fig. 7b did not show any signal around 1.73 eV but rather a single PL peak centred at 1.40 eV, indicating the CdSe layer is fully consumed following the CHT step, yielding a ternary alloy with estimated composition of $0.35 \leq x \leq 0.45$. When observed via STEM/EDX line profile, the peak composition for these samples appears to be just below $x = 0.2$ (Fig. 7c). These results suggest that the buried junction phenomenon observed in this device needs a different explanation than parasitic

absorption due to a remanent CdSe layer. The literature on undoped Cd(Se,Te) alloys show that CdSe and Se-rich Cd(Se,Te) ($x > 0.2$) compositions are naturally n-type, whereas Se-poor Cd(Se,Te) ($x < 0.2$) compositions are p-type [30, 31]. Using electron beam induced current (EBIC) imaging and selected area diffraction (SAD), Poplawsky *et al.* [28] showed that hexagonal Cd(Se,Te) compositions and CdSe are photo-inactive and hence do not contribute to PV activity. The composition for the cubic to hexagonal transformation of the Cd(Se,Te) layer in the FTO/SnO₂/CdSe/CdTe:As devices appears to exceed $x = 0.3$ (see Fig. 3a). However, the peak Se composition in post CHT devices remains below $x = 0.2$ (Fig. 7c) indicating cubic structure. Therefore, based on the STEM data, we can exclude both n-type or hexagonally structured Se rich ternary compositions to be the main cause of the buried junction/parasitic absorption. Further investigation is needed to root out the cause of parasitic absorption that scales with starting CdSe thickness in these devices.

Additionally, our SIMS data reveals that As diffuses back into the CdSe layer from the CdTe:As absorber, during device processing, which is believed to be promoted by the strong Se/Te interdiffusion (see Fig. 7a and Fig. S4). Because arsenic is a p-type dopant in II-VI compounds, we believe that the Cd(Se,Te) alloy formed at the front interface, following device fabrication, is p-type. The PL data also confirms the presence of arsenic within the Cd(Se,Te) layer: in-situ As doping in CdTe followed by chlorine activation treatment causes an infrared tail to emerge in its PL peak, usually with the strength of the tail scaling with the bulk acceptor concentration due to As doping [32, 33]. Band tailing due to arsenic incorporation in CdTe or Cd(Se,Te) confirms formation of defect level(s) near the valence band but it does not reveal how much of the incorporated arsenic is active (usually below 1% for polycrystalline CdTe). A similar effect can be seen here in the long wavelength response of the front interface region of the FTO/SnO₂/CdSe/CdTe:As device following chlorine treatment and the consequent As back-diffusion from CdTe:As layer to the newly-formed Cd(Se,Te) layer. In contrast, PL emission from the undoped CdSe layer for this device, as well as that of the Cd(Se,Te) ($x = 0.4$) reference layer, display narrow Gaussian-like profiles.



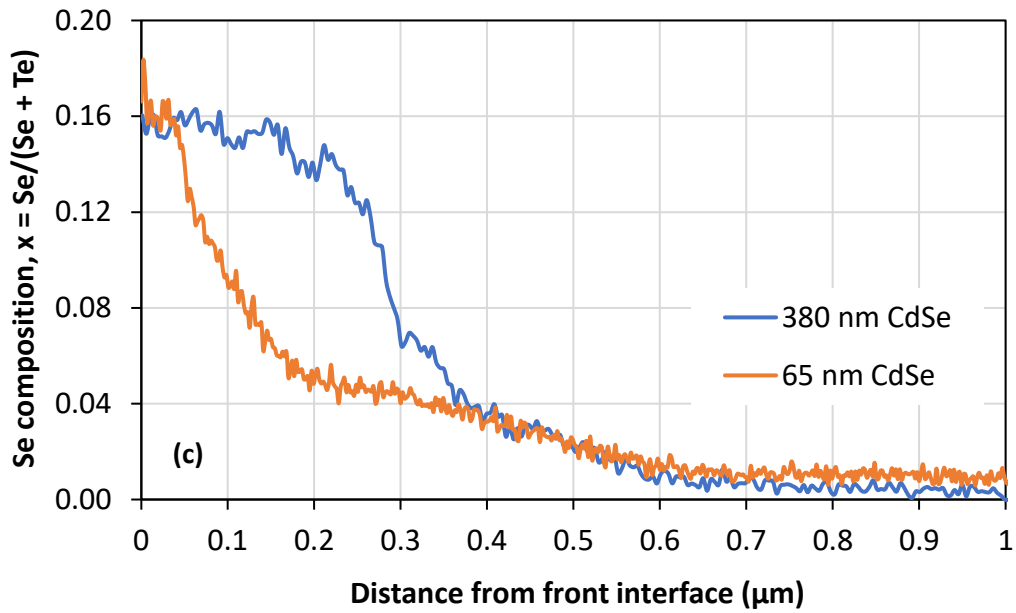


Figure 7: Se, As, and Te SIMS profiles (a) and front-interface PL spectrum (b) of a FTO/SnO₂/CdSe/CdTe:As device utilising 380 nm CdSe; PL spectrum of the 380 nm CdSe layer as well as reference films of as-deposited (undoped) CdTe, CHT arsenic doped CdTe, and an as-deposited (undoped) Cd(Se,Te) ($x = 0.4$, $x = 0.2$) alloy are also shown. (c) TEM/EDX Se line profile for devices utilising 65 and 380 nm CdSe.

Next, Se bilayers in the device structure FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As, with undoped- and As-incorporated Cd(Se,Te) layers were investigated. As incorporation was varied by adjusting As flow between 10, 20 and 30 sccm (corresponding to partial pressures of 2.88×10^{-5} , 5.76×10^{-5} and 8.59×10^{-5} bar, respectively) during fabrication. Fig. 8 compares the PL spectrum of a CdSe/CdSe_{0.2}Te_{0.8} film with 20 sccm As precursor flow before and after device incorporation. The spectrum of the Se bilayer shows two distinct PL bands at 1.70 and 1.40 eV, associated with CdSe and Cd(Se,Te) layers, respectively. Compared with the PL emission of a single CdSe layer peaking at 1.73 eV, a slight redshift by 30 meV can be seen, suggesting a slight intermixing occurring at the CdSe/Cd(Se,Te) interface during Cd(Se,Te) deposition onto the CdSe film. From the optical data (Fig. 4b) the presence of 3% Te inside the CdSe layer can be estimated. Following CdTe:As absorber deposition and device processing, only one PL peak at 1.40 eV can now be seen at the front interface. This clearly indicates that the bilayer CdSe/Cd(Se,Te) is converted to a single ternary alloy following intermixing due to CHT-driven Se/Te interdiffusion [5]. Similarly, a slight increase in the band tail can be seen in the front interface PL spectrum of the processed device in this work (compared to untreated bilayer), indicating incorporation of the As atoms in the now formed Cd(Se,Te) ternary alloy.

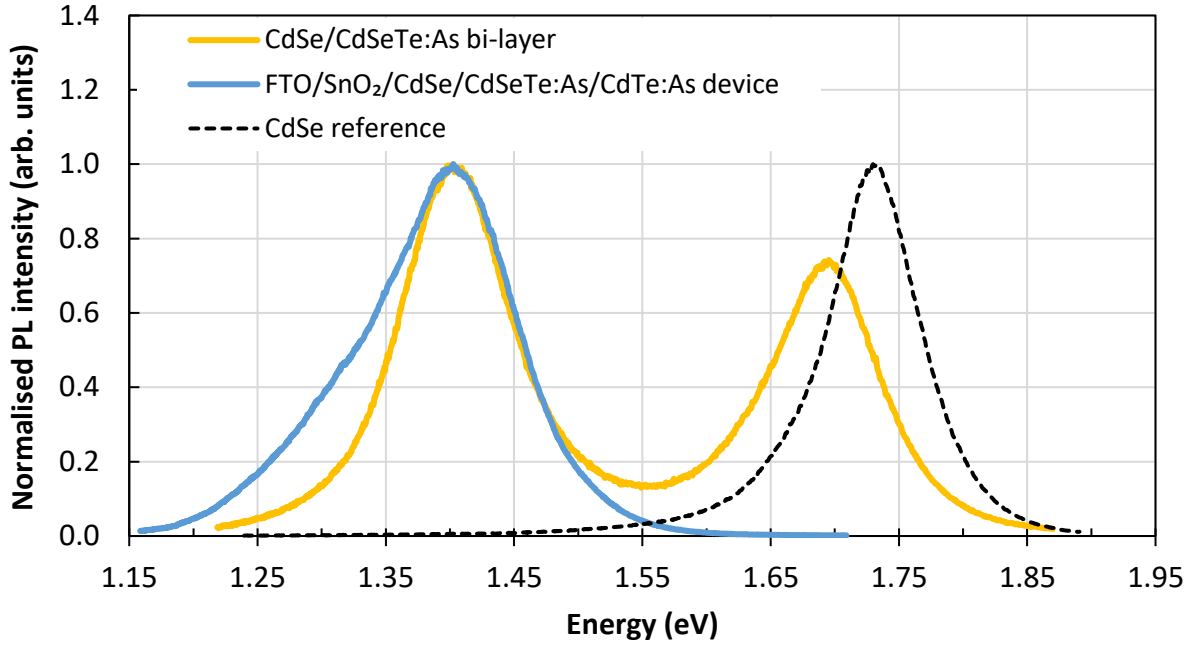


Figure 8: Front interface PL spectrum of a FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}:As/CdTe:As device in comparison to the PL spectrum of CdSe/CdSe_{0.2}Te_{0.8}:As bilayer and a reference CdSe film.

J-V curves and the EQE spectra for these devices are shown in Fig. 9, with cell performance parameters presented in Table S2. Devices with doped Cd(Se,Te) layers showed improvement in performance, due to enhancement in all PV parameters as depicted in Fig. 10. The best PCE of 8.1 % was measured in devices with Cd(Se,Te) doped using 20 sccm of As flow (5.76×10^{-5} bar partial pressure). J_{SC} is seen to slightly increase with As doping up to 28.3 mA/cm² at 20 sccm; however, it begins to drop with further As doping i.e., 30 sccm. This is consistent with the cells' spectral response, mostly in the 300 – 700 nm region, indicating a varying junction quality as a function of Cd(Se,Te) doping. This improves with 10 and 20 sccm doping levels, beyond which it is seen to slightly deteriorate (Fig. 9b). Although generally poor for all devices here, the FF also follows a similar trend to J_{SC} . The V_{OC} on the other hand increases linearly with in situ As doping of Cd(Se,Te) and is enhanced by as much as 89 mV compared to the undoped Cd(Se,Te) case.

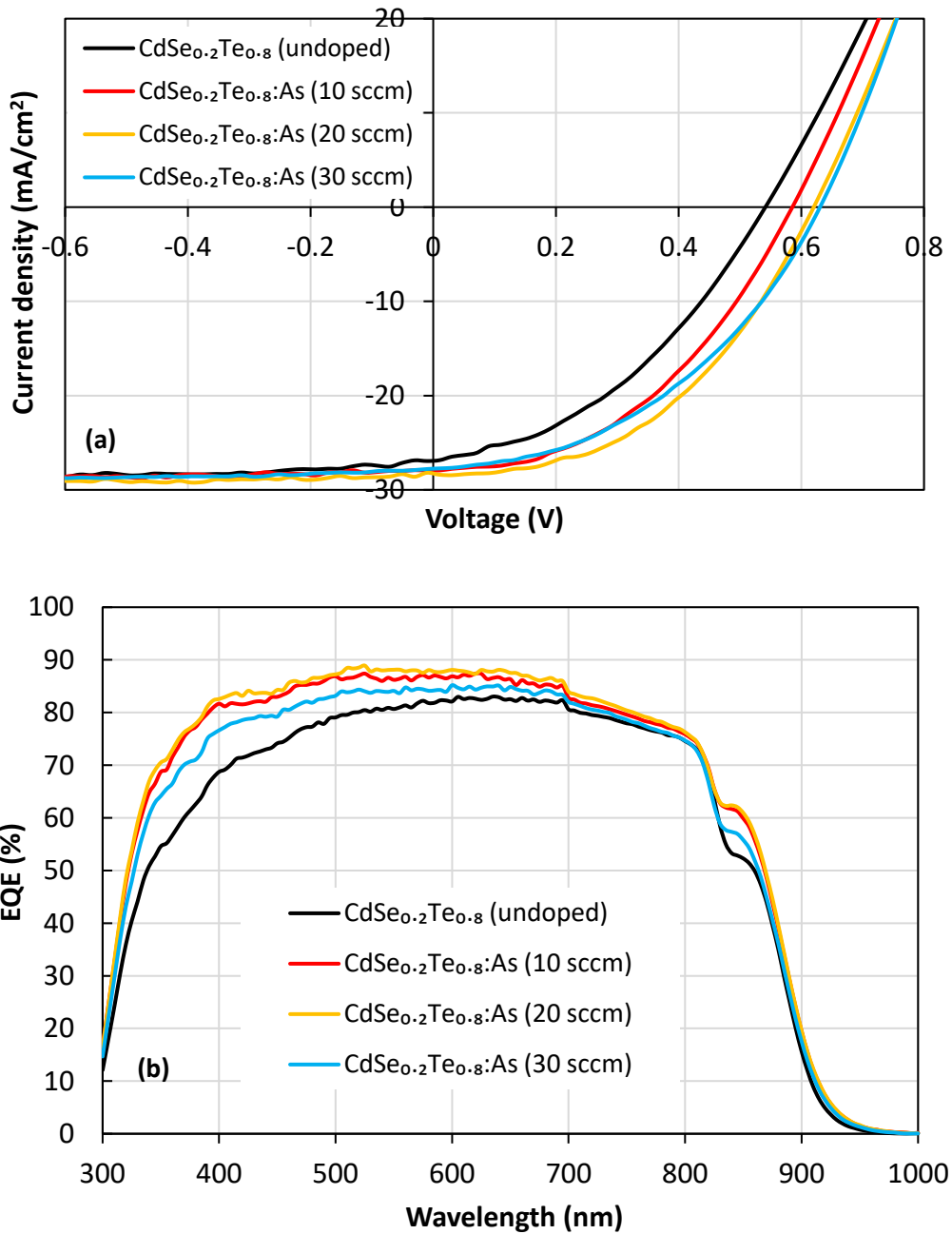


Figure 9: Light J-V curves (a) and EQE spectra (b) of FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As devices with undoped and As doped Cd(Se,Te).

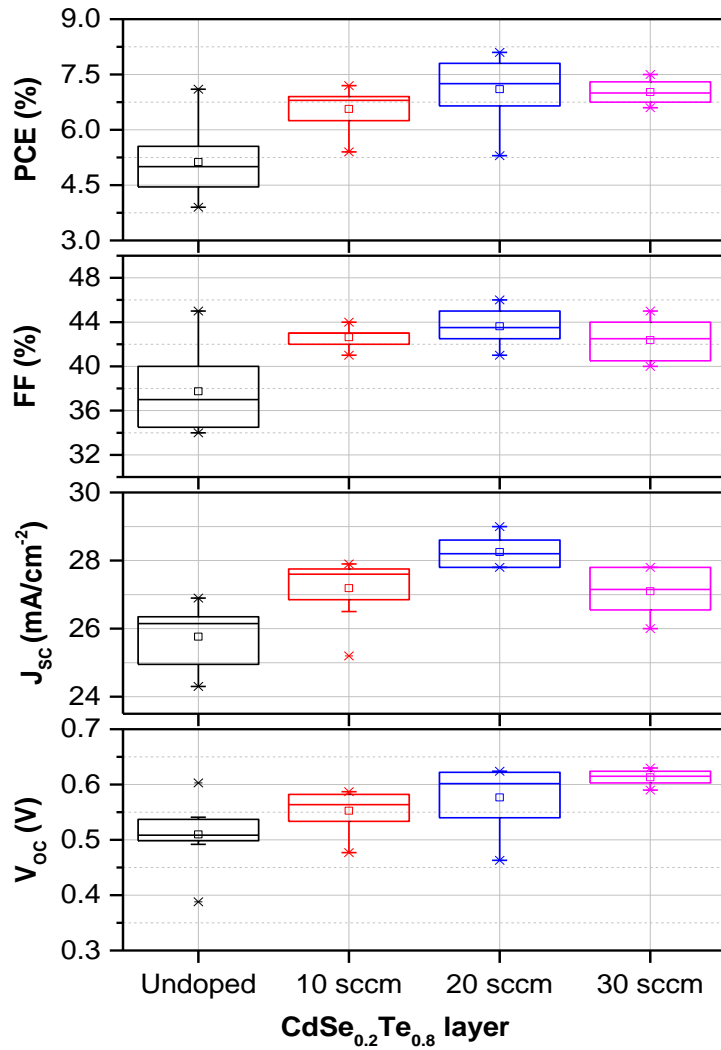


Figure 10: Box plot comparison of J-V parameters of FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As devices (8 cells per device) with undoped and As doped Cd(Se, Te).

The carrier density distribution in the FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As devices are compared in Fig. 11. Depletion width narrows with increased Cd(Se,Te) doping and average carrier density improves with respect to the undoped Cd(Se,Te), but becomes saturated beyond 10 sccm As flow.

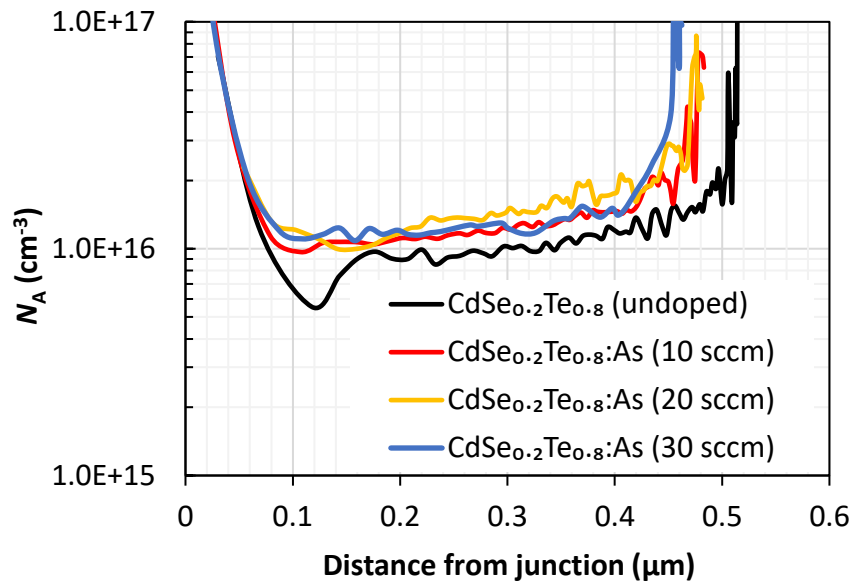


Figure 11: Carrier concentration (N_A) of FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As devices with undoped and As doped Cd(Se, Te).

A cross-sectional STEM image of a FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}:As/CdTe:As device with 10 sccm As incorporated Cd(Se,Te) along with the respective EDS elemental maps of Cd, Se, Te, Cl and O are shown in Fig. 12a. Small voids, mostly in the Cd(Se,Te) layer can be seen after CdTe:As absorber deposition and device processing, which were present in the as-deposited CdSe layers (Fig. 2 and Fig. S5). In some cases, these voids are seen to merge into larger ones (Fig. S6) deteriorating the interface quality with the substrate. EDS elemental maps show that there is a distinct segregation of Cl at the SnO₂/Cd(Se, Te) interface and at the absorber grain boundaries. This is typical of CdCl₂ heat treated CdTe solar cells [32, 34]. Further, high Se concentration can be seen at the SnO₂ side and diffused 0.8 – 1.0 μm into the CdTe:As absorber, beyond which it becomes undetectable by this method (Fig. 12b). In addition to high concentrations of Se within most grain interiors, there appears to be some Se segregated at the absorber grain boundaries. Comparing Se and Cl EDS maps, both elements appear to be concentrated in similar regions, which suggests co-passivation of grain boundaries by Cl and Se [3] and that the Se redistribution profile may be controlled via the CHT parameters. A similar observation was made by Colegrove and co-workers [5], whereby it is reported that effective Se diffusion aligns well with Cl diffusion coefficients. From this result, they suggested that other lattice elements, such as Group V dopants (Sb, As, P), can also go through similar mass transport to Se, facilitated by the Cl diffusion.

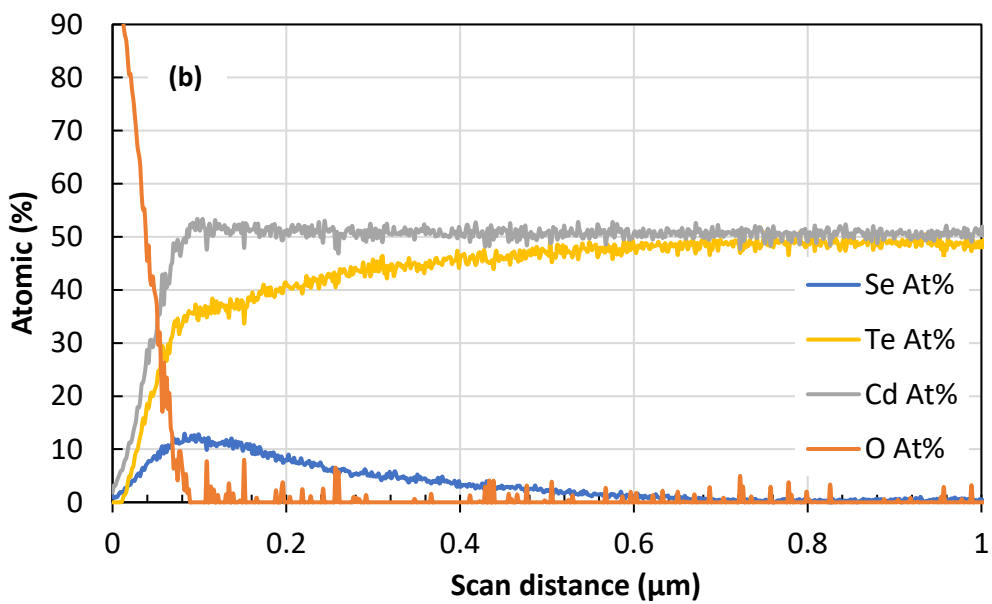
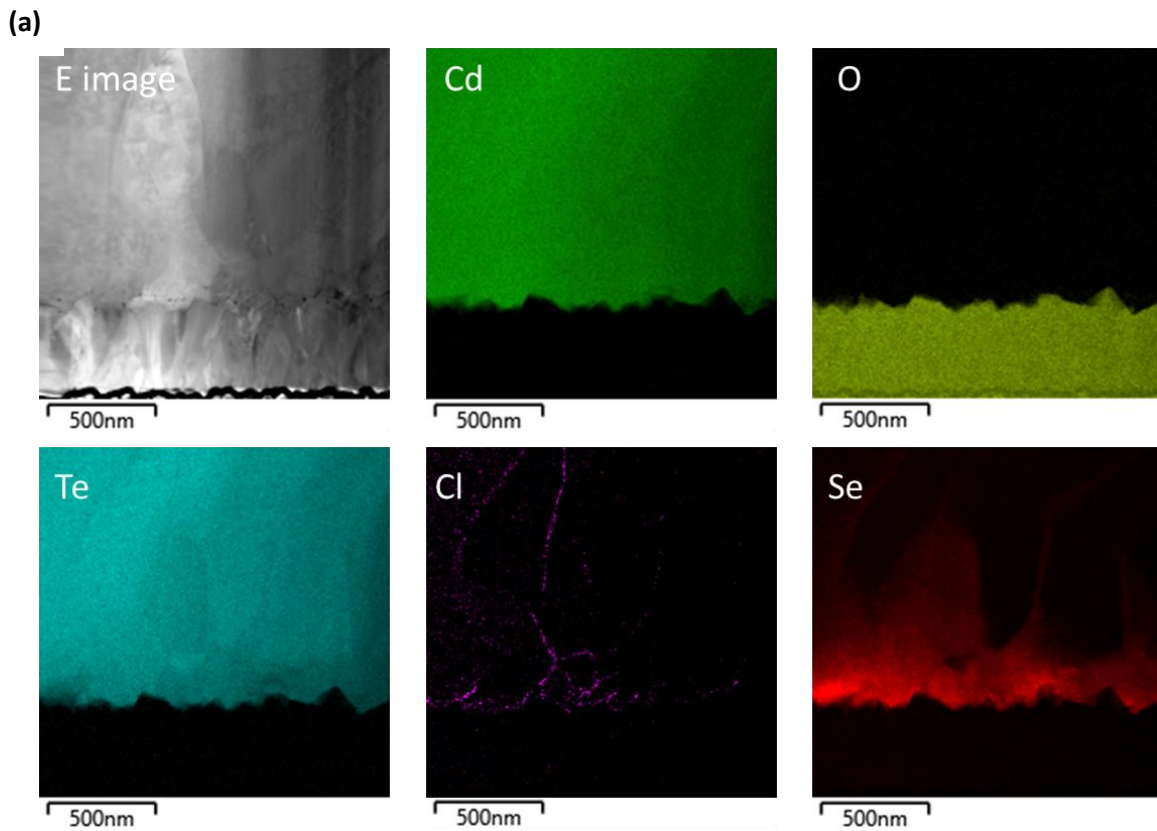
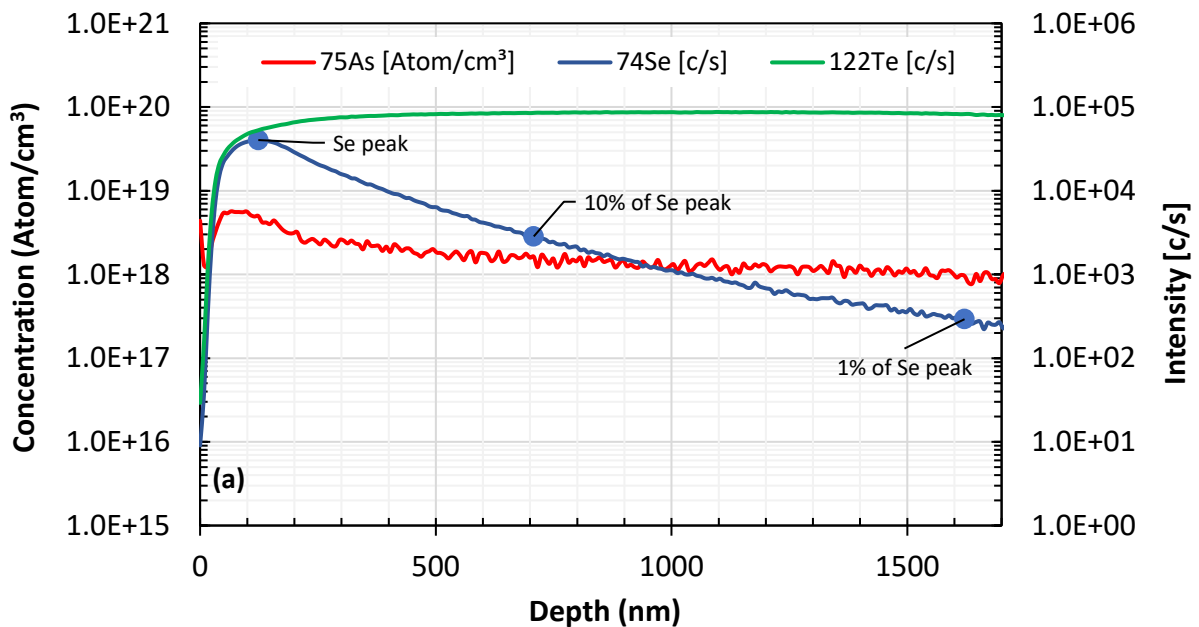


Figure 12: Cross section STEM images with EDS maps for Cd, O, Te, Cl and Se (a) and cross sectional EDS line scans for Se, Te, Cd, and O (b) in a FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}:As/CdTe:As device.

Fig. 13a gives the SIMS depth profiles for Se, As, and Te of the FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As device with 20 sccm As-doped Cd(Se,Te), measured after peeling off the whole device stack from the FTO/SnO₂ substrate, exhibiting ~ 1.6 μm Se diffusion length. As signal seemingly rises at the front interface for both materials, suggesting a clear back-diffusion of As from the CdTe:As absorber. While

it is unclear from this data whether this spike is due to a genuine build up of As at the front interface, since the As signal can only be quantified within the CdTe matrix, it does agree with previous observation of Group V dopant diffusion within Cd(Se,Te)/CdTe devices [35, 36], and verifies the prediction made by Colegrove and co-workers [5]. The Se profile in the FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As device with 10 sccm As-doped Cd(Se,Te) measured by STEM is compared to that of CdSe-only devices with 65 and 380 nm CdSe in Fig. 13b. It is clear that the Se peak near the front interface is significantly higher for device utilising a CdSe/Cd(Se,Te) bilayer. We suggest that only the width of the Se profile can be controlled by CdSe thickness, whereas the height can be controlled using the bilayer approach.



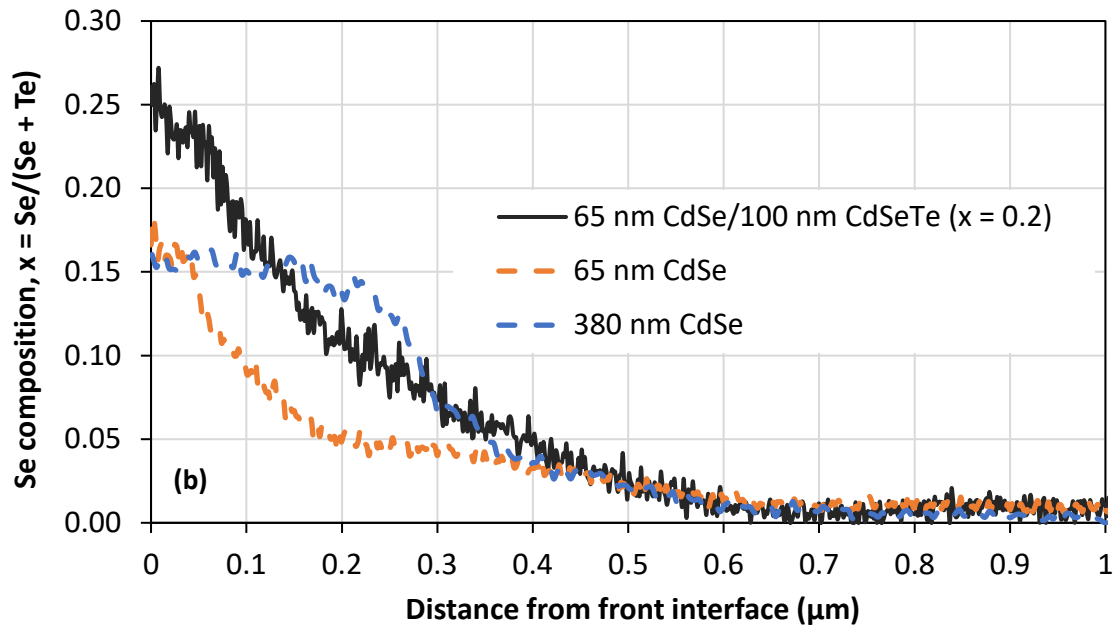


Figure 13: (a) SIMS depth profiles for Se, As, and Te of the FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As device with 20 sccm As-doped Cd(Se, Te). (b) The STEM/EDX Se line profile for the FTO/SnO₂/CdSe/CdSe_{0.2}Te_{0.8}/CdTe:As device with 10 sccm As-doped Cd(Se,Te), compared to devices utilising single CdSe layers of 65 and 380 nm.

Conclusions

Controlled deposition of Cd(Se,Te) thin films ($0 \leq x \leq 1$) with linear compositional control using a chamber-less inline AP-MOCVD technique has been demonstrated in this work. Films exhibited a phase transition from cubic to wurtzite for Se (x) alloying $x > 0.3$. Various thicknesses of CdSe layers were incorporated in the front of CdTe solar cells. SIMS and PL measurements showed that CdSe layers (up to 380 nm thickness investigated) were completely converted to graded Cd(Se,Te) alloys in processed devices, due to chlorine treatment driven Se/Te interdiffusion. STEM data showed that the width of the Se profile scaled with initial CdSe thickness, but not the height of it, which was limited to $x \leq 0.2$. This demonstrates that CdSe is not forming an n-type emitter layer in these devices. Additionally, arsenic back-diffusion from the CdTe absorber into the Cd(Se,Te) region was catalysed by this strong Se/Te interdiffusion. Device performance improved with reducing CdSe thickness, whereby 380 nm thick CdSe layer presented a buried junction effect, which requires further study. Alternatively, the effect of having an additional alloy film (100 nm CdSe_{0.2}Te_{0.8}), on top of a thin (65 nm) CdSe base layer, was also studied. This bilayer structure also led to graded Cd(Se,Te) alloy formation in finished devices with As back diffusion occurring toward the substrate interface. In-situ doping of the Cd(Se,Te) ternary layer was found to be crucial to device junction quality and V_{oc} . The device performances reported here are lower than state-of-the-art CdTe and Cd(Se,Te) absorbers,

which is attributed to the poor electronic quality of the emitter/absorber interface. In addition to having the ability to control the width of the Se profile via starting CdSe layer thickness, the peak height could be controlled using a CdSe/Cd(Se,Te) bilayer. Thus, this work provides unique insight into controlling the Se profile as well as in-situ and ex-situ (i.e., back diffusion) arsenic doping. The PV performance may be improved further by adjusting the Se redistribution profile and, more importantly, emitter material properties and emitter/absorber junction. To this end, further studies are needed on the effect of device processing parameters and characterisation of emitter properties, particularly the donor density and work function, and its band alignment to the Cd(Se,Te) layer.

Acknowledgements

The authors would like to acknowledge the European Regional Development Fund (ERDF) and the Welsh European Funding Office (WEFO) for funding the 2nd Solar Photovoltaic Academic Research Consortium (SPARC II). Authors would also like to thank Alison Chew at LSA Ltd for valuable discussions on SIMS measurements and data. C. L. Perkins is thanked for guidance and useful discussions on the device lift-off processing and critical reading of the manuscript. H.K.H. Lee and W.C. Tsoi would like to acknowledge the support given to the SPECIFIC Innovation and Knowledge Centre by the Engineering and Physical Science Research Council (EP/N020863/1); Innovate UK (920036) and by the European Regional Development Fund (c80892) through the Welsh Government. This work was authored in part by the National Renewable Energy Laboratory, operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by the U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office under contract number 34353 and the U.S. Department of Defence Office of Naval Research under contract number IAG-16-02002. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

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