Enhancing reliability of energy absorbers in DC circuit breakers

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Abstract — **Because of high energy absorption requirements, the energy absorbers in DC circuit breakers will consist of a large number of series- and parallel-connected surge arrester units. This study shows that owing to highly nonlinear I-V characteristic of surge arresters, the failure of a single arrester has a significant impact on the performance of the whole energy absorber. In particular, the arrester column containing the failed unit will draw considerably higher current compared to healthy columns which may lead to cascaded failure of arresters and destruction of the whole column. This paper evaluates and proposes new connection topologies for enhancing the robustness and reliability of energy absorbers in high-voltage DC circuit breakers. A matrix structure is proposed as the topology for the greatest reliability. The impact of the number of breaker modules is also investigated.**

Index Terms— **Energy absorber, DC circuit breaker, surge arrester, component failure, DC grid protection**

I. INTRODUCTION

DC circuit breaker (DCCB) is recognized as a key component for realization of multiterminal DC transmission systems [1][2]. Its main role is protecting converters and cables against fast-rising DC fault currents which require fault clearing times one to two orders of magnitude shorter than in conventional AC systems. Several full-scale DCCBs are already in operation in China [2] while full-scale prototypes have been independently tested in Europe [3], [4].

While numerous DCCB topologies are available [1], all topologies will have the residual current breaker (RCB), di/dt limiting inductor and the energy absorber (EA). The EA is a critical component which absorbs the fault energy, provide counter-voltage and force DC current suppression. Because of high energy absorption requirements [1], the EA will consist of a large number of individual surge arrester (SA) units.

The failure of a single or multiple SA units within the EA is feasible because of a number of operating or manufacturing reasons. A recent study [5] indicates the DCCB energy absorber of 72 arresters can have over 30% difference in current stress between individual arresters. Arrester aging can further exacerbate this problem as the arrester's I-V characteristic changes over time [5]. This paper investigates the performance EAs under failure of individual arresters and assesses the reliability and robustness of various EA topologies. A new topology will be proposed for improved absorber robustness.

II. IMPACT OF UNIT FAILURE IN ENERGY ABSORBERS

It is well recognized that DCCBs for application in high-voltage (HV) DC transmission grids will adopt a modular structure [1]-[3]. Several modules of around 70-80 kV will be connected in series to achieve the desired voltage rating

[1]. A single breaking module, shown in Fig. 1, will consists of a current-breaking element S_{MB} in parallel with an energy absorber. There are many ways in which S_{MB} can be implemented, but the main two types are a self-commutating semiconductor switch or an AC circuit breaker (ACCB) in parallel with an oscillating LC circuit [2].
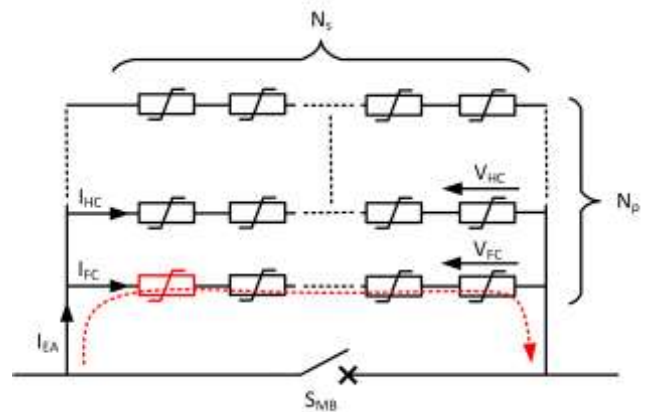

Fig. 1. Generic structure of a DCCB module

The EA will in the general case be implemented as a surge arrester (SA) bank with N_p parallel-connected columns, each column consisting of N_s series-connected individual SA units. It is assumed that surge arresters will normally fail in low-resistance state [6]. Therefore, if one unit fails, the voltage of the corresponding column reduces, and the column I-V curve shifts as if it has lower rated voltage. Because of low-slope I-V characteristic of SAs, even a small difference in the column's voltage can have a colossal difference in the current through that column.

Fig. 2 compares two typical SA's I-V characteristics with one characteristic corresponding to 100% of the rated voltage U_r and the other one corresponding to 90% of U_r. If the two arresters are connected in parallel and the voltage of 1.8 p.u. is applied across them, the arrester with the 100% U_r rating will draw 35 A while the arrester with the 90% rating will draw 2000 A, a difference of 5700%. This leads to the conclusion that failure of a single unit means that the corresponding column will draw majority of the EA current. For the example illustrated in Fig. 1, this can be written as

$$I_{HC} \ll I_{FC} \approx I_{EA} \qquad (1)$$

I_{HC} labels the current in the healthy column while I_{FC} labels the current in the column with a single unit failure. From (1), it is evident that a single-unit failure may lead to overloading of the healthy arresters in the same column. Therefore there is possibility for a cascaded failure in which case the whole column becomes damaged and the breaker module short-circuited. The absorber cascaded failure has

been demonstrated experimentally for a small 2x2 topology on a lab-scale kJ-size absorber in [7]. In a DCCB with several breaking modules, this will reduce the transient interruption voltage (TIV) [1] and lead to an increased fault current suppression time and energy absorption of the remaining healthy modules. Then, component overload may cause further EA failures and potentially a complete DCCB failure which would have severe implications for the remainder of the DC grid.
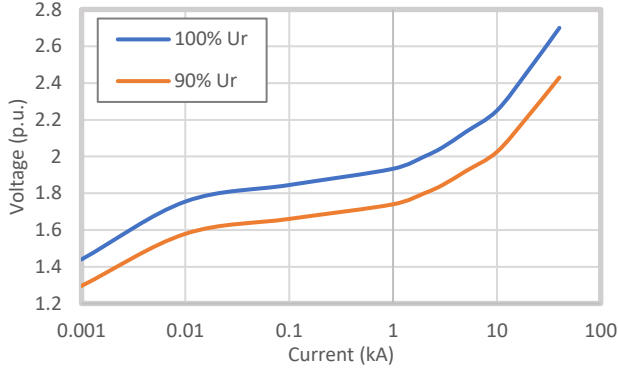

Fig. 2. SA's I-V characteristic at normal and reduced voltage rating

III. Test System Description

A. EA design

We consider the design of EA in a test DCCB with parameters outlined in Table I. The grid overvoltage coefficient K_{OV} is taken as 5%, which is the ratio between the maximum permissible DC voltage under normal grid operating conditions and the nominal DC voltage level [8]. The peak TIV coefficient K_{TIV} is the ratio between the maximum DCCB voltage during the current interruption process and the nominal grid voltage, measured at the DCCB's rated breaking current I_{pk}.

TABLE I.   INPUT PARAMETERS FOR THE EA DESIGN

Parameter	Symbol	Value
Nominal DC voltage	V_{dcN}	320 kV
Peak DCCB current	I_{pk}	16 kA
Series DCCB inductance	L_{dc}	100 mH
Grid overvoltage coefficient	K_{OV}	1.05
Peak TIV coefficient	K_{TIV}	1.5
Number of breaker modules	N_m	4

The goal of the EA design process is determining the rated SA voltage U_r and the number of parallel branches N_p which yields the desired TIV and prevent thermal overload of the arresters. The arresters are considered overloaded if they absorb more charge during a single breaking operation than their repetitive charge transfer rating Q_{rs} allows. The problem can also be defined in terms of absorbed arrester energy but using the charge is more convenient as it is independent of the DCCB voltage rating and N_s. Moreover, Q_{rs} is a constant parameter for all the SAs within the same product series while the SA energy rating changes with U_r[9]. From Fig. 1, the absorbed SA charge is defined as

$$Q_j = \int_0^{T_s} I_j \, dt \qquad (2)$$

where j denotes the subscript of the branch or bank current, in this case FC, HC or EA. The main breaker

opening occurs at $t = 0$ while T_s marks the ending of the fault current suppression period (when the residual current level is reached).

The EA design is an iterative process since any change in N_p changes the non-linear voltage characteristic of the arrester bank. The initial design parameters can be determined with reasonable accuracy using the following procedure. The rated TIV of the whole DCCB is

$$V_{pk} = K_{TIV} \cdot V_{dcN} \qquad (3)$$

Assuming firm DC bus voltage and flat EA voltage characteristic during the fault current suppression period, the L_{dc} current slope can be approximated as

$$\frac{dI_{dc}}{dt} = \frac{V_{dcN} \cdot (K_{OV} - K_{TIV})}{L_{dc}} \qquad (4)$$

The time to current zero from I_{pk} is obtained as

$$T_0 = \frac{I_{pk} \cdot L_{dc}}{V_{dcN} \cdot (K_{TIV} - K_{OV})} \qquad (5)$$

The charge absorbed in the EA between the main breaker opening ($t = 0$) and the current zero can be approximated as

$$Q_{pk} = \frac{I_{pk} T_0}{2} = \frac{I_{pk}^2 \cdot L_{dc}}{2V_{dcN} \cdot (K_{TIV} - K_{OV})} \qquad (6)$$

For the given input parameters, Q_{pk} is calculated as 89 C. The rated TIV of a single breaker module is

$$V_{pkm} = \frac{K_{TIV} \cdot V_{dcN}}{N_m} \qquad (7)$$

where N_m is the number of breaker modules. An arrester unit capable of providing V_{pkm} at I_{pk} is selected as PEXLIM P-Z with U_r of 54 kV [9][10]. The rated charge of this arrester is Q_{rs}=3.2 C while the I-V characteristic is shown in Fig. 2 (100% U_r). Applying a 50% margin to account for the uneven current distribution in the arrester bank and additional inductances in a DC system (MMC's arm inductors, cable inductances etc.), the required number of parallel-connected arrester columns is calculated as

$$N_p = \frac{1.5 \cdot Q_{pk}}{Q_{rs}} \qquad (8)$$

and yields $N_p = 42$ for the given input parameters. The values of $U_r = 54\ kV$ and $N_p = 42$ are used as the starting point for the parameter optimization. The final EA design is obtained through iterative PSCAD simulations, with the final parameters shown in Table II. It is worth noting that Q_{rs} is identical for the whole arrester column as for an individual arrester unit, and that Q_{rst} is identical for the whole DCCB as for a single breaking module.

TABLE II.   FINAL EA PARAMETERS FOR A SINGLE DCCB MODULE

Parameter	Symbol	Value
Rated column voltage (per module)	U_r	66 kV
Number of parallel columns	N_p	40
Repetitive charge transfer rating (per column)	Q_{rs}	3.2 C
Repetitive charge transfer rating (total)	Q_{rst}	128 C

B. Test system model in PSCAD

A test system shown in Fig. 3 is developed in PSCAD. The system consists of a constant DC voltage source with a series inductor L_{dc}. These components represent a strong DC bus with the added DCCB and line inductances. The equipment under test consists of four series-connected DCCB $N_m=4$, modules which are simultaneously operated when the line current exceeds a predefined threshold I_{th}. Since the other end of the DCCB is solidly grounded, the current in the test system rises at a constant slope of V_{dc}/L_{dc}. $S_1 - S_4$ are ideal switches and opening them instantaneously commutates the current into the EAs. Each SA bank consists of $N_s \times N_p$ individual SAs, as shown in Fig. 1.
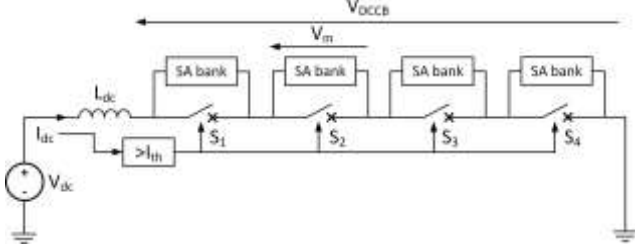

Fig. 3. Test system for EA characterization

C. EA design verification

To verify the EA design, four breaker modules with EA parameters from Table III are subject to a breaking with $V_{dc} = 336kV$ (1.05 p.u.) while $I_{th} = I_{pk} = 16$ kA. Table III compares the extracted performance indicators, given for the whole DCCB as well as a single module. Except for the peak TIV, the values of the remaining indicators are taken at the instance where dI_{dc}/dt becomes equal to -1 A/ms, signaling the end of the fault current suppression period. The peak TIV of the breaker is reasonably close to the 1.5 p.u. target while the absorbed charge per column, factoring in a 50% margin, is less than Q_{rs}.

TABLE III. MAIN CHARACTERISTICS OF TEST ENERGY ABSORBER

Performance indicator	Whole DCCB	Single module
Peak TIV	494.44 kV (1.55 p.u.)	123.6 kV (0.39 p.u.)
Absorbed charge per column	2.08 C	2.08 C
Absorbed charge per column (with 50% margin)	3.12 C	3.12 C
Total absorbed charge	83.17 C	83.17 C
Total absorbed energy	40.66 MJ	10.2 MJ
Fault current suppression time	11 ms	11 ms
Residual current level	35.4 A	35.4 A

IV. ENHANCING ENERGY ABSORBER RELIABILITY

A. Increasing the number of series-connected units

It is assumed that a SA unit fails in an ideal short circuit [6][7]. The relationship between the voltage of a single SA in the healthy column (V_{HC}) and the voltage of a single SA in the partially-failed column (V_{FC}) is given as

$$V_{FC} = \frac{N_s}{N_s - 1} \cdot V_{HC}, \quad N_s \geq 2 \qquad (9)$$

It is seen that the voltage on a single healthy unit in the failed column increases because the number of units sharing the voltage decreases. This in turn causes the failed column to draw much higher current and may cause cascaded unit failure. From (9) it is evident that the difference between V_{FC} and V_{HC} decreases with N_s. Therefore, increasing the number of series-connected units leads to a more uniform current distribution within the EA module and alleviates this issue.

Fig. 4 demonstrates the impact of a single-unit failure on the currents of the faulted column (I_{FC}), a healthy column in the faulted module (I_{HC}) and a column in a healthy module (I_{HM}). The column voltages, absorbed charge and energy are also shown. The abbreviations used in labeling of these variables are: FC – failed column, HC – healthy column and HM – column in a healthy module. The results are compared against the base case with no SA failures, while $N_s = 5$.

In comparison with the variables for the healthy columns, current, charge and energy of the units in the failed column are two orders of magnitude higher and hence cannot be properly shown on the same graph. The peak values of these variables in the observed time period are 11.57 kA, 2.11 MJ and 72.66 C, respectively. The discrepancy between I_{th} and peak I_{FC} arises because a small resistor (1.25 mΩ) is connected in series with each arrester column to suppress the PSCAD short-circuit check error. Consequently, the current distribution at the very beginning of the fault current suppression period may not be accurately represented.
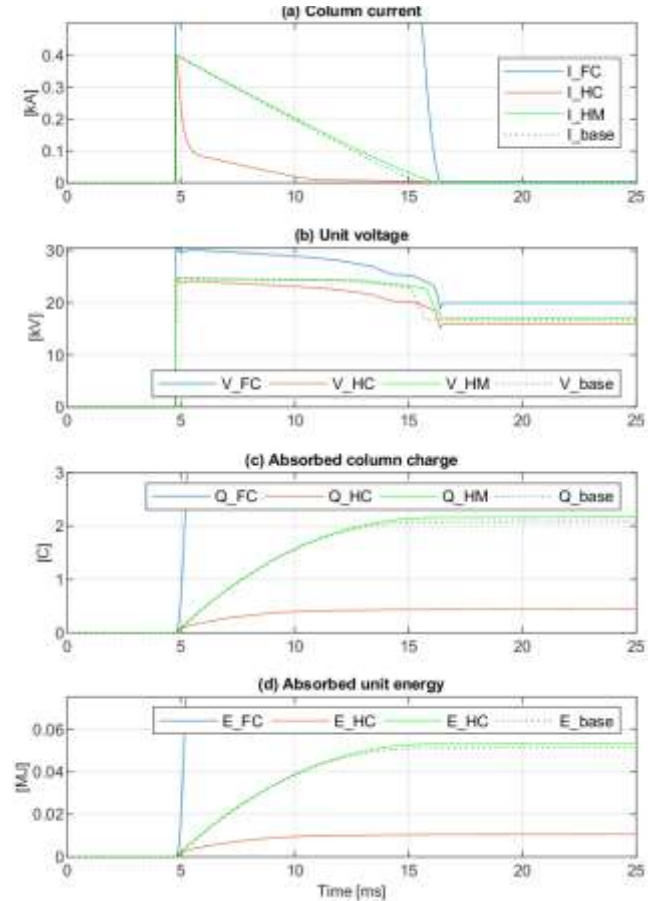

Fig. 4. Time-domain responses for a single SA unit failure (Ns=5).

Fig. 5 shows the relationship between the absorbed charge per column and the number of series-connected units. Only a single unit failure is simulated, however, the figure also encompasses the cases of multi-unit failures. The numbers in brackets below N_s indicate the percentages of failed units in a column. A case of $N_s = 5$, for example, illustrates a 20% column failure and is equivalent to a two-unit failure at $N_s = 10$ or a four-unit failure at $N_s = 20$. A

comparison is made between the base case with no failures (Q_{base}), as well as the repetitive charge transfer rating (Q_{rs}).
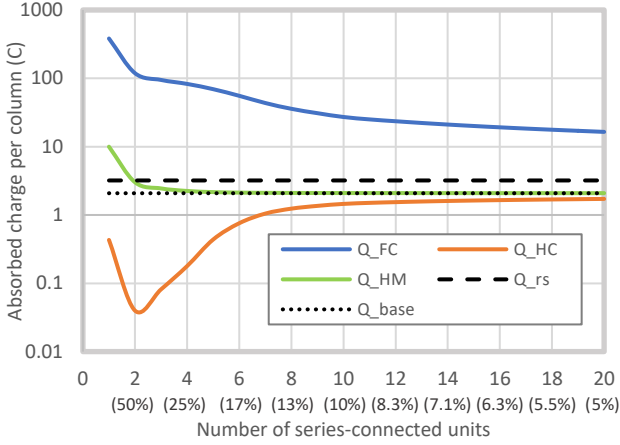

Fig. 5. Absorbed charge per column in case of a single unit failure

Even with a high N_s, Q_{FC} is several times higher than both Q_{base} and Q_{rs}. This implies that a cascaded failure is probable in a real module. Considering the SA thermal constants, it is very likely that one or more units would fail in one opening, but perhaps not the whole column. However, the failure of each additional unit would increase the proportion of EA current flowing through that column and exacerbate the overloading of healthy units, increasing the probability of a complete column failure.

In order to prevent the cascaded failure of arrester units in a failed column ($Q_{FC} < Q_{rs}$), a series connection of at least 135 units is required. It is highly unlikely that such a design would be feasible in practice because of limited voltage rating (commonly around 6kV) for commercial SA units [5]. It can be concluded that by merely increasing N_s, it would be difficult to enhance the reliability of EAs.

B. Increasing the number of modules

The above study indicates that the failure of one unit would likely lead to a failure of an entire column, and this implies the failure of one module. Fig. 5 shows that, in the case of a complete module failure (case of $N_s = 1$), the charge on a column in another healthy module reaches $Q_{HM} = 10\ C = 3.125\ Q_{rs}$, i.e. more than three times the rated charge. Therefore, the failure of an arrester column, caused by the failure of a single arrester unit, would possibly lead to the failure of the remaining three healthy modules.

Further investigation has revealed that $Q_{HM}(N_s = 1) < Q_{rs}$ when $I_{th} < 8.45\ kA$. Therefore, the DCCB could in theory absorb the fault energy using only three modules without overloading them if it opens under the current of less than 8.45 kA. However, the residual current level when only three modules are inserted is 334 A (compared to the rated 35.4 A) which implies that the RCB would not be able to open and the arresters would eventually overload, unless the backup protection in the DC grid acts and isolates the fault.

A potential remedy to this problem is increasing the number of breaker modules. The higher the number of modules, the smaller the peak TIV reduction that occurs in case one module fails. The relationship between the peak TIV of a healthy breaker ($V_{pk}(N_m)$) and the one with a single module failure ($V_{pk}(N_m - 1)$) is

$$V_{pk}(N_m - 1) = \frac{N_m - 1}{N_m} \cdot V_{pk}(N_m) \qquad (10)$$

It is evident that increasing N_m reduces the difference between the healthy and the partially failed DCCB.

The test of a single column failure from Fig. 5 is repeated using five modules while the voltage rating of each module is scaled by 0.8 to provide the same cumulative TIV. A comparison between the main performance indicators for a four- and five-module DCCB under a single module failure is given in Table IV. The base case from Table III is also provided for the reference.

TABLE IV. EA PERFORMANCE INDICATORS UNDER A SINGLE MODULE
FAILURE DEPENDING ON THE NUMBER OF MODULES

Performance indicator	4 modules	5 modules	No failure
Peak TIV	371.93 kV (1.16 p.u.)	396.63 kV (1.24 p.u.)	494.44 kV (1.55 p.u.)
Absorbed charge per column	9.99 C	5.65 C	2.08 C
Total absorbed charge	399.47 C	226.16 C	83.17 C
Total absorbed energy	147 MJ	88.79 MJ	40.66 MJ
Fault current suppression time	58.7 ms	32.7 ms	11 ms
Residual current level	334 A	213 A	35.4 A

Increasing the number of modules from four to five increases the peak TIV in case of a single module failure by 0.075 p.u. Although the difference is seemingly low, it results in a considerable reduction in the absorbed charge, energy, fault current suppression time and residual current level. While all measurements indicate that a five-module breaker would still be overloaded, there is substantial reduction in the module stress. Because the cost of a single module is highly dependent on the voltage rating, increasing N_m is not likely to produce significant cost penalties if the voltage rating of each module is proportionally reduced. Nevertheless, utilizing high N_m may exacerbate the challenges of voltage balancing during simultaneous module opening. In order to ensure that Q_{rs} is not exceeded, $N_m \geq 9$ would be required.

C. Energy absorber with parallel interconnectors

The problem of highly uneven current distribution in SA banks under a single unit failure can be tackled by employing parallel interconnectors between columns, as shown in Fig. 6. It is proposed that the interconnectors are inserted between every row of SA units, resulting in full meshing of the arrester bank. When a single SA unit fails, the circuit ensures that the corresponding row is bypassed. Since an equal number of healthy arresters remains inserted in the current path in each column, $V_{FC} = V_{HC} = V_{HM}$, now there is no discrepancy between column currents. Consequently, $Q_{FC} = Q_{HC} = Q_{HM}$, except for the bypassed row where the failed unit conducts majority of the current.
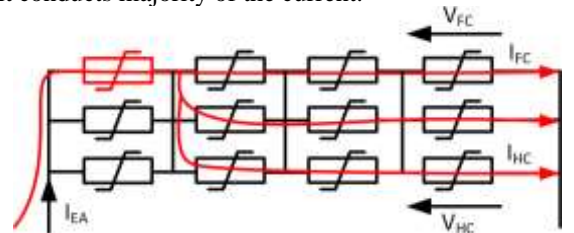

Fig. 6. Surge arrester bank with parallel interconnectors

The time-domain response for a single-unit failure with $N_s = 5$ in a SA bank with interconnectors is shown in Fig.

7. As expected, there is no difference between the voltages of healthy arresters in the failed and healthy column. No further overload occurs and cascaded failure is unlikely.
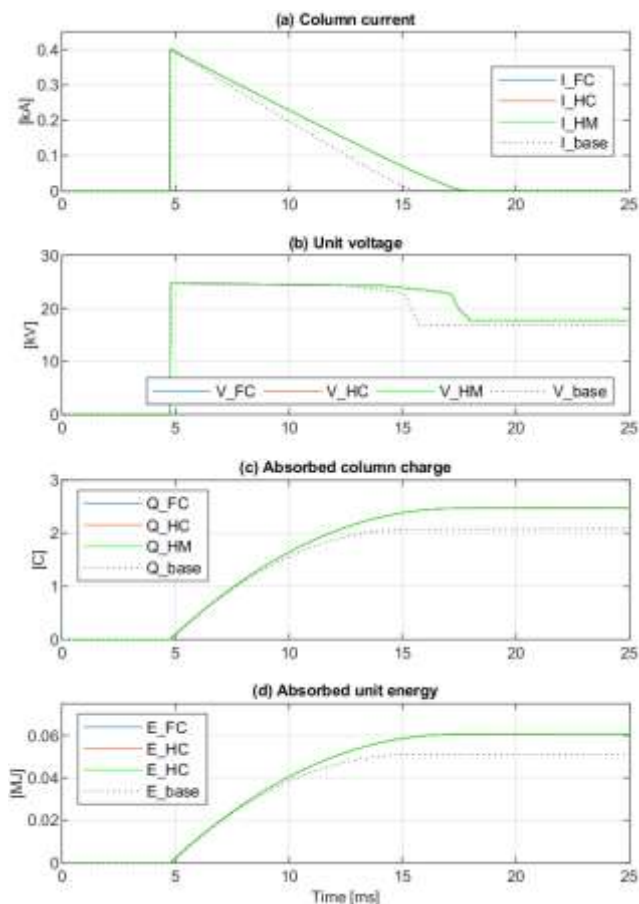

Fig. 7. Time-domain responses for a single SA unit failure with in a SA bank with interconnectors, (N_s=5).

Fig. 8 illustrates the impact of increasing N_s on the absorbed column charge when the interconnectors are used. For $N_s \geq 3$, $Q_{FC} < Q_{rs}$ which means that a cascaded failure will not occur if the number of series-connected units is 3 or more. As the N_s grows larger, the diminishing returns are evident. For $N_s \geq 9$, the difference between Q_{FC} and Q_{base} is less than 10% and further increase in N_s has no value.
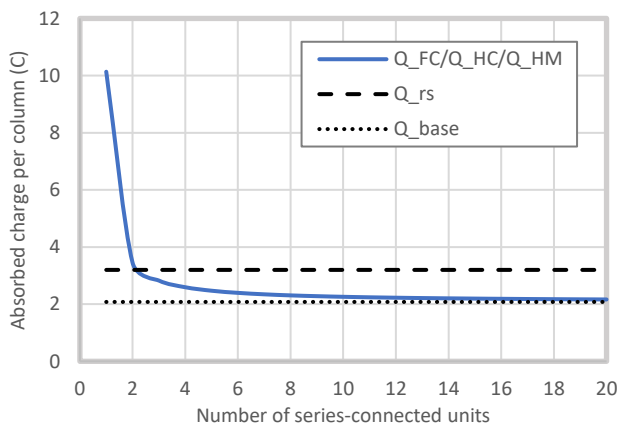

Fig. 8 Absorbed charge per column in case of a single unit failure in a SA bank with interconnectors

The potential downside of utilizing the meshed layout of SA banks is that such design pronounces the differences in individual arrester I-V characteristics and promotes a more uneven current distribution. The imperfections in individual SA units cancel each other out in topologies with long columns. In a fully meshed configuration, higher current always flows through the arrester unit with the lower voltage rating which could hasten the failure of these units. Nevertheless, this is not a major drawback of the meshed EA topology since N_s will in most cases be very low.

Another challenge is the mechanical design of meshed interconnectors which should have low inductance. However, the added cost and weight compared to conventional EA design should be minimal.

V. CONCLUSION

The conventional column-based topology of EA is very vulnerable to single-unit failures. The partially-failed column draws the majority of EA current which is likely to cause cascaded arrester failures in that column. This problem could be solved by utilizing a fully-meshed EA topology where each row of individual SA units is connected in parallel. Alternatively, the number of breaker modules can be increased for a similar effect, but this might cause voltage-sharing issues with mechanical DCCBs.

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