ONLINE JUNCTION TEMPERATURE ESTIMATION OF SIC POWER MOSFETS

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Abstract

Silicon Carbide (SiC) based power devices receive more and more popularity in the field of power electronics as they operate at higher voltages, higher switching frequencies and higher temperatures compared to traditional Silicon (Si) based power modules. As for SiC-based power devices, the temperature of SiC chip must be monitored in order to operate the device within its limit.

However, it is not straight forward to directly measure the junction temperature (T_j) of a power device non-intrusively due to the package obstruction. Therefore, indirect T_j measurement methods like Temperature Sensitive Electrical Parameters (TSEPs) are preferred by researchers and been intensively investigated for Si devices as the dominant power devices in the past. However, those TSEPs which are effective for Si devices are mostly not applicable to SiC devices. This is due to different physical and electrical behaviour between SiC-based device and Si-based device. Thus, it is necessary to develop new method to implement indirect T_j measurement for SiC devices.

This thesis presents a new on-line technique to estimate the T_j of discrete SiC MOSFET devices. In this work, small amplitude, high frequency chirp signals are injected into the gate of a discrete SiC device during its off-state operation. Then, the gate-source voltage (V_{GS}) is measured and its frequency response (FR) characteristic is determined by using Discrete Fast Fourier Transform (DFFT) analysis. The captured V_{GS} signal is a direct function of the gate-source loop impedance. The derived function becomes a linear function in respect T_j as it represents only the resistive elements of the gate-source loop. As the gate channel resistance of the SiC MOSFET (R_{int}) is the largest resistance in that loop and it is temperature dependent. As a result, the temperature of the SiC MOSFET chip can be estimated.

The new method in the thesis will be explained in details and the theory will be backed up by analytical simulations. A 3D numerical model for the discrete SiC MOSFET is also established and simulated. Furthermore, a network analyser is used for initial validation of the new method and finally a boost circuit was built with signal injection circuit integrated within the gate driver circuit to demonstrate the feasibility of using this innovative method to extract junction temperature of a discrete SiC MOSFET.

Keywords- SiC MOSFET, Junction Temperature, Small AC Signal Injection

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List of Abbreviations

α	Base Transport Factor
α_{ge}	Proportional Constant
β_{PNP}	Current Gain of IGBT
ε_s	Permittivity of Semiconductor
μ	Electron Channel Mobility
μ_n	Electron Mobility
μ_{ns}	Surface Mobility of Electrons
τ_G	Time Constant
τ_n	Lifetime of Space charge region
τ_p	Carrier Lifetime
a	Atomic Spacing
A	Junction Area
A_{eff}	Effective Cross-sectional Area
A_I	Current Gain
AC	Alternating Current
BJT	Bipolar Junction Transistors
c	Lindeman Constant
C_{DS}	Drain-source Capacitance
C_{GC}	Gate-collector Capacitance
C_{GD}	Gate-drain Capacitance
C_{GS}	Gate-source Capacitance
C_{iss}	Input Capacitance
C_{oss}	Output Capacitance
C_{rss}	Reverse Recovery Capacitance
C_{ox}	Oxide Capacitance
C_O	Charge extraction capacitance
CET	Coefficients of Thermal Expansion
CO_2	Carbon Dioxygen

d	Diameter
D_n	Diffusion Coefficient of an Electron
D_p	Hole Diffusion Coefficient
DBC	Direct Bond Copper
DC	Direct Current
DCB	Direct Copper Bonding
DFT	Discrete Fourier transform
DPT	Double Pulse Test
DUT	Device Under Test
EV	Electric Vehicle
FWD	Free-wheeling Diodes
g_m	Transconductance
G	Thermal Dynamic Model
GaN	Gallium Nitride
h	Planck's Constants
HEMT	High Electron Mobility Transistor
I_C	Collector Current
I_{CE}	Collector-emitter Current
$I_{DS(on)}$	On-state Current of MOSFET
I_{GON}	Turn-on Gate Current
I_{GOFF}	Turn-off Gate Current
I_{Gpeak}	Gate Current Peak
I_{leak}	Collector leakage current
I_m	Measurement Current
I_s	Saturation Current
I_{sat}	Saturation current
I_{SC}	Short-circuit Current
I_{tail}	Tail Current
IGBT	Insulated Gate Bipolar Transistor

k	Boltzman's Constant
k_t	Thermal Conductivity
kV	Kilovolts
L_{air}	Air-core Inductor
L_C	Channel Length
L_g	Gate Inductance
L_n	Diffusion Lengths in N Region
L_p	Diffusion Lengths in P Region
m	Atomic Mass
m_{de}	Electron Effective Masses
m_{dh}	Hole Effective Masses
$Magnitude_{Total}$	Integrated Magnitude
MEA	More Electric Aircraft
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
N_A	Acceptor Carrier Densities
N_{Amax}	Surface Concentration
N_B	Doping Concentration in Low-doped Region
N_b	Base-doping Concentration
N_D	Donor Carrier Densities
n_i	Intrinsic Carrier Doping Concentration
NTC	Negative Temperature Coefficient
P_{dlss}	Power loss dissipation
P_{loss}	Power Loss
Q	Total Amount of Heat
r	Radius
r_0	Ohmic Resistance at Reference Junction Temperature
$R_{DS(ON)}$	On-state Resistance
R_{ext}	External Gate resistance
R_G	Total Gate Resistance

R_{int}	Internal Gate Resistance
R_{ref}	Reference Resistance
SEM	Scanning Electron Microscopy
SiC	Silicon Carbide
Si	Silicon
T_C	Case Temperature
$t_{d(on)}$	Turn-on Delay Time
$t_{d(off)}$	Turn-off Delay Time
T_j	Junction Temperature
T_{j0}	Reference Junction Temperature
T_{j_avg}	Average Junction Temperature
T_{jmax}	Maximum Junction Temperature
t_{Miller}	Duration of the Miller Plateau
TDDB	Time-dependent Dielectric Breakdown
TSEP	Temperature Sensitive Electrical Parameter
u	Average Vibration Amplitude
V_{GE}	Gate Emitter Voltage
V_{TH}	Threshold Voltage
V_{CEsat}	Collector-emitter Saturation Voltage
$V_{CE(on)}$	On-state voltage drop
V_{CE0}	On-state Voltage Drop at Reference Junction Temperature
V_{FB}	Flat-band Voltage
V_{dc}	DC-link voltage
V_{on}	On-state voltage
$V_{GG(OFF)}$	Gate Drive Voltage during Turn-off
V_b	Breakdown Voltage
V_a	Avalanche Breakdown Voltage
V_{CC}	Gate Driver Supply Voltage High
V_{EE}	Gate Driver Supply Voltage Low

v_{sat}	Saturation Drift Velocity
v	velocity
V_F	Forward Voltage
V_{ir}	Current Induced Voltage Drop
V_{BE}	Base-emitter Voltage
$V_{DS(on)}$	On-state Voltage of MOSFET
V_{eE}	Voltage between Power and Kelvin Emitter
v_{sat}	Saturation Drift Velocity
V_{AC}	AC Voltage Source
V_{GSpeak}	Gate-Source Voltage Peak
V_{leads}	Lead Voltage
$V_{bond\text{-}wire}$	Bond wire Voltage
V_{stray}	Stray Voltage
V_{sweep}	Sweeping voltage
V_{ext}	External Gate Resistance Voltage
V_{int}	Internal Gate Resistance Voltage
$V_{GSPeaktotal}$	Integrated Gate-Source Voltage
WBG	Wide-band Gap
x_d	Diffuse Length
Z_C	Channel Width
$Z_{th(JC)}$	Equivalent Thermal impedance between Junction and Case
$Z_{bond\text{-}wire}$	Bond wire Impedance
Z_{stray}	Stray Impedance
Z_{sweep}	Sweeping Impedance
Z_{ext}	External Gate Resistance Voltage
Z_{int}	Internal Gate Resistance Voltage
Z_{leads}	Lead Impedance

Chapter 1 Introduction

1.1 Background

One main requirement for many power electronics applications such as electric vehicles (EV) and more electric aircraft (MEA) is to achieve converters with high power density in compact sizes. Power switching modules, which are the heart of any power converter, must therefore be light and small too. However, increased power density generally incurs bigger electrical, mechanical and thermal stresses in power electronic components, including power switching modules [1]. These stresses induce the likelihood of devices failure, which may cause catastrophic failure in the whole converter system. According to an industry-based survey of the reliability of power electronic converters [2], power switching modules are still the most fragile components, as shown in Figure 1.1.

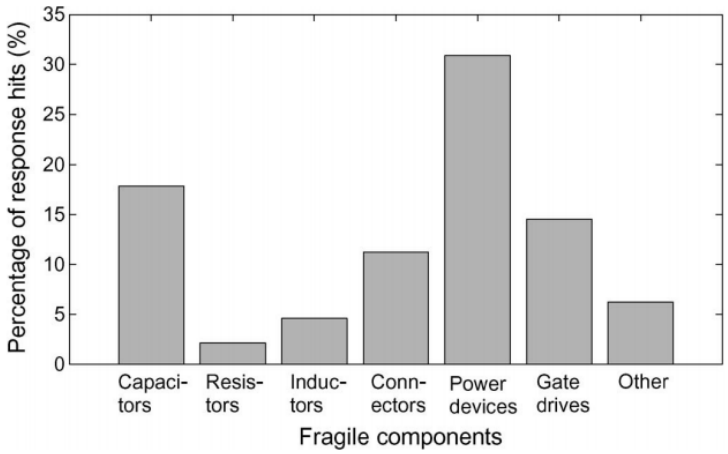


Figure 1. 1 Industrial survey of fragile components in power electronic converters [2].

In power devices, bond wire fractures, heel-cracks and lift-off, chip surface metallization and case direct bond copper (DBC) or chip-DBC fatigue are the most commonly seen of the main failure types in power switching modules [3]. All of the aforementioned failures are caused mainly by the heavy thermal-mechanical stress [4, 5], and thus electrical performance and reliability of power electronic systems are closely related to the junction temperature (T_j) of power devices. Therefore, it is essential to establish a measurement method to precisely determine the value of T_j in a device without interfering the normal operation of the power converter system.

a. Model-based estimation of T_j

Analysis based on simplified electrical and thermal models in conjunction with the semiconductor datasheet values is one of the classic ways to estimate the value of T_j. Usually, the average junction temperature (T_{j_avg}) can be estimated via stationary thermal models taking into consideration the thermal resistances and capacitances [6]. It is also possible to determine the junction temperature swing (ΔT_j) and even the maximum junction temperature (T_{jmax}) if non-stationary conditions are assumed. An example of the T_j profile of a power device is presented in Figure 1.2. The value of ΔT_j depends on the total power dissipation generated by the device and the thermal impedance of the circuit, the range of the ΔT_j can vary from several milli-degrees to several tens of degrees.

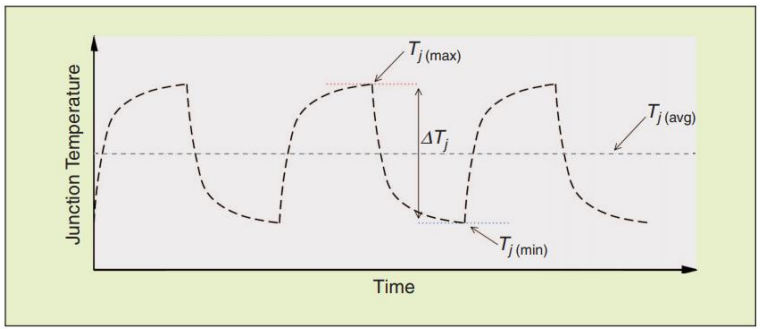


Figure 1. 2 An example of T_j profile of a power electronic device.

Although such modelling methods based on the manufacturer data have been extensively utilized [7], these techniques are limited due to poor accuracy. This is because the thermal values given by the manufacturer usually take into account the worst-case scenarios and may not be appropriate for different topologies.

A more critical problem is that the thermal and electrical parameters of a power device or module will change due to the degradation of the converter [8, 9], which will make the estimation even more inaccurate given the degradation of the power device or module.

b. Temperature sensors embedded in the device

Due to the obstacles of module packaging and dielectric gel, it is not possible to directly gain access to chips, which prevents optical and physical solutions for the measurement of temperature such as by using infrared cameras or optical fibres. Thus, alternative methods have

been proposed to integrate temperature sensors within the power chip structure. Such industrial applications have been implemented; for instance, Moto and Donlon [10] fabricated a string of diodes on the surface of the IGBT chip and utilized the linear relationship between the forward voltage drop of the string diodes and the temperature to estimate the value of T_j of the IGBT chip. However, this method can only provide a local temperature measurement, which means it cannot reflect the thermal gradient of the whole chip and is not able to determine the peak temperature where degradation is most likely to appear [7]. A solution with multi-temperature sensors has been proposed [11] which gives the global surface temperature of the chip. However, extra wires are required for connections to the sensors to acquire the data and this method still requires some modification of the chip surface, which is not desirable.

c. Temperature-sensitive electrical parameters

Over the past few decades, intensive research has been conducted to investigate the relationship between T_j and inherent electrical parameters that depend on it. Those electrical parameters are called temperature-sensitive electrical parameters (TSEPs) [12]. State-of-the-art TSEPs have been summarized [12] and are discussed in detail in chapter 3. These studies reveal the potential of using TSEPs to precisely extract T_j during the operation of a converter for traditional Si IGBT or MOSFET. However, the requirement to modify the converter structure or its control strategy to accomplish the TSEP measurement circuit or measuring time window can be seen as serious issues in real applications.

1.2 Wideband-gap semiconductor

In order to increase power-density and reduce size, Si semiconductor devices are being replaced with wideband-gap (WBG) semiconductors like silicon carbide (SiC), Gallium Nitride (GaN) or diamond (C). WBG power switching modules promise the potential to switch at higher-power, and they have higher-temperature capability, better thermal conductivity and faster switching speeds. Some key characteristics of WBG semiconductors have been reviewed and compared with Si [13].

Among these WBG semiconductors, discrete SiC MOSFETs have been successfully manufactured by several companies and are now commercially available [14]. As with Si power switching modules, knowledge of T_j is equally important. In fact, SiC MOSFETs can operate at much higher temperatures, and so temperature swings and therefore stresses on the different

layers that form the SiC power switching module are much greater. However, the aforementioned T_j measurement methods can hardly be applied to discrete SiC MOSFETs [15]. The difficulties of extracting T_j value for discrete SiC MOSFET has encouraged the author to investigate a new method to measure T_j for discrete SiC MOSFETs online.

1.3 Objectives

1. Examining TSEPs that applicable for Si device on discrete SiC MOSFET to gain thorough understanding of the behaviour of those TSEPs for SiC-based electronic devices.
2. Establishing a precise small AC signal equivalent circuit to enable simulation for discrete SiC MOSFET and study the its off-state operation.
3. Creating 3D thermal model of SiC MOSFET and utilizing FEM software to determine the internal T_j rise caused by power dissipation. The aim is to calibrate the actual T_j with the measured T_j in the experiments in order to reduce errors.
4. Propose the new method to determine T_j of discrete SiC MOSFET based on analysis carried out as indicated in point 1, 2 and 3.
5. Conducting practical experimental to validate the method developed.

1.4 Contribution to knowledge

The main original contribution of this research are as follows:

- State-of-the-art T_j measurement methods for Si power devices are examined on discrete SiC MOSFET to check the viability of those methods. And it turns out that those methods have their limits to be applied to SiC-base devices.
- The use of small AC signal analysis as a method to accurately extract the junction temperature for SiC MOSFETs is proposed for the first time.
- A small AC signal equivalent circuit of a Cree 2rd generation discrete SiC MOSFET is developed for an unbiased SiC MOSFET. The model includes all individual parasitic factors and all parameters have been calculated. The designed small AC signal equivalent circuit has been simulated.
- The gate-source impedance curve for an unbiased SiC MOSFET is measured as a function of temperature using a network analyser. The results are compared with the small AC signal equivalent circuit model for validation purpose.

- The proposed AC sweeping technique is implemented in an existing SiC MOSFET gate drive circuit applied to a biased SiC MOSFET. It is shown by experiment that the proposed technique can detect the temperature of the chip with an error of 5%.
- The proposed technique is implemented and validated in practical work.

The work conducted has resulted in the following publications:

[1] L. Xiang, C. Chen, M. Al-Greer, V. Pickert, and C. Tsimenidis, "An investigation of frequency response analysis method for junction temperature estimation of SiCs power device," i*n 2018 IEEE 10th CIPS conference.*

[2] L. Xiang, C. Cuili, M. Al-Greer, V. Pickert, and C. Tsimenidis, "Signal processing technique for detecting chip temperature of SiC MOSFET devices using high frequency signal injection method," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, 2017, pp. 226-230.

The author has also contributed to the following research:

[3] C. Chen, V. Pickert, M. Al-Greer, C. Tsimenidis, T. Logenthiran, X. Lu, "Signal sweeping technique to decouple the influence of junction temperature and bond wire lift-off in condition monitoring for multichip IGBT modules," i*n 2018 IEEE 10th CIPS conference.*

1.5 Thesis outline

This thesis consists of six chapters. Chapter 1 gives a brief introduction of the background to the thesis, including state-of-the-art T_j detection technique for Si power electronic devices or modules and the progress of WBG semiconductors as well as the importance of the development of a corresponding T_j measurement solution.

In Chapter 2, a specific overview of the SiC MOSFET and some state-of-art junction temperature measurement techniques are presented, including a detailed comparison between Si and SiC semiconductors. To begin with, the physical characteristics of Si and SiC are compared and the results show that the superior capabilities of SiC materials can potentially break the performance ceiling of SiC semiconductors. Then the switching characteristics of both Si and SiC devices are compared as well which suggests that those differences may lead to difficulties in implementing T_j measurement. Then, several T_j measurement methods used to implement for Si devices with similar packaging technologies are presented. These techniques are divided into three classes: direct and indirect temperature measurement techniques and thermal model-based approaches. The direct temperature measurement techniques can be listed as follows: infrared thermal camera techniques, embedded temperature sensor methods and diode-on-die temperature sensing methods. These techniques are intrusive, which means either

the devices or module should be opened, or modifications should be carried out during the manufacturing process. These features therefore limit the application of direct temperature measurement. On the other hand, indirect temperature measurement methods use the TSEPs to estimate the T_j values of the devices or modules. State-of-the-art TSEP measurement techniques are presented and compared and principal measurement circuit are plotted for each method. The third measurement technique is the thermal model-based method. Both open-loop and close-loop thermal models used for estimating T_j are explained. Finally, their advantages and disadvantages are concluded and compared as well.

Chapter 3 presents a 3D model of a Cree/Wolfspeed discrete SiC MOSFET (part number: C2M0080120D[16]) with TO247-3 packaging is created by using Autodesk Inventor 3D computer-aided design software. The implementation of the 3D model is based on the information provided by manufacturer's datasheets including dimensions of each components as well as materials of each parts. In addition, a 3D model of a heat plate which will be used in the later experimental test is established as well and it is fully constrained at the bottom of the SiC MOSFET. After successfully producing the 3D model, both models of the discrete SiC MOSFET and the heat plate are imported into the ANSYS finite element analysis software to perform thermal analysis. The main purpose of the thermal study is to determine the temperature difference between the hottest die body and the case surface temperature. The temperature difference will be used later to calibrate with the experimental results to reduce error.

Chapter 4 starts with simulation results for traditional TSEPs applied to the discrete SiC MOSFET and the results suggests that these TSEPs are unsuitable for SiC MOSFET due to either lower sensitivity or reduced T_j dependency. Therefore, the motivation for proposing a new method to estimate T_j values for SiC MOSFET arises. The author proposes a new technique to extract the T_j value of the SiC MOSFET by a technique which analyses using small AC signal. An equivalent small AC signal circuit for a SiC MOSFET during its off-state is developed and individual parasitic values are calculated as well. The proposed model is simulated in LTspice and then the simulation results are compared the practical results with the help of an impedance analyser. The results indicate a good alignment between the two sets of values.

Chapter 5 describes the experimental test for the estimation of T_j in a discrete SiC MOSFET by using small AC signal analysis. The experimental circuits are explained in detail at first and then experimental results under different DC bias conditions are presented and analysed. The results show that the proposed method has promising potential to fulfil the capability to give accurate estimations of the T_j values of SiC MOSFETs. In addition, Cree/Wolfspeed discrete SiC evaluation board (part number: KIT8020-CRD-8FF1217P-1) is utilized to create a standard

non-synchronous boost converter with a Cree/Wolfspeed SiC Schottky diode (C4D20120D) and a discrete SiC MOSFET (part number C2M0080120D). The proposed method is used during normal operation of the boost converter, and the small AC chirp signal is superimposed via the gate driver of the evaluation board. The results will be presented and analysed.

Finally, Chapter 6 summarizes the research work which has been carried out and the advantages and disadvantages of the proposed method are discussed. Future work which can be carried out afterwards to improve the proposed method is also recommended.

Chapter 2 Overview of SiC MOSFET and State-of-Art T_j Measurement Techniques

Wideband-gap (WBG) semiconductor devices have become more and more attractive in power electronics applications [17-19], due to their superior characteristics compared to silicon-based semiconductors. The more efficient manufacturing of WBG devices has seen a drop in the cost of making them and they are now attractive for mainstream use. The most popular device is the discrete normally-off n-channel SiC MOSFET with break-down voltages ranging between 600 V and 1.2 kV. For example Cree introduced the 1.2 kV, 33 A SiC MOSFET in 2011 [20]. Other manufacturers like Rohm and POWEREX are also developing discrete SiC MOSFETs [21-23].

2.1 Comparison of physical structure and characteristics of Si and SiC MOSFET

SiC-based power devices are becoming more and more popular as they provide the opportunity to build power converters which are smaller and lighter. SiC MOSFETs have advantages over Si MOSFETs due to the former's physical material properties. As illustrated in Figure 2.7, SiC material offer three main advantages over Si: firstly, higher band-gap energy and increased electric field capacity resulting in higher voltage operation; secondly, extended thermal conductivity and a higher melting point, which makes SiC applicable for higher temperature operations; and thirdly, faster electron velocity, which gives SiC-based devices increased switching frequencies compared to Si-based devices [24].

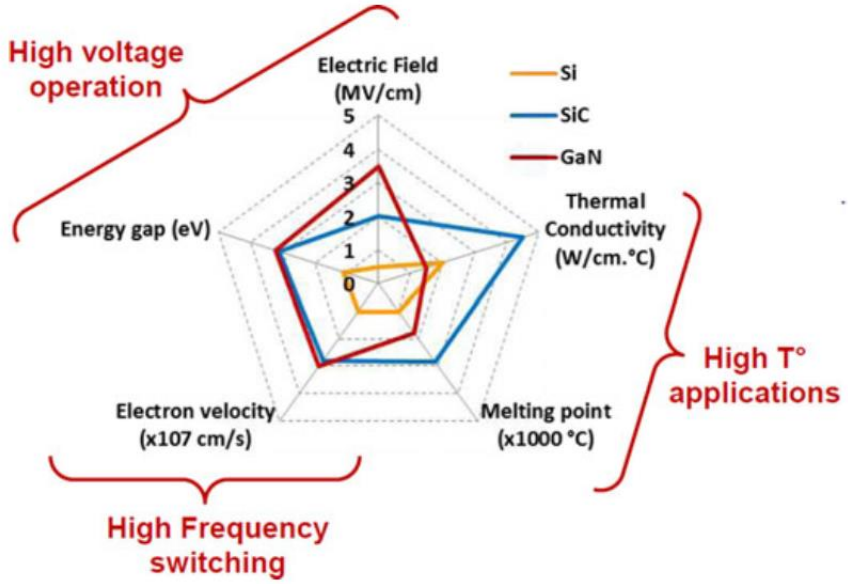


Figure 2. 1 Comparison of Si, SiC, and GaN material characteristics [18].

All of the five listed characteristics in Figure 2.7 can be described analytically. In the following sections, the key equations in semiconductor physics are shown.

a. Energy Gap

The temperature and band-gap energy of semiconductor materials determine the intrinsic carrier density n_i, and the relationship between them is given by equation 2.1.

$$n_i = \left(\frac{2\pi kT}{h^2}\right)^{3/2} (m_{dh} m_{de})^{3/4} exp\left(\frac{-(E_c - E_v)}{2kT}\right) \tag{2.1}$$

where k and h represent the Boltzman's and Planck's constants respectively, T is the absolute temperature, m_{de} and m_{dh} are the electron and hole effective masses respectively, and (E_c-E_v) is the band-gap energy. Equation 2.1 shows that the influence of temperature on the intrinsic carrier density weakens in cases of higher band-gap energy material. This is an important characteristic that is favoured in high-temperature applications [25]. The bandgap of SiC is 3.2 eV and of Si is1.12 eV. Also, a higher band-gap energy results in a lower intrinsic carrier density, which results in smaller leakage currents at the p-n junction. The relationship between the leakage current of a p-n junction and the intrinsic carrier density is given by equation 2.2 [26]:

$$j_s = q n_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) \tag{2.2}$$

In equation 2.2, N_D and N_A are the donor and acceptor carrier densities respectively, D_p and D_n are diffusion constants of the p and n regions respectively and L_p and L_n are the diffusion lengths in the p and n regions.

b. Electric field

The n-drift region determines the breakdown voltage capability in a vertical MOSFET, and a higher critical electric field provides the capability for it to withstand higher breakdown voltage. SiC has a critical field of $2.2\ \mathrm{MV/cm}$ and for Si it is $0.25\ \mathrm{Mv/cm}$. Equation 2.3 describe the breakdown voltage of a p-n junction [26]:

$$V_{BD} = \frac{\varepsilon_s E_{crit}^2}{2qN_B} \tag{2.3}$$

Where ε_s is the permittivity of the semiconductor, E_{crit} is the critical electric field at breakdown and N_B is the doping concentration of semiconductor in the low-doped region.

The conductivity of the drift region is given by equation 2.4 [26]:

$$\delta = q\mu_n N_D \tag{2.4}$$

Where μ_n is the electron mobility, N_D is doper concentration and to be specified in the n drift region. Assuming N_D=N_B, the equation 2.3 and equation 2.4 combine to become equation 2.5:

$$V_{BD} = \frac{\mu_n \varepsilon_s E_{crit}^2}{2\delta} \tag{2.5}$$

It can be interpreted from the above equation that a higher critical electric field makes it possible to achieve higher conductivity at the same breakdown voltage.

c. Electron velocity

The theoretical channel transition time of the MOSFET is defined as the time that carriers travelling in a channel at their saturation drift velocity v_{sat}, and is represented by equation 2.6 [27]:

$$\tau_t = \frac{L}{v_{sat}} \tag{2.6}$$

For SiC, v_{sat} is $20\ \mathrm{Mcm/V}$ and for Si it is $10\ \mathrm{Mcm/V}$ [11].

The channel transition speed can also be described as the transition frequency $1/\tau_t$. Higher saturation velocity means a higher transition frequency. For MOSFETs, theoretical transition frequency cannot be achieved due to parasitic capacitance, and instead, the transition frequency is given by equation 2.7 [27]:

$$f_T = \frac{1}{2\pi C_{iss} R_G} \tag{2.7}$$

where the C_{iss} is the input capacitance and it is the combination of the gate-source capacitance C_{GS} and gate-drain capacitance C_{GD}. R_G is the gate resistance which is a combination of external gate resistance R_{Gext} and internal gate resistance R_{Gint}. Since the SiC MOSFET has smaller parasitic capacitance in comparison with the Si MOSFET, the former can operate at higher frequency.

d. Thermal conductivity

SiC has a thermal conductivity about 2 to 3 times higher than this property in Si material (SiC: 4 $\mathrm{W/(cm \cdot K)}$ Si: 1.5 $\mathrm{W/(cm \cdot K)}$ [11]). Equation 2.8 shows the relationship between thermal conductivity and the amount of heat the material can dissipate [11]:

$$k_t = \frac{QL}{A\Delta T} \tag{2.8}$$

where k_t is the thermal conductivity of the material, Q is the total amount of heat transfer through the material in J/S or W, A is the surface area of the material body in cm^2, L is the length of the material body in cm, and ΔT is the temperature difference. As can be seen from the equation, higher thermal conductivity enables SiC MOSFETs to dissipate heat more efficiently, which makes it capable of working in higher temperature conditions.

e. Melting point

Assuming that all atoms in a crystal vibrate with the same frequency, v, the average thermal energy (E) can be estimated using the equipartition theorem [28] as follows:

$$E = 4\pi^2 m v^2 u^2 = kT \tag{2.9}$$

where m is the atomic mass, v is the velocity, u is the average vibration amplitude, k is the Boltzmann constant, and T is the absolute temperature. If the threshold value of u^2 is c^2a^2, where c is the Lindeman constant and a is the atomic spacing, then the melting point is estimated as:

$$T_m = \frac{4\pi^2 m v^2 c^2 a^2}{2k_B} \tag{2.10}$$

The melting temperature for SiC is around 2700 ˚C and for Si material is only 1400 ˚C. This fact means that SiC material has the potential to operate in circumstance of much higher ambient temperature.

2.2 Comparison of switching characteristics of Si and SiC MOSFETs

Due to the significant different material on-state and switching performance of SiC MOSFETs and Si MOSFETs, the SiC material makes SiC MOSFETs superior in switching performance.

a. Non-linear on-resistance

One obvious difference between SiC and Si MOSFET is the temperature dependence of on-state resistance ($R_{DS(ON)}$) at different values of V_{GS}. The relationships of $R_{DS(ON)}$ against temperature are presented in [29] and the main results are shown in Figure 2.5. For a SiC MOSFET $R_{DS(ON)}$ plotted versus temperature shows a U-shape curve in contrast to that for the Si Cool MOSFET which shows a linear relationship with temperature.

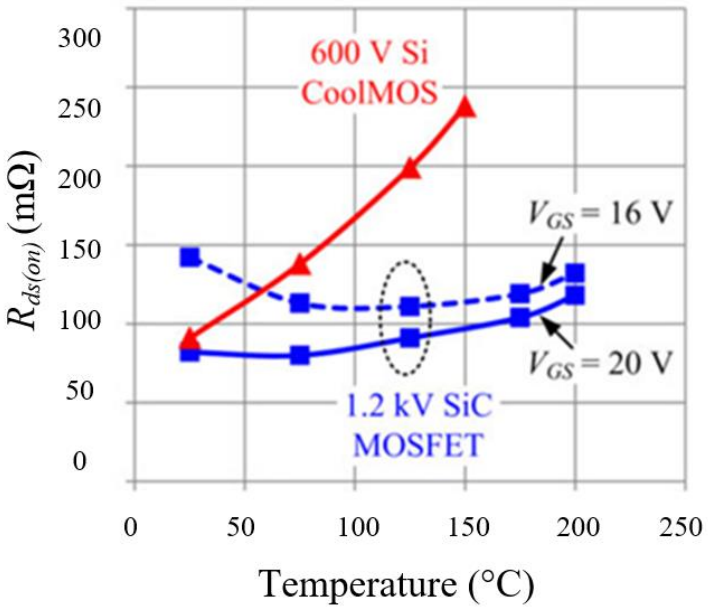


Figure 2. 2 Comparison of on-state resistance versus temperature of Cool MOSFET and SiC MOSFET at various gate voltages [29].

b. Negative turn-off gate voltage

Another characteristic difference in terms of gate drive considerations is the turn-off voltage level. Due to the ultra-fast switching speed, a negative turn-off bias gate voltage (usually -2 to -5 V) is recommended for the SiC MOSFET in order to increase the threshold margin and *dv/dt* immunity, which would be helpful to avoid the false triggering in phase-leg operations [30]. Appendix B describes gate drive circuits for SiC MOSFETs in more detail.

c. Non-flattened Miller plateau

The much smaller Miller capacitance (C_{GD}) of the SiC MOSFET also leads to different switching characteristics in comparison with the Si MOSFET. One result of the smaller Miller capacitance of the SiC MOSFET is a significantly faster V_{DS} switching transient for the Si counterpart. Another result is a non-flat Miller plateau [31], which means that the SiC MOSFET will be less temperature-sensitive during the switching transient in comparison with the Si MOSFET.

For power devices, it can be concluded that one of the fundamental causes of degradation is a mismatch in the coefficients thermal expansion (CTEs) between the different layers in the power module structures. CTE mismatch results in bond wire lift-off and solder cracks. Thus, these particular thermo-mechanical effects lead to increase in chip temperature. Consequently, the values of the device's T_j represents information on power module degradation, and this information can be used to detect forthcoming failures of power semiconductor modules. However, the precise extraction of T_j values in real time is difficult and therefore has become a hot topic in both academic and industrial research. The following section summarizes various techniques that have been proposed in extracting T_j for Si power semiconductor devices, but those techniques can be applied to SiC devices. It is because of SiC devices are still using those packages used by Si devices which enables those T_j measuring techniques potentially viable for SiC devices. The advantages and disadvantages of the different methods are also listed. A more detailed description of some of the selected measurements is provided in Appendix A.

2.3 Direct temperature measurement techniques

There are three different methods used to measure chip temperature directly via an infrared camera, a thermos-coupler attached to the die, and using a chip with an integrated semiconductor temperature sensor.

a. Infrared thermal camera

For the bare die type or unpackaged power devices, it is viable to utilize an infrared (IR) thermal camera [32]. The benefit of this is that this camera captures the temperature over the full device surface allowing a thermal distribution map of the chip to be generated. A test bench utilizing

IR camera to observe the surface temperature of an IGBT module has been presented [33] as shown in Figure 2.3. A dedicated un-encapsulated power module free of gel is used which has been developed in order to carry out IR surface temperature measurements of the IGBT module, as illustrated at the top left corner of Figure 2.3. One of the downsides of using IR is that large measurement errors may occur due to the surface degradation of materials and the intrinsic low emissivity of aluminium in combination with the complex geometry of the active parts inside the IGBT module [34]. To reduce the error, the IR measurement should be conducted by controlling the surface emissivity with a paint solution in order to achieve relatively even surface emissivity. Furthermore, in order to obtain more accurate chip temperature measurements, the emissivity of the black paint should be estimated, and a numerical procedure is necessary to extract the real temperature of the active part of the device, excluding the electrical connections, the inactive areas, and also artefacts due to radiative reflections [33].

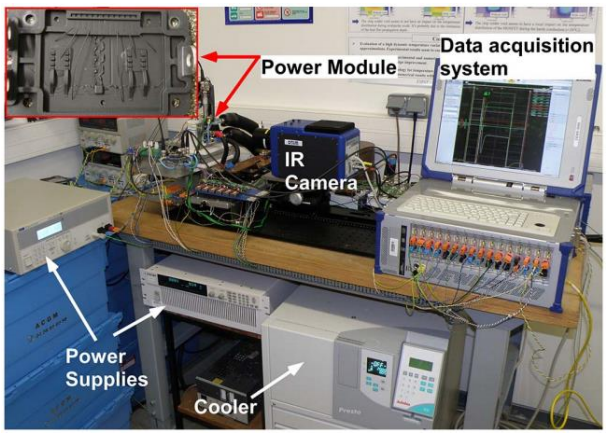


Figure 2. 3 Test bench for IR measurements [33].

The advantage of IR measurement is that the whole surface temperature distribution can be obtained, which is very helpful in determining the exact location of hot spots that indicate failure or in case of large modules in which chips suffer the most thermal stress [35]. However, a thermal camera can only be used in a laboratory environment. The camera is also expensive, and therefore is often used for calibration or validation purposes [12, 36-38] only, rather than for use in real field operations.

3.1 *Embedded temperature sensor*

Embedded temperature sensors for power semiconductor modules are commonly used in large power modules [39]. This technique is not widely applied in commercially available power

devices and is preferred by certain industrial organizations working in high-end applications such as electric vehicles, aerospace applications or large industrial drives [39]. For example, companies like Toyota and Tesla are designing power modules with these temperature sensors [40]. The negative temperature coefficient (NTC) thermistor is one popular type of embedded temperature sensor for large power modules, it is usually located on the same ceramic substrate as the IGBT and diode chips. An example showing a Mitsubishi NX6 and NX6.1 IGBT module with an embedded NTC is illustrated in Figure 2.4. The IGBT chip temperature can be calculated by using a thermal model and measuring the temperature of the NTC in steady state [41].

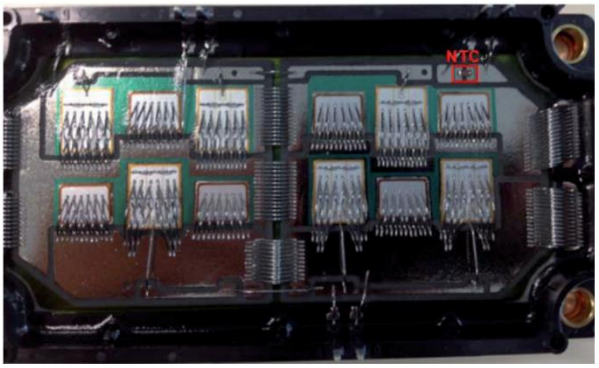


Figure 2. 4 An IGBT module with embedded NTC sensor [41].

c. Diode-on-die temperature sensor

The third option is to integrate a temperature sensor within the chip. It is known that the forward voltage drop of a p-n junction under certain current conditions is temperature-sensitive [42]. It is possible for the manufacturer to embed a temperature-sensitive p-n junction onto the power semiconductor chip die area with the support of today's die fabrication techniques [10, 43, 44]. A part of the chip area is doped to create a diode which is not electrically connected to the gate emitter or collector of the chip. The polysilicon with insulation technique [45, 46] is utilized to fabricate p-n junction sensors on IGBT and SiC MOSFETs respectively. Usually not one but several p-n junctions are connected in series [10] when fabricated on a power semiconductor chip as an on-die temperature sensing indication. A half-bridge IGBT module with two IGBTs and free-wheeling diodes (FWDs) in parallel has been proposed [47]. As shown in Figure 2.5, each IGBT chip has a string of diodes fabricated in the polysilicon, which is on the surface of

the IGBT chip's emitter side. Chip temperature can be detected by measuring the forward voltage drop when it is forward-biased. As with most silicon diodes, the forward voltage-drop decreases with increasing T_j. To alleviate noise problems, a string of diodes is used to provide a high enough sensing voltage. However, using the temperature sensing diode during continuous switching operations is still challenging due to several facts listed below.

The first challenge is low forward voltage (V_F) sensitivity, where low signal amplitude and sensitivity make it vulnerable to noise which makes it hard to accurately sense T_j during switching transients.

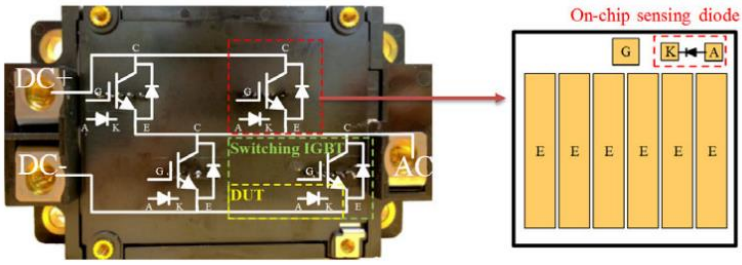


Figure 2. 5 IGBT module with on-die temperature sensing diodes [47].

The second issue is that, since the T_j sensing diodes are sited on the die area, the short distance to sources of noise would induce noise propagation. The parasitic capacitances between the two parallel IGBTs are likely to be larger than the NTC solution, as illustrated in Figure 2.6. A displacement current incurred during the *dv/dt* switching transient may also affect the sensor's output signal, which will be even more critical in WBG devices. Moreover, these capacitance values are difficult to measure directly as they are all interconnected with the device's parasitic capacitances.

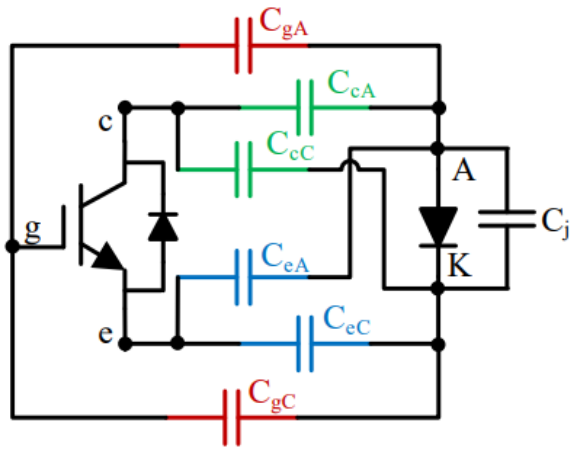


Figure 2. 6 Parasitic capacitances between the sensing diode and power device [47].

Polysilicon with insulation technique has been utilized [45, 46] to fabricate p-n junction sensors on IGBT and SiC MOSFETs respectively. Usually not one but several p-n junctions are connected in series [10] when fabricated on a power semiconductor chip as an on-die temperature sensing indicator.

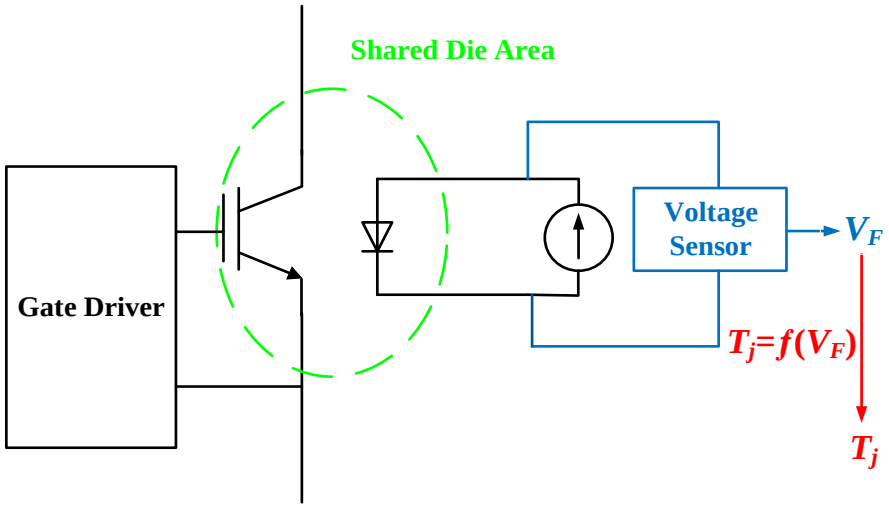


Figure 2. 7 Principal circuit for IGBT T_j sensing based on diode forward voltage.

As shown in Figure 2.7, in order to use the on-die diode as a T_j indicator, a constant current is required to flow through the diode and then the voltage across the diode can be measured and used for online T_j extraction. After proper correlation, the relationship between the diode

forward voltage drop and T_j can be established and in a previous study the sensitivity was $-6.7\ \mathrm{mV/^{\circ}C}$ [10].

This T_j sensing technique based on the diode forward voltage drop is capable of providing a fast thermal-dynamic response to the semiconductor chip due to the small size of the diode itself. Signal processing in this method is easy to implement as well, because only the forward voltage is captured and only the relationship between the forward voltage V_F and T_j. T_j is required. A Fuji 7MBP50RA060 IGBT module using the above described method gave a $2\ \mathrm{ms}$ response time for an over-temperature alarm [45],.

The sensing of T_j with a constant current source and voltage measurement [9] can be integrated inside the power module. Although sharing the same die, the temperature-sensitive p-n junction is isolated from the power semiconductor except for its capacitive coupling, which can limit its usefulness during transients [11]. This is not the only limitation of this technique, and some other issues have been identified. Firstly, the consistency of sensing can be challenging given the limited number of diodes used for T_j sensing. As a result, the performance of the sensors fabricated in the same batch can vary significantly [11]. Secondly, the on-chip p-n junction T_j sensor is usually fabricated on a small area on the power semiconductor chip as shown in previous studies [39, 41]. This location may not provide an accurate picture of the thermal gradient of the chip. Thirdly, another issue is caused by the small size of the p-n junction in that it is quite tricky to connect the relevant area to the measurement circuit via wire bonds or DBC, and those wire bonds or DBC would also insert a certain amount of parasitic and contact resistance as well [48]. Finally, the close location involved becomes a disadvantage when considering that the performance of the sensing of T_j would be distorted by the noise generated by the switching power semiconductor.

2.4 Indirect temperature measurement techniques

Over the last two decades a lot of researches have focused on the indirect measurement of T_j. Rather than measuring the temperature directly, a relationship between voltage and current signals measured at the gate, emitter and the source and the temperature is investigated. This is because most semiconductor parameters, such as the on-state collector-emitter voltage of the IGBT or the on-state resistance of the power MOSFET, are temperature-dependent.

Parameters that have a strong relationship with T_j are called temperature-sensitive electrical parameters (TSEPs) [12]. TSEPs must fulfil minimum requirements in order to be used. These

requirements are firstly, that the parameters can be measured offline in order to determine the relationship between the TSEP electric parameter of voltage or current and T_j. Secondly, the measured relationship must be stored as reference. Thirdly, it must be possible to capture the electrical parameter on the in-field power semiconductor module during operation and it must be possible to compare the measurement with the stored reference. The reference will then provide the T_j.

So far 20 different TSEPs have been proposed and the most promising TSEPs are those which have a linear relationship between the monitored electric parameter and temperature. In addition, TSEPs should have a fixed gradient, so that there is no change from positive to negative gradient or vice versa over the entire temperature range. Furthermore, the gradient angle should be large enough to provide for enough sensitivity to determine the correct temperature. Obviously, the resolution of the sensors is important and must be considered in the entire TSEP chain. Finally, the measurement itself should not disrupt the operation of the converter. The next sections provide an overview of traditional TSEPs.

2.4.1 Component-on-die T_j extraction

Some components such as internal gate resistance that are located near the die area can be used as an indication of the value of T_j, this method has the advantages that, since those components are sitting extremely close to the die, thermal impedance and capacitance between the semiconductor junction area and those temperature sensitive components are small which means that the T_j sensing bandwidth is high.

a. Internal gate resistance as T_j indicator

The internal gate resistance can be used as an indicator of T_j in some IGBT and MOSFET chips, as the internal gate resistors are located in the centre of the die in those chips and this variable itself is temperature dependent. T_j can be estimated by measuring the value of internal gate resistance [49, 50].

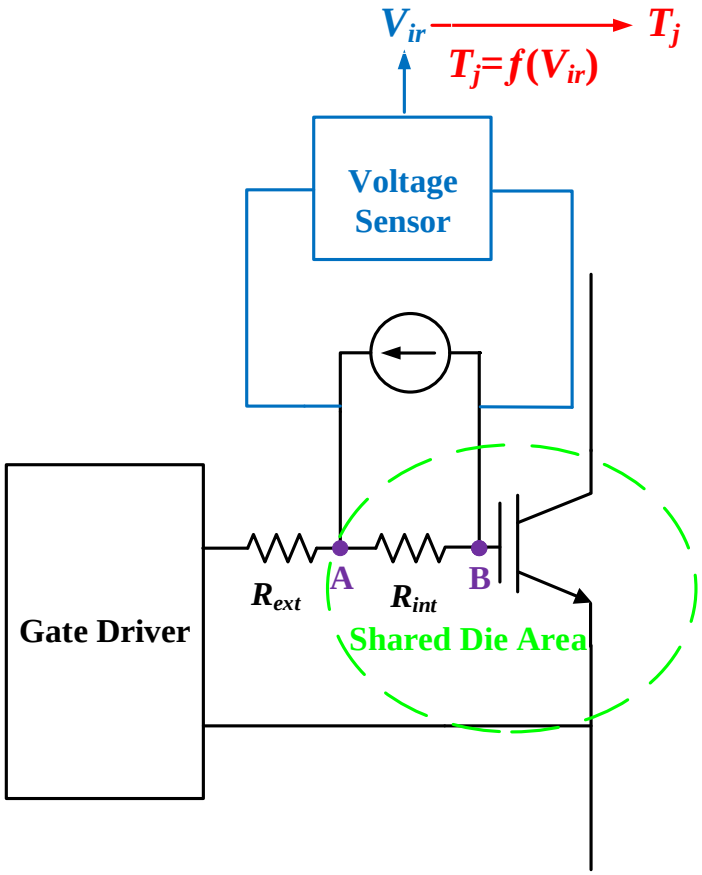


Figure 2. 8 Principal circuit for internal gate resistor measurement.

A principal circuit for online internal gate resistor measurement is presented in Figure 2.8, which is based on a previous study [49]. A constant measurement current is injected into the R_{int}, which results in a voltage drop (V_{ir}). The sensitivity of the measured voltage has been reported to be 0.75 mV/℃ when this technique was applied to 6.5 kV IGBTs [49].

There are concerns about applying this T_j measurement concept utilizing internal gate resistor. The first limitation is that, normally, point B in Figure 2.8 is not always accessible because it is actually part of the semiconductor structure. The second concern is that a voltage sensor with high resolution is required as the resistance changes only by several mΩ/℃. Measurements at larger voltages across the resistor are possible by injecting larger currents, but this would start to heat up the device. The last point of concern is that switching noise from the power module will interfere with the measurements as the voltage sensor must sit close to the die area [49].

2.4.2 Measurement of T_j during device on-state

Temperature dependent parameters during the device on-state have been developed to be a viable choice and have been proposed several times in the literature; for example, using the

base-emitter voltage V_{BE} in BJTs, the on-state voltage drop $V_{CE(on)}$ for IGBTs, and the on-state resistance $R_{DS(on)}$ for MOSFETs are typical thermal-dependent parameters that can be implemented as indicators of T_j [5].

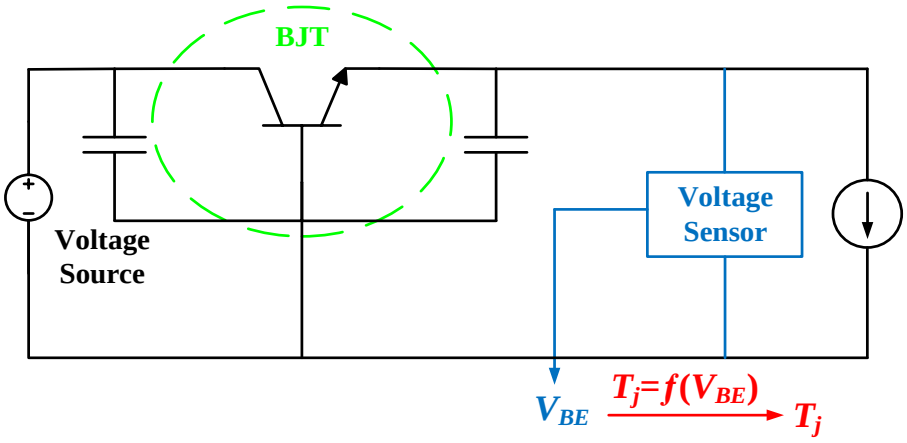


Figure 2. 9 Principal circuit for sensing base-emitter voltage for BJT.

In case of BJTs, T_j sensing can be achieved by the set-up shown in Figure 2.9, which can be only used in the laboratory environment to evaluate T_j but cannot be used during normal operation in a power converter. As indicated in Figure 2.9, a constant current is circulating between the BJT base and emitter which produces voltage V_{BE} which is used to estimate T_j. The test set-up was modified in order to be applied to achieve online sensing for BJTs [51].

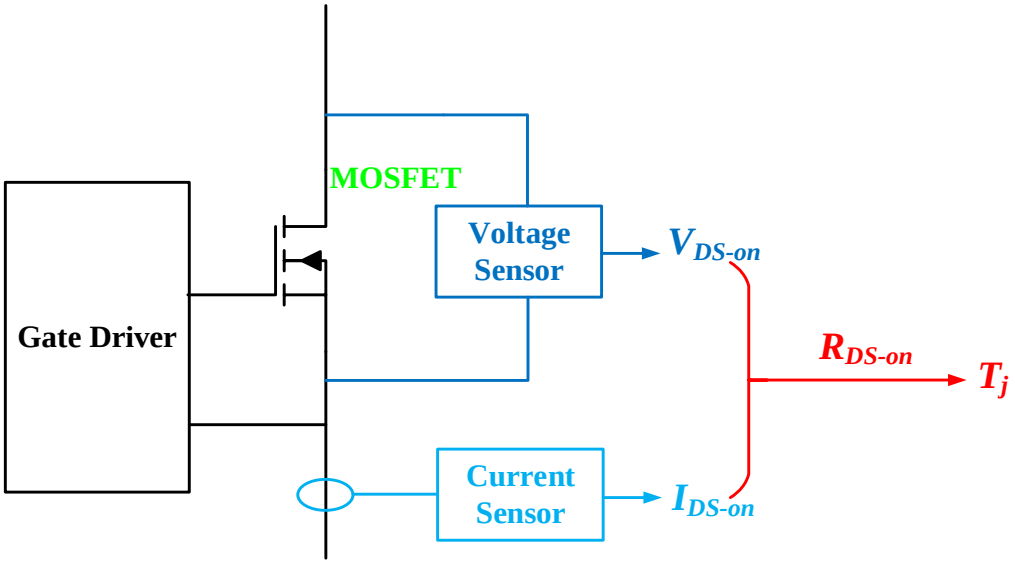


Figure 2. 10 Principal circuit for sensing the on-state resistor for MOSFET.

For power MOSFETs, the on-state resistance $R_{DS(on)}$ is a valuable TSEP [52]. The power MOSFET $R_{DS(on)}$ can be derived by measuring the on-state voltage $V_{DS(on)}$ and on-state current $I_{DS(on)}$ [53] at the same time, as shown in Figure 2.10. After the measurements, the on-state resistance can be calculated using Ohm's law (equation 2.1):

$$R_{DS(on)} = \frac{V_{DS(on)}}{I_{DS(on)}} \tag{2.1}$$

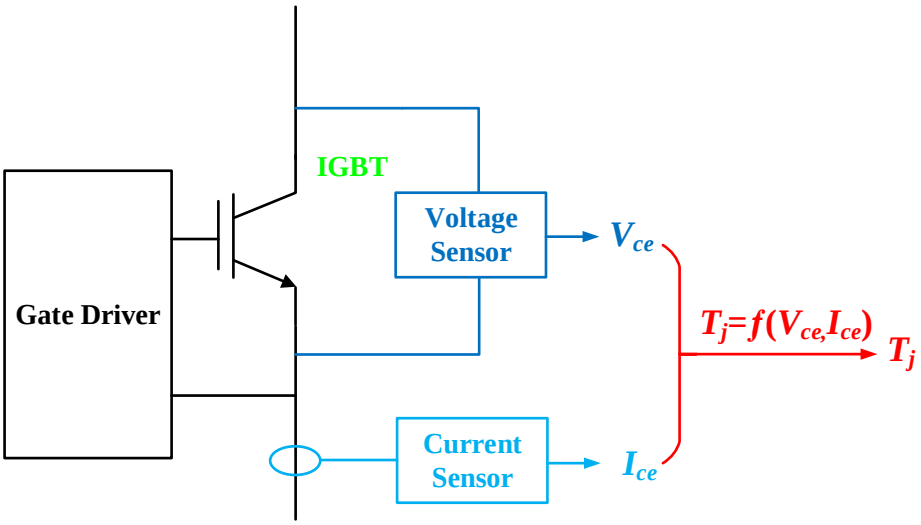


Figure 2. 11 Principal circuit for sensing on on-state voltage for IGBT

An important TSEP for IGBTs is the on-state collector-emitter voltage, V_{CE}, which has been extensively described in the literature [54, 55]. It is also necessary to synchronize the measurement to the collector-emitter current, I_{CE}, as V_{CE} is a function of current and T_j. Consequently, a current sensor is required too, as shown in Figure 2.11. The values of T_j of IGBT can be presented in a three-dimensional graph [55]. The temperature gradient of an IGBT chip has been investigated previously [56].

The aforementioned T_j sensing is based on the $R_{DS(on)}$ for power MOSFET and the V_{CE} for IGBT, it is required to measure both the voltage across the device during the on-state and the current flowing through it. The current flowing through the device can be directly measured at the phase level in many applications. Under these scenarios, it is crucial to determine the precise period of the device's forward conduction and to avoid the measurement of the commutation between the transistor and diode. Galvanic isolation is necessary for the voltage sensor, since it is directly connected to the power terminals of the MOSFET/IGBT. When the power electronic semiconductor is fully turned on, the voltage across the device is rather lower than 1V. However, when the switching device is completely turned off, the high DC voltage will be providing

directly across the device as well as the voltage sensor. Therefore, a floating voltage sensor is required with a strong voltage endurance ability and high resolution.

During the operation of the power converter, noise is generated which could interfere with the precision of the T_j estimation method based on on-state parameters. The sensitivity of the on-state voltage drop is usually only several $\mathrm{mV/°C}$, which is vulnerable to the influence of noise from the switching of the power semiconductor.

It is also important to accurately measure the on-state current for T_j estimation, utilizing on-state temperature-dependent parameters. For example, it is clearly shown in equation 2.1 that $R_{DS(on)}$ is directly linked to the on-state current, $I_{DS(on)}$, which means that any incorrect measurement of the current would induce error in estimating the real value of T_j. Other than the outside measurement limitation, there are some issues inside power semiconductor devices as well which might weaken the accuracy of measurement. The parasitic resistance of both the DBC and the bond wires would induce an extra voltage drop in addition to the on-state voltage drop of the device [56, 57]. An overestimation of T_j might result. This estimation error could be eliminated by establishing a detailed packaging module and calculating the influence of both DBC and bond wire parasitic [58]. Aged or the failure of the bond wires may cause the evaluation to be inaccurate when degradation appears [59].

The measurement of T_j based on on-state T_j-dependent parameters is applicable for simple converter topologies like buck/boost converters. For multi-switch converter topologies, multiple high-voltage and high-resolution voltage sensors need to be installed, which would increase the size of the converter system as well as the overall costs. As explained above, the voltage measurement circuit sits between the two power terminals of the power semiconductor, which might also face thermal-mechanical and electromagnetic interference issues.

One advantage of this method is that data processing is rather easy to implement by a simple digital computation of the measured on-state voltage and on-state current. The frequency of the on-state current (load current) is much lower than the switching frequency, which means that the on-state current can be seen as a constant within limited numbers of switching cycles. Under these circumstances, there is no need for high-bandwidth current measurement for the load current, and the T_j bandwidth will solely depend on the on-state voltage measurement bandwidth [60].

2.4.3 T_j measurement during device switching transient

The measurement of T_j during the semiconductor switching transients is an alternative solution in comparison to on-state T_j sensing. Basically, the device switching transients of device currents and voltages vary either in rising or falling time, amplitude or delay depending on the value of T_j and the TSEP parameter that is observed.

a. Switching transient methods based on time period

It is essential to implement accurate time counters to precisely measure a certain time period of a switching event. The IGBT Miller plateau width of the gate emitter voltage V_{GE} during the turn-off transient has been reported to be an indicator of the value of T_j [61]. As presented in a previous study [54],the relationship between the duration of Miller plateau and the IGBT T_j has been estimated. The principal circuit for this is depicted in Figure 2.12. The measured IGBT gate-emitter voltage during the turn-off period requires a threshold voltage detector in order to detect when the Miller plateau begins, and it requires a counter counting the length of time of the plateau. The sensitivity of the Miller plateau width can vary from 0.8 ns/°C to 3.4 ns/°C for different IGBT modules.

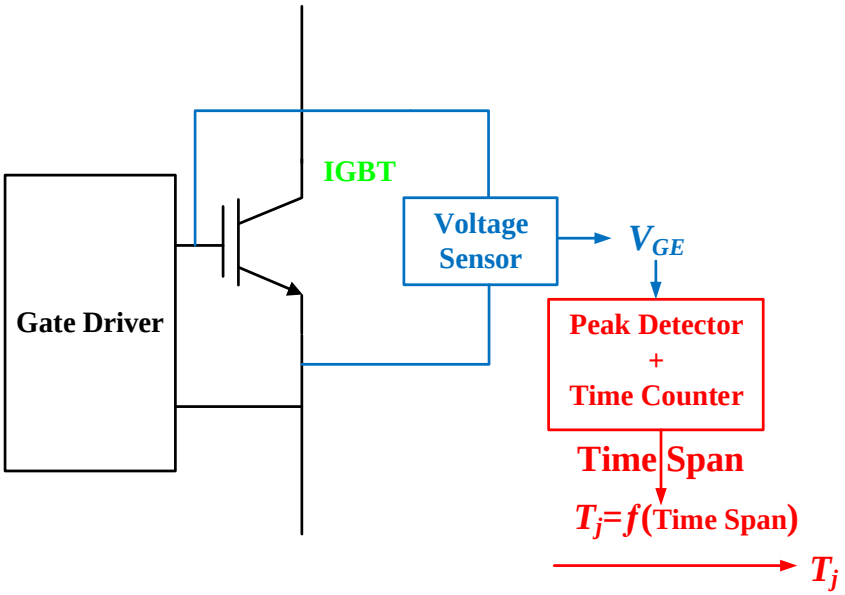


Figure 2. 12 Principal circuit for the detection of Miller plateau width during turn-off transient.

In the IGBT module, there are two emitters. One is the power emitter "E" and the other is the Kelvin emitter "e". The voltage between the two emitter terminals (V_{eE}) can also be used as an indicator of T_j [62]. Two spikes with amplitudes of 3 V and 5 V respectively appear during the IGBT turn-off transient in the V_{eE} [55]. It has been claimed that the time span (also referred as "V_{eE} delay time") between the two spikes is sensitive to T_j in the IGBT module [62, 63]. Figure 2.13 illustrates the principal measurement circuit for online measurement. The measured V_{eE} data is analysed by a pulse detector and a time counter and, as a result, the V_{eE} delay time can be determined. The variation in the V_{eE} delay is 8 ns/°C.

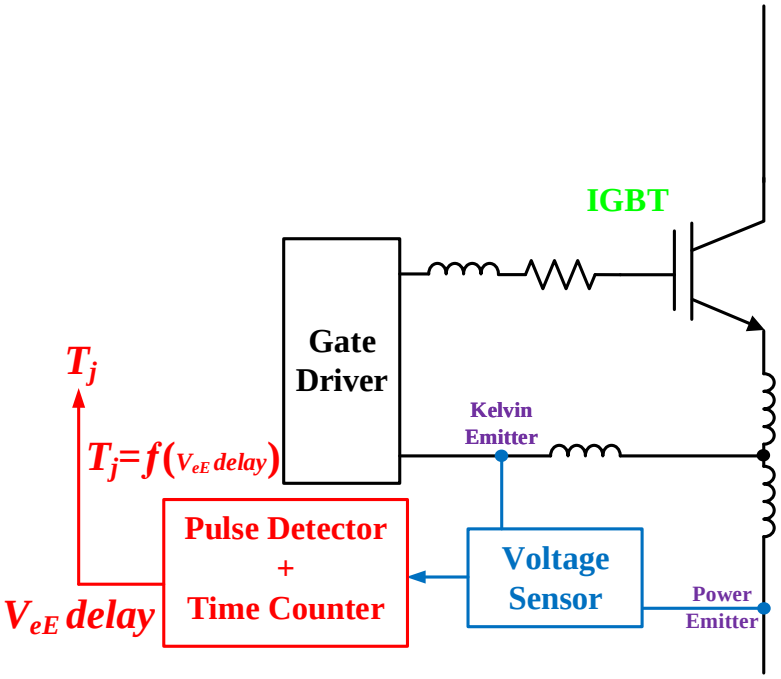


Figure 2. 13 Principal circuit to measure V_{eE} delay time.

The IGBT switching transient period during turn-on and turn-off are reported to both be sensitive to T_j [64, 65]. The turn-off time of the IGBT can be utilized to estimate the IGBT T_j online, and has been illustrated that with the increment in value of T_j, smaller dV_{CE}/dt and longer turn-off time can be detected [66, 67]. The principal measurement set-up is shown in Figure 2.13. By processing the V_{CE} data captured by the voltage using the threshold detector and time counter, the turn-off time of the IGBT can be extracted. The sensitivity of the IGBT turn-off time would change from 3 to 4 μs/°C depending on different values of DC bus voltage and load current [67].

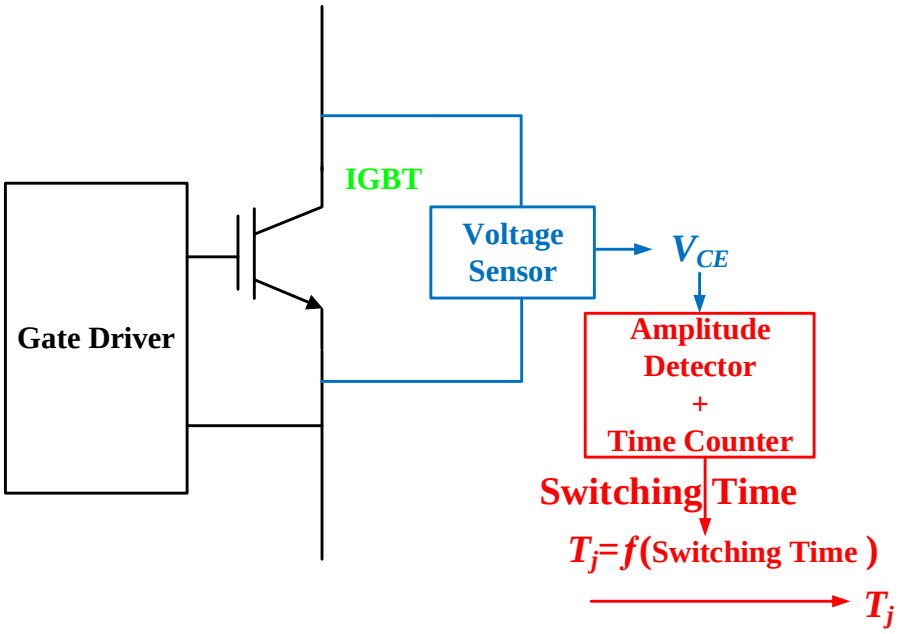


Figure 2. 14 Principal T_j measurement of the voltage switching times.

There are various requirements for these three aforementioned methods in order for them to be realized. Firstly, they require high bandwidth voltage comparators (1 GHz minimum), and secondly, they require high resolution time counters (1 ns/step). The measurement circuitry of the proposed Miller plateau method [61] can be integrated in the gate driver since it measures V_{GE}. According to another study [62], the V_{eE} delay time requires access to both the Kelvin emitter and power emitter, which means that the sensing circuitry must be located very close to the power module. Galvanic connection between the IGBT collector and emitter is necessary for the method to measure the switching times as proposed [67].

b. T_j measurement based on amplitude of temperature-sensitive electrical parameters

Measurement of the amplitude of specific voltages and currents as TSEPs have been reported for T_j [68]. For example, it has been claimed that the IGBT short-circuit current, I_{SC}, can be used to estimate T_j [61]. Results [68] have shown that the value of I_{SC} is not vulnerable to device voltage stress, gate drive voltage, or load condition. As shown in Figure 2.15, a short-circuit pulse is created to enable the measurement of I_{SC}. A sensitivity of 0.17%/°C has been reported [61]. The short circuit current can be measured by a current transducer, which is a non-intrusive

measurement. However, the downside of this is that frequent short-circuit pulse injection could accelerate device degradation which has also been pointed out [68].

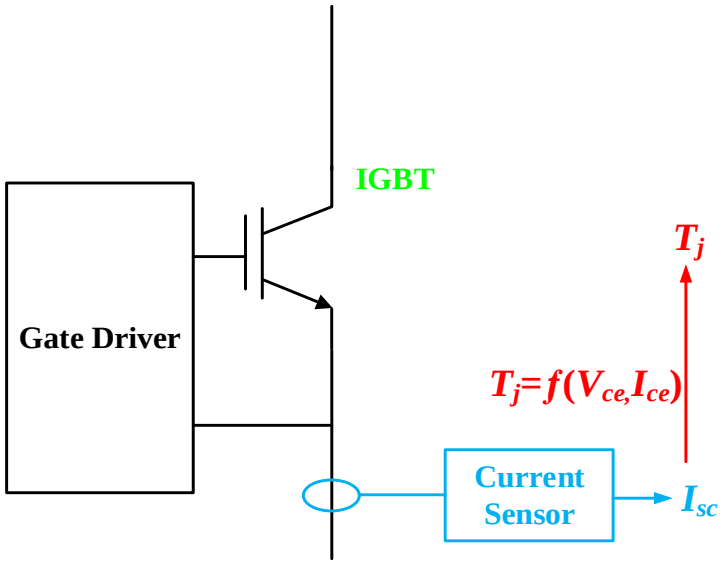


Figure 2. 15 Principal circuit for short-circuit T_j measurement.

The voltage between the Kelvin emitter and the power emitter V_{eE} has once again been proposed as a T_j measurement indicator [69]. Instead of investigating the V_{eE} delay time between two voltage pulses, the amplitude of the bigger pulse during the turn-off process has been studied [62]. As shown in Figure 2.16, the V_{eE} peak is measured by a peak detector and then correlated with the corresponding IGBT T_j.

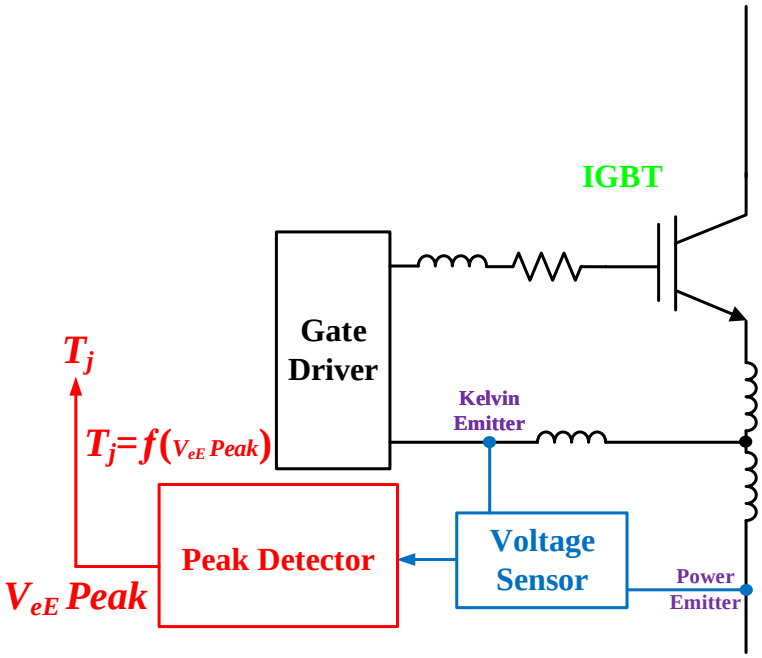


Figure 2. 16 Principal circuit for IGBT V_{eE} peak measurement.

The semiconductor T_j has been extracted depending on the gate voltage during the turn-on transient for MOSFETs [50] and IGBTs [70]. The gate threshold voltage, V_{TH}, has also been studied and implemented for online T_j sensing, and the experimental results show that the sensitivity of V_{TH} is 3 mV/°C. The principal measurement set-up is shown in Figure 2.17. Synchronized high-speed measurement circuitry is essential to accurately capture the turn-on transient of V_{GS} and the drain current. This is a significantly hard task to fulfil in order to successfully synchronize the voltage and current during the semiconductor turn-on transient. Alternatively, it has been claimed that the integration of the IGBT turn-on V_{GE} transient can be used as an indicator for T_j extraction [44], where the resolution of the integrated V_{GE} sensitivity is 84 mV/°C. This eliminates the requirement for synchronization, since only the gate-emitter voltage is measured, and the measurement circuit can be condensed into the gate driver circuit. The relevant measurement set-up is shown in Figure 2.18.

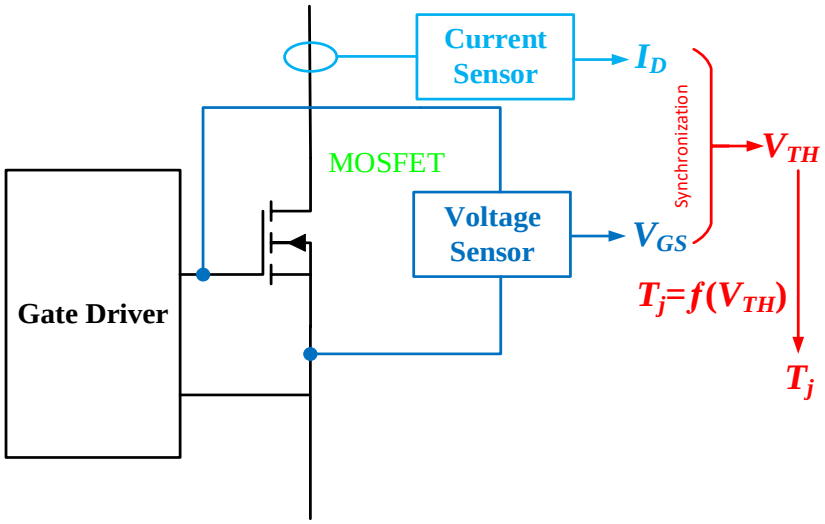


Figure 2. 17 Principle circuit for MOSFET V_{TH} measurement.

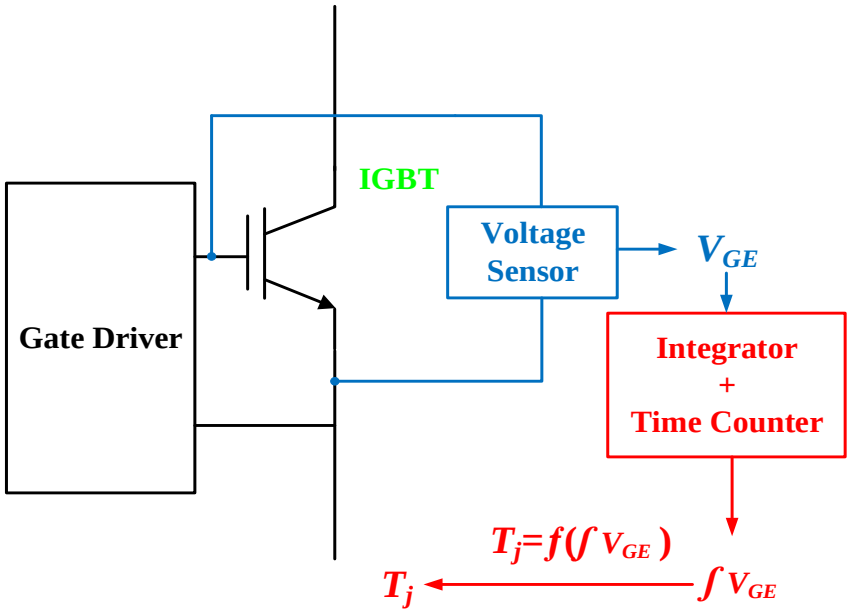


Figure 2. 18 Principle circuit of integration of V_{GE} measurement.

It is known that TSEPs can affect the dynamic characteristics of both the switching power electronic devices and their gate driver systems. This means that some of the gate driver output parameters can be dependent on T_j. For instance, the gate drive output current during the turn-on transient can be selected as an indicator of T_j for Si MOSFET [71], the Si IGBT [72] and the GaN HEMT [73]. The T_j measurement circuit can be integrated within the gate driver circuit and there will be no intrusive access needed for power semiconductors. The measurement circuits for the MOSFET gate current peak (I_{Gpeak}) and IGBT gate current integration ($\int I_{Gpeak}$) are illustrated in Figures 2.19 and Figure 2.20 respectively.

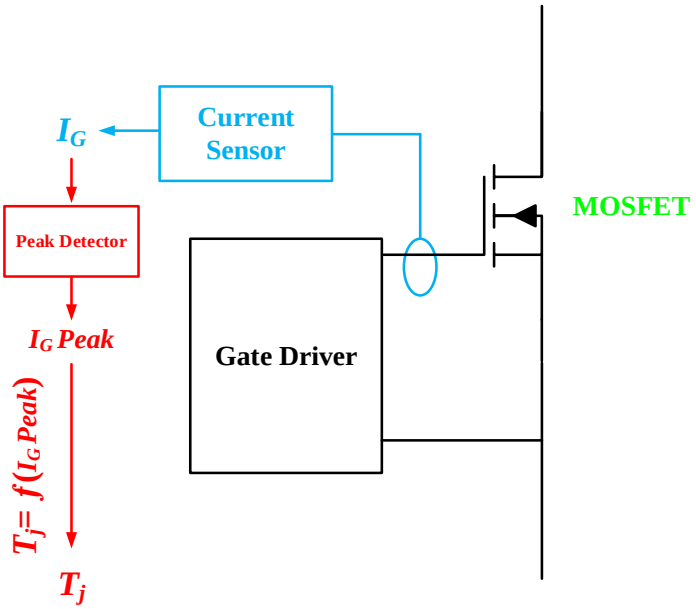


Figure 2. 19 Principle circuit for MOSFET I_{GPeak} measurement.

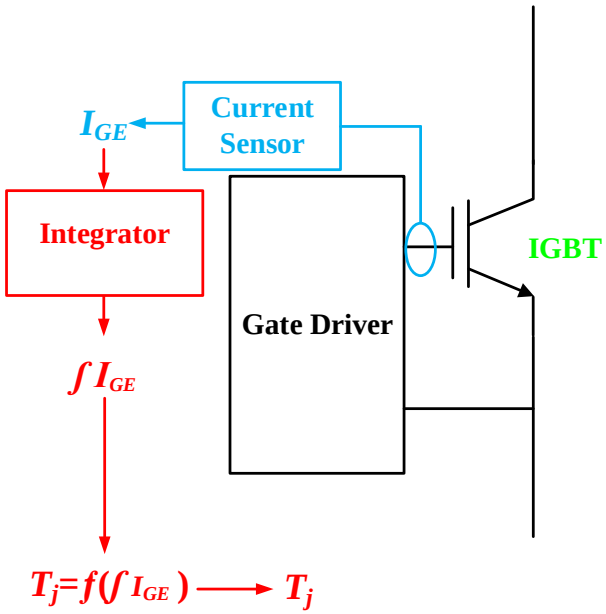


Figure 2. 20 Principle circuit for IGBT I_{GE} integration measurement.

2.4.4 Thermal model based T_j acquisition

Other than these TSEPs aforementioned in 2.3 and 2.4, knowledge of the thermal dynamic model and power dissipation of the semiconductor chip can be used to estimate T_j [74]. The switching losses and the conduction losses of the semiconductor form the total power dissipation. Individually, both types of losses vary during switching [75]. Establishing the device's thermal dynamic model can be useful in order to analyse power dissipation and consequently to estimate T_j [76]. A device T_j observer can be built for online T_j estimation by analysing the information concerning the semiconductor device's power dissipation with a properly built thermal dynamic model. There are basically two types of T_j observers: open-loop T_j and closed-loop T_j observers.

a. Methods based on an open-loop T_j observer

The voltage and current in conjunction with the T_j condition determine the switching losses of the power semiconductor [77]. The device's power losses P_{loss_k} need to be continuously updated based on the device voltage V_k as measured during the on-state and off-state, the current I_k flowing through the device, the duty ratio d_k of the switching cycle and the estimated value of T_j of the previous switching cycle, T_{j_k-1}. A cross-coupled model for power-dissipation based on T_j estimation is simplified and represented in equations 2.2 and 2.3:

$$P_{\mathrm{loss_k}} = F\left(V_k, I_k, d_{k,} T_{j_k-1}\right) \tag{2.2}$$

$$T_{\mathrm{j\_k}} = G\left(T_{j_k-1}, P_{loss\_k}\right) \tag{2.3}$$

where F is the device's loss model and G is its thermal dynamic model. It has been assumed here that ambient temperature and convection at the device surface do not vary [77]. The accuracy of the loss model F and the thermal dynamic model G would ultimately determine the precision of this method.

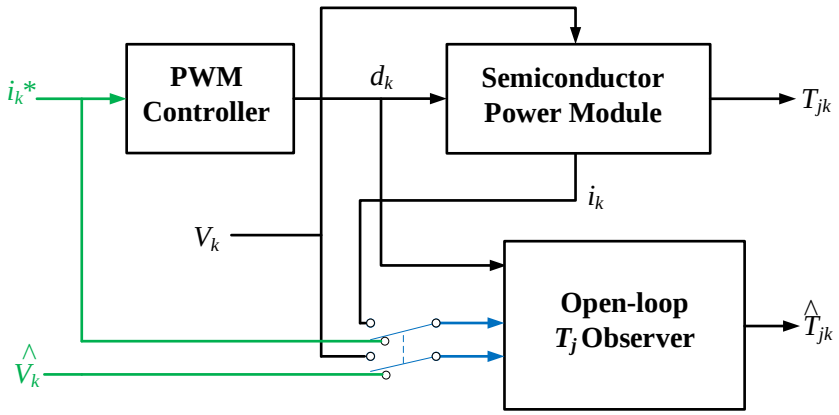


Figure 2. 21 T_j estimation based on an open-loop observer.

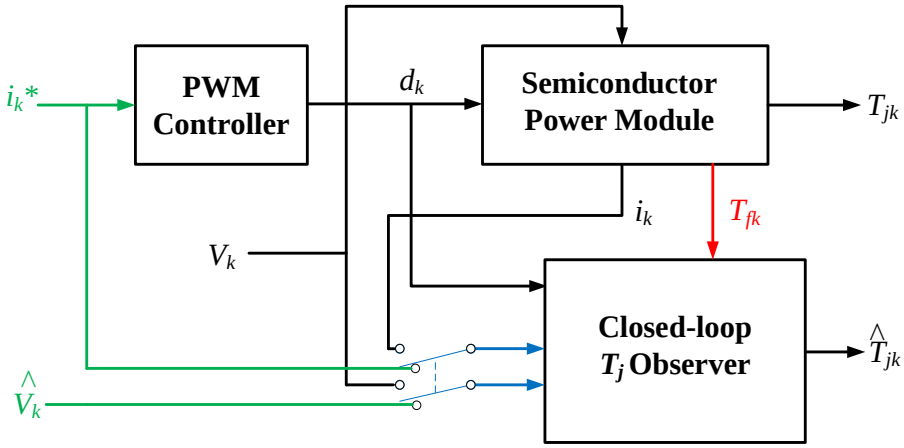


Figure 2. 22 T_j estimation based on a closed-loop observer.

The open-loop T_j observer can be established without measuring the device voltage, current, and duty ratio. Instead, as shown in Figure 2.21, reference values (with superscript *) and estimated values (with superscript ∧) are utilized in the loss model F as described in equation 2.4:

$$P_{\mathrm{loss_k}} = F\left(V_k^*, I_k^{\wedge}, d_k, T_{j_k-1}\right) \tag{2.4}$$

This method has been implemented in different topologies [70, 78] . Another study [67], the experiment has been conducted on a Mitsubishi Electric 2-in-1 IGBT module and the results show that the T_j error is around 2 °C and feedback is provided with a 2 ms delay.

The weakness of the open-loop observer method is that accuracy solely depends on the device loss model and the thermal dynamic model since there is no T_j feedback, and so the accuracy will be significantly affected by any thermal disturbance.

b. Method based on closed-loop T_j observer

As shown in Figure 2.22, the open-loop T_j observer can be optimized by imposing feedback signals from the power semiconductor; for example, as shown in equation 2.5, the module base-plate temperature, DBC temperature, and so on can be used as a feedback signal T_f.

$$T_{j\_k} = G\left(T_{j_k-1}, T_{f_k-1}, P_{loss\_k}\right) \tag{2.5}$$

An enhanced Luenburger style T_j observer which use the baseplate temperature as the feedback signal has been proposed and has been applied on a $1200\ \mathrm{V}/150\ \mathrm{A}$ Fuji IGBT [79]. The IGBT T_j was controlled within a $\pm 15\ ^{\circ}\mathrm{C}$ range of the desired temperature. The temperature feedback signal can be measured by using an isolated temperature sensor which will either be intrusive (DBC temperature sensor) and non-intrusive (base-plate temperature sensor).

The power loss model F is claimed to be influenced by device age [80, 81]. It has been shown [81], that the IGBT on-state voltage V_{CE} can be 13% bigger than the value when the device is healthy after 100,000 power cycles. For the open-loop T_j observer, this effect induced by degradation cannot be justified and consequently error would appear in estimating the value of T_j. In the case of a closed-loop observer, a feedback signal could be helpful in correcting the error.

2.5 Conclusion

In the beginning of this chapter, the physical and electrical behaviour of Si and SiC materials are compared. It shows that SiC-based power devices have lots of advantages over traditional Si-based power devices and enable SiC-based devices have the potential to replace Si-base devices in near future. It is important to monitor the T_j of SiC devices because they have the ability to be operated at much higher ambient temperature than Si devices. Thus, it is important to summarize the state-of-the-art methodologies that have been proposed to capture T_j online for power semiconductors. Additionally, principal measurement set-ups have been illustrated for each method. It has been concluded that for discrete SiC MOSFET, only indirect T_j

measurement methods could potentially be applied. In later chapter 4, preferred indirect T_j measurement methods which have been successfully applied to Si devices, especially methods that utilizing TSEP, will be used onto discrete SiC MOSFET in order to exam whether those methods can be employed on SiC-base devices or not.

Chapter 3 3D Thermal Model Establishment and FEM Thermal Simulation

The previous chapter summarized the physical and electrical behaviours of the SiC materials and highlighted the difference between the Si-based devices and SiC-based devices. It can be concluded that the SiC-based devices have better performance over the Si-based devices. SiC-based devices are becoming preferred for applications that require extremely high reliability, because the fact that the SiC device can be operated under much higher temperature and much harsher environment. Which means that it is important to supervise the health condition of the SiC-base devices. However, the literature review regarding the state-of-art junction temperature detection technique reveals that current techniques are not suitable for discrete SiC devices. Those techniques either need modification to the device itself which is not suitable for discrete device or they cannot be applied to SiC device due to SiC's unique physical and electrical attributes. Under this circumstance, it is viable to do further investigation in terms of the thermal behaviour of SiC MOSFET.

In this chapter, in order to further investigate the thermal behaviour and temperature distribution of the SiC MOSFET, a 3D thermal model of the C2M0080120D SiC MOSFET is established using Autodesk inventor.

3.1 Establishing 3D Thermal Model

The reason why it is important to investigate the thermal performance of the SiC MOSFET package is that this simulation could be helpful to precisely estimating the junction temperature rise induced by the combination of conduction losses and switching losses during operation. As a result, the true junction temperature can be derived to reduce the error of measured temperature which would influence the accuracy of the final collaboration.

The first step of building up a 3D model is to create the outer structure of the object under study. And it is crucial to using accurate data to construct the object. The SiC MOSFET is using TO247-3 package and the dimensions of the package has been presented in Fig 3.1 below provide by Wolfspeed[16].

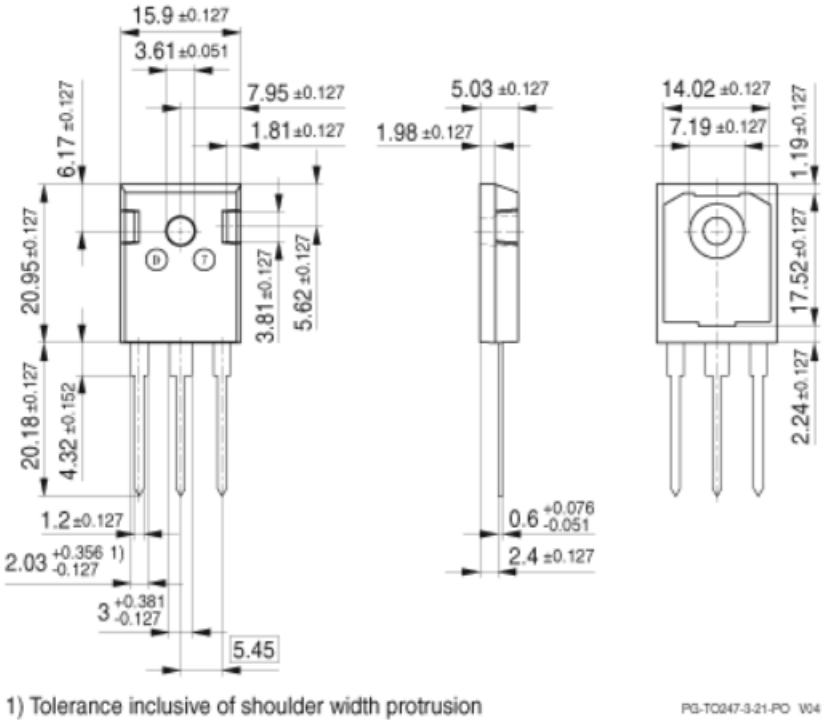


Figure 3. 1 TO247-3 Package outer dimension.

The second step is to create the inner content of the object. In this case, it is basically the inner bare die and the bond-wires. The dimension of the inner die can be found in the Wolfspeed C2M0080120D bare die datasheet as shown in Fig 3.2. The dimension information is also summarized in table 3.1.

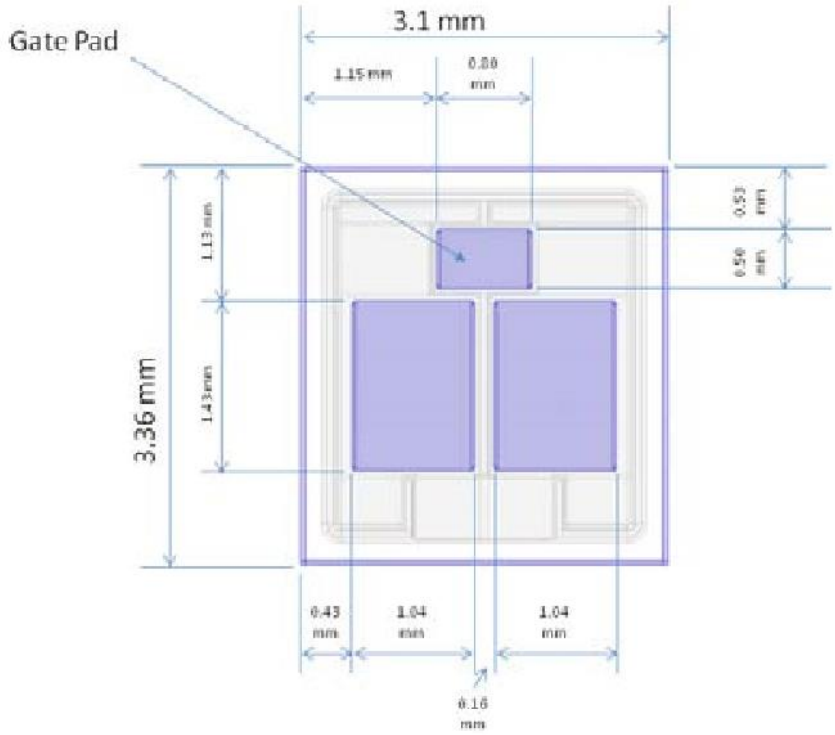


Figure 3. 2 C2M0080120D bare die dimension graph.

Table 3. 1 C2M0080120D bare die parameter and material of each components

Parameter	Typical Value	Unit
Die Dimensions (L x W)	3.10 × 3.36	mm
Exposed Source Pad Metal Dimensions (LxW) Each	1.04 × 1.43	mm
Gate Pad Dimensions (L x W)	0.80 × 0.50	mm
Die Thickness	180 ± 40	µm
Top Side Source metallization (Al)	4	µm
Top Side Gate metallization (Al)	4	µm
Bottom Drain metallization (Ni/Ag)	0.8 / 0.6	µm

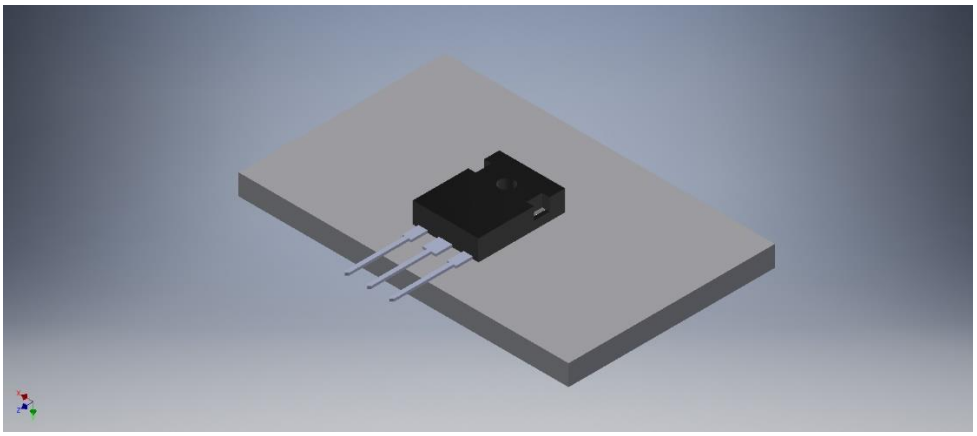
The final step is to assemble all the pieces created above with correct constrain condition and then allocate materials for each part of the object accordingly base on their attributions indicated in the datasheet. The bill of materials (BOM) is provided by the manufacturer.

The major difficulty of establishing the 3D model is the accuracy of the position of each component especially the exact position of the bare die. In this simulation process, the bare die

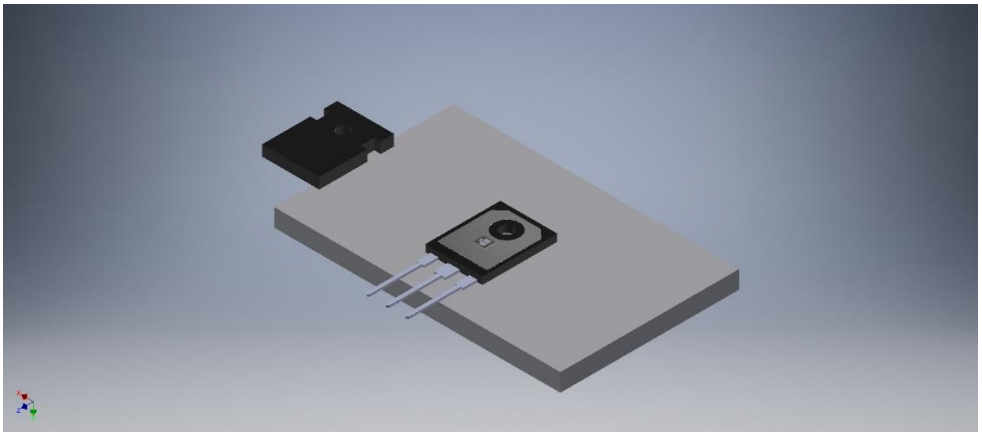
is assumed to be allocated at the centre of the TO-247-3 package. And the gate pad is sitting at the left of the bare die pad while the source pad and drain pad are located at the right-hand side of the bare die pad, which is a common arrangement for TO247-3 discrete MOSFET.

Figure 3.3 shows the established 3D model of C2M0080120D with a heat plate underneath it by using Autodesk inventor. Fig 3.3 (a) shows the full image of the SiC MOSFET with straight leads.

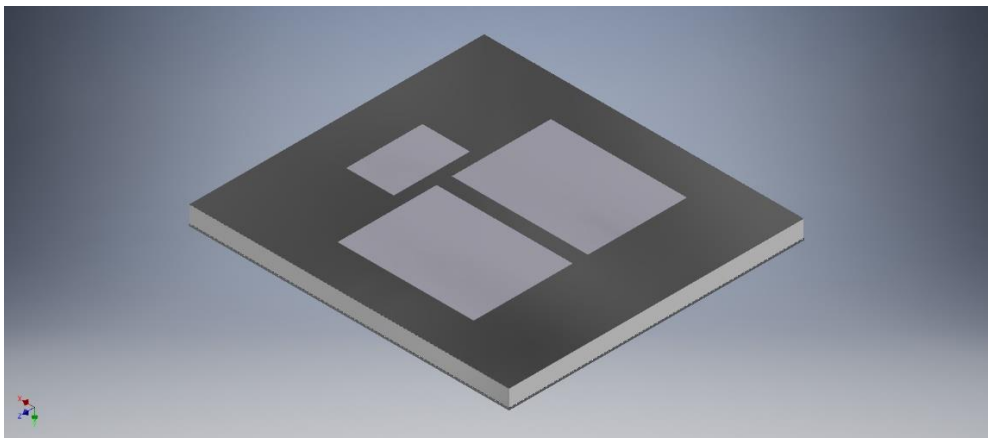
Fig 3.3 (b) presents the internal view of the SiC MOSFET when the top capsule is removed. It can be seen that the bare die is sitting at the middle of the package and the drain pad at the bottom of die is directly attached to the drain terminal metal. While the gate pad and two source pads are connected to the gate leads and sources leads respectively. At last, Fig 3(c) gives a close view of the bare die.



(a)



(b)



(c)

Figure 3. 3 3D thermal model of C2M0080120D SiC MOSFET with heat plate: (a) complete package model, (b) internal view with top capsule removed, (c) bare die model.

3.2 3D Model Internal Power Loss Calculation

In order to precisely evaluate the internal losses generated by the MOSFET junction. It is required to determine the total power losses of the MOSFET.

Power losses in the MOSFET of boost converter are basically due to the following contributors: 1. Conduction loss of MOSFET and 2. Turn on and turn off switching losses of MOSFET.

Conduction loss of MOSFET is due to the channel on state resistance or commonly known as R_{DSon}. R_{DSon} is dependent to the applied gate-source voltage (VGS) and the junction temperature as shown in the figure below from C2M0080120D datasheet[16].

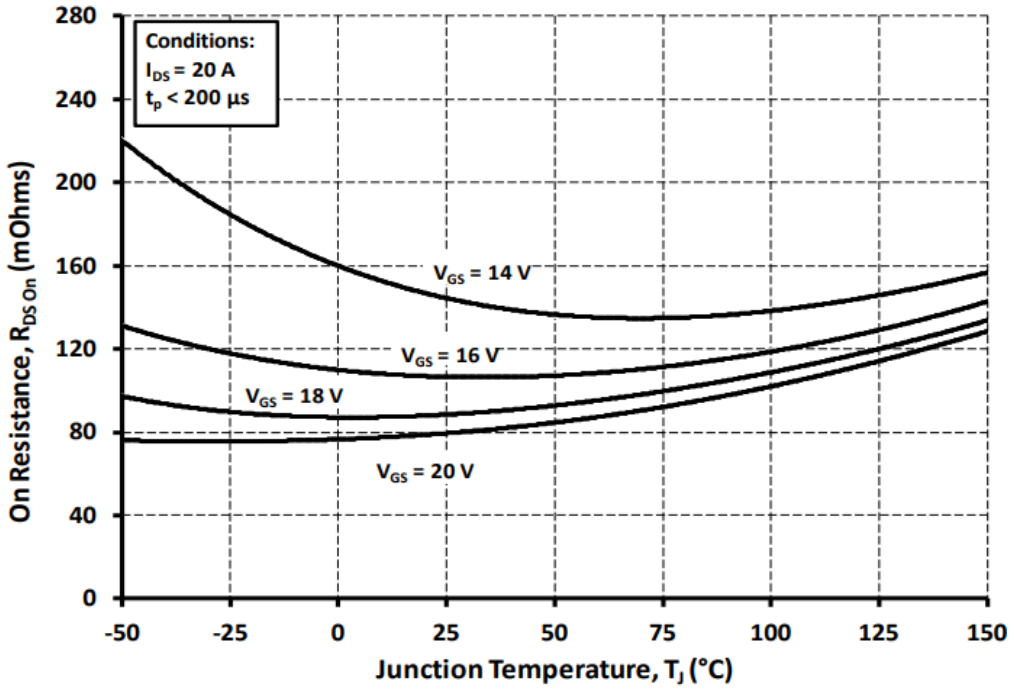


Figure 3. 4 On-Resistance VS. Temperature for different gate source voltages.

It can be interpreted from Fig 3.4 that with the increase of the gate source voltage (V_{GS}), the R_{DSon} reduces under each different operating temperature. To lower the conduction losses of the MOSFET, the manufacturer would recommend users to use optimal $V_{GS.}$ In case for C2M0080120D discrete SiC MOSFET, the recommended V_{GS} is 20 volts. At 20V V_{GS}, the R_{DSon} homogenously rise with the increment of temperature.

The conduction loss due to R_{DSon} can be calculated by equation listed below:

$$P_{\text{lossRDSon}} = {I_{Drain}}^2 \times R_{DSon} \tag{3.1}$$

Where I_{DRAIN} is the RMS drain current while R_{DSon} is the correct on-state resistance considering V_{GS} and corresponding junction temperature. R_{DSon} of the C2M0080120D SiC MOSFET at different T_j conditions are summarized in table 3.2 below.

Table 3. 2 On-state resistance at different junction temperature conditions.

Junction Temperature (°C)	On-state Resistance (mΩ)
25	109
50	111
75	116
100	120
125	129

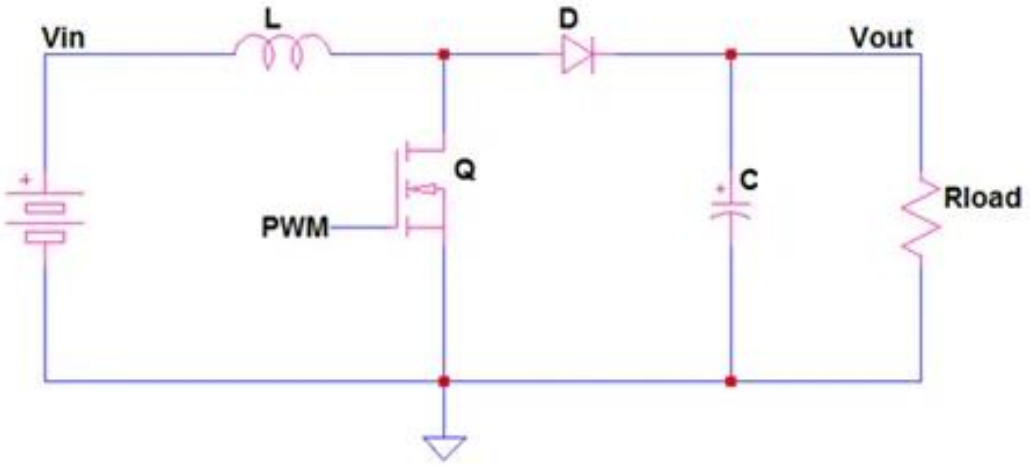


Figure 3. 5 Typical boost converter topology used for MOSFET power loss calculation.

Considering below boost circuit in Fig 3.5, the RMS drain current is can be computed using below equation:

$$I_{RMS_{FET}} = \frac{di\sqrt{D}}{\sqrt{3}} + \sqrt{D \times (I_{max} - di)^2} \tag{3.2}$$

Where

$$I_{max} = \frac{2 \times I_{out} + di \times (1-D)}{2 \times (1-D)} \tag{3.3}$$

$$di = \frac{D \times V_{in}}{L \times F_{sw}} \tag{3.4}$$

$$D = \frac{V_D - V_{in} + V_{out}}{V_D + V_{out} - V_S} \tag{3.5}$$

Where I_{out} is the DC load current of the boost converter, F_{sw} is the switching frequency of the MOSFET, di is the inductor current ripple, L represents the boost inductor, V_{in} is the input voltage, V_D is forward drop of the diode, V_S is the voltage drop of the MOSFET during on-state and V_{out} is the output voltage. The value of the passive components in Fig 3.5 has been summarized in Table 3.3 below.

Table 3. 3 Passive components summary of boost converter.

Passive Components	Value (Unit)
Boost Inductor (L)	75 (uH)
Input Capacitor (C_{in})	300 (uF)
Output Capacitor (C_{out})	600 (uF)
Load Resistor (R)	30-300 (Ω)

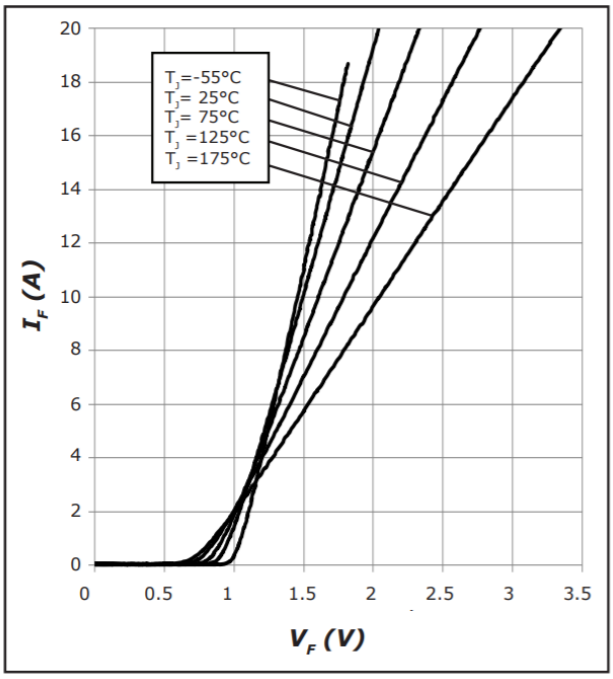


Figure 3. 6 Forward characteristics of Cree/Wolfspeed C4D20120D SiC Schottky diode.

The diode used in the boost converter is Cree/Wolfspeed C4D20120D SiC Schottky diode and its forward characteristics graph is shown in Fig 3.6. The forward voltage of the diode can be derived by measuring the diode current and corresponding junction temperature of the SiC Schottky diode. Then the value can be put into the equation 5 to calculate the duty cycle with measured input and output voltage values of the boost converter. Assuming the maximum current seen by the diode is 3A, then the forward voltage drop of the diode can be derived from Fig 3.6. The results are summarized in table 3.4 below.

Table 3. 4 SiC Schottky diode forward voltage drop at different junction temperatures.

Diode Temperature (°C)	Forward Voltage Drop (V)
25	1.09
50	1.08
75	1.08
100	1.07
125	1.07

There is an interesting point need to be addressed is that forward characteristic of the SiC Schottky diode (C4D20120D) used in the calculation presents a knee area. It means that when the forward current is lower than about 6A the forward voltage drop shows a decreasing trend when the junction temperature of the diode increase. While when the forward current is higher than 6A, the forward voltage-drop of the SiC Schottky diode present an opposite behaviour that with the increasing of the junction temperature the forward voltage drop increase.

The voltage-drop of the SiC MOSFET during turn-on can be also determined by looking up the datasheet graph. Under 3A drain-source current condition, the V_S is 0.275V. Other input parameters are listed below: the input voltage is 15V, the output voltage is 50V and the switching frequency of the SiC MOSFET is 20KHz. Assign all the input parameters into equation (3.5), and then the duty cycle D can be calculated to be 71%. The inductor current ripple can be also calculated by substituting values in equation (3.4) and the result is 7.1A. The output resistance is tuned to be 100ohm during the test, thus the output current can be derived as 50V/100ohm equals to 0.5A. By substituting values of I_{out}, di and D into equation (3.3), the maximum current can be determined and result for I_{max} is 5.27A. The next step is assigning all calculated results in equation (3.2), the RMS current can be found, and it equals to 3.75A. Finally, the conduction loss can be computed using equation (3.1). The result of conduction loss is summarized as below: under 25°C junction temperature condition and 3.75A RMS drain current, the conduction loss is 1.53W; under 50°C junction temperature condition and 3.75A RMS drain current, the conduction loss is 1.56W; under 75°C junction temperature condition and 3.75A RMS drain current, the conduction loss is 1.63W; under 100°C junction temperature condition and 3.75A RMS drain current, the conduction loss is 1.69W and under 100°C junction temperature condition and 3.75A RMS drain current, the conduction loss is 1.82W.

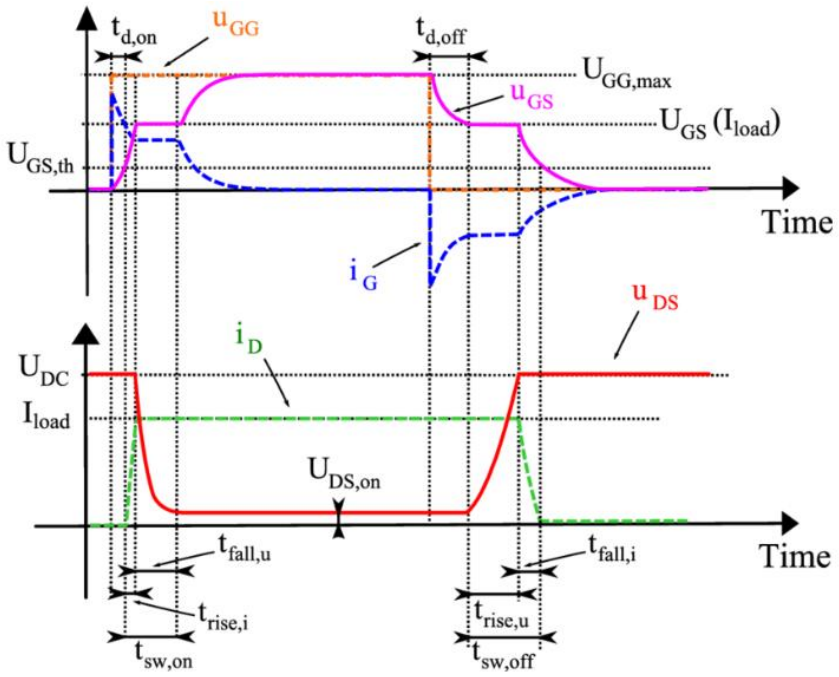


Figure 3. 7 Typical characteristics of power MOSFET switching transients.

Switching losses of MOSFET during turn on and turn off are associated with the rise and fall time of the MOSFET. Switching time measurement circuit and input/output waveform are shown below in Fig 3.7.

Where $t_{d(on)}$ is turn-on delay time: the time from when the gate-source voltage rises above 10% of V_{GS} until the drain-source voltage reaches 90% of V_{DS}, t_r is the rise time: the time taken for the drain-source voltage to fall from 90% to 10% of V_{DS}, $t_{sw,on}$ is the turn-on time: the turn-on time is equal to $t_{d(on)}+t_r$. While $t_{d(off)}$ is turn-off delay time: the time from when the gate-source voltage drops below 90% of V_{GS} until the drain-source voltage reaches 10% of V_{DS}, t_f is the fall time: the time taken for the drain-source voltage to rise from 10% to 90% of V_{DS} and $t_{sw,off}$ is turn-off time: the turn-off time is equal to $t_{d(off)}+ t_f$.

The information of t_r and t_f of C2M0080120D SiC MOSFET is summarized in Table 3.5 as below.

Table 3.5 turn-on time and turn-off time of C2M0080120D

Symbol	Symbol Parameter	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	-	11	-	ns
t_r	Rise time	-	20	-	
$t_{f(on)}$	Turn-off delay time	-	23	-	
t_f	Fall time	-	19	-	

The switching losses of SiC MOSFET can be approximated by using the below equation:

$$P_{\text{loss\_switching}} = \frac{1}{2} \times (t_r + t_f) \times I_{RMS\_FET} \times V_{DS} \times F_{sw} \quad (3.6)$$

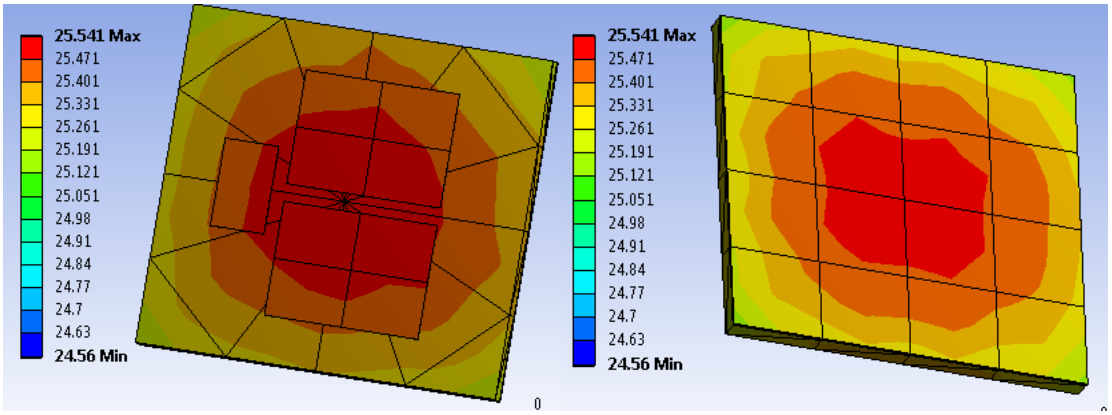
Where t_r is the rise time, t_f is the fall time, I_{RMS_FET} is the RMS current of the MOSFET, V_{DS} is the drain source voltage of the MOSFET and finally F_{sw} is the switching frequency.

The total switching loss of the SiC MOSFET under 3.75A RMS current can be derived by substituting all relevant parameters into equation (3.6). The total switching loss is 0.02W

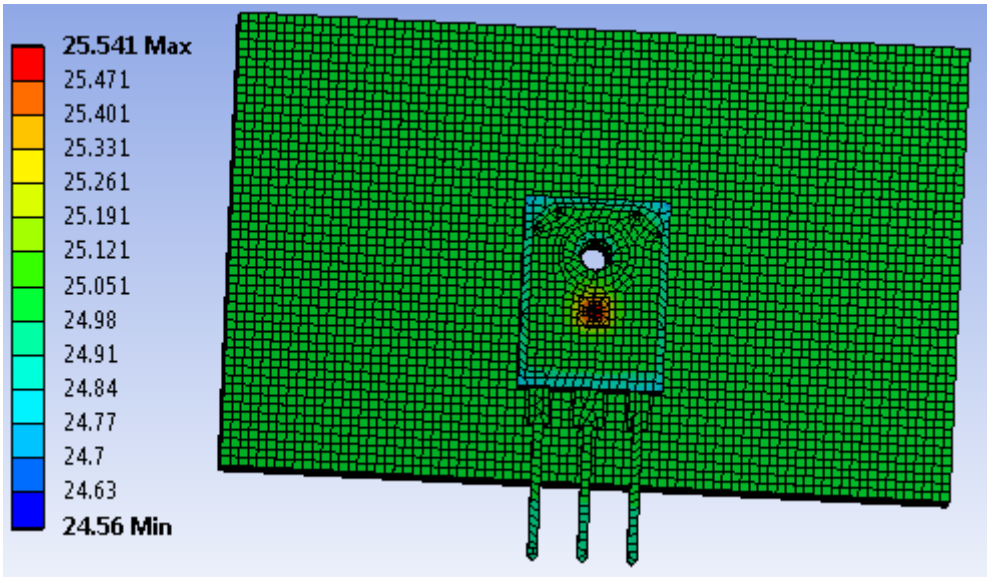
The total losses produced by the MOSFET is the sum of the total loss and the switching losses. The total losses are listed here: under 25°C junction temperature condition and 3.75A RMS drain current, the total loss is 1.55W; under 50°C junction temperature condition and 3.75A RMS drain current, the total loss is 1.58W; under 75°C junction temperature condition and 3.75A RMS drain current, the total loss is 1.65W; under 100°C junction temperature condition and 3.75A RMS drain current, the total loss is 1.71W and under 125°C junction temperature condition and 3.75A RMS drain current, the total loss is 1.84W.

After deriving the total losses of the SiC MOSFET, the value can be used to determine the internal heat generation of the SiC MOSFET junction. The volume of the die body is imported into Ansys (a 3D finite element analysis software), and it is calculated to be 1.9×10^{-9} m^3. Finally, the magnitude of internal heat generation can be derived as 0.82×10^9 W/m^3 at 25°C, 0.83×10^9 W/m^3 at 50°C, 0.87×10^9 W/m^3 at 75°C, 0.9×10^9 W/m^3 at 100°C and 0.97×10^9 W/m^3 at 125°C. Those internal heat generation parameters can be imported as the input for the junction temperature increment estimation. The results of the 3D thermal finite element analysis will be presented at 5 different temperatures which will be used as temperature setup for the practical experiments as well. The results of 3D simulation and practical work will be correlated in the experimental test chapter.

3.3 Finite Element Analysis of the 3D SiC MOSFET Model



(a) (b)



(c)

Figure 3. 8 Temperature distribution of SiC MOSFET sitting on voltage-controlled heat plate (25°C): (a). SiC die body temperature distribution; (b). SiC die body back temperature distribution; (c). Chip and heat plate temperature distribution when the top package is hided.

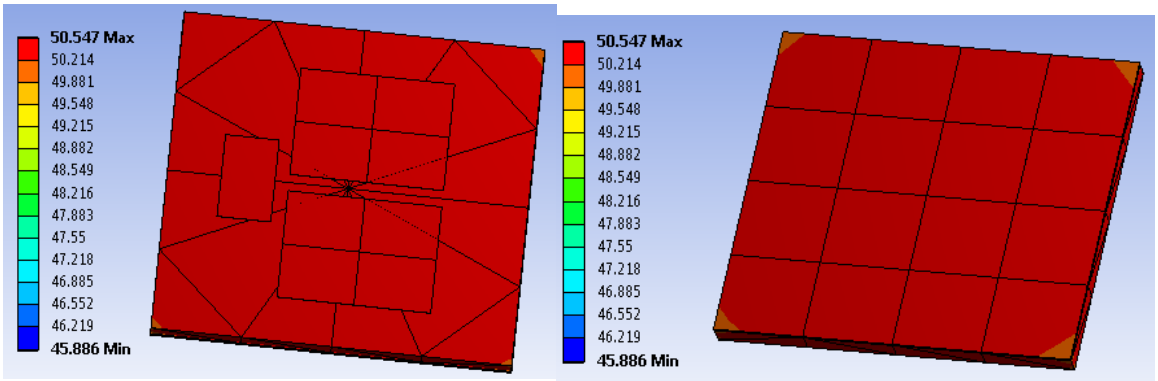
Figure 3.8 presents the temperature distribution of a discrete SiC MOSFET sitting on a voltage-controlled heat plate when the initial temperature of the heat plate is controlled at 25°C. And the internal heat generation of the SiC body die is calculated in the previous sections is used as the input. And it is assumed that the chip has reached thermal equilibrium with the heat plate which under this situation is 25°C. As can be seen from Figure 3.8 (a) and (b), the centre temperature of the die is the highest to be 25.541°C, there is 0.541°C temperature increment as a result of both the effects from the internal power loss and three types of heat transfer which are conduction, convection and radiation. The lowest temperature appears at the peripheral of

the SiC MOSFET due to big convection area and most heats are transferred to heat plate due to the fact that drain pad has much lower thermal impedance which provides an ideal thermal path for the power dissipation generated. The most important purpose of conducting this thermal analysis is to estimate the temperature difference between the hottest spot and the surface of the SiC MOSFET. It is because during the experimental test, the temperature can be only measured from the surface of the SiC MOSFET since it is not viable to access to the inner part of the SiC MOSFET. In fact, it can be found that the drain pad of the SiC MOSFET is thermal equilibrium with the heat plate. It is viable to measure the case temperature using thermal meter and then calibrate it with the 3D thermal simulation to estimate the real junction temperature. In this way, the error between the real T_j and measured value will be minimized.

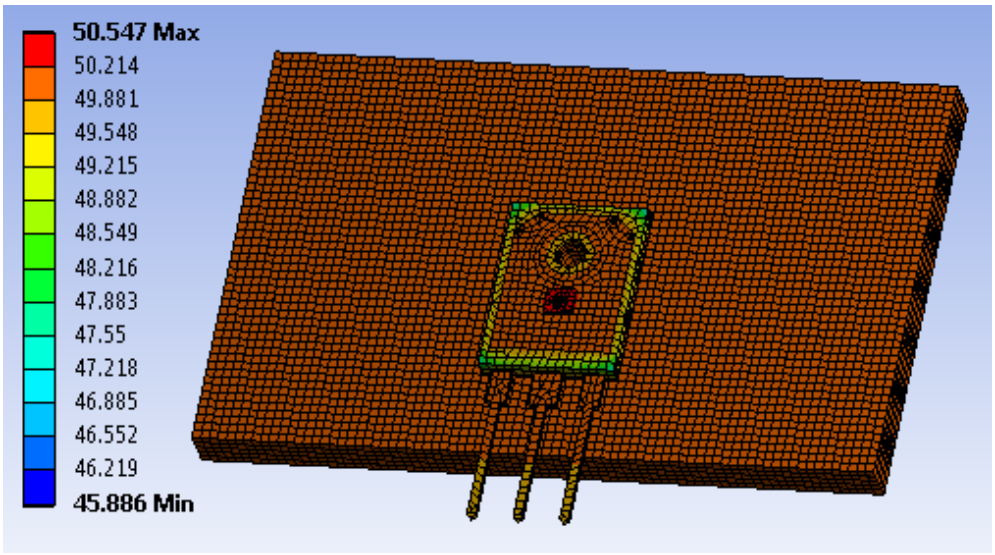
It is also important to notice that the internal power dissipation generated by the die body is increasing with the temperature of the heat plate. Because when the chip reaches thermal equilibrium with the heat plate before operating and generating any losses the parameters that influencing the power dissipation will change, for instance the body diode forward voltage and the on-state resistance which contributes the conduction loss. Thus, the internal heat generation will be assigned accordingly with the calculation results conducted previously to get precise T_j at each temperature steps will be tested in the practical experiments.

The detailed temperature distribution of the discrete SiC MOSFET die body and the whole chip with heat plate under 50°C initial heat plate temperature condition is presented in Figure 3.9. As the internal heat generation increases, it can be found the real T_j of the SiC MOSFET is 50.547°C and the temperature-rise is 0.547°C which is slightly higher than the temperature-rise under 25°C condition which matches the calculation results.

It is also can be noticed that the die body temperature is almost evenly distributed as shown in Figure 3.9 (a) and (b), only the temperature at four small corners of the die body is marginally lower. Similarly, the peripheral temperature of the SiC MOSFET is lower than the bottom drain pad and temperature approaching four corners of the SiC MOSFET is reducing as shown in Figure 3.9 (c). The four corners are proved not to ideal spots for measuring the case temperature, because there is temperature difference between the heat plate and those four corners.



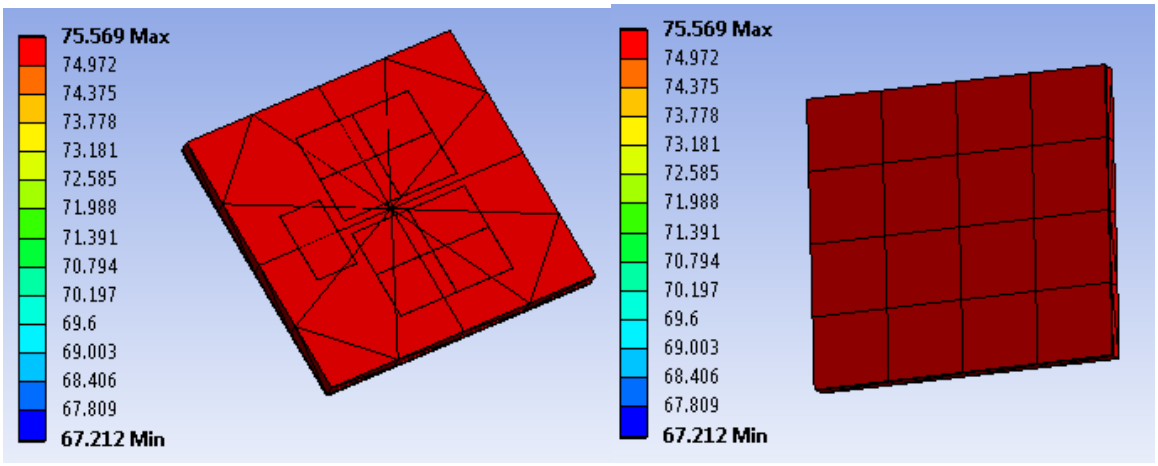
(a) (b)



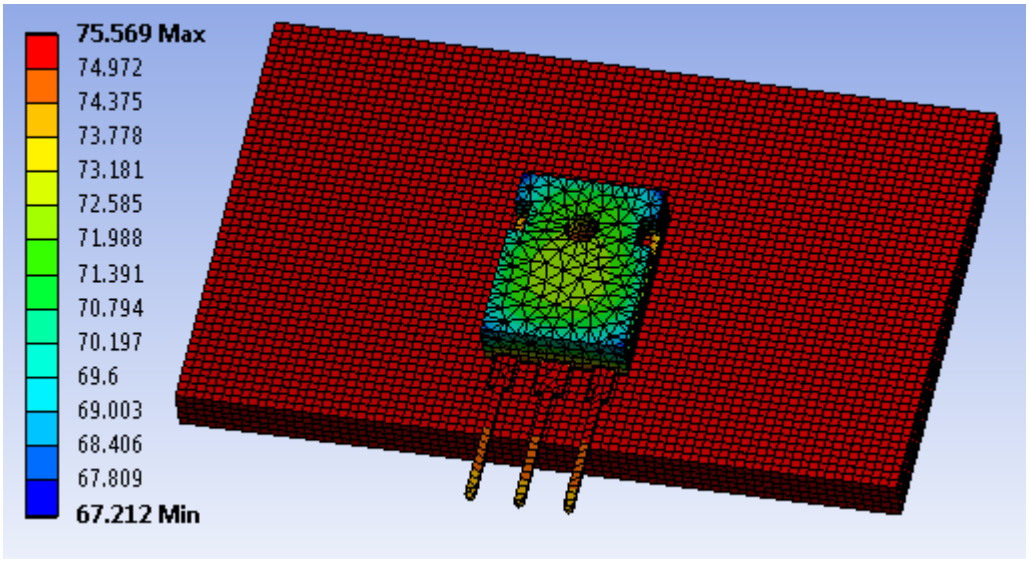
(c)

Figure 3. 9 Temperature distribution of SiC MOSFET sitting on voltage-controlled heat plate (50°C): (a). SiC die body temperature distribution; (b). SiC die body back temperature distribution; (c). Chip and heat plate temperature distribution when the top package is hided.

The die body top and bottom temperature distributions are presented in Figure 3.10 (a) and (b). It is worthy to notice that the whole die body reaches temperature equivalent under 75°C heat plate initial temperature condition and under thermal equilibrium between the SiC MOSFET and the heat plate. And Figure 3.10 (c) shows the top case temperature distribution of the SiC MOSFET. It is clearly indicated that the temperature of the whole top case temperature is lower than the heat plate due to the large convection area of the top case while the temperature decrease gradually from the centre part where the internal heat is generating beneath the case to surrounding cases edges where no extra heat is generated. Which again support the theory that only bottom drain pad temperature is the closed to the hottest die body temperature.



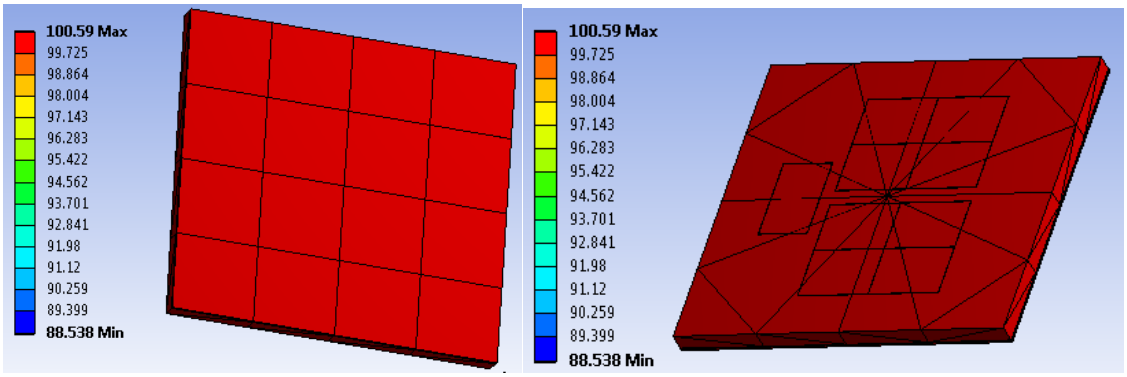
(a) (b)



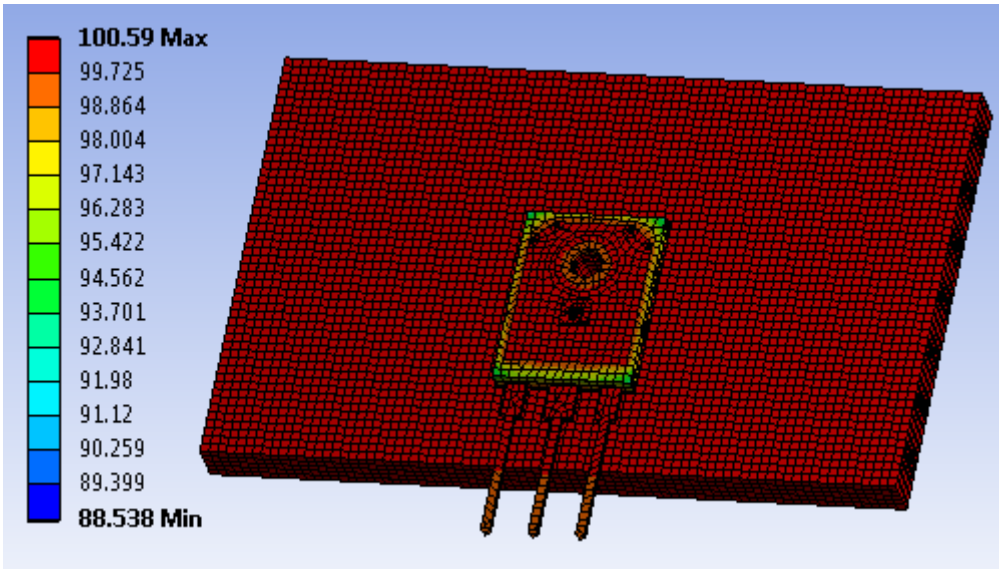
(c)

Figure 3. 10 Temperature distribution of SiC MOSFET sitting on voltage-controlled heat plate (75°C): (a). SiC die body temperature distribution; (b). SiC die body back temperature distribution; (c). Chip and heat plate temperature distribution when the top package is hided.

For the last two sets of 3D thermal simulation, the temperature rise of the die body is 0.59°C and 0.63°C respectively for 100°C and 125°C initial heat plate temperature conditions as being illustrated in Figure 3.11 and Figure 3.12 respectively. And the temperature distributions are almost the same with the 75°C initial heat plate temperature conditions.

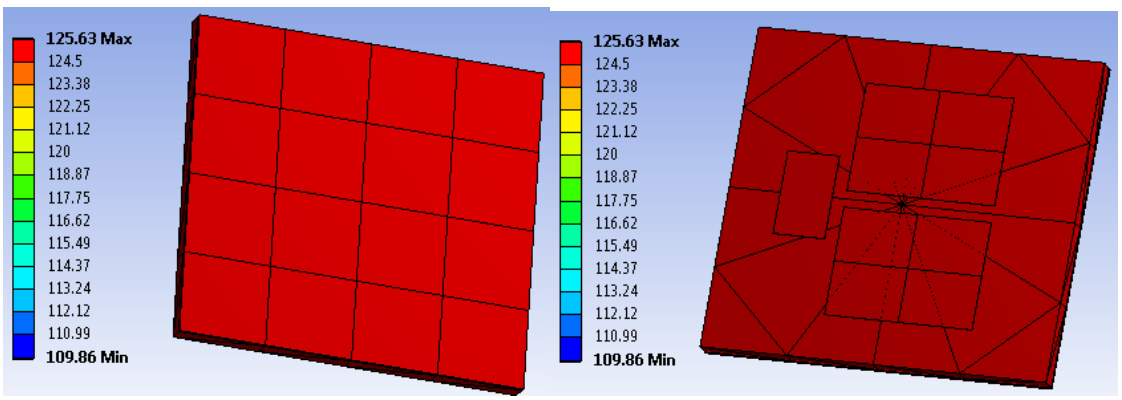


(a) (b)

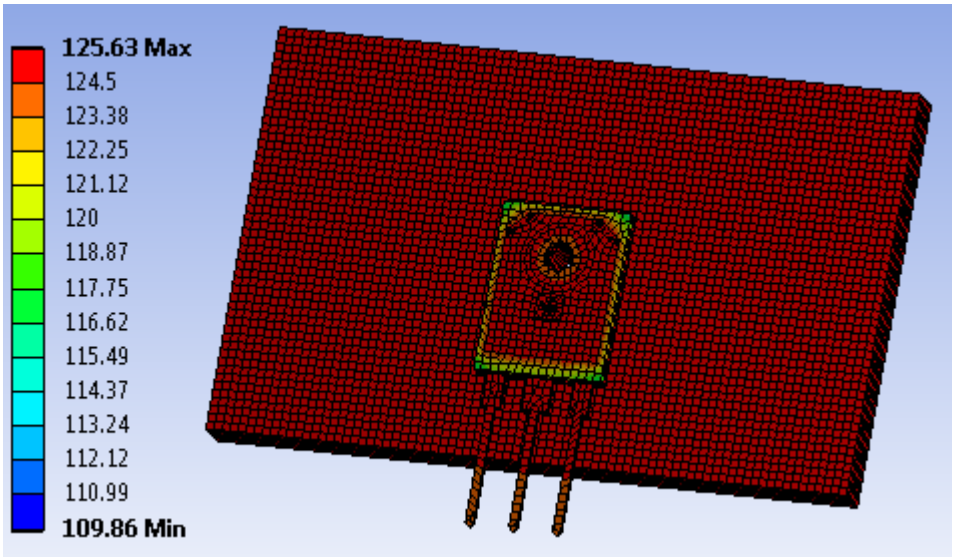


(c)

Figure 3. 11 Temperature distribution of SiC MOSFET sitting on voltage-controlled heat plate (100°C): (a). SiC die body temperature distribution; (b). SiC die body back temperature distribution; (c). Chip and heat plate temperature distribution when the top package is hided.



(a) (b)



(c)

Figure 3. 12 Temperature distribution of SiC MOSFET sitting on voltage-controlled heat plate (125°C): (a). SiC die body temperature distribution; (b). SiC die body back temperature distribution; (c). Chip and heat plate temperature distribution when the top package is hided.

3.4 Conclusion

In this chapter, a 3D model of the Cree/Wolfspeed C2M0080120D has been established using Autodesk Inventor 3D software. The 3D model is produced based on the SiC MOSFET datasheet and instructions of the TO-247-3 packaging. The established 3D model is then imported into ANSYS finite element analysis software where corresponding materials of each components of the SiC MOSFET are assigned accordingly. To emulate the die body power losses generated during its operation, internal heat loss model is established in the simulation and the amount of power losses are determined to distinguish different temperature rise under various initial temperature conditions. It is determined that the bottom drain pad is the most suitable position to measure the case temperature and the real T_j can be derived by adding the die body temperature rise produced by its power losses. Further investigations will be carried over in later experiment chapter.

Chapter 4: Small signal modelling of SiC MOSFETs

In the beginning of this chapter, traditional TSEPs for Si devices have been simulated to examine whether these methods can be applied to SiC MOSFET which turns out to be not a way out for SiC MOSFET. Under this circumstance, it is crucial to propose new method to precisely estimate T_j of SiC MOSFET. Following the simulation results, a small AC signal injection method is proposed, and corresponding equivalent circuit is presented. The proposed equivalent circuit is also verified via experimental test.

4.1 TSEP simulation in the SiC MOSFET

Traditional TESPs applied to Si devices have been proven not quite suitable for SiC power devices. The main reason why traditional TSEPs fail to produce good results is that SiC is a material that is less temperature-dependent and has a lower reverse recovery peak current and a much faster rates of current and voltage change during the turn-on and turn-off process. Figure 4.1.1 shows results highlighting some differences in the behaviour of electrical parameters during T_j changing in Si and SiC devices [15]. Figure 4.1.1 (a), shows the normalized $R_{DS(on)}$ for the SiC MOSFET, Si MOSFET and COOLMOS. Both the Si MOSFET and COOLMOS show good linearity, with a temperature resolution of around 1 $\mathrm{m\Omega/°C}$ which is a reasonable value as a TSEP [82]. However, the normalized $R_{DS(on)}$ of the 1st generation SiC MOSFETs is not linear and has opposite temperature changing direction depending on the T_j value. Here, when the value of T_j is lower than around 75 °C the normalized $R_{DS(on)}$ presents negative T_j dependency, but when T_j becomes greater than 75 °C the normalized $R_{DS(on)}$ becomes positively dependent on T_j. Furthermore, the 2nd generation of SiC MOSFETs, which is the latest technology, show unified T_j dependency, but the even lower sensitivity makes it hard to be utilized like in case of Si MOSFET. Clearly, as summarized, the $R_{DS(on)}$ is not applicable for implementation as a TSEP for SiC MOSFETs. The diode technology for both Si and SiC materials are also compared in Figures 4.1.1(b) and (c), showing the difference in the turn-off process of a Si PIN diode and a SiC Schottky diode [15]. In case of the Si PiN diode, the reverse recovery current peak (I_{PEAK}) and reverse recovery current slope (dI/dt) increase along with increments of in T_j. Both parameters can be measured and used as indicators of T_j. However, for the SiC Schottky diode there is no visible change in I_{PEAK} and dI/dt at different values of T_j [15]. Figures 4.1.1 (d) and (e) show the gate voltage during turn-off transient for Si IGBTs and SiC MOSFETs respectively. The turn-off time of the Si IGBT increases linearly with rising T_j;

however, the turn-off time of the SiC MOSFET doesn't present the same characteristic. Instead, the turn-off time does not change linearly with increasing T_j [15].

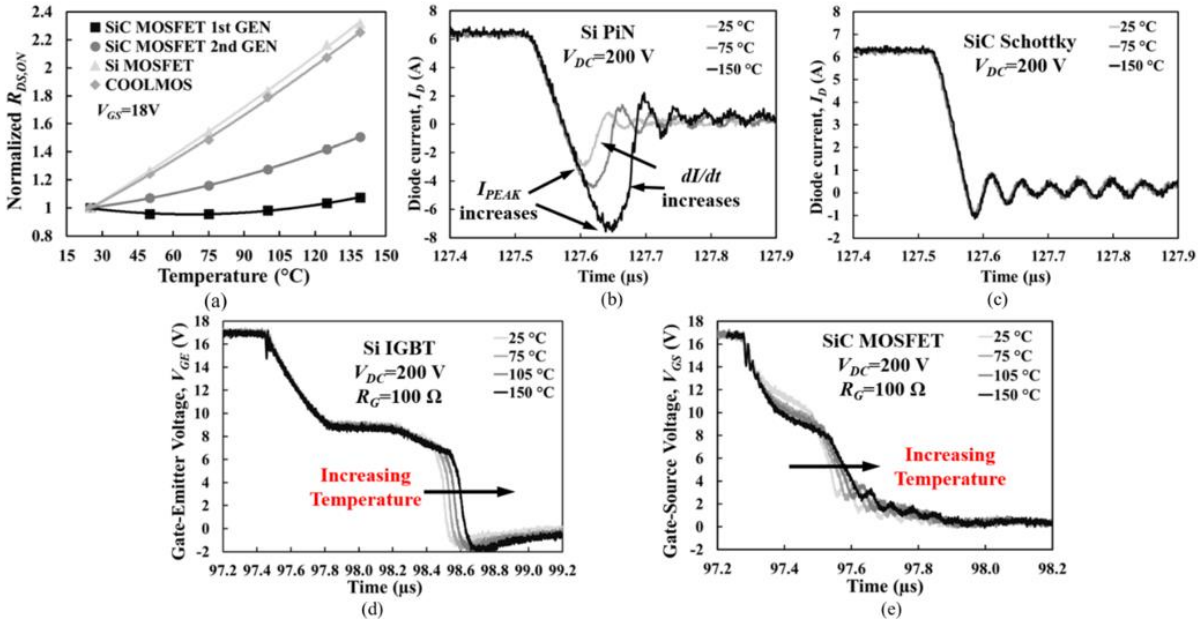


Figure 4. 1(a) Dependency of n-state resistance on temperature for different MOSFET technologies; (b) silicon PiN diode reverse recovery characteristics at different temperatures; (c) SiC Schottky diode turn-off characteristics at different temperatures; (d) silicon IGBT gate voltage during turn-off at different temperatures; (e) SiC MOSET gate voltage during turn-off at different temperatures [15].

These aforementioned comparisons between Si and SiC MOSFETs indicate that the traditional TSEPs which can be utilised to extract the T_j of Si power electronic devices can hardly be applied to the SiC MOSFET. In cases where the power device is a discrete SiC MOSFET, it is also not viable to embed temperature sensors due to the small die-area and packaging limitations. Also, the use of an infrared camera to extract values of SiC MOSFET T_j in online applications is not feasible. However, the value of T_j of power electronic devices is one of the most crucial parameters that indicates potential wear-out failures such as bond wire lift-off or solder fatigue. For this reason, alternative solutions should be developed in order to precisely measure T_j in discrete SiC MOSFETs during operation. In order to further investigate the behaviours of different TSEPs for the discrete SiC MOSFET, double pulse test (DPT) simulations have been established using LTspice simulation software. Specifically, in this research, the Cree 2rd generation discrete SiC MOSFET (part number: C2M0080120D) is used. The analytical model is provided by Cree [83] and is used in the simulations. As shown in Figure 4.2, a DPT test circuit is presented. The basic rule for the double pulse test is to generate two different successive gate pulses in the device to turn it on and off and to use appropriate probes and an oscilloscope to capture the relevant current and voltage waveforms so as to analyse the behaviour of the switch itself in both electrical and thermal terms. In this particular set-up,

terminals T_j and T_c are specifically included in the design to analyse the self-heating of the device as a function of time. The terminal T_c represents the case temperature and T_j represents the junction temperature. The temperature connections are working as voltage pins. Therefore, a potential difference of 1 V refers to a temperature difference of 1 °C.

The voltage at the T_j node contains information about the time-dependent T_j which in turn acts directly on the temperature-dependent electrical model.

The T_c terminal has to be connected to either a voltage source (which denotes the ambient case temperature) or to an external RC network (heat sink model) to observe its effect on T_j.

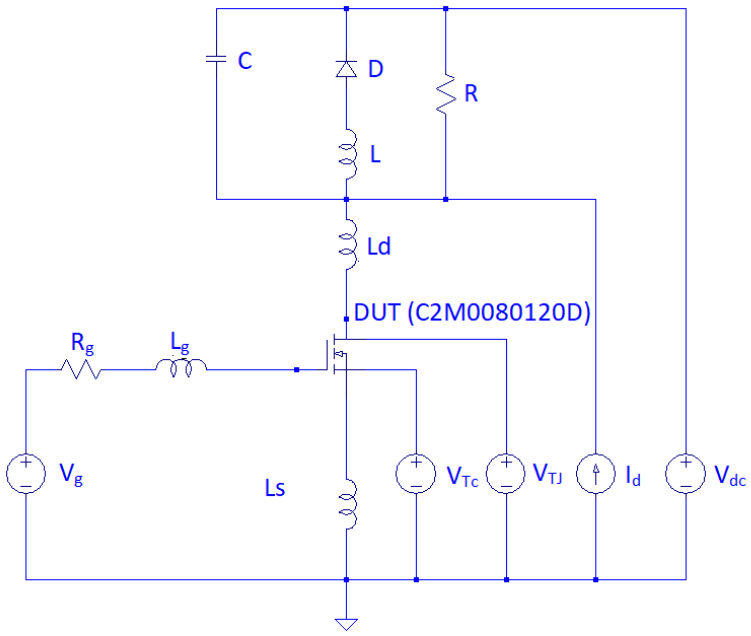


Figure 4. 2 DPT test based on Cree C2M0080120D discrete MOSFET.

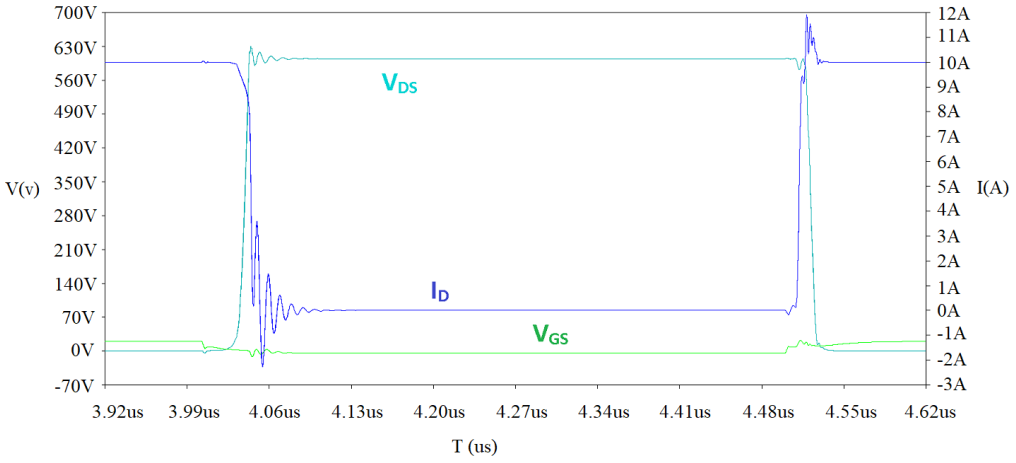


Figure 4. 3 Simulation results of DPT tests, including V_{DS}, V_{GS} and I_D.

Figure 4.2 shows the connection of the T_c terminal to an ambient temperature of 25°C.

Another point which is worth mentioning is that the inductor in parallel with the freewheeling diode in the DPT set-up is replaced by a constant current source (10 A) for simplification. Parasitic circuit components (values are suggested by Cree/Wolfspeed user manual) have been added to better match the experimental set-up and achieve more accurate simulation results. The switching waveforms of the DPT test presented are illustrated in Figure 4.3, including both turn-on and turn-off transient behaviour as well as the steady-state behaviour of V_{DS}, V_{GS} and I_D. TSEPs that have been applied in practice to Si power electronic devices and that were presented in the previous chapters are monitored by the embedded oscilloscope. Changes in these TSEPs can be observed and recorded. Despite the direct TSEP measurement, the sensitivity was also calculated where the rate represents change of the electrical parameter against change in T_j. Measured TESP results are listed in the following Table 4.1.

Table 4.1 Measured data of various TSEPs and calculated sensitivity values

Temperature (°C)	25	50	75	Sensitivity rate from 25 °C to 75 °C
V_{th} (V)	3.209	3.201	3.190	-0.38 mV/°C
Leak current(μA)	7.36	9.82	23.42	0.32 μA /°C
Miller plateau width (ns)	152.29	153.84	155.24	0.059 ns/°C
$t_{d(on)}$ (ns)	31.05	30.31	29.72	-0.026 ns/°C
$t_{d(off)}$ (ns)	126.76	127.97	129.05	0.0458 ns/°C
V_{ds} slope delay time (ns)	6.05	5.98	5.91	-0.028 ns/°C
I_{peak} (A)	10.6574	10.6563	10.6556	$-3.6e-4$ A/°C

The inherent parameters of the SiC MOSFET are either not linearly temperature-dependent or the sensitivity levels of the parameters are low compared to Si power electronic devices, which causes difficulties for current measurement technologies [4]. Therefor a new method for the determination of T_j must be found. In the next section of this chapter, a new method is proposed.

4.2 Introduction of small signal AC analysis in power electronics

The general definition of small signal AC analysis can involves the superimposition of small sinusoidal terminal currents and voltages upon an established steady-state (DC) device bias to discover the device's small signal AC characterization [84]. Here, small means that a tiny amplitude of the injection signal will be limited so as to generate no harmonics within the device. The relationship between the superimposed current and voltage will be characterized as a function of frequency. On the other hand, large-signal AC behaviour, including harmonics generation, is beyond the scope of this work, although the effects of harmonics generation within the device can often be estimated by a parametric study of small-signal AC behaviour versus DC bias [84].

Small-signal ac device analysis gives the possibilities to investigate useful device characteristics like voltage gain A_V, current gain A_I as well as estimating the stability and noise behaviour. The information collected from ac analysis can be critically useful to gain circuit-level descriptions of device behaviour.

During the progress of this research and in the literature review, it can be found that small AC signal analysis has been widely implemented in aspects of power electronic such as power converter impedance detection and system identification [85-87].A method of impedance measurement has been introduced for three-phase AC systems [84]. All impedance information can be determined by injecting an unbalanced line-to-line current between two lines of the AC system. Another example shows how a small-signal is injected into the inductor of a current-controlled boost converter to determine the online inductor resistance [87]. So far, small signal analysis has been applied to determine the resistance of the inductor, except where the technique has been used to realize the optimisation of the controller [86]. These inspiring studies invoke the possibility of the use of small AC signal analysis to investigate impedance change induced by T_j based on the fact that the internal gate resistance R_{int} in the gate-source loop of the SiC MOSFET is T_j dependent. If the value of R_{int} can be precisely estimated via small AC signal analysis then the corresponding value of T_j can be extracted [88]. Under these circumstances, a new method based on small AC signal analysis is proposed in this work.

In the present study, small signal analysis is applied to a single power electronics device to determine. In this chapter, the equivalent parasitic circuit of the Cree SiC MOSFET in TO-247-3 housing is derived and verified in order to utilize small signal analysis to estimate the impedance loop change induced by the variation in T_j. In the following sections, small signal models of SiC MOSFET are established and presented in order to further implement small AC signal analysis and to investigate the influence of T_j on it. This is crucial in implementing condition monitoring and to understand the parasitic loops so as to extracting the relevant information.

4.3 Small AC signal modelling of the SiC MOSFET

In this section, a typical small signal model of the dynamic switching of an inductive load is presented in order to explain how the small signal model can be used to extract individual impedance parameters. Then the on-state and off-state small AC signal models are compared to select the better one to be implemented in detail and to be used as the model to estimate the T_j of the SiC MOSFET.

As shown in Figure 4.4, a typical inductive switching small signal model is investigated to explain how the small AC signal analysis works. The gate-source switching loop is forced because the parameter that needs to be estimated is R_{int}.

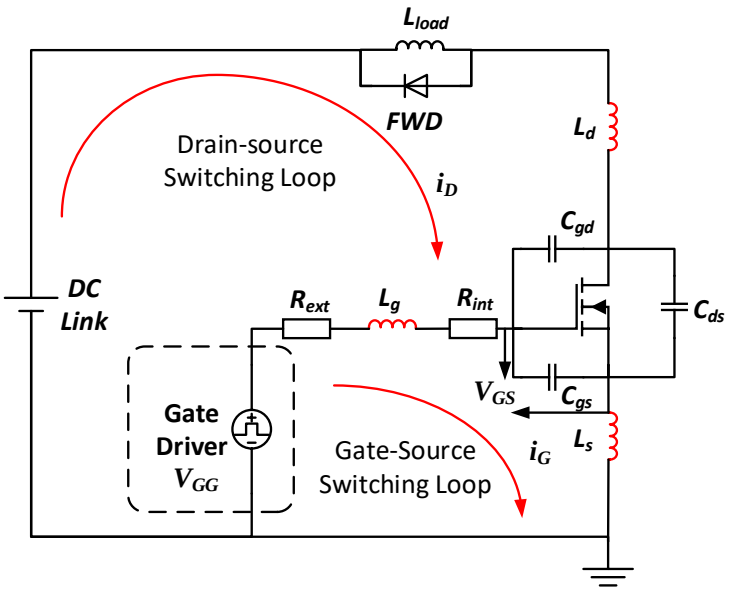


Figure 4. 4 Typical switching loop of an inductive load circuit.

During the switching transient of the SiC MOSFET, the gate-source voltage can be described as in equation 4.1:

$$V_{GS} = V_{GG} - R_G i_G - L_G \frac{di_G}{dt} - L_S \frac{d(i_G+i_D)}{dt} \tag{4.1}$$

where V_{GS} is the gate-source voltage, V_{GG} is the gate driver output voltage, R_G is the sum of R_{ext} and R_{int}, i_G is the gate current, i_D is the drain current and L_G and L_S are gate string inductance and source string inductance respectively.

According to equation 4.1, during the transient and on-state of the SiC MOSFET, the variation in V_{GS} will induce a change of the value of i_D [12]. In the case of a small signal injection, V_{GS} is superimposed with a small chirp signal which changes the output i_D although this scenario should be avoided in the normal operation of power devices. The values of di_G/dt and di_D/dt are also T_j-dependent which makes it hard to pick up only the change in R_{int}. Then the small AC signal model is narrowed down to the off state, which is established and investigated compared in the following sections.

4.4 Off-state small AC signal equivalent circuit modelling of the SiC MOSFET

An unbiased off-state small AC signal equivalent circuit is established and analysed in this section, and the model is used to simulate the frequency response which is also compared later with the results of impedance analyser.

Figure 4.5 illustrates an unbiased off-state small signal parasitic equivalent circuit for a Cree second generation discrete SiC MOSFET (C2M0080120D) packaged in TO-247-3 housing.

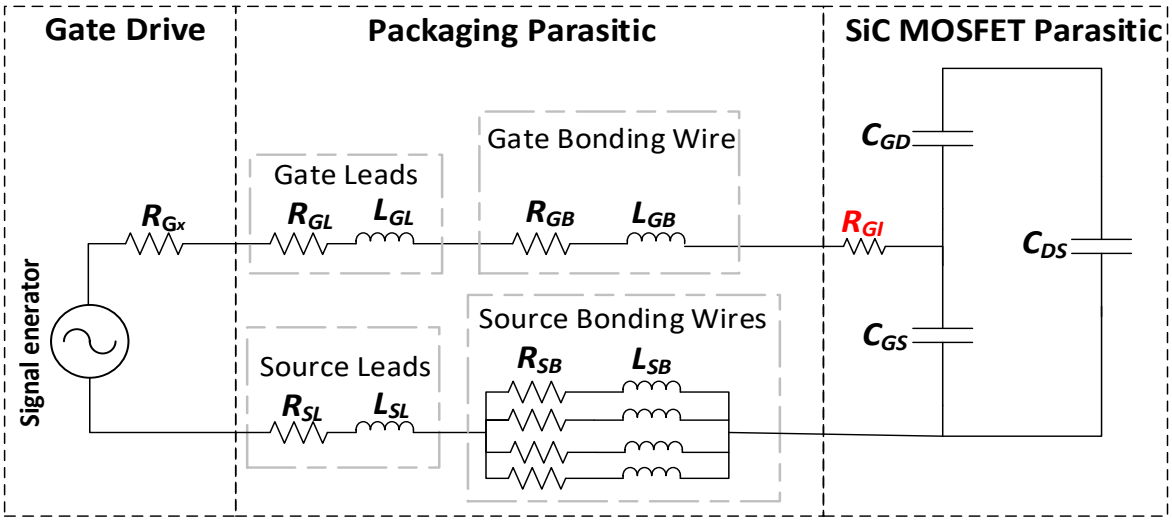


Figure 4. 5 Off-state equivalent circuit of a SiC MOSFET.

To analyse the effect of the influence of a change in T_j upon the internal gate resistance of the SiC MOSFET, not only are the chip parasitic included in the equivalent circuit but also the packaging parasitic and gate driver side parameters are presented. The values of parasitic capacitances are calculated according to the relationships between input capacitor C_{iss}, output capacitor C_{oss} and reverse recovery capacitor C_{rss}, as shown as equations 4.2, 4.3 and 4.4:

$$C_{iss} = C_{GD} + C_{GS} \tag{4.2}$$

$$C_{oss} = C_{GD} + C_{DS} \tag{4.3}$$

$$C_{rss} = C_{GD} \tag{4.4}$$

Here the values of C_{iss}, C_{oss}, C_{rss} are obtained from the datasheet provided by Cree, as shown in Figure 4.6.

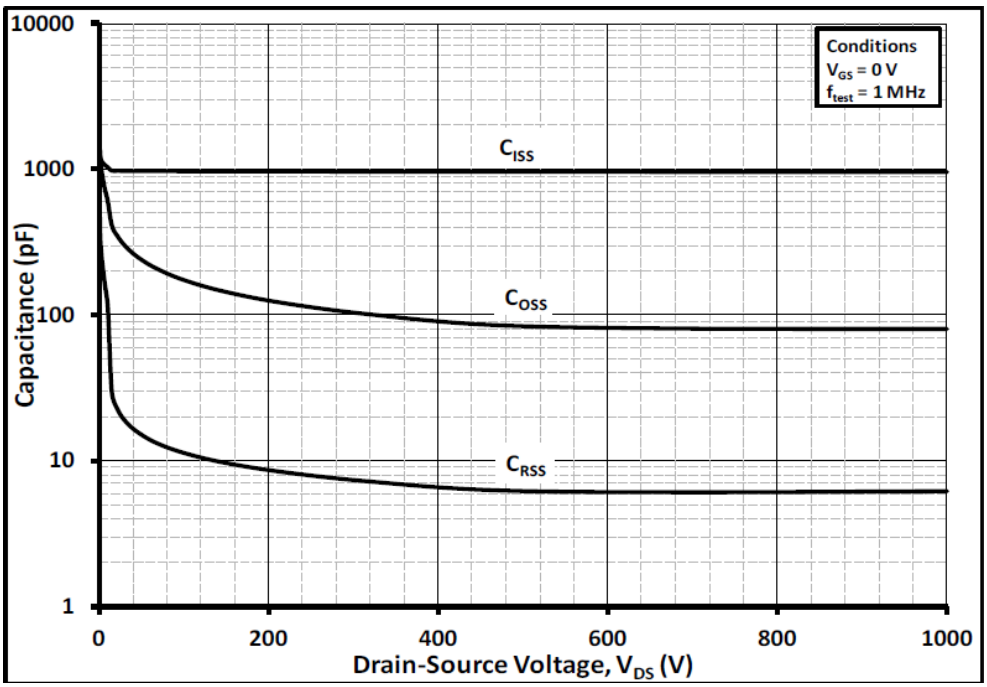


Figure 4. 6 Typical parasitic capacitance VS V_{DS} for C2M0080120D [83].

It is worth noting that these parasitic capacitances are voltage-dependent and thus the values are extracted at the instance in which the drain-source voltage is equal to the DC link voltage. During the unbiased test, the capacitance value is estimated as the drain-source voltage equal to 0 V to emulate the unbiased condition. Then, during the biased test, the drain-source voltage is set to be 600 V and the parasitic capacitors are accordingly: C_{GD}=6.5 pF, C_{DS} =73.5 pF, C_{GS} =943.5 pF. The individual package component value is calculated based on the diameter of the TO-247-3 housing provided for the Cree SiC MOSFET (C2M0080120D) in its data sheet [83].

4.5 Parametric calculation of individual parasitic for MOSFET

4.5.1 Nominal values calculation of parasitic of SiC MOSFET

In the off-state equivalent parasitic loop, the only temperature-dependent component is the gate internal resistance, and as stated in the literature review the temperature sensitivity of the internal gate resistance is 1 mΩ/C° to 2 mΩ C° [88, 89].

Then, the values of parasitic parameters should be derived in order to be simulated later. The device under study is in a TO-247 package. According to Cree, the standard for the sources bond wire of TO-247 and TO-220 are either 4 15 mil diameter bond wires in parallel or 3 20 mil diameter bond wires in parallel. In this thesis, all the simulation results are based on 4 bond wires in parallel. The bond wire is made of aluminium.

a. Calculation of bond wire resistance

The DC resistance of a conductor is calculated according to equation 4.5:

$$R_{dc} = \frac{\rho l}{A} \tag{4.5}$$

where ρ is the resistivity of the material in $\Omega * \text{mm}$, l is its length in metres and A is the cross - sectional area in square millimetre.

By checking the size of the bond wire in the TO-247, the length of the bond wire is usually 7 mm and the diameter as mentioned before is $15\ \text{mil}$, and the resistivity of aluminium is $2.6548 * 10^{-11} \Omega * \text{mm}$.

Thus, one single bond wire's DC resistance can be calculated as $16.8\ \text{u}\Omega$.

When there are 4 bond wires in parallel, the total resistance can be calculated as $4.2\ \text{u}\Omega$.

The AC resistance of a round straight wire is calculated according to equation 4.6:

$$R_{ac} = \frac{\rho x l}{A_{eff}} \tag{4.6}$$

Where ρ is the resistivity of the conductor in $\Omega * \text{m}$, l is the Length of the conductor in mm and A_{eff} is the effective cross-sectional area used in mm.

Equation 4.7 below represents the skin surface effect:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{4.7}$$

Where ρ is the resistivity of the conductor in $\Omega * \text{m}$, f is the frequency in Hertz, and μ is the absolute magnetic permeability of the conductor.

The absolute magnetic permeability is $(\mu) = \mu_o \text{ x } \mu_r$

where $\mu_o = 4\pi \text{ x } 10^{-7}\ \text{H/m}$

The A_{eff} can thus be expressed as equation 4.8:

$$A_{eff} = \delta \pi d \tag{4.8}$$

Where d is the diameter of the conductor.

This means that the cross-sectional area used is too large from high frequencies down to the point where the skin depth becomes about half of the radius of the conductor, at which point

the inaccuracies increase and eventually the calculated area used becomes bigger than the actual conductor. Therefore, the calculation method is only an approximation and is then only usable when $r >> \delta$, where in the case of bond wire it matches such a scenario.

As a result, the AC resistance at different frequencies could be calculated. For a frequency of 40 MHz, the AC resistance of a single wire is 12.6 mΩ.

When 4 bond wires sit in parallel, the total resistance is 3.15 mΩ.

Bond wire resistances with different numbers of bond wire lift-offs can be derived accordingly.

b. Calculation of bond wire inductance

For the calculation of the bond wire inductance, the following approximated equation 4.10 is used:

$$L = \frac{\mu_0}{2\Pi} * l \left[ln\left(\frac{l}{r} + \sqrt{1 + \frac{l^2}{r^2}}\right) - \sqrt{1 + \frac{l^2}{r^2}} + \frac{r}{l} + \frac{1}{4} \right] \quad (4.10)$$

where r is the bond wire radius, l is its length and μ_0 is the permeability of free space.

($1.2566e^{-6}$ H/m)

For $l>>r$, a simplification can be derived from the above as in equation 4.11:

$$L = \frac{\mu_0}{2\Pi} * l \left[ln\left(\frac{2l}{r}\right) - 0.75 \right] \quad (4.11)$$

In this case, the length of the bond wire is 7 mm and the radius of the bond wire is 187.5 um. As a result, the single bond wire inductance is calculated as 5 nH, and accordingly the total inductance can be derived based on the number of bond wires in parallel.

c. Calculation of lead resistance and inductance

Similarly, based on the normal lead size of TO-247 package, the resistances and inductances of both gate lead and source lead can be calculated using the aforementioned equations and formulae. The results are shown below.

The typical gate lead resistance is about 14.6 mΩ, which is equal to the source resistance and the inductance is calculated as 15 nH.

In summary, the individual parasitic values of each component appearing in the equivalent circuit are listed in the following Table 4.2.

Table 4. 2 Results of small AC signal equivalent circuit parameters calculation

External gate resistance	10 Ω
Lead resistance	14.6 mΩ
Lead inductance	6 nH
Internal gate resistance	4.6 Ω @25 °C [83]
Gate source capacitance	1263 pF @25 °C [83]
Single bond wire resistance	12.6 mΩ
Single bond wire inductance	5 nH

4.5.2 Parasitic parameters of SiC MOSFET when considering temperature influence.

Among all those parameters calculated in section 4.5.1, gate-source capacitance is temperature invariant, inductances including lead inductance and bond wire inductance are also not changing against temperature. The only temperature dependent parasitic is resistors. In this section, all the resistance listed in the Table 4.2 will be calibrated against T_j. Consider the material of external resistor and lead are pure copper, it consists of 99% copper in datasheet, to simplify calculation and the temperature coefficient of copper is 0.393% per degree C (3.93×10^{-3}/°C) at 20°C. And the bond wire is pure aluminium and the temperature coefficient of aluminium is 4.308×10^{-3}/°C at 20°C.

The generic formula of temperature effects on resistance is as follow:

$$R = R_{ref} \times [1 + \alpha(T_j - T_{ref}) \tag{4.1}$$

Where R is the conductor resistance at temperature T_j, R_{ref} is the conductor resistance at reference temperature T_{ref}, which is usually 20°C, α is the temperature coefficient of resistance of the conductor material, T_j is the conductor temperature in degrees Celsius and T_{ref} is the reference temperature that α is specified at for the conductor material. The temperature dependent of external gate resistance, lead resistance and bond wire resistance can be calculated

using equation 4.1 by assigning all parameters needed. The results are summarized in table 4.3 below:

Table 4. 3 Temperature dependent resistances of parasitic in SiC MOSFET

Parameter	Nominal	25°C	50°C	75°C	100°C	125°C
External gate resistor (Ω)	10	10.20	11.18	12.16	13.14	14.13
Lead resistance (mΩ)	14.6	14.89	16.32	17.75	19.18	20.63
Bond wire resistance (mΩ)	12.6	12.85	14.09	15.32	16.56	17.80

Although the external gate resistance values are listed, the external gate resistor will remain 10Ω in the simulation since it is at the gate driver side and the ambient temperature will be much lower than the T_j of the SiC MOSFET. For lead resistance and bond wire resistance, the value of resistance at each test temperature will be imported into the simulation software to minimize the simulation error.

4.6 Verification of small ac signal equivalent circuit

The first step in testing the equivalent circuit is to use simulation software to examine its behaviour. In this research, LTspice [90] software is used to fully simulate the operation of the small AC signal equivalent circuit. At the very beginning, an unbiased off-state circuit is simulated, and the simulation schematic is shown in Figure 4.7.

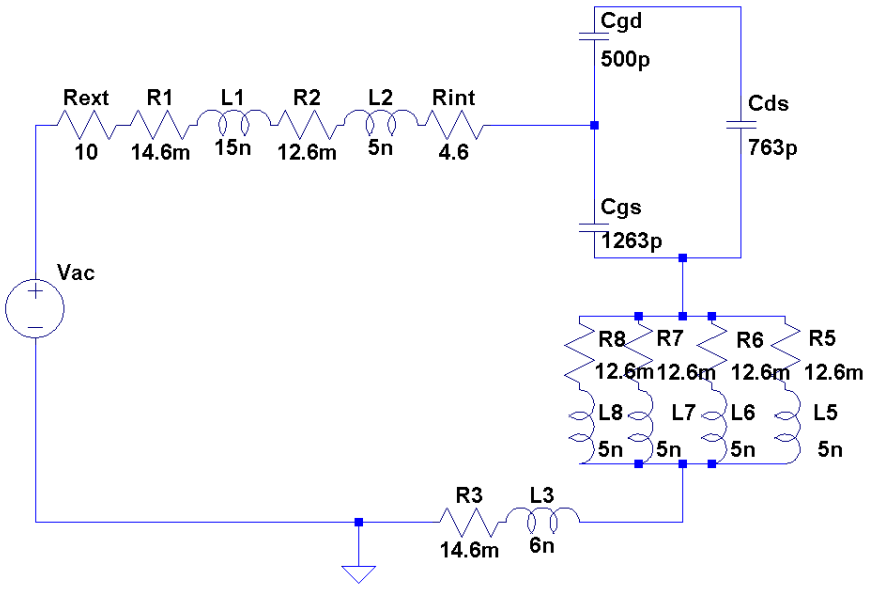


Figure 4. 7 Schematic of un-biased off-state gate-source equivalent circuit for SiC MOSFET.

Here R_{ext} is the external gate resistance, R_{int} is the internal gate resistance, R_1 and R_3 are gate lead resistance and source lead resistance respectively, R_2 is the gate bond wire resistance, R_5, R_6, R_7, R_8 are 4 individual source bond wire resistances, L_1 is the gate lead inductance, L_2 is the gate bond wire inductance, L_3 is the source lead inductance and L_5, L_6, L_7, L_8 are 4 individual source bond wire inductances. C_{GD} is the gate-drain capacitance, C_{GS} is the gate-source capacitance and C_{GD} is the gate-drain capacitance, and finally the V_{AC} is the AC signal injection voltage source.

The simulation is running in AC signal sweeping mode from 300 KHz to 100 MHz at room temperature, and the gate-source loop impedance is calculated by measuring the values of V_{GS} and I_G as illustrated in Figure 4.8 below.

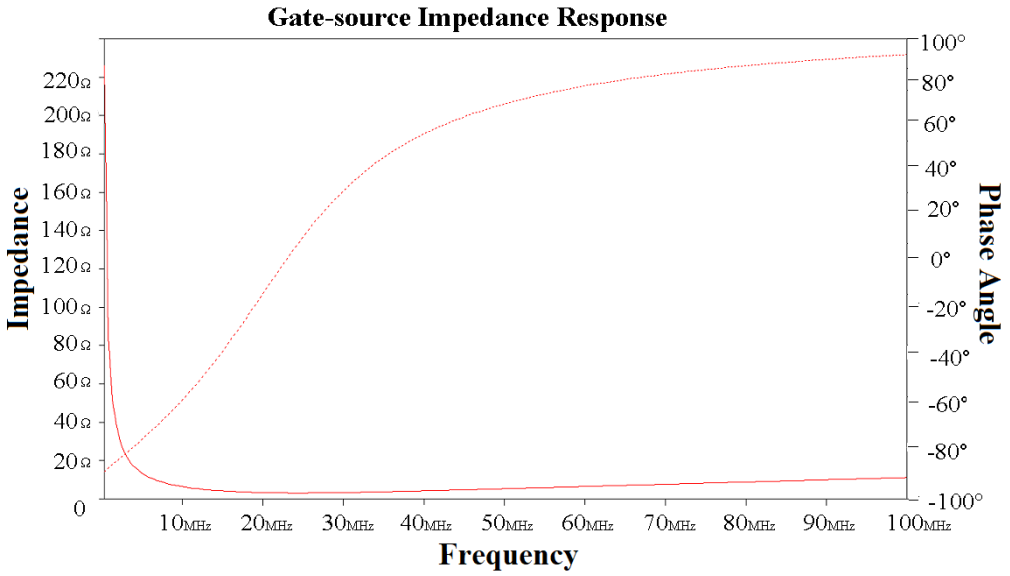


Figure 4. 8 Simulation results for gate-source loop impedance response at room temperature.

The solid line in the figure indicates the amplitude of the gate-source loop impedance and the dotted line illustrates the phase response of gate-source loop impedance. The results are then compared with the practical results.

In order to verify the equivalent circuit, experimental work was conducted with the help of a network analyser (Agilent Keysight E5071B) and the test set-up is shown in Figure 4.9. An unbiased SiC MOSFET was placed on a controlled heat plate and connected to the network analyser. In this test, a small AC signal sweep starting from 300 kHz to 100 MHz was injected into the gate-source terminal and the reflected signal captured. Fixed temperature steps were achieved by manipulating the heat plate power source to change the chip temperature. After the

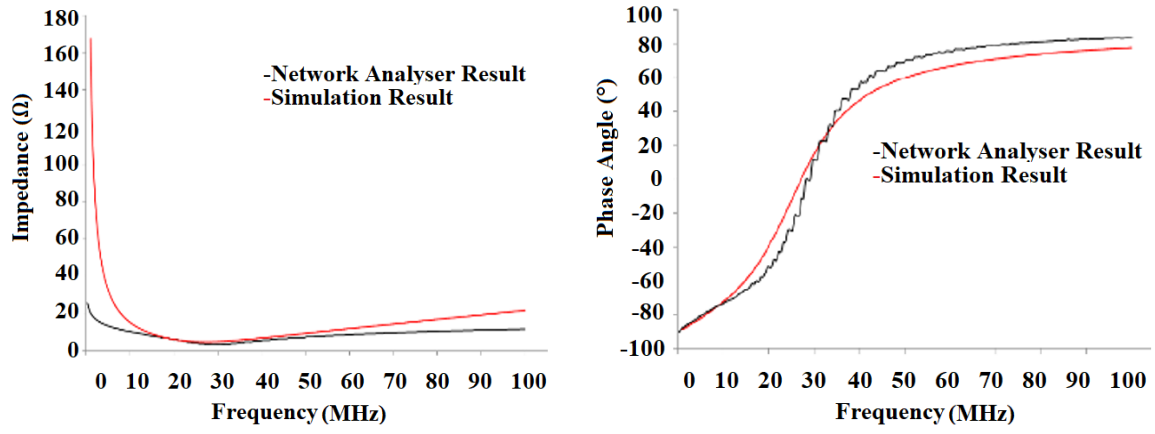
capture of the reflected signals, data was processed in MATLAB to generate the corresponding impedance frequency response for various temperatures.

(a) (b)

Figure 4. 9 Experiment set-ups: (a) Agilent Keysight E5071B Network analyzer;

(b) temperature-controlled heat plate.

The same small signal analysis was carried out with the data generated from experiments. Figures 4.10(a) and 4.10(b) show the simulated and measured data for impedance magnitude and phase respectively. Both figures represent results at one chip temperature and simulation and experimental results are in close proximity.



(a) (b)

Figure 4. 10 Simulation results and network analyser results: (a) impedance magnitude at T=25°C; (b) impedance phase at T=25°C.

The test bench shown in Figure 4.9 gives the impedance of the off-state gate-source loop under unbiased conditions. Five different temperatures have been tested and the results are presented in Figure 4.11. These impedance frequency responses are processed by importing the network analyser data into MATLAB, which is the frequency response of the reflected signal of the off-state gate-source loop.

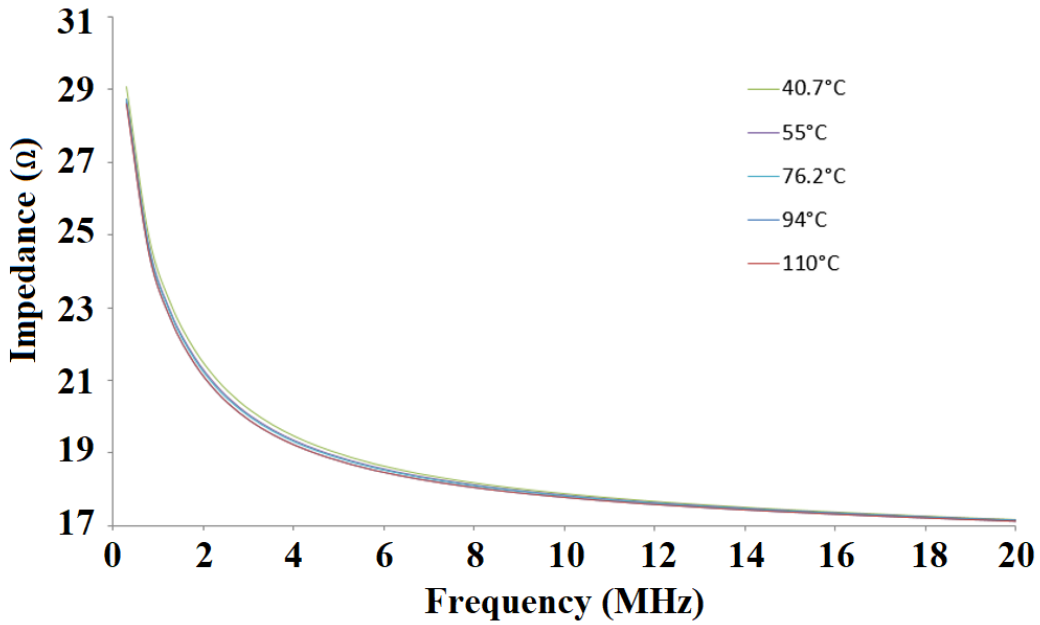


Figure 4. 11 Off-state gate-source loop impedance frequency response at 5 different T_j.

As can be seen from the Figure 4.11, the impedance of the off-state loop at each frequency decreases with increasing junction temperature. The impedance changes between each temperature steps at 10 MHz is depicted and plotted in Figure 4.12. The relationship between the impedance and junction temperature shows good linearity. The sensitivity is calculated to be $-1.5\ \mathrm{m\Omega/°C}$, which is reasonable in order to distinguish the impedance variation induced by the rising of the T_j. This linearity can now be used as a new indicator for T_j for SiC devices.

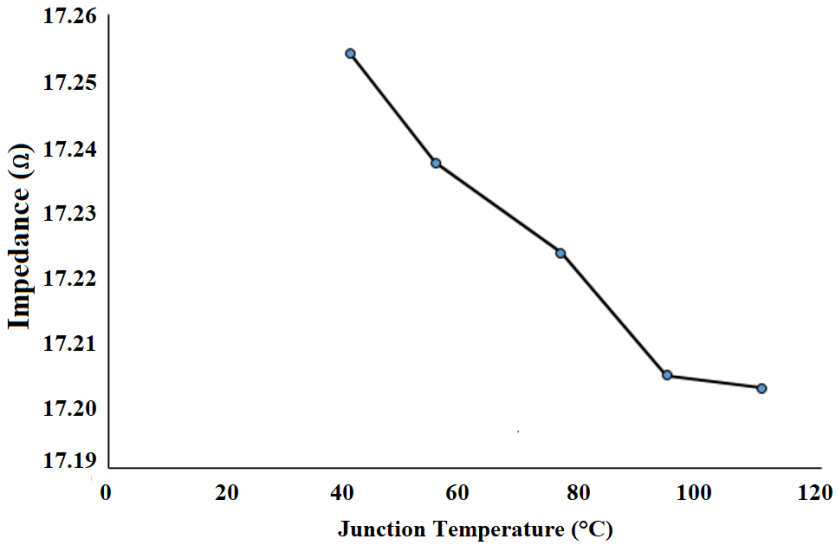
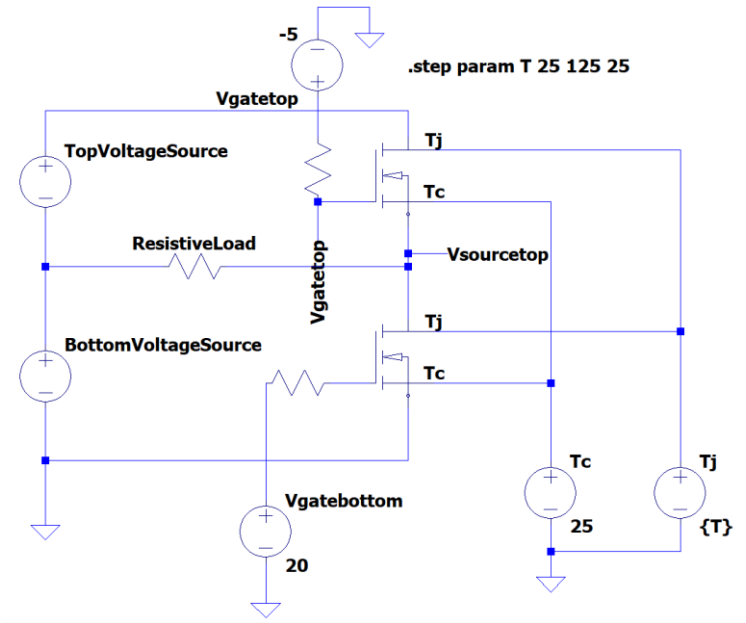


Figure 4. 12 Impedance VS T_j at 10 MHz.

In addition, the proposed method is investigated in SiC module as well to examine whether the method can be extended to SiC module or not.

A single phase-leg SiC Module is used to conduct simulation to examine the proposed method. As can be seen from Figure 1 that a single-phase half bridge inverter with a resistive load is presented, the simulation is divided into two parts: the first part is assuming that when the top MOSFET is at its off state (Figure 4.13(a))and then the small AC chirp signal is injected into the gate-source terminal of the top switch and the bottom switch is constantly on, the second part of the experiment is doing the opposite (Figure 4.13(b)). Finally, as a comparison set, a discrete SiC MOSFET is simulated and small AC chirp signal is superimposed into the gate terminal when the MOSFET is during its off state with a resistive load as demonstrated in Figure 4.13(c).


-5
.step param T 25 125 25
Vgatetop
TopVoltageSource
Tj
Tc
ResistiveLoad
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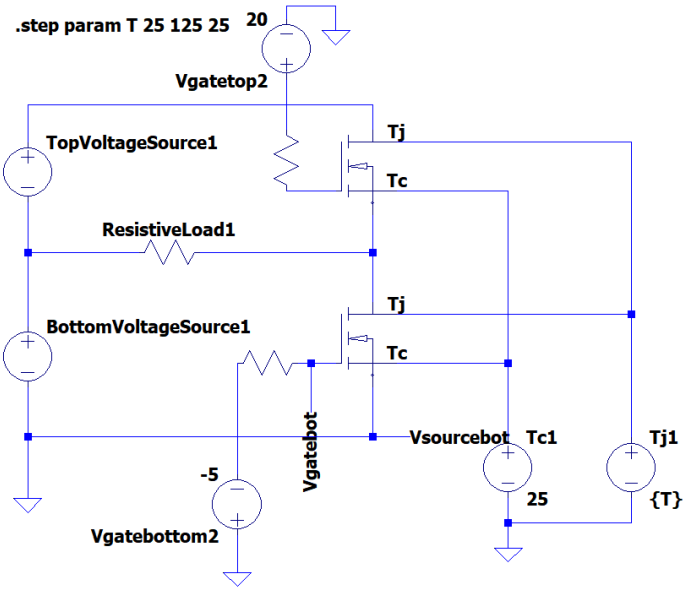
(a)


.step param T 25 125 25
20
Vgatetop2
TopVoltageSource1
Tj
Tc
ResistiveLoad1
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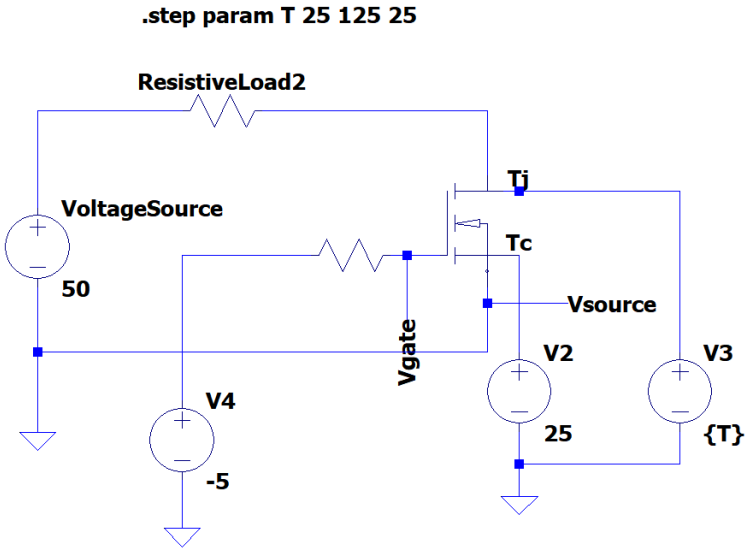


(c)

Figure 4. 13 LTspice Simulation Schematics: (a) Top switch is off and the small AC signal is superimposed into the gate terminal of the SiC MOSFET while the bottom switch is at its on-stated; (b) Top switch is at its on-stated while the small AC signal is superimposed into the gate terminal of bottom switch; (c) Small AC chirp signal is superimposed into the gate terminal of a discrete SiC MOSFET when it is completely off.

All the parameters used in simulation for all three simulating conditions are identical: those parameters include supply voltage of all three DC voltage supply, maximum gate-source voltage when the switch is on, minimum gate-source voltage when the switch is off, the resistance of the resistive load, the case temperature of all three SiC MOSFETs. Those input parameters are listed in Table 4.4 below.

Table 4. 4 Input Parameters for SiC MOSFET Module Simulation

Parameter	Value
DC Voltage Source	50V
Maximum Gate-Source Voltage During On-state	20V
Minimum Gate-Source Voltage During Off-state	-5V
External Gate Resistance	10Ω
Amplitude of Small AC Chirp Signal	500mV
Sweeping Frequency Range	300KHz to 100MHz with 1000Hz increment
Case Temperature	25℃
Junction Temperature	5 Conditions with equal time step difference (25℃, 50℃, 75℃, 100℃, 125℃)

The models of SiC MOSFET module and discrete SiC MOSFET are provided by Cree/Wolfspeed and the models include parasitic parameters. The simulations are performed under 5 different T_j conditions to evaluate the different gate-source voltage performances. Figure 14 presents the frequency response of gate-source voltage for all three different arrangements with a resistive load under small AC chirp signal injection during their off-states.

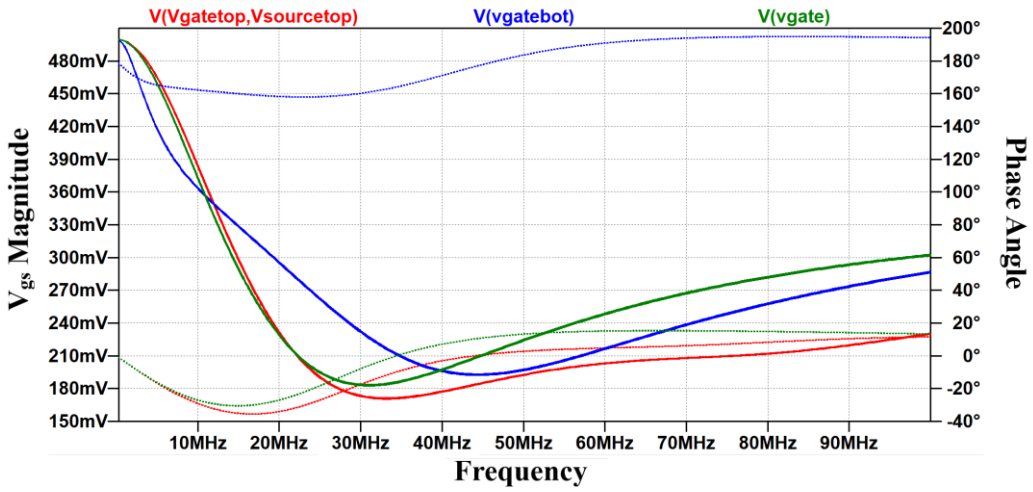
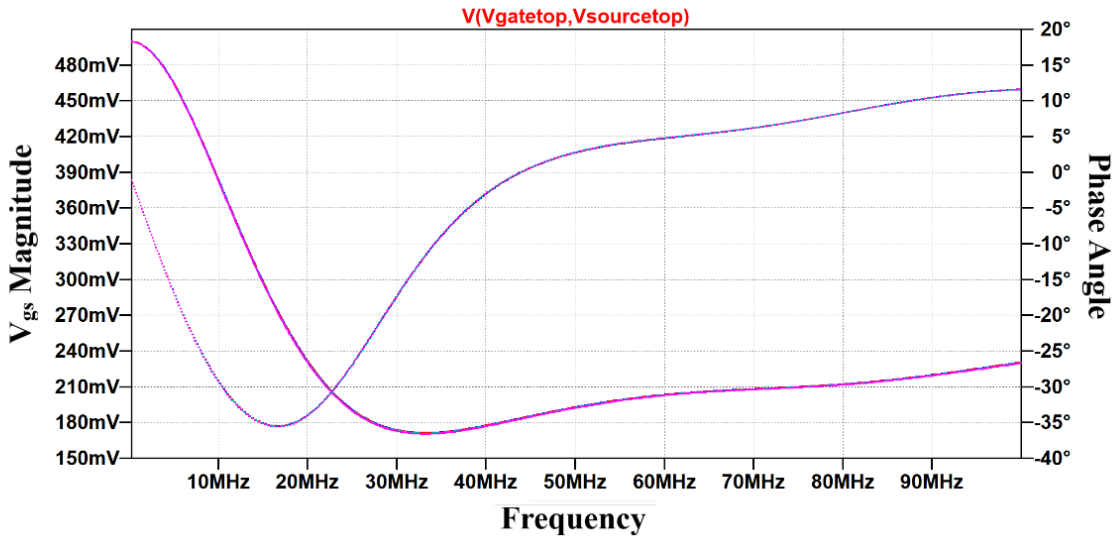


Figure 4. 14 Frequency response comparison of three different simulation setups.

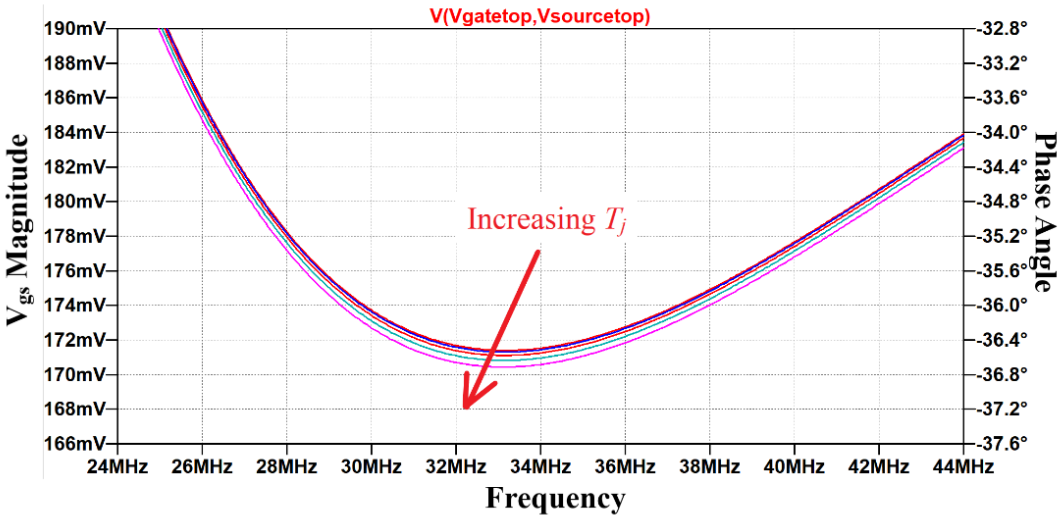
The red solid line is the magnitude of gate-source voltage frequency response of the top switch and the dashed red line is the phase angle of gate source voltage frequency response of the top

switch. And the blue solid line is the magnitude of gate-source voltage frequency response of the bottom switch and the dashed blue line is the phase angle of gate source voltage frequency response of the bottom switch. And lastly, the green solid line is the magnitude of gate-source voltage frequency response of the discrete SiC MOSFET simulation result and the dashed blue line is the phase angle of gate source voltage frequency response of the discrete SiC MOSFET. It can be seen from Figure 4.14 above that all three sets of results have similar frequency response, but their behaviours are not the same. For all of them due to the change of T_j there is small frequency response differences between each T_j. To further analyse the details of those results, each set of simulation results will be illustrated in along with zoomed in frequency response of each set of data.

The frequency response of gate-source voltage of the top switch with small AC signal injection when it is off while the bottom switch is on is illustrated in Figure 4.15(a) and corresponding zoomed in frequency response is presented in Figure 4.15(b). Figure 4.16(a) and (b) demonstrate the frequency response of gate-source voltage of the bottom switch with small AC signal injection when it is off while the top switch is on, and its zoomed in frequency response respectively. Finally, the frequency response of a discrete SiC MOSFET with a resistive load and its zoomed in frequency response are demonstrated in Figure 4.17(a) and (b).

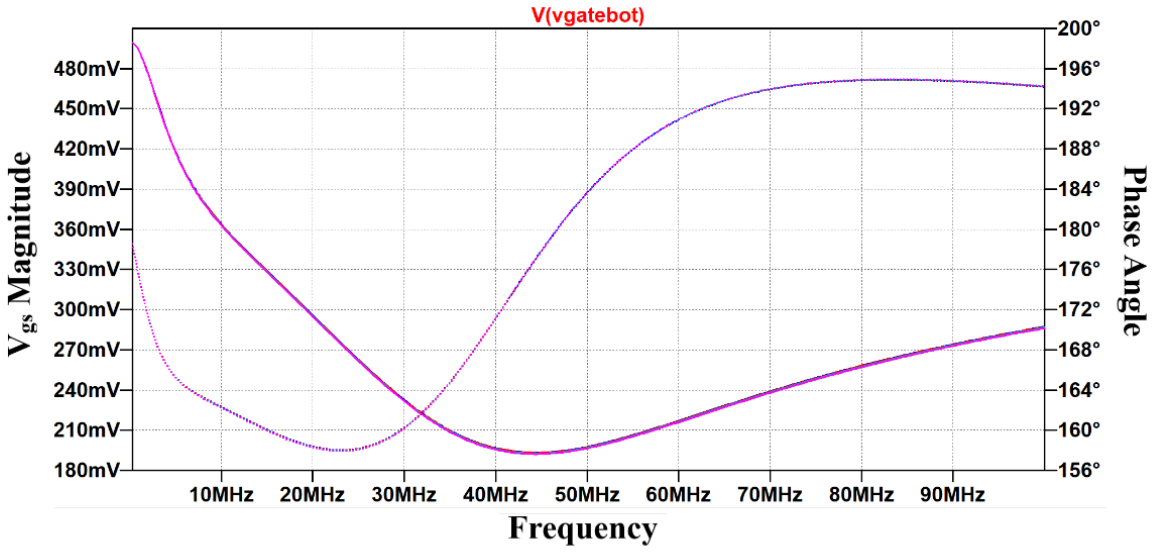


(a)

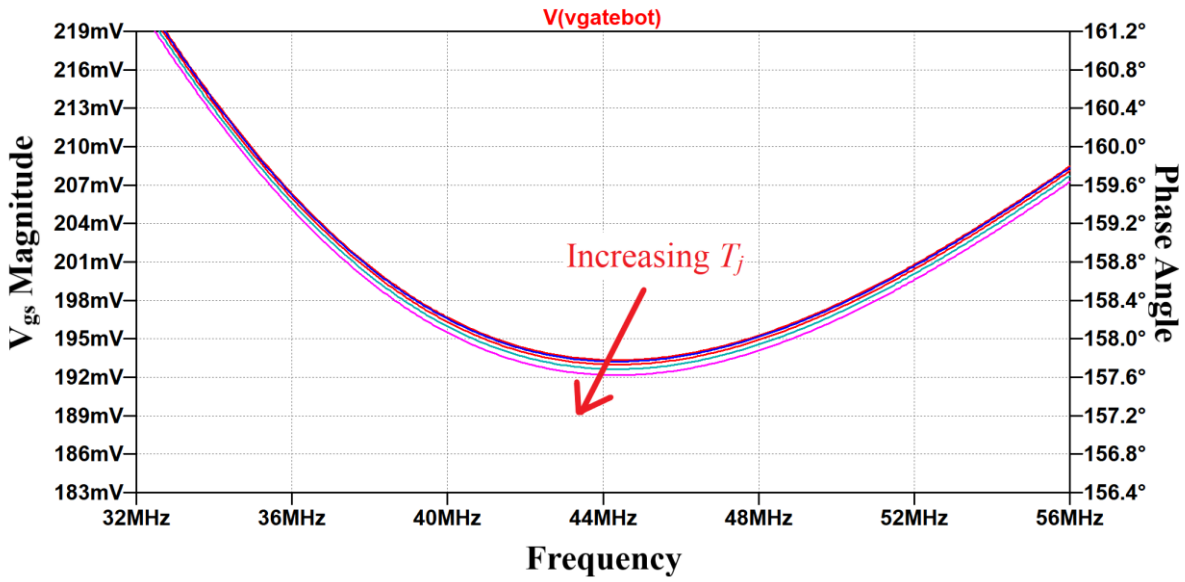


(b)

Figure 4. 15 The frequency response of gate-source voltage of the top switch with small AC signal injection when it is off while the bottom switch is on:(a) Full sweeping frequency range; (b) Zoomed in frequency response at resonant frequency.

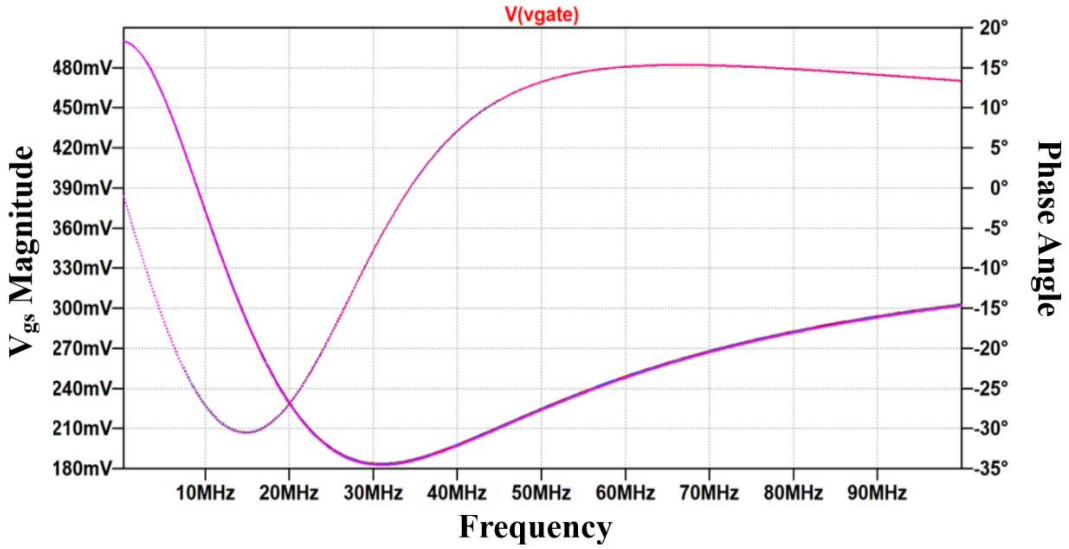


(a)



(b)

Figure 4. 16 The frequency response of gate-source voltage of the bottom switch with small AC signal injection when it is off while the bottom switch is on:(a) Full sweeping frequency range; (b) Zoomed in frequency response at resonant frequency.



(a)

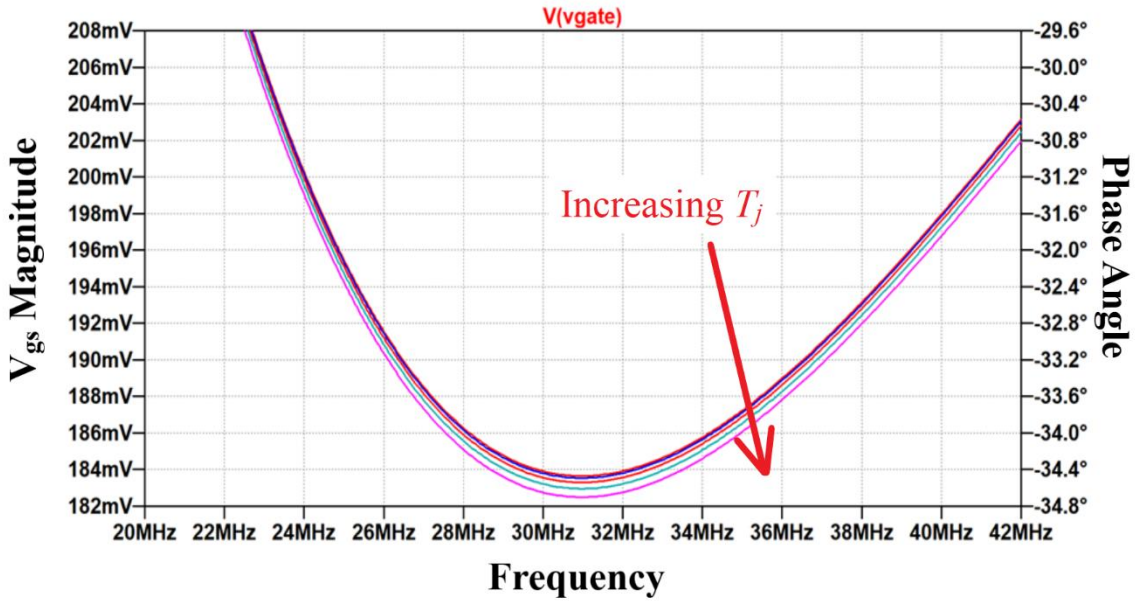


Figure 4. 17 The frequency response of gate-source voltage of the single discrete SiC MOSFET with small AC signal injection when it is off while the bottom switch is on:(a) Full sweeping frequency range; (b) Zoomed in frequency response at resonant frequency.

It can be concluded from results illustrated above that under all three conditions, the magnitude of the gate-source voltage frequency response exhibit a homogenous decreasing trend with the increasing of the T_j. However, it is clearly indicated in those zoomed in frequency responses that the resonant frequency where the gate-source loop presents the lowest impedance is different. The results shown above means that the proposed small AC signal injection method can be applied to SiC modules since the frequency response shows similar behaviour. But individual calibration tests need to be carried out for each SiC MOSFET inside the module to establish individual look-up table.

4.7 Conclusion

In this chapter it has been concluded that the traditional TSEPs are difficult to apply to SiC MOSFETs and an alternative method is proposed for detecting the T_j of SiC MOSFETs using a small AC signal analysis technique. An unbiased SiC MOSFET is excited by injecting a high frequency perturbation signal into the gate lead, and the frequency response is calculated using a signal processing technique. Simulations and practical work were carried out. A precise small-signal gate-source equivalent circuit was developed and used in simulations and the results compared with practical results gained from a network analyser. The two sets of results exhibit a good match. The temperature dependence of loop impedance was tested and captured using the network analyser. It was found that, at a certain frequency, the impedance frequency response shows good linearity and reasonable sensitivity which can be easily detected. The results obtained have demonstrated the capability of the proposed technique. In the next chapter, experimental results with fully biased test set-ups are demonstrated and discussed.

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Chapter 5. Experimental Implementation Based on Small AC Signal Injection Technique

In the previous chapter, the internal gate resistance (R_{int}) of a Cree C2M0080120D SiC MOSFET is extracted with the help of a network analyser under unbiased conditions. However, using such expensive equipment to extract thermal information is impractical in real applications. Thus, an alternative solution needs to be developed. In this chapter, practical tests are established using a function generator to generate a high frequency chirp signal. All the experimental set-ups and results are presented including the high frequency chirp signal injection circuit set-up, along with experimental results for the unbiased and biased signal injection and finally the method is validated using a Cree/Wolfspeed SiC MOSFET evaluation toolkit.

5.1 Gate source voltage dependency against temperature

To further examine the temperature dependency of the internal gate resistance and to establish circuit which is in applicable practice instead of using a network analyser which is in principle not suitable for online or in-situ monitoring, a gate-source voltage measurement test circuit is proposed based on the equivalent circuit of the gate-source loop of the SiC MOSFET during the off-state. Initially, an unbiased test is established to compare the results with those using the network analyser and to verify the proposed theory. Then, after the verification, the SiC MOSFET is tested under various DC bias conditions to determine the influences of different DC biasing and corresponding gate-source voltage frequency responses in terms of the relationship with changes in T_j.

5.1.1 Unbiased test

As mentioned in previous chapters, it is impractical to directly measure the device's T_j of devices packaged with TO housing. This study uses the small signal injection technique to find the frequency response of the gate-source impedance loop during the off-state and to analyse the variation in internal gate impedance induced by changes in T_j. Following the tests using the network analyser described in Chapter 4, a small signal injection circuit is designed based on the off-state equivalent parasitic circuit illustrated in Figure 5.1. As shown in Figure 5.1, the SiC MOSFET is unbiased between drain and source. A Tektronix AFG3102 waveform generator sweeps a chirp signal which frequencies varying from 300 kHz to 100 MHz with a

peak amplitude of 600 mV, although only the frequency range from 5 MHz to 10 MHz is required. A Pico-scope 3206b for data acquisition is used. This device has a sampling rate of 100 Msps. Detailed introduction of this Pico-scope is organized in Appendix F. A 1.2 kV SiC MOSFET from CREE/Wolfspeed with the reference number C2M0080120D has been placed on a voltage-controlled heat plate and connected to the Pico-scope to capture the gate-source voltage signal. The heat plate temperature was varied between to 100 °C under control of its voltage source. Increments in temperature step of 20 °C were selected, which means that a total of 5 temperature steps are used during the off-stated test. At each temperature step, the temperature is measured by a thermal coupler and displayed by a thermometer. In order to achieve thermal equilibrium and to make sure that the test is undertaken when the chip temperature does not change, the gate-source voltage is captured 5 minutes after the thermometer displays no further changes. After the chip temperature has stabilized, the aforementioned chirp signal generated by the waveform generator is injected into the gate-source terminals and the voltage between the gate terminal and the source terminal is captured by the Pico-scope. The information acquired is directly saved to a PC to be processed afterwards. A photograph of the unbiased small signal injection test set-up is presented in Figure 5.2.

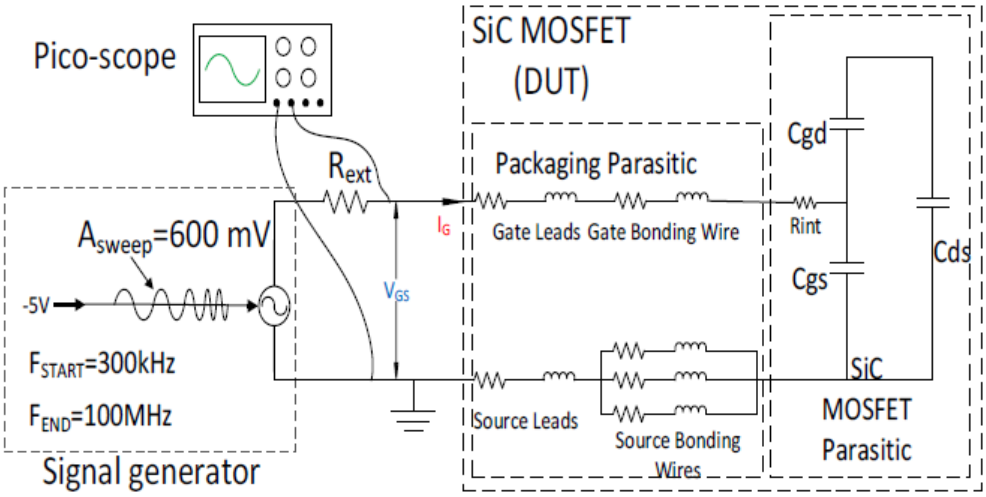


Figure 5. 1 Small chirp signal injection into gate-source terminals of SiC MOSFET during off-state under un-biased condition.

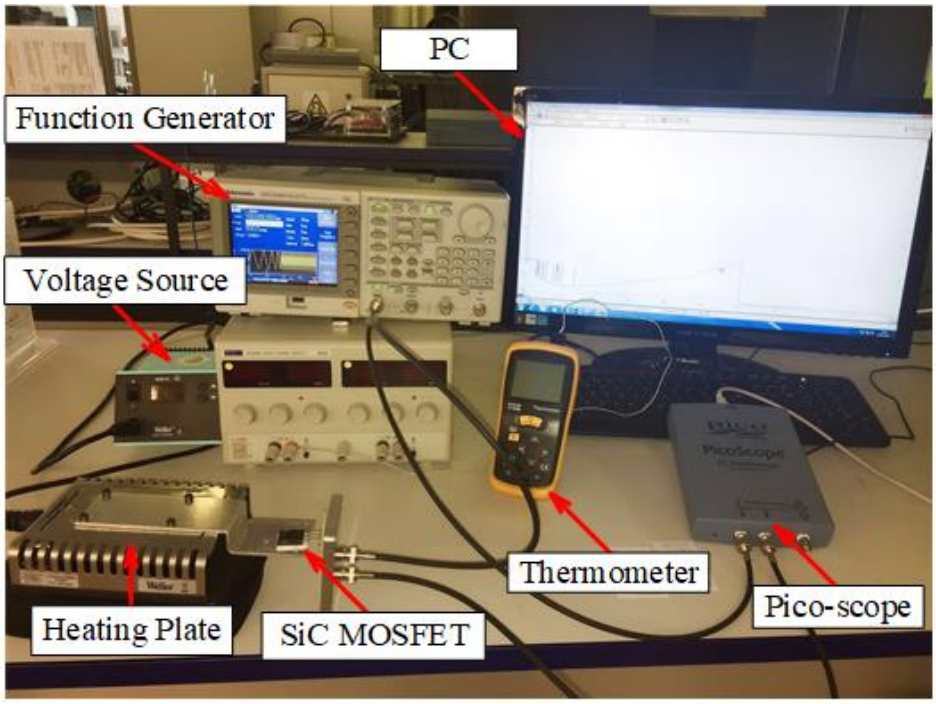


Figure 5. 2 Photograph of unbiased experimental test set-up.

As the external gate resistor is not so exposed to the high temperature fluctuation and a resistor which is less temperature-dependent can be selected as well, the voltage measured after the external gate resistor will only be influenced by change in the internal gate impedance, which is temperature dependent. The voltage measured is than processed by using the discrete Fourier transform (DFT) and peak-hold function to determine the frequency response of the gate-source loop. In order to extract enough information from the captured data to identify the change in frequency response induced by T_j, the FFT windowing function and number of bins must be carefully selected. The hamming window function has been selected and the number of bins set

to 1024, and 247 data points are captured in order to produce the frequency response of the V_{GS}. This selection is intended to achieve a balance between accuracy and the time taken to process the data.

Figure 5.3(a) shows results of the magnitude frequency response for the gate-source loop at different junction temperatures between 5 MHz and10 MHz. As illustrated in Figure 5.3(a), change in values of amplitude is in a nearly linear fashion with the T_j over the full frequency range; however, at single frequencies, the difference between the amplitudes is very small (approximately-0.03 mV/°C). Furthermore, the linearity is not constant for each frequency point.

In order to increase resolution, a new but simple method is proposed. Rather than presenting one value of magnitude against its corresponding frequency over the frequency range, the values of magnitude are integrated over the full frequency range for one junction temperature point, as shown in equation (5.1).

$$Magnitude_{Total} = \sum_{F_{start}}^{F_{end}} Magnitude_{sample\ point} \tag{5.1}$$

where, $Magnitude_{Total}$ is the integrated magnitude of the V_{GSpeak} over the whole frequency range, $Magnitude_{sample\ point}$ is the magnitude of V_{GSpeak} captured at each sampling data point and F_{start}, F_{end} represent the starting and ending frequencies respectively.

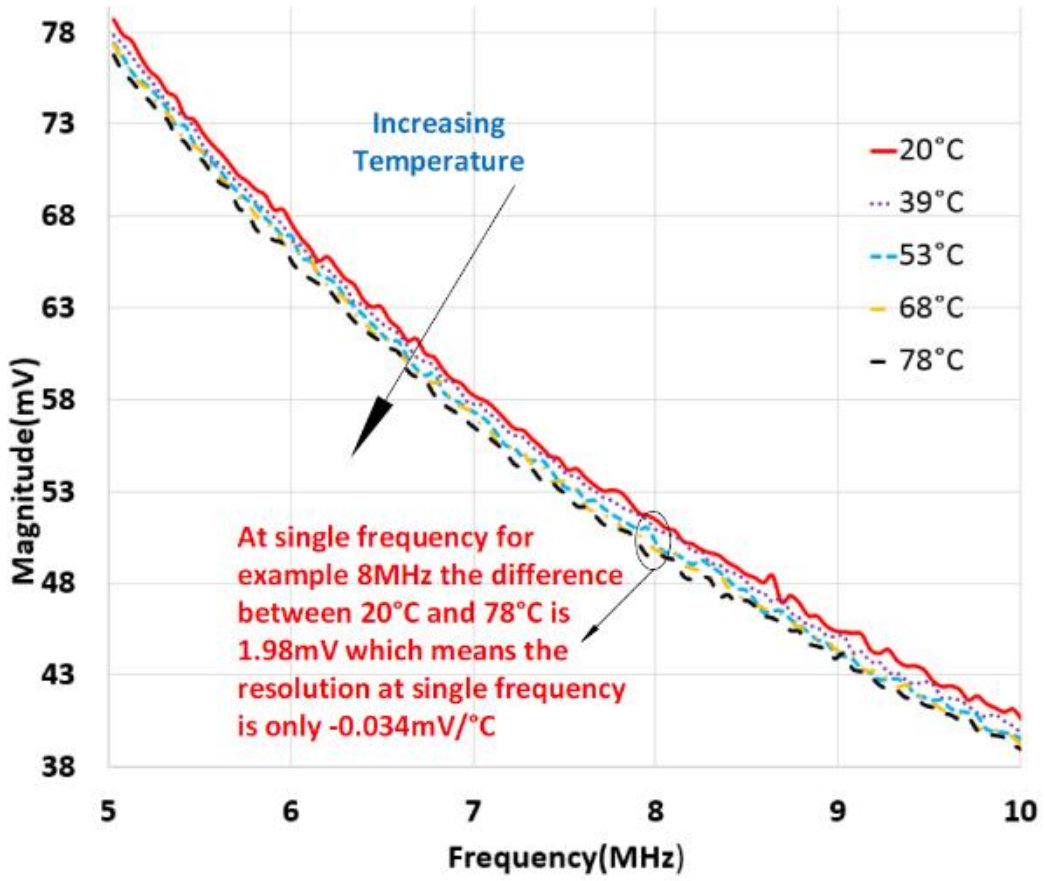
The accumulation of magnitude at each frequency consequently leads to a larger sensitivity number which is more useful in practical applications. The accumulated magnitude at five different T_j are presented which means that only five data points are presented where each data point represents one temperature. Figure 5.3(b) shows results based on the data from Figure 5.3(a), where there are only 5 data points. The change in measured integrated magnitude of V_{GSpeak} is nearly linear with respect to temperature. However, a linearization fitting curve has been added and is shown in Figure 5.3(b) too. The relationship between the integrated magnitude of V_{GSpeak} and temperature can be derived from the graph as follows:

$$Magnitude_{Total} = -3.0227 \times T_j + 5854.6 \tag{5.2}$$

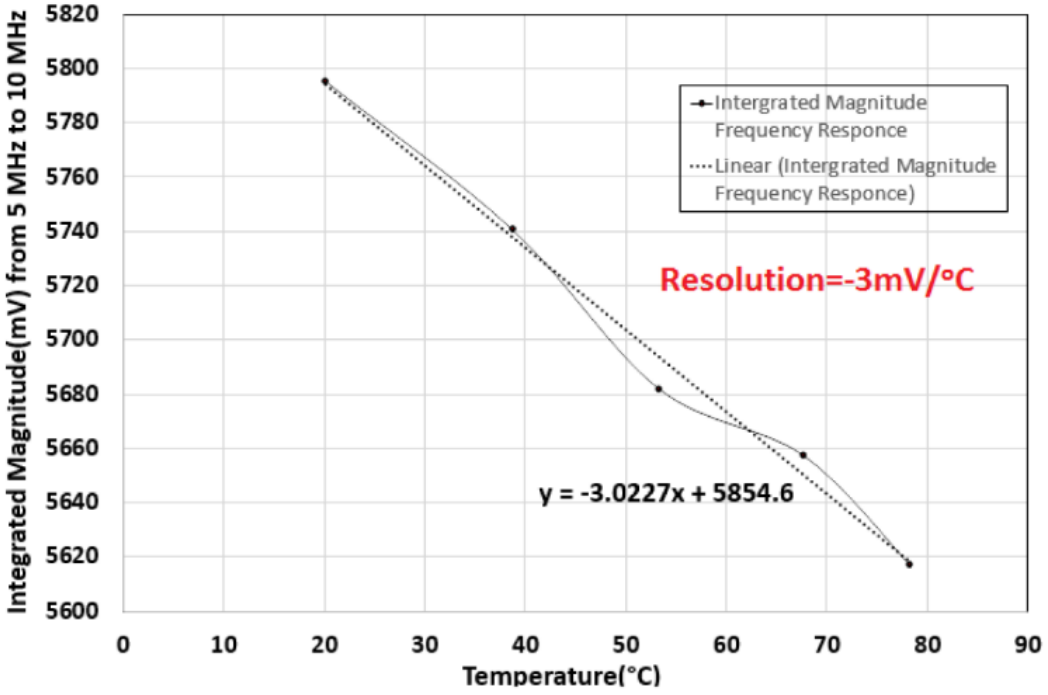
where T_j is the junction temperature.

Figure 5. 3(b) shows a sensitivity of -3 mV/°C, which is 100 times greater compared to that derived in the method described previously. In Chapter 4, the impedance frequency response of the gate-source was -1.5 mΩ/°C (linearly) for the same SiC MOSFET. However, in the

verification test set-up in Chapter 4, an expensive network analyser was used. In this experimental set-up, the magnitude frequency response of gate-source voltage is analysed, and the results also present a nearly linear relationship with a good resolution factor of $-3\mathrm{mV}/^{\circ}\mathrm{C}$. However, the proposed technique only requires a standard frequency generator and a Pico-scope, which reduces the hardware complexity and cost.



(a)



(b)

Figure 5. 3 Frequency response analysis: (a) Frequency response of magnitude of V_{GSpeak} from 5 MHz to 10 MHz; (b) integrated magnitude of V_{GSpeak}.

In this section, a possible alternative to determine the junction temperature of SiC MOSFETs is tested under unbiased conditions. High frequency voltage signals with low amplitude are injected into an unbiased SiC MOSFET to excite the gate-source impedance. The voltage is recorded and an FFT analysis is performed. All values of magnitude of V_{GSpeak} for each frequency are integrated over a frequency range from 5 MHz to 10 MHz at different temperatures. It can be seen that the integrated amplitude shows a nearly linear dependence on temperature with a sensitivity of $-3\mathrm{mV}/°\mathrm{C}$. The proposed solution requires little hardware and costs much less compared to the previously described method proposed in Chapter 4, where a network analyser was used to determine the T_j of the SiC MOSEFET. In the next section, the biased tests performed under different DC biasing conditions are presented and discussed.

5.1.2 Biased test with chirp signal injection

a. Biased test with different DC bias voltages with chirp signal directly injected

After the unbiased test has been conducted and analysed, the next step to further extend the experiment is to apply a DC bias voltage to the drain-source terminals of the SiC MOSFET. In order to achieve such a test configuration, a 4-leg inverter designed at Newcastle University is used (the schematic of the 4-leg inverter is presented in Appendix D). The schematic of the test set-up is presented in Figure 5.4.

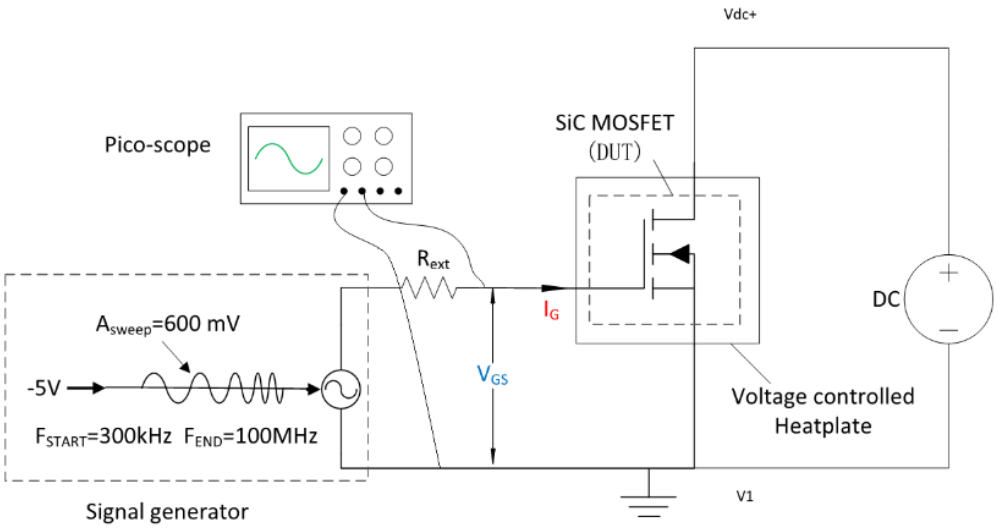


Figure 5. 4 Schematic of signal injection test under DC biased condition using a 4-leg inverter.

As shown in Figure 5.4, the SiC MOSFET is sitting in one phase leg and the drain terminal is connected to node V_{dc+} while the source terminal is connected to node V_1. The V_{dc+} and V_1 nodes are also connected to a TopCon Quadro programmable DC power supply manufactured

by Regatron. The rating of the DC power supply is 600 V, 32 A and the maximum output power is 18000 W. The power supply is capable of producing constant DC voltage for various values of voltage from 0 V up to 600 V which can provide the required test conditions for the biased experiment. The low amplitude high-frequency chirp signal is generated by the function generator used in the unbiased test in the previous section. The chirp signal starts from 300 kHz to 100 MHz and the signal increment period is 1 ms which is limited by the capabilities of the signal generator. The amplitude of the chirp signal is 600 mV while comparisons are made with different amplitudes. The Pico-scope is connected between the gate and source terminals of the SiC MOSFET to collect information concerning the gate-source voltage of the device. The SiC MOSFET chip is sitting on a voltage-controlled heat plate, the temperature of which is controlled by the voltage source. This heat plate is used to heat up the SiC MOSFET chip in fixed temperature steps in order to achieve different values of T_j. To give a direct impression of the test set-ups, several photographs of the test rig are presented below.

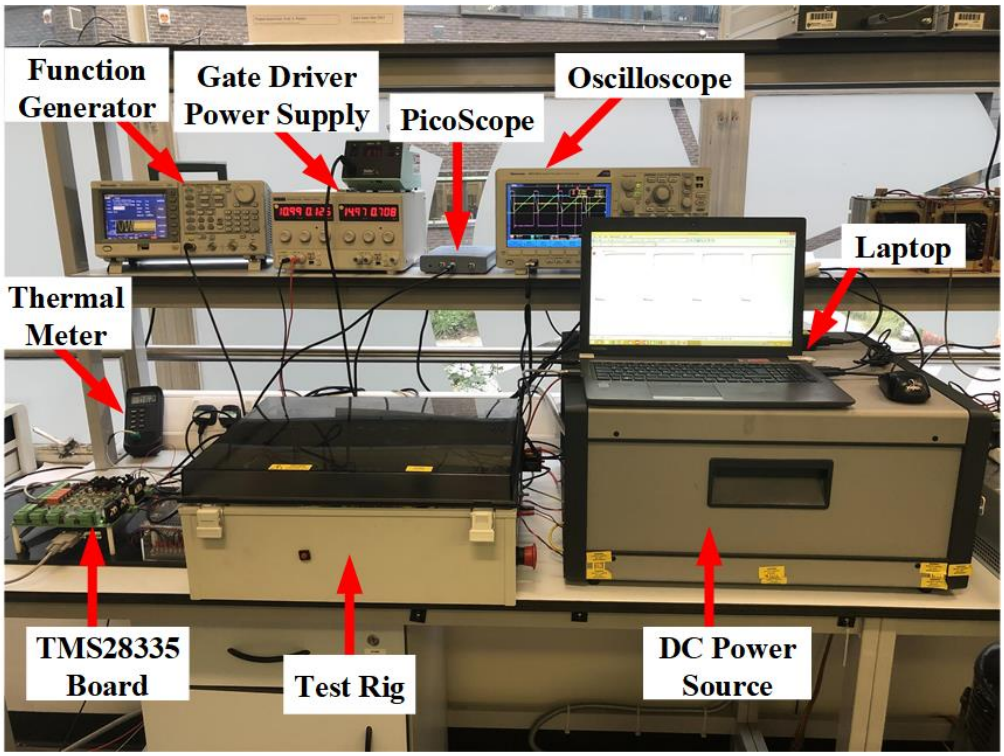
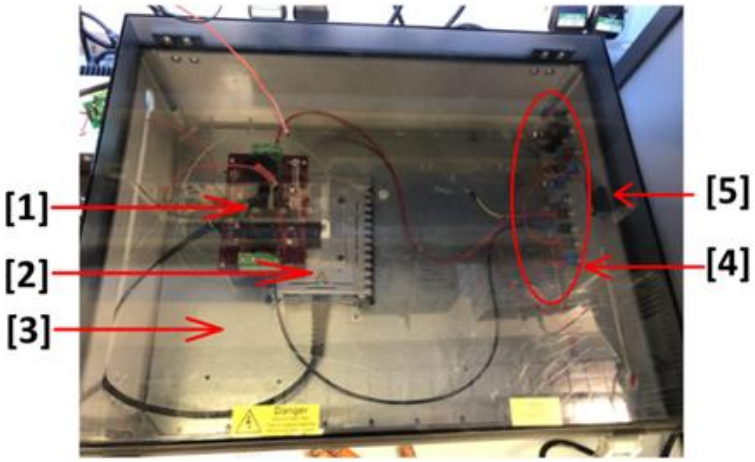


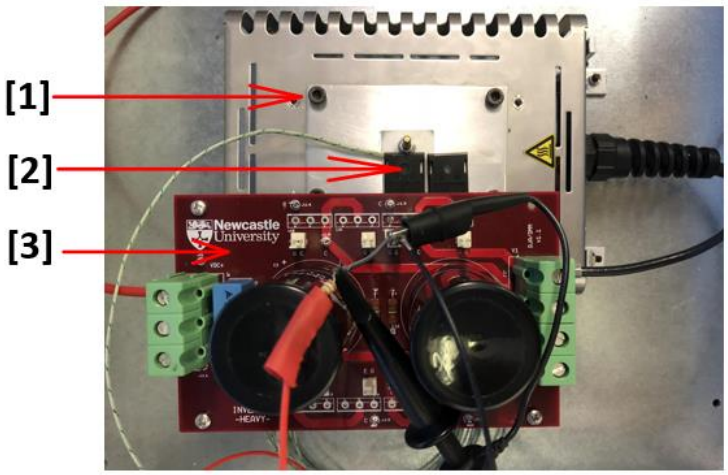
Figure 5. 5 Photograph of the overall test rig set-up.

The experimental test set-up is presented in Figure 5.5. Firstly, the function generator will generate small chirp signal and inject it into the gate of the SiC MOSFET via the gate driver. And then, the Pico-scope will measure the gate-source voltage and transfer the data to the laptop

connected to the Pico-scope. Finally, data will be stored and analysed after all need data is collected. The detailed test set-ups are described in the following sections.



(a)



(b)

Figure 5. 6 Biased tests: (a) test rig overview; (b) 4-leg inverter with SiC MOSFET in phase leg on voltage-controlled heat plate.

As can be seen from Figure 5.6 (a), the 4-leg inverter and the voltage-controlled heat plate are placed in an electrically isolated test rig, where [1] is the prototype 4-leg inverter, [2] is the voltage-controlled heat plate, [3] is the metal plate sitting at the bottom of the test rig, [4] is the connection points and protection circuit, and [5] is the button switch enabling the protection circuit. A protection configuration is established on the right hand-side of the test rig to make sure that the circuit cannot be switched on until the lid of the test rig has been fully closed and

the button switch connected to the interlock of the power supply is completely closed. Both the 4-leg inverter and the heat plate are firmly screwed onto a metal plate which is connected to the earth. Figure 5.6 (b) specifically focuses on the 4-leg inverter, where [1] is the voltage-controlled heat plate, [2] is the device under test (DUT) and [3] is the 4-leg inverter. As can be seen from Figure 5.6 (b), the SiC MOSFET is firmly screwed onto the heat plate. There is a Si sheet sitting between the SiC MOSFET and the heat plate to establish electrical isolation between them since the SiC MOSFET is a non-isolated type.

The experimental tests are carried out based on the test set-ups described above and the experimental results are illustrated and discussed in the following sections. The small AC signal injection test is carried out under various DC bias conditions. To begin with, a 50 V DC bias voltage is applied to the drain-source terminal of the SiC MOSFET. The gate voltage is set to be -5 V to ensure that the device is completely off during the test and then the DC voltage is directly applied over the drain-source terminal of the DUT. The small AC chirp signal sweeping from 300 kHz to 100 MHz with an amplitude of 600 mV is superimposed onto the -5 V DC bias. The signal is sent into the gate terminal of the SiC MOSFET via a 10 Ohm external resistance to limit the gate current peak. The gate-source voltage is measured by a Tektronix 500 MHz bandwidth voltage probe (Part number: P6139A). The probe is connected to the Pico-scope, and the peak values at each frequency bin are captured. The value of T_j of the SiC MOSFET is assumed to be the same as the surface temperature of the voltage controlled heat plate, and this assumption is made based on the fact that the heating time is long enough to make sure that the SiC MOSFET and the surface metal of the heat plate have reached thermal equilibrium. Once the peak voltage has been extracted at one temperature, the voltage source for the heat plate is manipulated to increase the temperature of the heat plate in fixed temperature steps. The data for the gate-source voltage peak at each temperature are stored in the PC connected to the Pico-scope. The results are shown in Figure 5.7 below.

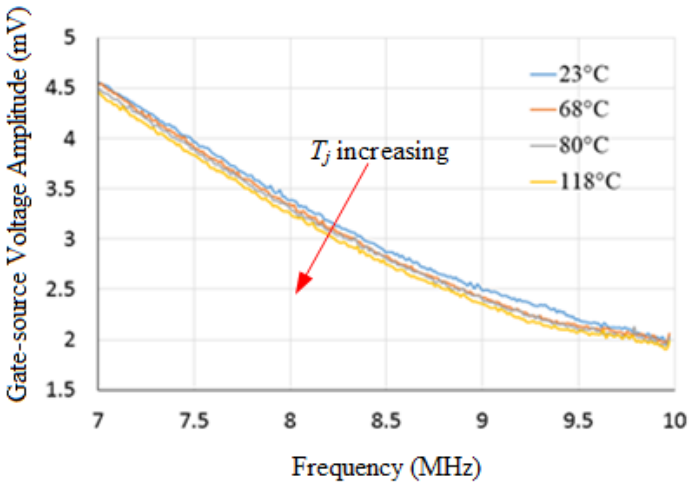


Figure 5. 7 V_{GSPeak} against f (from 7 MHz to 10 MHz) at different values of T_j under 50 V DC biasing.

It can be seen clearly from the graph in Figure 5.7 that, with the increment in T_j, the peak gate-source voltage across the gate-source terminal is reduced. This is due to the decrease in the impedance value of the internal gate resistance (R_{int}). This can be explained by considering the equivalent circuit of the gate-source loop of the SiC MOSFET during the off-state. The equivalent circuit can be described using the equation 5.3 below:

$$V_{sweep} = V_{ext} + V_{int} + V_{leads} + V_{bond-wire} + V_{stray} \tag{5.3}$$

where V_{sweep} is the voltage of the injected small AC chirp signal, V_{ext} and V_{int} are the voltages across the external resistance and across the internal resistance respectively, V_{leads} is the sum of the total voltage across the gate and the source leads, $V_{bond\text{-}wire}$ is the total voltage across both the gate bond-wire and source bond-wires, and V_{stray} is the voltage across the stray impedance.

It has been assumed in the previous analysis in chapter 4 that the impedance of the external gate resistor, the gate and source leads and gate and source bond-wires as well as the stray impedance are merely influenced by the change of the T_j, and thus the only parameter that changes with the fluctuations in T_j is the internal gate resistance. As the experimental test in the chapter 4 indicated, the impedance of the internal gate resistor is reduced linearly with increasing T_j. In these circumstances, the value of V_{int} can be expressed as equation 5.4:

$$V_{int} = V_{sweep} \times \frac{Z_{int}}{Z_{ext}+Z_{int}+Z_{leads}+Z_{bond-wire}+Z_{stray}} \tag{5.4}$$

where Z_{int} is the impedance of the internal gate resistor, Z_{ext} is the impedance of the external resistor, Z_{leads} are the impedances of the sum of the gate lead impedances and source lead

impedances, $Z_{bond\text{-}wire}$ is the sum of the gate bond-wire impedance and the source bond-wire impedance and Z_{stray} is the stray impedance.

When T_j increases, Z_{int} becomes smaller while the rest of the impedances remain the same. Then V_{int} becomes:

$$V_{int} = V_{sweep} \times \frac{Z_{int\_smaller}}{Z_{ext}+Z_{int\_smaller}+Z_{leads}+Z_{bond-wire}+Z_{stray}} \tag{5.5}$$

The values of V_{int} at lower T_j and higher T_j can be compared, as shown in equation 5.6 below:

$$V_{inlowT} - V_{inhighT} = V_{sweep} \times \left(\frac{Z_{inlowT}}{Z_{ext}+Z_{inlowT}+Z_{leads}+Z_{bond-wire}+Z_{stray}} - \frac{Z_{inhighT}}{Z_{ext}+Z_{inthighT}+Z_{leads}+Z_{bond-wire}+Z_{stray}}\right) \tag{5.6}$$

where $V_{intlowT}$ is the voltage across the internal gate resistor at low T_j and $V_{inthighT}$ is the voltage across the internal gate resistor at high T_j, and accordingly $Z_{intlowT}$ and $Z_{inthighT}$ are the impedance of the internal gate resistor at low and high values of T_j respectively.

The total impedance excluding the internal resistor can be written as follows:

$$Z_{total} = Z_{ext} + Z_{leads} + Z_{bond-wire} + Z_{stray} \tag{5.7}$$

Then equation 5.7 is inserted into equation 5.6, equation 5.7 becomes:

$$V_{inlowT} - V_{inhighT} = V_{sweep} \times \left(\frac{Z_{inlowT}}{Z_{inlowT}+Z_{total}} - \frac{Z_{inhighT}}{Z_{inhighT}+Z_{total}}\right) \tag{5.8}$$

And equation 5.8 can then be rewritten as:

$$V_{inlowT} - V_{inhighT} = V_{sweep} \times \left(\frac{Z_{total}(Z_{inlowT}-Z_{inhighT})}{(Z_{inlowT}+Z_{total})\times Z_{inhighT}+Z_{total})}\right) \tag{5.9}$$

As mentioned in the previous section, the value of Z_{inlowT} is bigger than $Z_{inthighT}$, while the other terms in the equation are all positive, and so it can be concluded that $V_{intlowT}$ is always higher than $V_{inthighT}$, which is matched with the experimental results.

Frequencies ranging from 7 MHz to 10 MHz are extracted from the whole frequency range due to the bigger peak voltage discrepancy between different values of T_j and the relatively linear relationship between the gate-source peak voltage and T_j. Not only is this frequency range is close to the resonant frequency of the gate-source impedance loop, which means that resistance becomes the most dominant component in the composition of the impedance, but also the

bandwidth capability of the sensing equipment utilized in the experiment has been taken into consideration.

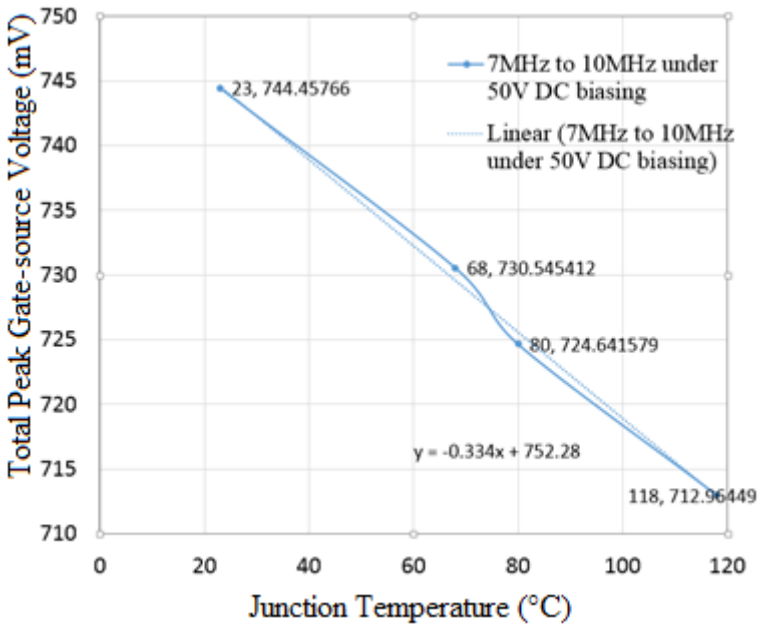


Figure 5. 8 Value of $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 50 V DC biasing against T_j.

In Figure 5.8, the dependency of the total peak gate-source voltage ($V_{GSPeakTotal}$) in the frequency range between 7 MHz and 10 MHz are plotted against the measured T_j based on the data captured by the Pico-scope. A total of four temperatures are recorded during this test starting from room temperature (25 °C), however due to thermal convection and conduction, the actual value of T_j is lower than expected, and in this test, it is only23 °C. Another three temperatures，68 °C， 80 °C and118 °C, are used as well. The results illustrated in Figure 5.8 clearly show that the accumulated $V_{GSPeakTotal}$ is reduced linearly with increasing T_j. The data points are linearized, and a trend line can be estimated, as shown in Figure 5.8, and the relationship between $V_{GSPeakTotal}$ and T_j can be expressed as:

$$V_{GSPeakTotal} = -0.334 \times T_j + 752.28 \tag{5.10}$$

This means that the sensitivity of $V_{GSPeaktotal}$ is -0.334 mV/°C. Further discussion of sensitivity and related parameters which would influence the sensitivity of $V_{GSPeaktotal}$ will be presented in the following sections.

To further examine the influence of the variation in DC biasing voltage, the above-described tests are carried out at DC biasing values of 100 V, 200 V, 300 V, 400 V, 500 V and 600 V.

As with the test at 50 V DC biasing, values of V_{GSPeak} at 100 V DC biasing between the frequencies of 7 MHz and 10 MHz (increment step is 1220Hz) are shown in Figure 5.9.

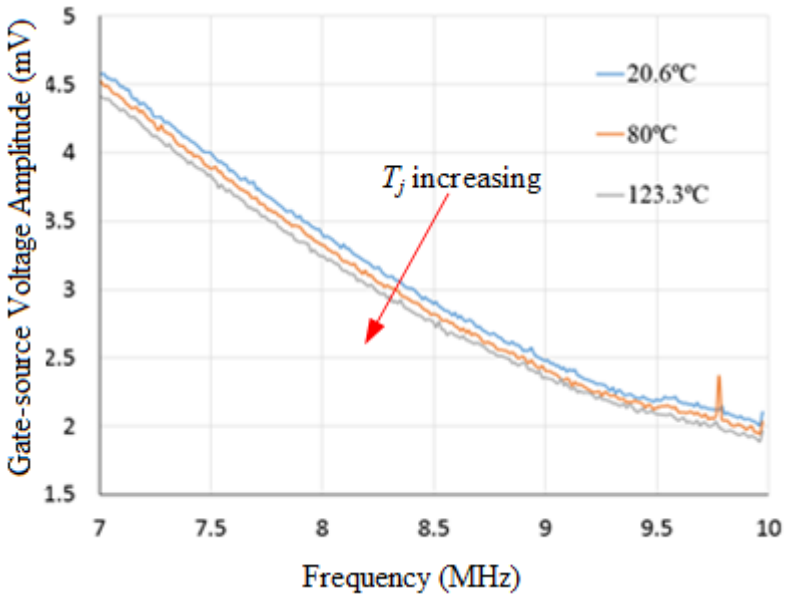


Figure 5. 9 V_{GSPeak} against f (from 7 MHz to 10 MHz) at different T_j under 100 V DC biasing.

The results for $V_{GSPeaktotal}$ against T_j under 100 V DC biasing conditions are also plotted and presented in Figure 5.10.

The linearized relationship between $V_{GSPeaktotal}$ and T_j under the 100 V DC biasing condition can be determined as:

$$V_{GSPeakTotal} = -0.3398 \times T_j + 754.68 \tag{5.11}$$

The sensitivity of $V_{GSPeaktotal}$ under the 100 V DC biasing condition is therefore -0.3398 mV/°C.

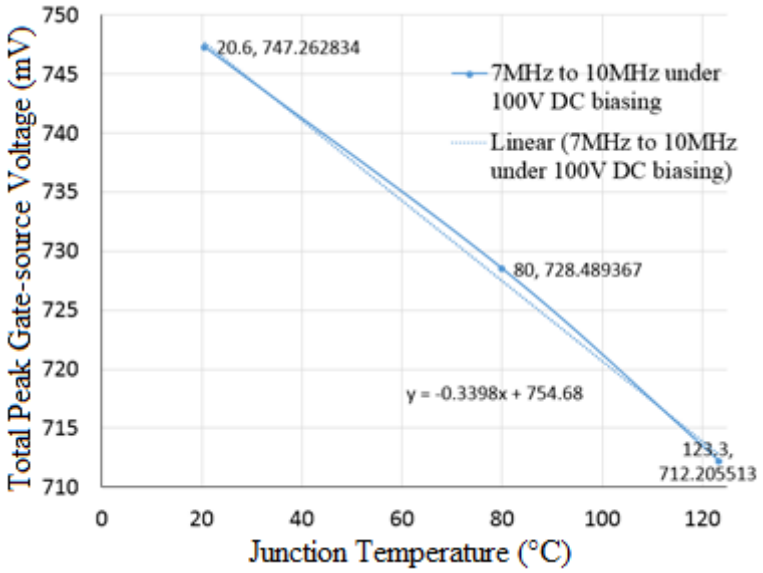


Figure 5. 10 $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 100 V DC biasing against T_j.

For the 200V DC biasing condition, the change in V_{GSPeak} between 7 MHz and 10 MHz is illustrated in Figure 5.11.

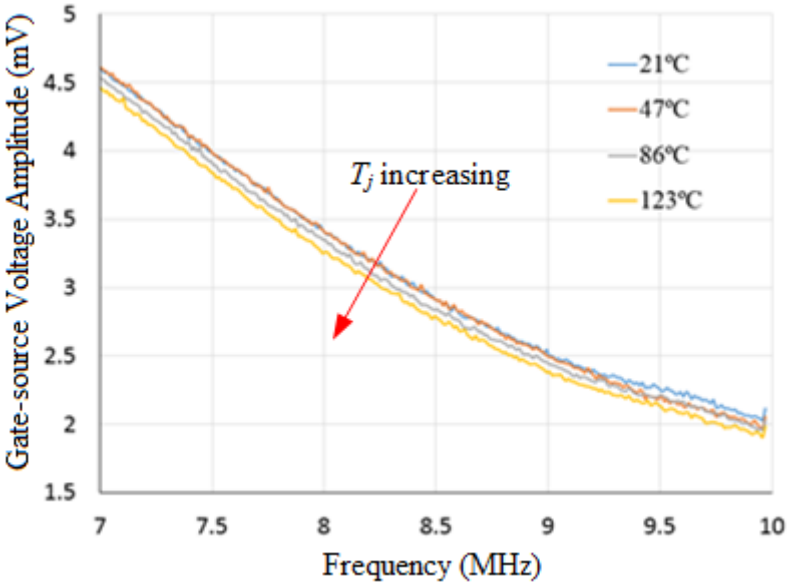


Figure 5. 11 V_{GSPeak} against f (from 7 MHz to 10 MHz) at different T_j under 200 V DC biasing.

Similarly, the change in $V_{GSPeaktotal}$ against T_j under 200 V DC biasing is presented in Figure 5.12.

The linearized relationship between $V_{GSPeaktotal}$ and T_j under the 200 V DC biasing condition can be calculated as:

$$V_{GSPeakTotal} = -0.3381 \times T_j + 758.7 \quad (5.12)$$

The sensitivity of $V_{GSPeaktotal}$ under 200 V DC biasing condition is thus -0.3381mV/°C.

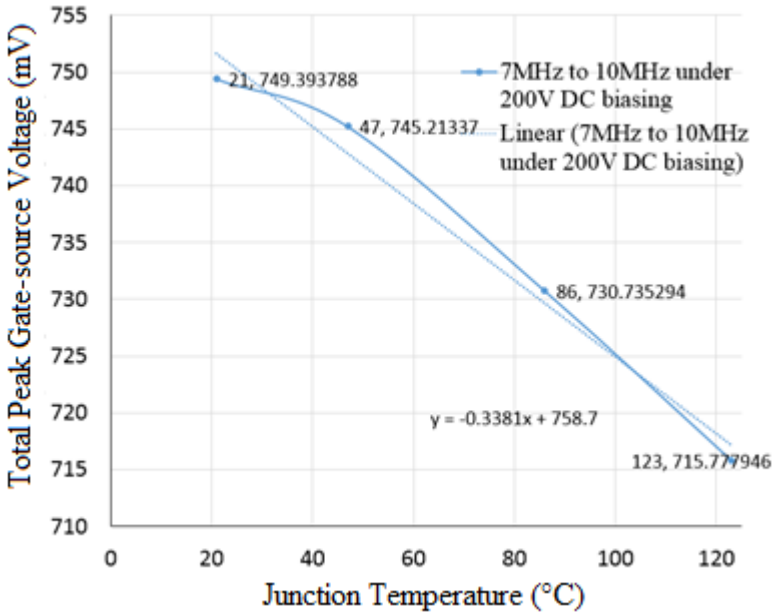


Figure 5. 12 $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 200 V DC biasing against T_j.

When the DC biasing is increased to 300 V, the change in V_{GSPeak} between 7 MHz and 10 MHz is illustrated in Figure 5.13.

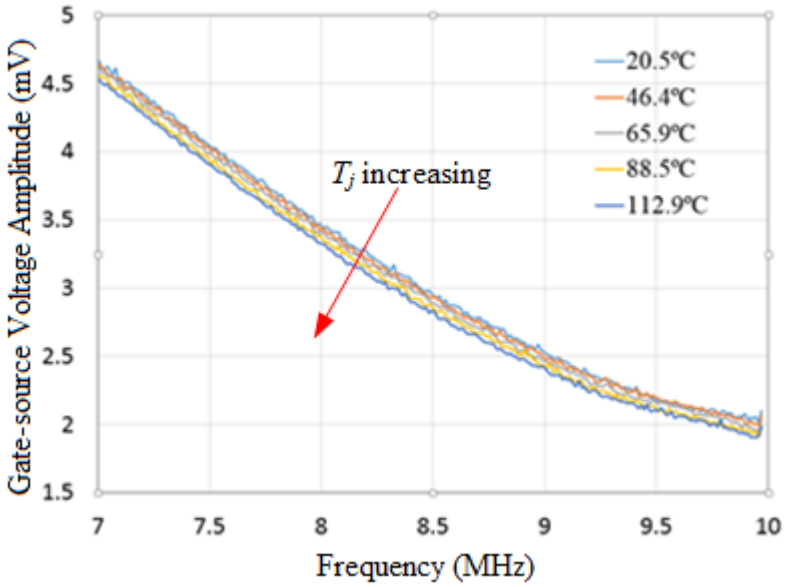


Figure 5. 13 V_{GSPeak} against f (from 7 MHz to 10 MHz) at different T_j under 300 V DC biasing.

To examine the sensitivity of $V_{GSPeaktotal}$, it is compared with T_j as illustrated in Figure 5.14.

The linearized relationship between $V_{GSPeaktotal}$ and T_j under 300 V DC biasing condition can be calculated as:

$$V_{GSPeakTotal} = -0.3561 \times T_j + 766.16 \tag{5.13}$$

The sensitivity of $V_{GSPeaktotal}$ under 300 V DC biasing condition is then -0.3561mV/°C.

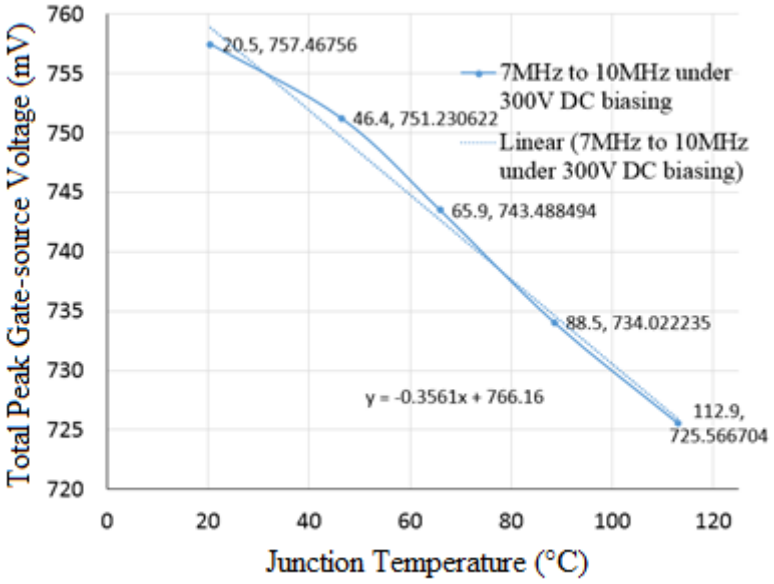


Figure 5. 14 $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 300 V DC biasing against T_j.

For the 400 V DC biasing condition, the change in V_{GSPeak} in the frequency range from 7 MHz to 10 MHz is depicted in Figure 5.15.

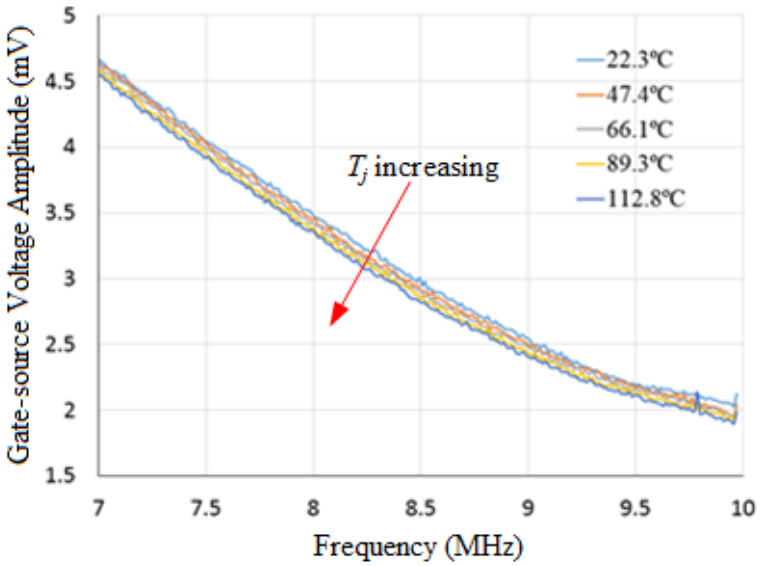


Figure 5. 15 V_{GSPeak} against f (from 7 MHz and 10 MHz) at different T_j under 400 V DC biasing.

The relationship between the 400 V DC biased $V_{GSPeaktotal}$ and different T_j conditions is illustrated in Figure 5.16.

The linearized relationship between $V_{GSPeaktotal}$ and T_j under the 400 V DC biasing condition can be determined as:

$$V_{GSPeakTotal} = -0.3465 \times T_j + 765.85 \tag{5.14}$$

The sensitivity of $V_{GSPeaktotal}$ under the 400 V DC biasing condition is -0.3465mV/°C.

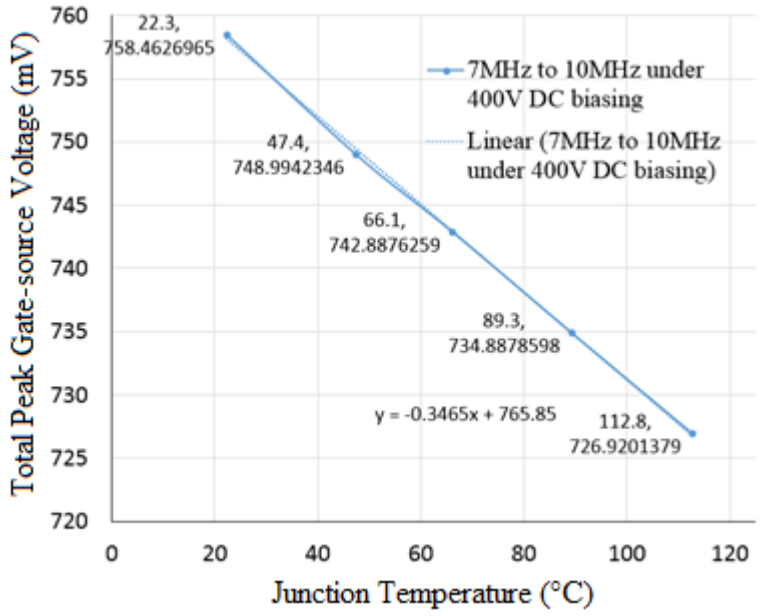


Figure 5. 16 $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 400 V DC biasing against T_j.

When a 500 V DC biasing voltage is applied to the drain-source terminal of the SiC MOSFET, the results for V_{GSPeak} in the frequency range from 7 MHz to 10 MHz are plotted in Figure 5.17.

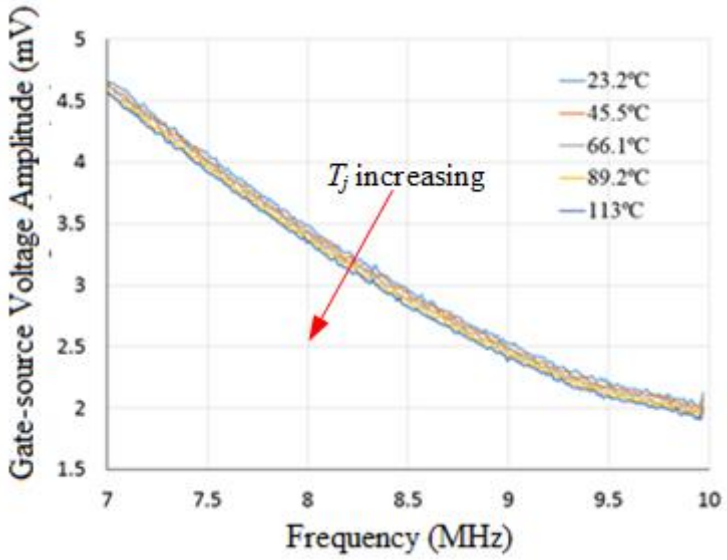


Figure 5. 17 V_{GSPeak} against f (from 7 MHz to 10 MHz) at different T_j under 500 V DC biasing.

The corresponding values of $V_{GSPeaktotal}$ under the 500 V DC biasing condition are compared with the changing T_j and plotted in Figure 5.18.

The linearized relationship between $V_{GSPeaktotal}$ and T_j under the 500 V DC biasing condition can be determined as:

$$V_{GSPeakTotal} = -0.3235 \times T_j + 765.62 \tag{5.15}$$

The sensitivity of $V_{GSPeaktotal}$ under 500 V DC biasing condition is thus $-0.3235\text{mV}/°\text{C}$.

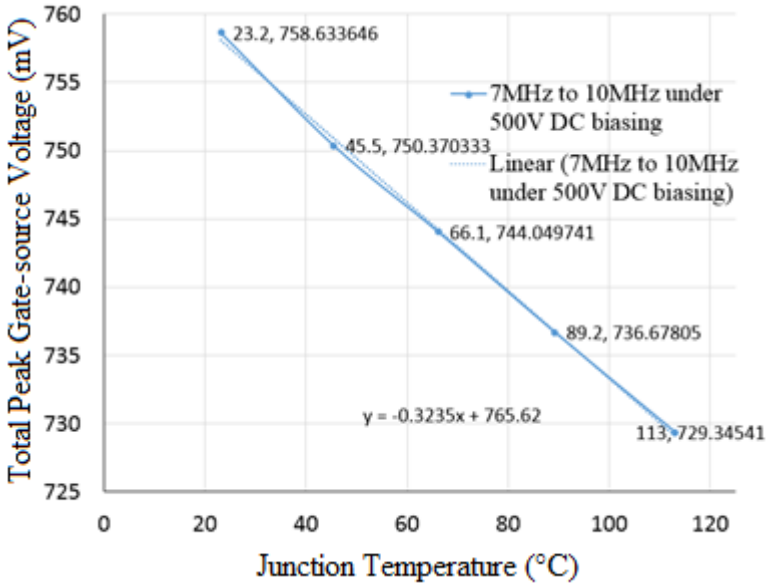


Figure 5. 18 $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 500 V DC biasing against T_j.

The final set of tests is carried out under 600 V DC biasing. The change in V_{GSPeak} at frequencies between 7 MHz and 10 MHz at this voltage level is presented in Figure 5.19.

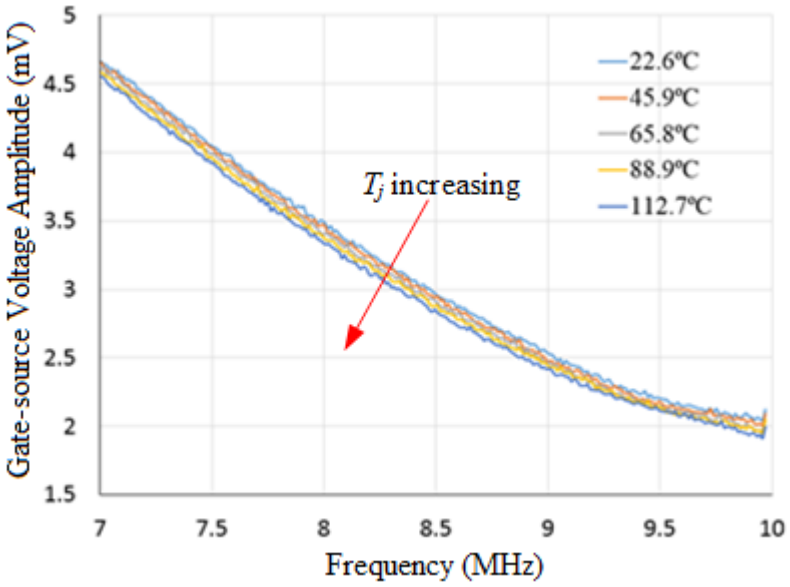


Figure 5. 19 V_{GSPeak} against f (from 7 MHz to 10 MHz) at different T_j under 600 V DC biasing.

The change in $V_{GSPeaktotal}$ under the 600 V DC biasing condition against varying T_j is illustrated in Figure 5.20.

The linearized relationship between $V_{GSPeaktotal}$ and T_j under the 600 V DC biasing condition can be determined as:

$$V_{GSPeakTotal} = -0.32 \times T_j + 766.25 \quad (5.16)$$

The sensitivity of $V_{GSPeaktotal}$ under the 600 V DC biasing condition is then -0.32mV/°C.

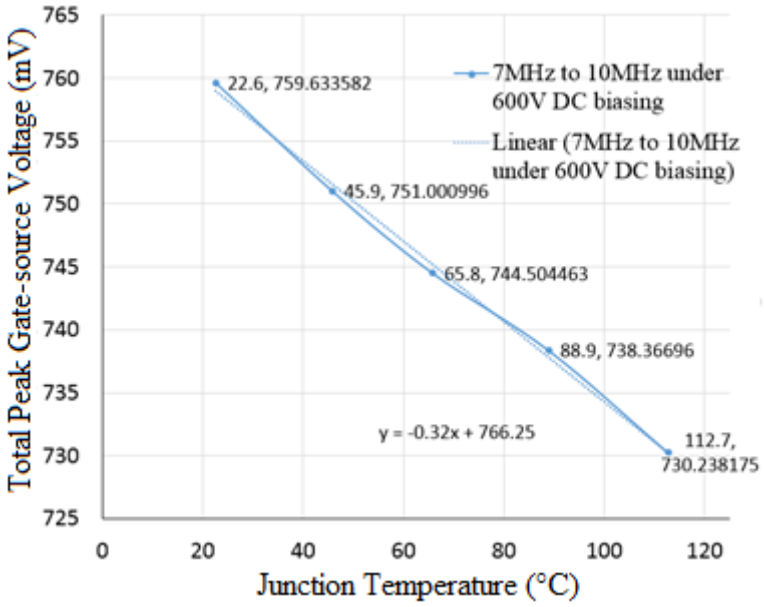


Figure 5. 20 $V_{GSPeaktotal}$ between 7 MHz and 10 MHz under 600 V DC biasing against T_j.

All of the above the DC biasing conditions are compared to investigate the influence of DC biasing voltage on the estimation of T_j based on the small AC signal injection. As shown in Figure 5.21, the above 7 different DC biasing conditions are plotted in one chart.

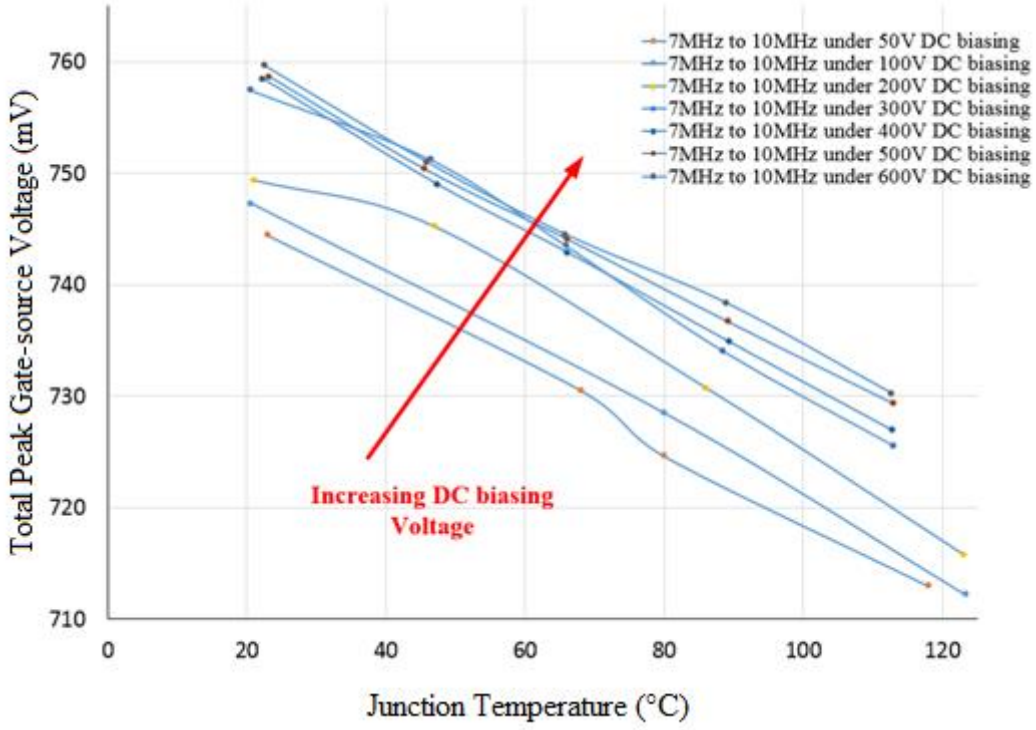


Figure 5. 21 Comparison of DC biasing conditions for small AC signal injection technique.

As can be seen from Figure 5.21, the trend lines for $V_{GSPeaktotal}$ for different DC biasing conditions are almost entirely in parallel with each other, which indicates that the slopes of the trend lines are almost the same. This means that the sensitivity for each DC biasing conditions are very close to each other. This can be summarized in Table 5.1.

Table 5. 1 Sensitivity of $V_{GSPeaktotal}$ at different DC biasing voltage conditions

DC biasing voltage	Sensitivity of $V_{GSPeaktotal}$
50 V	-0.3340 mV/°C
100 V	-0.3398 mV/°C
200 V	-0.3381 mV/°C
300 V	-0.3561 mV/°C
400 V	-0.3465 mV/°C
500 V	-0.3235 mV/°C
600 V	-0.3200 mV/°C

The average sensitivity of the $V_{GSPeaktotal}$ under these seven DC biasing conditions can be calculated as -0.3369 mV/°C. The highest sensitivity is under 300 V DC biasing, at -0.3561 mV/°C and the lowest is under the 600 V DC biasing condition at -0.32 mV/°C. The

difference between the highest and average sensitivity is $0.0192\ \mathrm{mV/°C}$, which is a difference of about 5.7%. Meanwhile the discrepancy between the lowest sensitivity and average sensitivity is $0.0169\ \mathrm{mV/°C}$ which is a difference of 5%. The sensitivities for the versions DC biasing conditions remain almost the same within a tolerance range of $\pm 5\%$.

Another point worth noting is that the absolute V_{GSPeak} at fixed frequency changes due to the variation in DC biasing voltage. It can be seen from Figure 5.21 that, with increasing DC biasing voltage, the trend line moves upwards which indicates that at each frequency the V_{GSPeak} value is higher when the DC biasing voltage is higher. This is due to the fact that the T_j-dependent R_{int} is not a lumped resistance but an equivalent resistance of the parasitic capacitance.

b. Biased test under DC biasing voltage with chirp signal injected via gate driver

In the previous section, the small AC chirp signal and the minus DC biasing voltage are both generated by the function generator. This is a viable solution that can be implemented in a laboratory environment. However, in order to apply this small signal injection technique in real applications, the minus bias DC voltage should be provided by a SiC MOSFET gate driver. Thus, how to superimpose the small signal onto the minus DC bias voltage generated by the gate driver and then to apply it to the gate terminal of the SiC MOSFET becomes an issue. To address this issue, a solution utilizing a pulse transformer is proposed, and this is discussed in detail in the following sections.

In this particular test, a Cree gate driver board for the 2nd generation (C2M™) SiC MOSFET (Part number: CRD-001) is utilized to drive the C2M0080120D SiC MOSFET. The basic schematic of the gate driver is presented in Figure 5.22, and other documents regarding this gate driver board are presented in Appendix E including specifications and relevant schematics.

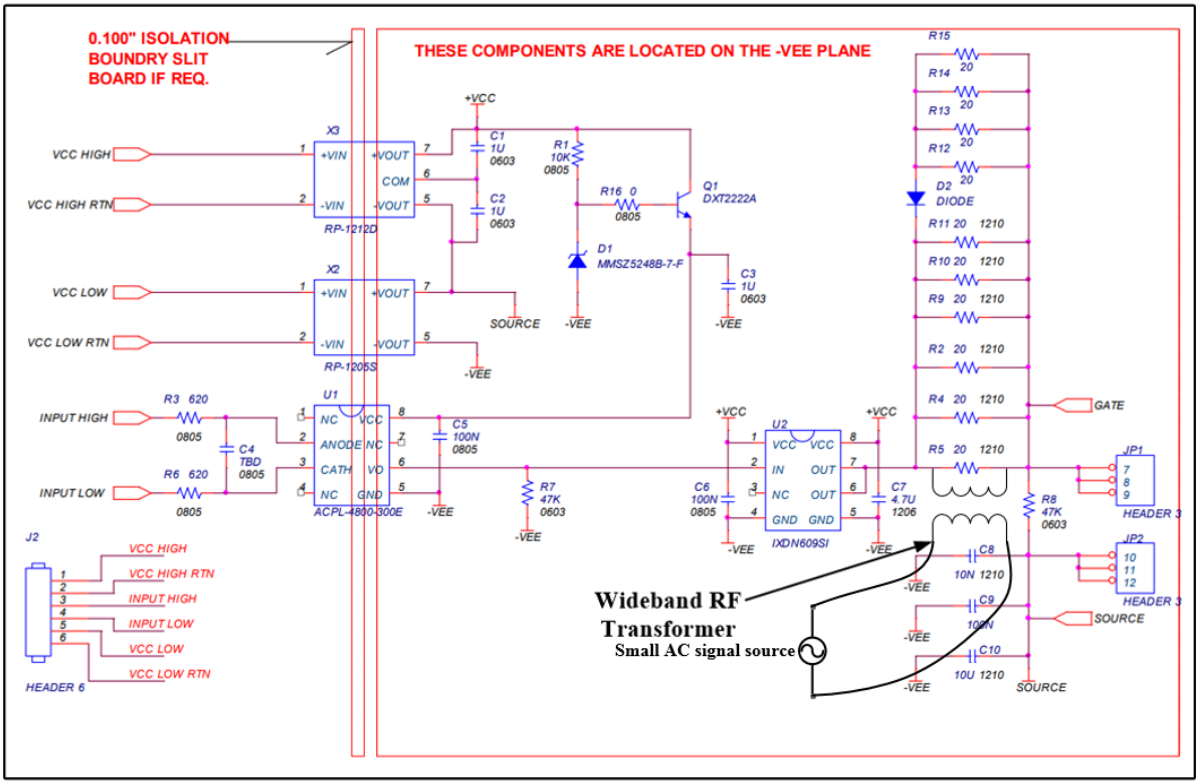


Figure 5. 22 Schematics for Cree CRD-001 gate driver for 2nd generation SiC MOSFET.

The gate driver used in this test is basically a pull-push voltage gate driver. The high level and low levels of the gate signal can be manipulated by changing the input voltage level into the gate driver. As shown in Figure 5.22, the value of V_{CCHIGH} determines the high level of the gate signal while V_{CCLOW} determines its low level, and in this test the low-level gate signal is set to be -5 V. Since the input voltage from the voltage source for the gate driver is isolated by two DC-DC converters, the top isolated DC-DC converter (RP-1212D) is for the high level gate signal and the bottom isolated DC-DC converter (RP-1205S) is for the low level gate signal. However, it is not easy to superimpose the small AC chirp signal from the voltage source side directly. Therefore, in this test, the alternative of a wideband RF transformer is applied to superimpose the high frequency small AC chirp signal. The wideband RF transformer is manufactured by Coilcraft (part number: PWB1010L), and its bandwidth is 0.0035 MHz to 125 MHz. The impedance ratio of the primary winding against the secondary winding is selected to be 1:1 in order to lead the small AC signal at the secondary side to follow the signal generated at the primary side. The attenuation of the transformer between 0.02 MHz to 30 MHz is approximately equal to zero [91]. According to the data sheet provided by the manufacturer, the phase and magnitude imbalances in the same frequency range are extremely close to 0 dB [91]. These characteristics make this transformer be quite suitable for implementation in this test. A chirp signal of peak-to-peak 1.2 V sweeping from 5 MHz to

10MHz is injected into the wide-band RF transformer and the input and output signals are compared and presented in figures illustrated below. In these three figures, the dark-blue curve is the input signal (channel 1) and the light-blue curve is the output signal (channel 2).

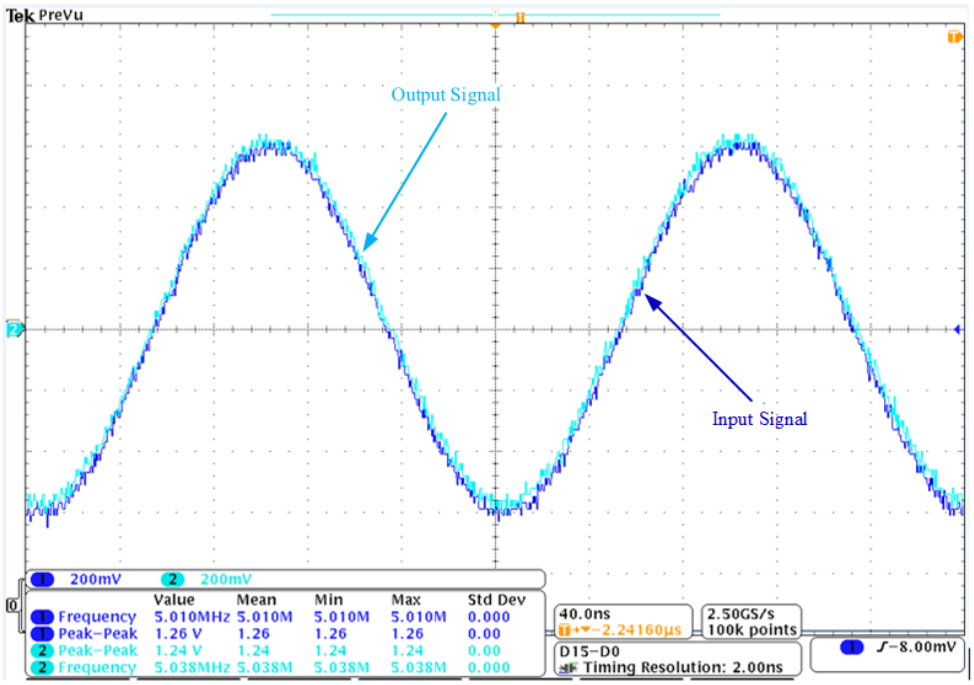


Figure 5. 23 Chirp signal input and output comparison at 5 MHz by using wide-band RF transformer.

It can be seen from Figure 5.23, for the chirp signal at 5 MHz, despite there is a little shift between the input and output waveforms two waves forms are still almost fully overlapped with each other. It can be seen that the peak-to-peak value of the input signal is 1.26 V and the output signal is 1.24 V which means there is a 1.6 % difference which is negligible. In terms of frequency the input signal is 5.010 MHz and the output signal is 5.038 MHz the difference between two signals is 0.028 MHz which is also insignificant.

To further exam the capability of the wide-band transformer, waveforms captured by the oscilloscope around 7.4 MHz and 9.3 MHz are illustrated in Figure 5.24 and 5.25 respectively. Similar with the results presented in Figure 5.23, the output signal via the wide-band RF transformer is closely follow the pattern of the input signal.

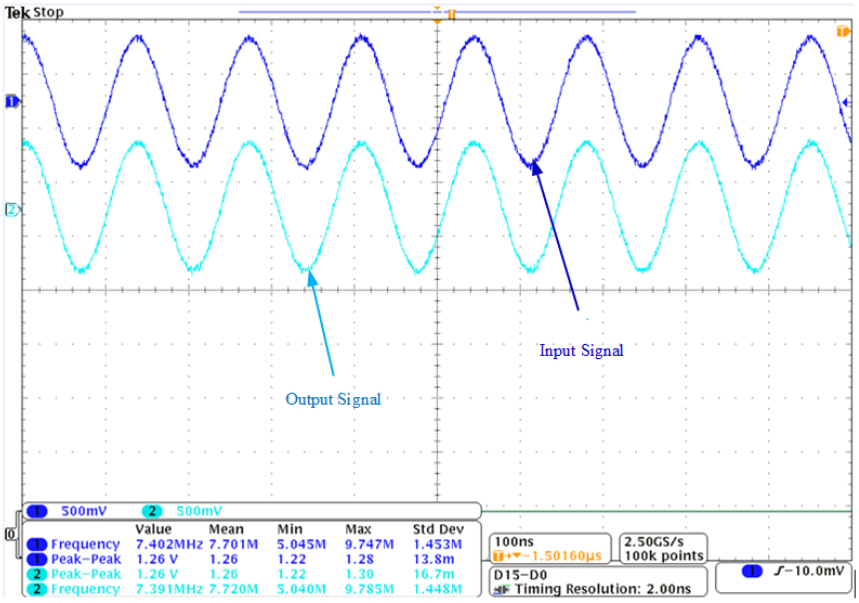


Figure 5. 24 Chirp signal input and output comparison at 7.4 MHz by using wide-band RF transformer.

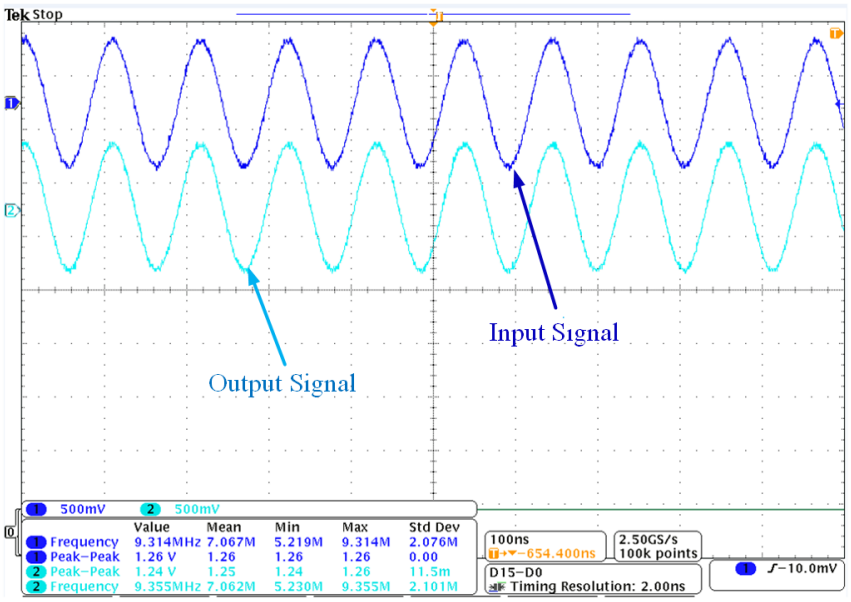


Figure 5. 25 Chirp signal input and output comparison at 9.3 MHz by using wide-band RF transformer.

As indicated in Figure 5.22, the RF transformer is sitting at the top of the output resistance R5, which means that the small AC chirp signal can be successfully superimposed onto the -5 V gate voltage.

The issue regarding how the gate driver can be used in combination with the small signal generation device to generate the required chirp signal with minus DC biasing has now been resolved, and the test can proceed by injecting the small AC chirp signal via the gate driver.

Figure 5.26 shows V_{GSPeak} against frequencies between 7 MHz to 10 MHz under 300 V DC biasing with an injection signal with a peak-to-peak amplitude of 5 V via the gate driver at different values of T_j. The reason for using a relatively large value of amplitude of the injection signal is that it is weakened by the wideband RF transformer which means that the of actual signal passing into the gate-source terminal of the SiC MOSFET is smaller than the original signal. This amplitude of the signal is controlled in a suitable range to avoid false triggering.

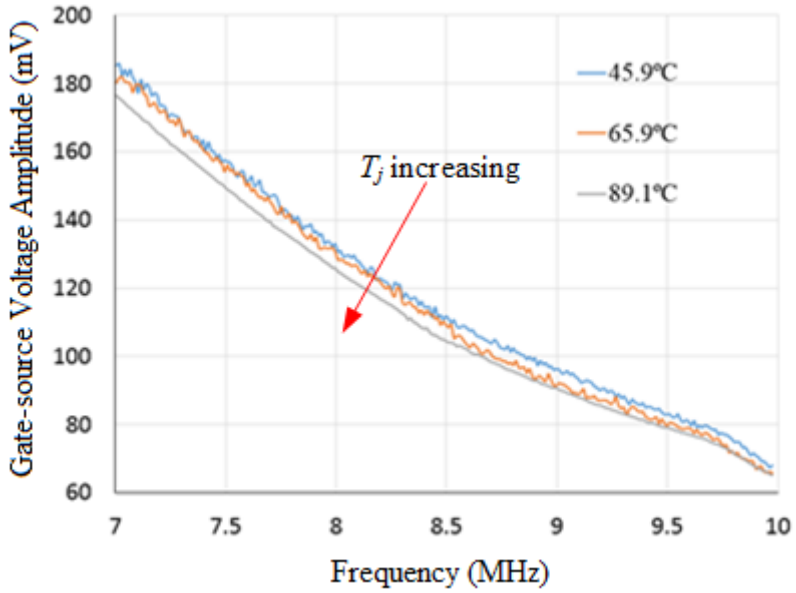


Figure 5. 26 V_{GSPeak} against f at 300 V DC biasing with injection via gate driver with 5 V peak-to-peak injection amplitude.

The V_{GSPeak} still shows a negative dependency on T_j, as illustrated in Figure 5.23. The accumulated V_{GSPeak} is also calculated and plotted in Figure 5.27. As can be seen, the $V_{GSPeaktotal}$ decrease linearly with t increasing T_j of the DUT.

The relationship between $V_{GSPeaktotal}$ and the corresponding T_j is derived as:

$$V_{GSPeakTotal} = -33.44 \times T_j + 30415 \tag{5.16}$$

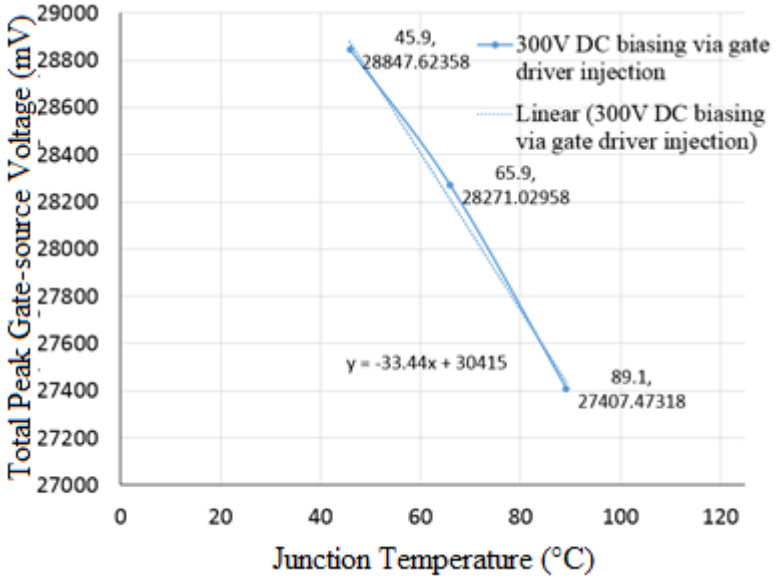


Figure 5. 27 $V_{GSPeaktotal}$ against T_j under 300 V DC biasing with injection via gate driver with 5 V peak-to-peak amplitude injection signal.

To investigate the influence of the amplitude of the injected high frequency AC signal, its amplitude is tuned to be 2 V from the function generator. The result is also presented below in Figure 5.28.

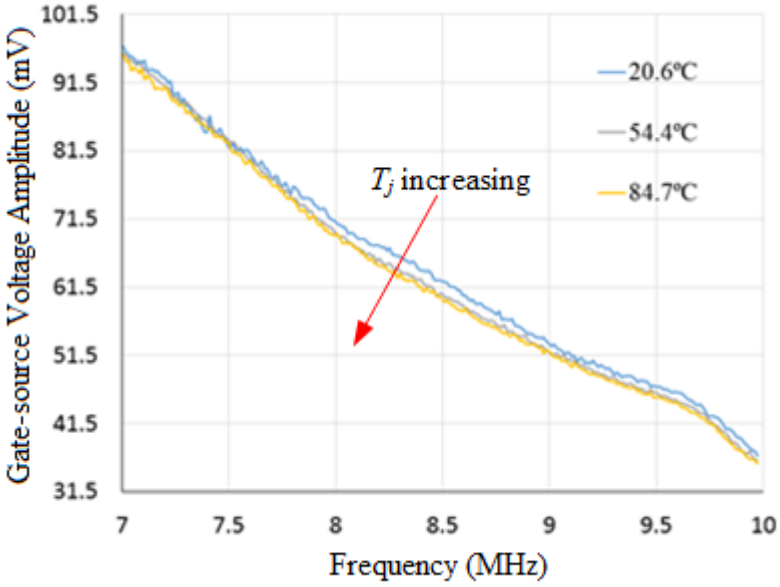


Figure 5. 28 V_{GSPeak} against f under 300 V DC biasing with injection via gate driver with 2 V injection amplitude.

When comparing Figure 5.26 and Figure 5.28, which depict V_{GSPeak} under two different amplitudes of injected voltages, it can be clearly seen that, with the higher amplitude of injected signal, the resulting V_{GSPeak} has a correspondingly higher amplitude and the differences in

V_{GSPeak} between two different T_j are also larger. This finally confirms that the sensitivity of the $V_{GSPeaktotal}$ increases with the higher injected signal amplitude. As represented in Figure 5.29, $V_{GSPeaktotal}$ is plotted against T_j of the SiC MOSFET and the linearized trend line is also derived and the relationship between the $V_{GSPeaktotal}$ and T_j can be presented as in equation 5.17:

$$V_{GSPeakTotal} = -8.1161 \times T_j + 15849 \tag{5.17}$$

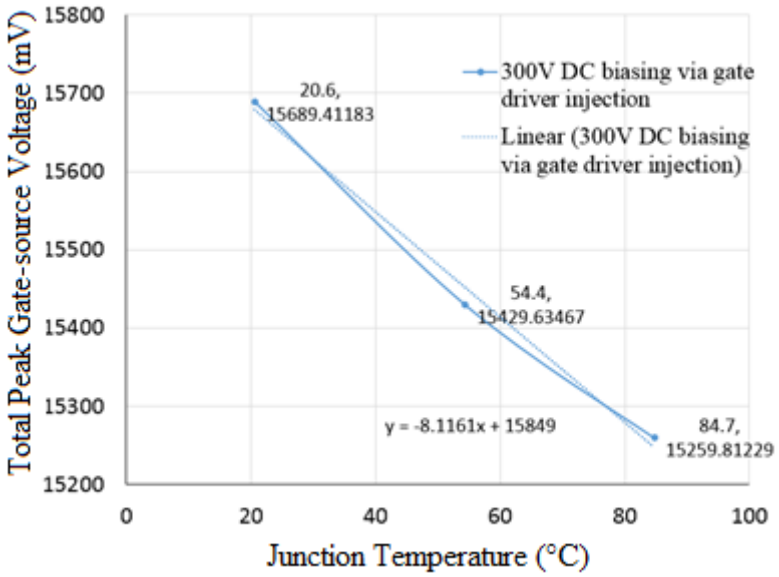


Figure 5. 29 $V_{GSPeaktotal}$ against T_j under 300 V DC biasing with injection via gate driver with 2 V peak to peak amplitude injection signal.

The values of sensitivity of $V_{GSPeaktotal}$ against T_j under a 5 V injection signal and 2 V injection signal is -33.44 mV/°C and -8.1161 mV/ °C respectively. It is obvious that higher amplitude of injection signal results in a bigger discrepancy in $V_{GSPeaktotal}$, which means a greater sensitivity. This phenomenon can be utilized to optimize the sensitivity of the $V_{GSPeaktotal}$ to find a suitable value that is big enough so as to be easily detected based on state-of-the-art sensor techniques to generate reasonable sensitivity. Meanwhile the amplitude of the injected signal should not be so big as exceed the required minus gate voltage in order to avoid the false triggering of the SiC MOSFET during normal operation.

The boost converter test is carried over based on the Cree/Wolfspeed kit8020-CRD-8FF1217P-1 evaluation boar[92]. A C2M0080120D SiC MOSFET and a C4D20120D SiC Schottky diode are used to form a non-synchronous boost DC/DC converter, the schematic is shown in Fig 5.30 that SiC MOSFET is deployed at Q1 position and SiC Schottky diode is located at Q2 position.

Appropriate input capacitor, output capacitor and input inductor are calculated and connected onto the evaluation board accordingly.

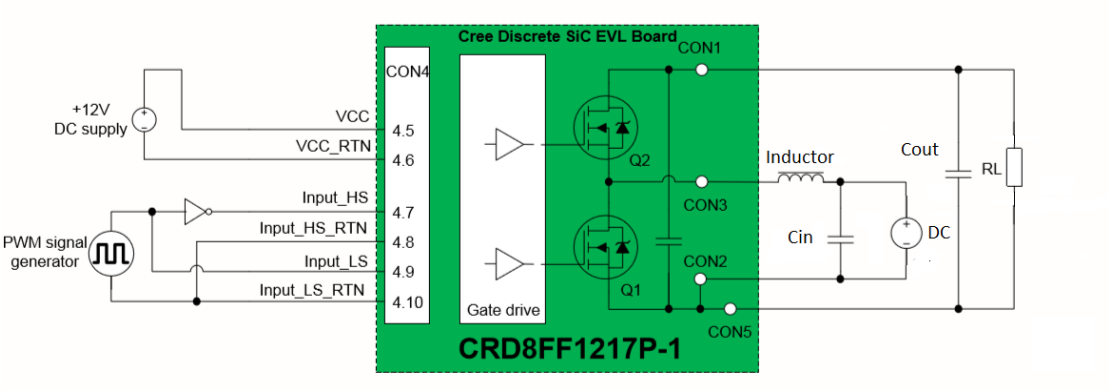
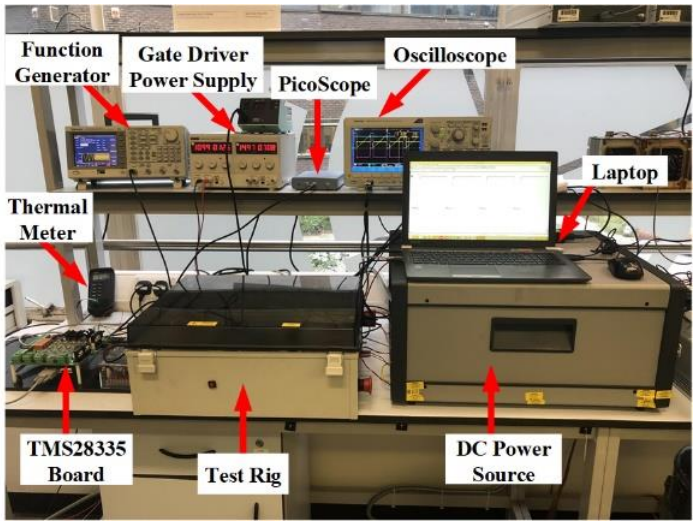
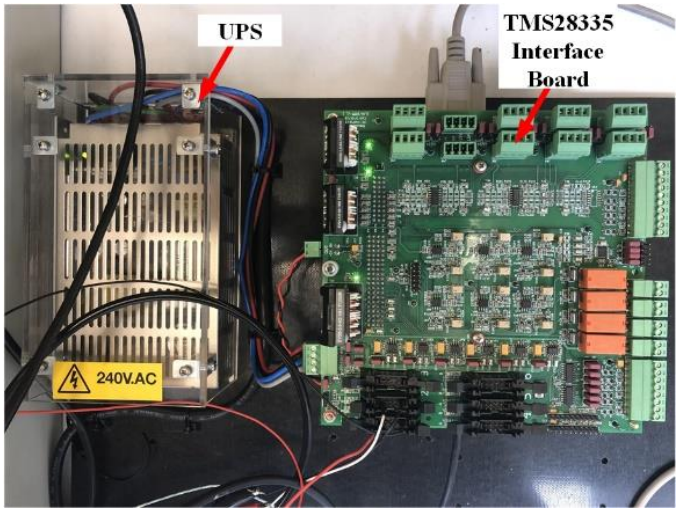


Figure 5.30 Non-synchronous boost converter configuration using Wolfspeed evaluation board.



(a)



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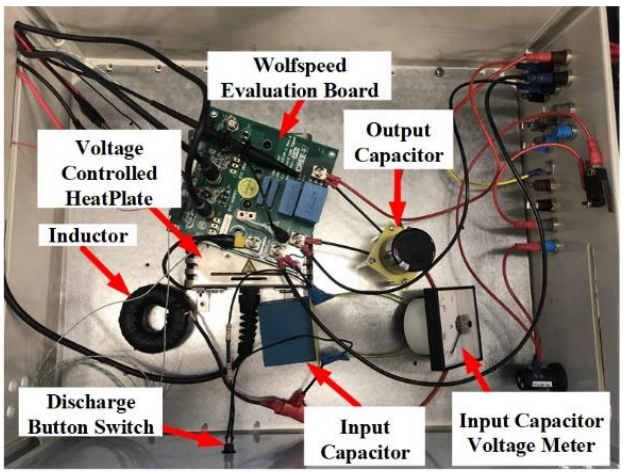


(c)

Figure 5.31 Boost converter test setup: (a) overall test bench; (b) TMS28335 PWM generating board; (c) test rig inside view.

The overall test bench is presented in Fig 5.31(a). The output of the boost converter is connected to a viable resistive load. The PWM signal is generated and controlled by using an interface board developed in Newcastle University with TMS28335 DSP board as shown in Fig 5.31(b). The output of the interface board is connected to the on-board gate driver of the evaluation board. Duty cycle can be manipulated via LabView interface in real time depending on the requirement.

As shown in Fig 5.31(c), the device under test (DUT) is soldered under the evaluation board and sitting on a voltage-controlled heat-plate, the DUT is isolated from the heat-plate with a silicon thermal pad. The heat-plate has a resolution of 1°C. The output of the DC/DC converter is a variable resistive load which has a tuning range between 30ohm and 300ohm.

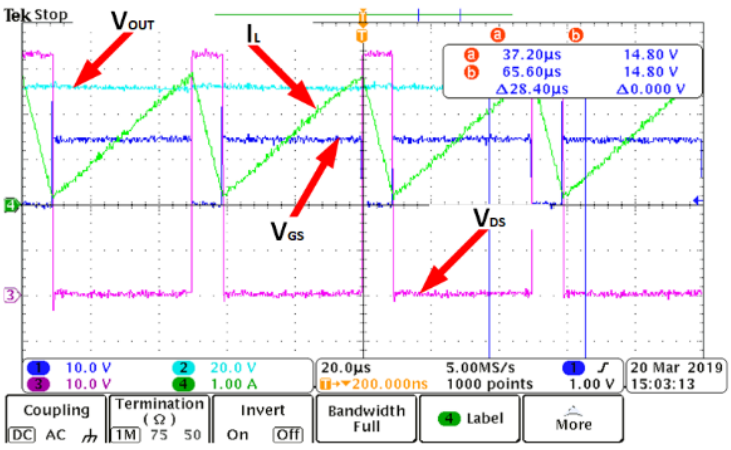


Figure 5.32 Measured oscilloscope waveforms of boost converter including output voltage, gate-source voltage, drain-source voltage and inductor current.

An example of operating voltage and current waveforms under 80% duty cycle operation is presented in Fig 5.32 Small AC chirp signal sweeping from 5MHz to 10MHz is superimposed onto the gate signal via a RF transform in parallel with the external gate resistor. As can be seen from the graph that the boost DC/DC converter is working under CCM mode. The gate-source voltage is extracted and analysed after the data has been stored in the PC.

The measured temperature is corelated with the die body temperature rise derived by the 3D thermal model at each temperature steps. The temperature rise value at each temperature are listed in the table below.

Table 5. 2 Ture junction temperature consider die body temperature rise

Tempeture Step (°C)	Die Body Temperature Rise (°C)	Measured Tempearture (°C)
25	0.541	33
50	0.547	45
75	0.569	65
100	0.59	82
125	0.65	101

The corelated temperture is calculated by adding the measured temperature with the die body temprature rise as the true T_j since the thermo coupler is detecting the SiC MOSFET temperature near the bottom drain pad. There is small fraction of change for each temperature steps, and by applying the simulated T_j rise induced by the SiC die body would minimise the error between the true T_j and measured T_j. The corelated T_j and measured off-state gate source voltage are plotted in the Figure 5.33 illustred as follow.

There is -1.6%, -1.2%, -0.08%, -0.07% and -0.064% temperature difference between the true T_j and measured T_j at 25°C,50°C,75°C, 100°C and 125°C heat plate temperature conditions respectively. The estimated ture T_j helps to increase the accuracyof the proposed method.

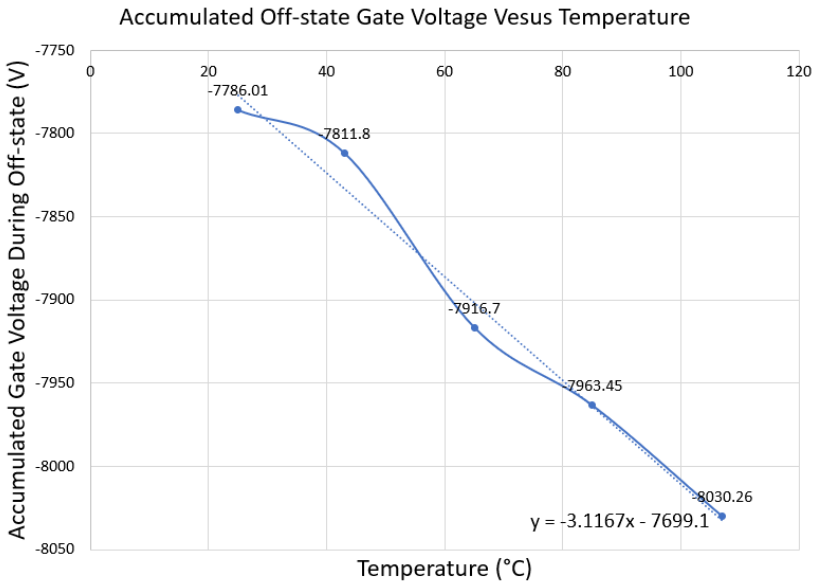


Figure 5.33 Gate-source voltage measured under 50V input DC voltage, 1.5A inductor current under 80% duty cycle at different junction temperature with superimposed 5MHz to 10MHz chirp signal.

The first experiment is carried out to test the temperature dependence of the off-state gate-source voltage with 5MHz to 10MHz superimposed chirp signal. The accumulated gate-source voltage results show a -3.1167V/°C changing rate. Each accumulated voltage value contains 1500 data points captured which is equivalent to 2mV/°C sensitivity. This is a reasonable big enough to be implemented by existing signal measurement equipment.

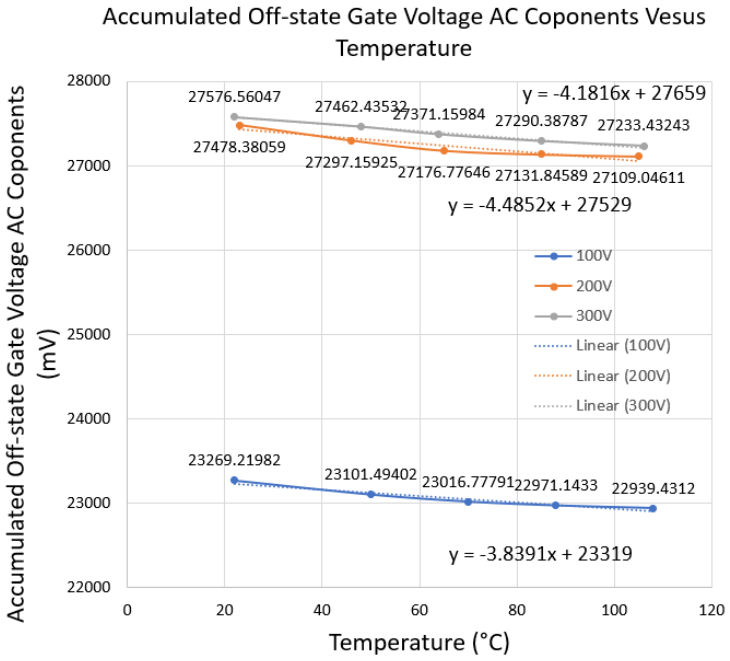


Figure 1.34 Comparison between different DC bias conditions under 50% duty cycle.

The second set of tests are established to investigate the influence of the value of the input DC voltage. The reason why this test is carried out is that the impedance contributed by the intrinsic gate-source capacitor in the off-state small signal equivalent circuit is DC voltage dependent. The test is conducted under 50% duty cycle.

The results shown in Fig 5.34 confirm that the accumulated ac components of off-state gate voltage present a linear decrease trend while a y-axis shift appears when the DC bias voltage changes. It can be concluded that the gate -source voltage difference between 100V and 200V is significantly bigger than the gate-source voltage difference between 200V and 300V. This is because with the increment of the DC bias voltage the gate-source capacitance will continuously increase while the increasing rate will reduce with the DC bias voltage become bigger as indicated in C2M0080120D data sheet.

The operation of the T_j estimation principle can be described with the flowchart shown in Figure 5.35. The controller will identify the necessity to start the T_j estimating process. If it is necessary to detect instantaneous T_j of SiC MOSFET, the procedure is presented in the flowchart. Information on the device that was measured is stored and further data processing will take place. The measurement results will be compared with the look-up table established during the calibration to estimate value of T_j.

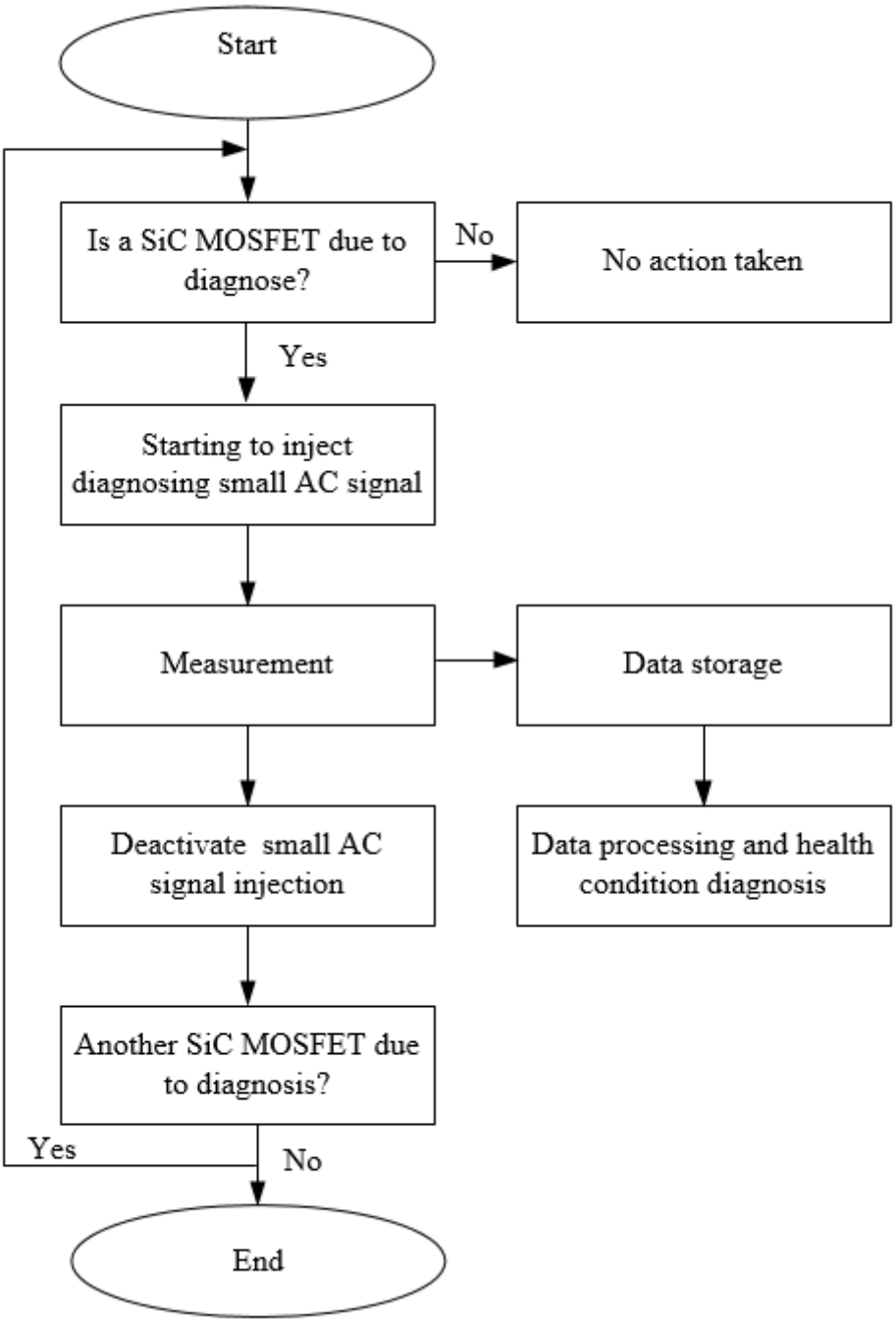


Figure 5. 35 Principles of small AC signal injection analysis for SiC MOSFET T_j extraction.

The timing of when the SiC MOSFET is to be diagnosed need to be predefined, for example, one diagnostic operation will be carried out every 1000 hours. Another point worthy to be noticed is that currently the data need to be stored and processed afterwards which means that it cannot be identified as fully in-situ measurement while the proposed method does not require to remove the device to do the diagnose or interrupting the normal operation of the SiC MOSFET.

5.2 Conclusion

In this chapter, the experimental set-up utilizing small AC signal injection is presented. Unbiased, biased experimental tests and finally test based on Cree/Wolfspeed discrete SiC MOSFET evaluation board are carried out. The values of T_j of the SiC MOSFET can be extracted by determining the relationship between peak gate-source voltages under small AC signal injection conditions. The biased DC tests are carried out under two different situations, where initially the small AC signal is directly injected into the gate terminal of the SiC MOSFET. For real applications, tests utilizing a gate driver to provide a minus gate voltage in combination with a superimposed small AC signal are also conducted. The results of both tests verify the proposed small AC signal injection technique. As presented in the previous section, the value of T_j of the SiC MOSFET can be derived since $V_{GSPeaktotal}$ is linearly dependent on T_j, and once data for $V_{GSPeaktotal}$ have been captured at different values of T_j then a look-up table can be established. Calibration should be performed under different DC biasing conditions and also based on different injection signal amplitudes in order to match real application conditions. Finally, the look-up table can be used to determine the value of T_j during the normal operation of the SiC MOSFET.

Chapter 6 Conclusion and future work

Global warming has been a serious issue for the past several decades. To restrict the continuously increasing emissions of CO_2, many efforts have been made, including the development of EVs and MEA, to reduce the consumption of fossil fuels. This in turn increases the need for robust power electronic systems to avoid catastrophic failure.

Si power electronic devices or modules have dominated the power electronic scene and the physical limitations of Si material have already been reached. In these circumstances, in order to achieve higher temperature capability, faster switching speed, higher break-down voltage and lower switching and conduction losses, WBG materials are being developed as potentially the future of power electronics to replace traditional Si semiconductors. However, the reliability of WBG semiconductor is still an important issue which needs to be addressed. In this thesis, a SiC discrete MOSFET is used as the device that being studied.

Traditional T_j estimation methods are reviewed including direct temperature measurement methods, indirect temperature measurement methods and thermal model-based methods. Each type is presented in detail and its advantages and disadvantages are also listed. Among those methods, the TSEP-based indirect temperature measurement method is preferred because there is no requirement to modify the power device or module, it is non-intrusive, and with a proper set-up it will not interfere with the normal operation of the power electronic system. So state-of-art TSEPs are analysed in detail and the results show that these methods are not entirely suitable for SiC discrete MOSFET, due to the unique physical behaviour of SiC material.

Thus, in this thesis a new method based on small AC signal analysis is proposed to extract the T_j of the SiC discrete MOSFET. The proposed method is non-intrusive and will not interfere with the normal operation of the MOSFET. A high frequency, small amplitude AC chirp signal is superimposed onto the negative biasing gate voltage by using a high frequency pulse transformer during the off state of the SiC discrete MOSFET. The frequency response of the gate-source voltage is extracted and analysed to find the change in internal gate resistance (R_{int}) induced by the variation in T_j. By establishing a look-up table of the relationship between R_{int} and T_j, it is possible to estimate the value of T_j of the SiC discrete MOSFET online.

To achieve the proposed method, an equivalent small AC signal circuit is established and the values for all individual parasitic components are calculated. The equivalent circuit model is simulated in LTspice and an experimental test is achieved by using an impedance analyser. The

results of both simulations and experiments are compared and prove that the model is precise enough for use. After the validation of the model, further simulations and experimental tests are carried out under unbiased and biased conditions. The results are in good agreement with the simulation results.

In this work, the experiments are only performed on a single SiC discrete MOSFET in a simple DC bias topology and in a boost converter topology. Thus, more research should be conducted in the future and should mainly focus on the following aspects.

In the test, due to the large amount data collected from the experiment, it is hard to process the data immediately. The data must be stored and processed afterwards, which means that values of instantons T_j cannot be derived instantaneously. Further efforts should be made to establish improvements in signal processing to calculate the value of T_j simultaneously with the data acquisition.

The proposed technique might not be applicable to other SiC devices like SiC IGBT, since the physical topology of SiC MOSFET and SiC IGBT are not completely the same, so the relationship between the T_j and measured gate-source voltage under superimposed small AC signal would be different. Thus, if there is need to apply this method to SiC IGBT, delicated calibration should be carried out to examine the feasibility.

Although the proposed technique is designed to detect the value of T_j for SiC discrete MOSFETs, it should be able to be applied to SiC MOSFET modules as well. Simulation work has been carried out to examine proposed method. The implementation of this method would be more complex since small AC signal injection need to be established for each MOSFET in the power module via their gate driver respectively. In addition, the parallel structures of SiC MOSFET modules may lead to challenges if the superimposed signal enters the impedance loop of other chips in parallel, making it difficult to extract the T_j of the targeted chip accurately.

Similar to the above issue, if the values of parasitic components in the topology are of similar magnitudes as the parasitic components in the gate-source loop of the SiC MOSFET, the injected signal might pick up the change in the parasitic components of the topology due to degradation. This will result in inaccurate T_j estimation, and for this reason further research should be conducted to decouple the effects of the parasitic components of the topology from the parasitic components of the SiC MOSFET.

Appendix A: State-of-art of TSEPs

A.1 Introduction

The main difficulty in accomplishing temperature measurement is to extract the relevant thermal information while devices are in operation. Gel in the module and the packaging of devices do not allow direct measurement methods like the use of an infrared camera or embedded thermal sensors. TSEPs are seen as an alternative as they measure voltages and currents at the terminals of the device. Changes in voltage and current can be translated into temperature by knowing the relationship between the physical properties and their temperature dependencies. TSEPs are widely used to extract the thermal information from chips [4]. In the following sections, state-of-art TSEPs are described and summarized.

A.2 Steady-state TSEPs

TESPs can be categorized as steady-state TSEPs and dynamic TSEPs. Steady-state TSEPs refer to the fact that parameters are extracted during either the on-state or the off-state of the power device, and dynamic TSEPs are captured during the switching transient periods of the power device [93]. In the next section, the steady-state TSEPs which have been proposed by researchers in the past several decades are presented.

a. Saturation current (I_{sat})

The first steady-state TESP presented here is the saturation current (I_{sat}) which can be defined as the collector current [94, 95] when:

$$V_{CEsat} = V_{GE} - V_{TH} \tag{A1}$$

and I_{sat} can be expressed as in equation A2:

$$I_{sat} = ((1 + \beta_{PNP}) \frac{u_{ns}(T_{ch0}) C_{OX} Z_c}{2 L_c} \times (V_{GE} - V_{TH}(T_{ch0}))^2 \tag{A2}$$

where I_{sat} is the saturation current, β_{PNP} is the current gain of the bipolar transistor in the IGBT (for MOSFETs: β_{PNP} =0), μ_{ns} is the surface mobility of electrons in the channel, C_{ox} is the oxide capacitance, Z_C is the channel width, L_C is the channel length, V_{CEsat} is the collector-emitter saturation voltage, V_{GE} is the gate-emitter voltage and V_{TH} is the threshold voltage. The relationship between the I_{sat} and the T_j has been presented for different V_{GE} and V_{CE} conditions as shown in Figure A1 [96].

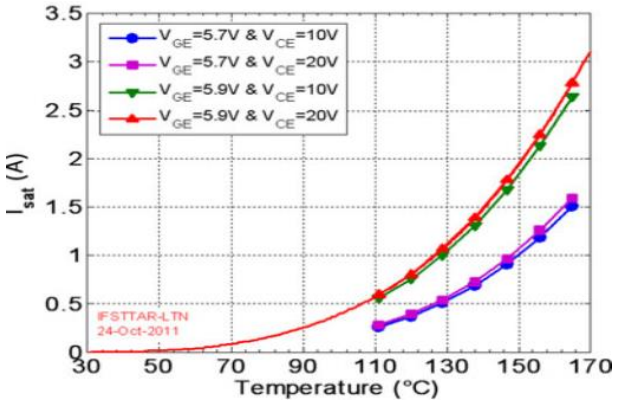


Figure A 1 I_{sat} value as a function of T_j at different voltage conditions [96].

It can be seen from Figure A1 that, with the increment of T_j, I_{sat} increases accordingly. Beside this, the collector-emitter voltage V_{CE} and the gate-emitter voltage V_{GE} influence I_{sat} too, as shown in the figure. I_{sat} increases slightly only when V_{CE} doubles (10 V to 20 V), which indicates that V_{GE} is the dominant parameter that affects I_{sat} at fixed T_j. Another aspect worth noting is that the sensitivity of I_{sat} against T_j become bigger with higher V_{GE}.

b. Collector leakage current (I_{leak})

Another current type of TSEP is the collector leakage current (I_{leak}). I_{leak} is defined as the passing collector current when gate-emitter is shorted and rated voltage is applied to collector-emitter [97]. I_{leak} can be represented as shown in equation A3:

$$I_{leak} = qA\frac{{n_i}^2}{N_o}\sqrt{\frac{D_n}{\tau_n}} + \frac{qAn_i x_d}{\tau_n} \tag{A3}$$

where A is the junction area, n_i is the intrinsic carrier doping concentration, τ_n is the lifetime of the space charge region, D_n is the diffusion coefficient of an electron and lastly x_d is the diffuse length at high temperature. Some practical results have been published [97] as illustrated in Figure A2 where a 1200 V, 50 A IGBT was used.

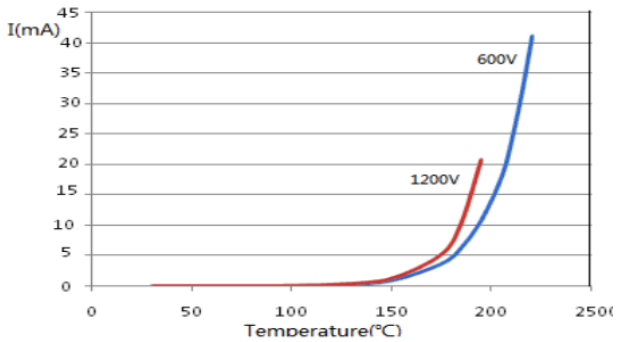


Figure A 2 Comparison of collector leakage current under different V_{CE} [97].

As shown in Figure A2, at low T_j (roughly below 150 ℃) there is only a small change in $I_{leak.}$ When T_j goes beyond 150 ℃ a significant increment of I_{leak} is observed.

c. On-state voltage drop ($V_{CE(on)}$)

$V_{CE(on)}$ is a measures of the voltage drop between the collector-emitter terminals during the IGBT's on-state. A defined measurement current (I_m) is flowing through the collector-emitter. The voltage builds up due to inner resistance and intrinsic voltage across the built-in PN junction [97]. The equation relating $V_{CE(on)}$ to I_m is approximated as [97]:

$$V_{CE(on)} = V_{CE0} + \Delta V_{CE0}(T_j - T_{j0}) + I_m[r_0 + \Delta r_0(T_j - T_{j0})] - \alpha_{ge} \cdot \Delta V_{GE} \qquad \text{(A4)}$$

where $V_{CE(on)}$, T_j, I_m and V_{GE} represent the on-state voltage drop, junction temperature, measurement current and gate-emitter voltage respectively, V_{CE0} and r_0 are the on-state voltage drop and ohmic resistance at the reference junction temperature T_{j0}, ΔV_{CE0} and Δr_0 are the temperature coefficients for V_{CE0} and r_0 correspondingly, and ΔV_{ge} is gate-emitter voltage difference. From equation A4, $V_{CE(on)}$ can be described as a function of T_j, I_m and V_{ge}. If it is possible to keep I_m and V_{ge} constant, then the above equation can be simplified and $V_{CE(on)}$ is only influenced by T_j, as shown in equation A5:

$$V_{CE(on)} = V'_{CE0} + \Delta V_{CE0}(T_j - T_{j0}) \qquad \text{(A5)}$$

Where V'_{CE0} is the on-state voltage drop at the reference T_j, I_m and V_{ge}.

In this way, T_j can be effectively estimated by obtaining the value of $V_{CE(on)}$.

As shown in Figure A3, five different I_m current values are injected into the collector-emitter and the corresponding $V_{CE(on)}$ is plotted [93].

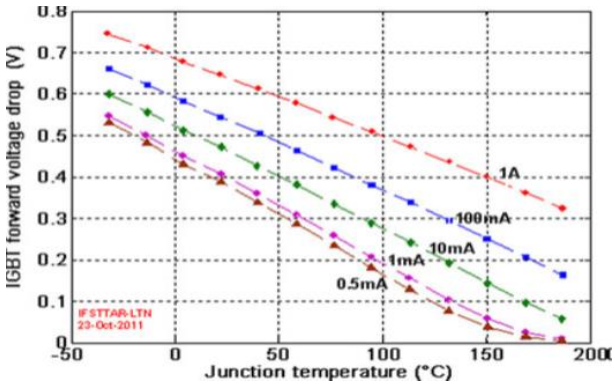


Figure A 3 $V_{CE(on)}$ of an IGBT as a function of T_j for different *Im* [93].

It is clear from Figure A3 that, with increasing T_j, $V_{CE(on)}$ changes linearly.

A.3 Dynamic TSEPs

Dynamic TSEPs are captured during the switching transient period of power electronics devices [98].

a. Transconductance (g_m)

Transconductance (g_m) is the gain of the transistor and refers to the magnitude of output current (collector current I_C) obtained for a given input voltage (gate voltage V_{GE}) [99]. It can be expressed as in equation A6:

$$g_m = \frac{dI_C/dt}{dV_{GE}/dt} = \frac{1}{1-\beta_{pnp}(T)}\left[\mu(T)C_{OX} \times \frac{W}{L}(V_{GE} - V_{threshold}(T))\right] \quad \text{(A6)}$$

Where $\beta_{pnp}(T)$ is the current gain of the p-n-p transistor structure within an IGBT, which is temperature-dependent, $\mu(T)$ is the electron channel mobility (in centimetres squared per volt per second ($cm^2/V \cdot s$)) and the dependence on temperature is presented in equation A7:

$$\mu(T) = 1350 \times \left(T/300\right) - 2.42 \; (when\; T \geq 200K) \quad \text{(A7)}$$

C_{OX} is the oxide capacitance (in Farads per centimetre square (F/cm^2)), and W and L are the channel width and length respectively (in centimetre (cm)).

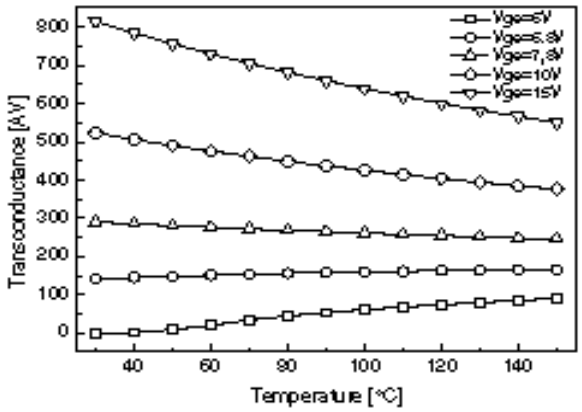


Figure A 4 Transconductance of a 3 kV 1200 A IGBT Module [100].

In Figure A4, it can be observed that, for a gate voltage below 7.8 V, transconductance increases with temperature, whereas for higher V_{GE} values, g_m decreases with temperature and exhibits larger signal dynamics, especially in the highest V_{GE} range.

b. Threshold voltage (V_{TH})

V_{TH} is the gate voltage at the instance when the IGBT turns on and collector current (I_C) begins to flow [99]. V_{TH} can be described as in equation A8 below:

$$V_{th} = V_{FB} + 2\emptyset_{FB} + \frac{Q_{Bmax}}{C_{OX}} = V_{FB} + 2\emptyset_{FB} + \frac{\sqrt{2\varepsilon_0\varepsilon_s q N_{Amax}(2\emptyset_{FB})}}{C_{OX}} \quad \text{(A8)}$$

where V_{FB} is the flat-band voltage, $2\Phi_{FB}$ is surface potential, N_{Amax} is surface concentration, amd C_{ox} is gate oxide capacitance [101]. In the above equation, Φ_{FB} is the most temperature-dependent parameter and is given by:

$$\emptyset_{FB} = \frac{kT}{q}\ln\frac{N_{Amax}}{n_i} \quad \text{(A9)}$$

Where T is the channel or junction temperature.

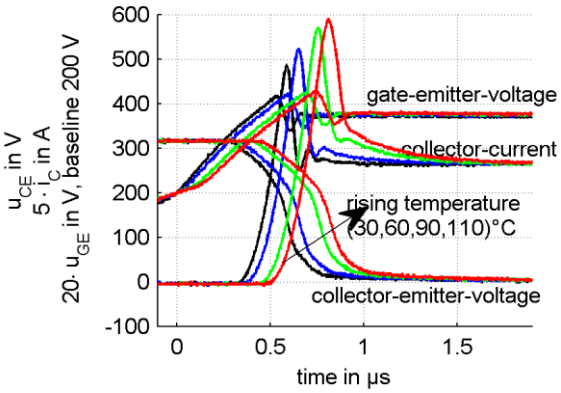


Figure A 5 Turn-on transient behaviour of V_{GE} at different T_j [102]

In Figure A5, it can be clearly seen that, during the turn-on process of an IGBT, the instance where I_C begins to flow is delayed with increasing T_j, and the point where I_C starts to be bigger than 0 A shifts towards the right on the graph. The corresponding V_{GE} can be detected and plotted to find V_{TH} accordingly.

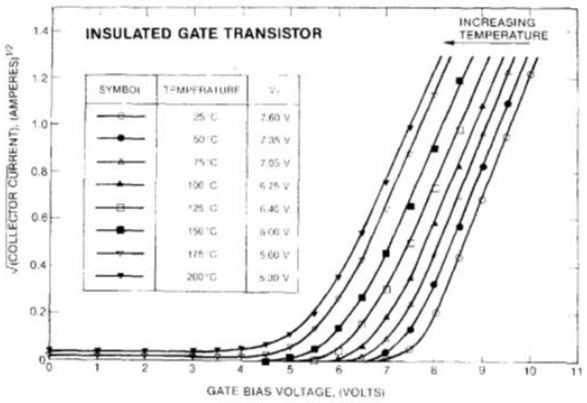


Figure A 6 Change in IGBT V_{TH} with increasing T_j [100].

It is shown in Figure A6 that, for the IGBT used in the test, V_{TH} decrease homogeneously with the increment of T_j. For the case in Figure A7, V_{TH} was extracted under various I_C and V_{CE} conditions as illustrated. Overall, the V_{TH} value declines along with the rise in T_j. For higher values of I_C, V_{TH} is slightly higher but for different V_{CE} levels there is merely a change in V_{TH} at fixed T_j.

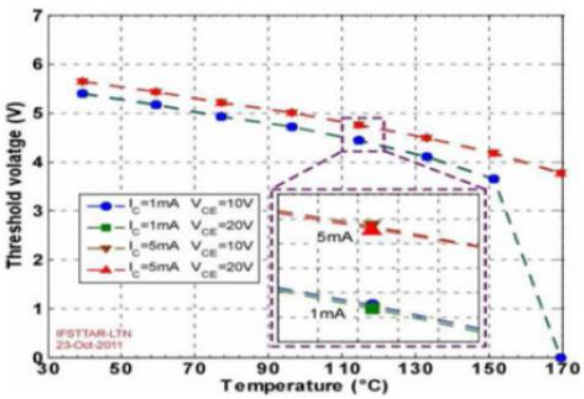


Figure A 7 V_{TH} as a function of T_j for different I_C and V_{CE} value [98]

c. Gate voltage miller plateau width during turn-off

The Miller plateau exists due to the effective capacitance between the gate and collector in the case of the IGBT (C_{GC}), and for a MOSFET it is the capacitance between the gate and drain (C_{GD}). The time duration of the Miller plateau (t_{Miller}) can be expressed as in equation A10:

$$t_{Miller} = \frac{R_G \cdot C_{GC} \cdot (V_{dc} - V_{on})}{(\frac{I_L}{g_m} + V_{th})} \tag{A10}$$

where t_{Miller} is the duration of the Miller plateau, R_G is the total gate resistance which is composed of internal and external resistance, C_{GC} is the gate-collector capacitance (Miller capacitance), V_{dc} is the DC-link voltage, V_{on} is the on-state voltage, I_L is the load current, g_m is the transconductance, and V_{TH} is the threshold voltage. From the equation above, it can be seen that t_{Miller} is proportional to C_{GC}. The effect of variation in T_j upon V_{on} can be neglected because the change of V_{on} is much smaller in comparison with V_{DC}. R_G is also T_j-dependent and increases with T_j due to the decline in electron mobility, which in turn increases the internal gate resistance. Those effects together result in the fact that t_{Miller} increases with rising T_j.

A typical V_{GE} waveform found [103] during the IGBT turn-off is plotted as shown in Figure A8. As illustrated in Figure A8, it can be observed that, for a fixed 25˚C T_j step increase, the end points of the Miller plateau are shifted to the right-hand side while the starting points of the plateau almost remain the same, which indicates that the time period becomes bigger with the rise in T_j.

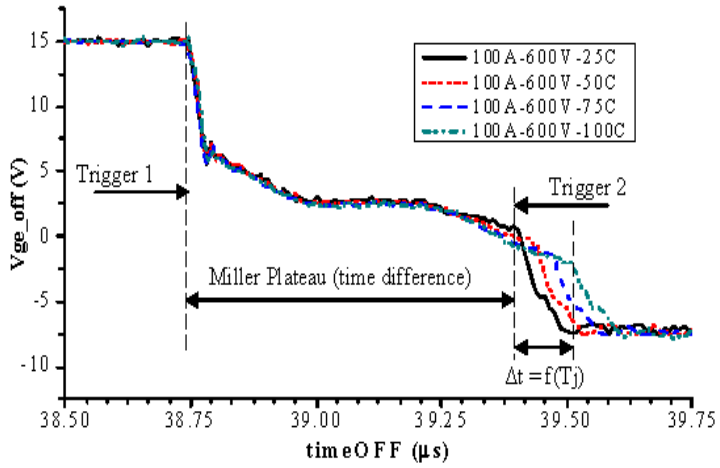


Figure A 8 V_{GE} waveforms at different temperatures for an IGBT measured at a 600 V, 100 A switching condition [103].

The value of t_{Miller} at various T_j levels [103], are also plotted as shown in Figure A9, which indicates that t_{Miller} increase linearly with rising T_j.

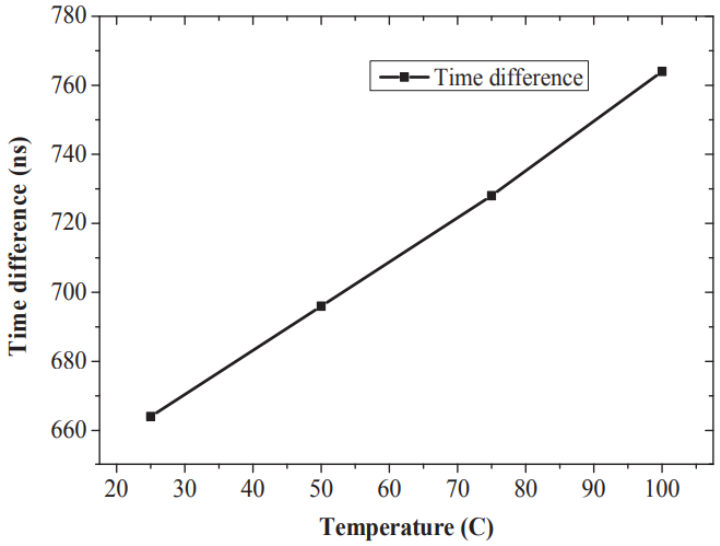


Figure A 9 Time difference between the first falling edge and second falling edge of the V_{ge} waveform at the 600 V, 100 A switching condition [103].

d. Turn-on delay time ($t_{d(on)}$)

The $t_{d(on)}$ can be defined as the specific period between the triggering instance of the gate driver or the instance when V_{GE} reaches a certain level, for example 10% of its final value, and the instance when I_C has reached a given level such as 10% of its final value when the device is fully on [104]. Mathematically, $t_{d(on)}$ can be presented as shown in equation A11:

$$t_{d(on)} = R_G(C_{GE} + C_{GC}) \ln(\frac{1}{1-\frac{V_{TH}}{V_{GE}}}) \quad \text{(A11)}$$

where R_G is the gate resistance, C_{GE} and C_{GC} are parasitic capacitances and V_{TH} is the threshold voltage.

As illustrated in Figure A10, the dashed lines indicate the duration of $t_{d(on)}$.

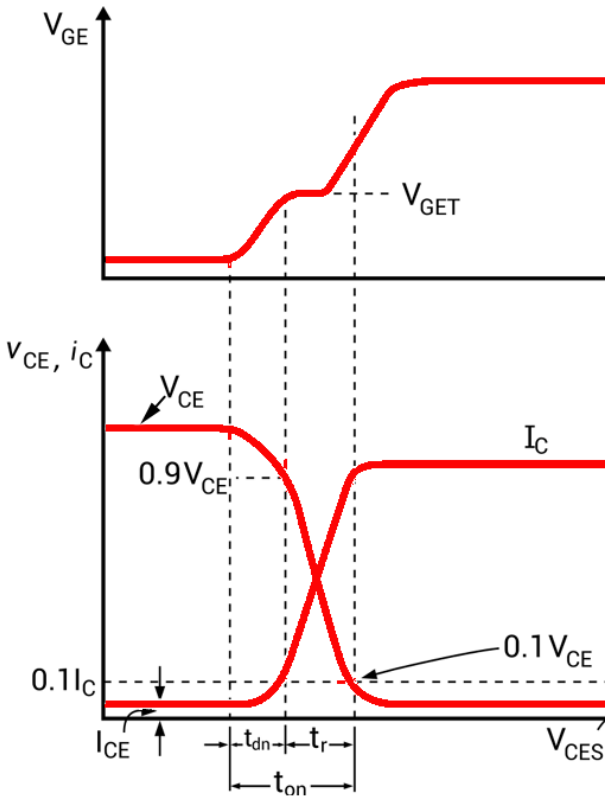


Figure A 10 Typical turn-on process of IGBT [67].

Test results [102] show the influence of the load current and applied DC voltage on $t_{d(on)}$ while T_j is changing.

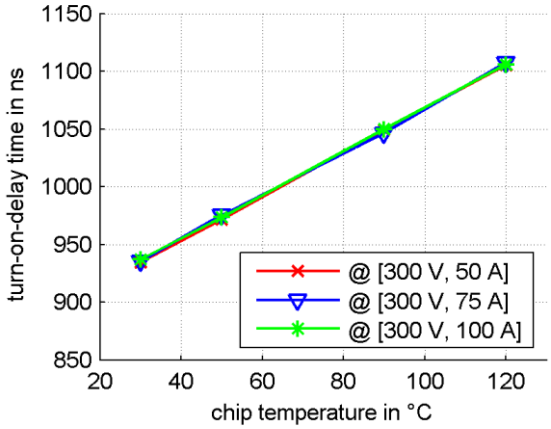


Figure A 11 $t_{d(on)}$ as a function of T_j and I_D [102].

As shown in Figure A11, I_D has barely any influence on the duration of $t_{d(on)}$. However, $t_{d(on)}$ shows a strong dependence on V_{DC} as illustrated in Figure A12. With increased V_{DC}, $t_{d(on)}$ is declining, and this can be explained by equation A11. In equation A11 the parasitic capacitances C_{GE} and C_{GC} are V_{DC}-dependent, and with the increment of V_{DC} the values of C_{GE} and C_{GC} are drastically reduced [88, 105]. Because $t_{d(on)}$ is proportional to the sum of C_{GE} and C_{GC}, $t_{d(on)}$ will become smaller while V_{DC} becomes bigger.

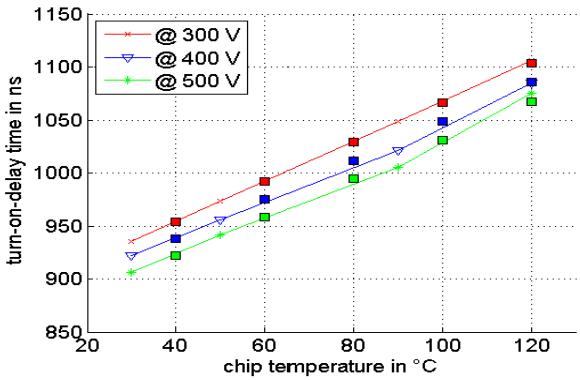


Figure A 12 $t_{d(on)}$ as a function of T_j and V_{DC} [102].

e. Turn-off delay time ($t_{d(off)}$)

This TSEP detects the period between the falling edge of the gate-emitter voltage (for example 90% of its initial value at the turn-off instance) and the moment when the collector current reaches a certain level (90 % of the initial value) [106]. Alternatively, since the gate turn-off time is dominated by the tail in the collector current waveform, the gate turn-off time is also

defined as the time taken for the anode current to decay to 90 % of its original value after the termination of the gate pulse, as illustrated below in Figure A13 [100].

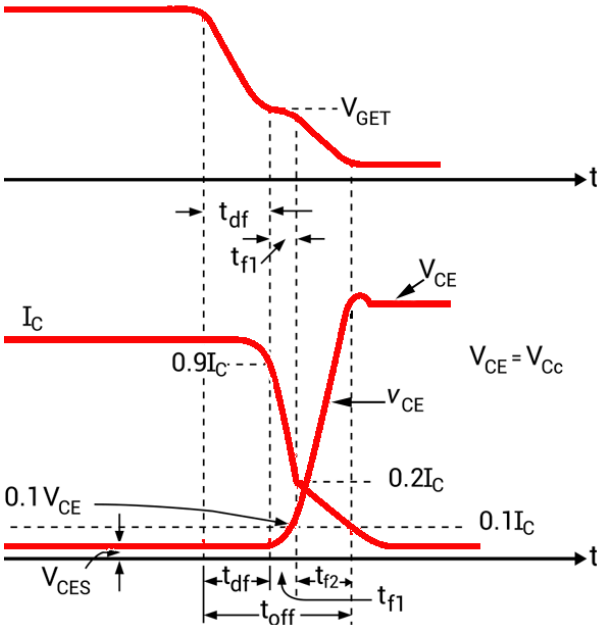


Figure A 13 Typical turn-off process of IGBT [67].

Previous results [67] presenting variations of $t_{d(off)}$ with T_j and I_L and results presenting variations of $t_{d(off)}$ with T_j and V_{DC} are illustrated in Figures A14 and A15, respectively.

It can be seen from Figure A14 that, for fixed I_L and V_{DC} test conditions, $t_{d(off)}$ is proportional to T_j, as shown. However, $t_{d(off)}$ is not only dependent on T_j but is also related to the load current as well, as the fixed T_j, $t_{d(off)}$ drops when I_L increases. In Figure A15, the results shown prove that, for fixed I_L, $t_{d(off)}$ will increase with V_{DC}.

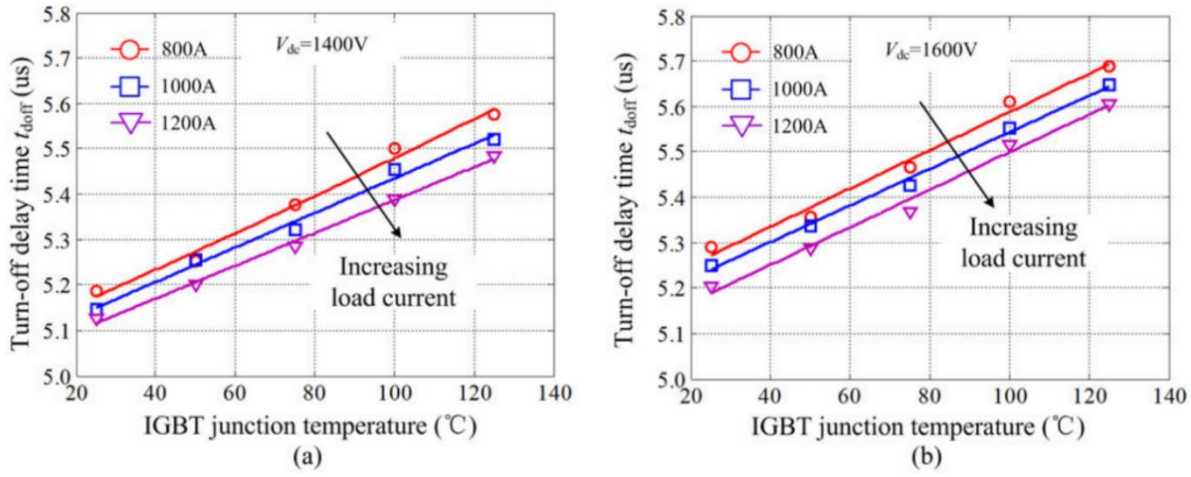


Figure A 14 Variation in $t_{d(off)}$ with T_j and I_L: (a)V_{DC}=1400 V and (b) V_{DC}=1600 V [67].

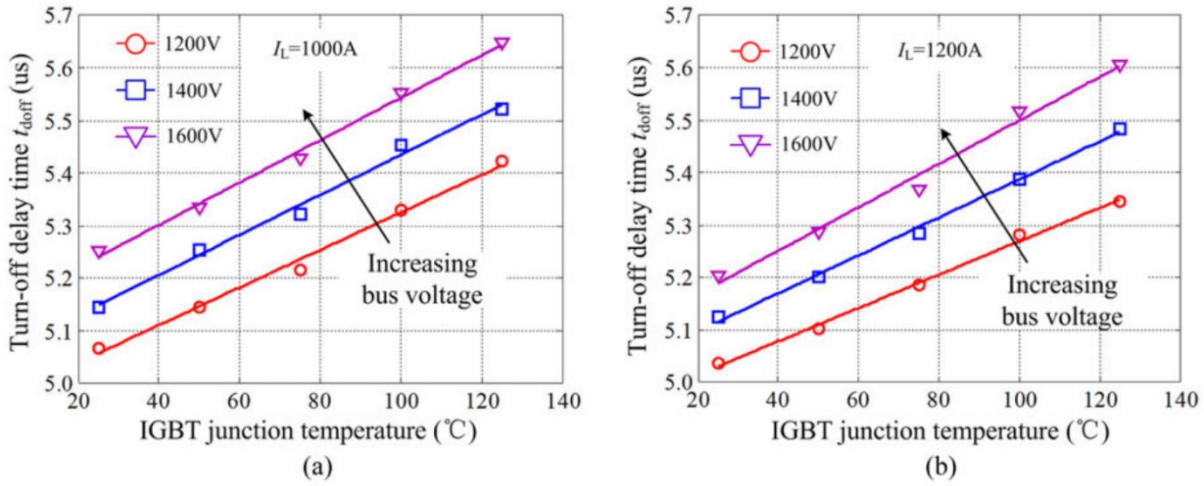


Figure A 15 Variation of $t_{d(off)}$ with T_j and V_{DC}: (a)I_L=1000 A and (b) I_L=1200 A [67].

f. dV_{CE}/d_t slope during turn-off

The changing rate of V_{CE} during the turn-off state has also been proposed as a dynamic TSEP [107]. The dV_{CE}/d_t slope can be expressed as in equation A12:

$$\frac{dV_{CE}}{d_t} = \frac{1}{\tau_G}\left(\frac{V_{GE(ON)} - V_{GG(OFF)}}{1+(C_O/g_m\tau_G)}\right) \quad \text{(A12)}$$

Where τ_G is the time constant equal to $R_G.C_{GC}$, $V_{GG(OFF)}$ is gate drive voltage during turn-off state, $V_{GE(ON)}$ is the gate-emitter voltage at the instant of Miller plateau during turn-off, C_O is the charge extraction capacitance.

In Figure A16, the relationship between dV_{CE}/d_t and T_j at two different V_{DC} conditions is illustrated [107]. It can be seen from both graphs that, at fixed V_{DC}, dV_{CE}/d_t shows a negative co-efficient against T_j.

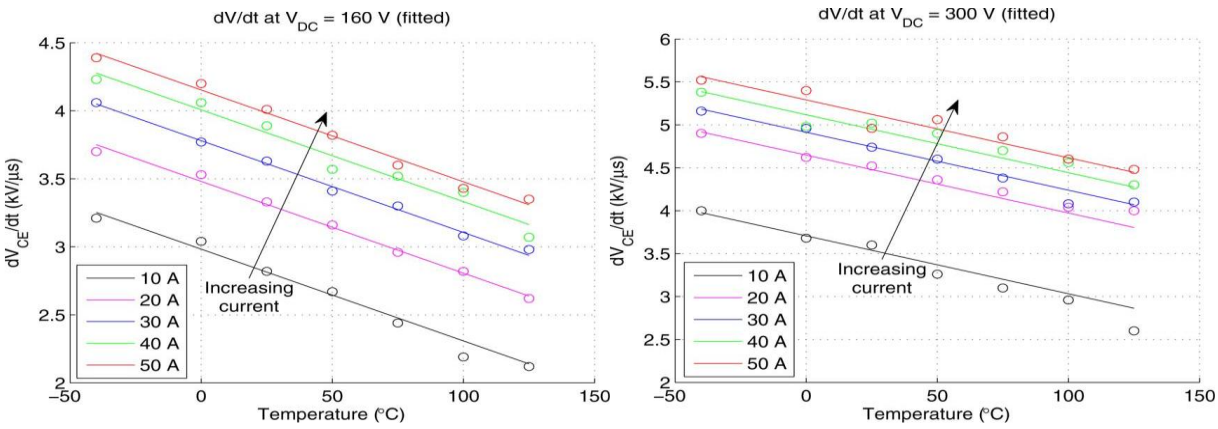


Figure A 16 Measured dV_{CE}/d_t values and linear fitted curves against T_j for varying I_L at: (a) V_{DC} of 160 V; (b) V_{DC} of 300 V [108].

g. dI_C/d_t slope during turn-on

As shown in Figure A5 and described in the previous section, at fixed V_{CE} the instantaneous change in I_C is proportional to the instantaneous change of V_{GE}, and the proportionality factor is represented as gm as shown in equation A13:

$$\frac{dI_C}{dV_{GE}} = \frac{dI_C}{d_t} \times \frac{d_t}{dV_{GE}} = g_m \tag{A13}$$

Substituting equation A6 in equation A13, dI_C/d_t can be obtained as:

$$\frac{dI_C}{d_t} = \frac{dV_{GE}}{d_t} \times \frac{1}{1-\beta_{pnp}(T)} \left[\mu(T) C_{OX} \times \frac{W}{L} \left(V_{GE} - V_{threshold}(T)\right)\right] \tag{A14}$$

where β_{PNP} is the gain in the inherent bipolar transistor, μ is the mobility, and W/L is the ratio between the width and the length of the MOS channel [106].

A graph presenting the relationship between dI_C/d_t and T_j at two different V_{GE} conditions from a previous study is illustrated [109] in Figure A17. The unique performance of dI_C/d_t is that, at lower V_{GE} (10 V) it is positively proportion to T_j but at higher V_{GE} (14.2 V) it here is negatively proportion to T_j.

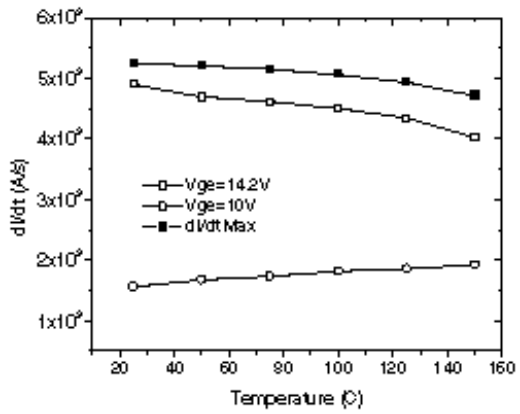


Figure A 17 The Measured dI_C/d_t at two different gate voltages [109].

h. Collector current tail (I_{tail}) during turn-off

I_{tail} is generally defined as that part of I_C waveform where I_C continues to flow after an initially abrupt fall. As shown in Figure A18, I_{tail} starts when the rate of change of the collector current is distinctly reduced. I_{tail} appears due to the recombination of minority carriers in the IGBT [110] Depending on the technology of the IGBT, the magnitude and duration of I_{tail} can have a strong dependence on temperature [111].

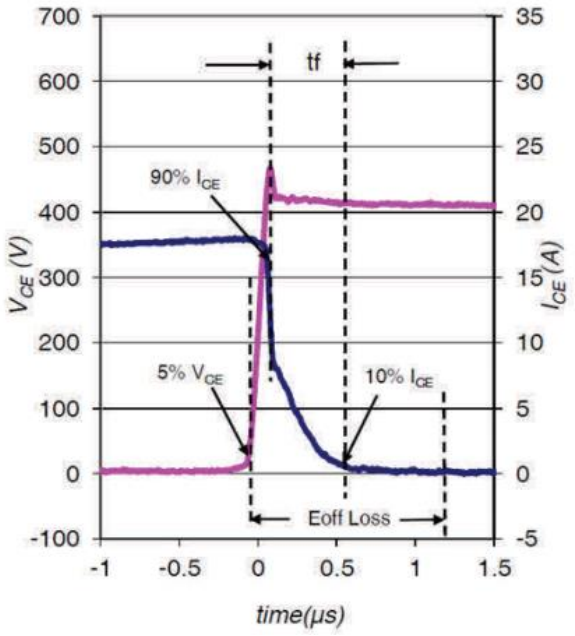


Figure A 18 Turn-off waveform of a commercial IGBT at 150 ℃, rated current (IRG7IC23FD) [110].

Figure A19 illustrates I_{tail} behaviour during the IGBT turn-off period under different T_j. It can be observed from the graph that rate of change of I_{tail} becomes smaller, which means that it takes more time for the I_{tail} to drop to a certain current level at higher T_j.

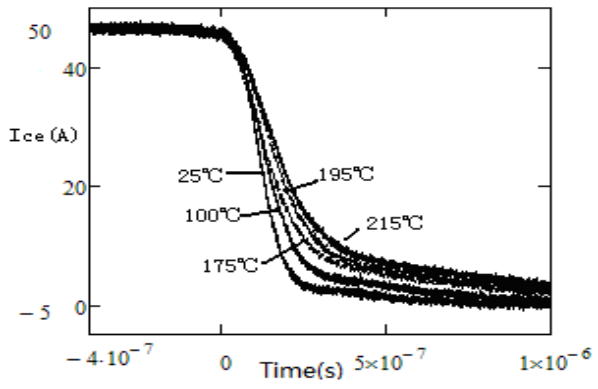


Figure A 19 Behavior of I_{tail} at different T_j [101].

A.4 Other TSEPs

Other than the steady-state and dynamic TSEPs, there are TSEPs that fall in between these two categories. In this section, three of those kinds of TSEP are briefly introduced.

a. Power loss dissipation (P_{dlss})

P_{dlss} is the total loss, which takes into account both switching losses and conduction losses. The relationship between P_{dlss} and T_j can be described as shown in equation A15:

$$T_j = T_C + P_{dlss} \cdot Z_{th(JC)} \tag{A15}$$

where T_C *and* T_j are the case and junction temperatures respectively and $Z_{th(JC)}$ is the equivalent thermal impedance between the junction and the case of the IGBT [112].

T_C is acquired by applying a thermal sensor at the bottom surface of the base-plate under the IGBT chip to improve the accuracy of T_j estimation [112].

One study [102], P_{dlss} was measured only at turn-on transients under different T_j conditions and the results are presented in Figure A20. It can be seen that, with the increase in T_j, P_{dlss} becomes bigger.

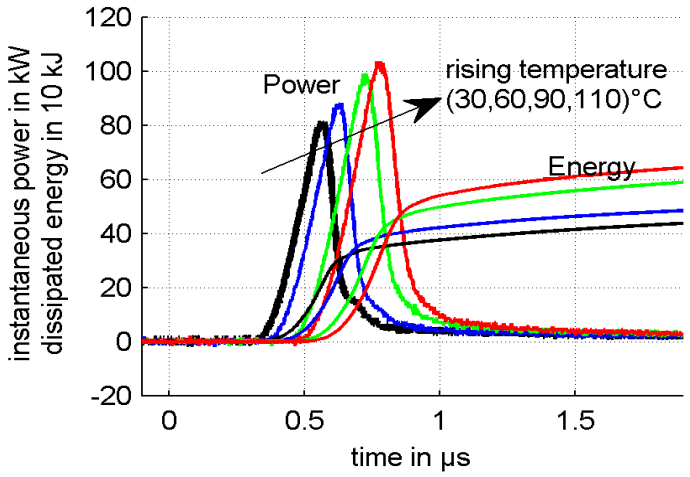


Figure A 20 Energy dissipation at turning-on as a function of T_j [106].

b. Internal gate resistance (R_{int})

R_{int} is not identical in its properties to the external gate resistance due to the fact that R_{int} is generally considered to be a distributed parameter rather than a lumped resistance, and it is the result of a combination of individual cells in the die substrate [50]. R_{int} is a function of mobility and is proportional to $1/\mu$, where μ is the channel mobility [106]. Since μ decreases with rising T_j, resistance increases. Hence internal resistance can be used as a TSEP.

c. Breakdown voltage (V_b)

The occurrence of a temperature dependent avalanche breakdown has been confirmed [9] when an increasing blocking voltage capability was found with increasing T_j. V_b is given by equation A16:

$$V_b = V_a(1-\alpha)^{1/n} \tag{A16}$$

Where V_a is the avalanche breakdown voltage, α is the base transport factor and n is a constant. α can be expressed as:

$$\alpha = \frac{1}{\cosh(W/\sqrt{D_p\tau_p})} \tag{A17}$$

Where W is the un-depleted base width and D_p and τ_p are the hole diffusion coefficient and carrier lifetime respectively. For an abrupt junction, the avalanche breakdown voltage V_a can be approximated to:

$$V_a = 5.34 \times 10^{13} \times (\frac{T_j}{300})^{0.35} \times N_b^{-0.75} \tag{A18}$$

It can be seen from equation A18 that V_a is a function of T_j and base-doping concentration (N_b). If equations A17 and A18 are substituted into equation 16, it can be shown that V_b is T_j-dependent.

A IGBT with a rated voltage of 600 V has been tested [111] to investigate the relationship between the value of the avalanche breakdown and T_j. The values of avalanche breakdown voltage at different values of T_j are listed in Table A1.

Table A 1 Avalanche breakdown voltage under different T_j conditions [111]

T_j (°C)	25	75	125	150
V_b (V)	805	840	875	890

From the test result in Table A1, the value of the avalanche breakdown voltage of the tested IGBT increases with temperature and shows a sensitivity of 0.7 V/°C.

A.1 Conclusion

T_j has a big impact on both the efficiency and reliability of a power module, and consequently knowledge of chip temperature is of paramount importance. In this section, state-of-the-art TSEPs are presented. TSEPs allow the indirect measurement of T_j non-intrusively and can therefore be applied in-situ. There are a large number of TSEPs, but no simple and generalized solution exists today for online junction temperature measurements. Dynamic TSEPs tend to suffer from EMI problems, and steady-state TSEPs require expensive sensors. It is therefore necessary to direct research efforts in this domain in order to continue the progression of condition monitoring and the temperature-based control of power converters.

Appendix B: State-of-art Gate Driver Topologies

B.1 Comparison of Si and SiC MOSFET gate drivers

In this appendix, three basic gate driver structures are introduced and then the gate driver for Si and SiC MOSFET devices are compared and discussed.

Gate drivers can be divided into three basic types: voltage source-based, current source-based and resonant-based [113]. Voltage source-based gate drivers include the push-pull output and bootstrap capacitor as well as other types of drivers and this type of gate driver can tune its output voltage [114]. The current source-based gate drivers include the current mirror-based and inductor-based current source gate drivers and this type can manipulate the output current [114]. The operation of both voltage source-based and current source based gate drivers are explain in detail in the following sections.

a. Push-pull voltage source gate driver

One of the advantages of the push-pull gate driver is that controlling the turn-on or turn-off states is a relatively simple process and fast hard switching can be achieved [115]. In the case of the SiC MOSFET, in order to fully turn on the device, the gate source voltage V_{GS} is usually set to be $+20$ V, and to properly turn off the device -2 to -10 V is required [21]. To form a push-pull voltage gate driver, one N-type MOSFET is employed to pull-up the voltage during the turn-on process and one P-type MOSFET is implemented to pull-down the voltage at turn-off. Figure B1 shows a dynamic equivalent circuit for a push-pull gate driver. The equivalent circuit includes a logic buffer in the input stage to limit the input PWM signal current rating, a push-pull output stage, and loop parasitic R_{g1}, R_{g2}, L_{g1}, L_{g2} as well as gate driver resistance are presented.

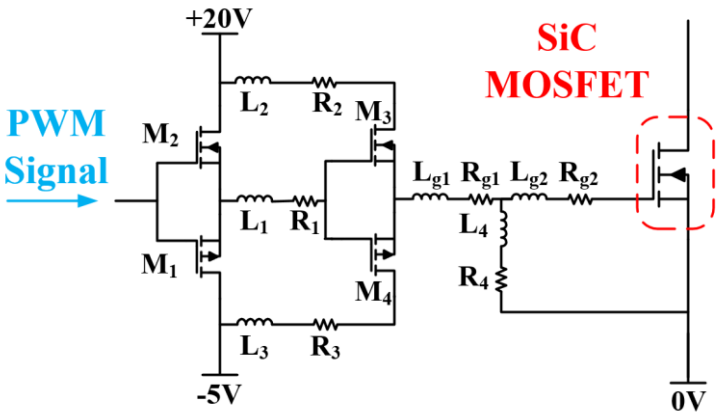


Figure B 1 Push-pull voltage source gate driver.

During the turn-on transient, as shown in Figure B2, the MOSFET M_1 in the logic buffer is turned on when the external turn-on signal is trigged. Once the M_1 is fully turned on, the gate driver pull-up switch M_3 consequently turns on, and as a result the SiC MOSFET gate terminal is then connected to the $+20$ V and the gate is charged by the current I_{GON} that passes through R_1. During the turn-off transient, as illustrated in Figure B3, the M_4 is turned on after the M_2 in the logic buffer is turned on when the external turn-off signal is activated, and the gate is then connected to -5 V and the gate discharges with a turn-off current I_{GOFF}.

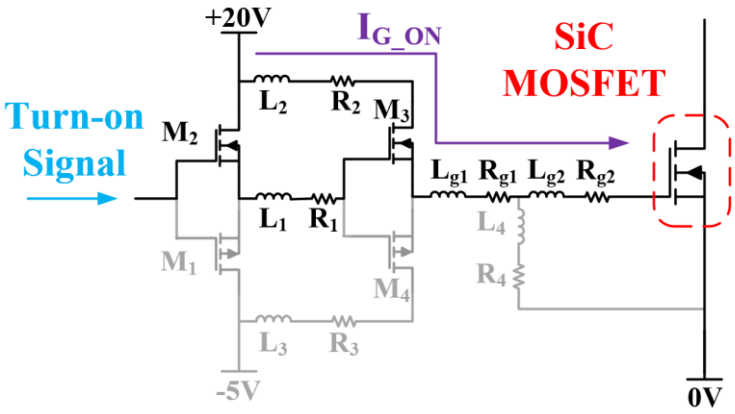


Figure B 2 Push-pull gate driver turn-on transient.

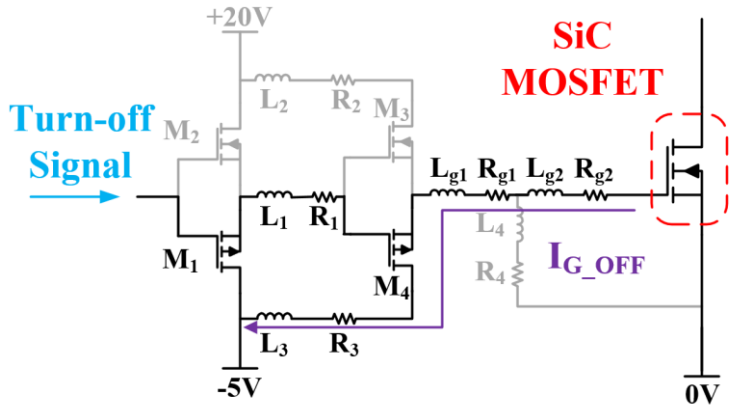


Figure B 3 Push-pull gate driver turn-off transient

b. Current mirror based current gated driver

WBG semiconductors have a smaller gate charge in comparison with traditional Si devices, and so a large drain current overshoot is induced due to the ultra-fast turn-on transient [116, 117]. This fast turn-off transient would cause a sizeable V_{DS} overshoot if the parasitic parameters were not carefully handled [118, 119]. The device's degradation might be accelerated due to the aforementioned overshoots and extra switching losses would potentially be produced as

well. A current mirror based current source gate driver is able to control the output current and achieve better switching behaviour. As shown in Figure B4, a current mirror set-up formed by multiple P-type bipolar junction transistors (BJTs) is applied to the current-source gate driver. In this configuration, the current mirror BJTs (B_1 and B_2), the current mirror activating MOSFET M_1, the pull-down MOSFET M_2, gate driver resistance and the parasitic of the circuit layout are depicted. By changing the values of reference resistance R_{ref}, the gate driver output current mirror can be tuned in a controlled manner. The current mirror is turned on by switch M_1 and then $+20$ V is connected to the SiC MOSFET gate terminal, as shown in Figure B5. To turn off the SiC MOSFET, the M_2 is turned on and the SiC MOSFET will then be connected to -5 V, as illustrated in Figure B6.

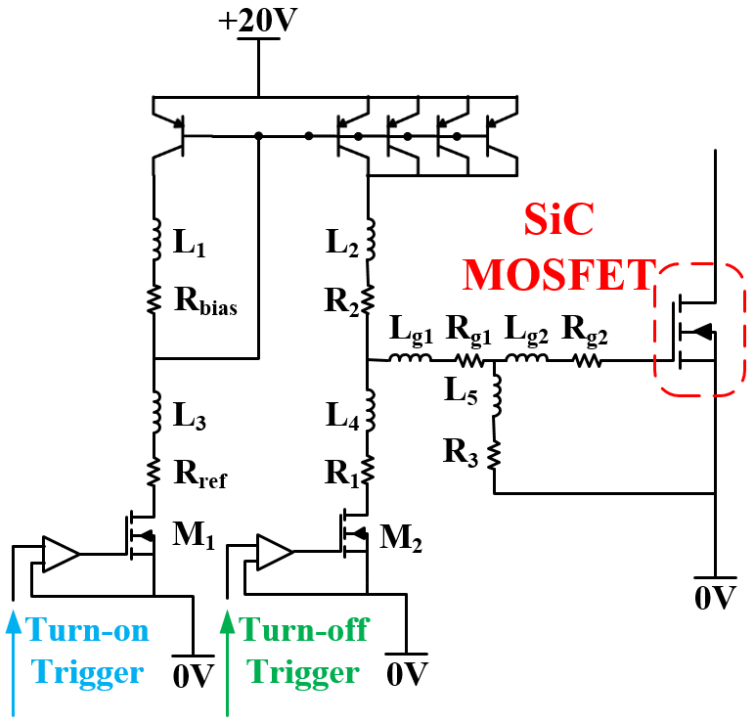


Figure B 4 Current mirror gate driver.

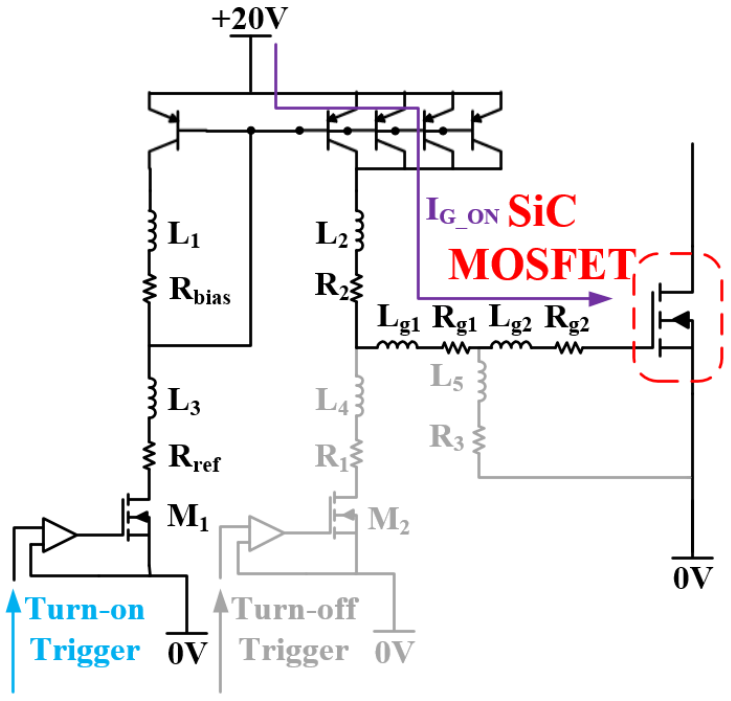


Figure B 5 Current mirror gate driver turn-on transient.

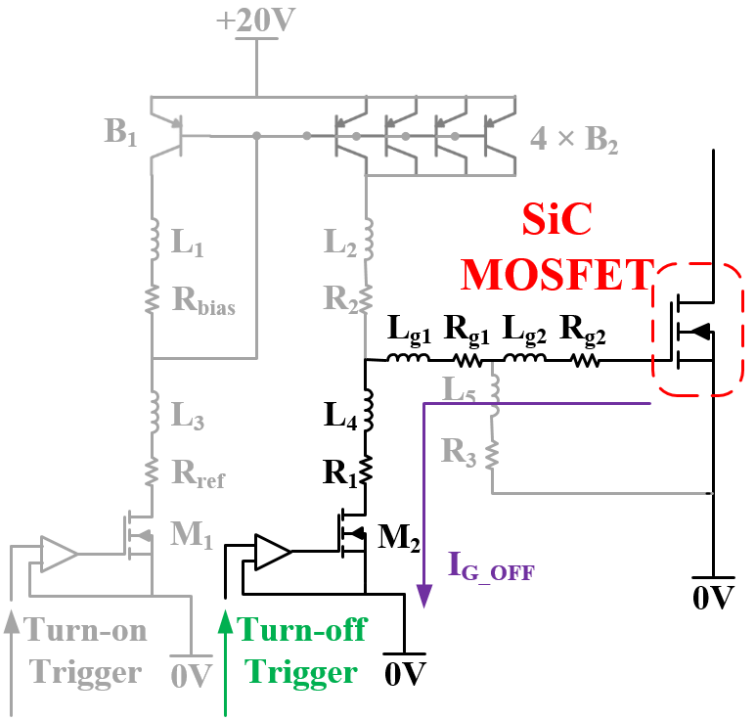


Figure B 6 Current mirror gate driver turn-off transient.

c. Current source gate driver with a regulated inductor stage

A current source gate driver implemented with an inductor has been proposed [113], and its topology is presented in Figure B7. An H-bridge configuration is formed by four switches (M_1, M_2, M_3 and M_4) and their antiparallel diodes (D_1, D_2, D_3 and D_4) and the load is an air-core inductor acting as the load of the H-bridge set-up. In this configuration, the SiC MOSFET can be turned on or off with a non-zero pre-charged current by deliberately controlling these four switches. The excess energy would be saved in the inductor during the turn-on and turn-off of the SiC MOSFET and this would then be returned to the 20 V power supply.

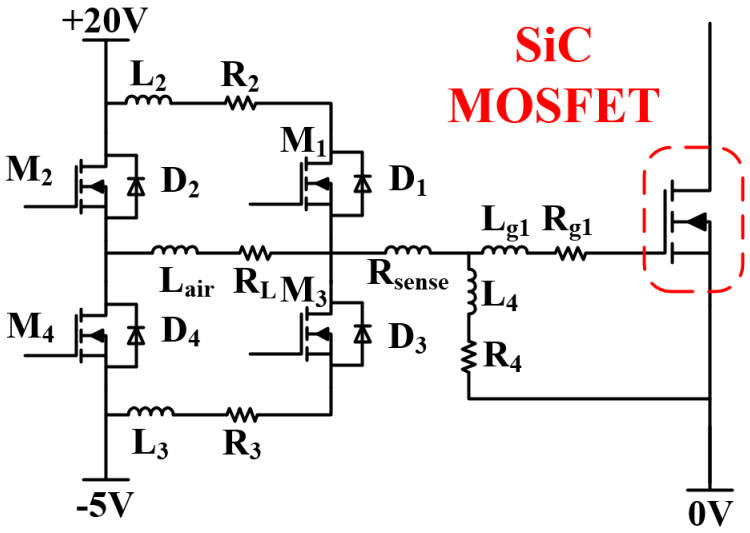


Figure B 7 Inductor-based current source gate driver.

The turn-on and turn-off processes are explained below in detail.

The turn-on process can be divided into 4 steps:

Step 1: Prior to the charging of the SiC MOSFET gate, switches M_2 and M_3 are turned on so as to charge L_{air} so as to establish the current potential as shown in Figure B8.

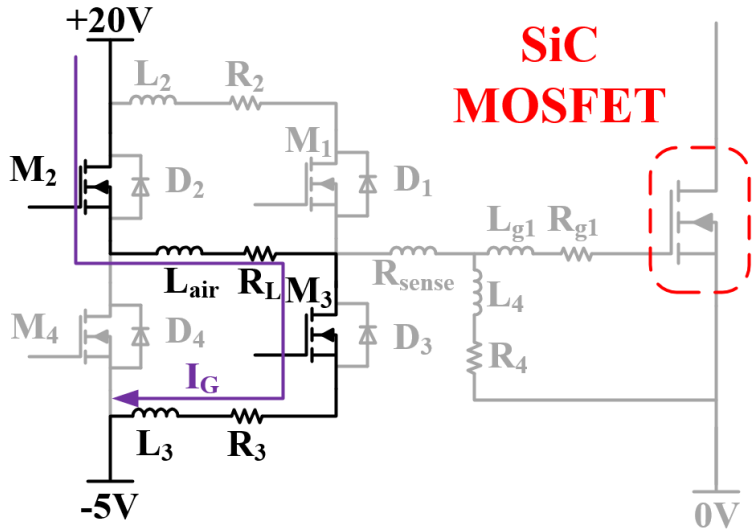


Figure B 8 Inductor-based gate driver turn-on transient: step 1.

Step 2: As illustrated in Figure B9, the level of current established in L_{air} can be accurately controlled by manipulating the switching-off of M_3. M_3 is turned off while L_{air} is charged to the desired current level. The current is then injected into the gate terminal of the SiC MOSFET from the inductor.

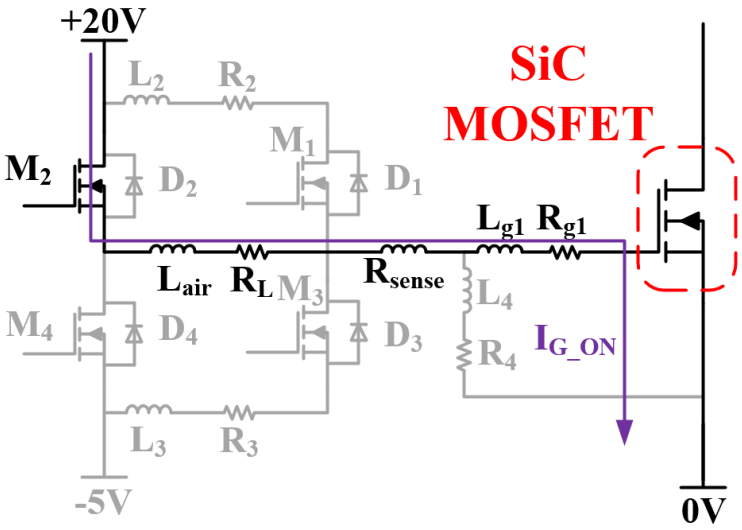


Figure B 9 Inductor-based gate driver turn-on transient: step 2.

Step 3: The remaining energy stored in inductor L_{air} is subsequently sent back to the +20V voltage supply via the anti-parallel diodes D_4 and D_1 when the gate voltage V_{GS} reaches +20V. During this process, M_1 is switched on following the gate signal and the current that fed back to the power supply is able to pass through the anti-parallel diode D_4 and switch M_1, as shown in Figure B10.

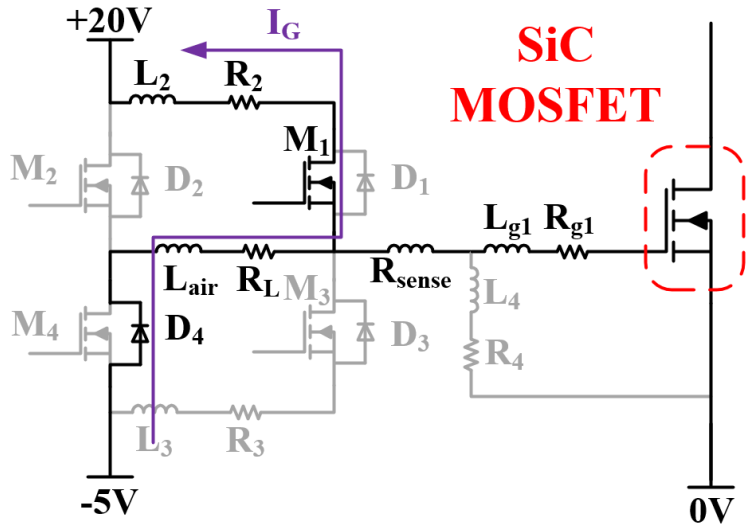


Figure B 10 Inductor-based gate driver turn-on transient: step 3.

Step 4: During the on-state of the SiC MOSFET, switch M_1 is also fully turned on in order to ensure that the gate terminal of the SiC MOSFET is always connected to the +20 V supply, as indicated in Figure B11.

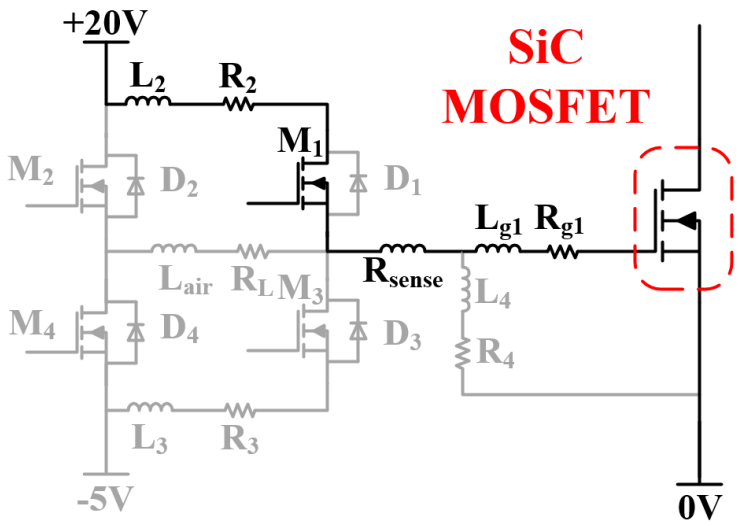


Figure B 11 Inductor-based gate driver turn-on transient: step 4.

The control strategy for switches M_1, M_2, M_3 and M_4 has been fully discussed elsewhere [120], and the turn-off transients can also be described in four steps as follows:

Step 5: L_{air} is pre-charged by turning switches M_1 and M_4 simultaneously on before the procedure of discharging the SiC MOSFET gate, as depicted in Figure B12.

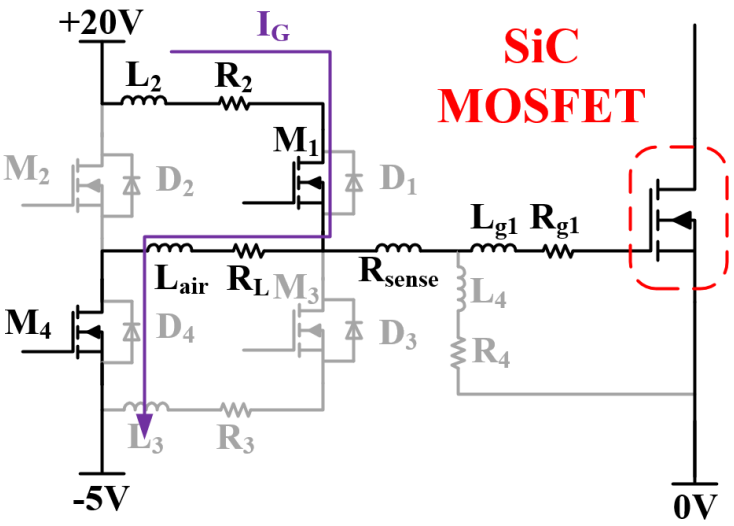


Figure B 12 Inductor-based gate driver turn-off transient: step 5.

Step 6: The current will be withdrawn from the gate terminal of the SiC MOSFET when the inductor L_{air} has been charged to the desired current by turning off the switch M_1, as illustrated in Figure B13.

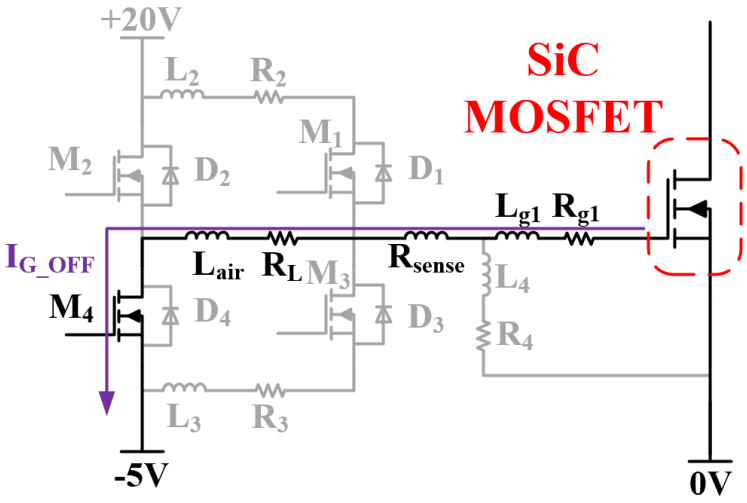


Figure B 13 Inductor-based gate driver turn-off transient: step 6.

Step 7: The remaining energy saved in the inductor will be fed back to the $+20$ V supply as the SiC MOSFET gate voltage approaches its off-state voltage (-5 V) by activating the switch M_3, as illustrated in Figure B14.

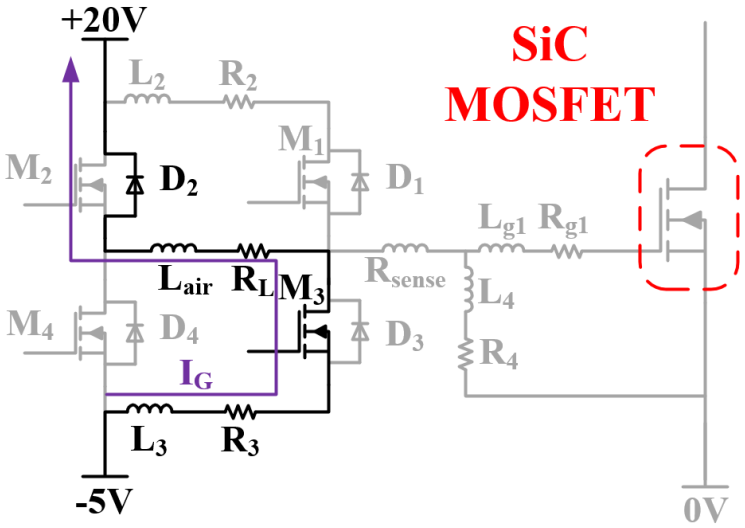


Figure B 14 Inductor-based gate driver turn-off transient: step 7.

Step 8: In order to make sure that the SiC MOSFET gate is always connected to −5 V during the off-state, switch M_3 should be kept turning on, as shown in Figure B15.

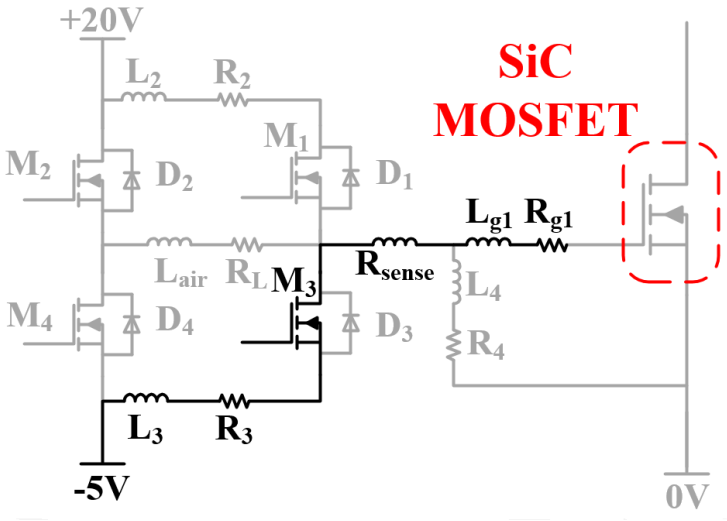


Figure B 15 Inductor-based gate driver turn-off transient: step 8.

B.2 Conclusion

When comparing the state-of-art of the gate driver concept for Si MOSFETs or IGBTs and SiC MOSFETs, it is shown in case of SiC MOSFET, there are more issues should be considered. For SiC MOSFET gate drivers, the first characteristic that is different from those in Si devices is the output capacitance typically has smaller transconductance (g_m) which results in a higher drain-source voltage between the on-state and off-state transition. Other than this, another feature worth noting is related to this low g_m which is that the gate voltage needed to fully turn on the SiC MOSFET is higher where +20 V is normally the gate voltage value recommended by the manufacturer. However, this high gate voltage does not lead to higher gate driver power usage due to the significantly smaller SiC MOSFET parasitic capacitances. Another further difference is that the required turn-off gate voltage is usually −2 to −5 V. Meanwhile there is a relatively low threshold voltage V_{TH} of typically about 5 V which decreases with increments in T_j. The combination of the above two features gives the SiC MOSFET better immunity against *dV/dt* noise. In this context, the design of low-impedance paths is critical because of the extremely short transition between the negative V_{GS} to V_{TH}. However, despite the differences indicated above, the totem-pole gate driver configuration has been extensively applied to Si MOSEFTs and Si IGBTs, and this still seems to be the most suitable type of gate driver. It is easy to select and implement different values of gate resistance R_G to tune the turn-on and turn-

off switching transient due to the asymmetry structure of the gate driver supply voltage V_{CC} ($+20$ V) and V_{EE} (-5 V

Appendix C: Unbiased Test

The schematic of PCB board used for the unbiased test has been shown in Figure C1.

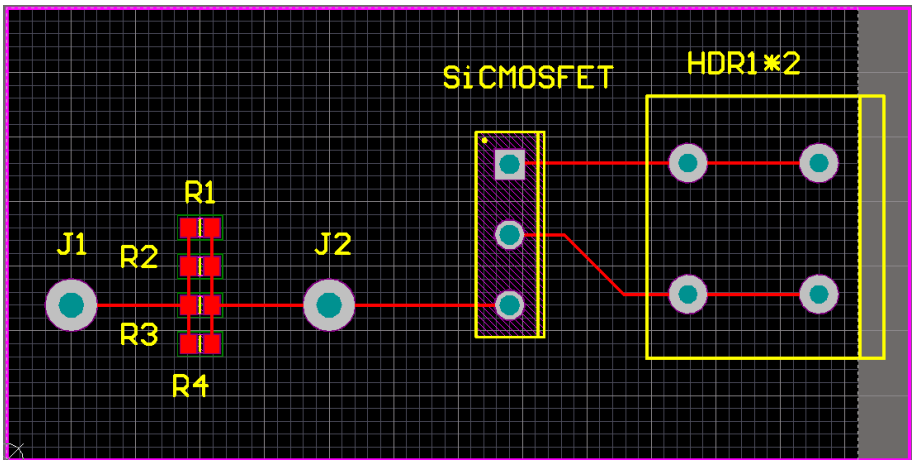


Figure C 1 Schematic of PCB board used for unbiased test.

The Matlab script which is used to calculate the impedance of the gate-source loop based on the data collected by the network analyser is presented as follows:

f=S11MAG3(:1)/1e6;

mag=S11MAG3(:2);

load S11PHASE3.CSV

phi=S11PHASE3(:2);

impedance=mag*exp(1j*s11phi*pi/180);

Z_0=50;

Zin=Z_0*(1+s11)/ (1-s11);

where *f* is the frequency, *mag* is the reflected magnitude data collected, *phi* is the reflected phase data collected, S11MAG3 and S11PHASE3 are the reflected magnitude and phase file, Z_0 is the network analyser output impedance value and *Zin* is the gate-source loop impedance value that is calculated.

Appendix D: Schematic of 4-leg Inverter

Schematic of 4-leg inverter is presented in Figure D.1.

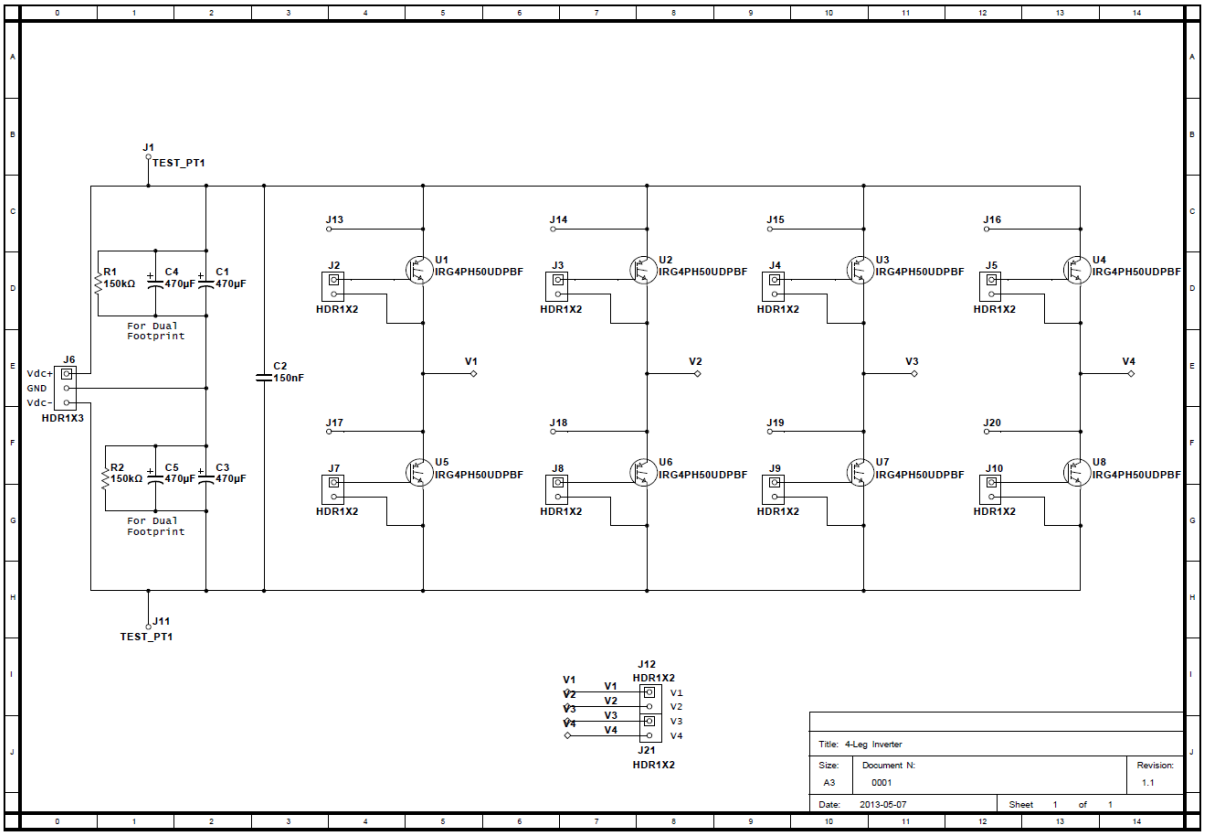
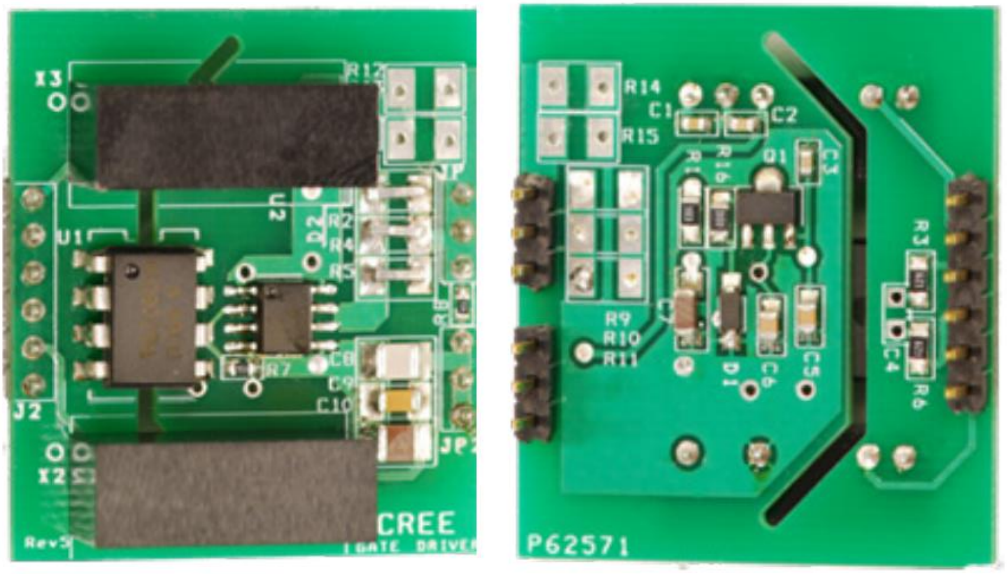


Figure D. 1 Schematic of 4-leg inverter.

Appendix E: SiC MOSFET Gate Driver Pictures

In this Appendix E, the SiC MOSFET isolated gate driver used in chapter 5 provided by Cree [121] is introduced and relevant graphs are presented as well.

The top and bottom views of the isolated gate driver are illustrated in Figure E1 (a) and (b).



(a) (b)

Figure E 1 Isolated gate driver: (a) top view; (b) bottom view [121].

The schematic for the isolated gate driver is shown in Figure E 2.

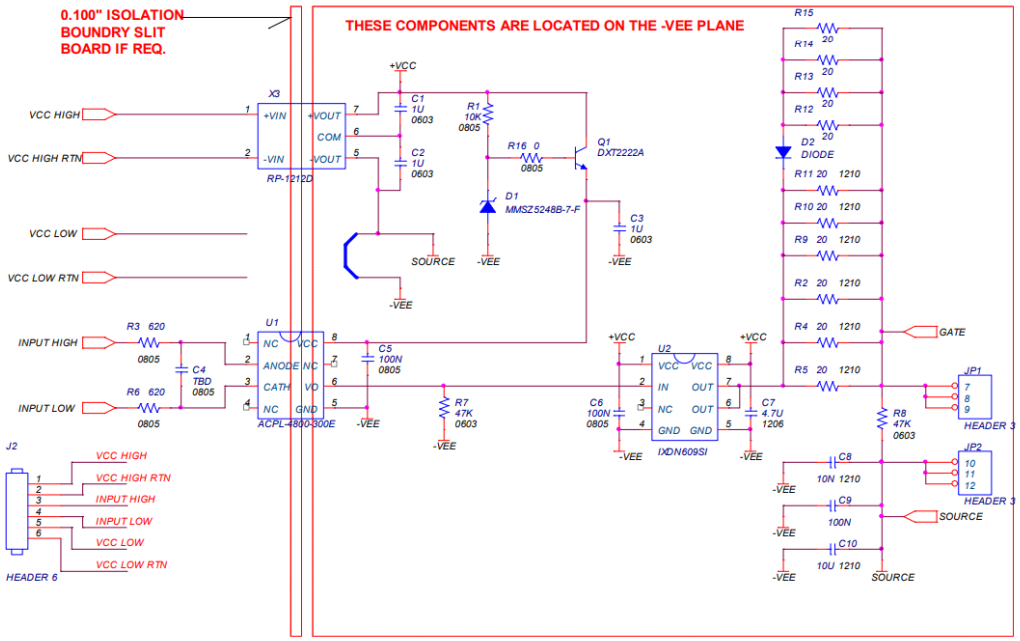


Figure E 2 Isolated gate driver schematic [121].

The mechanical drawing is presented in Figure E3 (units in inches).

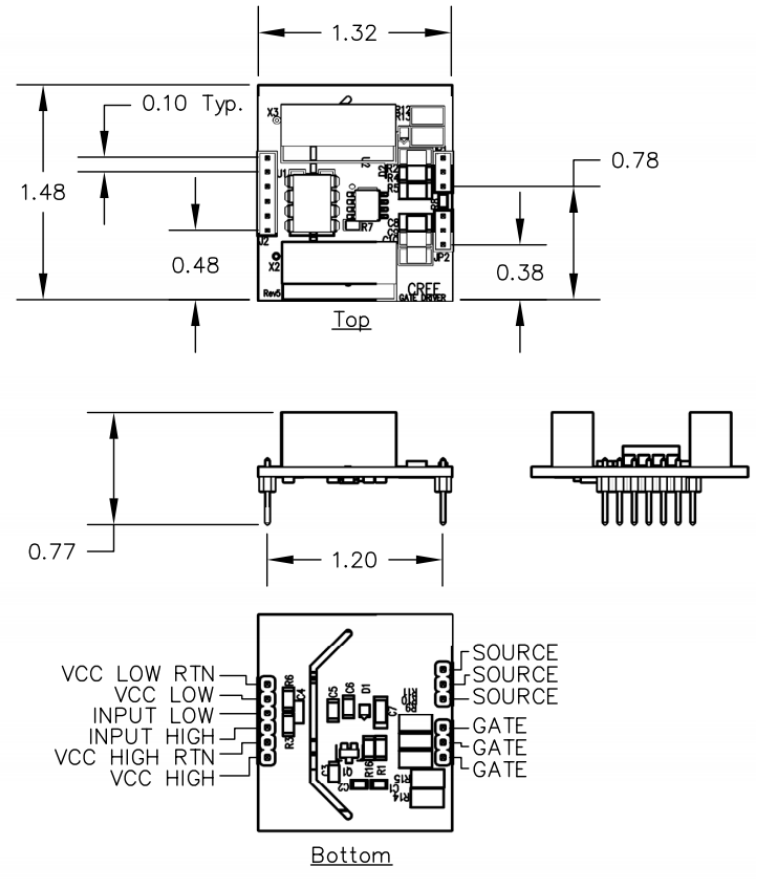


Figure E 3 Mechanical drawing of isolated gate driver *[121]*.

Appendix F: Pico-scope Spectrum Mode

In this Appendix, spectrum mode of PicoScope 6 is introduced.

F.1 Basic controls of Pico-scope spectrum mode

In Pico-scope, spectrum mode plots amplitude on the vertical axis versus frequency on the horizontal axis. The vertical range is measured in dB (decibels) and the horizontal range in Hz (hertz). The Spectrum mode is useful for analysing the frequency components of a signal.

A 700 kHz sine wave is shown in Figure F 1. Which should have just one frequency component at 700 kHz, but since it is not a perfect sine wave some higher frequency components appear with lower amplitude.

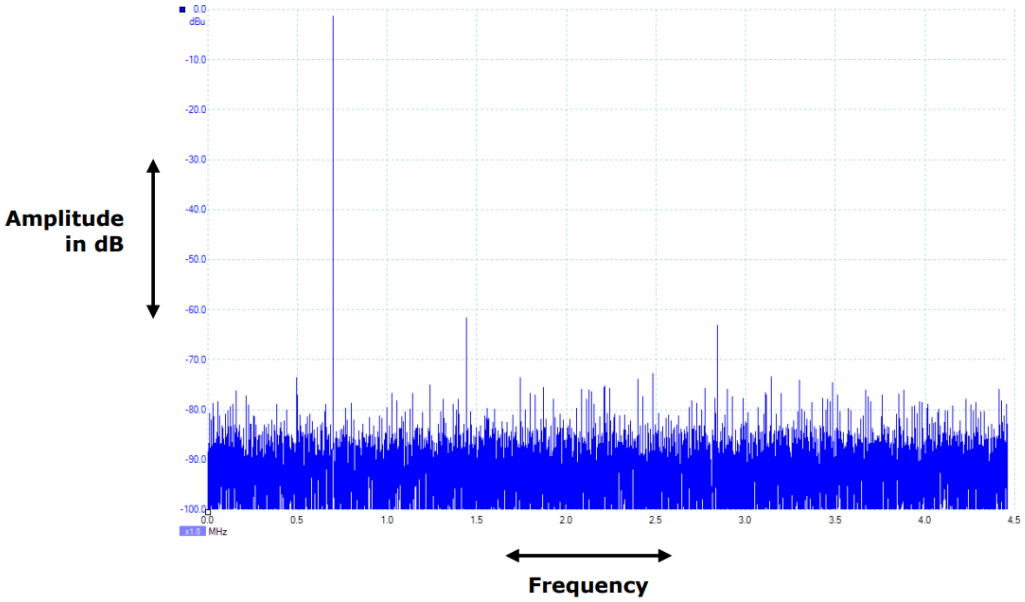


Figure F 1 Spectrum example of a 700 kHz sinusoidal waveform.

The voltage range of the Pico-scope is the full voltage range across all 10 divisions and the full voltage range is from $-20V$ to $+20V$. The minimum and maximum voltage range varies between products. In each of these ranges, the device maintains its full resolution, so a 12-bit device will be 12 bits in each of those ranges. It is important to choose the appropriate voltage range for individual test. In terms of frequency range, multiple frequency ranges are available, from a few hertz up to the full bandwidth of the scope.

F.2 Spectrum options

The spectrum options are depicted in Figure F 2 below.

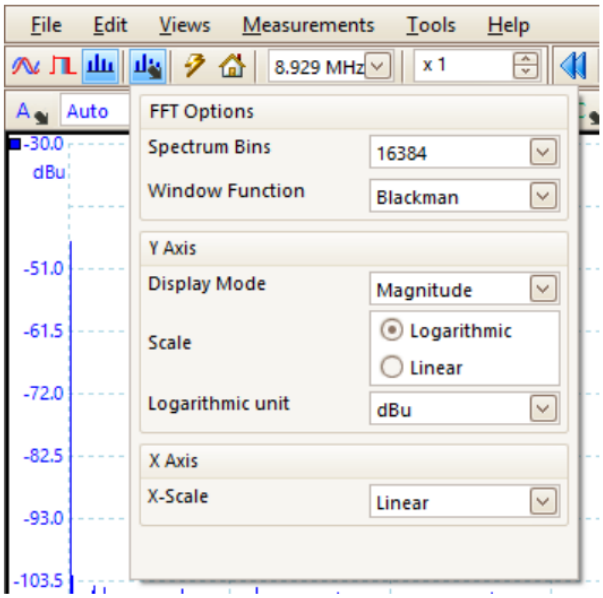


Figure F 2 Spectrum options are presented.

F.2.1 Spectrum bins

Spectrum bins defines the number of frequency bins into which the spectrum is divided. The maximum number of frequency bins can be set, and in this study, it is set to be 1024. One main constraint is that the number of bins cannot greatly exceed half the number of samples in the source waveform. An example showing a frequency range of 199 kHz and 8192 bins across this frequency range is presented in Figure F 3.

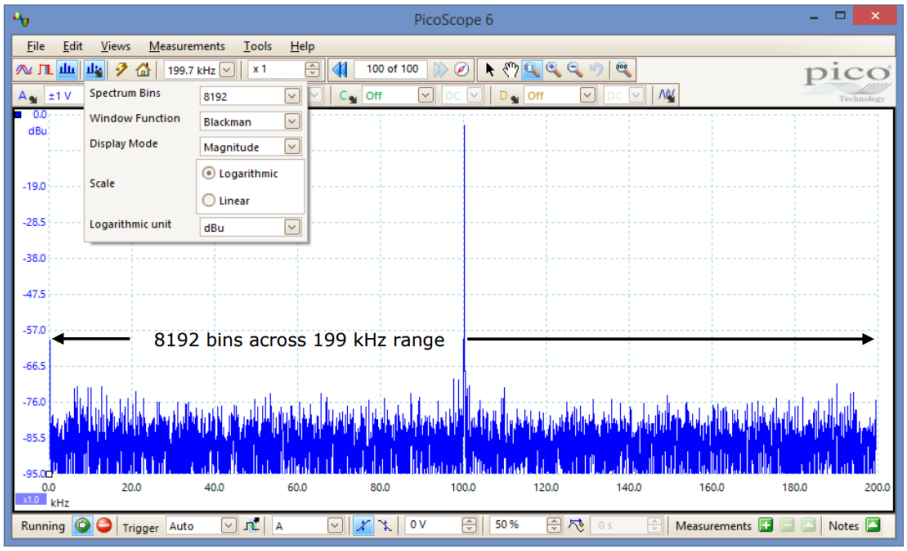


Figure F 3 An example of spectrum bins.

If the source waveform contains fewer samples than required (that is, fewer than twice the number of frequency bins), Pico-Scope zero-pads the waveform up to the next power of two. For example, if the scope view contains 10000 samples, Spectrum Bins is set to 16384, then Pico-Scope zero-pads the waveform to 16384 samples, which is the nearest power of two above 10000. It then uses these 16384 samples to provide 8192 frequency bins, not the 16 384 requested.

F.2.2 Window function

A number of standard window functions are available in Pico-scope. And a brief introduction of each window function is presented in Table F1.

Table F 1 Window function in Pico-scope

Window	Main peak width (bins @ -3 dB)	Highest side lobe (dB)	Side lobe roll-off (dB/octave)	Notes
Blackman	1.68	-58	18	Often used for audio work.
Gaussian	1.33 to 1.79	-42 to -69	6	Gives minimal time and frequency errors.
Triangular	1.28	-27	12	Also called Bartlett window.

Hamming	1.30	-41.9	6	Also called Raised sine squared. Used in speech analysis.
Hann	1.20 to 1.86	-23 to -47	12 to 30	Also called sine squared. Used for audio & vibration.
Blackman-Harris	1.90	-92	6	General-purpose.
Flat-top	2.94	-44	6	Negligible pass-band ripple. Used mainly for calibration.
Rectangular	0.89	-13.2	6	No fading. Maximal sharpness. Used for short transients.

F.2.3 Display mode

There are three display modes available in spectrum mode: Magnitude, Average and Peak Hold.

a. Magnitude

In the Magnitude mode, the spectrum view shows the frequency spectrum of the last waveform captured, whether live or stored in the waveform buffer. An example of Magnitude view is presented in Figure F4.

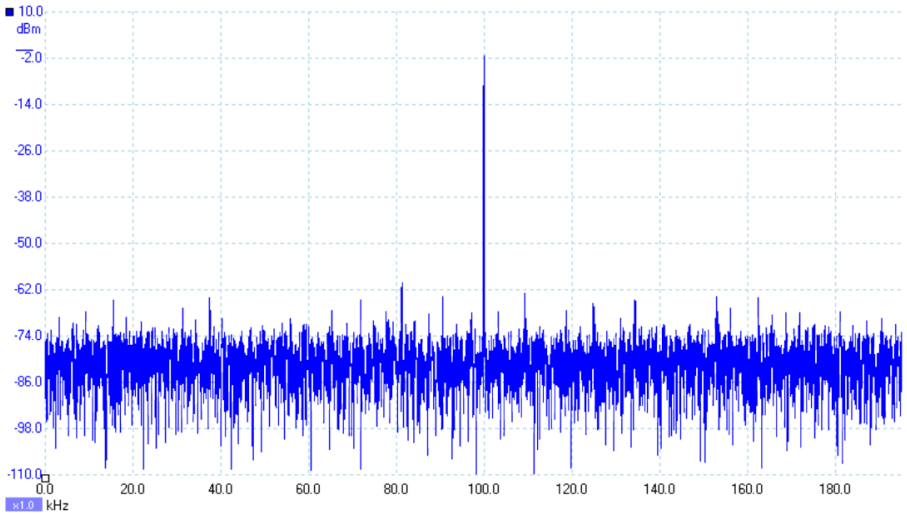


Figure F 4 Example of Magnitude view of spectrum mode in Pico-scope.

b. Average

The spectrum view shows a rolling average of spectra calculated from all the waveforms in the waveform. This has the effect of reducing the noise visible in the spectrum view. The Figure below shows the noise floor being averaged of the above Magnitude view.

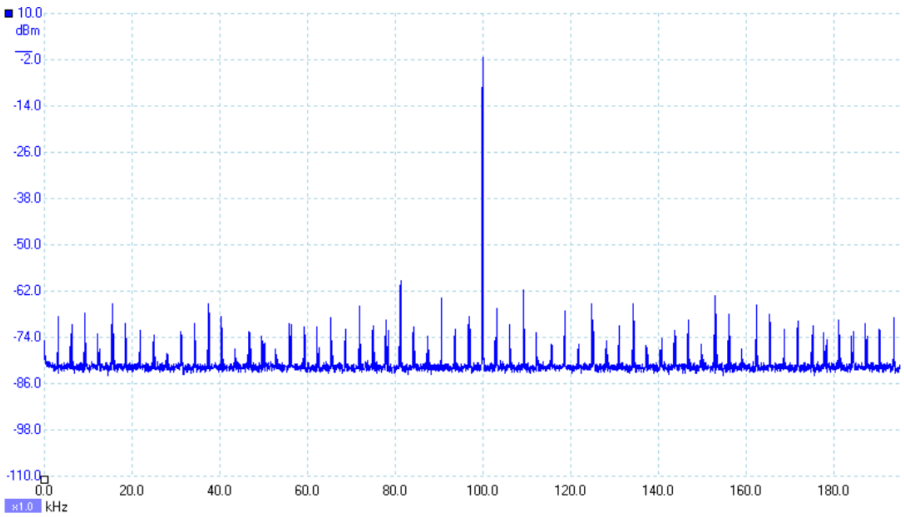


Figure F 5 Example of Average view of spectrum mode in Pico-scope.

c. Peak Hold

The spectrum view shows a rolling maximum of the spectra calculated from all the waveforms in the buffer. In this mode, the amplitude of any frequency band in the spectrum view will either stay the same or increase, but never decrease, over time. The Figure blow shows the effects of peak hold on a waveform that is sweeping up and down in frequency from 1 kHz to100 kHz.

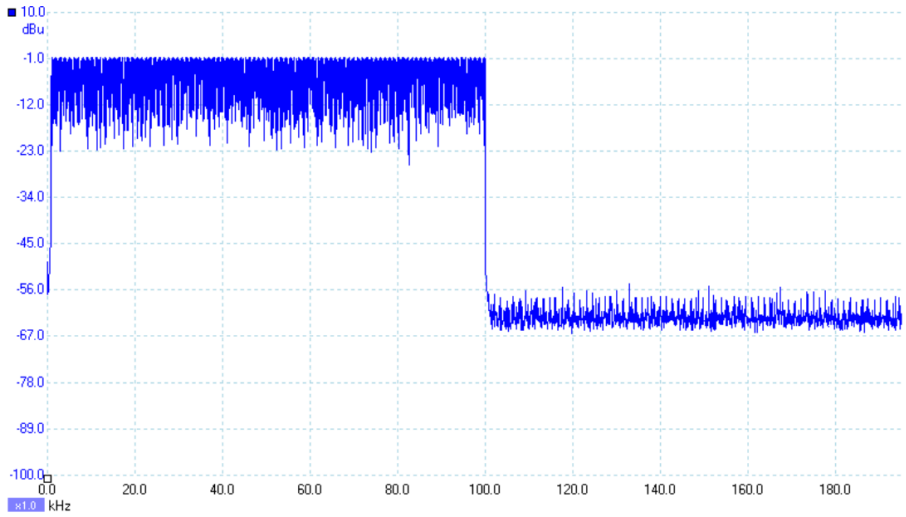


Figure F 6 Example of Peak Hold view of spectrum mode in Pico-scope between 1 kHz and 100 kHz.

In this study, the Peak Hold view function is utilized to find frequency response of the V_{GSpeak}.

F.2.4 Scales

a. Vertical Axis

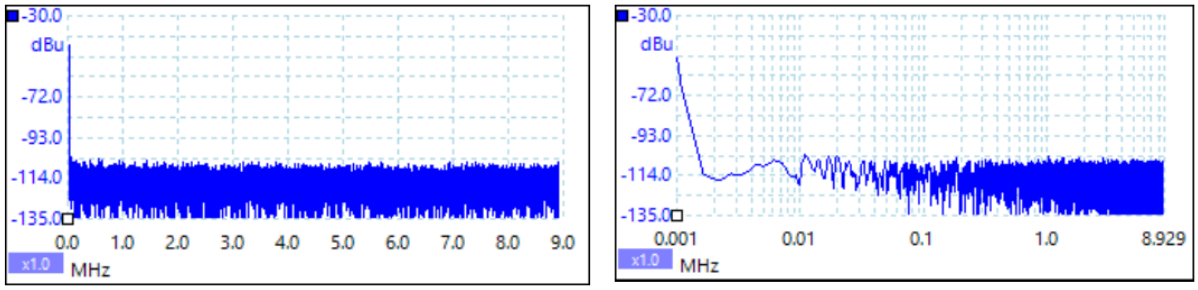
The options of labelling and scaling of the vertical (signal) axis are listed in Table F2 below.

Table F 2 Labelling and scaling types of vertical axis in spectrum mode

Linear	The vertical axis is scaled in volts.
Logarithmic	The vertical axis is scaled in decibels, referred to the level selected below in the Logarithmic unit control.
dBV	Reference level is 1 volt.
dBu	Reference level is 1 milliwatt with a load resistance of 600 ohms. This corresponds to a voltage of about 775 mV.
dBm	Reference level is one milliwatt into the specified load impedance. Enter the load impedance in the box below the Logarithmic unit control.
Arbitrary dB	Reference level is an arbitrary voltage, which you can specify in the box below the Logarithmic unit control.

b. X Axis

The x axis can be set to either linear or log10 as shown in Figure F7 (a) and F7 (b) respectively.



(a) (b)

Figure F 7 X axis display modes: (a) linear mode; (b) log10 mode.

F.3 Conclusion

In this Appendix, the spectrum mode of the Pico-scope is briefly introduced including basic controls, spectrum options, display mode and scales.

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