Suppression of First Side-Band Switching Harmonics Using DC-DC converters with an Advanced Modulation Scheme

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Abstract- **The common DC bus concept has become an attractive solution for future aircraft electrical power systems. This paper considers the case where a battery connected DC-DC converter and a permanent magnet generator connected AC-DC converter are supplying a common dc bus. Applying a proper modulation scheme for DC-DC converters, suppression of the first-band harmonics ($f_c \pm 3f_0$) from the AC-DC converter can be achieved. The proposed harmonic suppression scheme essentially uses the fact that two sinusoidal waveforms with phase shift of π will counteract to each other. For an aircraft engine driving generator, the fundamental frequency f_0 is time-varying and dependent on aircraft engine speeds. This time-varying f_0 is normally derived with a resolver and some measurement error is expected. To ensure the effectiveness of the proposed harmonic suppression scheme, an enhanced pulse width modulation (PWM) compensation scheme has been proposed and implemented every fundamental cycle when the rotor position is detected a zero crossing. The effectiveness of the proposed suppression scheme is validated by experimental results with selected f_c-$3f_0$ component for one DC-DC converter.**

Index Terms- **Power quality, AC-DC converter, DC-DC converter, PWM compensation.**

I. INTRODUCTION

More electric aircraft (MEA) concept has been one of the major trends towards future aerospace development due to its decreased fuel consumption, low maintenance cost [1][2]. To provide more sufficient and reliable power supply, single DC-bus power generation system with parallel-connected generators and battery systems has attracted significant interest [3]. Fig. 1 shows a conceptual diagram of this structure. Expected benefits that can be achieved including less need of cables, convenient integration of energy storage system, and higher redundancy ability under fault condition.

In the DC power generation system shown in Fig. 1, the capacitor bank is used to filter out high-frequency fluctuated currents and flatten the DC-bus voltage [4], such that the DC-bus voltage meets the DO-160E [5] and MIL-STD-704F [6]

standards. This paper is to further optimize the system shown in Fig. 1 and minimize the harmonics on the DC bus capacitors. Capacitors are always bulky and expensive. Minimizing harmonics on the capacitor is critical which can potentially reduce size and improve maintainability of the capacitor [4].
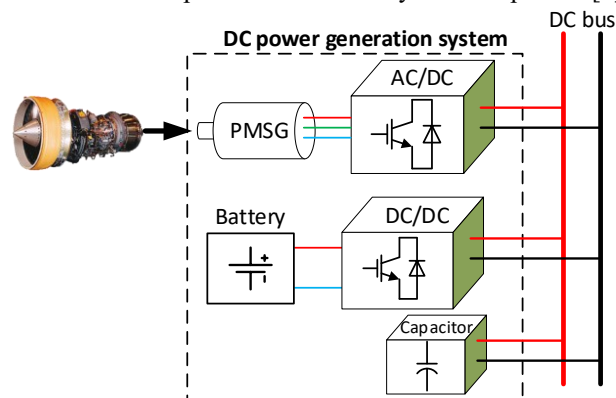

Fig. 1. DC power generation system on MEA.

Active suppression method is to adjust the switching actions of power converters to minimize the harmonics across capacitors. It has received significant attention recently because of its high flexibility and effectiveness. In [7]-[9], solutions with additional circuits are investigated for reducing switching frequency harmonics on capacitors. Those methods require extra power electronic elements and thus increases the cost and complexity of systems.

Without using additional device, some methods minimize the DC-link harmonic based on active control of existing converters. In [10], the capacitor current ripple is reduced by applying nonadjacent switching vectors. In [11] and [12], harmonics on a DC capacitor were reduced on paralleled three-phase voltage-source converters through a fixed phase shift angle on converters. In [13], capacitor harmonics of a dual-generation system are suppressed by applying a 90-degree phase shift on the carrier signal between two AC-DC converters. However, only AC-DC converters supply the DC-link in [10]-[13], which is not the case shown in Fig. 1.

For the system with DC-DC converter, as shown in Fig. 1, modifying the control of DC-DC converter has been well studied to suppress the DC-link harmonics. In [14], suppressed capacitor harmonics are achieved by reducing DC-link voltage using the DC-DC converter. However, the DC-link voltage becomes variable, which is not the case in the DC power system (the DC voltage should be constant in DC power systems). In [15], the authors developed a modified PWM scheme to minimize DC-link harmonics when a boost converter is

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connected to a 2-level DC-AC converter. In [16], DC-link harmonics are suppressed by a real-time calculation of phase-shift angle on the DC-DC converter.

In these publications, most of the methods only focus on suppressing harmonics in the second switching frequency. For example, in [15] and [16], switching frequency of the DC-DC converter are fixed as twice of that on the AC-DC converter. However, first band harmonics are also nonnegligible on DC-link harmonics. In MEA, the permanent magnet synchronous generator (PMSG) is always driven by a high-speed shaft of the engine, thus it should work under flux weakening control with a high modulation index. When the modulation index is higher than 0.9, the first side-band harmonic will cause higher voltage fluctuation on the DC-link capacitor[11][17]. In the DC power generation system of MEA, to the best of the authors' knowledge, there are so far very limited publications addressing suppressing components in the first side band switching harmonics. The reasons for the limited research are as follow:

- There is more than one component in the first switching band, and their frequencies are adjacent. Therefore, it is difficult to filter out an exact component and measure the frequency and phase angle of it.
- To suppress harmonic in the first switching band, the fundamental frequency of AC-DC converter is time-varying and potentially measured with minor errors. This will result in accumulated errors when applying harmonic suppression scheme.

In this paper, we will fill these gaps and focus on suppressing harmonic on the first side band harmonic. A harmonic estimation model of the first-band harmonic from AC-DC converter is provided to solve the first difficulty. For the second difficulty, the measuring error will cause an accumulated error, and compensation should be applied. In [18], the author proposed a method to compensate the accumulated error when the two digital controllers are with a tiny error of crystal frequencies. The switching frequencies of the converters are the same, and the compensation can be applied at any time. However, this is not the case in our method, as the DC-DC converter is involved, and the two carrier frequencies are different. Therefore, this paper proposes an enhanced PWM compensation method. In the proposed method, accumulated errors are compensated in each fundamental cycle, and as a result, the DC-link harmonics show a suppression effectively in consistency.

The paper is organized as follows: Section II gives the basic principle of the proposed harmonic suppression method. Section III presents the impact of the measured fundamental frequency errors which will impose challenges on the effectiveness of harmonic suppression. Section IV gives the proposed PWM compensation method. Section V validates the proposed suppression method and the PWM compensation method with experimental results. Lastly, the conclusion is given in section VI.

II. PROPOSED CAPACITOR HARMONIC MINIMIZATION METHOD

A more detailed system of the DC power generation centre is shown in Fig. 2. The voltage of the DC-link is 270V which is the developing trend of the future electric power system [6]. Comparing to 28V DC power system, higher DC-link voltage

results in lower output current at the same rated power. Therefore, a lower cable diameter can be achieved which will benefit the system. A PMSG supplies electrical power to a DC bus through a two-level AC-DC converter. A high-voltage battery supplies power to the DC bus via a DC-DC converter. The battery is mainly to provide a flexible power flow, and thus the system performance (i.e., efficiency, fault tolerance) can potentially be improved. For the battery capacity, it is determined by the desired optimized objectives. Meanwhile, a bidirectional buck-boost converter is chosen because of its simple structure and high reliability. The AC-DC and DC-DC converters share a common DC-link capacitor. The two converters are controlled with their local primary controllers. A system controller is also used for high-level supervision (secondary) control. The system-level control is to define the power sharing between PMSG system and the battery. This is achieved by defining their load current references ($I_{dc}^{[g]*}$ and $I_L^{[b]*}$). The local controllers of AC-DC and DC-DC converters will receive command and control AC-DC converter and DC-DC converter to inject required DC currents to the DC bus.

Fig. 3 shows the harmonic spectrum of the DC-link current ($i_{dc}^{[g]}$) from the PMSG system when the AC-DC converter works under sinusoidal pulse width modulation (SPWM). It can be noticed that significant components of the current harmonics are observed in $f_c \pm 3f_0$ and $2f_c$. In [11], we used harmonic components (which is of the frequency $2f_c$, f_c is the carrier signal frequency) generated from one AC-DC converter to suppress that from another AC-DC converter. Within this section, we will build upon our previous findings and explore the potentiality to use a DC-DC converter to suppress harmonics from an AC-DC converter, especially the $f_c \pm 3f_0$ components (where f_0 is the fundamental frequency). The proposed method is illustrated by focusing on the $f_c - 3f_0$ harmonic component studies.
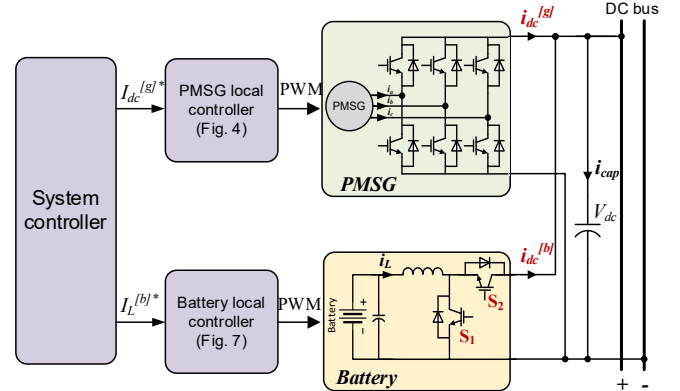

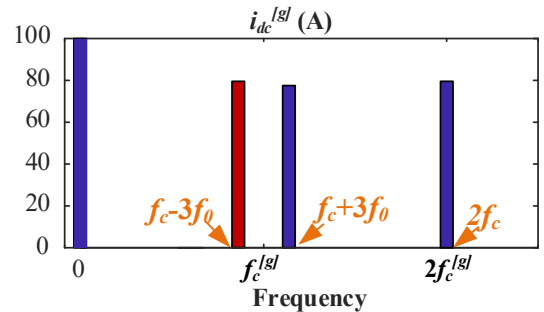Fig. 2. Control architecture of the hybrid generation system.

Fig. 3. Spectrum of DC-link current from PMSG system.

A. Harmonic analysis of a two-level AC-DC converter

This harmonic analysis of a PMSG connected AC-DC converter has been well studied in [11]. There, we pointed out that the current harmonic component of f_c-$3f_0$ frequency, from the PMSG connected AC-DC converter can be expressed as

$$i_{dc,1,-3}(t) \approx \frac{3\sqrt{i_d^2+i_q^2}}{\pi}J_4\left(\frac{\pi}{2}M\right)\cos\left[2\pi(f_c-3f_0)t+\theta_c-3\beta-4\alpha\right]$$
$$-\frac{3\sqrt{i_d^2+i_q^2}}{\pi}J_2\left(\frac{\pi}{2}M\right)\cos\left[2\pi(f_c-3f_0)t+\theta_c-3\beta-2\alpha\right] \quad (1)$$

where i_d and i_q are d- and q-axis currents, $J_n()$ is the Bessel function of the first kind, M is the modulation index, θ_c is the phase angle of the carrier signal, α is the phase angle between fundamental AC currents and voltages (i.e. power factor angle), and β is the phase angle of AC current with reference to the electrical generator back-EMF. In (1), it is assumed that when t=0s, the machine rotor position is aligned with phase A (no initial angle). Angles α and β can be achieved from voltages and currents in dq-frame which are

$$\beta = \text{Arg}\left(i_d + ji_q\right) \quad (2)$$

$$\alpha = \text{Arg}\left(v_d + jv_q\right) - \beta \quad (3)$$

where v_d and v_q are d- and q-axis voltages. The function Arg() gives the angle of complex number $(x+jy)$. From (1), the phase angle $(\theta_{dc,1,-3}^{[g]})$ of the $i_{dc1,-3}(t)$ when t=0 can be given as

$$\theta_{dc,1,-3}^{[g]} = \text{Arg}\left(\begin{matrix} \frac{3\sqrt{i_d^2+i_q^2}}{\pi}J_4\left(\frac{\pi}{2}M\right)\angle(\theta_c-3\beta-4\alpha) \\ -\frac{3\sqrt{i_d^2+i_q^2}}{\pi}J_2\left(\frac{\pi}{2}M\right)\angle(\theta_c-3\beta-2\alpha) \end{matrix} \right) \quad (4)$$

With measured currents i_d, i_q, voltage references v_d, v_q, and modulation index M, the information of harmonic component f_c-$3f_0$, i.e. $i_{dc1,-3}(t)$, can be derived using (1) - (3). Its phase angle $\theta_{dc1,-3}^{[g]}$ can be derived from (4). Information of the AC-DC converters, i.e., i_d, i_q, v_d, v_q, M, and f_c-$3f_0$, will be sent to the controller of the DC-DC converter, as shown in Fig. 4. For the PMSG control, a cascaded control structure has been used, with current control being the inner loop. A flux-weakening control is applied in the outer control loop. This is due to the fact that in MEA applications, PMSG is driven by the high-speed shaft of an aircraft engine. The stator output voltage $\sqrt{v_d^2+v_q^2}$ is controlled by injecting a negative flux current component i_d. The output current i_{dc} of the AC-DC converter is also controlled with its reference $i_{dc}^{[g]*}$ given by the system-level controller.

In Fig. 4, it can also be seen that a compensation pulse is generated when the rotor position hits zero. The usage of these information will be discussed in Section IV.B.

B. Harmonic analysis of a bidirectional buck-boost DC-DC converter

Switching signals from a buck-boost DC-DC converter (shown in Fig. 2) are normally generated by comparing the duty cycle reference and the carrier signal with a triangle waveform as shown Fig. 5.

The two switches S_1 and S_2 are operated in a complementary manner. If the carrier signal is above the duty cycle line, switch S_1 is on. If the carrier signal is below the duty cycle line, switch

S_2 is on. With this switching pattern, the current $i_{dc}^{[b]}$ is generated and its spectrum is shown in Fig. 6. It can be seen that harmonic components are essentially around switching frequencies and its multiple times (i.e. $f_c^{[b]}$, $2f_c^{[b]}$ …). The first switching harmonics of $f_c^{[b]}$ is of most significance and this component will be used to suppress the f_c-$3f_0$ from AC-DC converter.
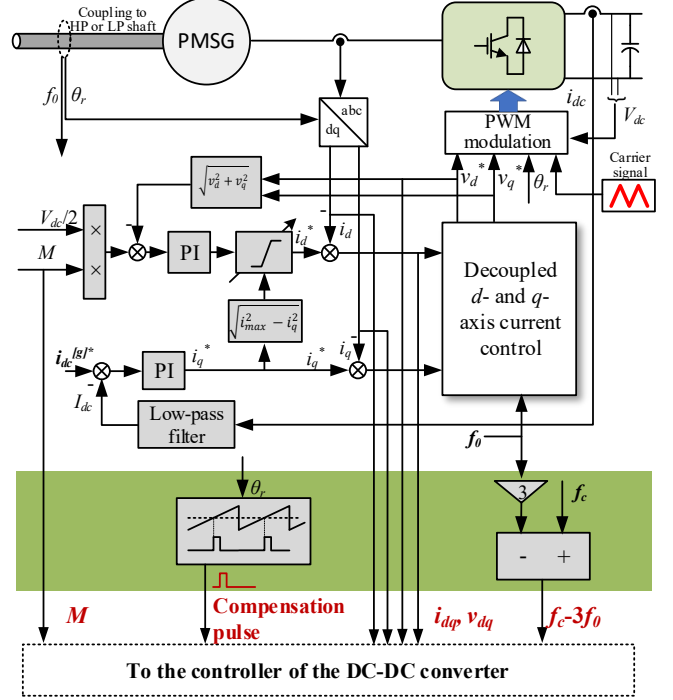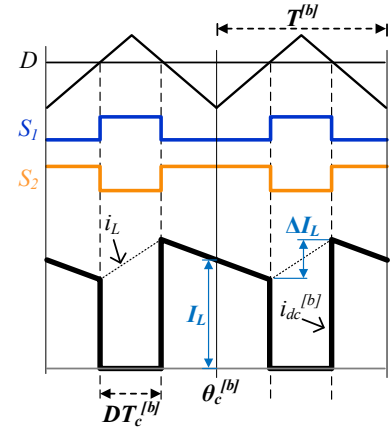

Fig. 4. Control diagram of PMSG system.

Fig. 5. PWM modulation of DC-DC converter and the dc-link current $i_{dc}^{[b]}$.

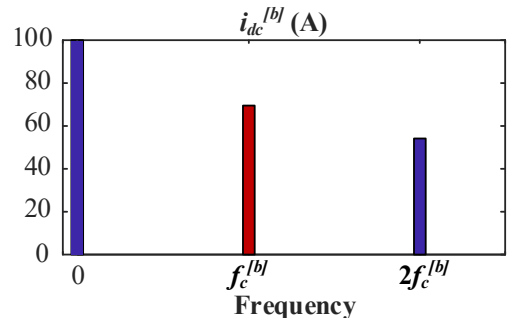

Fig. 6. Spectrum of DC-link current from DC-DC converter.

To simplify the analysis, it is assumed that the inductor current is constant as I_L, and the converter works under continuous current mode. Thus, the dc current flowing into the dc-bus capacitor, $i_{dc}^{[b]}$, can be given as

$$i_{dc}^{[b]} = \begin{cases} I_L, & 0 < t < \dfrac{(1-D)T^{[b]}}{2} \\ 0, & \dfrac{(1-D)T^{[b]}}{2} < t < \dfrac{(1+D)T^{[b]}}{2} \\ I_L & \dfrac{(1+D)T^{[b]}}{2} < t < T^{[b]} \end{cases} \quad (5)$$

Considering its symmetry, the current $i_{dc}^{[b]}$ in (5) can be expressed using Fourier expansion as

$$i_{dc}^{[b]} = I_0^{[b]} + \sum_{k=1}^{\infty} I_k^{[b]} \cos\left(2k\pi f_c^{[b]} t + k\theta_c^{[b]}\right) \quad (6)$$

where

$$f_c^{[b]} = \frac{1}{T^{[b]}} \quad (7)$$

From (6), it can be seen that the phase angles of $i_{dc}^{[b]}$ harmonics depend on the carrier signal phase angle $\theta_c^{[b]}$. In addition, the Fourier coefficients in (6) are given as

$$I_0^{[b]} = I_L(1-D) \quad (8)$$

$$I_{k(k \neq 0)}^{[b]} = 2 f_c^{[b]} \int_0^{\frac{1}{f_c^{[b]}}} i_{dc}^{[b]}(t) \cos\left(2k\pi f_c^{[b]} t\right) dt$$
$$= \frac{2I_L}{k\pi(1-D)} \sin(k\pi D) \quad (9)$$

As mentioned before, this paper illustrates to use the DC-DC converter to suppress the first side band harmonic from an AC-DC converter (i.e. f_c-$3f_0$), thus only the first harmonic from the DC-DC converter, i.e. k=1 in (6) and (9), will be used. This harmonic is denoted as $i_{dc,1}^{[b]}$ and can be expressed as

$$i_{dc,1}^{[b]} = \frac{2I_L}{\pi(1-D)} \sin(\pi D) \cos\left(2\pi f_c^{[b]} t + \theta_c^{[b]}\right) \quad (10)$$

From (10), it can be concluded that active control of the phase angle of current $i_{dc}^{[b]}$ can be achieved by adjusting the carrier signal's phase angle $\theta_c^{[b]}$.

In practice, the battery current i_L is not constant, but with a ripple ΔI_L (peak-to-peak), and ΔI_L is always designed to be within $0.2I_L$. In digital controller, measuring ΔI_L will make the control complicated. Hence, we neglect ΔI_L and use (10) to predict $i_{dc,1}^{[b]}$. To evaluate the influence of neglecting ΔI_L, we calculated the errors of magnitude and phase angle when considering the ripple, as shown in Fig. 7a and b. Under any duty cycle (D), the magnitude error is within 0.15%, which is quite neglectable. Meanwhile, the error of phase angle is less than 3°. Compared to desired phase angle difference (180°) which will be discussed in the next section, 3° error will not cause significant reduction of harmonic suppression effect.
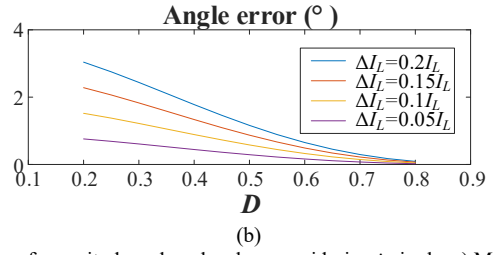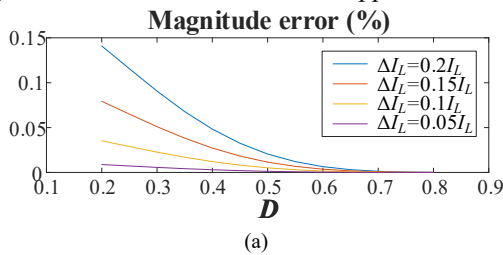

(a)

(b)

Fig. 7. Errors of magnitude and angle when considering i_L ripple. a) Magnitude. b) Angle.

C. Proposed harmonic minimization method using a DC-DC converter

Our proposed current harmonic suppression scheme essentially is based on the fact that two sinusoidal currents of the same magnitude will counteract each other if they are of 180° phase shift. With this fact, we can use $i_{dc,1}^{[b]}$ from the DC-DC converter as an active harmonic injection source to cancel the f_c-$3f_0$ harmonic component from the AC-DC converter $i_{dc,1,-3}(t)$. To achieve that, the frequency of the carrier signal ($f_c^{[b]}$) of the DC-DC converter should be set to be f_c-$3f_0$, i.e.

$$f_c^{[b]} = f_c - 3f_0 \quad (11)$$

To achieve the phase angle difference of 180° between two harmonics, the phase angle of the PWM carrier signal in the battery connected DC-DC converter should be set as

$$\theta_c^{[b]} = \theta_{dc,1,-3}^{[g]} + \pi \quad (12)$$

where $\theta_c^{[b]}$ is the phase angle of the carrier signal of the DC-DC converter, $\theta_{dc,1,-3}^{[g]}$ is the phase angle of the carrier signal of the AC-DC converter.

With (11) and (12), the modulation scheme of the DC-DC converter control can be developed as shown in Fig. 8. There, the carrier frequency $f_c^{[b]}$ ($1/T_c^{[b]}$) is set to be f_c-$3f_0$ and its phase angle $\theta_c^{[b]}$ is set to be $\theta_{dc,1,-3}^{[g]} + \pi$ using information from PMSG control system and equation (2)-(4). Together with the duty cycle D, the modified PWM signals are generated.
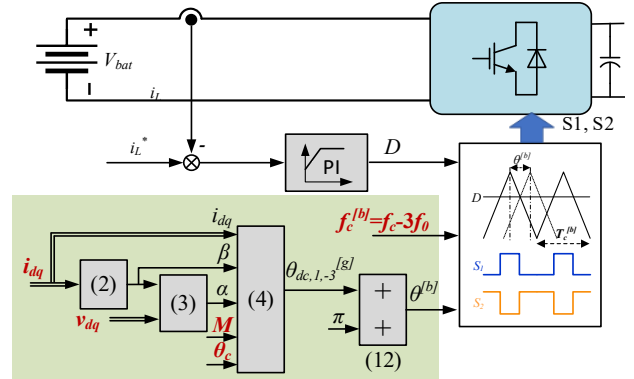

Fig. 8. Control diagram of battery system.

For the bi-directional buck-boost converter, the inductor is designed to limit the current ripple of i_L (ΔI_L). With a lower switching frequency, the converter will generate higher ΔI_L. Hence, the inductance should be designed when the switching frequency is set as

$$f_c^{[b]} = f_c - 3f_0^{max} \quad (13)$$

where f_0^{max} is the maximum value of f_0.

III. IMPACT OF SWITCHING FREQUENCY ERRORS

In the previous section, we have pointed out that setting the carrier frequency $f_c^{[b]} = f_c\text{-}3f_0$ and $\theta_c^{[b]} = \theta_{dc,1,-3}^{[g]} + \pi$, the first sideband harmonic of $f_c\text{-}3f_0$ from the AC-DC converter can be suppressed using the first harmonic component from the DC-DC converter. However, during implementation, setting $f_c^{[b]} = f_c\text{-}3f_0$ is not that straightforward.

One reason is that although the modulation frequency f_c for the AC-DC converter is set by the controller, the frequency f_0 is a measured value $\hat{f}_0$ and is normally derived from a PMSG speed resolver. Since the measured frequency $\hat{f}_0$ is subject to some degree of errors because of the resolution of the position sensor, it can be concluded that using this measured $\hat{f}_0$ can potentially result in discrepancies between $f_c^{[b]}$ and $f_c\text{-}3f_0$. This, in return, will undermine the performance of harmonic suppression since this error (which can be tiny) will be accumulated and resulted in significant difference between $\theta_c^{[b]}$ and $\theta_{dc,1,-3}^{[g]} + \pi$. As a result, the effectiveness of harmonic suppression cannot be achieved at all.

Meanwhile, if each converter is using their local controller, the frequencies of crystals inside digital controllers cannot be exactly the same, which will induce the deviation between f_c and $\hat{f}_c$ [11]. $\hat{f}_c$ is the "virtual" switching frequency if the digital controller of AC-DC converter uses the same crystal of DC-DC converter. In this case, communication between the two local controllers should be designed, i.e., CAN, RS485.

Fig. 9 illustrates a scenario of the case when $f_c^{[b]}$ and $f_c\text{-}3f_0$ are not equal due to the errors. There, two components, i.e., $i_1(t)$ and $i_2(t)$ are used to represent harmonic components of $f_c^{[b]}$ (assumed to be f_1) and $f_c\text{-}3f_0$ (assumed to be f_2) from DC-DC and AC-DC converters, respectively. Due to the error in f_c and f_0, the carrier frequency $f_c^{[b]}$ is set to $\hat{f}_c - 3\hat{f}_0$ instead of $f_c\text{-}3f_0$. Assuming that $f_1{:}f_2\ (\hat{f}_c - 3\hat{f}_0{:}\ f_c - 3f_0) = 0.96{:}1$ and these two harmonic components have a phase difference of π initially. These two components counteract each other fully at the beginning. However, due to the discrepancy of the two frequencies, the phase difference between these two is actually fluctuating instead of being a constant value of π. Thus, the two components are essentially modulating each other rather than suppressing each other as shown in Fig. 9.

To mitigate the impact of such f_0 measurement error and achieve an effective suppression in a consistent way, compensation of such error is essential. This will be discussed in the next section.
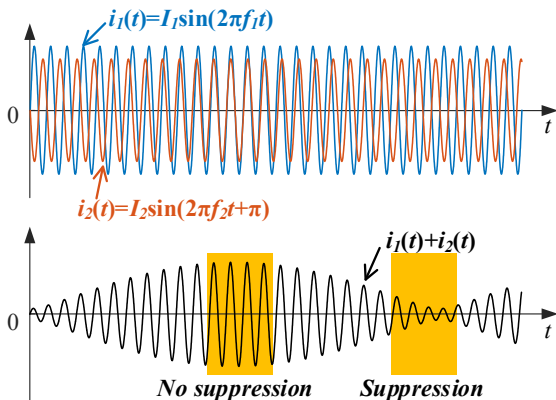

Fig. 9. Sum up of two un-synchronized components.

IV. MITIGATION OF FUNDAMENTAL FREQUENCY ERROR WITH PWM COMPENSATION

A. Applying compensation to avoid the accumulated error

As discussed before, error of $f_c^{[b]}$ will lead to a situation that the phase angle of the targeted harmonics from the AC-DC converter and the DC-DC converter are fluctuating rather an of π phase shift. To mitigate the impact of this error, compensation should be applied before this error becomes significant. One way to mitigate such accumulated error is simply resetting the phase angles as shown in Fig. 10. It can be seen that adding two components (i_1 and i_2) with initial π phase difference and very small frequency discrepancies will result in a fluctuated waveform. However, to avoid situation in Fig. 9, compensation will be applied when the accumulated error is not significant ($\pi/6$ in Fig. 10). The compensation essentially is to reset the phase angle of $i_2(t)$ to be with a π phase difference again compared to that of $i_1(t)$. After each compensation, although the error between $i_1(t)$ and $i_2(t)$ will be accumulated again, the error can be always kept within a tolerable range by taking compensation actions in every a few cycles.
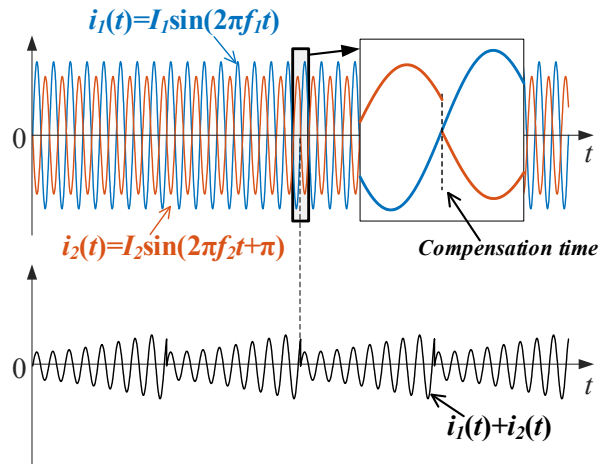

Fig. 10. Compensation actions on accumulated errors.

B. Compensation instant identification

The same concept in Fig. 10 can be used to mitigate the errors of $\hat{f}_c$ and $\hat{f}_0$ when setting the frequency of PWM carrier signal within the DC-DC converter $f_c^{[b]}$ to be $f_c\text{-}3f_0$ (in reality it is $\hat{f}_c - 3\hat{f}_0$). One of the key implementation aspects of the compensation is to identify the time instant when to apply such compensation.

Considering the fact that f_0 varies according to the rotor speed of PMSG, the carrier frequency of the DC-DC converter ($f_c\text{-}3f_0$) is thus not fixed. On the other hand, the carrier signal of the AC-DC converter is a triangle waveform with a fixed frequency and phase angle. In that case, we can take the carrier signal of the AC-DC converter (of frequency f_c) as the reference signal. The carrier signal (of frequency $\hat{f}_c - 3\hat{f}_0$) of the DC-DC converter needs to be compensated every a few cycles to avoid accumulated error as it should be with a frequency of $f_c\text{-}3f_0$. One potential good choice is to select the compensation time instant to be when the PMSG rotor position is detected "Zero". It is a very logic selection as a fundamental cycle of the PMSG is a reasonable small amount of time and the zero-detection signal from rotor position is convenient to derive in practice.
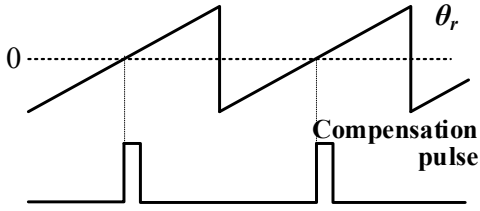
Fig. 11. Compensation pulse generation.

As shown in Fig. 11, a compensation pulse is generated when rotor position θ_r hits zero. The controller of the AC-DC converter sends this pulse together with information for phase-shift angle calculation, i.e., i_{dq}, v_{dq}, M, θ_c, to the controller of the DC-DC converter, as shown in Fig. 12.
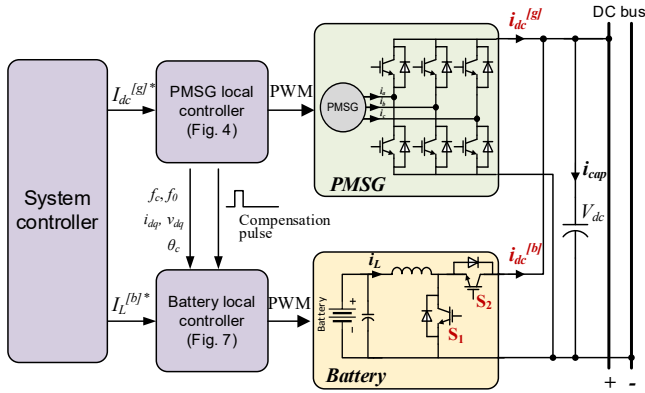

Fig. 12. Control architecture of the hybrid generation system considering PWM compensation.

After the DC-DC controller receives the pulse, compensation will be applied immediately. At that time instant, the frequency of the DC-DC converter carrier signal will be refreshed to a new $\hat{f}_c - 3\hat{f}_0$ at that time instant. A time shift (ΔT) of the carrier signal will also be applied to the DC-DC converter microcontroller as shown in Fig. 13. This time shift ΔT is given as

$$\Delta T = \frac{\theta_c^{[b]}}{2\pi\left(\hat{f}_c - 3\hat{f}_0\right)} \tag{14}$$

In the digital controller we used during experiment (TI DSP TMS320F28379D), the carrier signal is generated from a time-base counter [20]. The desired time shift ΔT is achieved by setting the proper counting direction and the initial counting value when the compensation pulse comes.

V. EXPERIMENT RESULTS

To validate the proposed harmonic suppression-scheme, an experimental rig has been set up as shown in Fig. 14. PMSG is represented by a programmable AC source together with three-phase inductors. A phase-locked loop (PLL) is implemented in the controller to achieve the phase angle of fundamental AC voltages. The battery system is represented by a DC power supply which is connected to a DC-DC converter. Since the harmonic suppression scheme is related to AC-DC and DC-DC converter, using a three-phase AC source and a DC power supply to represent the PMSG and battery will not really affect the effectiveness of the proposed harmonic suppression scheme. The DC source is used to represent the battery with a

constant voltage output of 200 V. The system is controlled using TI DSP TMS320F28379D. The parameters of the experiment are shown in Table I. The total output power of the AC-DC converter and the DC-DC converter is 2 kW. The AC fundamental frequency is 50Hz. The switching frequency of the AC-DC converter, f_c, is set at 4000Hz. However, to emulate the two converters controlled by two digital controllers (thus with different crystal frequencies), f_c is set as 4.00016kHz. When no harmonic suppression scheme is applied, the DC-DC converter uses the "same" carrier signal as that of the AC-DC converter with is 4kHz, which means $f_{cl}^{[b]}$=4kHz. For the proposed suppression method, the carrier signal frequency of the DC-DC converter ($f_c^{[b]}$) is set to be f_c-3f_0, i.e., 3.85 kHz.
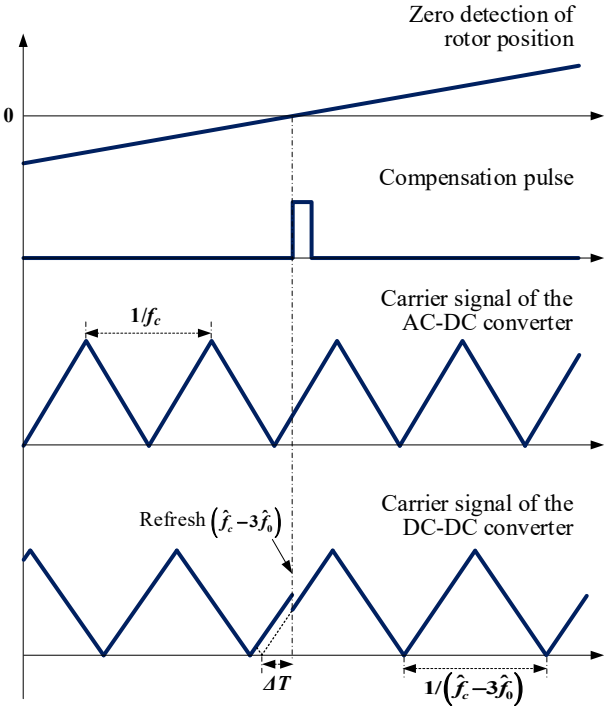

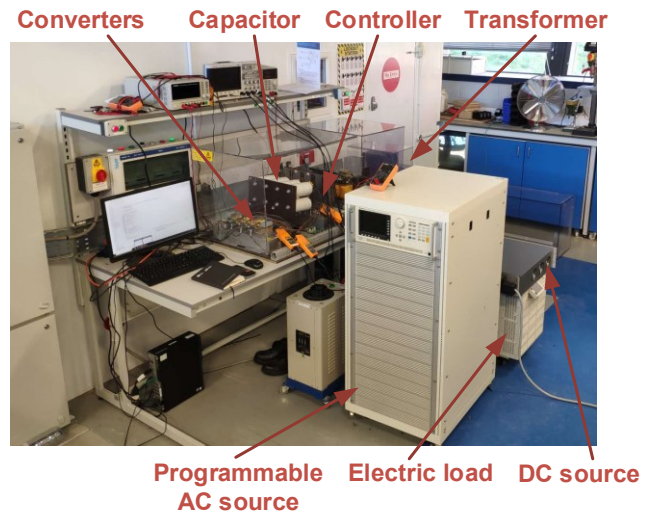Fig. 13. Compensation actions on carrier signals from PMSG and battery.

Fig. 14. Experiment setup.

TABLE I. Experimental parameters

Category	Parameters	Values
DC-link	DC link capacitance	4.4 mF
	DC bus voltage	270V
	Output power	2 KW
The AC-DC converter	Phase inductance	1 mH
	Frequencies of AC side f_0	50 Hz
	Voltages of AC side	250 V
	Switching frequency f_c	4 kHz
	Modulation index	0.90
The DC-DC converter	Battery voltage	200V
	Carrier frequency f_{c1} [b]	4 kHz
	Carrier frequency f_c [b]	3.85 kHz

The experimental diagram is the same as Fig. 12. The AC-DC and DC-DC converters supply the DC-link according to the reference sent by the system-level controller. DC-bus currents, including $i_{dc}^{[g]}$, $i_{dc}^{[b]}$ and i_{cap}, are measured to validate the proposed method. The effectiveness of suppression can be validated more obviously in frequency domain, and thus FFT results of i_{cap} will be given in following analysis.

When the DC power system works without harmonic suppression scheme, Fig. 15 shows the DC-bus currents from the AC-DC converter and the DC-DC converter ($i_{dc}^{[g]}$ and $i_{dc}^{[b]}$). The current flowing into the capacitor i_{cap} and its spectrum are shown in this figure. Both converters use the same carrier signal. The AC-DC converter generates harmonics on $f_c \pm 3f_0$ and $2f_c$, and the DC-DC converter generates harmonics on f_c and $2f_c$. These components are summed up together on the DC-link capacitor current.
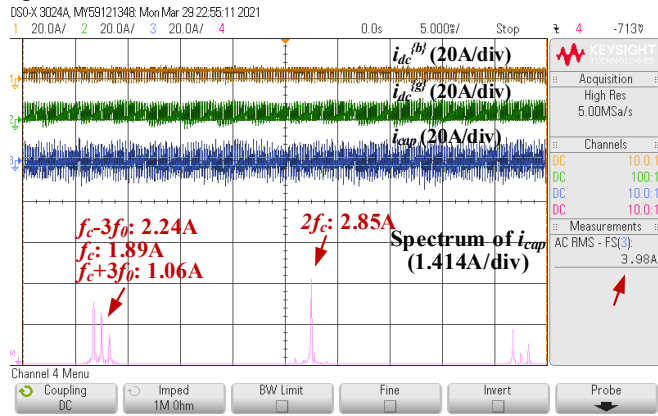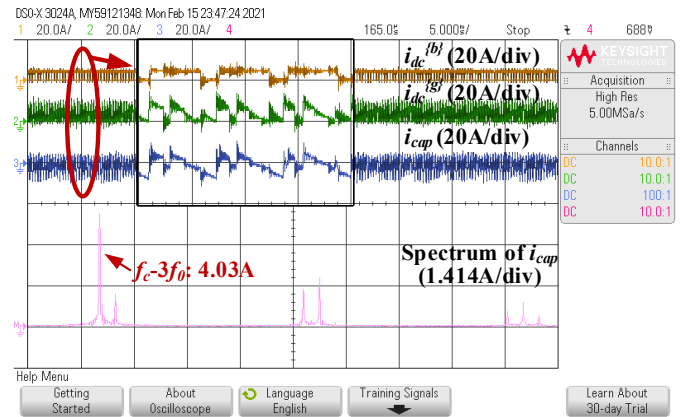

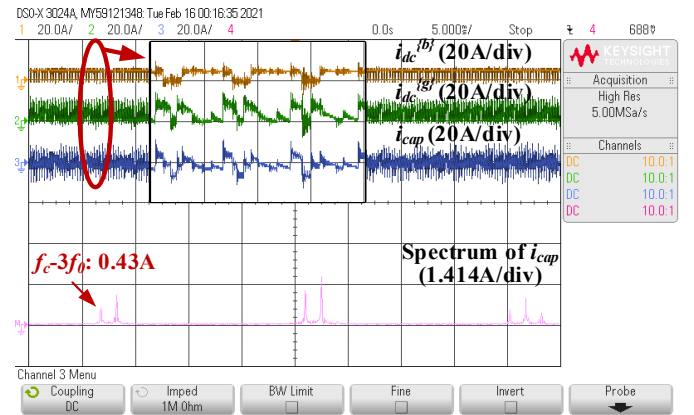Fig. 15. Experimental results with no harmonic suppression scheme.

To suppress the f_c-$3f_0$ harmonic, the carrier frequency of the DC-DC converter is set as f_c-$3f_0$, i.e., 3.85 kHz. As discussed in Section III, the accumulated error caused by measuring error of $\hat{f}_c$ and $\hat{f}_0$ will undermine the performance of harmonic suppression scheme and result in a fluctuating component. Two screen shots from scopes are shown in Fig. 16a and b at different time instant during one test. It can be seen that the magnitudes of the f_c-$3f_0$ component of i_{cap} are different with a value of 0.43A and 4.03A. We also record a video to clearly show the fluctuation of this component.

To compensate this accumulated error, the proposed suppression method together with the PWM compensation scheme are implemented. Compensation pulses are generated in every 20 ms (50 Hz), which is the same as the periods of fundamental AC voltages, as shown in Fig. 17. It can be seen that, with continuous compensation in every fundamental cycle,

the f_c-$3f_0$ harmonic can be suppressed in consistency, as shown in Fig. 17. Compared with the case without harmonic suppression scheme in Fig. 15, harmonic in the frequency of f_c-$3f_0$ is suppressed from 2.24A to 0.42A (81.2% reduction). For harmonic of the frequency f_c, there was a component with 2.08A in the conventional case (Fig. 15), but no component showing in f_c when the proposed method is applied (Fig. 17). This is because the switching frequency of the DC-DC converter is changed from f_c to f_c-$3f_0$. It is also interesting to notice the change of second-order harmonics of i_{cap}. With the proposed scheme, there are two components on the second band, i.e. $2f_c$ and $2f_c$-$6f_0$. The $2f_c$ is from the AC-DC converter, the $2f_c$-$6f_0$ component is actually from the DC-DC converter. This does not mean that the proposed scheme will generate more harmonics at the second switching frequency level. Actually, without using the harmonic compensation scheme, both AC-DC and DC-DC converters will generate $2f_c$ components and these two components will add on each other at $2f_c$ in the spectrum. The suppression scheme helps reduce the root mean square (RMS) value of i_{cap} from 3.98A to 2.93A (26.4% reduction). This will extend the lifetime of the capacitor because a lower hotspot temperature can be achieved with lower RMS current. To further validate the effectiveness of the proposed PWM compensation method, a video is given to show the comparison between the spectrums with and without PWM compensation as the time elapses.

(a)

(b)

Fig. 16. f_c-$3f_0$ harmonic suppression without PWM compensation. a) Two components modulate each other. b) Two components counteract each other.
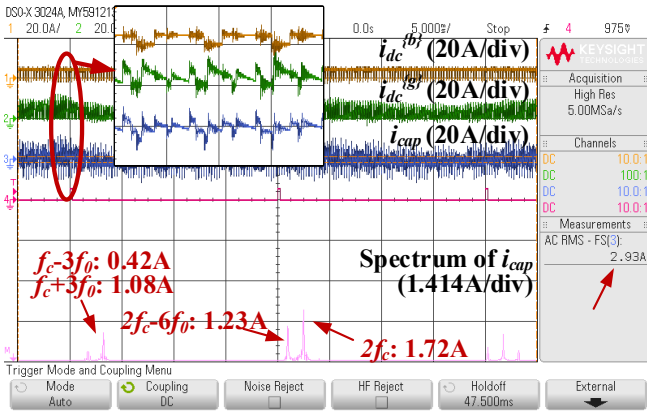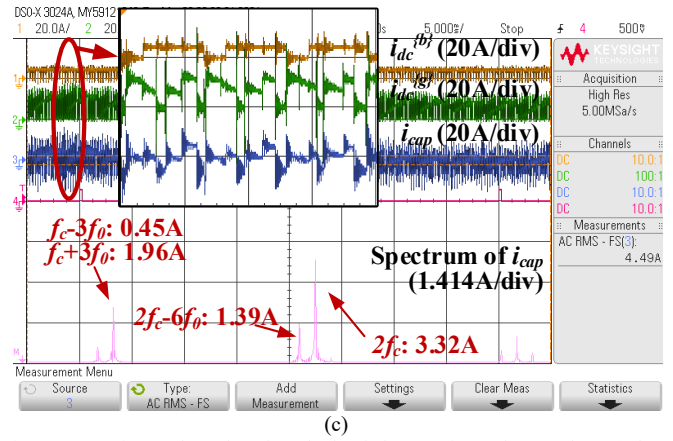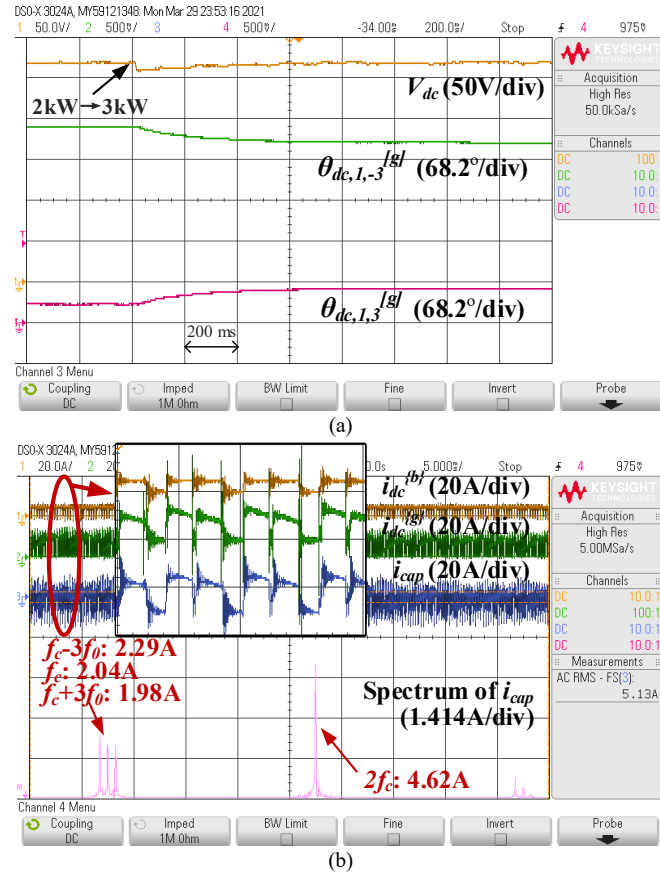
Fig. 17. Experimental results with the proposed harmonic suppression scheme.

The experimental results when the load changes from 2kW to 3kW is conducted, as shown in Fig. 18a. Because of the large scale (200ms/div) on the oscilloscope, the capacitor current (i_{cap}) shows a large distortion, and thus it will not be shown in Fig. 18a. The output power of DC-DC converter is remaining the same, and the AC-DC converter compensates the 1kW step change. The DC-link voltage (V_{dc}) shows a drop and recovery after the load change. Meanwhile, a higher output power of the AC-DC converter results in a variation of the phase angle of f_c-$3f_0$ component ($\theta_{dc,1,-3}^{[g]}$), as shown in Fig. 18a.

When the system operates back to steady state, the total output power is 3kW. The proposed method can still effectively suppress the f_c-$3f_0$ on i_{cap}, as shown in Fig. 18c. Compared to the case without suppression (Fig. 18b), f_c-$3f_0$ harmonic of i_{cap} is suppressed from 2.29A to 0.45A (80.3% reduction). RMS value of i_{cap} is also reduced from 5.13A to 4.49A.

(a)

(b)

Fig. 18. Experimental results when the load changes from 2kW to 3kW. a) $\theta_{dc,1,-3}^{[g]}$ variation. b) 3kW, without harmonic suppression scheme. c) 3kW, with harmonic suppression scheme.

VI. CONCLUSION

For a DC power generation system in MEA, this paper proposed a suppression method of DC-link harmonic in the first switching band frequency. The method is to actively adjust the switching frequency and phase-shift angle of the carrier signal in the battery system. An enhanced PWM compensation method is also proposed because there are measuring errors on the AC fundamental frequency. Finally, experiment results are given to validate the effectiveness of the proposed suppression method. The new PWM compensation scheme is proven to provide a continuous suppression on the DC-link harmonic. The proposed work is extremely useful to improve the power quality of the power electronic dominated DC grid in consistency. The lifetime of the DC-link capacitor can also be extended.
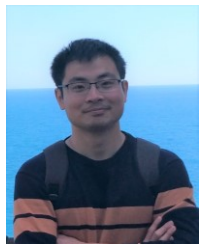
ACKNOWLEDGEMENT

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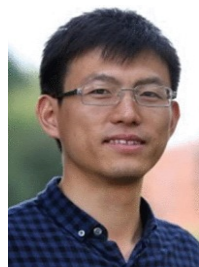
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