UNIVERSITÉ DE MONTRÉAL

UNDERSAMPLING BANDPASS MODULATOR ARCHITECTURES

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DEDICATION

To the memory of my grand parents.

To my parents.

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First and foremost, I would like to thank my research supervisors, Professor Mohamad Sawan and Professor Yvon Savaria who supported me technically and financially through all these years. There was much for me to learn from them, both in and beyond the technical realm.

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I am very grateful to my brother, Ghasem, for his helps and supports during all these years.

It is impossible to find appropriate words with which to thank my parents. This thesis is dedicated to them.

RÉSUMÉ

Cette thèse présente des approches et des techniques de conception pour réaliser un convertisseur analogique à numérique (ADC) pour les récepteurs radiofréquence consacrés aux applications de radio configurable par logiciel. Elle propose des techniques architecturales et de niveau circuit pour réaliser une conception efficace pour une telle application. Les avantages des modulateurs de type sigma delta en comparaison à d'autres types d'ADC sont discutées. Les défis de conception des modulateurs à signaux continus dans le temps sont expliqués pour des fréquences d'entrée de l'ordre de 2GHz. L'approche retenue est également soutenue par une revue de la littérature qui fait le point sur la situation actuelle. On propose un modulateur de type delta sigma basé sur le sous échantillonnage applicable à des fréquences d'entrée aussi élevées que 1.8GHz, une fréquence populaire dans les systèmes de communication sans fil. On montre par simulation que l'approche et les circuits proposés pour la mettre en oeuvre peuvent convertir le signal d'entrée en données numériques avec une gamme dynamique (DR) de 46 dB à une fréquence d'échantillonnage de 810.1 MHz, lorsque la tension d'alimentation est de 1.2V, pour un circuit mis en œuvre avec une technologie CMOS de 0.13μm. Un nouveau modulateur delta (DM) est proposé. Ce circuit conçu pour recevoir un éventail de fréquences d'entrée assez large (2 GHz) a une architecture qui facilite la conception de son filtre passe-bande. Une simulation d'un modèle circuit extrait du dessin des masques réalisé montre un SFDR (Spurious Free Dynamic Range) de 41dB pour une tension d'alimentation de 1.2V. Ce modulateur delta a été fabriqué et des résultats

expérimentaux sont présentés. Ce circuit consomme une puissance totale de 37.2mW mesurée pour une fréquence d'échantillonnage de 500MHz. Un SFDR de 25dB a été mesuré pour une gamme de fréquences d'entrée allant de 500MHz à 2.6GHz quand la largeur de bande du modulateur est ajustée à 1MHz. Le facteur de qualité et la fréquence centrale du filtre actif-RC passe-bande sont réglables et les caractéristiques mesurées de ce filtre sont conformes aux résultats de simulation.

ABSTRACT

This thesis presents design approaches and techniques to realize an analog-digital-converter (ADC) for radio-frequency receivers dedicated to software-defined-radio applications. It proposes architectural and circuit-level techniques to achieve an efficient design for such applications. Advantages of the delta sigma modulators over other types of ADCs are discussed. The design challenges associated with continuous time modulators are explained for input frequencies of the order of 2GHz. A proposed approach to address these challenges is also supported by a literature survey of the state of the art. A novel delta sigma modulator based on undersampling is proposed. It is applicable to input frequencies of the order of 1.8GHz, a popular frequency with wireless telecommunication standards. It is shown by simulations that the proposed design can convert the input signal into digital data with a dynamic range (DR) of 46 dB at a sampling frequency of 810.1 MHz and a low supply voltage of 1.2V using a 0.13μm CMOS technology. This design is then applied into a new delta modulator (DM) to receive a wide range of input frequencies and to reduce the design effort in its bandpass filter block. Post-layout simulation of the proposed DM shows a Spurious Free Dynamic Range (SFDR) of 41dB at a low supply voltage of 1.2V. The delta modulator is fabricated and experimental results are presented. The total power consumption is measured at 37.2mW for a clock frequency of 500MHz. The maximum measured post-silicon SFDR is 25dB for input frequencies ranging from 500MHz to 2.6GHz when the bandwidth of the modulator is set to 1MHz. The Q-factor and the center frequency of the

tunable bandpass active-RC filter were measured and are shown to be in agreement with simulation results.

CONDENSÉ

L'emploi de systèmes électroniques devient de plus en plus répandu dans notre vie quotidienne, pour augmenter notre efficacité dans différentes tâches, et pour améliorer la qualité de vie. De tels systèmes exigent le traitement le plus rapide possible de quantités de données toujours croissantes. Pour cela, des systèmes numériques sont développés pour réaliser de tels objectifs. Cependant, la communication des données entre les différentes parties d'un système exige des systèmes analogiques et mixtes qui devraient être programmables et compatibles avec différentes normes. Aussi, une basse puissance de consommation est essentielle pour les applications portables. Par conséquent, les convertisseurs de données à haute vitesse et basse puissance (convertisseur analogique numérique (CAN) / convertisseur numérique analogique (CNA)) sont nécessaires dans les émetteurs-récepteurs des systèmes de communication et entre les parties analogiques et numériques des systèmes portatifs.

Les radiofréquences présentement utilisées dans les normes de communication sont plus élevées que 1 GHz, alors qu'elles portent une largeur de bande de signal plus étroite que 5 MHz. Afin d'acquérir de tels signaux, la porteuse est habituellement enlevée par au moins un ensemble de mélangeur et de filtre passe-bas, et un CNA est alors employé pour la numérisation. Cette méthode peut être améliorée si le CNA pourrait numériser le signal RF directement avec la même consommation de puissance. L'amélioration est attribuée à l'élimination des composantes analogiques et à

l'implantation d'un système programmable. Notre motivation dans cette recherche est d'explorer diverses idées et de proposer de nouvelles architectures de CAN. La programmabilité des émetteurs-récepteurs peut relier un utilisateur à tous les services de communication disponibles de manière continue, alors que ces services sont offerts à travers différents liens. Bien qu'un tel avantage soit partiellement accessible pour les téléphones cellulaires tri-bandes modernes, il exige du matériel additionnel qui augmente le coût final. De plus, le matériel additionnel est basé sur les normes connues, car l'emploi de nouvelles normes ferait que les vieux téléphones cellulaires ne seraient plus utilisables. Une telle requête pour obtenir toutes les normes possibles, qui était fondamentalement une demande militaire, a été présentée dans les années 90 pour des radios logicielles. La bande primaire de fréquences pour un tel récepteur se situait entre 2 MHz et 2000 MHz – ce qui n'est pas trivial même avec les technologies d'aujourd'hui. Cependant, cela introduit des avantages qui font que ça vaille le coup. De tels récepteurs se composent idéalement d'une antenne, d'un CNA, et d'un processeur de signaux numériques équipé de mémoire. En chargeant le logiciel dans la mémoire du processeur, le récepteur entier pourrait être contrôlé et adapté à une nouvelle norme. Ce logiciel pourrait même être automatiquement téléchargé dans les téléphones des utilisateurs comme une rustine (patch) venant du fournisseur de service. Mais *a priori*, quelques questions doivent être résolues, en commençant par la conception d'un CNA à basse puissance et haute résolution.

Le but de cette recherche est de concevoir et d'implémenter un modulateur delta-sigma (MDS) dédié aux radios logicielles qui pourraient recevoir des signaux à bande

étroite modulant une porteuse atteignant des fréquences qui peuvent excéder 2 GHz. Cette thèse propose des techniques aux niveaux circuit et architecture afin de parvenir à une solution efficace.

Avant de proposer la classe de solutions envisagées, nous discutons de diverses méthodes de conception et des techniques de pointe applicables aux radios logicielles. Les limites des techniques existantes nous amènent à proposer un nouveau modulateur delta-sigma passe-bande à sous-échantillonnage et à temps continu (**Figure 4-1**). L'architecture proposée convient à la numérisation RF, sans mélangeur analogique dans le chemin de rétroaction. Les équations de conception correspondantes sont dérivées et appliquées pour optimiser le point de fonctionnement pour un signal d'entrée de 1.8 GHz. L'architecture fondamentale proposée peut recevoir des porteuses à haute fréquence modulées par des signaux de largeurs de bande aussi grandes que 10 MHz. Nous démontrons que l'architecture proposée peut convertir le signal d'entrée en données numériques avec une plage dynamique sans bruit (Spurious Free Dynamic Range; SFDR) de 46 dB à une fréquence d'échantillonnage de 810.1 MHz en utilisant la technologie CMOS 0.13μm. La consommation de puissance totale a été estimée à moins de 22mW avec une tension d'alimentation de 1.3V. La méthode de conception qui a conduit à ce modulateur peut être appliquée pour développer des modulateurs d'ordre plus élevé qui produiraient un rapport signal à bruit plus élevé. L'adaptation entre les fréquences intermédiaires des côtés numériques et analogiques est effectuée en faisant du sur-échantillonnage du côté numérique. Le modulateur proposé ne présente aucun délai de boucle supplémentaire attribué au réglage du taux d'échantillonnage. Le sur-

échantillonnage augmente le taux d'échantillonnage et la largeur de bande du CNA. Par conséquent, les images à haute fréquence ne seront pas trop atténuées par le CNA. Une telle technique réduit également l'effet des images du signal et améliore le rapport signal à bruit. Le MDS passe-bande proposé offre une performance sensiblement supérieure pour les hautes fréquences lorsqu'il est comparé aux convertisseurs $\Delta\Sigma$ existants dans la littérature.

L'architecture proposée a été validée en utilisant MATLAB (**Figure 4-4**). Quelques circuits ont été proposés et conçus avec la technologie CMOS 0.13μm d'IBM. Les résultats de simulation au niveau circuit confirment également le concept proposé (**Figure 4-8**). Les effets des non-idéalités sont discutés et quelques solutions ont été proposées.

Un des effets reliés à cette architecture est qu'en augmentant la fréquence centrale du modulateur delta-sigma (MDS) à plusieurs GHz, les caractéristiques du filtre passe-bande du chemin direct dans le modulateur delta-sigma ne sont plus pratiques dans la technologie CMOS commerciale, sinon nous devrions avoir recours à des marges de tolérance excessive pour la conception. Compte tenu des considérations pratiques décrites ci-dessus, un modulateur delta à temps continu est proposé (**Figure 5-2**). Ce modulateur fonctionne avec la même performance que le modulateur delta-sigma et il est capable de recevoir des signaux à haute fréquence. En outre, la fréquence centrale n'est pas identique à la fréquence d'entrée de la porteuse, ce qui permet de relaxer les contraintes reliées à sa valeur élevée. Comme discuté plus tôt, le mélangeur dans la boucle de rétroaction et le réglage du filtre passe-bande sont deux limitations importantes des modulateurs delta-

sigma. Nous pouvons gérer les deux en considérant le fait que le but principal du filtre passe-bande est de former le spectre du bruit de quantification. Nous supposons que le signal d'entrée est déjà filtré par un filtre d'anti-recouvrement. Par conséquent, un filtre passe-bande dans le chemin direct ne change pas le spectre du signal d'entrée. Il n'a également aucun effet sur le signal de rétroaction si le gain passe-bande est unitaire. En conséquence, le filtre passe-bande dans le chemin direct peut être déplacé au chemin de rétroaction s'il est centré à la fréquence intermédiaire (FI) au lieu de la fréquence d'entrée. Dans ce cas, nous pouvons enlever le mélangeur ainsi que l'effet de toutes ses imperfections. D'ailleurs, la fréquence du signal d'entrée n'est pas limitée par la fréquence centrale du modulateur delta-sigma.

Le modulateur que nous avons conçu est un modulateur du quatrième-ordre qui a une architecture à double-boucle avec deux filtres passe-bandes de second ordre. Le filtre passe-bande utilisé dans le chemin de rétroaction est un filtre actif-RC de second ordre. Sa fréquence centrale et son facteur de qualité sont ajustables pour obtenir la performance désirée après la fabrication. Par conséquent, une entrée et une sortie sont disponibles pour le réglage pendant les périodes inactives. En outre, le système peut également être accordé en utilisant le signal de sortie du modulateur quand une porteuse de référence est disponible. Un échantillonneur bloqueur à bande ultra-large dans le chemin direct acquiert des signaux avec une fréquence maximale de 2 GHz. Des fréquences plus élevées peuvent également être capturées par cette architecture, mais cela dépend de la technologie et de l'implémentation du circuit. La fréquence d'échantillonnage suit la porteuse d'entrée. Dans ce cas-ci, un taux d'échantillonnage de 495 MHz est nécessaire

pour avoir une FI numérique à 20 MHz. La fréquence de l'horloge est deux fois plus élevée que la fréquence d'échantillonnage. En utilisant un diviseur de fréquence, la fréquence diminue et donc réduit la gigue et réalise un facteur d'utilisation (duty cycle) de 50%. Le quantificateur est un comparateur d'un bit et conduit un tampon (buffer) et un CNA. Les résultats des simulations après les dessins de masques donnent une gamme dynamique de 41dB pour une bande passante de 1 MHz (**Figure 5-11**). Le modulateur a été fabriqué et testé. Il absorbe un courant de 31mA pour une tension d'alimentation de 1.2V (37mW). Le rapport signal à bruit maximal mesuré est de 30dB pour une largeur de bande de 1MHz.

Contributions

Plusieurs contributions ont été apportées par cette recherche et elles sont résumées ci-dessous :

1. Conception d'un modulateur delta-sigma à 1.8GHz. Une nouvelle architecture a été proposée au niveau du schéma fonctionnel et des équations mathématiques ont été développées. Le modulateur a été également conçu au niveau circuit et des résultats de simulation ont été présentés en utilisant la technologie CMOS 0.13μm d'IBM.
2. Conception, fabrication et test d'un modulateur delta à 2GHz. Une nouvelle architecture a été développée basée sur la technique de sous-échantillonnage pour acquérir des signaux d'entrée de 2GHz. L'architecture a été vérifiée en utilisant la technologie CMOS 0.13μm d'IBM et des résultats expérimentaux ont été présentés.
3. Conception, fabrication et test d'un filtre actif-RC passe-bande réglable convenable au modulateur delta.
4. Conception d'un filtre passe-bande réglable RF pour le modulateur delta-sigma.
5. Conception d'un filtre à 2GHz réglable pour l'antirecouvrement.

Conclusion

Dans cette thèse, plusieurs idées originales ont été présentées afin d'aider à améliorer la conception de DSM et de DM dans des récepteurs de radiofréquences. Des contributions ont été apportées au niveau système et circuit. Nous avons proposé

l'utilisation de sur-échantillonnage dans la rétroaction de le modulateur an chapitre 4. Des équations de conception applicables à cette architecture ont été développées aussi bien que des techniques de mise en œuvre au niveau circuit. L'adaptation entre les fréquences intermédiaires des côtés numériques et analogiques est effectuée en faisant du sur-échantillonnage du côté numérique. Le modulateur proposé ne présente aucun délai de boucle supplémentaire attribué au réglage du taux d'échantillonnage. Le sur-échantillonnage augmente le taux d'échantillonnage et la largeur de bande du CNA. Nous démontrons que l'architecture proposée peut convertir le signal d'entrée en données numériques avec une plage dynamique sans bruit (Spurious Free Dynamic Range; SFDR) de 46 dB à une fréquence d'échantillonnage de 810.1 MHz en utilisant la technologie CMOS 0.13μm. La consommation de puissance totale a été estimée à moins de 22mW avec une tension d'alimentation de 1.3V.

Cette approche de conception a été encore développée pour permettre la mise en œuvre d'un nouveau modulateur delta capable de recevoir un éventail de fréquences d'entrée afin de faciliter la conception du bloc de filtre passe-bande. Basé sur l'application présentée au chapitre 2, qui vise la numérisation de signaux RF, nous avons proposé un DM qui utilise le sous échantillonnage. Ce modulateur est réalisé sous la forme d'un schéma fonctionnel ainsi qu'au niveau circuit. Il est conçu pour s'intégrer dans des récepteurs radiofréquences. En utilisant le sous échantillonnage dans le chemin direct, il produit une deuxième fréquence intermédiaire (IF) à 20MHz. Le modulateur delta utilise un filtre passe-bande du 4ième ordre dans le chemin de rétroaction. Ce filtre a une fréquence centrale à 20MHz. Le quantificateur est un comparateur d'un bit qui

conduit un tampon (buffer) et un CNA. Les résultats des simulations après les dessins de masques donnent une gamme dynamique de 41dB pour une bande passante de 1 MHz. Le modulateur a été fabriqué et testé. Il absorbe un courant de 31mA pour une tension d'alimentation de 1.2V. Le rapport signal à bruit maximal mesuré est de 30dB pour une largeur de bande de 1MHz.

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog Digital Converter
ADM	Asynchronous Delta Modulator
APDM	Asynchronous Pulse Delta Modulator
ARWDM	Asynchronous Rectangular Wave Delta Modulator
CIC	Cascaded Integrator-Comb
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
DAC	Digital Analog Converter
DC	Direct Current
DE	Delayed Encoding
DEM	Dynamic-Element-Matching
DFF	D Flip-Flop
DM	Delta Modulator
DR	Dynamic Range
DSM	Delta Sigma Modulator
DSP	Digital Signal Processing
DT	Discrete Time
ECDM	Externally Companded Delta Modulator

ET	Element-Trimming
FET	Field-Effect Transistor
IC	Integrated Circuit
ICDM	Instantaneously Companded Delta Modulator
IF	Intermediate Frequency
LHP	Left-Half-Plane
LNA	Low Noise Amplifier
LO	Local Oscillator
MOS	Metal Oxide Semiconductor
NMOS	MOS transistor having electrons as majority carriers (N-type)
NTF	Noise Transfer Function
OSR	Over Sampling Ratio
PCM	Pulse-Code Modulation
PLL	Phase Locked Loop
PM	Phase Margin
PMOS	MOS transistor having holes as majority carriers (P-type)
PPM	Parts Per Million
RF	Radio Frequency
RHP	Right-Half-Plane
rms	root mean square
S/H	Sample and Hold
SCALE	Syllabically Companded All Logic Encoder

SCDM	Syllabically Companded DM
SFDR	Spurious Free Dynamic Range
SiGe	Silicon Germanium
SMC	Simple Miller Compensation
SNDR	Signal to Noise Distortion Ratio
SNR	Signal to Noise Ratio
STF	Signal Transfer Function
UGBW	Unity Gain Bandwidth
USR	Undersampling Ratio
Vth	Threshold Voltage of a Transistor

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Chapter 1

Introduction

1.1. Motivation

Electronic systems are increasingly being used in our everyday life, to boost our performance in various tasks, and to enhance quality of life. Such systems need to process ever increasing volume of data as fast as possible. Digital implementations are increasingly popular for such purposes. However, communications of data between modules composing such systems are often performed by analog and mixed-mode sub-systems. Ideally, these modules should be programmable and compatible with different communication standards. Furthermore, low power consumption is essential in portable applications. Hence, high speed and low-power data converters are needed in transceivers and portable systems linking analog and digital parts.

The radio frequencies used in communication standards are currently higher than 1 GHz, while they carry a signal bandwidth narrower than 5 MHz. In order to recover such signals, the carrier is usually removed by at least one set of mixers and lowpass filters, and then an ADC is used for digitization. This method can be improved if the ADC could digitize the RF signal directly with the same power consumption. The improvement is due to removing the analog components and having a programmable system. Our motivation for this research is to propose new ADCs for radio frequency

applications. Programmability of the transceivers could allow connecting a user to multiple available communication services seamlessly, even if those services are offered over different links. Although such advantage is partly accessible in modern tri-band cellular phones, it requires additional hardware that increases their final price. Furthermore, introducing new communication standards usually makes old cellular phones unusable if they are based on separate dedicated hardware for each software. The demand to support all possible standards is partly rooted in military requirements, which led in the 1990s to the concept of software defined radios. The primary frequency frame for such a receiver was between 2 MHz to 2000 MHz, which is considerable even with today's technologies. However, its benefits are worthwhile. Such receivers are ideally composed of an antenna, ADC, and then a digital signal processor with memory. By loading software into the memory of the processor, the whole receiver could be controlled and adapted to a new standard. This software may even be automatically downloaded into the users' phones via a patch by the service provider. To make this possible, we first need a low-power and high resolution ADC.

The goal of this research is to design and implement a delta sigma modulator dedicated to software-defined radios that could receive narrow-band signals modulated over carrier frequencies up to 2 GHz. This thesis proposes architectural and circuit-level techniques to achieve this goal. It also validates the proposal with analytical models, circuit simulation, chip layouts and prototype integrated circuits.

1.2. Thesis Organization

Chapter 2 reviews the fundamental concepts in the design of delta sigma modulators. It begins with basic theory and design variations in delta-sigma modulators. We discuss about continuous-time and discrete-time modulators. Then it presents design methods and trade-offs in the delta modulators. The chapter ends by review of receiver's architectures as an application of ΔΣM (delta sigma modulators) and conclusion.

Chapter 3 investigates design issues and factors limiting performance in the undersampling delta sigma modulators. Effect of undersampling in continuous-time modulators are considered in term of noise and aliasing. Such effect is formulated for some existing architectures. The information presented in this chapter is a reference for the work presented in the next chapters.

Chapter 4 describes a new undersampling CT (continuous time) band-pass ΔΣM and its circuit implementation. The proposed architecture is suitable for RF digitization, without an analog mixer in the feedback path. Related design equations are derived and applied to the optimization of its operating point for a 1.8 GHz input signal. Practical issues due to non-idealities are also discussed.

Based on the design trend in the previous chapters, which aims at RF signal digitization, Chapter 5 presents the proposed delta modulator suitable for radio frequency applications dealing with a carrier frequency of the order of 2 GHz. Stability of the modulator is analyzed and associated relations are developed. Simulation and

experimental results are given for IBM 0.13μm CMOS technology. Conclusions and future works are discussed in Chapter 6.

1.3. Contributions

This research makes the following contributions:

1. Design of a 1.8GHz delta sigma modulator[71][75]. A new architecture was proposed at the block diagram level and mathematical relations were developed. The modulator was also designed at the circuit level and simulation results were presented using IBM 0.13μm CMOS technology.
2. Design, fabrication and test of a 2GHz delta modulator[73]. A new design was developed based on the undersampling technique to capture 2GHz input signals. The design was verified by IBM 0.13μm CMOS technology and experimental results were presented.
3. Design, fabrication and test of a tunable bandpass active-RC filter dedicated to the delta modulator [74].
4. Design of a tunable RF bandpass filter for delta sigma modulator [75].
5. Design of a tunable 2 GHz filter for anti-aliasing purposes [72].

Chapter 2

Continuous-Time Delta Sigma Modulators

In this chapter, we review basic theory of the delta sigma modulators. Then we move on to design methods applicable to ΔΣM that cover discrete and continuous time implementations. Then design issues and factors limiting performance in the design of delta sigma modulators and delta modulators are compared and discussed.

2.1. Basic Theory

Delta sigma modulators are a class of circuits that allow quantizing while providing an excellent trade-off between power, speed, and resolution. **Figure 2-1** shows a general form of the modulator and required post-processing to digitize an analog signal.

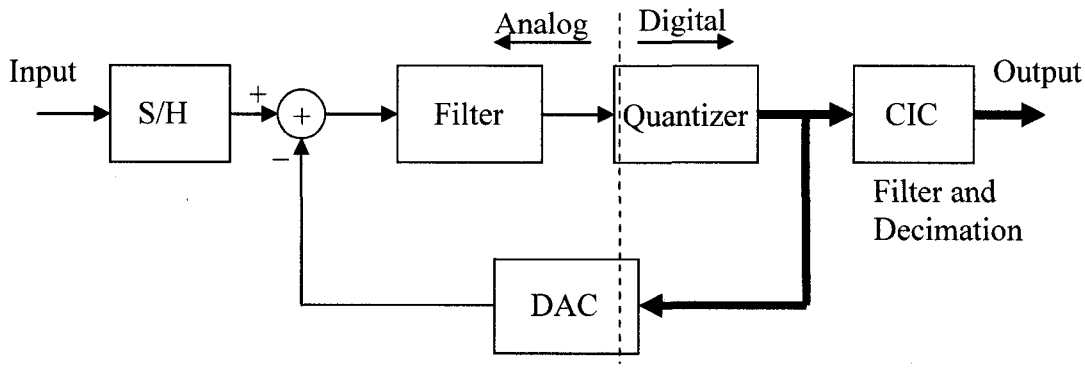


Figure 2-1: Block diagram of a typical delta-sigma ADC.

The input is sampled at a rate higher than Nyquist rate. The quantizer works at the same rate with a low resolution. The output error is fed back and shaped spectrally using the characteristics of the filter. The system, therefore, shapes quantization error and pushes most of its power out of band. The out of band signals are removed using a digital filter, and a pure digital signal remains. Then the data rate is reduced by decimation to reach the Nyquist rate. This is the general form of any delta sigma ADC and all variations are about the modulator section rather than the digital filtering and decimation sections.

Figure 2-2 shows a block diagram of a first order delta sigma modulator where a single-bit ADC is used as the main quantizer.

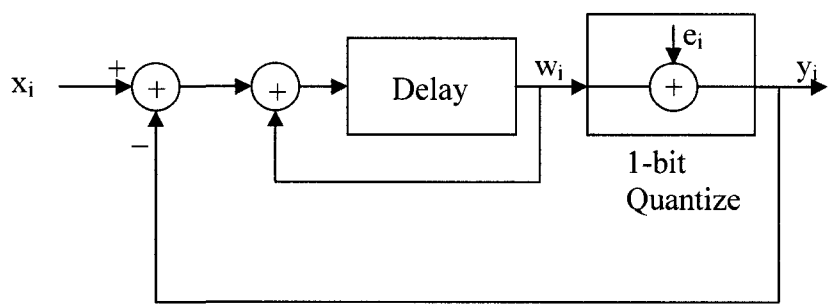


Figure 2-2: Block diagram of a first-order Delta Sigma modulator.

By considering a linear model for the components, a transfer function for input and output of the modulator can be derived as follows [79]:

$$w_i = x_{i-1} - e_{i-1} \qquad (2\text{-}1)$$
$$y_{i-1} = w_{i-1} + e_{i-1}$$

$$y_i = x_{i-1} + e_i - e_{i-1} = x_{i-1} + n_i \qquad (2\text{-}2)$$

$$N(z) = E(z)\left(1 - z^{-1}\right), \quad z = e^{j\omega T} \qquad (2\text{-}3)$$

$$N(\omega) = 2e_{rms}\sqrt{2T}\sin\left(\frac{\omega T}{2}\right) \tag{2-4}$$

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2-5}$$

in which T is the sampling period, Δ is quantization step, and ω = 2πf. The N(ω) is the overall output noise that presents effect of feedback on attenuation of quantization noise as shown in **Figure 2-3**. As a result, there is a part of the signal that can pass through the system with much less noise than the rest of the frequency band.

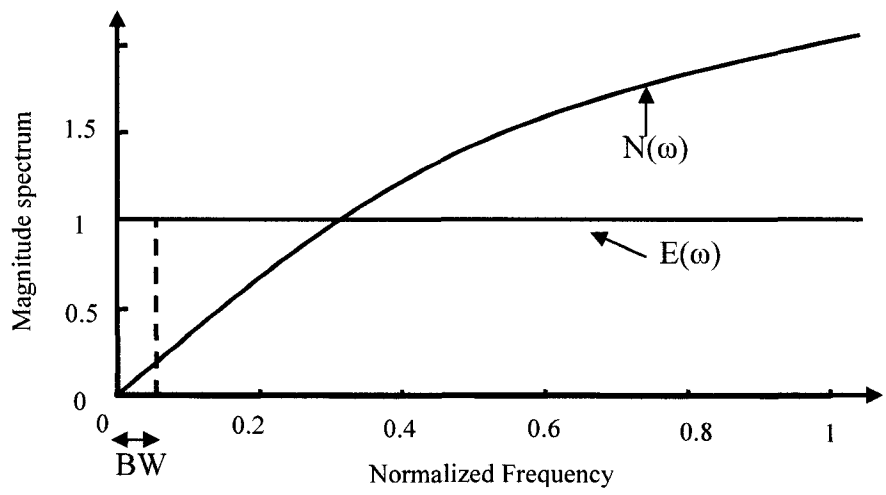


Figure 2-3: Spectral density of noise (N(f)), and quantization noise of 1-bit ADC (E(f)) in a first-order Delta Sigma modulator.

The power of the noise in that bandwidth can be expressed as follows[79]:

$$n^2 = \int_0^{f_0} |N(f)|^2 df \tag{2-6}$$

$$n^2 = e_{rms}^2 \frac{\pi^2}{3} OSR^{-3} \tag{2-7}$$

$$OSR = \frac{1}{2 f_0 T} \tag{2-8}$$

in which f_0 is the signal bandwidth. By increasing OSR the noise power decreases. The above system is a first-order system because it contains a first-order lowpass filter in the loop. The noise power also decreases when a higher order filter is used in the loop. In a system with order L loop, if it is not over-loaded, the rms noise in the signal band is given by [79]:

$$n = e_{rms} \frac{\pi^L}{\sqrt{2L+1}} OSR^{-(L+0.5)} \tag{2-9}$$

And, in a general case, if the loop filter is expressed by H(z), the signal-transfer-function (STF) and noise-transfer-function (NTF) are given as:

$$STF = \frac{H(z)}{1+H(z)} \tag{2-10}$$

$$NTF = \frac{1}{1+H(z)} \tag{2-11}$$

Wherever there is a pole in H(z), the signal passes through the system while quantization noise does not. Therefore, in high order systems, poles are separated over the band of interest to get maximum signal-to-noise ratio (SNR). All the above relations were explained in the discrete-time domain. The system, however, can be implemented in a continuous-time form by using a continuous-time filter. In order to apply discrete-time rules to such a system, an equivalent discrete-time system is obtained using inverse Laplace transform. But matching of the equivalent system with the rules to get high SNR may be somewhat difficult, or needs pure and accurate continuous-time components.

Hence, usually, discrete-time systems have higher performance than continuous-time ones. On the other hand, discrete-time systems are limited to low frequency operation.

As loop filters can also be designed to get a bandpass architecture, we can derive results for bandpass sigma delta modulators that are similar to those obtained for lowpass modulators. This is useful when the input signal is modulated over a carrier frequency much higher than the signal bandwidth. Nevertheless, the sampling frequency must be high enough according to Nyquist theorem. Therefore, when the input carrier frequency is at radio frequency range, such as 1 GHz, in an oversampling architecture, the sampling frequency must be of the order of 4 GHz. Such high operation frequency creates many practical issues, such as power consumption and fabrication cost [32][48][49][27][19][9]. A bandpass system has the following advantages in comparison to a lowpass system [79][53][101][67][33].

A) Band-pass converters are immune to *1/f* noise.

B) Conversion to digital at either Intermediate frequency (IF) or Radio frequency (RF) provides opportunities for dealing with the multiple standards present in commercial broadcasting and telecommunications.

C) There is no need to introduce an extra multiplier and local oscillator to convert RF to base-band.

D) Because of digital nature of the implementation, matching between I and Q channels can be obtained with no special effort.

E) A decimator section is not necessary when conversion rate is not higher than the carrier frequency.

Some advantages in comparison to other video rate ADCs are:

A) Inherent linearity (for single-bit systems).

B) Reduced anti-aliasing filter complexity. They can even be eliminated when it is not necessary to design the filter for a very sharp cut-off.

C) Band-pass converters are immune to *1/f* noise.

D) The smaller structure consumes smaller on-chip area and lower power.

E) Sample-and-Hold can be omitted when a Continuous-Time filter is used.

However, there are some disadvantages in comparison to the lowpass modulators. These are:

A) A typical bandpass (BP) converter consumes larger power than a typical lowpass (LP) one.

B) A 2Nth order BP converter has a SNR as high as an Nth order LP converter.

C) In LP converters, achieving an accuracy as high as 28-bit is feasible, while the best reported BP converters present an accuracy lower than 16-bit for IF < 10MHz and 12-bit for IF > 10MHz.

2.2. Design Variations in Delta-Sigma

Delta sigma modulators are very challenging in terms of having mixed analog and digital parts. In addition, the quantizer is a nonlinear component that makes modeling of the system extremely difficult, especially when the system is using continuous-time RF filters. Hence, practical realization of the system is not a trivial task. We will discuss later in this chapter non-idealities of the implementations and modeling, but here we review useful general design methodologies regardless of circuit level challenges.

As we have already mentioned, there is a significant trade-off between power, and speed/resolution of the quantizer. Processing higher speed signals usually means using higher oversampling-ratio (OSR), and therefore higher power consumption. By having higher resolution in the quantizer, the accuracy improves at the cost of higher power consumption. The accuracy of a modulator can also be increased by increasing the order of the loop filter, which puts more power of the quantization noise out of the signal band. Therefore, we can generally divide design methods to achieve high accuracy into two categories in terms of filter order and resolution of the quantizer; 1-high-order and single-bit, 2- high-order and multi-bit. When we deal with very high accuracy in the modulator, linearity of the conversion is a big concern. A single-bit quantizer is inherently linear and ideally suited for very high accuracy modulators, while a multi-bit quantizer requires a linearization algorithm to fix this issue. The order of the modulator sets the number of system poles. When the modulator order exceeds the second-order, like in any feedback system, instability is expected. Hence, stability is the main issue with high-order

modulators, and linearity is the main problem of a multi-bit quantizer. All design methods are turning around some solutions for such issues. **Figure 2-4** shows some variations of the delta-sigma modulator based on the above discussion.

When the order of the system is higher than two, stability can be obtained, either by controlling the out-of-band noise power or splitting the high-order loop into several low-order loops. In the first method, the out-of-band noise power is controlled by having a few zeros in the transfer function of the system distributed over the signal bandwidth. The new zeros can reduce out-of-band power, and, consequently, stabilize the whole system. In the second method, the high order loop is converted into several low order loops by making multi-feedback or feed-forward ("Distributed feedback/feed-forward"), or by making several single loops in series (Cascade) as shown in **Figure 2-5**, and **Figure 2-6** [29].

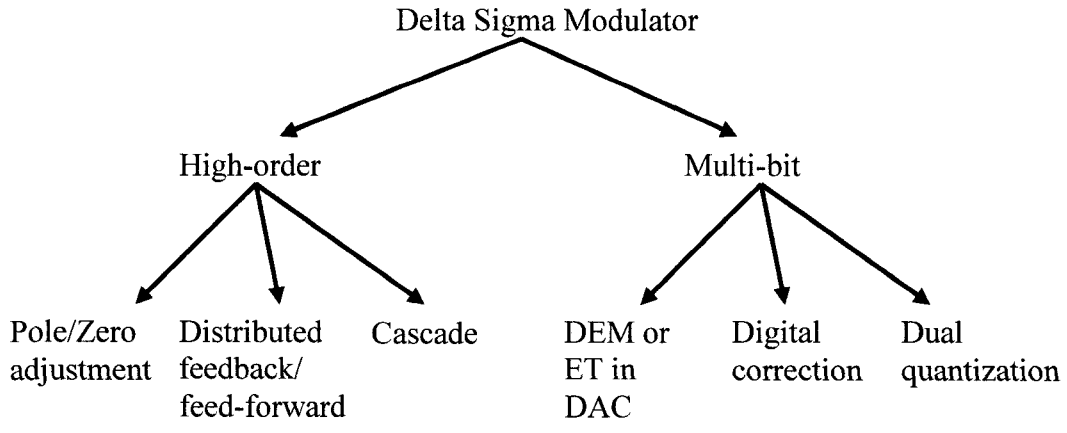


Figure 2-4: Delta sigma modulator variations.

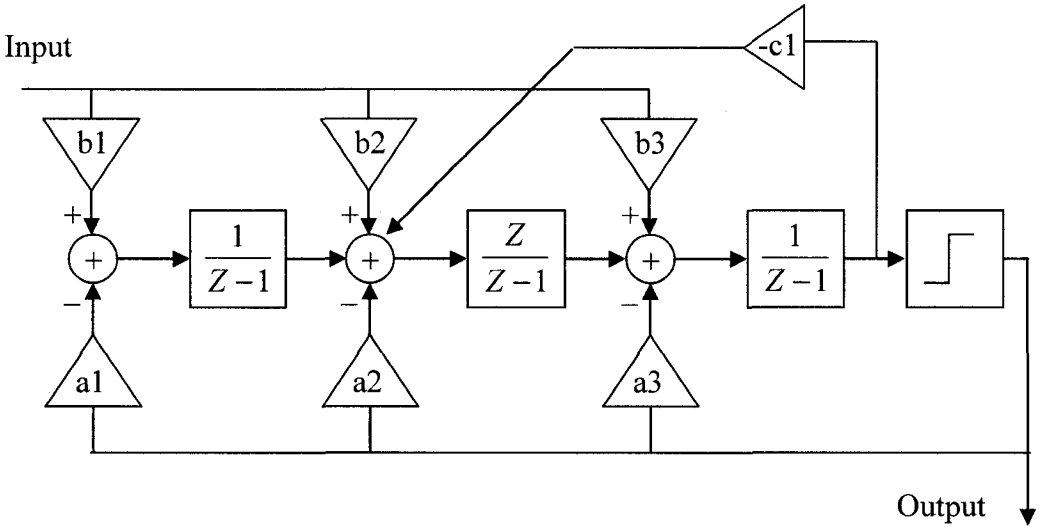


Figure 2-5: A distributed feedback/feed-forward architecture in delta sigma modulator.

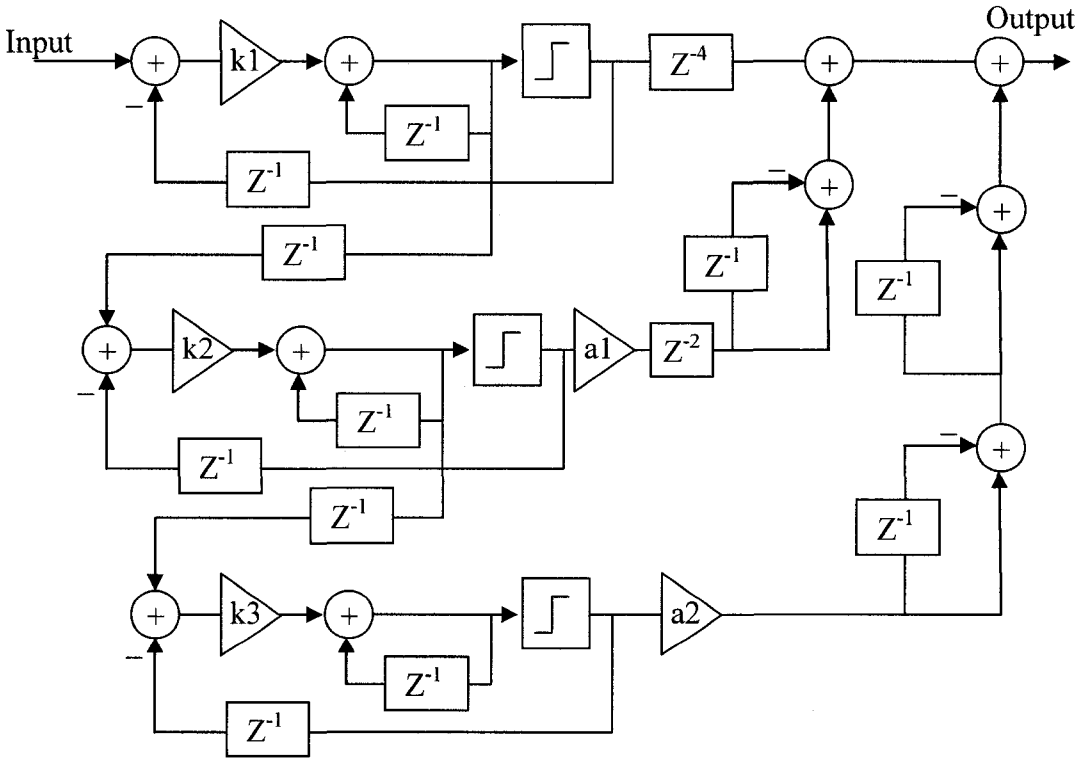


Figure 2-6: A cascade (1-1-1) architecture in delta sigma modulator.

Delta sigma modulators with multi-bit converters are more stable than single bit converters. The converted signal also has much higher SNR in the multi-bit systems. However, a notable limitation is that the output signal in a multi-bit modulator is not as linear as that in the single-bit modulator, while linear conversion is a must in many applications. The mismatches in a practical implementation of a modulator exacerbate nonlinearity issues, and require some solutions in the high level design. In a multi-bit modulator both ADC and DAC are multi-bit. However, the nonlinearity in the DAC makes the whole system nonlinear, and its error and nonlinearity must be less than the ultimate nonlinearity of the modulator. For example, in order to get 16-bit linearity in a modulator, the internal DAC should have accuracy better than 16-bit. This level of accuracy needs an almost perfect element matching that can be obtained by element-trimming (ET) after fabrication, which costs a lot [79], or by some circuit methods in the design step, such as dynamic-element-matching (DEM) [12][11].

Another method to increase the linearity of the multi-bit modulator is post-processing of the data. This correction is carried out by a memory block that contains all possible outputs and is placed after the modulator. Therefore, it can correct all errors by assigning each output to a right value [93]. The last method for improving the linearity is having a single bit DAC, instead of multi-bit, in the feedback, even though the ADC can still quantize signal multi-bit. This reduces the overall SNR and stability in the original multi-bit modulator, but it still has better performance than single-bit and enjoys inherent linearity.

2.3. Continuous-Time vs Discrete-Time Design

A delta sigma modulator is continuous-time when the loop filter is continuous-time. In this case, the system is a mixture of discrete and continuous time parts that make the analysis complex. As most techniques of linearization and stabilization are easier to develop in discrete-time, we can replace an equivalent discrete-time filter in the loop and assume the whole system is discrete-time. There are some tools such as MATLAB [65] which provide such one-to-one discrete-continuous transforms. For example, a first-order loop filter in a discrete-time modulator is mapped to continuous as follows:

$$H(z)=\frac{-z^{-1}}{1-z^{-1}} \Leftrightarrow H(s)=\frac{-1}{s} \tag{2-12}$$

The above technique is the main technique used in the analysis of continuous time modulators. However, there is another option, in which by converting the discrete time part into continuous time, the system is seen to be purely continuous. This method is ostensibly easier, because we need only to replace a quantizer with a delay, and the DAC with a lowpass filter. The quantizer and the DAC are the common parts in all modulators and they are not dependent on the architecture of the loop filter of the modulator. Although a unique transfer function can be obtained in Laplace domain by this method, it is not a linear model due to nonlinear behaviour of the DAC. Therefore, finding the poles and zeros of the system is not trivial, and it requires very sophisticated mathematical tools for nonlinear equations. Hence, it may not be suitable for optimization analysis.

2.4. Delta-Sigma vs Delta Modulator

The main difference between DM and DSM is which one of the filter or quantizer is placed first in the forward path. All basic rules explained in the previous section for the delta sigma modulator (DSM) are also valid for the delta modulator (DM), a variation of oversampling modulators. However, there are a few concerns with the delta modulator and some solutions that make it more suitable for some applications such as voice, adaptive modulators and signal timing measurements [36][99].

Delta modulators were developed mostly based on applications, which were often related to voice or video processing. By improving integrated circuit technology and having more complex filters on the chip, most of the designs were delta sigma modulators. Although the design method and results in DM and DSM are similar, signals at each point of a DM contain different information from those in a DSM. Hence, there are some trade-offs that differ from those explained for DSM. **Figure 2-7** shows a linear DM that is also called an exponential DM.

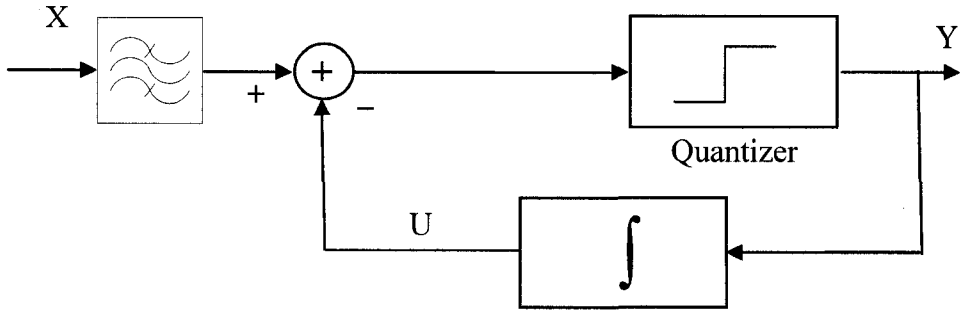


Figure 2-7: Exponential delta modulator.

The signal U shown in **Figure 2-7** is actually a copy input signal, X, reproduced by the system. Therefore, U should always track the input signal with good accuracy. The digital output signal, Y, is the difference between the U and input signal. Hence, the quantizer's steps and rate of quantization are key points in which to have minimum error. In a similar fashion, DSM idling tones appear at the output when the step size in the quantizer is larger than the input amplitude or its variations. This issue is shown in **Figure 2-8**.

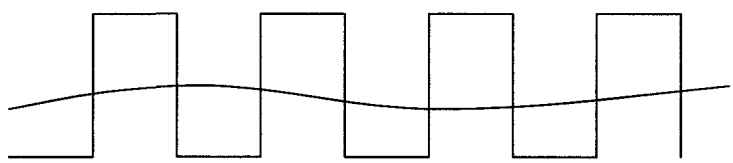


Figure 2-8: Stream of one and zero at the output due to large quantization step.

Having very small quantization steps could also prevent the modulator tracking input signals properly. This issue, which is called slope overload, may occur even when the input signal changes quickly. As shown in **Figure 2-9**, the maximum swing at the output is a variable of the quantization rate and step.

One of the main differences between DM and DSM is position of the filter in the loop, and the issues discussed here are the consequences of such a difference. If a signal is filtered first, and then quantized, the modulator is a DSM. As far as the DM and DSM are used for analog-to-digital-conversion, the output of the modulator is always probed at

the output of the quantizer. Hence, in a DM the filter is seen in the feedback path. However, in some applications like signal timing measurement [41], output of the filter is required as the modulator is not intended for analog to digital conversion.

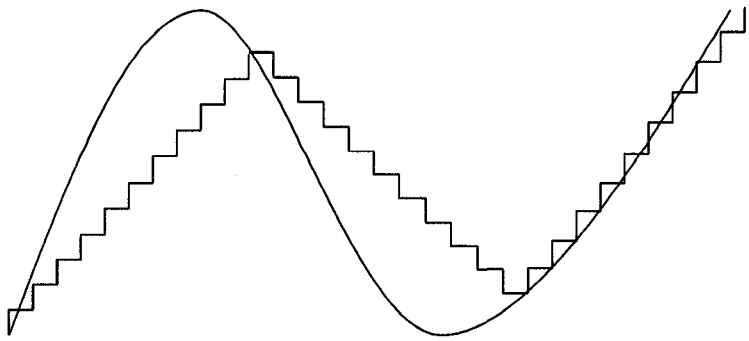


Figure 2-9: Slope overload condition.

Figure 2-10 shows the main variations of DM as a solution for different applications [99]. Asynchronous DMs (ADMs) use a quantizer to digitize the magnitude of the signal without sampling or synchronization with a clock. The output of the modulator is a stream of pulses based on the output of the quantizer. The idle tones, which are due to sampling clock frequency, would not appear in this modulator when there is no sampling block. However, this version is not usable for digitization of an analog signal.

As we discussed, when the digital signal cannot follow the input analog signal, the modulator is overloaded. In order to predict overload conditions, the system may need to know about the future of the signal. If the signal is delayed enough before being entered into the modulator, then the current signal can be used to predict that the overload

condition may appear in the near future and then allow the system to be prepared for that condition. A DM based on this idea is said to use delayed encoding (DE).

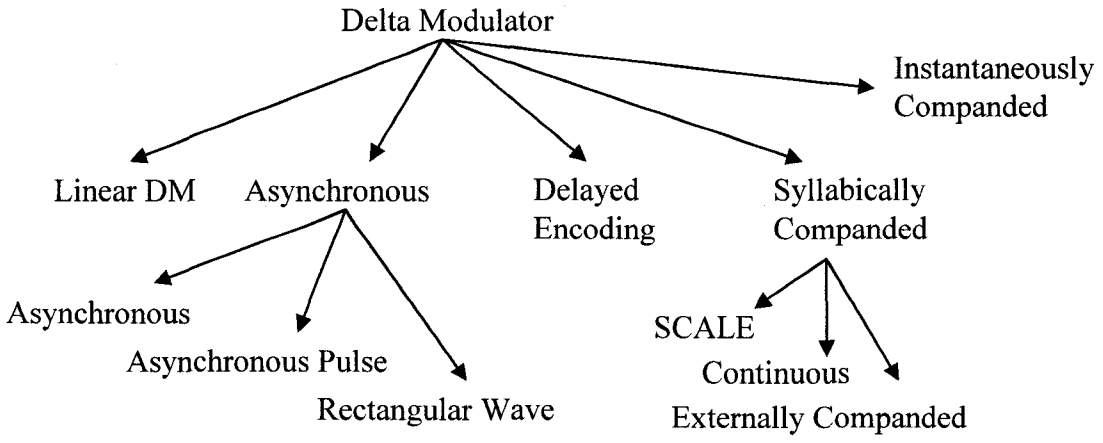


Figure 2-10: Main variations in delta modulator [99].

In all described variations, there is a minimum level for input signal amplitude that produces the maximum SNR in the modulator. The modulator does not have the highest performance for small input amplitudes. One solution to address this issue is to use a compressor and expander in the transmitter and receiver. By compressing the signal prior to the modulator, a large-amplitude signal becomes closer to the smaller one, and the performance of the modulator for the whole range is improved. The combination of a compressor and an expander is called a compander. The distortion introduced by the compressor is removed by the expander after digitization. Another method to mitigate the issue is to adjust automatically the feedback signal amplitude, and to keep the ratio

between them constant. This solution requires less effort and has fewer drawbacks than the use of a compander, (companded delta modulator or SCDM).

Another method to adapt the feedback signal with the input one is to use some recent samples of the modulator output, which needs a short memory to store the samples. This method is known as instantaneously companded delta modulator (ICDM) and in comparison with the linear DM, an ICDM has a DR about 10 dB higher.

All methods to design better delta modulators briefly described in this section are suitable usually for very low frequencies depending on the technology of fabrication. Although design methods in DM and DSM are very similar, the design concerns in the above methods are far from those covered in the previous section. However, there are many other approaches in both system and circuit levels which could ease issues in some applications. In the next chapter, we focus on the issue associated with reaching high input frequencies and the proposed design is presented at system and circuit levels.

2.5. Conclusion

The basic theory of the oversampling modulators was introduced and design variations of the DSM and DM were briefly discussed. We discussed possible applications of the modulators for wireless receivers, where high dynamic range is needed over the bandwidth of the signal. However, with most existing architectures, the mandatory high oversampling-ratio severely limits their application to low frequencies when implemented in CMOS technology. Consequently, undersampling modulators were proposed to enable applications up to multigigahertz frequencies using standard CMOS. Aliasing that is the main issue in undersampling modulators needs to be controlled, as will be discussed in the next chapter.

Chapter 3

Undersampling Delta-Sigma Modulators for Radio Receivers

3.1. Introduction

Advanced communication standards are demanding higher carrier frequencies, while the growing demand for portable devices creates a strong need for low power and low cost devices implementing these standards. This creates a strong need for alternative architectures and design methods. Band-pass delta sigma modulators are ideally suited for wireless receivers, where high dynamic range is needed over the bandwidth of the signal. However, with most existing architectures, the mandatory high oversampling-ratio severely limits their application to low frequencies when implemented in CMOS technology. Undersampling is an alternative to the well-known oversampling approach in delta sigma modulators. It enables applications up to multigigahertz frequencies using standard CMOS technologies by mixing a signal's carrier down to lower IF (Intermediate Frequency) and mitigating imperfections of analog mixers. However, for undersampling to be used successfully, the aliasing it causes should be controlled, which introduces variations into the design.

In this chapter, receiver's architectures as an application of ΔΣM (delta sigma modulators) are introduced. We present an LC bandpass filter as an essential RF block in receivers. Then we move on the main part of the receiver and the design consideration in

undersampling modulators is discussed and advantages and disadvantages of exiting structures are investigated. Noise analyses are presented for existing architectures and accordingly some solutions are proposed.

3.2. Delta Sigma Modulators in Receiver's Architectures

In order to clarify possibilities of ΔΣMs in receiver's architectures, we briefly review existing receiver architectures. In the most common direct-conversion receivers, RF signals are down-converted directly to baseband using a mixer and they are filtered by a low-pass filter. In the case of I/Q modulation, the filtered signal is duplicated into two branches, and mixers driven by sine and cosine quadrature versions of a local oscillator frequency (**Figure 3-1**a) are used to recover the signal. This topology is very cost-effective and requires a small number of analog components. However, DC-offset, Flicker noise, and I/Q mismatches are among the critical issues associated with this architecture [1], [88].

It is of interest that DC-offsets due to the fact that the local oscillator (LO) and input signal have similar frequencies can be eliminated by introducing an intermediate frequency stage in super-heterodyne receivers, as shown in **Figure 3-1**b. In this architecture, after amplification of the input signal by a low noise amplifier (LNA), LO1 can convert the RF signal into an IF in the first stage, and then LO2 can bring that signal into the base band. In contrast to the direct-conversion approach, an image rejection filter

is required on the RF side of the heterodyne receiver. Image rejection and channel filtering quality define the IF parameters or the necessity of using multiple IFs.

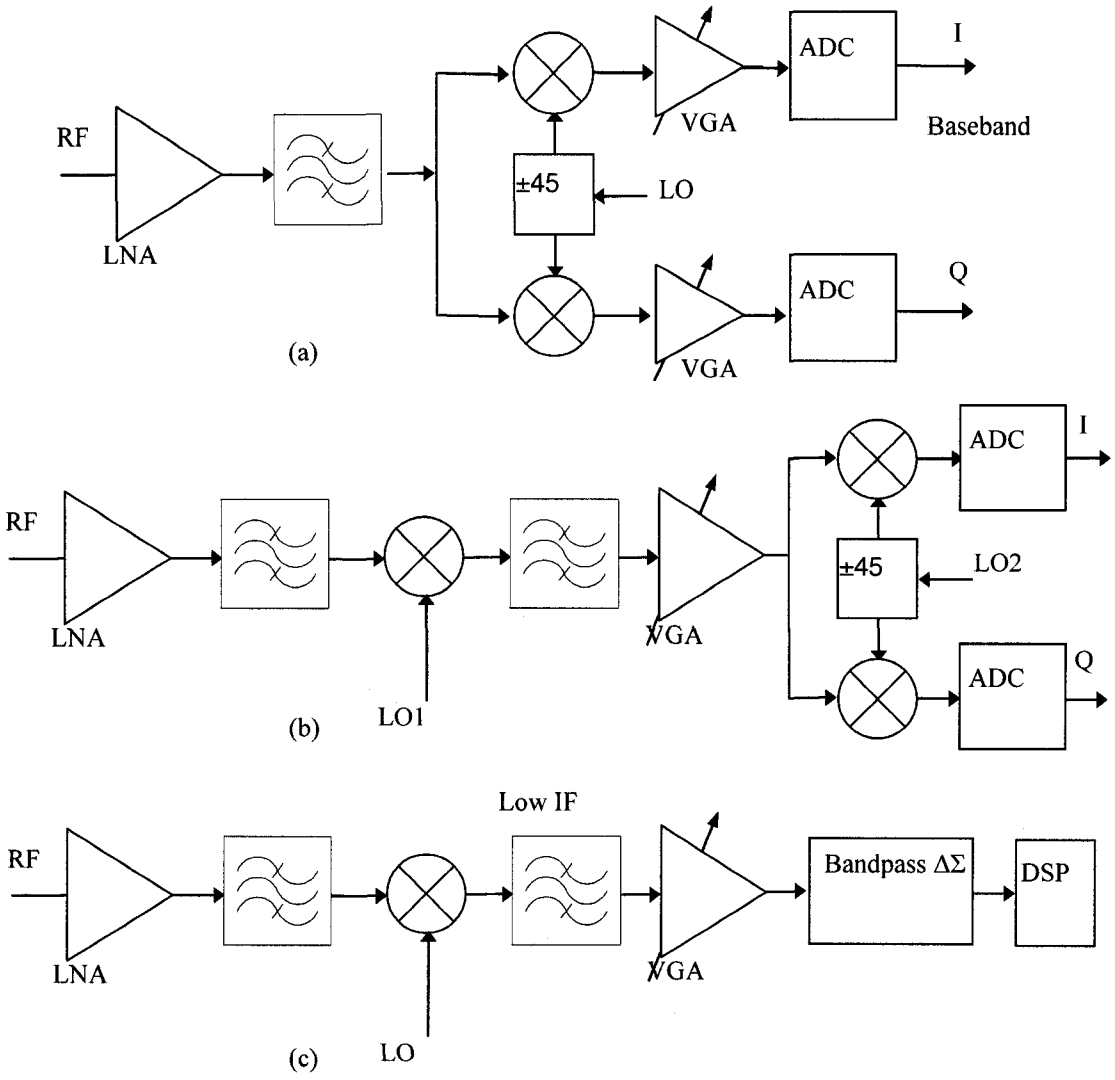


Figure 3-1: Receiver block diagram of (a) Direct conversion, (b) Superheterodyne, (c) Superheterodyne using band-pass delta sigma modulator.

The heterodyne receivers have some known limitations, such as analog mismatches in the I/Q channels, as well as imperfections and parasitics due to the use of

analog off-chip components [89]. As the receiver is implemented by analog components, device mismatches are inevitable. Furthermore, programmability of the receiver is poor, while compatibility with multiple standards in communication systems is highly desired.

An architecture of growing popularity employs an analog to digital converter (ADC) feeding some digital signal processor (DSP), implementing the IF stage that extracts the I/Q channels (**Figure 3-1**c). Hence, demodulation of the signal is no more degraded by analog imperfections [110][110][94]. In theory, extensions to this scheme can even eliminate the analog mixer, and digitize signals directly after the LNA. The feasibility of architectures for which analog-digital conversion is performed directly on the RF signal depends on the conversion speed of ADCs and processing speed of digital signal processors (DSPs).

As current communication standards use carriers at frequencies larger than one gigahertz, direct digitization of a signal at those frequencies is extremely challenging. The challenge increases when considering the typical requirements for low power consumption, high resolution, and large bandwidth. Hence, in most cases, a low IF is still required to relax constraints on the ADC. However, when compared with a classical heterodyne receiver, the second mixer and filtering are often performed on the digital side to improve immunity to analog mismatches.

There is clearly a trade off in adopting a low IF as it imposes high Q-factor in the anti-aliasing filter, but adopting a high IF requires faster ADCs and DSPs. In addition, a Nyquist-rate ADC digitizes very wide bandwidth, which is not necessary when the signals of interest are in fact narrow-band. By contrast, band-pass delta-sigma modulators

are appealing when a narrow-band signal is modulated over an IF carrier. The main limitation for this architecture is the power consumption of the modulator that increases with the frequency of the IF signal [52][106]. Furthermore, the receiver can be enhanced and realized even without an IF stage if an undersampling band-pass ΔΣM is used after the RF filter. The undersampling process works basically as a mixer that converts the RF signal down in frequency to a digitized IF signal. This helps to keep the power dissipation of the ADC relatively low.

3.3. LC Bandpass Filter

An analog RF filter is an essential block in most transceivers and RF bandpass sigma-delta modulators, and its characteristics directly affect the final received signal. On-chip implementation of filters decreases performance in terms of dynamic range, power consumption, and quality factor (Q). Communication systems are, however, demanding fully integrated and programmable transceivers compatible with multiple RF standards. Active implementations of bandpass filters, Gm-C and active-inductors are usually limited to low frequencies and require high power [40]. Q-enhanced LC technique is the most appropriate method adopted by IC designers [26]. A summary of representative published results is given in **Table 3.1**.

Table 3.1: Performance summary of RF filters in the literature.

Reference / *Parameter*	*[26]*	*[63]*	*[70]*	*[54]*	*[6]*
Filter order	2	4	4	2	2
f_O (GHz)	2.1	1.88	1.8	0.9	1.04
Q	20-170	5-20	22.5	45	5-180
Vdd (V)	1.3	2.7	2.7	3	2.7
Power consumption (mW)	5.2	48.6[a]	43.2	39	11.4-15.5
DR (dB)	34	63	42	78	80
Technology	0.35μm CMOS	0.25μm BiCMOS	0.5μm CMOS	Not available	0.35μm CMOS

a Excluding automatic tuning.

Dynamic range and power consumption generally decrease with the supply voltage. However, high Q filters are desired while tuning of Q and center frequency is still an open problem. On-chip automatic tuning using master-slave method has been investigated in [63]. This technique doubles the power and silicon area requirements. On-chip transformers were employed in [63][55] to get a fourth-order LC filter while poles of each stage of the filter never meet each other due to the loading effect of the transformer. Unfortunately the pass-band characteristics are variable unless the coupling factor, k, is as small as 0.005 - 0.04. This choice severely reduces the filter gain and increases noise and distortion due to coupling with bond-wires. Moreover, the coupled inductors must be sufficiently separated to produce low k, which consumes more area. Also, on-chip inductors suffer from high series resistance in CMOS technology and their Q-factor is usually very low. In addition, maximum Q may happen at a frequency higher than

desired. Optimization of Q at operating frequency requires more die area which leads to higher fabrication cost.

In a LC tank, energy is lost due to series resistance of inductor and eddy currents in the substrate. A loss compensation mechanism is necessary to increase the quality of the tank. This can be provided by a negative resistance in series with the inductor's resistance. As shown in **Figure 3-2**, positive feedback by two transistors presents a negative conductance equals to –gm/2. This leads to frequency dependent inductance values [98], but resulting distortion in narrow-band signals is often negligible. Moreover, this negative resistance can be used in many configurations. When positive feedback is used as a negative resistance, large swings become another source of distortion.

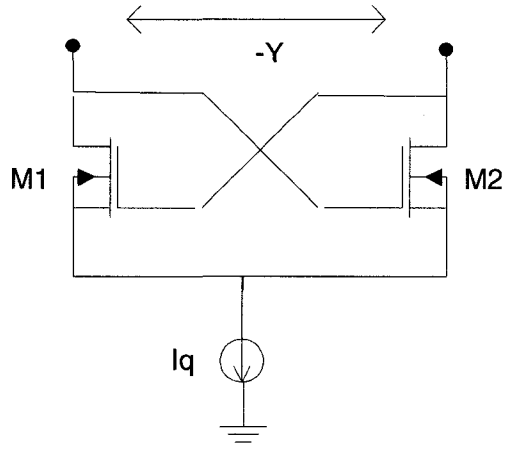


Figure 3-2: Negative conductance (-Y) generator.

If output swing is large enough, the value of such negative resistance varies and provokes distortion. Also, when the DC biasing makes the circuit operation close to Vdd [26], the dynamic range decreases significantly. In the proposed filter, the output DC

voltage is set around Vdd/2. Employing a transformer allows adjusting the output DC voltage with a DC current. Hence, a high dynamic range is expected from a low supply voltage. **Figure 3-3**(a) shows the proposed Q-enhanced LC bandpass filter.

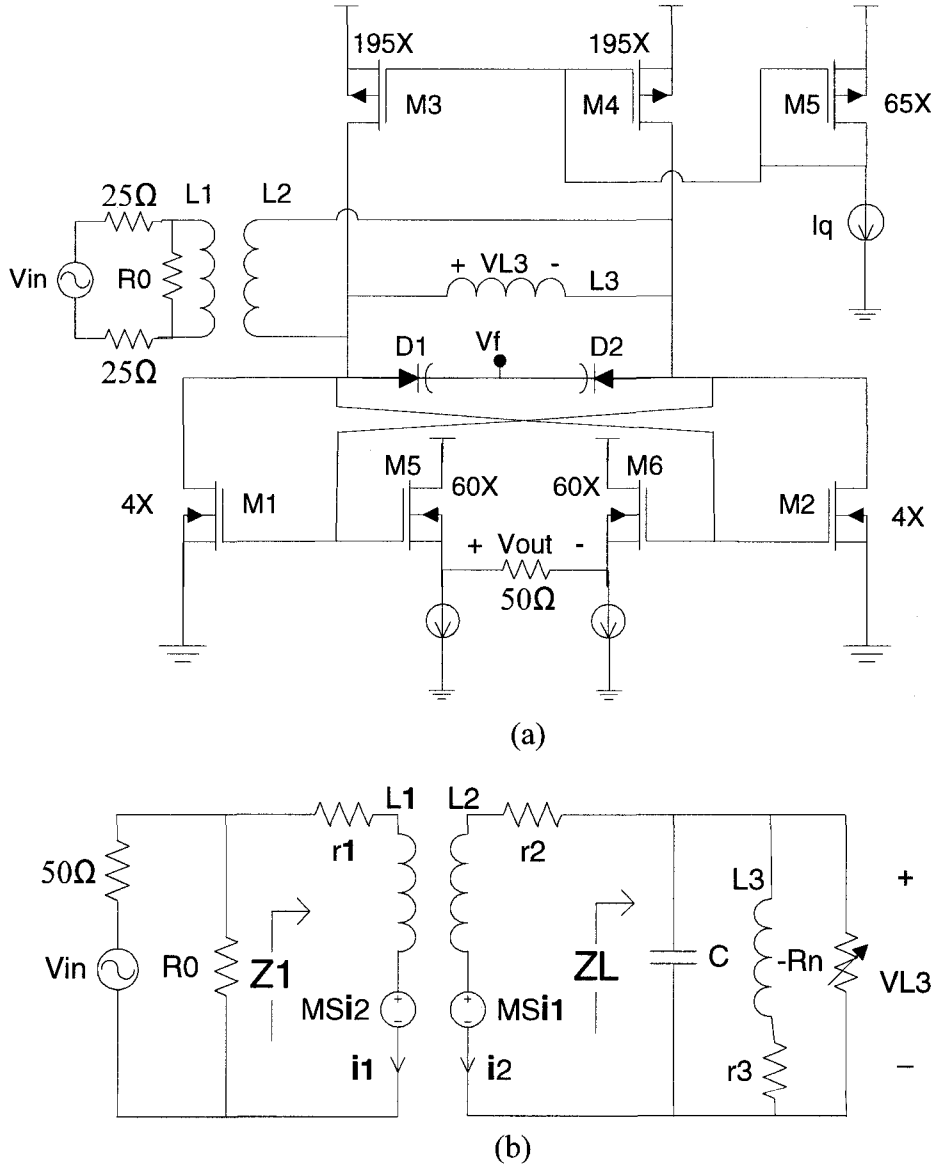


Figure 3-3: Proposed bandpass filter: (a) Circuit implementation. (b) Model of filter.

The input signal is fed to the filter using an on-chip transformer. The filter's center frequency is tuned by changing the varactors' differential capacitance. Negative resistance due to NMOS transistors helps to increase the Q-factor of the filter. DC voltage of output signals is approximately set to Vdd/2 by a DC current, which flows through NMOS transistors (M1 and M2). Output voltage swing increases to maximum possible value at this operating point. While minimum output swing is limited by the system's noise floor, increasing the output swing improves the dynamic range of the filter. The output signal can be buffered to allow driving a 50Ω load using M5 and M6. In our application, no buffer is necessary because an integrated comparator will be driven by this filter when embedded in its target application.

Nevertheless, effects of output matching and buffer transistors were considered in the simulations. High DC currents in most RF circuits are necessary to obtain good linearity. In this filter, the input stage consumes no DC current; consequently, the corresponding power consumption is low. An AC Model of the proposed circuit is shown in **Figure 3-3**(b). Series resistances in the transformer are significant due to on-chip implementation of inductors. Although low-Q varactors decrease the main performances of the filter, parasitics of the inductors are dominant. The transfer function of this filter is derived as:

$$H(s) = \frac{V_{L3}}{V_{in}} = \frac{Ms}{(r_1 + L_1 s) + \frac{(r_1 + L_1 s)(r_2 + L_2 s)}{Z_L} - \frac{M^2 s^2}{Z_L}} \tag{3-1}$$

In which, Z_L is expressed by:

$$Z_L = \frac{1}{Cs - \frac{1}{R_n} + \frac{1}{r_3 + L_3 s}} \tag{3-2}$$

where L1 and L2 are inductances of primary and secondary transformers respectively, M is the mutual inductance between them, and -Rn is the negative resistance due to the positive feedback. Therefore, the transfer function of the filter can be rewritten as:

$$H(s) = \frac{\frac{1}{k_0 k_2}}{L_3 C s^2 + (r_3 C - \frac{L_3}{Rn})s + 1 - \frac{r_3}{Rn} + \frac{k_1}{k_0 k_2}} \tag{3-3}$$

where,

$$k_0 = \frac{(r_1 + L_1 s)(r_2 + L_2 s)}{M^2 s^2} - 1 \tag{3-4}$$

$$k_1 = \frac{(r_1 + L_1 s)}{Ms} \tag{3-5}$$

$$k_2 = \frac{Ms}{(r_3 + L_3 s)} \tag{3-6}$$

By choosing proper values for L_1 and L_2, the transfer function of the filter shows second-order properties. Magnitudes of k_0, k_1 and k_2 converge to constant values at high frequencies. Frequency dependence of series resistances may increase the order of the system in equation (3.3) for frequencies higher than the operating frequency. Center frequency of the filter can be derived as

$$\omega_0^2 = \frac{1 - \frac{r_3}{R_n} + \frac{k_1}{k_0 k_2}}{L_3 C} \tag{3-7}$$

From equation (3.3), a relation between M and the maximum of H(s) can be found by $\partial H / \partial M = 0$, which guides toward a suitable value for the coupling factor of the transformer. Numerical analysis shows the filter has the highest Q at coupling factor, k, equal to 0.45, which can be provided by a compact transformer structure. In addition, weak couplings with other elements are negligible at this value of k. Circuit level simulations also confirm filter gain is the highest at this point. **Figure 3-4** shows a transformer structure, designed with ASITIC [78]. Outer diameter of the primary inductor is 350 μm, and the secondary is laid out inside with a diameter of 240 μm. All inductors use the last layer of metal with 5 μm width. There is also 5 μm distance between lines. A BFMOAT ground plane has been used to obtain a low noise implementation.

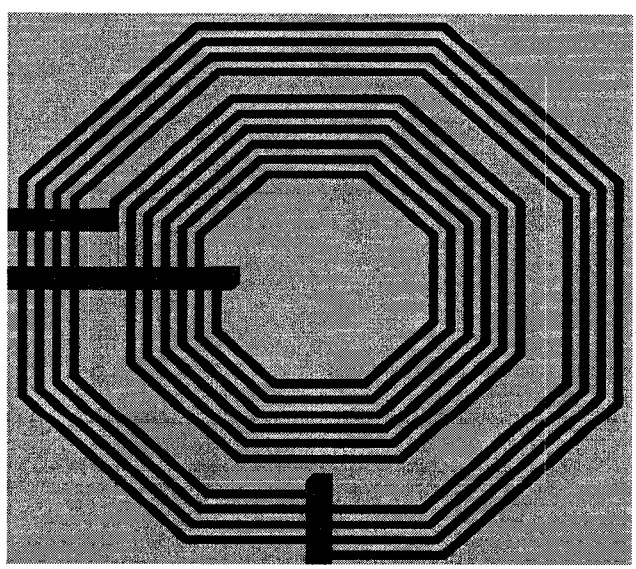


Figure 3-4: On-chip transformer structure.

Input impedance of transformer, Z1, is given by

$$Z_1 = r_1 + L_1 s - \frac{M^2 s^2}{r_2 + L_2 s + Z_L} \tag{3-8}$$

Considering technology and design parameters, its value can be estimated at (-20+j0.2) for narrow-band signals. In order to match input impedance with 50Ω sources and to avoid oscillation, a 14.3Ω-resistor (R0) is employed in parallel with the transformer. It makes input impedance of the filter equal to (50.1+j1.2). IBM CMOS8RF (0.13μm) technology has been used for implementation and post-layout simulation of the bandpass LC filter. Simulated responses of the proposed filter are plotted in **Figure 3-5** using Spectre simulator. It shows that the center frequency of the filter can be tuned over a 144 MHz range, from 1946 MHz to 2090 MHz, with a Q of 100. To obtain such filter characteristics, the control voltage of varactors, Vf, changes from 0.9 V to 1.2 V, and Iq, the bias current, is varied between 100 μA and 150 μA. The input signal has a 1 mV magnitude for this simulation. **Figure 3-6** shows frequency responses when the Q-factor varies up to 150 for a constant center frequency.

The power consumption of the filter is 1.008 mW at Q=81 and 1.7 mW for the buffer. The output power of the filter versus input power is shown in **Figure 3-7** when Q = 100. The 1-dB compression point at the filter's output is -23.54 dBm. Dynamic range of the filter can be estimated by [54]:

$$DR = \frac{P_{1dB} Q_0^2}{4kT(F+1)B_{IF} Q^2} \tag{3-9}$$

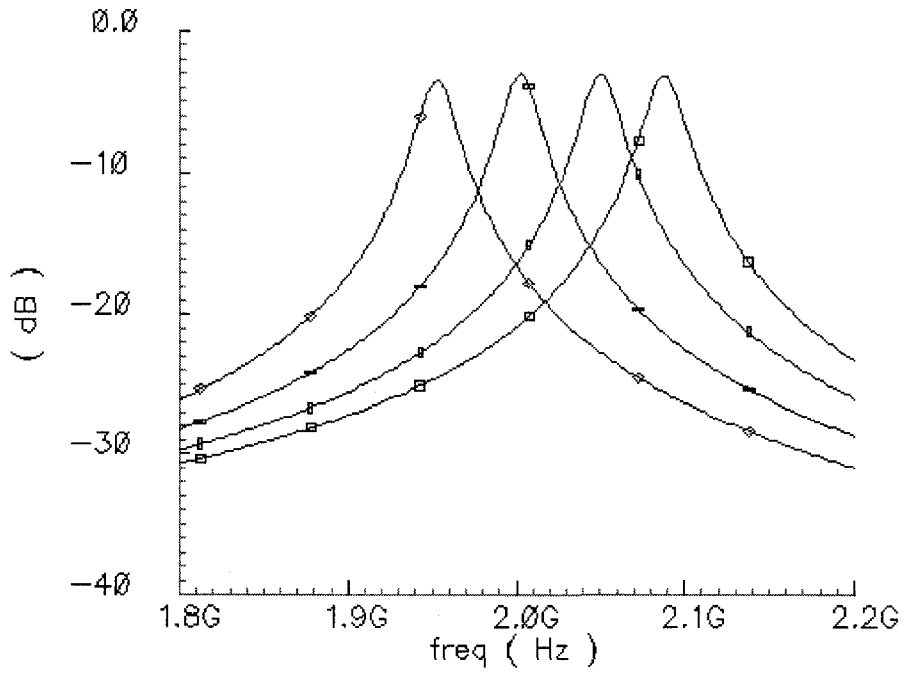


Figure 3-5: Filter responses for different center frequencies when Q=100.

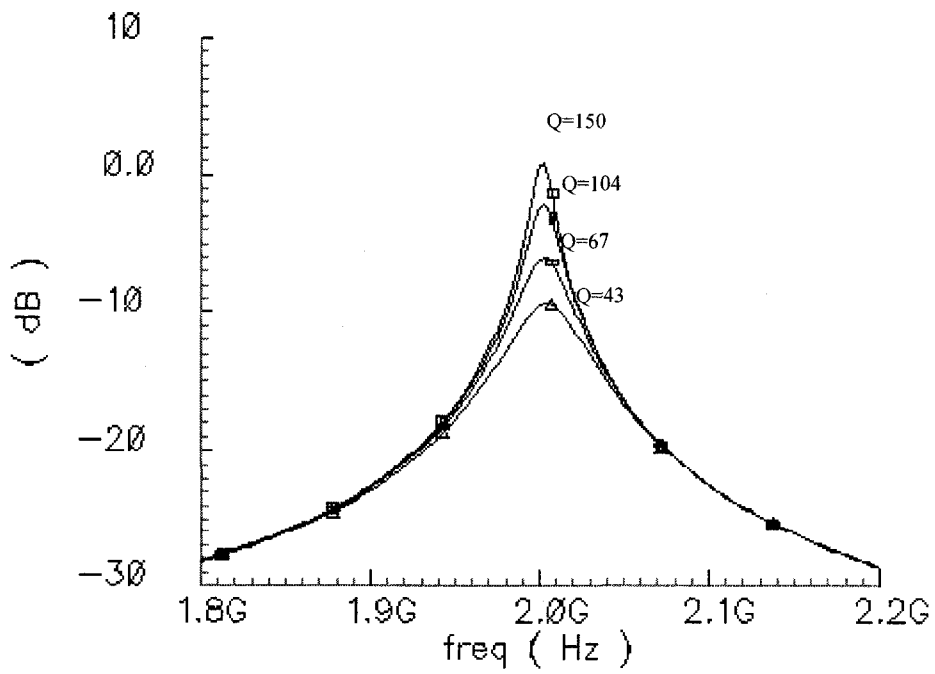


Figure 3-6: Filter responses for various Qs when center frequency is 2 GHz.

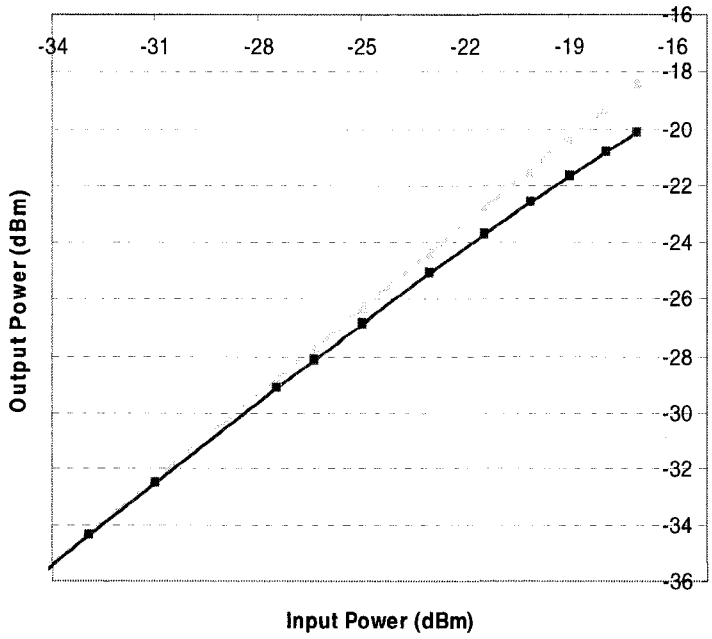


Figure 3-7: One-tone simulation results (solid line) and reference (dash line).

where, Q_0 and Q are resonant circuit quality factor before and after Q-enhancement. *k* is the Boltzman's constant and T is the temperature. B_{IF} is the bandwidth of the signal at baseband and F is the noise factor associated with the negative resistance. Therefore, DR of the filter is 50.1 dB for Q=100, which is comparable with results presented in **Table 3.1**.

3.3.1 Noise Analysis

AC model of the filter is shown in **Figure 3-8**. All transistors are in parallel with the resonator, and therefore one noise source is considered in the model that presents total noises of the transistors.

In a FET transistor, the thermal noise of the channel can be expressed by:

$$\bar{i}_n = \sqrt{\Delta f}\sqrt{\gamma 4kT(g_m + g_{mb} + g_{ds})} \tag{3-10}$$

Where, γ is 2/3 for both long and short channel devices [95]. Assuming the gds is negligible in compare with gm, and that gmb is zero due to a short between the source and the bulk, I_n (shown in **Figure 3-8**) can be derived as:

$$I_n = \sqrt{\Delta f}\sqrt{\gamma 4kT}\left(\sqrt{g_{m1,m2}} + \sqrt{g_{m3,m4}}\right) \tag{3-11}$$

Z1, the impedance of the resonator is given as follows:

$$Msi_2 = -i_1(r_1 + L_1 s + R_0) \rightarrow \frac{i_1}{i_2} = -\frac{Ms}{r_1 + L_1 s + R_0} \tag{3-12}$$

$$V_2 = i_2(r_2 + L_2 s) + Msi_1 \rightarrow \frac{V_2}{i_2} = \frac{(r_2 + L_2 s)(r_1 + R_0 + L_1 s) - M^2 s^2}{r_1 + R_0 + L_1 s} \tag{3-13}$$

$$Y_1 = \frac{1}{Z_1} = \frac{r_1 + R_0 + L_1 s}{(r_2 + L_2 s)(r_1 + R_0 + L_1 s) - M^2 s^2} + Cs + \frac{1}{r_3 + L_3 s} - \frac{g_{m1}}{2} \tag{3-14}$$

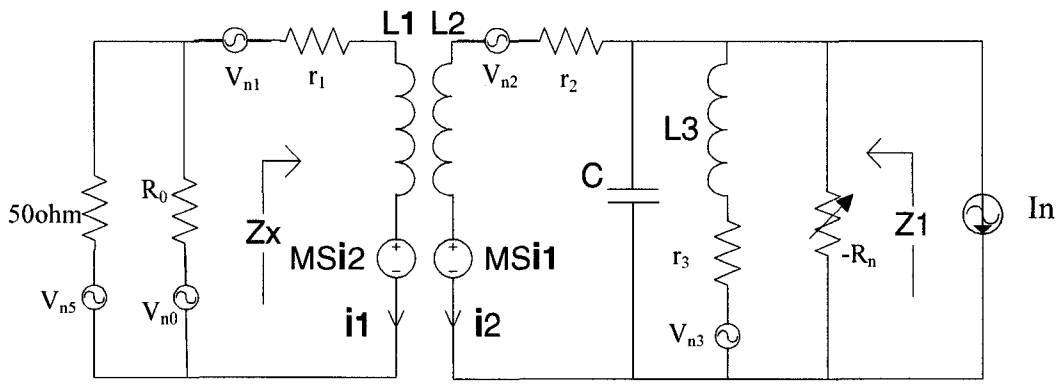


Figure 3-8: AC models of the bandpass LC filters.

Therefore, the thermal noise powers of the transistors appear over the resonator as:

$$V_n^2 = \frac{\gamma 4kT\left(\sqrt{g_{m1,m2}} + \sqrt{g_{m3,m4}}\right)^2}{Y_1^2} \tag{3-15}$$

The resistors in the circuits can also contribute to the final noise power by the following expression:

$$V_n^2 = \Delta f 4kTR \tag{3-16}$$

The Zx shown in **Figure 3-8** is calculated as:

$$Z_X = \frac{(r_1 + L_1 s) + \left[(r_1 + L_1 s)(r_2 + L_2 s) - M^2 s^2\right]\left(Cs + \frac{1}{r_3 + L_3 s} - \frac{1}{R_n}\right)}{1 + (r_2 + L_2 s)\left(Cs + \frac{1}{r_3 + L_3 s} - \frac{1}{R_n}\right)} \tag{3-17}$$

Therefore, recall from equations C-5 and C-6, noise due to R0 and 50-ohm (see **Figure 3-8**) is as follows:

$$V_{n50}^2 = 4kT\left(R_0 \| 50\right)\left[\frac{Z_X}{Z_X + R_0 \| 50}\frac{Ms}{(r_1 + L_1 s) + \frac{(r_1 + L_1 s)(r_2 + L_2 s)}{Z_L} - \frac{M^2 s^2}{Z_L}}\right]^2 \tag{3-18}$$

And the noise of the r1 is estimated as:

$$V_{nr1}^2 = 4kTr_1\left[\frac{R_0 \| 50}{Z_X + R_0 \| 50}\frac{Ms}{(r_1 + L_1 s) + \frac{(r_1 + L_1 s)(r_2 + L_2 s)}{Z_L} - \frac{M^2 s^2}{Z_L}}\right]^2 \tag{3-19}$$

Output noise due to r2 is also given by:

$$V_{nr2}^2 = 4kTr_2\left[\frac{Z_L}{r_2 + L_2 s - \frac{M^2 s^2}{R_0 \| 50 + r_1 + L_1 s} + Z_L}\right]^2 \tag{3-20}$$

And finally output noise due to r3 is expressed by:

$$V_{nr3}^2 = 4kTr_3\frac{1}{\left(1 + (r_3 + L_3 s)\left[\frac{r_1 + R_0 + L_1 s}{(r_2 + L_2 s)(r_1 + R_0 + L_1 s) - M^2 s^2} + Cs - \frac{g_{m1}}{2}\right]\right)^2} \tag{3-21}$$

3.4. Design Consideration

According to Nyquist sampling theorem, for a bandwidth limited signal (BW) with a maximum frequency of f_{max}, the sampling frequency (f_s) must be greater than twice of f_{max} to get a signal without aliasing. This sampling rate is called Nyquist rate. If the signal is sampled at such a rate, it can be reconstructed again with no difference with the original signal. If the sampling rate is even greater than Nyquist rate, then there is an oversampling situation, which is valuable in term of noise power reduction. When the signal is band-limited, the noise is also limited, and consequently by oversampling the limited-power noise is distributed over greater bandwidth (half of the sampling rate), and the level of the noise over the signal bandwidth decreases.

It is of interest when oversampling in sigma delta modulators that the sampling rate must be greater than the signal bandwidth, but not necessarily greater than f_{max}. For instance, when a narrow-band signal (let's say 1 MHz) modulated over a radio frequency carrier (let's say 1 GHz) is sampled by a sampling frequency of 100 MHz there will be no critical aliasing because the sampling rate is still greater than signal bandwidth. There is, however, missing information about the carrier frequency after sampling due to violating Nyquist rate from the standpoint of the carrier. This is called undersampling. In this case, the oversampling ratio (OSR) is defined as $f_s/(2BW)$ while the undersampling ratio (USR) can be defined as f_c/f_s.

When the sampling rate is less than f_c, the carrier frequency can change as follows:

$$Y(t) = Ax(t)\sin(2\pi f_c t + \Theta) \tag{3-22}$$

$$T_s = \frac{1}{f_s} \tag{3-23}$$

$$Y(nT_s) = Ax(nT_s)\sin(2\pi f_c nT_s + \Theta) \tag{3-24}$$

$$\underline{Y(n) = Ax(n)\sin(2\pi n USR + \Theta)} \tag{3-25}$$

$$Y(n) = \begin{cases} Ax(n)\sin(\Theta) & if \quad USR = m \in \mathrm{Z} \\ Ax(n)\sin(\Theta)(-1)^m & if \quad 2USR = m \in \mathrm{Z} \end{cases} \tag{3-26}$$

It should be noted that undersampling may cause aliasing when there are many signal channels available at the input. The other point is that undersampling increases the in-band noise power, even if the input is clean of those interference signals.

There are two types of implementation for undersampling ΔΣMs; Discrete-time (DT) and Continuous-time (CT). DT implementations are usually suitable for IF lower than 80 MHz with a resolution higher than 10 bits [16], while CT implementations can handle signals with carrier frequencies up to multigigahertz, but they produce a low resolution. The DT modulators have a sample and hold (S/H) at the front-end. This module plays a role similar to an analog mixer. Its characteristics must at least match the overall performance of the converter. Therefore, from an architectural perspective, the advantage of using undersampling DT modulators is due to the advantages of ΔΣMs and not so much to the removal of analog components. In fact, one design goal in CT modulators is to combine, spectrally shape, and attenuate the imperfections of undersampling S/H with quantization noise. **Figure 3-9** shows a common architecture used for undersampling DT modulators. Using undersampling, the S/H down converts the

IF to the baseband to make the signal suitable for a low-pass modulator [16]. Band-pass modulators can also be used in such an architecture by using different sampling rates. A complex band-pass ΔΣM is more efficient than a real one [47]. Therefore, Coppejans et al. suggested the use of a complex band-pass modulator in the I/Q channels [22], to get a dynamic range (DR) as high as 62dB. A DR up to 92 dB is also achievable using a 24 dB programmable gain in the receiver [37].

Band-pass modulators based on a similar architecture, but with higher IF were investigated. For instance, designs reported in [90] convert signal frequencies of 60 MHz and 100 MHz to a second IF of 20 MHz using a sampling frequency of 80 MHz [90]. The main reason mentioned for limiting the IF to 20 MHz in these works is the discrete-time implementation of loop filter in the ΔΣM. The center frequencies of the discrete-time filters are highly sensitive to the DC gain of the amplifiers, which may introduce distortion when the IF increases. As a design technique, any discrete-time band-pass filter of order N can be split into N parallel low-pass filters, with each filter working at a frequency N times lower than the sampling frequency as shown in **Figure 3-10**. Therefore, a band-pass filter can be implemented using low-pass filters, which are easier to design. This technique extends to the design of discrete-time band-pass filters with high center frequencies. However, mismatches among the parallel low-pass filters are a main source of errors and distortions. To alleviate these effects, a digital calibration technique was proposed [21]. By reducing mismatches, 10 to 15 dB improvement in the overall signal to noise distortion ratio (SNDR) was reported [21]. When a sampler is placed at the front end of a ΔΣM, the distortion due to the sampler may be considerable.

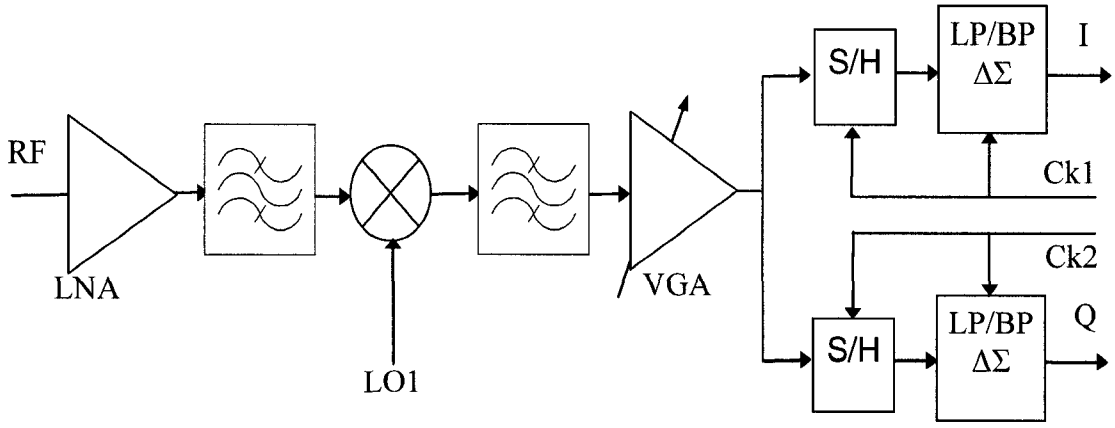


Figure 3-9: Receiver architecture using undersampling in S/H and low-pass/band-pass ΔΣ modulator.

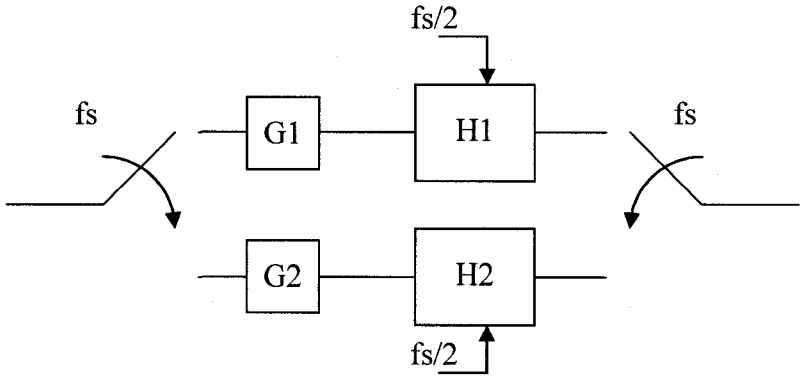


Figure 3-10: Two-path implementation of the filter.

This distortion is attenuated by increasing the W/L ratio of the switches. However, increasing the switch size makes other nonlinear parameters of the transistors significant [76]. If the signal can be sampled in the loop, the distortion is attenuated due to feedback. In [76][15] the sampler is entered into the modulator loop, which could

down-convert the IF signal to the baseband by undersampling, as shown in **Figure 3-11**a. In this method, the loop filter is a low pass and the frequency of the sampler is the same as the clock of the quantizer and the loop filter.

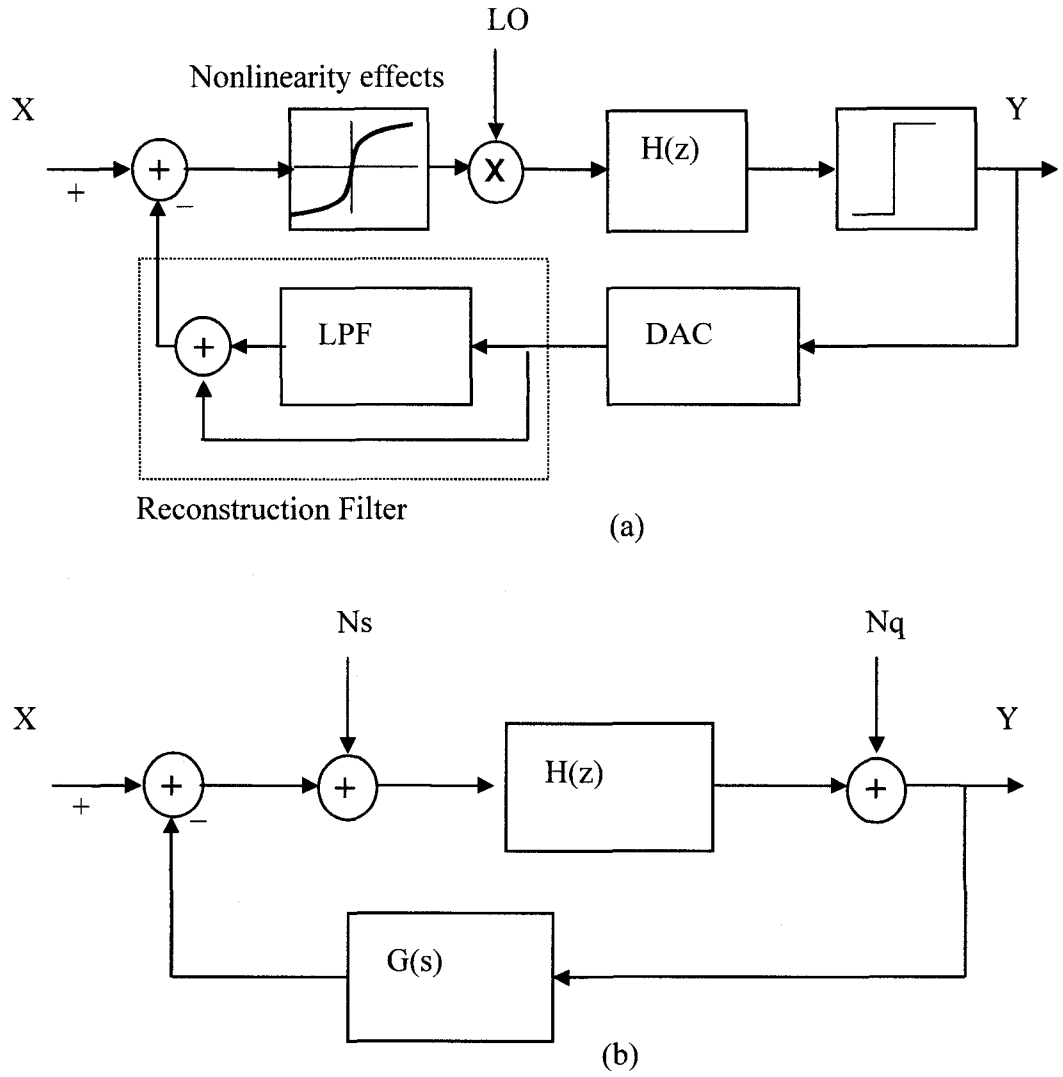


Figure 3-11: Undersampling delta sigma modulator using sampling in the loop: a) architecture, b) modeling.

Another architecture which uses undersampling to capture high frequency signals is shown in **Figure 3-12**, which is basically a delta modulator. This design is suggested in [41] for application of signal timing measurement. The input signal frequency, which can be as high as 1GHz, is down converted to DC, and integrator output signal can continuously track input signal. However, design aim in this approach was rise/fall time measurement and was not used for data conversion.

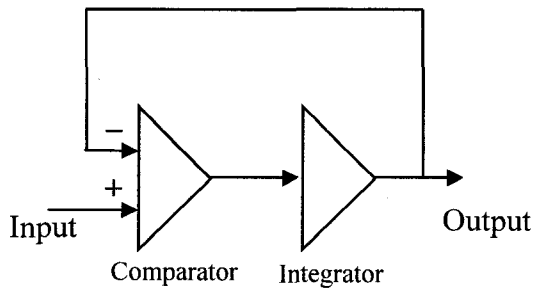


Figure 3-12: Delta modulator for signal timing measurement [41].

3.5. Noise Analysis

Because of undersampling, there is aliasing in the sampler used in **Figure 3-11**, which increases noise level. There is also some distortion due to nonlinearity of the sampler. The feedback path attenuates the distortion by a factor of (1+A*f*), in which A and *f* are the forward and feedback gains respectively. However, sampling noise is added to the input signal and is not shaped spectrally as a quantization noise, because it is entered into the system before the loop filter. By modeling a ΔΣM with a sampling inside of the loop as shown in **Figure 3-11**b, we derive the output signal as:

$$Y = \frac{H}{1+GH}X + \frac{H}{1+GH}N_S + \frac{1}{1+GH}N_q \tag{3-27}$$

where *Ns* and *Nq* are sampling and quantization noises respectively. The undersampling ratio (USR), which is the ratio of input carrier frequency to sampling frequency, is expressed by:

$$USR = \frac{f_C}{f_S} \tag{3-28}$$

The undersampling folds input noise floor (N_i) and output noise floor (N_q/(1+H)) into the signal bandwidth by a USR times factor. This led us to express the sampling noise as:

$$N_S \approx USR.N_i + \frac{N_q}{1+H}\sum_{n=1}^{SSR}\left|G(j\omega_S.n)\right| \tag{3-29}$$

where $\omega_s=2\pi f_s$. This expression neglects the noise introduced by other circuits such as the subtractor and the S/H, as well as images at frequencies higher than f_c. From

equations (3-27) and (3-29), we conclude that by increasing the USR, the sampling noise increases and that this noise cannot be canceled by the modulator. Furthermore, by increasing the USR, the number of signal images at the input increases, which sets a requirement for an anti-aliasing filter with a higher Q-factor on the RF side. Otherwise, distortion due to signal images increases.

Now, let us compare the above DT architecture with a CT architecture where the S/H is placed after the loop filter and before the quantizer. In this case, both errors due to the distortion and sampling noise will be attenuated by the modulator, and the distortion due to the nonlinearity of the S/H will remain low like before. This method requires that the loop filter be implemented as a continuous-time band-pass filter. This alleviates the stringent requirements on the S/H, especially when a 1-bit quantizer is used. Another advantage is that, unlike DT filters, CT filters are not limited to low center frequencies. However, because of undersampling, the digital-side IF is less than the analog-side IF, and the 1-bit DAC (a zero-order holder which is clocked at a frequency lower than the analog IF) in the feedback loop severely attenuates the high frequency replicas of the output signal. Hence, the system fails to operate properly.

As a solution, a CT ΔΣM that uses a mixer in the feedback loop, for up-conversion of the main replica of the digital signal to the analog IF (**Figure 3-13**), was proposed by [36]. Functionality of this approach for an IF as high as 195 MHz was later investigated by several authors [43]. Assuming the Q-factor of the loop filter is infinite, it was concluded that a $\pi/4$ phase difference between modulation frequency (f_M) and quantization frequency is necessary to have the highest SNR in the output signal [44].

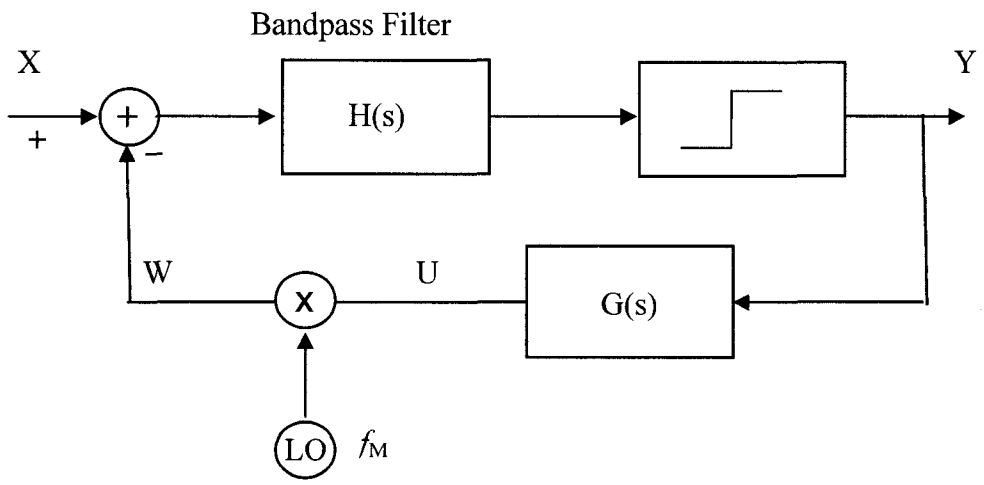


Figure 3-13: A continuous-time undersampling bandpass modulator [36].

We will demonstrate in the next chapter that when considering finite Q-factor, the loop filter transfers some distortion due to the mixer into the output, and consequently the output signal-to-noise plus distortion ratio (SNDR) decreases. Indeed, the analog mixer is the main source of noise and non-linearity when a high SNDR is required. By considering excess loop delay and phase error between the modulation and quantization frequencies, imperfections increase when signals in the gigahertz range are converted.

We can conclude that in both described techniques, gigahertz signals can be captured with a relatively low SNDR. In the DT method, the errors are mainly due to the high USR and the signal images, while in the CT method errors are due to the mixer and the CT loop filter. Another significant issue when we design a CT modulator is linked to the fact that CT filters with a low Q-factor do not attenuate the signal images sufficiently. Hence, a high-order band-pass filter may be required. Chen et al suggest using a second-order CT band-pass filter, followed by a S/H and a 4th-order discrete-time band-pass filter

[17] as shown in **Figure 3-14**. As we have already described, sources of errors are different in the CT and DT methods, and each of these sources would partly contribute to the overall error in such a hybrid design.

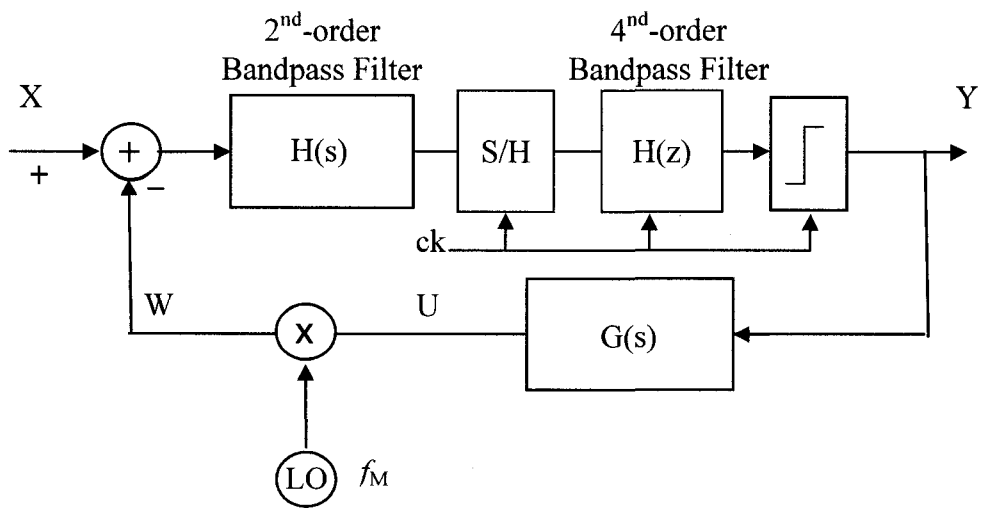


Figure 3-14: Block diagram of an undersampling modulator with a mixed continuous and discrete-time filter [17].

3.6. High Frequency Modulators

Table 3.2 presents performance summery of some high frequency modulators. In CMOS technology, we can see by increasing the center frequency from 70MHz to 1GHz the output SNDR reduces from 72dB to 38dB. In general, by decreasing the supply voltages, the SNDR also decreases. Power consumption is also considerable due to high sampling rate except in [10], which is using a superconductor technology.

Table 3.2: Performance summary of high frequency modulators in the literature.

Parameter	**[106]**	**[20]**	**[10]**	**[23]**	**[103]**	**[7]**
Center freq.	210 MHz	1 GHz	2.23 GHz	1 GHz	100MHz	70 MHz
BW (MHz)	1	20	20.8	0.5	0.1	4.4
Sampling rate	4 G	4 G	42.6 G	4 G	400 M	280 M
SNDR (dB)	78	40	49	38	54	72
Power (W)	3.2	0.45	1.9m	0.29	0.33	0.48
Vdd (V)	+/-5	5	-	1.8	2.7/3.3	3.3
Technology	AlInAs-GaInAs	0.5um SiGe	Josephson Junctions at T=4.2°K	0.18um CMOS	0.35um CMOS	0.35um CMOS

Figure 3-15 shows block diagram proposed in [20] to receive input frequencies as high as 1 GHz. The modulator is a 4th-order continuous-time and designed for wide

bandwidth up to 20 MHz. However, the used design procedure assumes an unjittered sampling clock, which may be important at such high speed.

Figure 3-16 shows block diagram of a complex frequency translation method. The input frequency is down-converted using mixers in the loop. Those mixers can be merged into sample-and hold in circuit level. Therefore, the inner delta sigma modulators should be discrete-time. As input frequency increases the operating frequency of such DT DSMs increases and consequently its realization is not trivial.

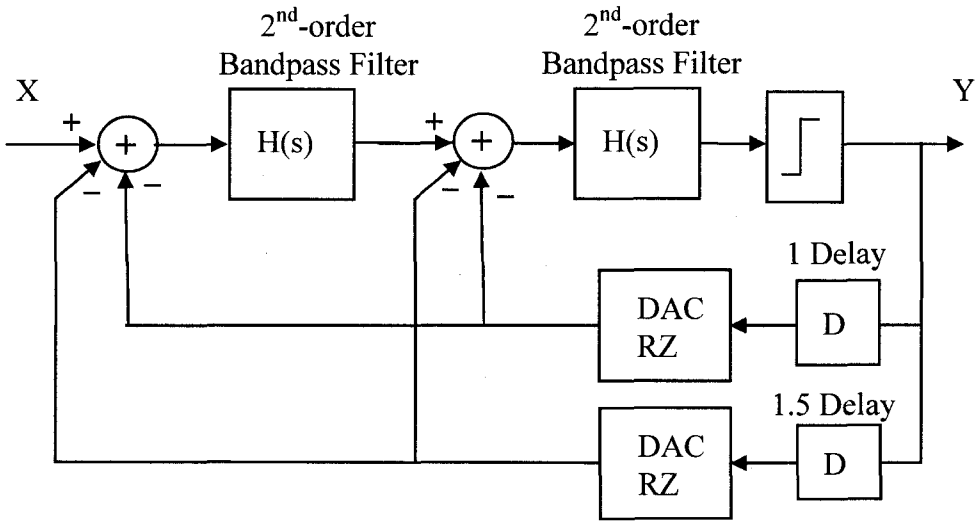


Figure 3-15: Block diagram of a multi-feedback modulator [20].

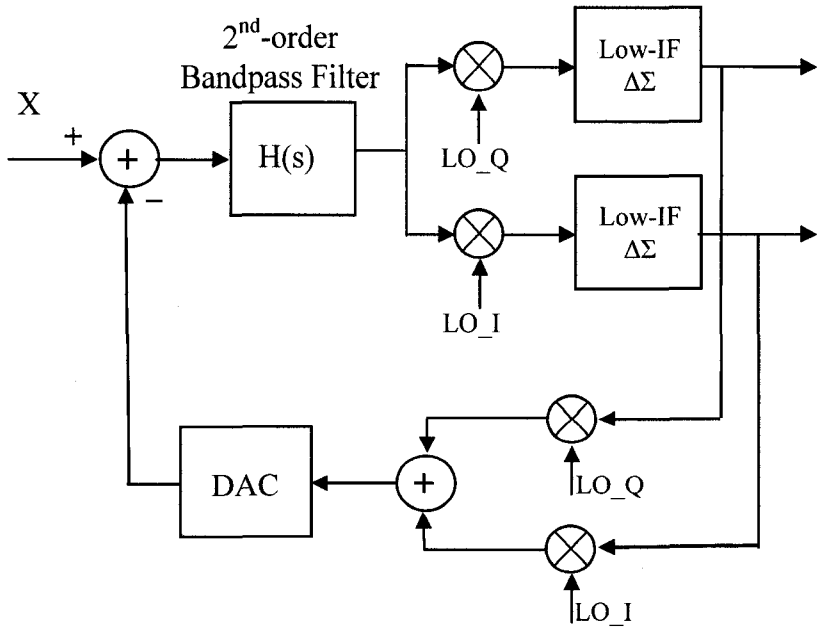


Figure 3-16: Block diagram of a complex frequency translation [103].

3.7. Conclusion

Current receiver's architectures were explained and position of the delta sigma modulators in those architectures was clarified. An RF bandpass filter was presented as an essential block in the receivers. Design methods and trade-offs in design of undersampling modulators were discussed. Design considerations in discrete-time and continuous-time modulators were presented. Discrete-time modulators are suitable for high resolution and input frequencies below 100MHz. While, continuous-time

modulators are more suitable for high frequency input signals with low resolutions. If the discrete-time modulators be designed for high frequency input signals, their output SNR may be as low as the continuous-time one. In the discrete-time method, the errors are mainly due to the high USR and the signal images, while in the continuous-time method errors are due to the mixer and the continuous-time loop filter. High Q-factor and high-order filters can increase the SNR in the continuous-time modulators.

Chapter 4

A Novel Continuous-Time Delta Sigma Modulator

4.1. Introduction

In the last chapter, we discussed about the various design methods and the state of the art. Moreover, the main problems of those methods in the application of SDR were introduced and based on identified problems, the framework of this research was defined. In this chapter, we propose a new undersampling CT (continuous time) band-pass ΔΣM and its circuit implementation. The proposed architecture is suitable for RF digitization, without an analog mixer in the feedback path. Related design equations are derived and applied to the optimization of its operating point for a 1.8 GHz input signal. The underlying proposed architecture can receive signals of bandwidth as large as 10 MHz modulated over high frequency carriers. It will be shown that the proposed design can convert an input signal into digital data with a SFDR of 46 dB at a sampling frequency of 810.1 MHz using a 0.13μm CMOS technology. The proposed band-pass ΔΣM offers significantly better performance at high frequencies when compared to all previously reported ΔΣ converters. Practical issues due to non-idealities will also be discussed.

4.2. Proposed Bandpass Delta Sigma Modulator Based on Undersampling

As discussed earlier in section 3.5, the zero-order-hold (ZOH) effect in a DAC is a low-pass filter with a bandwidth less than the input frequency of the modulator, and depends on the sampling frequency of the quantizer. This low-pass filter attenuates all replicas of the digital-side IF. However, as will be proposed, if the sampling rate increases using up-sampling, the bandwidth of the low-pass filter increases as well. Therefore, it is possible to use one replica of the output signal centered at the analog IF, as a feedback for the system. In our proposal, additional samples with a value of zero are placed between the real samples, which increase the bandwidth of the DAC (ZOH) as follows:

$$H_0(s) = \frac{m}{sT_S}\left(1 - e^{-s\frac{T_S}{m}}\right) \tag{4-1}$$

where m is the up-sampling ratio and T_s is the sampling period in the quantizer. **Figure 4-1** shows the proposed ΔΣM using up-sampling in the feedback path. The idea here is to omit the analog mixer and up-conversion block in the feedback path that is found in existing designs ([36], **Figure 3-13**), and use of a high-frequency replica of the digital output signal. In addition, the delays due to the quantizer, the up-sampling and the DAC are exploited to obtain the desired negative feedback. Unlike the conventional architecture, the feedback signal is added to the input signal as the negative feedback is produced by controlled delays. The delay in the up-sampling branch depends on its implementation. If all new samples are placed before the real sample, the introduced

delay will have a maximum value. The process of up-sampling with a ratio of m can be modeled as:

$$H_{up}(s) = e^{-s\frac{T_S}{m}n_o} \tag{4-2}$$

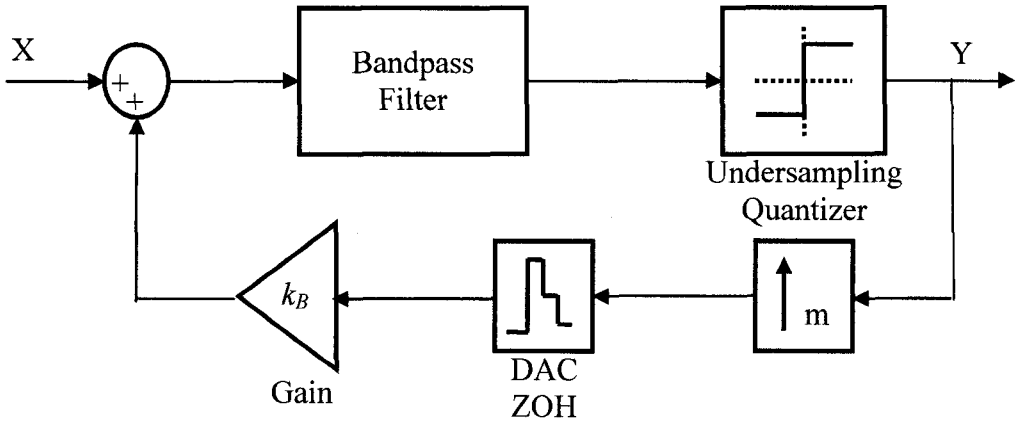


Figure 4-1: Proposed bandpass delta sigma modulator.

where n_o is the number of new samples by which the signal has been delayed. This number could be any integer value between 0 and m-1. The quantizer behaviour is also given by:

$$H_Q(s) = ke^{-sDT_S} \tag{4-3}$$

where D is the number of cycles required in the quantizer until the output signal becomes valid and k is the quantizer's gain. This gain is defined as a ratio of the rms output voltage produced by the quantizer divided by its rms input voltage.

If a second-order band-pass filter is used in the forward path, its transfer function can be expressed by:

$$G(\omega)=\frac{As}{s^2+BWs+\omega_0^2} \tag{4-4}$$

where BW and ω_0 are the bandwidth and the center frequency of the band-pass filter respectively. Now, considering equations (4-1)-(4-4), we can derive the noise transfer function (NTF) and the signal transfer function (STF) respectively as follows:

$$NTF(s)=\frac{s^2+BWs+\omega_0}{s^2+BWs+\omega_0^2-\frac{Ak_Bkm}{T_S}\left(1-e^{-s\frac{T_S}{m}}\right)e^{-sT_S\left(D+\frac{n_O}{m}\right)}} \tag{4-5}$$

$$STF(s)=\frac{Akse^{-sDT_S}}{s^2+BWs+\omega_0^2-\frac{Ak_Bkm}{T_S}\left(1-e^{-s\frac{T_S}{m}}\right)e^{-sT_S\left(D+\frac{n_O}{m}\right)}} \tag{4-6}$$

Because of the limited S/H bandwidth, we could consider that there is a low-pass filter in the forward path. However, in a practical design, its bandwidth is designed to be several times higher than the input signal frequency to minimize its delay. In this case, its impact can be neglected. If the quantization error is modeled as white noise bounded in the range $\pm\Delta/2$, the spectral density of the quantization noise can be expressed by:

$$N_q(f)=e_{rms}\sqrt{\frac{2}{f_S}}NTF(f),\quad \left(e_{rms}^2=\frac{\Delta^2}{12}\right) \tag{4-7}$$

Therefore, the in-band noise power can be estimated as:

$$n_0^2=\int_{f_0-BW/2}^{f_0+BW/2}\frac{\Delta^2}{6f_s}|NTF|^2\,df \tag{4-8}$$

In the proposed structure of the ΔΣM, the phase shift in the feedback can be controlled to be equal $(2k+1)\pi$ using the available design parameters such as m (up-sampling ratio), n_o (rank of non-zero samples in the up-sampled stream), D (quantizer

delay), and sampling frequency. Note that if D is large, even if the modulator is not undersampling, the resulting loop delay tends to limit the stable region. In an undersampling modulator, this is more critical, because each sampling period is longer than the input signal period. Hence, keeping the system stable is difficult for D higher than two periods of the sampling clock. When the up-sampling value, m, increases, the delay introduced by the DAC decreases. The main restrictions limiting the value of m are related to practical issues. For example, when m is equal to 8, and the sampling frequency is 800 MHz, circuits must provide very narrow pulse widths (shorter than 1/6.4 ns). Furthermore, when the pulse width becomes narrower, the signal power is further attenuated as the signal passes through the DAC. Hence, a gain of k_B in the feedback path is required to amplify the signals; otherwise, the input signal amplitude must be limited to avoid saturating the modulator. On the other hand, when choosing a value for m, the associated phase delay in the DAC should be considered. This delay, combined to the up-sampler and quantizer delays, must produce a total phase shift equal to $(2k+1)\pi$ degrees.

Figure 4-2 shows the total phase delay versus sampling frequency obtained from equations (4-1)-(4-3), for different n_o, when D=1, m=4, and the input frequency (fi) = 1800MHz. Using the parameters provided in **Figure 4-2**, we can find the sampling frequency and n_o that produce a negative feedback. For example, when n_o is 0, the sampling frequency can be 810.1MHz, which returns $-\pi$ phase. If the phase delay is $-2k\pi$ (e.g. phase=0 when sampling frequency (fs) = 675MHz), the system will oscillate due to positive feedback. Therefore, the adder in **Figure 4-1** must be converted to a subtractor to have the desired negative feedback.

Figure 4-3 shows STF and NTF obtained from equations (4-5) and (4-6) when D=1, fs=810.1MHz, fi=1800MHz, m=4, n_o=0 assuming a Q-factor=200. Note that a relatively large Q-factor was found necessary to obtain good performance in the MATLAB simulation. A Q-factor=200 is relatively large, but larger Q-factors are reported [113] in RF circuits, and means to get such Q-factors will be discussed later. Using up-sampling and a suitable phase delay, we can see that the system receives the proper negative feedback and the maximum in-band SNR is observed. If we set up the system for other operating points where the phase shift is -π that can be obtained from **Figure 4-2**, we get similar performance in terms of STF and NTF. It is also possible to select the phase delay to have three or five π phase shift. This increases the system order and the stability may decrease.

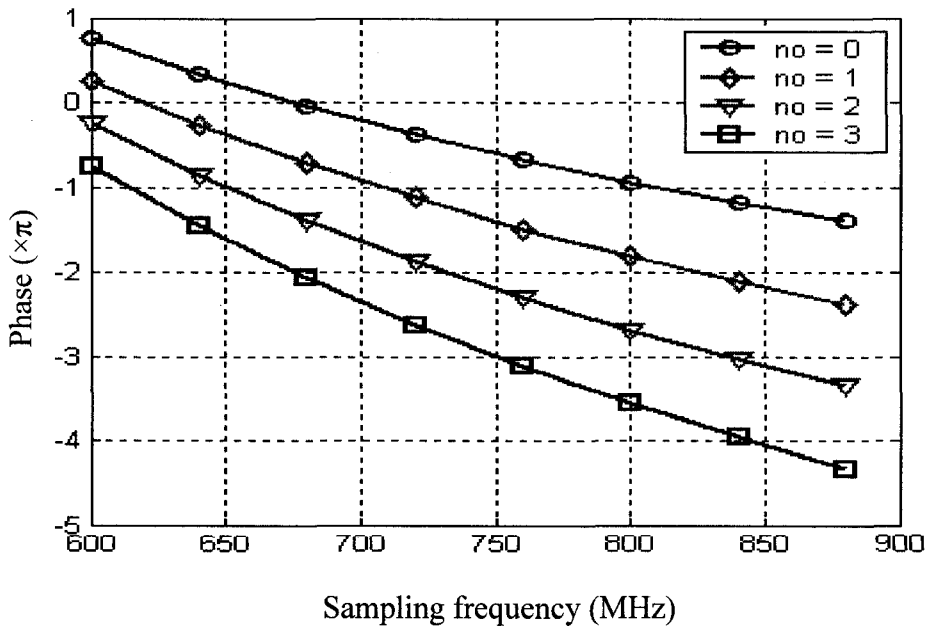


Figure 4-2: Phase delay due to quantizer, up-sampling, and DAC (m=4, D=1, fi=1.8GHz).

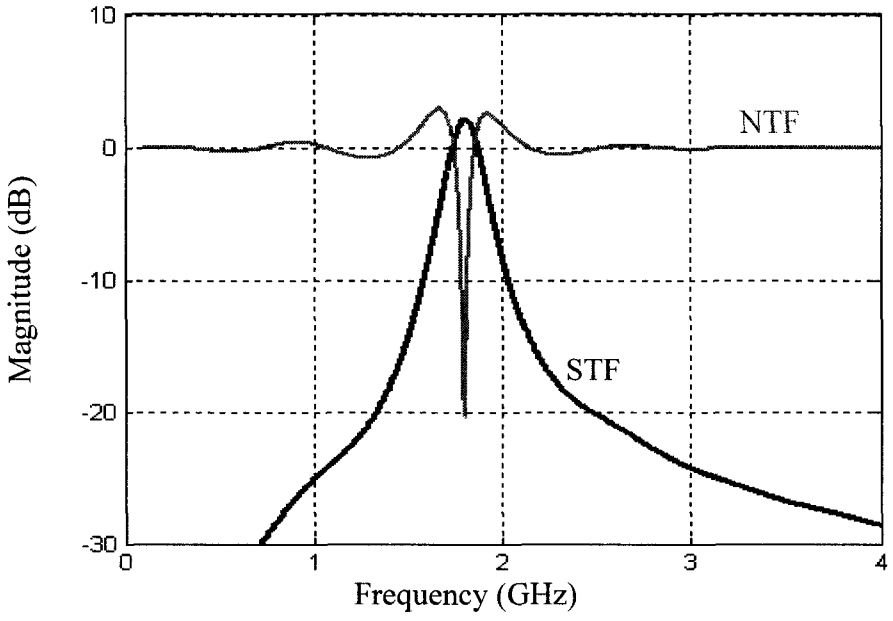


Figure 4-3: NTF and STF of the proposed delta sigma modulator.

The time domain behavior of the proposed ΔΣM can be simulated using MATLAB-Simulink. This was done for our preferred implementation (D=1, m=4, n_0=0 and Q-factor=200) and the resulting output power spectrum is presented in **Figure 4-4**a.

In this simulation, a single tone input signal, at a 1.8 GHz frequency, is shifted at 179.8 MHz due to undersampling at a frequency of 810.1 MHz. It is remarkable that in this output power spectrum, the quantization noise is symmetrically shaped around the desired signal. It shows that a SFDR higher than 50dB is achievable using the proposed architecture and suggested design parameters. Its relatively simple structure allows managing several shortcomings of band-pass ΔΣM, used as A/Ds applied on high frequency (up to multi GHz) carriers modulated with signals of relatively wide bandwidth

(up to 10 MHz). This method can be applied to higher order systems to obtain better results.

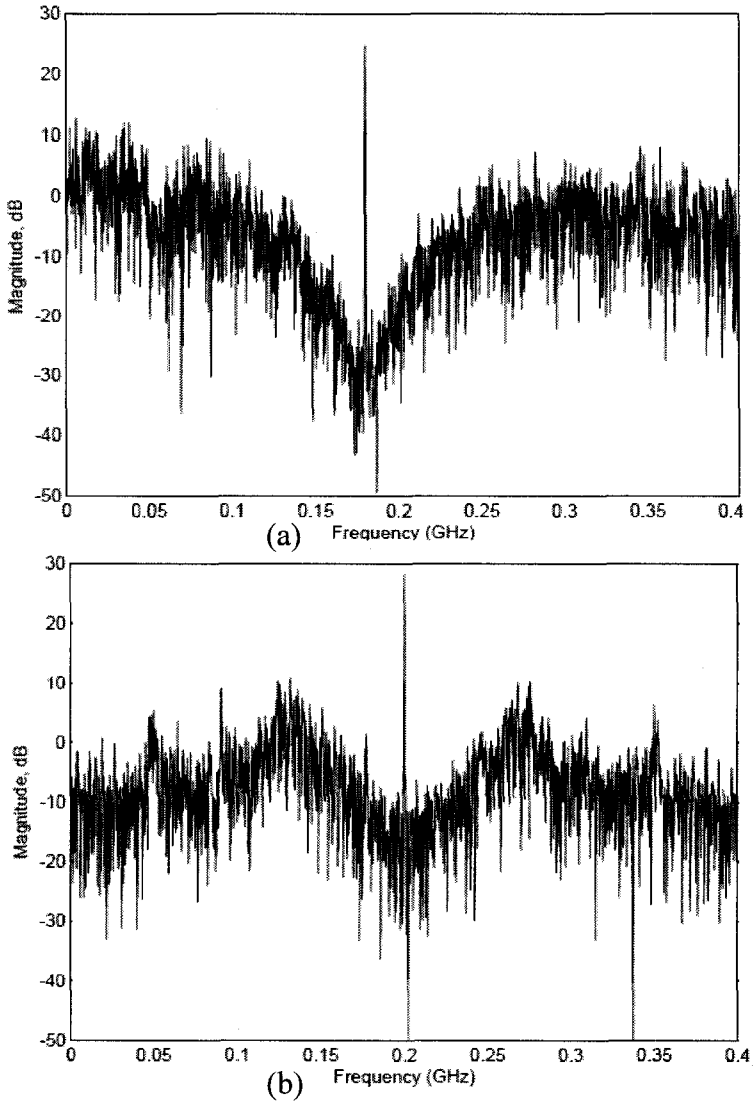


Figure 4-4: Output power spectrum of (a) proposed modulator, (b) modulator using analog mixer.

The performance of the proposed method can be compared with that of the method proposed by Gourgue et al [36] (**Figure 3-13**) when one set of sampling and

input frequencies are applied to both approaches. Using MATLAB, a simulation was performed when both modulators have a 2nd-order band-pass filter with a Q-factor of 200, and receive input frequency of 1.8GHz with an input-to-feedback amplitude ratio of 0.1. To keep similar USRs, the sampling frequency of the Gourgue's modulator is set to 800MHz. Therefore, the mixer frequency must be 1.6 GHz with a $\pi/4$ phase difference and the digital IF would be 200MHz. Finally, both modulators have one clock cycle delay at the 1-bit quantizer. Output power spectrum of the second modulator is presented in **Figure 4-4**b that shows higher in-band distortion and noise level in comparison with the proposed modulator.

The noise and distortion level due to the analog mixer is expected to increase in a practical design, but the above simulation demonstrates a systematic error in that design approach, which is a main difference between the two design methods. We can also derive this error of Gourgue's et al. architecture from the following analysis. Let us assume the output signal placed at the digital IF is given by:

$$Y(n) = \sin(\frac{n\pi}{2} + \Theta) \tag{4-9}$$

After passing through the DAC, by considering the ZOH effect, the main replica of the signal is expressed by:

$$U(t) = \sin(IFt + \frac{\pi}{4} + \Theta) \tag{4-10}$$

Then it is up-converted by the analog mixer (that has a $\pi/4$ phase shift to cancel out the delay of the ZOH) as:

$$W(t)=\sin\left((RF\pm IF)t+\frac{\pi}{4}\pm(\frac{\pi}{4}+\Theta)\right) \tag{4-11}$$

and, finally, after subtracting from the input signal and undersampling with the quantizer, the output changes as:

$$Y(n)=\sin\left(-(RF\pm IF)\frac{n}{f_s}-\frac{\pi}{4}\mp(\frac{\pi}{4}+\Theta)\right) \tag{4-12}$$

$$=\sin\left(-(2\pi N\pm\frac{\pi}{2})n-\frac{\pi}{4}\mp(\frac{\pi}{4}+\Theta)\right)$$

$$=\sin\left(\mp\frac{\pi}{2}n-\frac{\pi}{4}\mp(\frac{\pi}{4}+\Theta)\right)$$

As shown in equation (4-12), the image of the output signal generates another unwanted term when it turns in the loop. This is a systematic error due to a phase delay in the DAC, and it cannot be compensated only by a phase shift of $\pi/4$ in the mixing frequency. Although the image signal is somewhat attenuated in the band-pass filter of the modulator, the degree of attenuation depends on the Q-factor and the filter order, and in this case, a Q-factor higher than 200 would be needed to reject this unwanted image distorting the signal.

A possible circuit implementation of the upsampler and its signal timing are shown in **Figure 4-5** when m=4 and n_0=0. The sampling clock (f_s) is derived from a frequency four times higher ($4f_s$).

As we can see, the proposed implementation of the upsampler consists of an AND gate (*I3*) that is much simpler and less prone to introducing imperfections than an analog mixer. Moreover, all parameters, such as the sampling frequency and loop delay, depend only on the input clock frequency. This dependency makes it possible to tune the system

accurately for the required loop delay. An automatic tuning can also be developed for the modulator as most components are built in the digital domain. Note that the circuit in **Figure 4-5** uses an inverting input in the OR gate (*I1*) to avoid glitches, and that *I2* introduces the same delay as *I1* on the signal A to synchronize events as much as possible.

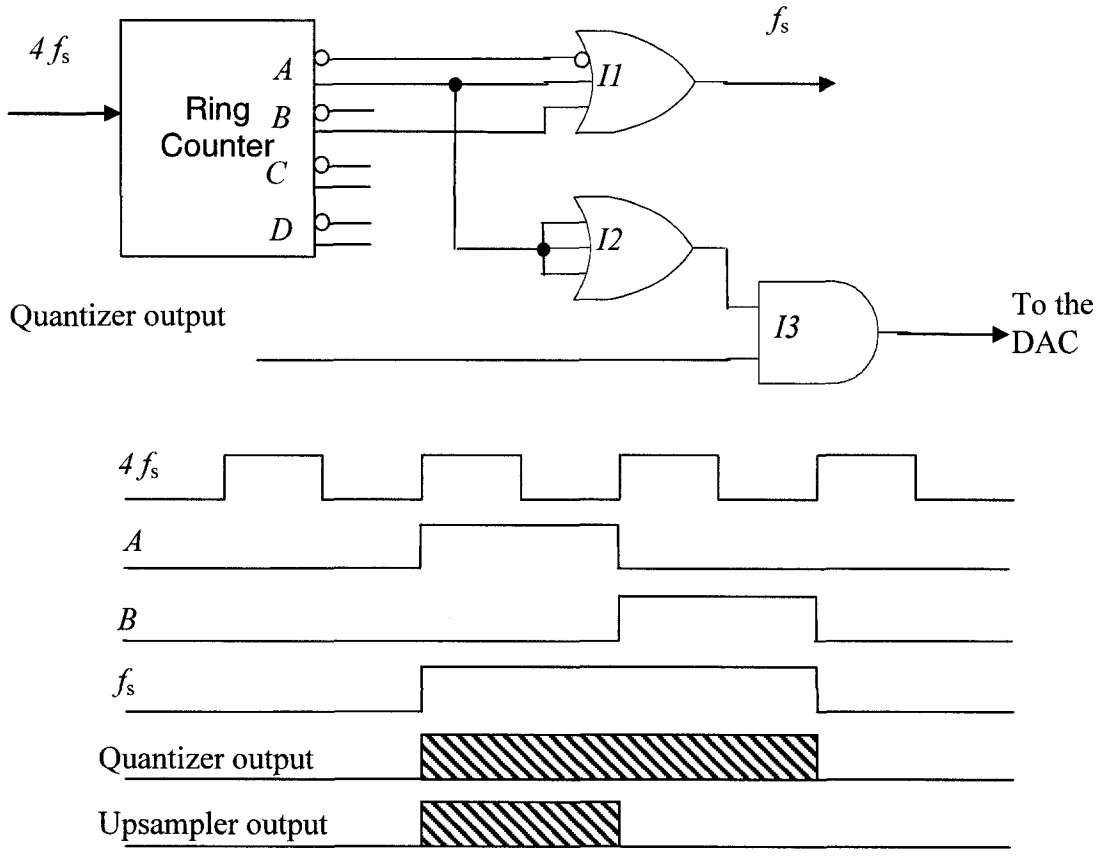


Figure 4-5: Upsampling of modulator output: a) block diagram, b) its timing diagram.

Figure 4-6 shows a LC band-pass filter implemented as a differential structure which more details are given in Appendix A:. A control voltage (Vc) is used to adjust gm of M1 and M2. Also, two diode varactors can be used as the capacitor of the tank (C),

which is used to tune the filter center frequency. The output of the filter is then buffered to increase the S/H's bandwidth.

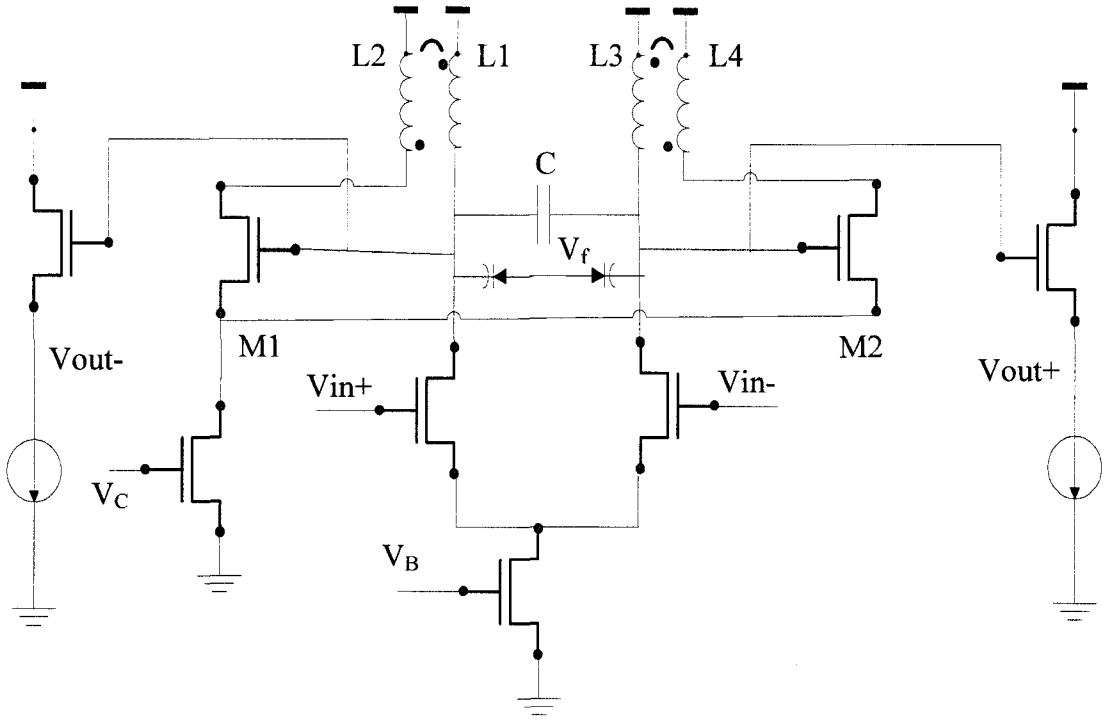


Figure 4-6: Q-enhanced LC band-pass filter.

Figure 4-7 shows the S/H circuit followed by a comparator implementing a 1-bit quantizer. The S/H drives a one-bit quantizer, and its bandwidth must be high enough to capture high frequency signals with minimum delay. Hence, the S/H's bandwidth is designed to be three times higher than the input signal frequency. The output impedance of the filter, in series with the switch impedance and the capacitance of the holding node (Cs), form a low-pass filter. This reduces the bandwidth of the S/H. One way to maintain that bandwidth is to increase the bias current of the filter output stage (see **Figure 4-6**). It reduces the output impedance, but it also increases power consumption, which is not

desirable. On the other hand, reducing Cs requires smaller transistors (Mb1 and Mb2) for the buffer in the S/H, which further attenuates the processed signal. There is a compromise, therefore, between power consumption of the filter and the voltage gain of the S/H.

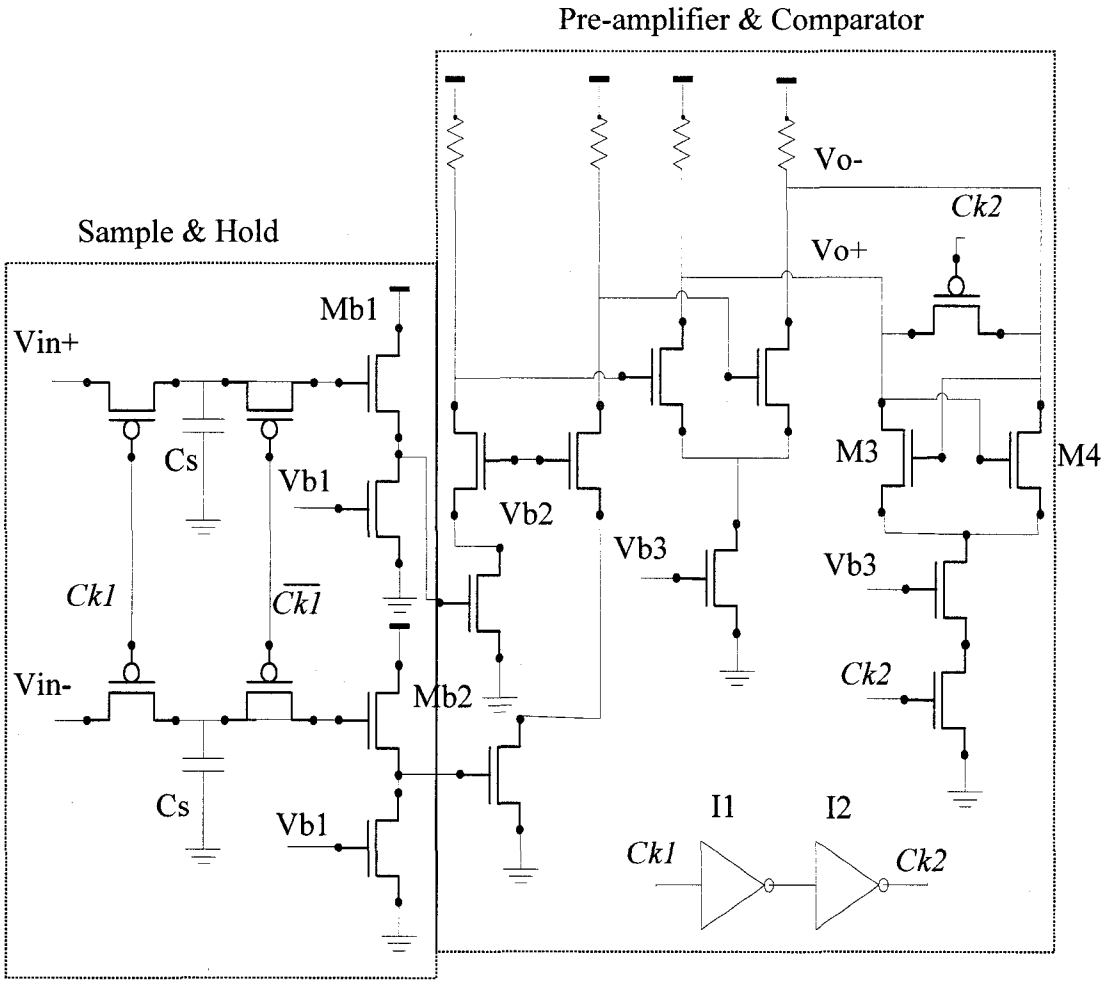


Figure 4-7: Differential "sample and hold" and comparator.

A differential pre-amplifier can be employed at the front-end of the comparator. In the proposed implementation, two back-to-back NMOS transistors (M3 and M4) are used to restore the digital signal levels for each sample. However, the comparator has

hysteresis, and the sample should be amplified and stabilized to avoid any error. In fact, if the comparator and the S/H are clocked simultaneously, the error in the comparator becomes significant for small input signal amplitudes. Therefore, the comparator's clock (Ck2) is delayed from the S/H's one (Ck1) using two inverters (I1 and I2). The comparator then drives a DFF to latch the sample for the whole cycle.

Figure 4-8 shows simulated modulator output spectrum for a transistor level implementation of the proposed ΔΣM using IBM 0.13μm CMOS technology when C=0.69 pF, Vf=480 mV, L1=L2=L3=L4=3 nH, k=0.8 (coupling factor), and Vdd=1.3 V.

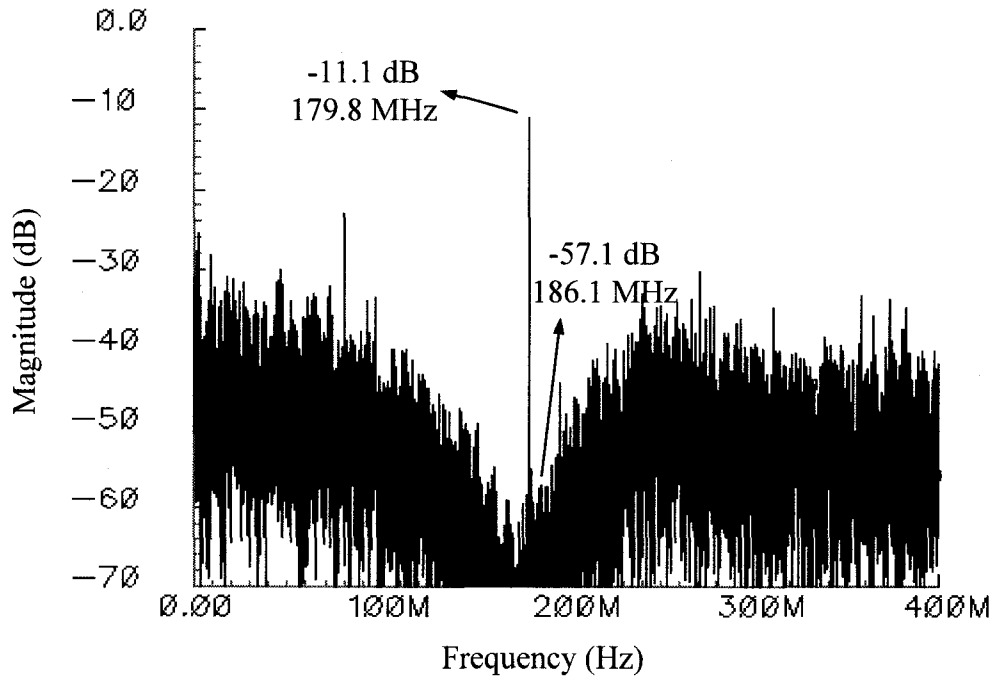


Figure 4-8: Simulated output spectrum of the proposed modulator.

The bandwidth of the filter is set to 10 MHz by a Vc=555 mV, which gives a Q-factor of 180 for an input frequency of 1.8 GHz. The SFDR of the output signal was

found to be 46 dB over a bandwidth higher than 10 MHz. The sampling frequency is 810.1 MHz, and the second IF is placed at 179.8 MHz. Based on that schematic level model, where circuits were not fully optimized, the whole modulator sinks an rms current of 16.72 mA and the total power consumption is estimated at less than 22 mW. This estimate is only provided to suggest the order of magnitude of the expected power dissipation to confirm that the proposed architecture can produce low power implementations.

4.3. Effect of Nonidealities

4.3.1 Clock Jitter

When the clock frequency is as high as the one reported, the clock jitter becomes important and difficult to manage. Continuous-time modulators are more prone to clock jitter than discrete-time ones, due to use of two clocks, one in the quantizer and one in the DAC. The clock jitter in the quantizer contributes to quantization noise, while the jitter of the DAC appears at the output by the signal transfer function of the modulator. In general, clock jitter introduces pulse width variations and clock delays. It is shown by [80] that in second-order modulators, signal transfer function mitigates the delay clock jitter, but the pulse-width clock jitter has a white noise spectrum that constitutes a

dominant effect on the final SNR. Therefore, the effect of pulse-width clock jitter in the DAC should be considered as a parameter in the design. The in-band noise power due to the clock jitter is given by:

$$P_j = \frac{\sigma^2 \Delta^2 f_s^2}{OSR} \tag{4-13}$$

where σ is the rms value of the jitter, and Δ is the quantization step. Recalling from equation (4-8), the clock jitter can be ignored if its power is less than in-band noise floor as expressed by:

$$P_j \leq \int_{f_0 - BW/2}^{f_0 + BW/2} \frac{\Delta^2}{6 f_s} |NTF|^2 df \tag{4-14}$$

Consequently, the maximum allowable ratio of the clock jitter to the sampling period is derived as:

$$(\frac{\sigma}{T_s})^2 \leq \frac{OSR}{6 f_s} \int_{f_0 - BW/2}^{f_0 + BW/2} |NTF|^2 df \tag{4-15}$$

From Eq. (4-5) and (4-15), it becomes clear that increasing the modulator order puts more stringent requirements for the clock; otherwise, it degrades the SNR performance. For example if T_s=1.23ns, BW=10MHz and if noise floor = -57dB, according to the model, the maximum allowable jitter is 15.5ps, and it is relatively easy to design a clock distribution network for a jitter smaller than that level.

4.3.2 Excess Loop Delay

Ideally, modulator must have zero delay due to DAC and continuous part of the system. In circuit level implementation of the high speed modulators, because of nonzero switching time in the DAC, signal is delayed. Output of the CT filter is usually buffered for the quantizer. This buffer also contributes in the loop delay. Total delay of the modulator can be modeled in one unit before the DAC at the digital side. This delay must be considered in the calculation of the sampling frequency. Therefore, the sampling rate should be tuned to a new rate to compensate the loop delay and keeping the phase delay equal 180 degrees for input frequency of 1800MHz. The up-sampling and the DAC can be viewed in a general form shown in **Figure 4-9**.

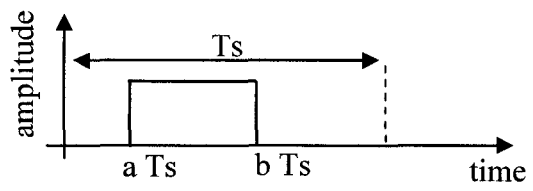


Figure 4-9: DAC pulse used in the modulator.

In the proposed modulator a=0 and b=0.25 when n0=0 and m=4. From equations (4-1) and (4-2), we have:

$$R(s)=\frac{1}{s}\left(e^{-as}-e^{-sb}\right) \tag{4-16}$$

Using impulse-invariant transformation method, an equivalent discrete-time model of the open loop system is expressed as:

$$Z^{-1}\{RG(z)\} = L^{-1}\{R(s)G(s)\} \tag{4-17}$$

Some equivalent systems are given in [19] as:

$$\frac{1}{s - s_k} \Leftrightarrow \frac{y_0}{z - z_k} \tag{4-18}$$

where

$$z_k = e^{s_k} \tag{4-19}$$

$$y_0 = \frac{z_k^{1-a} - z_k^{1-b}}{s_k} \tag{4-20}$$

If a partial fraction expansion of the loop filter can be presented as:

$$G(s) = \frac{A/2}{s - j\omega_0} + \frac{A/2}{s - (-j\omega_0)} \tag{4-21}$$

Equivalent of each part is found by equation (9) and therefore, by combining them an equivalent discrete-time model is expressed by:

$$G(z) = \frac{A}{\omega_0} \frac{cz + d}{z^2 - 2\cos\omega_0 z + 1} \tag{4-22}$$

where

$$c = \sin(\omega_0(1-a)) - \sin(\omega_0(1-b)) \tag{4-23}$$

$$d = \sin(\omega_0 a) - \sin(\omega_0 b) \tag{4-24}$$

Therefore, if the delay required in the quantizer is one clock period, the NTF is derived as:

$$NTF(z) = \frac{z(z^2 - 2\cos\omega_0 z + 1)}{z^3 - 2\cos\omega_0 z^2 + k_1 z + k_2} \tag{4-25}$$

where

$$k_1 = 1 - \frac{A}{\omega_0}\left(\sin(\omega_0(1-a)) - \sin(\omega_0(1-b))\right) \tag{4-26}$$

$$k_2 = -\frac{A}{\omega_0}\left(\sin(\omega_0 a) - \sin(\omega_0 b)\right) \tag{4-27}$$

When there is no excess loop delay, NTF(z,a,b)=NTF(z,0,0.25). In presence of loop-delay=ΔTs, NTF(z,a,b)=NTF(z,Δ,Δ+0.25). In order to find the effect of the new sampling rate in the NTF, we need to compare center frequency and damping-factor (DF) in the NTF for those sampling rates. Because of under-sampling the center frequency of the NTF changes by equation (4-28).

$$IF = \mathrm{mod}(RF, f_s) \tag{4-28}$$

Hence, two NTFs that are actually notch filters should be compared in term of bandwidth or DF. If the DFs be equal in the both cases, then quantization noise is suppressed in the same manner and consequently, the final SNR is kept constant. Pole-zero maps of the NTF for two sampling frequencies are shown in **Figure 4-10**. Although, the loop delay can change the DF of the poles, but its effect is compensated by the new sampling frequency. **Figure 4-11** shows magnitude and phase of the NTF when sampling frequency changes from 833MHz to 863MHz. As we expected, phase is balanced between +/-90 degrees at frequency=853MHz and shows zero loop delay.

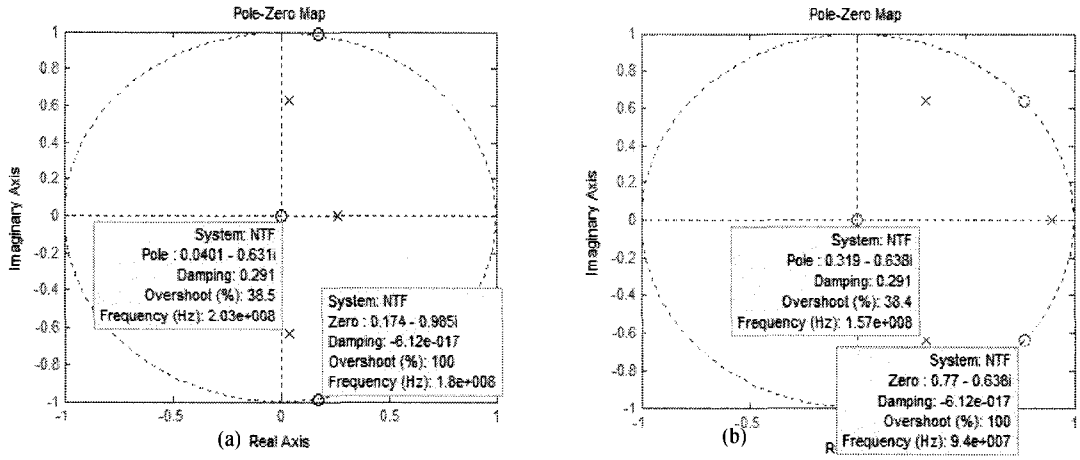


Figure 4-10: Pole-zero map of NTF when (a) *fs*=810MHz, Δ=0, (b) *fs*=853MHz, Δ=0.06.

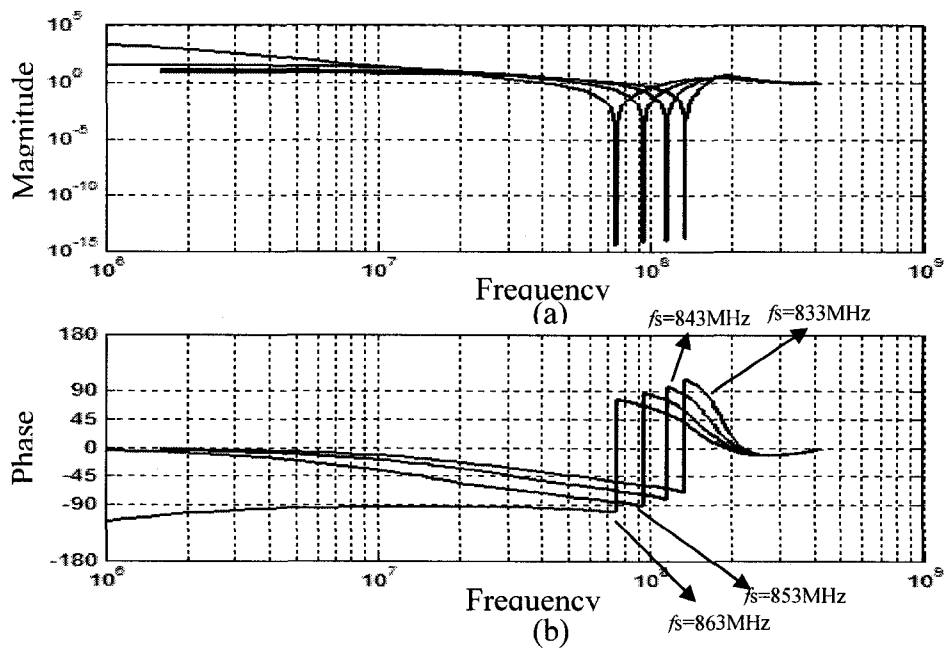


Figure 4-11: NTF of the modulator for different sampling frequencies (a) magnitude, (b) phase.

4.3.3 Filter Noise Analysis

In order to analyze the whole filter in term of noise, the small signal models of the LC filters are shown in **Figure 4-12**. The contribution of each element is derived analytically.

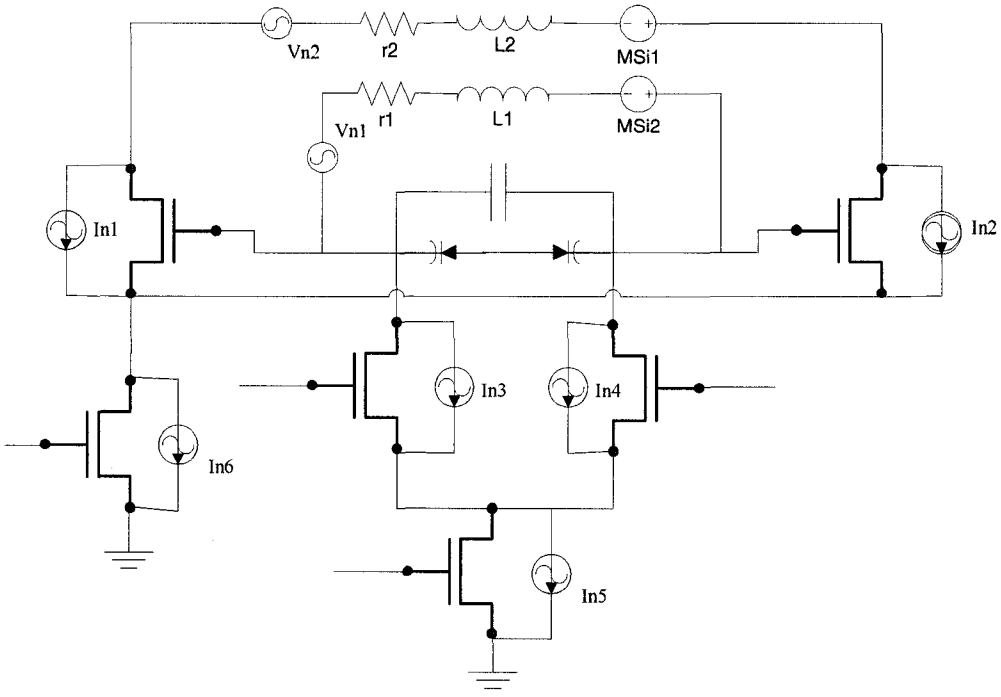


Figure 4-12: Ac models of the bandpass LC filters.

Recall from Equation 3-10, in a FET transistor, the thermal noise of the channel can be expressed by:

$$\bar{i}_n = \sqrt{\Delta f}\sqrt{\gamma 4kT(g_m + g_{mb} + g_{ds})} \tag{4-29}$$

Where, γ is 2/3 for both long and short channel devices. The resistors in the circuits can also contribute to the final noise power by the following expression:

$$V_n^2 = \Delta f 4kTR \tag{4-30}$$

The noise of common transistors (M5, and M6), which effects on common mode, is rejected in the differential signal. Hence, only M1-M4 contribute on output noise, estimated as:

M3 and M4:

$$\left.\begin{aligned} i_2 &= -g_{m2}V_1 \\ V_1 &= Msi_2 + (r_1 + L_1 s)i_1 \end{aligned}\right\} \Rightarrow \frac{V_1}{i_1} = \frac{r_1 + L_1 s}{1 + g_{m2}Ms} \tag{4-31}$$

$$\frac{i_1}{I_{n3}} = \frac{1}{\frac{r_1 + L_1 s}{1 + g_{m2}Ms}Cs + 1} \tag{4-32}$$

$$V_{n3}^2 = I_{n3}^2 \left[\frac{r_1 + L_1 s}{1 + (g_{m2}M + r_1 C)s + L_1 C s^2} \right]^2 \tag{4-33}$$

M1, and M2:

$$\left.\begin{aligned} i_2 &= -(I_{n2} + g_{m2}V_1) \\ V_1 &= Msi_2 + (r_1 + L_1 s)i_1 \\ i_1 &= -i_c \\ V_1 &= i_c Z_c \end{aligned}\right\} \Rightarrow \frac{V_1}{I_{n2}} = \frac{-Ms}{1 + (g_{m2}M + r_1 C)s + L_1 C s^2} \tag{4-34}$$

$$V_{n2}^2 = I_{n2}^2 \left[\frac{Ms}{1 + (g_{m2}M + r_1 C)s + L_1 C s^2} \right]^2 \tag{4-35}$$

By considering the resistance in the primary, the associated noise can be derived as:

$$\left.\begin{array}{l} i_2 = -g_{m2}V_1 \\ V_1 = V_{nr1} + Msi_2 + (r_1 + L_1 s)i_1 \\ i_1 = -i_c \\ V_1 = i_c Z_c \end{array}\right\} \Rightarrow \frac{V_1}{V_{nr1}} = \frac{1}{1+(g_{m2}M + r_1 C)s + L_1 C s^2} \tag{4-36}$$

$$V_{n2}^2 = V_{nr1}^2 \left[\frac{1}{1+(g_{m2}M + r_1 C)s + L_1 C s^2}\right]^2 \tag{4-37}$$

It should be noted that r2, the series resistance of the secondary inductor, does not contribute to the output noise because the secondary current is fixed by the M1 and M2 and, therefore, the noise can not change the current.

Therefore, the total output noise is estimated as:

$$V_{n\_out}^2 = 2I_{n3}^2 \left[\frac{r_1 + L_1 s}{1+(g_{m2}M + r_1 C)s + L_1 C s^2}\right]^2 + 2I_{n2}^2 \left[\frac{Ms}{1+(g_{m2}M + r_1 C)s + L_1 C s^2}\right]^2 + V_{nr1}^2 \left[\frac{1}{1+(g_{m2}M + r_1 C)s + L_1 C s^2}\right]^2 \tag{4-38}$$

4.4. Conclusion

Limitations of existing architectures were identified in undersampling delta sigma modulators that can be used to implement receivers' architectures. A main motivation for exploring this class of modulator is the possibility of using them to implement programmable receivers. Based on a detailed understanding of limitations found in

existing architectures, a new continuous-time band-pass modulator architecture was proposed. A set of design equations applicable to this architecture was developed as well as key circuit techniques needed to implement it. The proposed design can be used in receivers with no analog mixer to digitize signals modulated over high frequency carriers. Using a continuous-time modulator, noise and nonlinearity of the S/H are shaped together with the quantization noise and attenuated by the system. Matching of digital IF with analog IF is carried out using upsampling in the digital side. The proposed modulator has no excess loop delay due to delay tuning by sampling rate. Simulation results of a schematic circuit implementation using IBM 0.13 μm CMOS technology showed a SFDR of 46 dB at the output of the second-order modulator for an input signal with a bandwidth of 10MHz modulated at 1.8GHz. The total power consumption was estimated to be less than 22mW with a supply voltage of 1.3V. The design method can be applied to develop higher order modulators that would produce higher SNR.

Chapter 5

New Delta Modulator Based on Undersampling

5.1. Introduction

As we discussed in Chapter 3, in radio frequency receivers it is desirable to remove all analog components between the analog to digital converter (ADC) and the low noise amplifier (LNA), to make a receiver programmable and compatible with multiple standards present in commercial broadcasting and telecommunications [35]. This can also relax design constraints caused by imperfections and mismatches in the mixers and PLLs. However, in such systems, the ADC must be as fast as the radio frequency signal, and it must consume relatively little power. Over-sampling band-pass converters can be one way to implement required ADCs, because they consume less power and occupy a smaller silicon area than other converters. They have more immunity to $1/f$ noise and they also have a high linearity. Therefore, the ability to process fast signals is the main and virtually the only challenge in the design of over-sampling converters.

In order to move to high-frequency applications like RF receivers, there are two main ways to design over-sampling converters: using either a fast technology or undersampling techniques. The first method, which follows traditional architectures in over-sampling converters, usually employs non-CMOS technologies to get very high sampling rates [23]. Such solutions are expensive and power hungry, with power

consumption in the order of 3.2-6 W. According to our knowledge, there is no CMOS over-sampling converter in the literature that is faster than the design reported in [106] and that operates at 4 GS/s to receive signal modulated over an input carrier frequency of 1 GHz. CMOS is normally used for its low-cost and low-power advantages. However, the power dissipation is not less than 290 mW for a bandwidth of 500 kHz. Therefore, to meet current wireless commercial standards with carrier frequency around 2 GHz, it is necessary to use mixers that can handle these high frequencies. In this case, digitization of the signal by the first method with CMOS technology may not be as advantageous as are the traditional receiver architectures explained in Chapter 2.

The second method, based on undersampling, has more potential to increase the operating frequency with a little increase in the power consumption. In this method, which was explained in the previous chapter, the carrier frequency of the input signal goes down to low-IF (depending on the sampling rate) after conversion to digital. Although, low-IF at the output reduces the complexity of digital mixers, the low-pass characteristic of the DAC in the feedback path of the modulator severely attenuates the signal.

Most of the designs using this method have already been reviewed and their advantages and disadvantages investigated. However, there are a few more points that need to be mentioned here. First, the maximum operating frequency of the reported designs in the literature is on the order of a few hundred MHz, which indicates upgrading even the known methods to Giga Hertz range is a real challenge at the circuit level. Second, the SNR in the output signal is usually low (below 50dB). Regarding the low-order band-pass filter, attenuation of those unwanted images is not higher than 40 dB, and,

consequently, it is the main source of noise and non-linearity limiting the SNR. Third, by increasing the center frequency of the delta-sigma modulator, the characteristics of the forward band-pass filter in the delta-sigma modulator become almost impractical in commercial CMOS technology, or we need to over-design.

For example, trying to convert a 4-GHz signal using these techniques requires a Q-factor higher than 400 when the bandwidth of the signal is less than 10 MHz. Even if the delta-sigma modulator is designed for a wide bandwidth to reduce the Q-factor to values as low as 200, the band-pass filter must be controlled by a very accurate and automatic tuning system. Otherwise, any variation in the filter affects the final performance of the modulator. Even though undersampling DSM is theoretically able to operate at very high frequency, the practical issues cited above limit its application. In addition, the center frequency of the band-pass filter in a delta-sigma modulator should be the same as the input frequency of the modulator, while tuning ability of RF band-pass filters is usually less than 20% of their center frequencies. Hence, in this chapter we present a delta modulator as a solution to these problems. This design was implemented and fabricated and experimental results are reported.

5.2. Proposed Undersampling Delta Modulator

In order to compensate for the practical issues described above, a continuous-time delta modulator is proposed. It works with the same performance as delta-sigma

modulators and is capable of receiving high frequency signals. Furthermore, the center frequency is not the same as the input carrier frequency and there is no such limitation. As discussed earlier, the mixer in the feedback loop and tuning of the band-pass filter are two important limitations of delta-sigma modulators (**Figure 5-1**a). We can remove both of them by considering the fact that the main purpose of the band-pass filter is only to shape the spectrum of the quantization noise. **Figure 5-1**b shows equivalent system presented in **Figure 5-1**a. We suppose that the input signal is already filtered by an anti-aliasing filter. Therefore, a band-pass filter in the forward path does not change the spectrum of the input signal. It also has no effect on the feedback signal if the band-pass gain is one. Consequently, the band-pass filter in the forward path can move to the feedback path if it is centered at IF instead of at the input frequency (**Figure 5-1**c). In such a case, we can remove the mixer and all its imperfections. Moreover, the frequency of the input signal is not limited by the center frequency of the delta-sigma modulator.

The proposed modulator is shown in more details in **Figure 5-2**. The circuit is a fourth-order modulator in a double-loop architecture using two second-order bandpass filters. The bandpass filter used in the feedback path is the second-order active-RC filter. Its center frequency and Q-factor is tunable to meet the desired performance after fabrication. Hence, an input and output are considered for tuning purposes in idle times. Furthermore, the system can also be tuned using the output signal of the modulator when a reference carrier is available. The S&H in the feed forward path must have a very high bandwidth to capture signals with maximum frequency of 2 GHz.

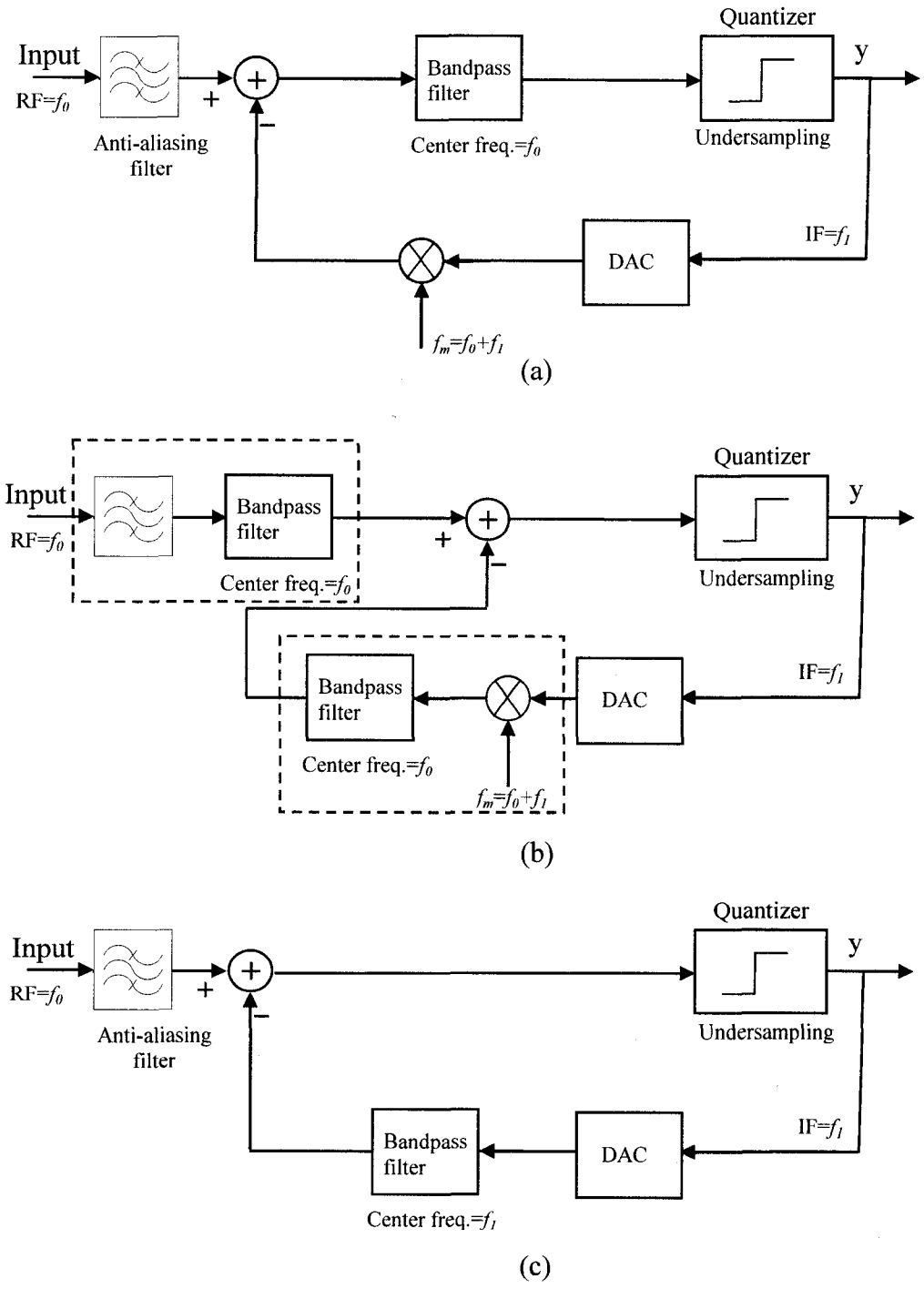


Figure 5-1: Block diagram of the modulator: (a) proposed in [36], (b) intermediate step, (c) proposed in this work.

Higher frequencies may also be captured by this architecture, but it depends on the technology and circuit level implementation. Sampling frequency follows the input carrier. In this case, a sampling rate of 495 MHz is needed to have the digital IF at 20 MHz. The clock frequency is two times higher than the sampling frequency. Using a frequency divider, the frequency decreases to achieve lower jitter and 50% duty cycle. The quantizer is a one-bit comparator that is driving a buffer and a DAC.

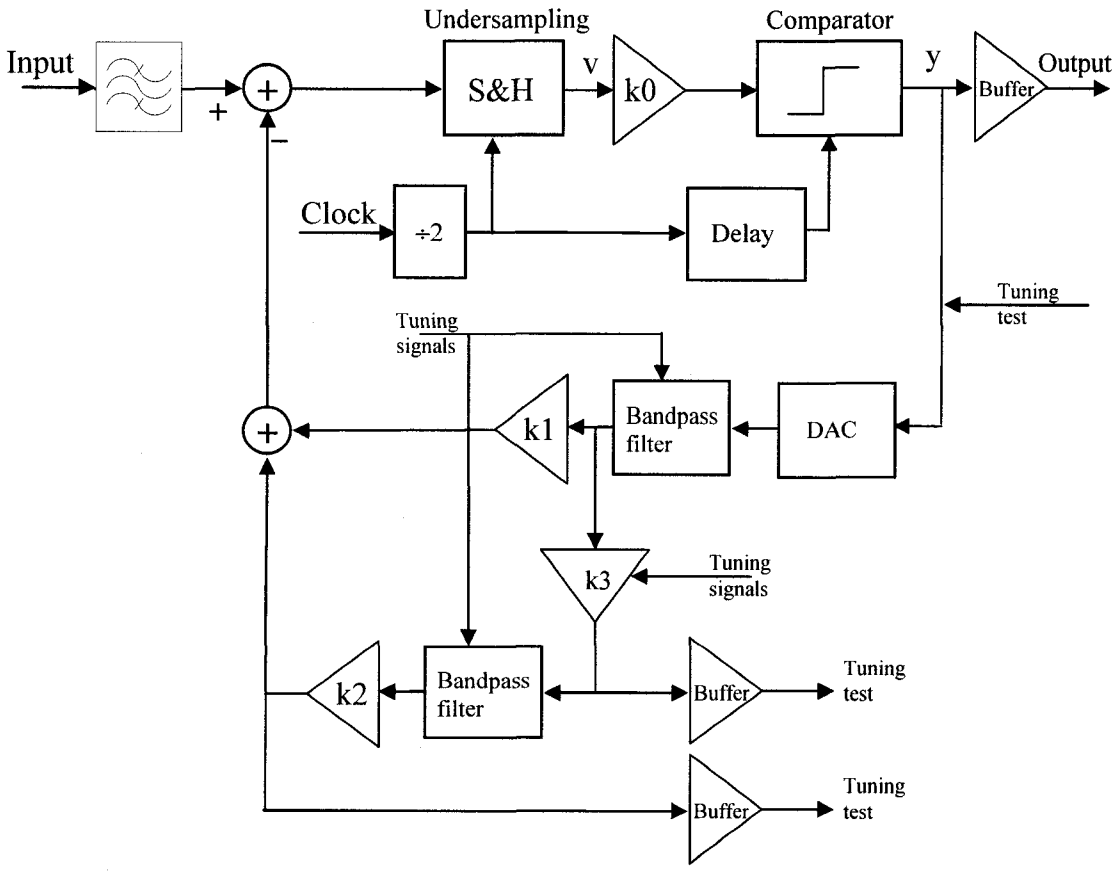


Figure 5-2: Block diagram of the proposed delta modulator.

The forward path is the critical path in term of circuits, because a combination of both high-frequency and low-frequency signals must propagate through that path. Therefore, circuits must be very linear for a wide range of frequencies; otherwise, they introduce a large distortion. The distortion could be in the phase or magnitude of signals, and none of them can be easily compensated. The forward path must also introduce as little delay as possible on the propagated signals. Indeed, the delay due to this path can cause an increase of the order of the system and therefore lead to a reduction of the stability. Assuming the quantization step is Δ, the error entered into the signal (noise power) through the 1-bit quantizer can be estimated by:

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de \tag{5-1}$$

$$E(f) = \frac{e_{rms}}{\sqrt{f_s/2}} = \frac{\Delta}{\sqrt{6 f_s}} \tag{5-2}$$

where f_s is the sampling frequency. Bandpass filter and quantizer are given by:

$$H(s) = \frac{As}{s^2 + sBW + \omega_0^2} \tag{5-3}$$

$$H_Q(s) = k_0 e^{-sT_s} \tag{5-4}$$

Where BW is the bandwidth of the input signal, A is the gain, ω_0 is the center frequency of the band-pass filter, and k_0 is the quantizer gain. The DAC in the feedback can also be modeled as:

$$Q(s) = \frac{1 - e^{-sT_s}}{sT_s} \tag{5-5}$$

The NTF is expressed by:

$$NTF = \frac{1}{1 + k_0 e^{-sT_s}(k_1 H + k_2 H^2)Q(s)} \tag{5-6}$$

where k_1, k_2 and k_3 are feedback coefficients shown in **Figure 5-2**. In order to avoid an overload error, the output signal should be able to track the sampled signal. Therefore, the sampling frequency must satisfy the following condition:

$$A_i \omega_0 < \Delta f_s \tag{5-7}$$

where A_i is the amplitude of the input sinusoidal signal. Granular noise usually happens in the output spectrum when the quantization step is large and cannot settle at any point. This noise is decreased by either increasing the sampling rate or decreasing the quantization step. Note, however, that multi-level quantization is not so interesting due to the lower complexity and better linearity obtained from the 1-bit quantizer. Let us assume the quantization step, Δ, is one in a 1-bit quantizer, and the input signal is a 2 MHz bandwidth modulated at 2 GHz shifted to $\omega_0=2\pi f_0$ due to undersampling. Thus we can choose 495 MSPS to get a 20MHz IF.

The NTF can define the magnitude of the noise at the output. If the loop gain for noise is large, stability of the system is at risk. A common rule found from many designs [79], states that out-of-band noise gain should not be more than 1.5. The higher gain increases the SNR but reduces the stability. Therefore, assuming k_3=1, we might set the loop gain constant around one:

$$k_0(k_1 + k_2) = 1 \tag{5-8}$$

The k_0 is the gain of the typical comparator which is given by:

$$k_0 = \lim_{N \to \infty} \frac{\sum_{n=0}^{N} y(n)v(n)}{\sum_{n=0}^{N} v(n)^2} \tag{5-9}$$

where y and v are shown in **Figure 5-2**. This value is dependent of input signal pattern and changes by changing the input signal. This parameter that is used for linearization of a nonlinear quantizer is one of the main reasons for some disagreement between simulation and analytical results [79]. The other important factor in setting the design parameters k_1 and k_2 is the maximum amplitude of the input. The modulator produces the maximum SNR at only one amplitude of the input signal, which is related to the amplitude of the feedback signal. In other words, the ratio between input signal and feedback signal defines the SNR. When all feedback and input signals are entered into the adder block, we may face linearity issues in circuit level design due to large incoming signals. Therefore, large values of k_0 can relax linear circuit design, but from another side they require very high gain bandwidth in the pre-amplifier of the quantizer.

In order to define a target ratio between k_1 and k_2, there are two rules. First, a modulator at higher order produces higher SNR. Thus, the larger k_2 the larger SNR. Second, a modulator at higher order has larger out-of-band noise gain. Hence, a smaller k_2, provides a better stability. Recalling the rule that limits maximum out-of-band noise gain to 1.5, we can set the value of the parameter from NTF magnitude as shown in **Figure 5-3**.

Another parameter that could change the output SNR is the Q-factor of the bandpass filters. A large Q-factor in the loop filter decreases the output SNR in the delta modulators. By increasing the Q-factor, the in-band filter gain increases, which reduces ratio of the input signal amplitude to the feedback signal amplitude. Recall from equation (5-3), when the BW is zero, the filter gain is infinite at the center frequency of the filter. Such a gain highly attenuates the quantization noise and NTF=0 at that frequency. But the feedback signal amplitude is extremely larger than the input signal amplitude at that frequency and consequently, the modulator tends to transfer the input signal to the output with a gain close to zero. Unlike a sigma delta modulator, which high Q-factor can improve output SNR, the Q-factor in the delta modulator should be properly defined to have the highest SNR. Indeed, we should design the bandpass filter for parameters Q-factor and filter gain in such way that the maximum feedback amplitude is equal to the maximum input amplitude.

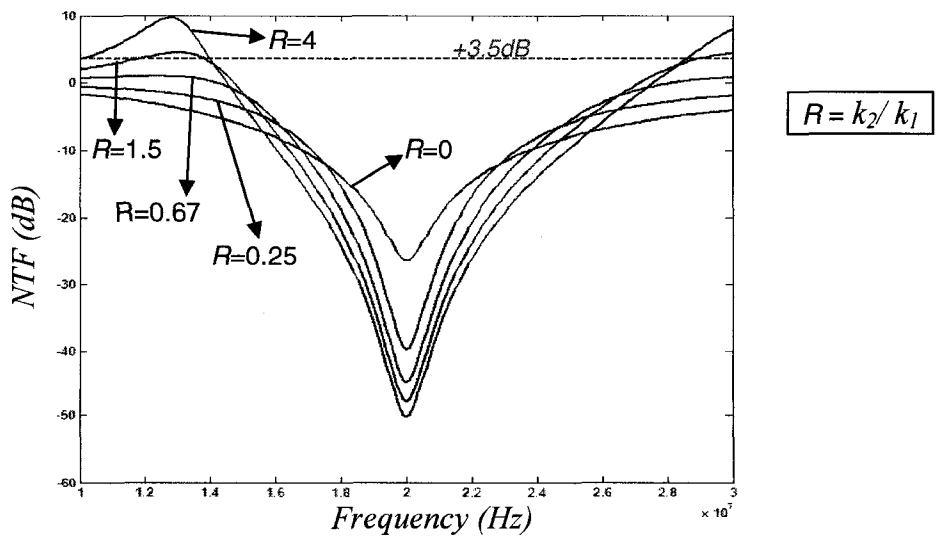


Figure 5-3: NTF magnitude for different k_1 *and* k_2.

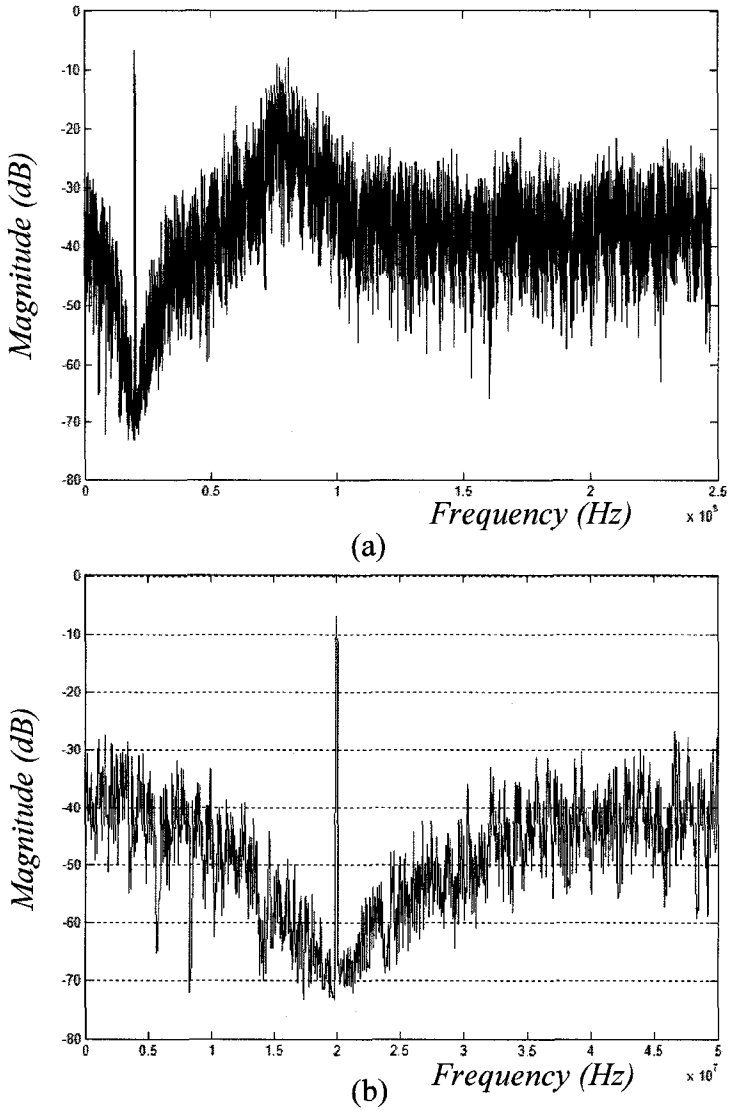


Figure 5-4: (a) Output power spectrum of the proposed modulator. (b) Magnified.

Figure 5-4 shows simulation result using MATLAB for the output power spectrum of the modulator. In those simulations, the IF is placed at 20 MHz for the input signal frequency of 2 GHz and the bandwidth is 2 MHz. The output SFDR is measured to be 55 dB, when the sampling rate is 495 MSPS. By correctly choosing the sampling rate

and quantization step, no idle tone appeared in the output spectrum. The output frequencies are shown to be up to half of sampling frequency (*fs*). This spectrum is mirrored in the range of *fs*/2 to *fs* and the whole spectrum is repeated for every *fs* that contain other replicas of the signal.

Figure 5-5 presents the output SFDR for different ratios of the input signal amplitude over the feedback signal amplitude. A comparison among simulation results is given by **Table 5.1**. Compared to previously reported results, carrier frequency of the signal has been increased by a 10-fold factor, as well as signal bandwidth, while implementation complexity was reduced. The input signal frequency can reach 2 GHz, independent of the center frequency of the band-pass filter.

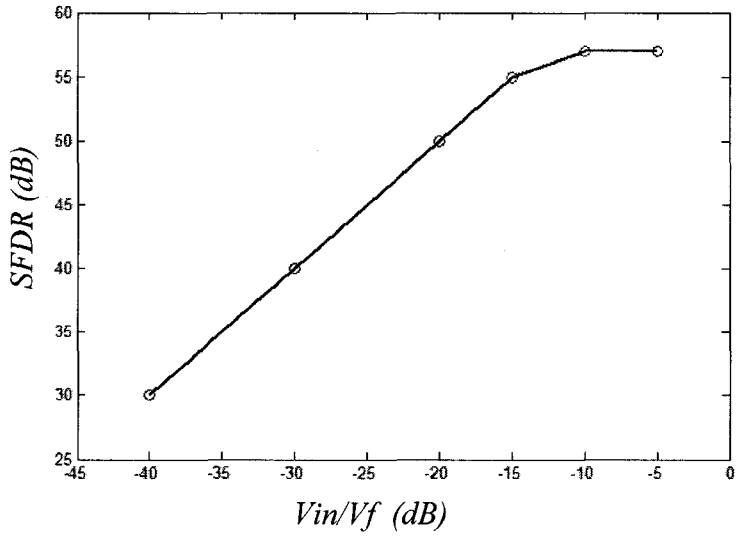


Figure 5-5: Output SFDR versus ratio of input signal over feedback signal.

For the band-pass filter, if on-chip implementation is desired, we can use either Active-RC or Gm-C filter. However, Active-RC filter presents better linearity for large

input swings, due to the use of feedback with passive components. It is also necessary that this filter be tunable in terms of its center frequency and Q-factor to mitigrate the effects of process variations. Although noise-shaping modulators are moderately immune to component imperfections (such as noise and linearity), those errors can be modeled as quantization error. Harmonics generated by the filters may get close to the signal when undersampling is using in the quantizer. Therefore, to control harmonics due to non-linearity, linearity has the highest priority among other design parameters for the band-pass filter if high dynamic range is needed.

Table 5.1: Simulated results of proposed delta modulator compared with other works.

Design	***[36]***	***[44]***	***This work***
Carrier frequency of input signal (*fc*)	10.7 MHz	195 MHz	2 GHz
Signal bandwidth	Not available	300 kHz	2 MHz
Sampling frequency	4.71 Ms/s	40 / 20 Ms/s	495 Ms/s
IF	1.28 MHz	5 MHz	20 MHz
SFDR	78 dB	49 / 40.2 dB	55 dB

The subtractor, which receives RF and IF signals, should be matched with a 50 Ohms impedance on the RF-side, and it should also exhibit a high impedance on the other side to get IF signals with acceptable gain. As far as wide input frequency range is concerned, using any LC-band-pass filter on the RF side may limit the input frequency, but low-noise matching is easier. We assume the LNA already provides enough gain for

the signal; therefore, wide-band resistive matching could be suitable, as shown in **Figure 5-6** for the differential structure.

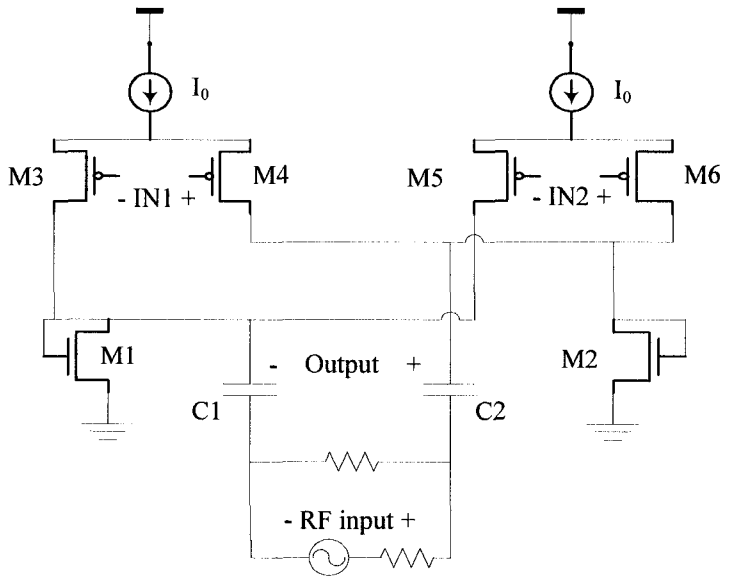


Figure 5-6: Transistor level of the subtractor.

When matching the impedance of the structure, the effect of capacitors C1 and C2 can be compensated by the parasitic inductors of the package. Diode configuration used with M1 and M2 provides DC biasing for the next stage, which is an amplifier. The output signal of the subtractor has a very wide bandwidth and the amplifiers should have a flat gain with a minimum of delay. Because of continuous-time implementation of the modulator, accuracy of the sample and hold in the quantizer are only 1-bit. However, the sample and hold block, which is driven by the on-chip amplifiers, must have a large bandwidth. While a moderate voltage gain of 10-40 is required by the amplifiers for such a bandwidth, the output impedance could be high. Therefore, the design of the forward

path begins from the sample and hold block (for the desired bandwidth); it then focuses on the pre-amplifiers, to finish with the subtractor.

Assuming up to 20 degree phase delay is acceptable as excess loop delay, if a system is designed for maximum frequency of 2 GHz, then required bandwidth in the S&H is estimated as:

$$BW = \frac{2\pi f}{\tan(\theta)} = 2\pi 5.5GHz \tag{5-10}$$

This implies to an RC smaller than 29 ps, and if total capacitance of the holding node be 150 fF, the maximum series resistance is less than 190 Ω. The low resistance can be achieved by a buffer stage between S&H and subtractor block as shown in **Figure 5-7**.

In order to satisfy the requirement of the S&H, the value of buffer resistor in **Figure 5-7** is set to be R=120 Ω. But such a load is too small for a CMOS amplifier and decreases the voltage gain. The voltage gain is extremely important in the quantizer for high frequency signals. Hence, a large gm is needed in the buffer that can be obtained by either large size transistor or large biasing current. The large size produces large parasitic capacitance, and consequently a reduction in bandwidth that is not acceptable. Using a large current seems to be the only solution. However, a small size transistor with a large current requires a large overhead voltage that is in conflict with low voltage supply available for CMOS 0.13μm.

This is one of the reasons why advanced technologies are not suitable for analog circuits. Hence, we performed a few simulations to find the appropriate threshold

voltages versus transistor size as shown in **Figure 5-8**. Four times the minimum size is chosen that gives small threshold voltage without making the transistor too large.

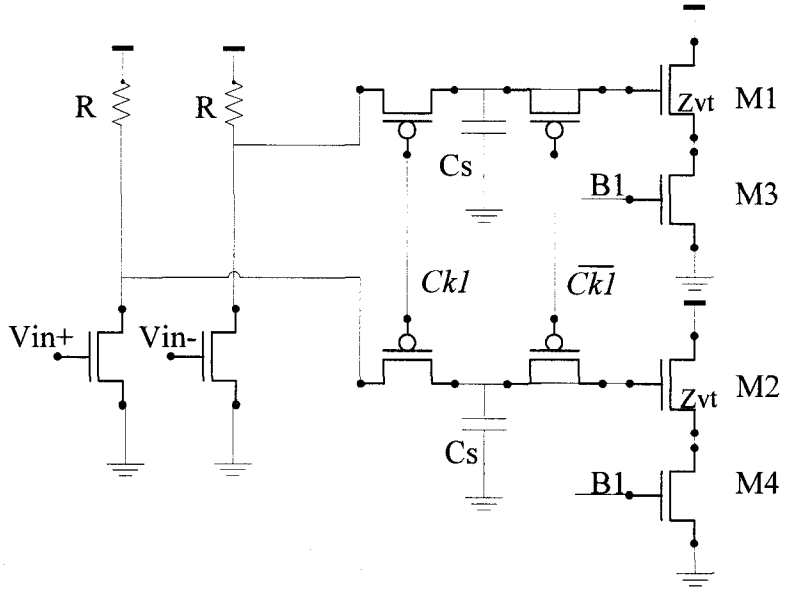


Figure 5-7: Buffer and S&H circuits.

By using a transistor at relatively low threshold voltage, a larger gm is reachable and buffer transistors and some biasing circuits are set up to get a voltage gain around one. However, there is another critical node in the S&H that is the DC voltage of the gate in M1 and M2 shown in **Figure 5-7**. Because of the large current through R, there is a large voltage drop and gate voltage is low. Again a large gm is needed in M1 and M2 to minimize the loss gain, while their size must be small to get non-dominant Cgs.

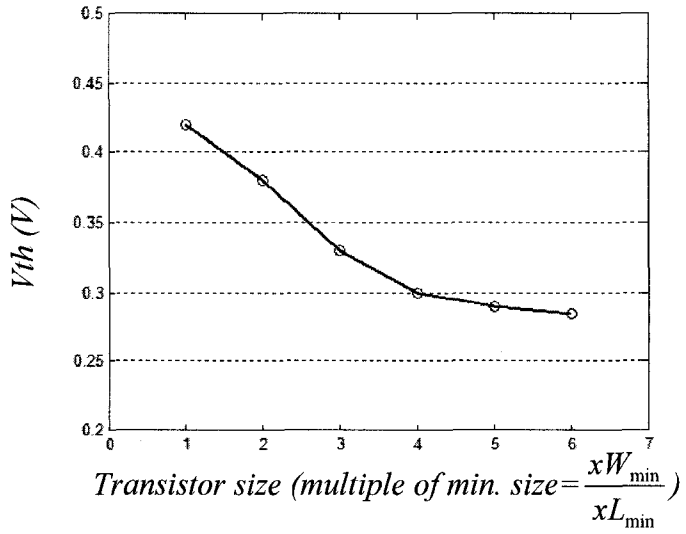


Figure 5-8: Threshold voltage of an NMOS transistor versus size of transistor.

The only transistor available in the technology which could cope with such conditions is zero-Vth NMOS, because its threshold voltage is as low as 80 mV, and a large gm is obtained for a minimum size zVth-NMOS. As the circuit is analog, the leakage drain-source current is not an issue, because the transistor is always on and leakage current is integrated by the bias current.

The comparator shown in **Figure 5-9** produces the output digital levels from the sampled signal. Due to low biasing voltage at the output of the S&H, the input stage of the comparator is PMOS. Two back-to-back inverters are set at the highest gain using a switch. The other inverters amplify the signal to reach the digital levels. It should be noted that settling to digital levels is needed as quickly as possible to run the quantizer at the highest OSR. It may seem that the digital levels can be low voltages to save power. However, the lower voltage levels take more time to settle and reduce the speed tremendously.

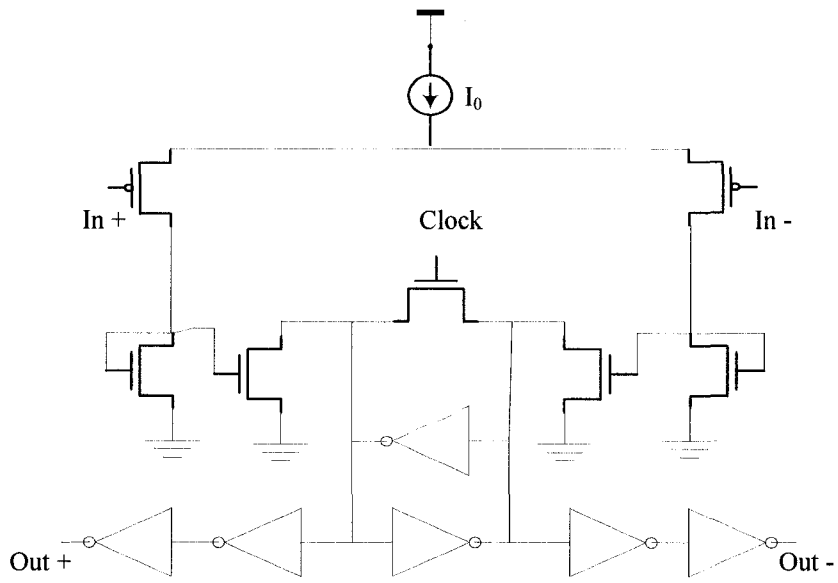


Figure 5-9: Circuit level of the comparator employed in the delta modulator.

Another issue is signal voltage level at different nodes of the modulator. At some nodes, a high voltage swing is required, while the next block can not receive and pass large signals linearly. The subtractor and Active-RC filter are using a small signal but the comparator produces a large signal. Simulation results for 1-dB compression point of the filter are given later in this chapter. This issue wastes the energy consumed in the comparator, and demands more linear gain in the feed-forward path. The levels of the signal are adjusted in the DAC, and a small signal is entered into the filters.

The layout of the modulator is shown in **Figure 5-10**. It occupies 0.7mm x 1.42mm = 1 mm^2 on silicon including pads using IBM 0.13μm CMOS technology. The modulator is simulated for 32k samples at the output using hamming window, and a power spectrum of the output signal is presented in **Figure 5-11**.

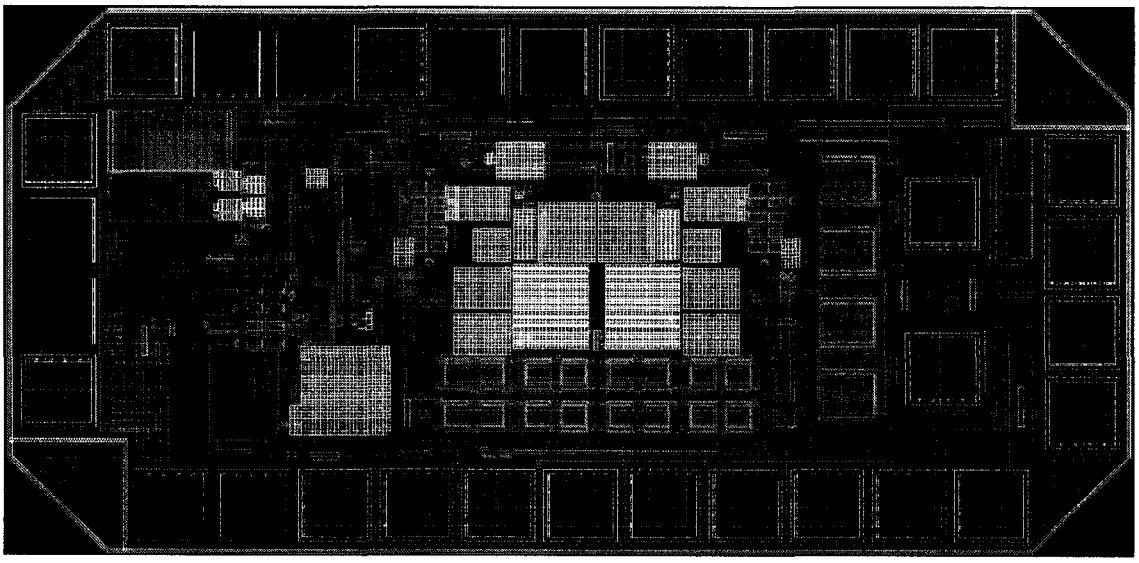


Figure 5-10: Layout of the delta modulator in CMOS 0.13μm.

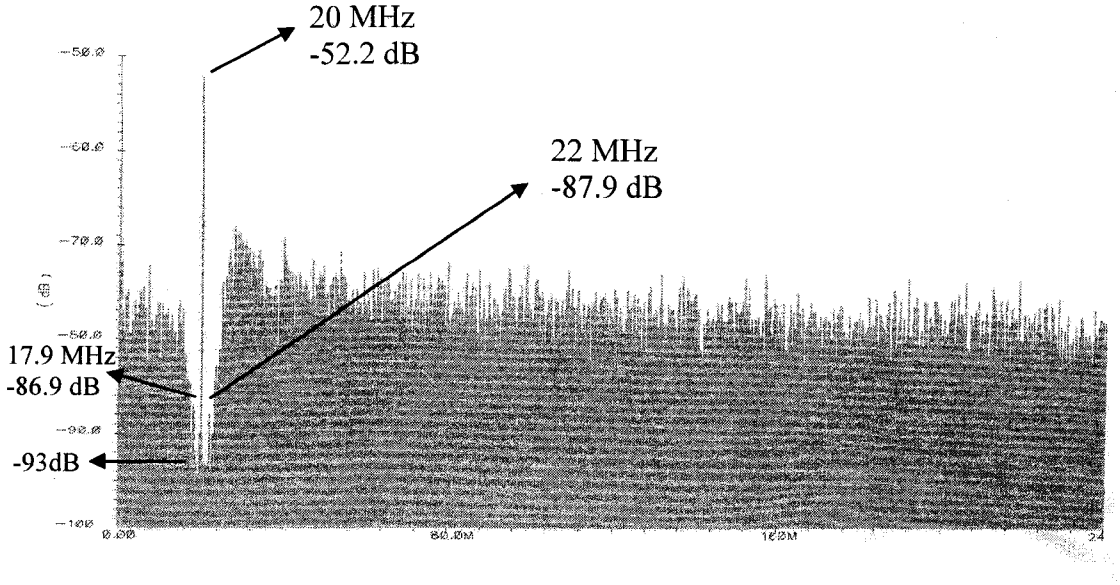


Figure 5-11: Simulated power spectrum of the modulator output.

5.3. Bandpass Active-RC Filter

In a passive filter, inductor and capacitor act as integrator in a current and voltage domain. But in an active filter, integrators are needed where inductors are not available.

Hence, the design parameters are resistance (R), and capacitance (C). Variation in the absolute value of such parameters on the chip requires tuning after fabrication. Depending on the process technology, key parameters (R and C) may vary 20-50%, which is a significant issue in filter design. When a parametric characteristic depends on the values of R or C, they must be tunable. MOS transistors can be used as tunable resistors or capacitors in small signal operation. However, there are a few points that must be considered in the design. First, MOSFETs are nonlinear, but mostly their I-V characteristics have second-order behaviour. Thus, in order to remove the even-order harmonics, circuits should be designed in a balanced form. Second, good performance of an op-amp can mitigate many issues due to having feedback in the filter.

In the proposed Delta Modulator the IF (20 MHz) was too low for on-chip implementation of the filter by LC resonance technique. Gm-C and active-RC filters are, therefore, the best candidates in terms of operating frequency for such modulator. Although undersampling could bring a RF signal directly down to the baseband, a low-IF is more desirable to avoid DC offset errors. Very low-IF also requires large on-chip capacitance to obtain low frequency poles [102]. The first issue in the design of the filter is to obtain a linear operation of input stage transconductance for large input swings and rejection of large adjacent channel signals and then tuning of the filter. Pre-filtering using a passive RC ladder can reduce the input swing and suppress the out of band signals [46]. However, a phase shift is added to the signal. This phase is also process dependent and disturbs systems like a delta modulator, where loop delay reduces system stability. In this application, the adjacent channels, which could be far from the signal, depend on the

sampling frequency, but the out of band noise is quite large. As far as linearity is concerned, the passive devices present high linearity, and, consequently, active-RC filters are more suitable for the mentioned application than the Gm-C filters. The amplifier receives a small signal swing in the active-RC filters due to the feedback with the passive components. However, linear tuning of the passive RC is difficult. The differential structure of the bandpass filter is shown in **Figure 5-12**. M1 and M2 are in the deep triode region and act like variable resistors with control voltage of Vf. If their resistance R0 is much smaller than R1, the first pole of the filter is placed at 1/(R0C1).

The second pole is defined by R2 and C2. There is also a positive feedback by gm0 that defines the Q-factor of the filter. Transfer function of the filter is given by:

$$H(s)=\frac{(-1/R_1)s}{\frac{g_{m0}R_2-1}{R_{01}R_2C_1}+\frac{(g_{m0}R_2-1)(C_1+C_2)}{R_2C_1}s+C_2s^2} \tag{5-11}$$

where R01 is R0R1/(R0+R1). The gm_0, which is implemented by a differential pair, can be controllable by a current source (Iq). Therefore, Center frequency and Q-factor of the filter are tunable by a control voltage and current. If error due to finite gain of the amplifier is negligible, the center frequency and bandwidth of the filter are given respectively by:

$$\omega_0=\sqrt{\frac{(1-g_{m0}R_2)}{R_{01}R_2C_1C_2}} \tag{5-12}$$

$$BW=\frac{(1-g_{m0}R_2)(C_1+C_2)}{R_2C_1C_2} \tag{5-13}$$

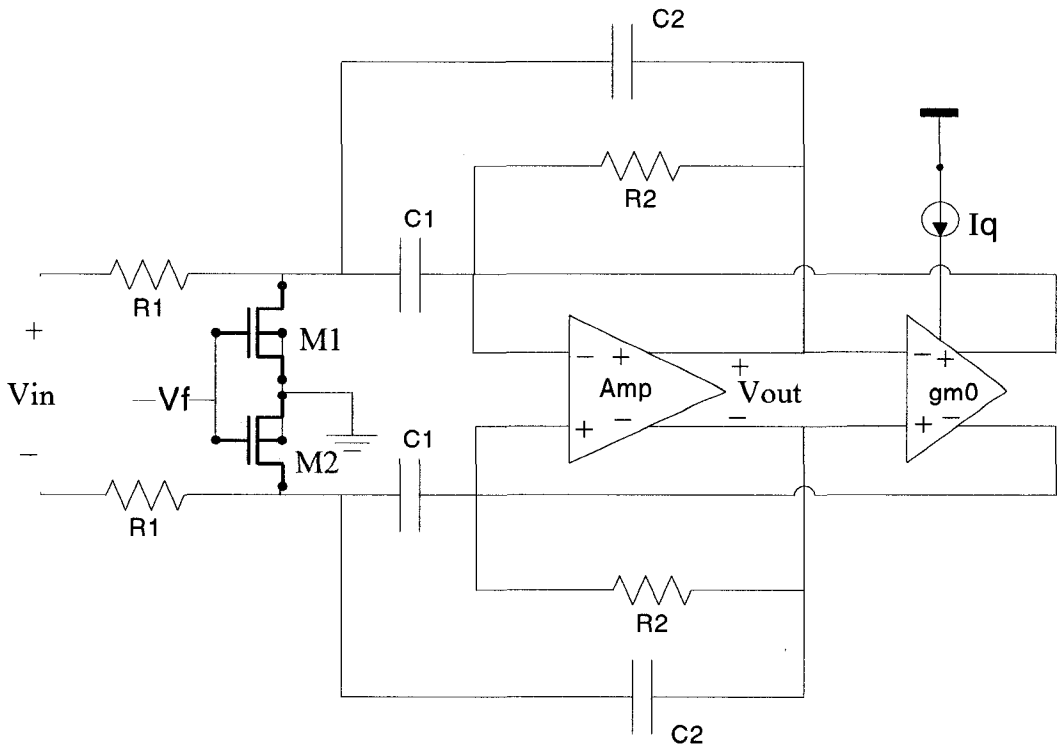


Figure 5-12: Differential architecture of the bandpass filter.

By applying the positive feedback as shown in **Figure 5-12** , voltage swing of the input stage in the amplifier increases and consequently, associated distortion increases. It also introduces some phase delay in the feedback signal due to heavy capacitive load. Hence, we applied the output of gm_0 to points A and B of the amplifier as shown in Figure 5-13. This reduces input voltage swing and increases linearity of the filter.

Frequency compensation methods are discussed in Appendix B: for wideband amplifiers. Based on the topology presented in Figure B-2, a wideband amplifier is designed for the proposed active-RC filter shown in Figure 5-13.

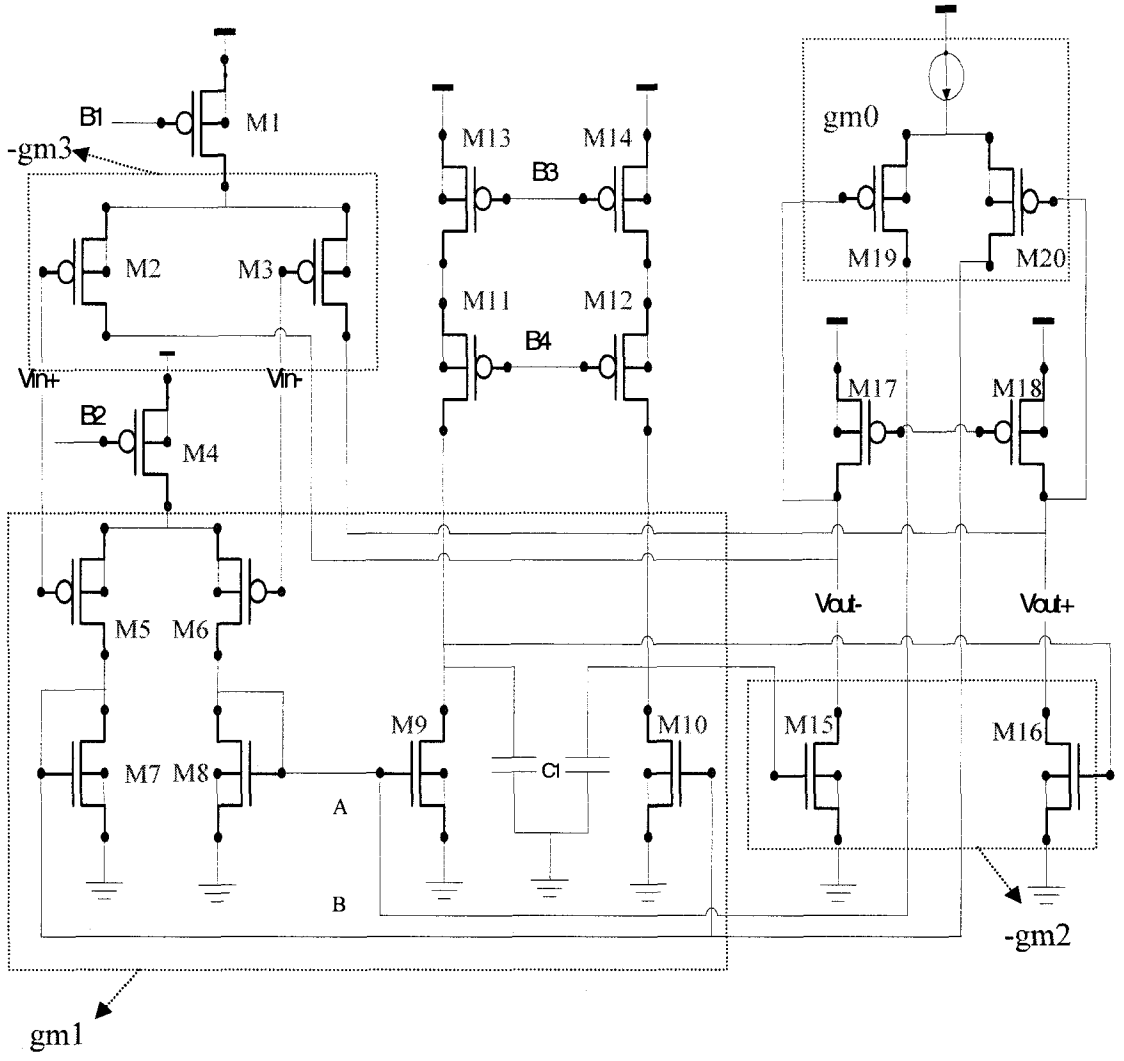


Figure 5-13: The amplifier with positive feedback to control Q-factor of the filter.

The requirements for such an amplifier are defined by the filter, in which the amplifier must have at least 40dB voltage gain at 20MHz to suppress error, and phase margin (PM) >45 degree for a stable feedback. The dominant pole is designed to be at the first stage, and the other pole of the amplifier at the second stage. The input signal is amplified differentially by the first stage and folded into a node, which has the dominant

pole. The capacitor C1 and the gm of each stage are the design parameters which must be adjusted to reach maximum bandwidth. The voltage supply being less than 1.2 V implies the number of stacked transistors at each branch is limited. Use of some architectures with high output impedance, like folded cascode, could facilitate insertion of a dominant pole without capacitor C1. However, a moderate voltage swing can make large distortion or may change operating conditions of transistors that have low effective voltage due to low supply voltage.

Frequency response of the amplifier is shown in **Figure 5-14**. Phase margin is 49 degree at unity gain frequency of 1 GHz and DC gain of 58 dB, while voltage gain is 43 dB at 20 MHz. A summary of the results are given in **Table 5.2** in comparison with simulation results of other works.

Table 5.2: Simulated characteristic performance of the amplifier and comparison.

Characteristic	**Design**		
	[31]	***[38]***	***This work***
Technology (μm)	0.25	0.35	0.13
DC gain (dB)	63	100	58
Power supply (V)	2.5	1.5	1.2
UGBW[1] (MHz)	327	205	1000
PM @ unity gain	85°	62°	49°

1: Unity Gain Bandwidth

The output signal of the filter is then buffered for 50-ohm impedance probing. The buffer circuit is shown in Figure 5-15 and sizes of the transistors are given in Table 5.3 .

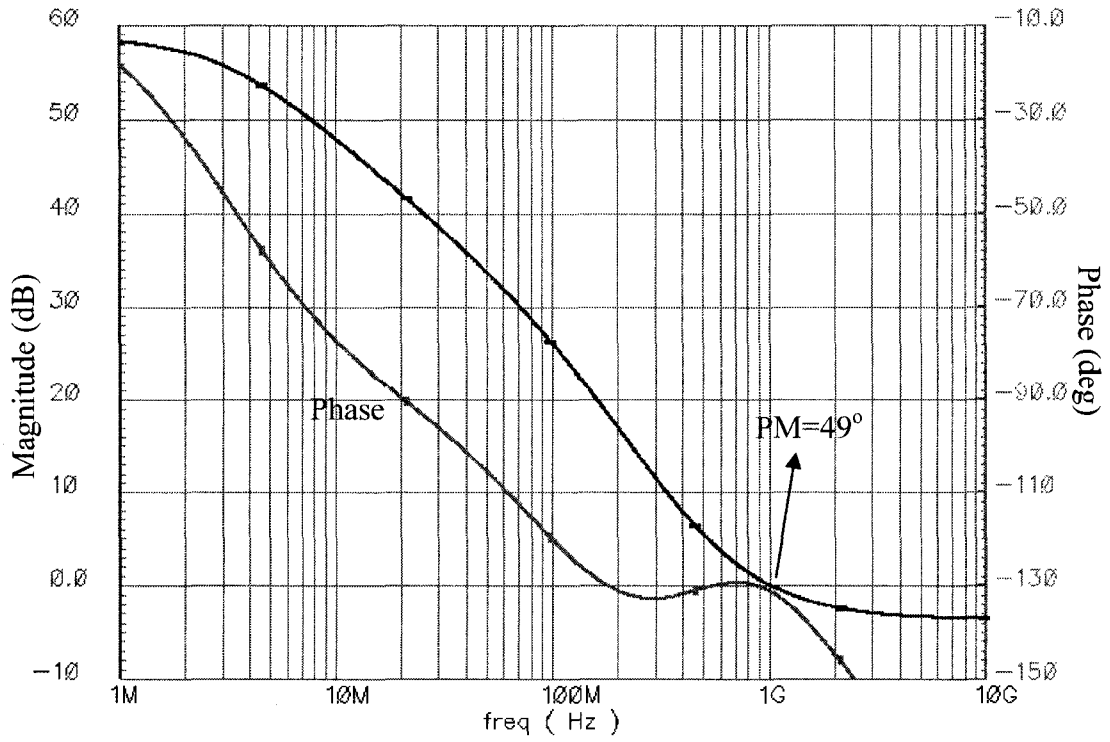


Figure 5-14: Frequency response of the amplifier.

Table 5.3: Sizes of the transistors used in the active-RC filter.

Transistor	W/L(μm)	Transistor	W/L(μm)	Transistor	W/L(μm)
M1	161.28/0.48	M9/M10	38.4/0.48	M19/M20	3.84/0.6
M2/M3	345.6/0.48	M11/M12	57.6/0.48	M21	1.92/0.24
M4	806.4/0.48	M13/M14	57.6/0.48	M22	28.8/0.24
M5/M6	96/0.48	M15/M16	107.52/0.48	M23	259.2/0.24
M7/M8	46.08/0.48	M17/M18	103.68/0.48		

Layout of the second order bandpass filter is shown in Figure 5-16. It occupies 330μm x 240μm in 0.13μm CMOS technology. C1 and C2 in the filter are identical with a value of 8.6 pF, while R1 and R2 are 2.1 kΩ and 3.4 kΩ respectively.

Total power consumption of the filter is less than 4.6 mW when power supply is 1.2 V. **Figure 5-17** presents frequency tuning of the filter for a constant bandwidth of 3.4 MHz. This tuning requires simultaneous adjustment of Iq and Vf between 70-320μA and 0.75-1.23 V respectively.

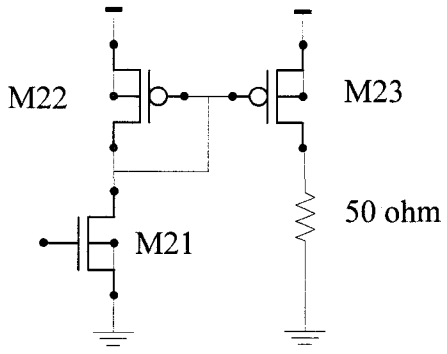


Figure 5-15: Output buffer in the active-RC filter.

We can see different Q-factors between 4 and 11 for a center frequency of 20 MHz in **Figure 5-18**. Finally, as shown in **Figure 5-19**, the filter achieves a 1-dB compression point of -9.4 dBm that demonstrates linearity of the filter for large input voltage swing. **Table 5.4** presents a summary of the results and compares them with other bandpass filters.

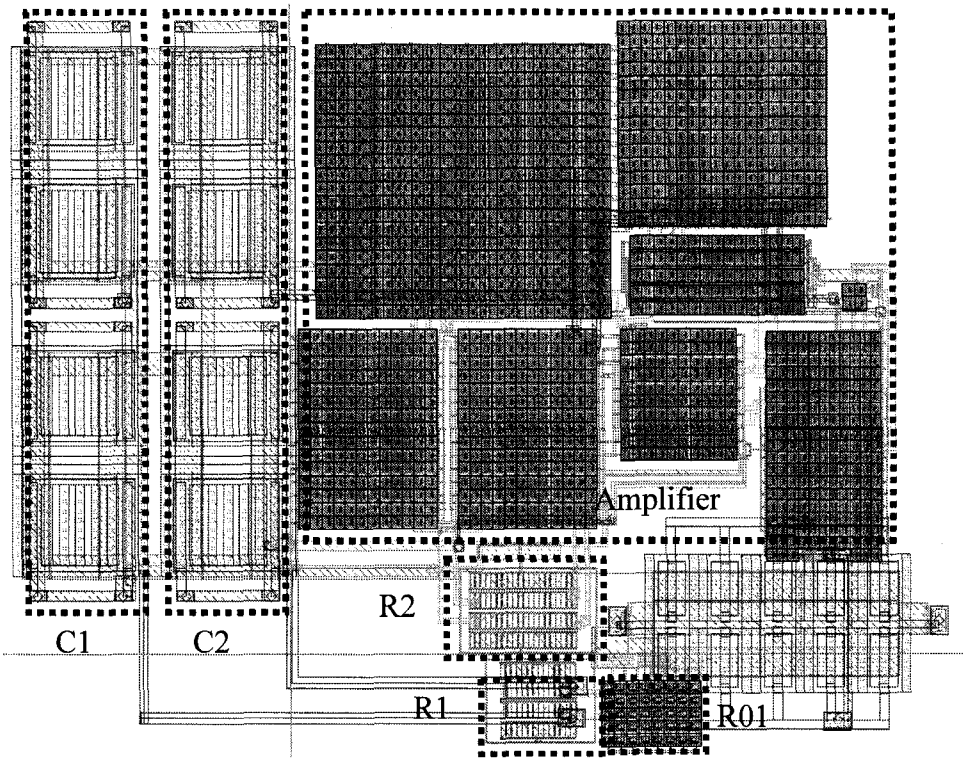


Figure 5-16: Layout of the active-RC filter in CMOS 0.13μm.

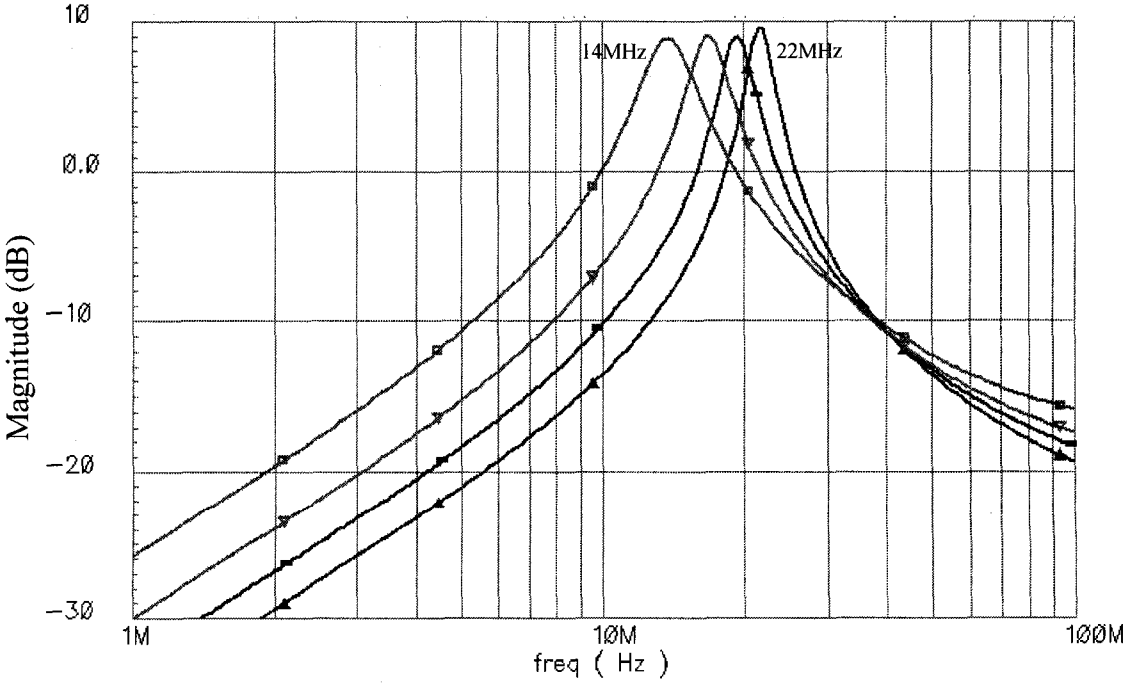


Figure 5-17: Frequency response of the active-RC filter for various center-frequencies.

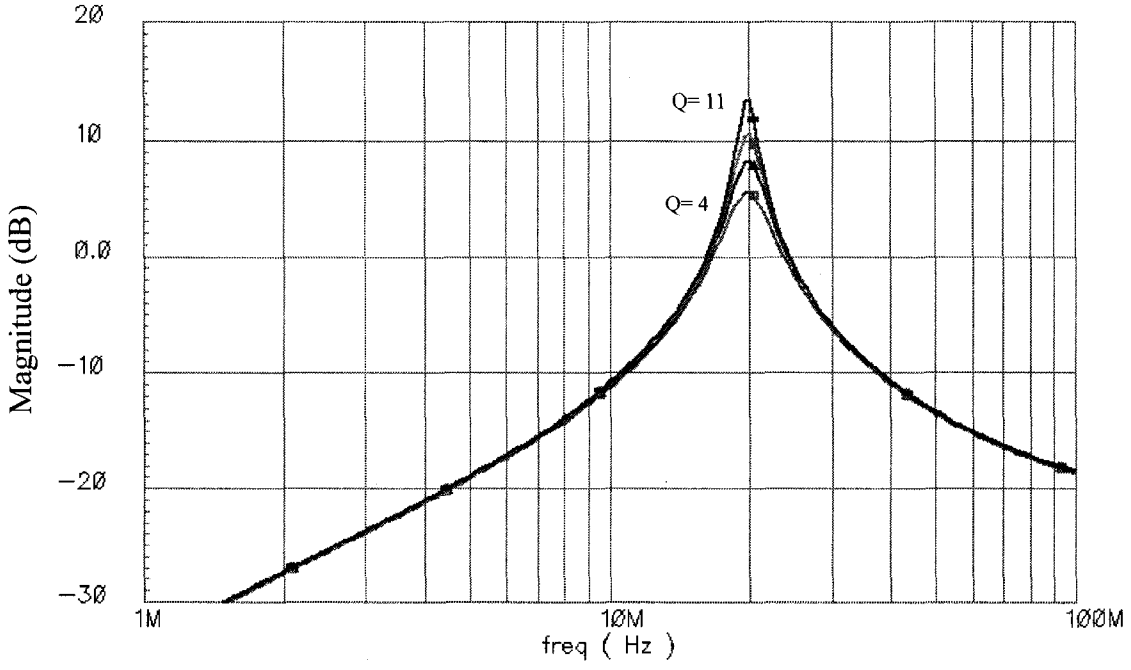


Figure 5-18: Frequency response of the active-RC filter for various Q-factors.

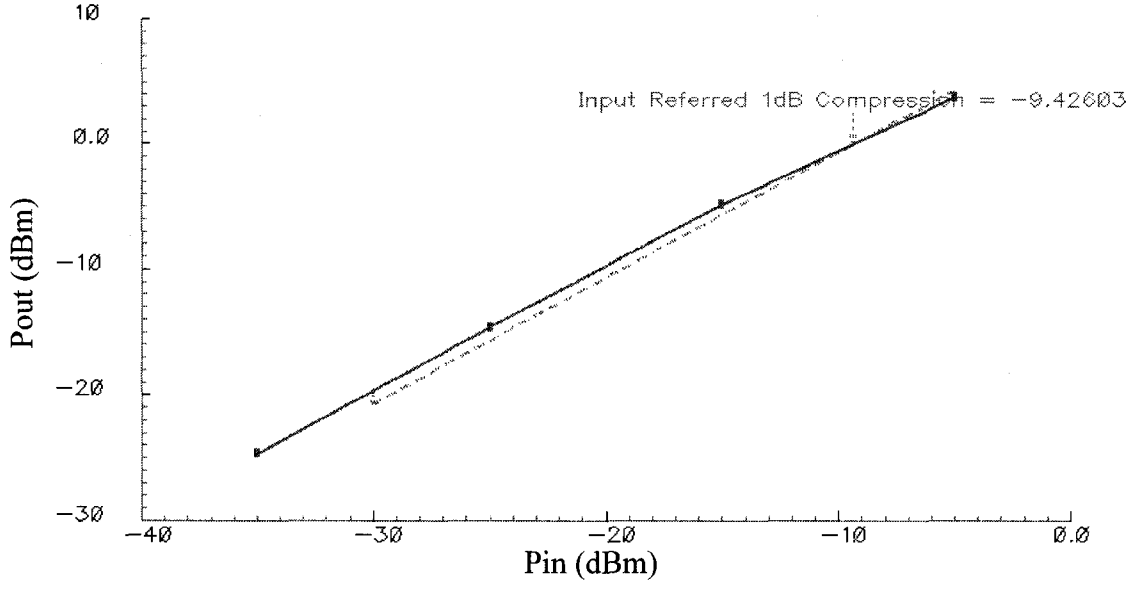


Figure 5-19: Simulation result for 1-dB compression point in the active-RC filter.

Table 5.4: Simulated characteristic performance of the filter and comparison.

Characteristic	Design			
	[57]	*[31]*	*[38]*	***This work***
Technology (μm)	0.18	0.25	0.35	0.13
Filter type	Gm-C	Active-RC	Active-RC	Active-RC
Power supply (V)	±0.9	2.5	1.5	1.2
Pd/order (mW)	2.6	9.25	NA	2.3
Center freq. (MHz)	10 – 126*	2	10.7	14 - 22
Q-factor	0.1-10.6*	2-7	32	4 - 11
1-dB compression point (dBm)	Not available	Not available	Not available	-9.4

*The range is not continuous

5.4. Experimental Results

The delta modulator shown in **Figure 5-2** was fabricated by IBM 0.13μm CMOS technology. The micrograph of the chip is shown in **Figure 5-20**. It occupies 0.7mm x 1.42mm = 1 mm^2 on silicon including pads. In order to test the chip, a test board was designed (Appendix C:). The fabricated modulator sinks total current of 31 mA (including buffers and clock) from supply voltage of 1.2 V. Hence, the total power consumption is 37.2 mW. Before performing the main test, the modulator must be tuned for the second IF = MOD (f_{in}, f_{Ck}).

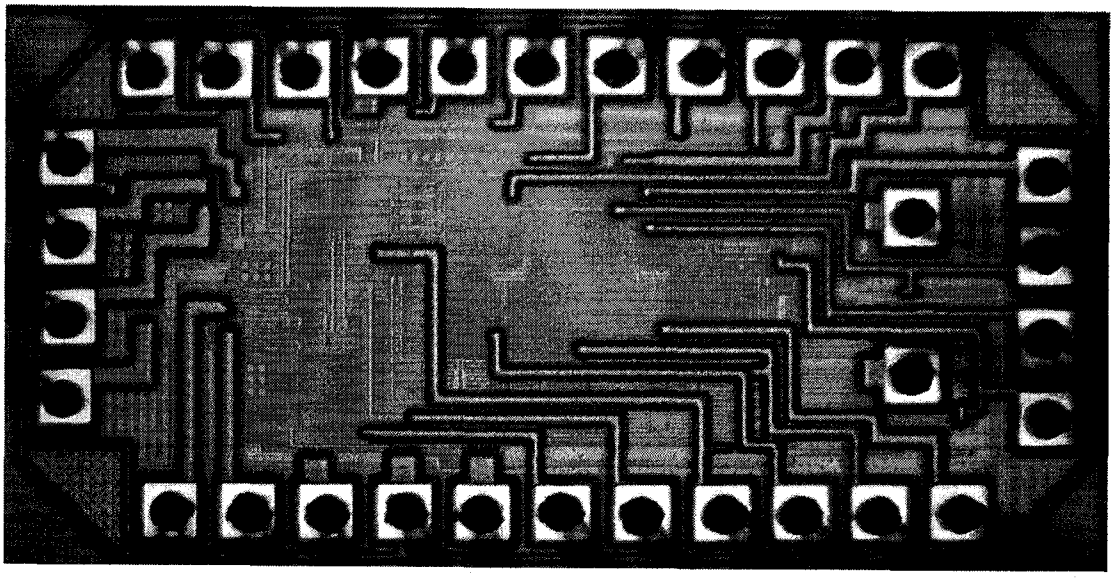
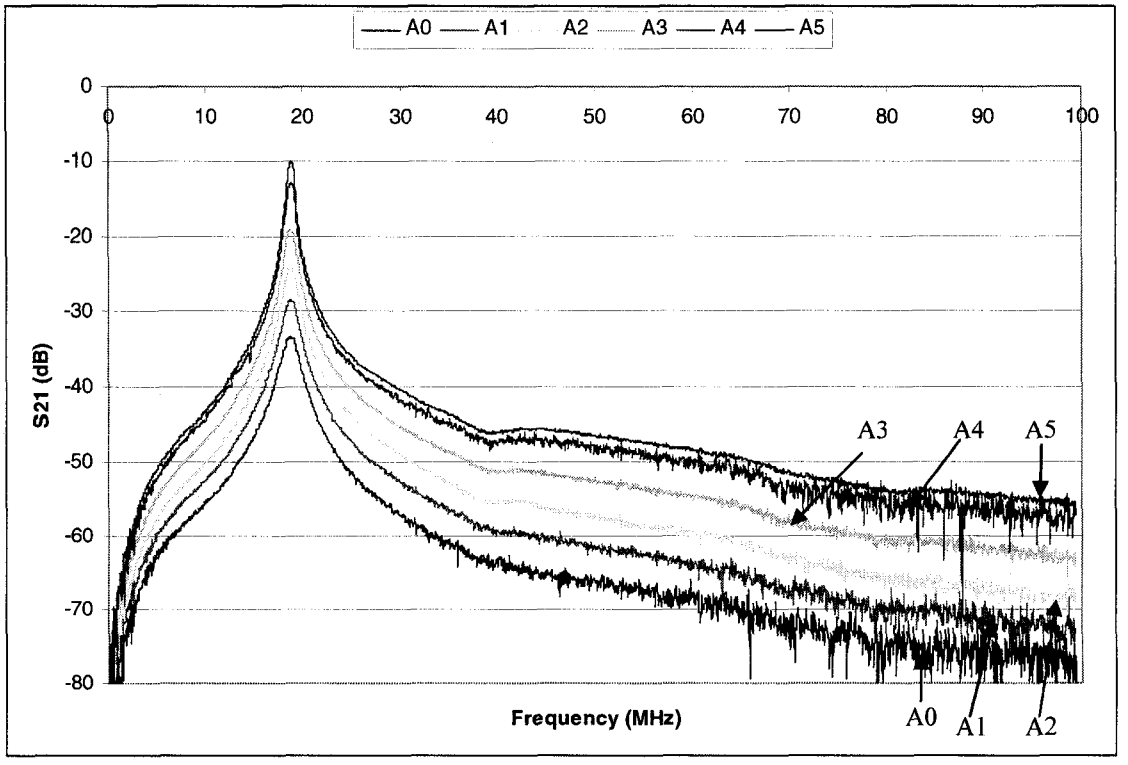


Figure 5-20: Microphotograph of the delta modulator.

The tuning can be done by using the network analyzer for a S21 test. The S21 curve shows the transfer function of the filter and by using the control voltages we can set the desired center frequency and Q-factor for the both filters. An HP8753 network analyzer was used to characterize the filters. The Qf control current was adjusted from 67μA to 105μA (injecting larger currents may reduce the reliability) to obtain the Q-factor (**Figure 5-21**). The output of the filter is buffered and the filter gain shown in the figure is somewhat different from the filter gain in the loop. Also, there is some loss due to the Balun to convert the single source to the differential signal.

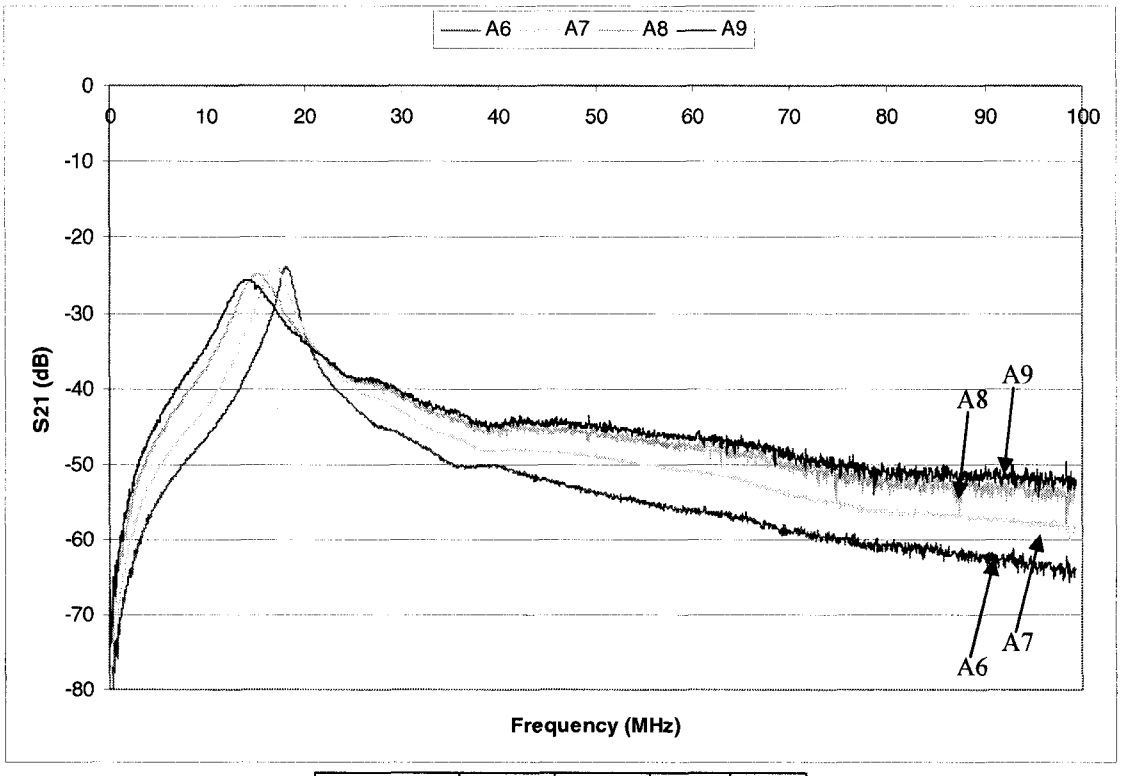
The effect of center frequency tuning by the control voltage, Vf, is presented in **Figure 5-22**. A frequency span of 5.6MHz (30%) was obtained when Vf varies between 1V to 1.61 V.



	A0	A1	A2	A3	A4	A5
Iq (μA)	67	73	78	87	99	105
Q	10	13	15.5	17.5	21	25

Figure 5-21: Q-factor tuning measurements of the 2nd-order filter.

After tuning the filters at center frequency of 19.5 MHz, the input power was swept from -25 dBm to -2 dBm to measure the 1-dB compression point at -3.6 dBm (**Figure 5-23**). **Figure 5-24** shows the output power spectrum of the modulator using HP8593 spectrum analyzer, when the input frequency is 2019.5MHz and clock frequency is 500MHz (off-chip clock is 1GHz). The bandwidth of the filter is set to 1MHz at center frequency of 19.5MHz. The maximum SFDR is measured 25dB for maximum input power of -10 dBm.



	A6	A7	A8	A9
Vf (V)	1.61	1.51	1.1	1
fc (MHz)	19.6	18.1	15	14

Figure 5-22 : Center frequency tuning measurements of the 2nd-order filter.

During the test, we realized that the noise of the on-chip power supply is large enough to produce an oscillation in the clock path. However, by applying the clock signal to the chip, the oscillation stopped and system could operate normally. However, that noise can exacerbate the phase noise of the clock signal, and consequently, decrease the output SFDR. The noise shaping seen in **Figure 5-24**, presents the functionality of the modulator at presence of large supply noise and large jitter power in the clock.

We identified a few reasons for the noise on the chip and reduction of the output SFDR. First, the board designed for the testing, loads the modulator with parasitics that

have larger values than those we had considered in the simulations. The bonding wires of the package also exacerbate this effect, and the on-chip decoupling capacitors are not sufficient to reduce the power supply coupling as needed.

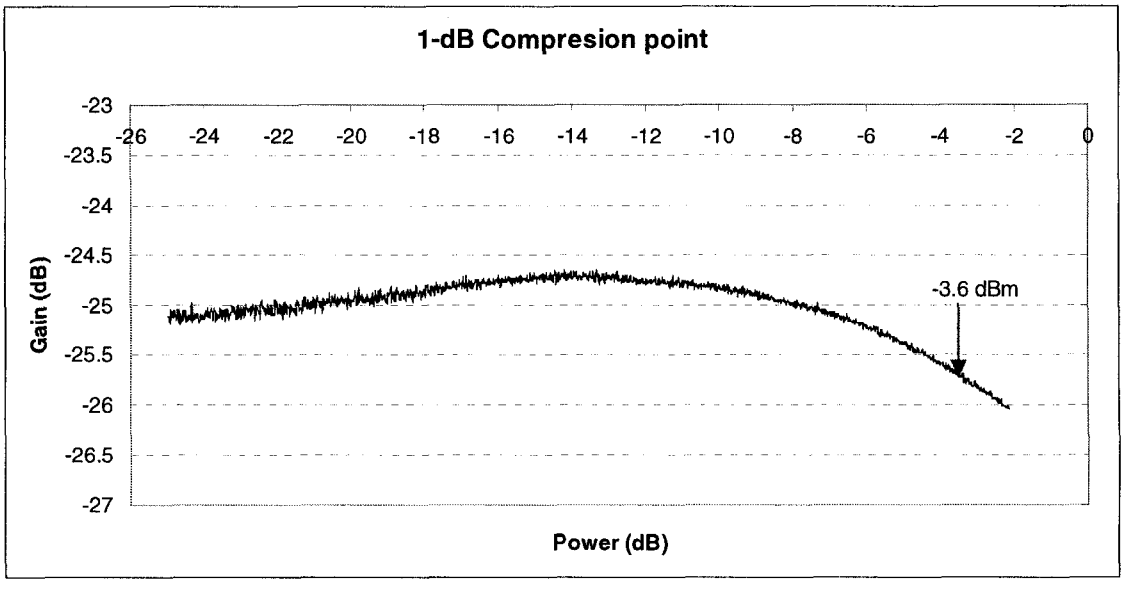


Figure 5-23: Input 1-dB compression point measurement.

Furthermore, the output bit rate is 500MS/s and it requires a large bandwidth on the board. Otherwise, the spectrum analyzer cannot capture the high frequency terms of the output signal and does not show the correct spectrum. Although we have used a wide band balun for converting a differential signal to a single output (to be matched with spectrum analyzer), the characteristic of the Balun changes during such a wide frequency band and inserts different attenuations for the signal harmonics.

The modulator can convert the input signals in a very wide frequency range of 500MHz to 2.6GHz only by changing the clock frequency as long as the IF = MOD (f_{in} ,

f_{CK}) is kept valid. **Figure 5-25** shows the SFDR of the output signal versus input power. The maximum SFDR is achievable at input power of -10dBm.

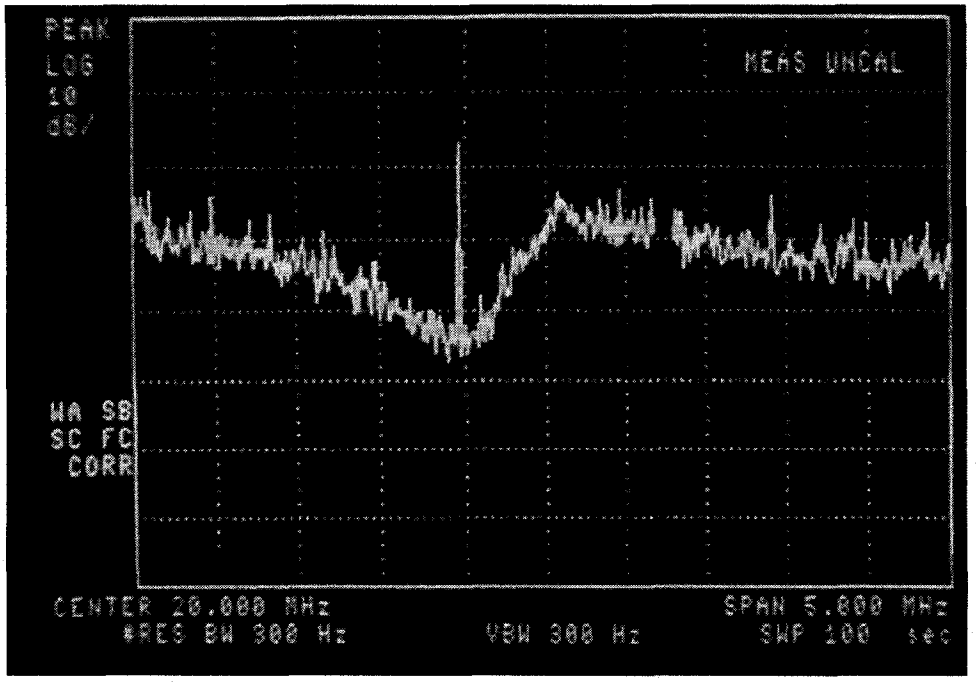


Figure 5-24: Output power spectrum of the modulator.

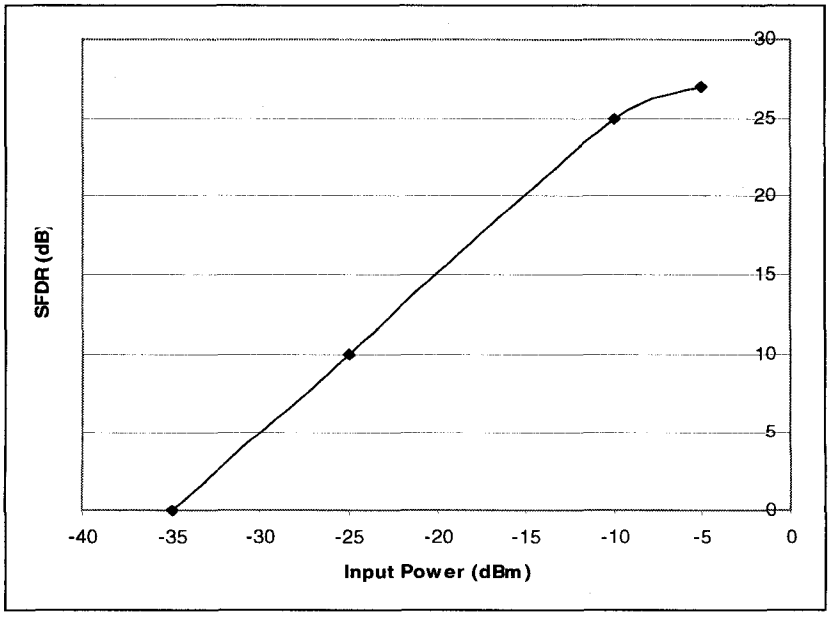


Figure 5-25: the SFDR versus input power.

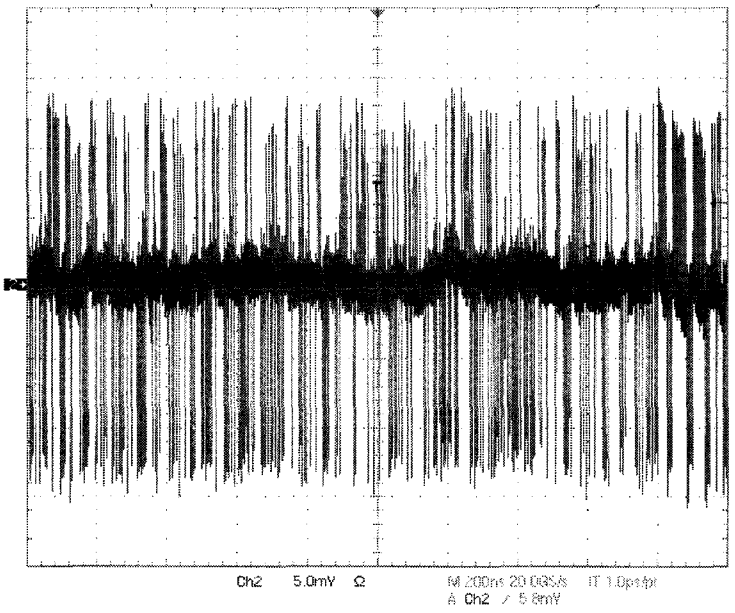
A time-frame of the modulator output signal was captured using a Tektronix TDS7154 digital oscilloscope, and is shown in **Figure 5-26**. Summary of experimental results of the filter and DM are given in **Table 5.5** and **Table 5.6** respectively.

Table 5.5: Summary of measured results in the filter.

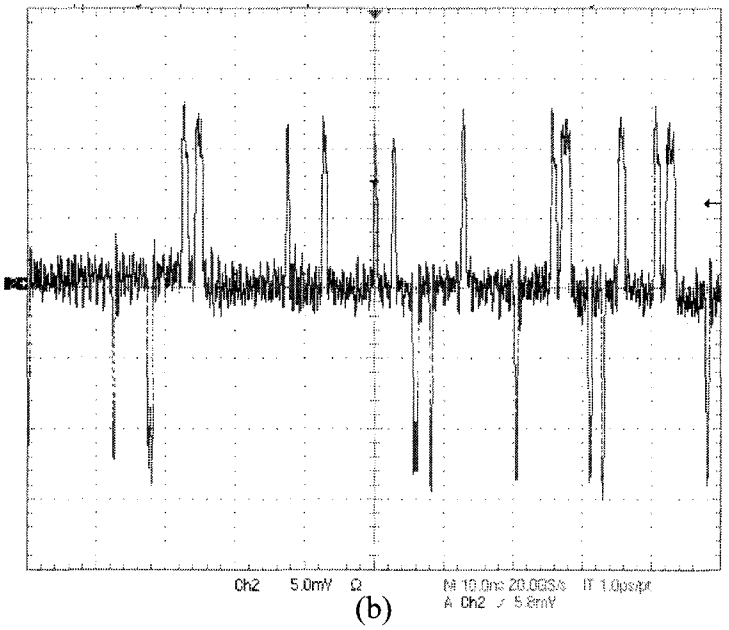
Characteristic	
Technology (μm)	0.13
Filter type	Active-RC
Power supply (V)	1.2
Center freq. (MHz)	14 – 19.6
Q-factor	10 - 25
1-dB compression point (dBm)	-3.6

Table 5.6: Summary of measured results in Delta modulator.

Characteristic	
Input frequency range	0.5-2.6 GHz
Nominal Input frequency	2.0195 GHz
Signal bandwidth	0.5 MHz
Sampling frequency	500 Ms/s
IF	19.5 MHz
Vdd	1.2 V
Pd	37.5 mW
Peak SFDR	25 dB



(a)



(b)

Figure 5-26: (a) The modulator output signal in time domain. (b) Magnified.

5.5. Conclusion

Based on the design trend in the previous chapters, which looks for RF signal digitization, a DM using undersampling was proposed in block diagram level and circuit level for radio frequency receivers. The proposed modulator overcomes the limitations we faced in DSM, such as filter design, Q-factor, and the upconversion in the feedback path. Low-voltage requirements in the advanced CMOS technologies along with linearity issues were discussed, and associated solutions were proposed in the circuit design to boost maximum input frequency to 2.6 GHz. Post-layout simulation and experimental results of the DM were presented in IBM 0.13μm CMOS technology. The total power consumption of the modulator was less than 37.2 mW when the supply voltage is 1.2V. The input frequency range was measured to be between 500MHz and 2.6GHz. The measurement results of the bandpass filter were found to be consistent with simulation results.

Chapter 6

General Conclusion and Future Works

In this thesis, several novel ideas were presented to help improve the design of delta sigma modulators and delta modulators in radio frequency receivers. Contributions were made at system level and circuit level.

The use of upsampling in the feedback path of the undersampling delta sigma modulator was proposed in chapter 4. A set of design equations applicable to this architecture was developed as well as key circuit techniques needed to implement it. The proposed design can be used in receivers with no analog mixer to digitize signals modulated over high frequency carriers. Using a continuous-time modulator, noise and nonlinearity of the S/H are shaped together with the quantization noise and attenuated by the system. Matching of digital IF with analog IF is carried out using upsampling in the digital side. The proposed modulator has no excess loop delay due to delay tuning by sampling rate. This was shown by design equations, which were derived by Laplace form of each block. Such method in design of DSM was proposed by investigating design approaches and techniques to realize an ADC for gigahertz signals and receivers dedicated to software defined radio applications. Advantages of delta sigma modulators over other types of ADCs were discussed, and it was shown that removing the analog mixers could improve the compatibility of the receiver with different communication standards. Hence, the design challenges of the continuous time modulators were

explained for input frequencies of the order of 2GHz. It was also supported by a survey of the literature and a presentation of the state of the art, which showed two variations in high frequency delta sigma modulators: ultra high sampling and undersampling. These variations present a trade-off between power consumption because of the high sampling rate and complexity of the design due to undersampling. By considering the fact that the target application requires low power consumption to boost portability, a novel delta sigma modulator based on undersampling was proposed for input frequency of 1.8GHz. The simulation showed that the proposed design could convert the input signal into digital data with a SFDR of 46 dB at a sampling frequency of 810.1 MHz and a low supply voltage of 1.2V using a 0.13μm CMOS technology. The total power consumption was estimated to be less than 22mW with a supply voltage of 1.2V. The design method can be applied to develop higher order modulators that would produce higher SNR.

This design was further developed to a new delta modulator to receive a wide range of input frequencies and to facilitate design of the bandpass filter block. Based on the application introduced in chapter 2, which looks for RF signal digitization, a DM using undersampling was proposed in block diagram level and circuit level for radio frequency receivers. The proposed modulator overcomes the limitations we faced in DSM, such as filter design, Q-factor, and the upconversion in the feedback path. Low-voltage requirements in the advanced CMOS technologies along with linearity issues were discussed, and associated solutions were proposed in the circuit design to boost maximum input frequency to 2.6 GHz. By using undersampling in the forward path a second IF is defined at 20MHz. Therefore, all input frequency can be tracked by

changing the sampling frequency of the modulator, in which the second IF be fixed at 20 MHz. The delta modulator is using a 4th-order bandpass filter in the feedback path at center frequency of 20 MHz. Design equations were explored to get the maximum output SFDR in the modulator. Post-layout simulation and experimental results of the DM were presented in IBM 0.13μm CMOS technology. The total power consumption of the modulator was less than 37.2 mW when the supply voltage is 1.2V. The input frequency range was measured to be between 500MHz and 2.6GHz.

6.1. Future Work

This thesis paves the way for several research topics. Based on conclusion in chapter 2, RF DSMs are needed in communication systems. Bandwidth required in the new standards such as WiMax demands up to 20MHz in some cases. Therefore, wideband delta sigma modulator design using the proposed technique for the DSM is an open research. Although the bandwidth of the proposed design is much wider than most of communication standards like WCDMA, but the proposed method is a base method and can be developed for new applications.

We used a 2nd-order continuous-time DSM to prove the proposed concept. Such architecture is not intended for high resolution DSM. Therefore, and interesting work is to apply the proposed method to high-order or multi-bit DSM to achieve high resolution output signal. This work can extend application of the DSM to more communication standards.

One way to increase the resolution of the modulator is to use a multi-bit quantizer with multi-bit feedback using proposed DSM. Such a method requires a new research on improving linearity of the system.

One advantage of the proposed DSM is ability to control process and temperature digitally. Implementation of that is a new work, which can boost the performance.

As we mentioned in chapter 4, bandpass filters with very high Q-factor are required in RF DSM. Although, they are design to be tunable in center frequency, an automatic tuning system is required to keep them tuned in spite of process-voltage-temperature variations (PVT). This is an open problem and demands more research to perform an automatic Q-factor and center frequency tuning.

During measurement of the results, we found that the system is sensitive to power supply noise, which is due to mixed-signal design. Hence, more research to resolve signal integrity and power supply noise will be beneficial.

Power optimization of the DSM and working with even lower supply voltage to support the most advance CMOS technologies, requires new design ideas. Using BiCMOS technology is recommended, which can even result increasing the input frequency by getting better performance in sample-and-hold and quantizer.

In the designed modulators, output data rate is at the order of a few hundred MSps. This is an issue in test step. More work is needed in testing method. Other solution can be recommended, is design of on-chip filters and decimation blocks to reduce output data rate.

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Appendix A:LC Bandpass filter

The design presented in section 4.2 and **Figure 4-6**, was based on a negative conductance generated by transistors shown in. Any positive feedback can compensate lost energy, and, therefore, can be used for Q-enhancement purposes. There are a few other methods which have been reported to enhance the Q-factor of high frequency band-pass filters [98]. The main idea in several designs is to have a magnetic coupling between two inductors to achieve Q-enhancement in a LC tank. In coupled inductors, drop voltage over the primary inductor is expressed by:

$$V_{L1} = R_1 i_1 + jL_1\omega i_1 + jM\omega i_2 \tag{A-1}$$

where, i_1 and i_2 are currents in the primary and secondary coils,. L_1 is the inductance of the primary coil and M is the mutual inductance of the two coils. If $i_2=-R_1 i_1/(jM\omega)$ then the resistive term becomes zero and V_{L1} and i_2 are:

$$V_{L1} = jL_1\omega i_1 \tag{A-2}$$

$$i_2 = -\frac{R_1}{\omega^2 L_1 M} V_{L1} \tag{A-3}$$

This relation shows that the loss in the LC tank can be compensated by adjusting the current in the secondary inductor. **Figure A-1** shows a LC band-pass filter implemented as a differential structure based on the described loss compensation method. L1 and L2 are the primary inductors, and L2 and L4 are the secondary ones. The currents of the latter are linked to the primary voltages by gm of transistors M1 and M2. Input signal is applied through a differential pair. Another differential pair can enter the

feedback signal into the modulator through the filter. A control voltage (Vc) is used to adjust gms of M1 and M2. Two diode varactors can also be used as the capacitor of the tank (C), which is used to tune the filter center frequency. The output of the filter is then buffered to increase the S/H's bandwidth.

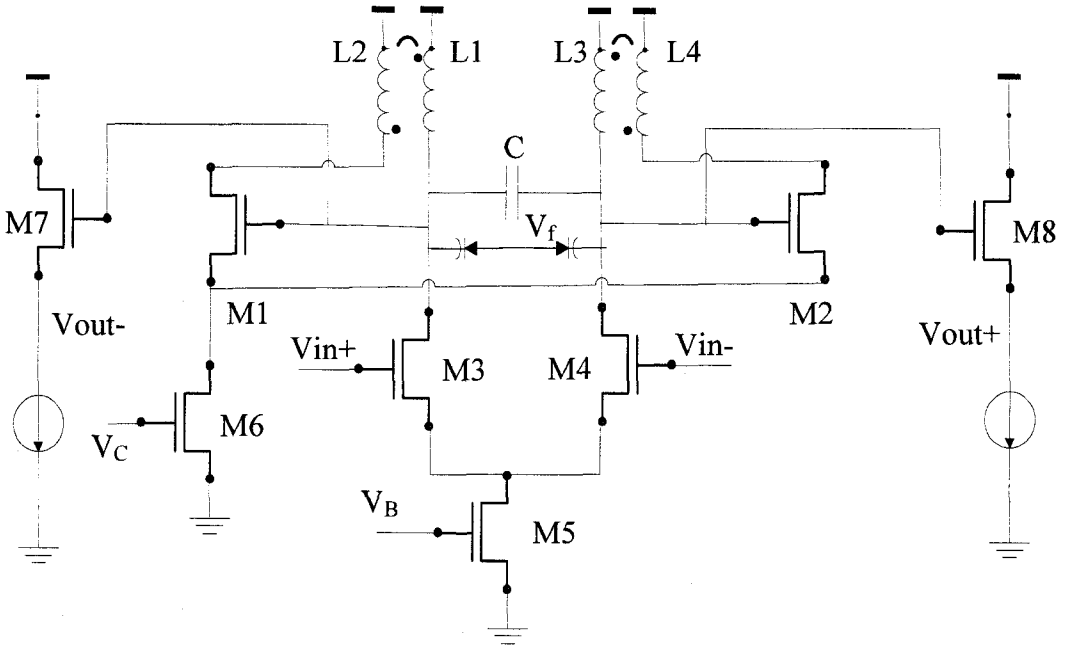

Figure A-1: Q-enhanced LC band-pass filter.

Appendix B:Amplifier Design and Compensation Methods for Continuous-Time Filters

The numerous and increasing challenges in the advanced sub-180nm technology include device variability, body effect, stress-induced mobility degradation, increase of junction capacitor, increase of threshold to supply voltage ratio, reduction of effective voltage, power consumption, sub-threshold leakage, gate induced drain leakage, and drain induced barrier lowering [112]. These problems must be considered in advance in circuit design to tape out successfully. Some challenges like reduction of supply voltage can even limit designs to use some popular architecture like cascode [61]. This leads to the use of only one simple amplifier in each stage to cope with low voltage supply. On the other hand, there is a growing demand for high gain wideband amplifiers. Consequently, multistage amplifier design is becoming more popular, and is used in many successful designs [61][115][18][64][84][118][28][116]. However, multistage amplifiers require a frequency compensation scheme to be stable in feedback systems. Hence, many frequency compensation topologies have been studied to alleviate instability issues[77][59][50][85][117][82][69][62]. **Figure B-1** shows simple miller compensation (SMC) topology in a two-stage amplifier. According to the Miller theorem, the capacitor first stage amplifier sees a capacitance of C1 = Cm (1+Av2) that in series with output resistance of first-stage amplifier produces the dominant pole of the system. Therefore, the non-dominant pole is placed at the output stage with a capacitance of C2 = CL+Cm. In another word, using a relatively small capacitor, Cm, the dominant is controllable to meet desirable performance in term of phase and gain margins. However,

the compensation capacitor produces an extra forward path for the signal that makes a right-half-plane (RHP) zero. The zero reduces stability and bandwidth of the amplifier.

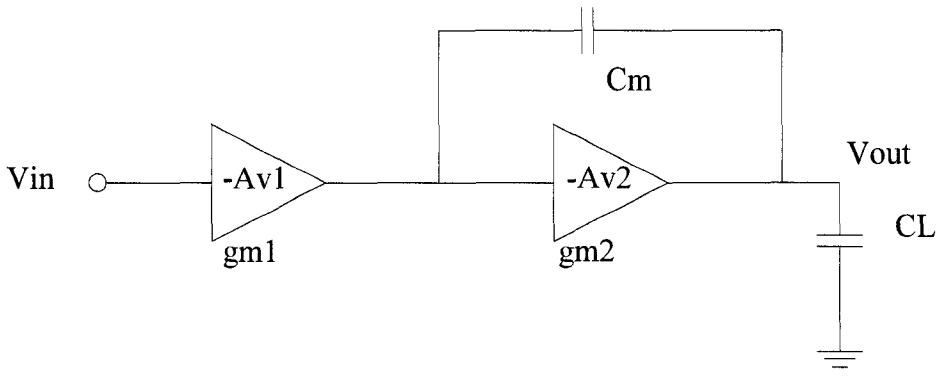

Figure B-1: Simple miller compensation.

In order to remove the right-half-plane zero in the SMC topology, a resistor can be added in series with the Cm, in which impedance of the forward path increases and effect of the RHP zero decreases. This nulling resistor also has effects on the place of the pole and, in fact, by increasing nulling resistor to infinity, the compensation path becomes an open circuit and the compensation network fails [61]. Therefore, nulling resistor can move RHP zero to higher frequencies and is a useful technique for phase margin (PM) improvement. The other method to remove that RHP zero is using a voltage follower or current follower in the compensation network [107]. The forward path is, therefore, blocked by the buffer, and it removes the RHP zero.

Another approach for frequency compensation of a multi-stage amplifier called multi-path compensation is shown in **Figure B-2** for a two-stage amplifier. In contrast with the Miller method, there is a forward path used to produce a left-half-plane (LHP)

zero that can compensate or alleviate the effect of the second pole of the system. In this case, the transfer function can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}R_1R_2 + g_{m3}R_L(1+R_1C_1s)}{(1+R_1C_1s)(1+R_2C_2s)} \tag{B-1}$$

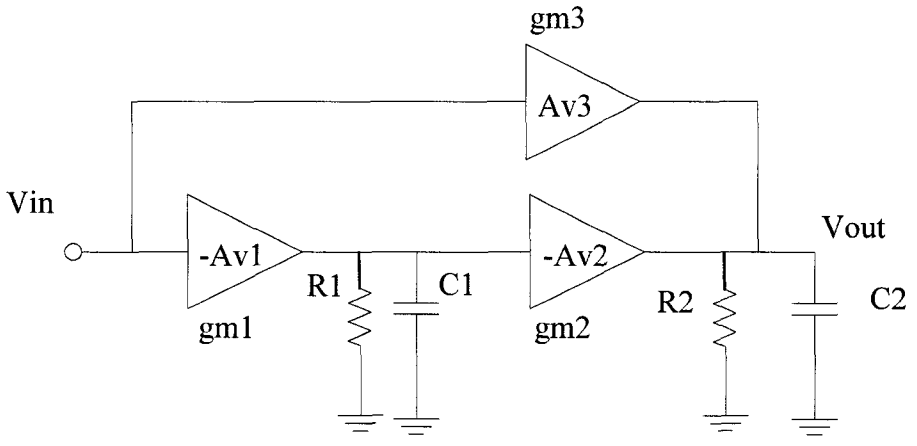

Figure B-2: Multi-path compensation topology.

Another stage can be added to the topology shown in **Figure B-2** as a buffer to drive the output load. In comparison with other phase compensation techniques like Miller capacitance, this scheme does not push the dominant pole to the lower frequencies and increases the bandwidth of the amplifier. There are, however, more variations of the above method that uses both feed-forward path and Miller capacitor as shown in **Figure B-3**. The difference is actually due to the operating conditions where load capacitor may be high and buffer at the load stage adds other requirements to the design equations. This comes up with more complexity when minimum power consumption is of interest. Then

it needs to consider all critical paths and nodes to develop a new topology as many schemes have been studied in the literature [61].

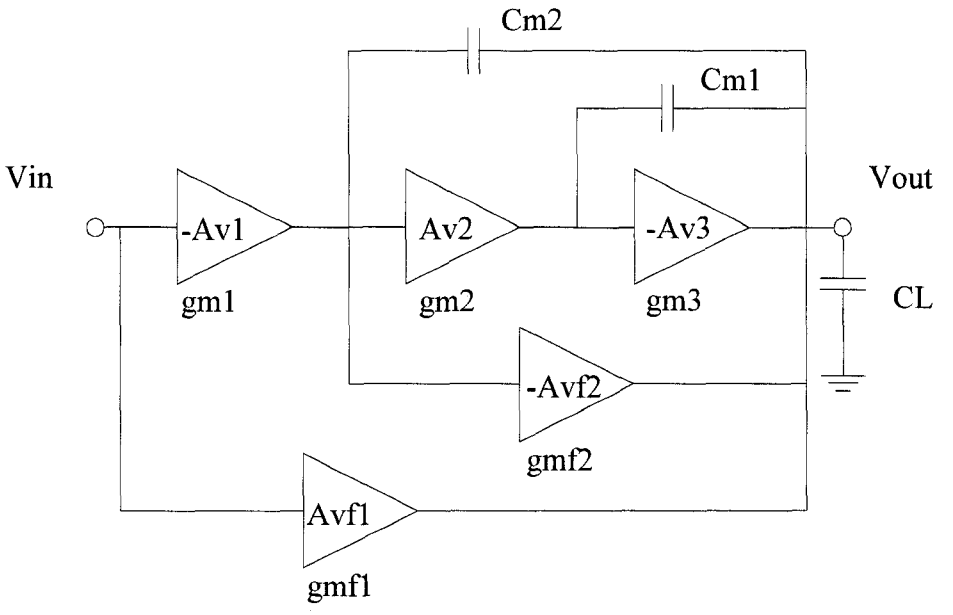

Figure B-3: Nested Gm-C compensation topology.

Appendix C: Test board

A custom board was design for testing because there are both high and low frequency signals available on the board. Furthermore, source signals are single-ended and must be converted to differential to be compatible with the inputs of the chip. This is also valid for the output that has a differential 495 MHz PCM format. However, the transmission line of the output must have enough bandwidth to pass several harmonics of the fundamental frequency.

When transmission line length is much less than signal wave length, λ, the reflection due to impedance mismatch is negligible. In our board, the maximum frequency could be 2 GHz, and λ=15 cm. Therefore, impedance matching is important in term of both maximum power transfer and reflection. Regarding all RF sources are terminated by a 50 ohm resistance, the microstrips on the board must also design for 50 ohm characteristics impedance. This can be carried out using some tools such as ADS-linecalc. However, for a mirostrip line as shown in **Figure C-1**, we can calculate the ratio of width of line to thickness of the substrate as follows:

$$\frac{W}{d} = \begin{cases} \dfrac{8e^{A}}{e^{2A}-2} & \dfrac{W}{d} < 2 \\ \dfrac{2}{\pi}\left\{B - 1 - \ln(2B-1) + \dfrac{\varepsilon_r - 1}{2\varepsilon_r}\left[\ln(B-1) + 0.39 - \dfrac{0.61}{\varepsilon_r}\right]\right\} & \dfrac{W}{d} > 2 \end{cases} \tag{C-1}$$

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left[0.23 + \frac{0.11}{\varepsilon_r}\right] \tag{C-2}$$

$$B = \frac{377\pi}{2Z_0\sqrt{2\varepsilon_r}} \tag{C-3}$$

Where Z_0 is the characteristic impedance of the line.

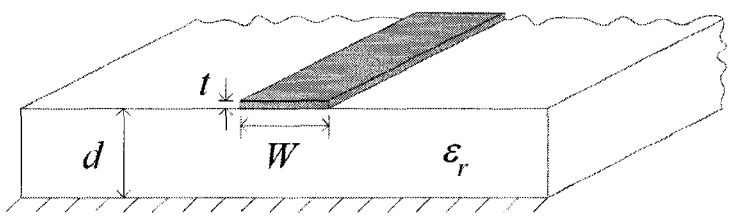

Figure C-1: Microstrip line.

The schematic and layout of the test board is shown in **Figure C-2**, and **Figure C-3** respectively.

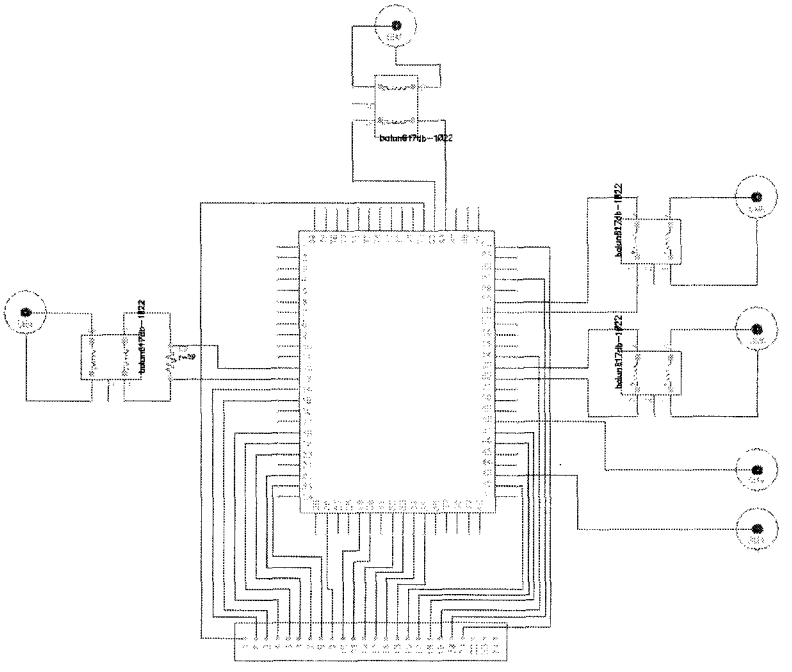

Figure C-2: Schematic of the testboard.

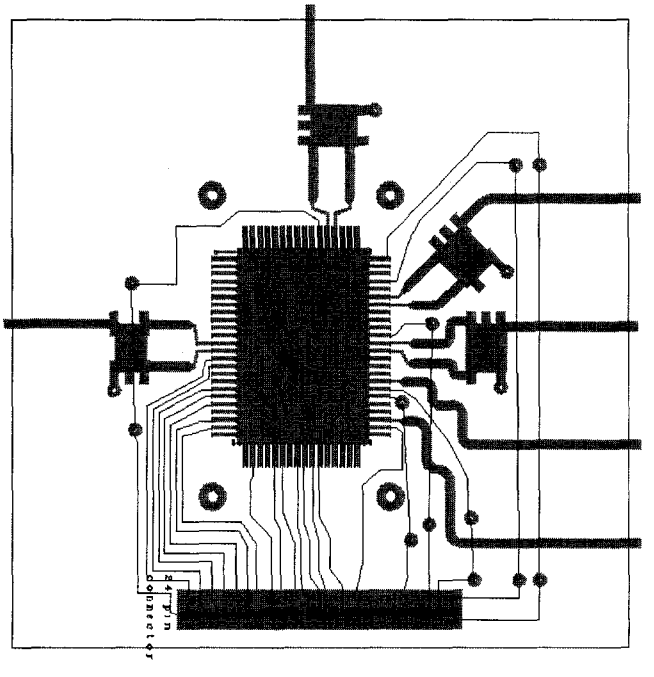

Figure C-3: Layout of the testboard.