UNIVERSITÉ DE MONTRÉAL

# ANALYSIS AND CHARACTERISATION OF DESIGN FOR TESTABILITY METHODOLOGIES FOR BIPOLAR CURRENT MODE LOGICS

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MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION
DU DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES
(GÉNIE ÉLECTRIQUE)
JUILLET 2002

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Ce mémoire intitulé:

ANALYSIS AND CHARACTERISATION OF DESIGN FOR TESTABILITY METHODOLOGIES FOR BIPOLAR CURRENT MODE LOGICS

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en vue de l'obtention du diplôme de: Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de:

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## ACKNOWLEDGEMENTS

I sincerely thank Dr. Yvon Savaria for the excellent guidance given throughout the project. His continuous encouragement and feedback has been of great value in accomplishing this task. He has been quite supportive in both the professional and personal aspects of my life. I express my sincere thanks to him for changing my life for the better.

I wish to express my sincere thanks to Dr. Pieter Trouborst of Nortel Networks, for the excellent guidance and valuable feedback given throughout the project. He was available whenever I needed him. Thank you for the excellent support, Sir. Also thanks for providing me the opportunity to work as a coop student at Nortel Networks.

I thank Bernard Antaki for mentoring me at the initial stage of my work. I would like to thank Ginette Monté for developing tools that enabled quick completion of the task on hand. I would like to thank the Canadian Microelectronics Corporation (CMC) for their tool supply and support. I would like to thank my colleagues at GRM for all the useful discussions we have had.

I extend my special thanks to friends and family for their continuous support, without whom this may not have been possible.

# RÉSUMÉ

Le test des familles CMOS a largement retenu l'attention de la communauté scientifique En effet les CMOS constituent la technologie dominante à cause de sa faible consommation de puissance et de sa grande densité d'intégration. Cependant, les familles logiques en mode courant (Current Mode Logic, CML) implémentées avec des technologies bipolaires, ont continuellement occupé des secteurs lucratifs tels que celui des circuits très rapides. L'évolution technologique a permi la réalisation de procédés bipolaires de basse puissance et haute densité. Ceux-ci, combinés avec la propriété d'opération à haute vitesse des circuits logiques CML bipolaires, en fait un excellent choix pour les applications qui opèrent à très haute vitesse. Comme aucun procédé de fabrication n'est parfait, le test de ces circuits est indispensable. Mentionnons que très peu de documentation existe sur les méthodes de test applicable aux technologies ECL ou CML. Les méthodes de test proposées pour des procédés CMOS ne peuvent souvent pas être directement transférées aux procédés CML bipolaires. Par conséquent, il est important d'étudier la testabilité des logiques CML bipolaires. L'objectif principal est d'éviter le recours aux tests à pleine vitesse, jugés coûteux. La conception pour la testabilité (Design For Testability, DFT) est utilisée pour réduire les coûts de génération de tests et augmenter la couverture de pannes.

Une équipe de recherche précédente a déjà identifié des défauts possibles avec la famille logique CML bipolaire, et a proposé des méthodes de test pour les détecter. Ce mémoire

étudie la propagation des défauts et la dégradation de performance de la famille logique CML bipolaire. Nous avons choisi un type de défectuosité appelé pont qui a un impact fort sur le comportement d'une porte logique CML et nous avons analysé la manière par laquelle elle se propage à travers les chaînes de portes. Cette étude nous a permis de saisir à quel point ces défauts peuvent dégrader la performance des portes CML.

Ce mémoire étudie aussi en détail deux des méthodes de test déjà publiées, afin de déterminer leur compatibilité avec les logiques CML bipolaires. La première méthode de test diminue le rendement. Réciproquement, il se peut qu'elle n'identifie pas les circuits défectueux. En effet, nous montrons pourquoi ce n'est pas une technique pratique pour les procédés CML bipolaires. La deuxième technique de DFT ne peut pas être directement appliquée à cause des contraintes de conception. Nous discutons également des manières de surmonter ces obstacles, afin de rendre ces techniques de DFT faisables. Un ensemble de règles de conception est conçu pour améliorer la testabilité des logiques CML bipolaires. En mode test, nous analysons les effets des méthodes de DFT et des facteurs environnementaux sur la tension de sortie des CML bipolaires.

Une puce de test conçue par une équipe précédente et fabriquée par Nortel est examinée. La génération de vecteurs de test pour cette puce de test est discutée, ainsi que certains résultats de tests préliminaires déjà disponibles. Cette puce est considérée une plate-forme d'évaluation des techniques de DFT proposées et appliquées aux portes CML bipolaires. Des méthodes de test, déjà proposées et mises en application dans la puce de

test par l'équipe précédente, ont été modifiées sur la base de nos travaux de recherche. Cependant, les principes de base des méthodes de DFT appliquées demeurent toujours inchangées. Par conséquent, les résultats de test de la puce de test sont très importants, dans la mesure ou ils permettent l'évaluation de la performance des structures DFT. La performance des portes CML bipolaires, en présence des défauts de fabrication, est bien caractérisée dans cette étude. En outre, on propose un ensemble de règles de conception pour la testabilité de ces portes CML bipolaires.

# ABSTRACT

CMOS logics have had much of the scientific communities' attention owing to their low-power and high-density characteristics. However CML logic families implemented with bipolar technologies have continuously occupied lucrative niches such as very high-speed circuits. Advancements in technology have lead to the realisation of high-density, low power bipolar processes. This combined with the high-speed property of bipolar Cols, makes them an excellent choice for high-speed applications. Since no manufacturing process is perfect, testing these logics is important. Very little specific literature exists on the testability of bipolar CML gates. Design For Testability (DFT) methods proposed for CMOS processes cannot be directly transferred to bipolar CML processes. Therefore, it is important to study the testability of bipolar CML logics. The main objective is to obviate the need for expensive at-speed testers. DFT is used to reduce test generation costs and enhance the fault coverage of tests.

A previous research team has reported defects possible with bipolar CML logic families, and test techniques to detect these defects. This thesis studies fault propagation and performance degradation for a bipolar CML logic family. We chose a bridging defect type that has strong impact on the behaviour of a CML logic gate, and we analysed how it propagates through gate chains. This study helped us understand how defects can degrade CML gates' performance.

This thesis also studies two of the reported test techniques in greater detail to determine their suitability for bipolar CML logics. The first test method decreases the yield. Conversely, it may also not be able to identify defective circuits. We show why this is not a practical DFT technique for bipolar CML processes. The second DFT technique cannot be directly applied due to design constraints. We also discuss ways to overcome these obstacles, thus developing practically feasible DFT techniques. A set of design guidelines is devised to enhance the testability of bipolar CML logics. In the test mode, we analyse the impact on the output voltage of bipolar CML by the DFT method due to changes in environmental factors.

A test chip designed by a previous team has been fabricated by Nortel and is being tested. Test pattern generation for this test chip is discussed, together with some of the preliminary test results available. This chip is an evaluation vehicle for the proposed DFT techniques for bipolar CML gates. Test techniques, originally proposed and implemented in the test chip by a previous team, have been modified based on our research. However, the basic principles of the implemented DFT methods still remain the same. Therefore, the test results from the test chip are useful in gauging the performance of the DFT structures. The performance of bipolar CML gates in the presence of manufacturing defects is well characterised in this study. Also a set of design rules is proposed for the testability of bipolar CML gates.

# CONDENSÉ EN FRANÇAIS

Historiquement, les familles logiques CMOS ont dominé grâce à leurs particularités de présenter une haute densité d'intégration ainsi qu'un faible consommation de puissance. Avec l'évolution technologique, les tailles des éléments bipolaires sont devenues de plus en plus faibles, et dans les applications qui opèrent à haute vitesse, la dissipation de puissance dynamique des portes bipolaires est devenue comparable à celles de type CMOS [27]. Les portes CML bipolaires sont utilisées dans les applications à haute vitesse, telles que le traitement des signaux, les communications par satellite, et les émetteurs/récepteurs de télécommunications.

L'utilisation avec succès des portes CML bipolaires dans les circuits VLSI complexes, nécessite l'application de méthodes de tests permettant de détecter leurs défauts de fabrication. Mentionnons que très peu de documentation existe sur leurs méthodes de test applicables aux familles bipolaires ECL ou CML. Les techniques de testabilité qui sont appropriées aux familles logiques CMOS sont moins adéquates pour les portes CML bipolaires [4, 29]. Étant donné qu'aussi bien les ECL que les CML, font parties des familles de logique non-saturées, certaines méthodes de testabilité proposées pour ECL peuvent être appliquées aux CML bipolaires.

La division microélectronique de Nortel Networks étudie la testabilité des portes CML bipolaires. La bibliothèque de conception NT25™ exploite un procédé bipolaire à haute performance. Dans la première phase du projet, Serge Patenaude et Bernard Antaki ont étudié les types de défauts possibles avec les portes CML bipolaires, et ont proposé aussi des méthodes de conception pour la testabilité (Design For Testability, DFT) qui permettent la détection de tels défauts. Cette thèse constitue une continuation de leurs travaux. Ginette Monté participe également à ces travaux.

Les techniques de conception par la testabilité (DFT) sont des méthodes de conception spécialement utilisées pour garantir la testabilité d'un dispositif. L'objectif principal de cette recherche est d'étudier la manière dont les défauts se propagent dans la famille CML bipolaire afin de déterminer leur contribution à la dégradation de la performance des portes CML bipolaires, et par conséquent, de concevoir des techniques de DFT permettant la détection de ces défauts de fabrication. Nous étudions, en détail, deux méthodes de test proposées par Patenaude et Antaki, qui sont applicables aux portes CML bipolaires. Un procédé de génération de vecteurs de test, qui utilise le flot de conception de Nortel et qui permet de tester une puce en appliquant toutes les méthodes de DFT qu'ils ont proposées, est décrit en détail. Certains résultats de test, déjà disponibles, sont présentés. Une des principales idées derrière la conception de telles méthodes de test pour les portes CML bipolaires est d'éviter, d'une part, le recours aux tests à pleine vitesse, qui sont coûteux, et d'autre part, l'utilisation d'un banc de tests fonctionnels à basse vitesse pour la détection des défauts de fabrication [9].

**Portes bipolaires CML**

La structure des portes bipolaires CML est définie au chapitre 1. La bipolaire CML est une famille de logique non saturée, purement différentielle. Un inverseur en logique CML bipolaire est présenté à la figure1. Un courant $I_1$ traverse le transistor $Q_1$ lorsque l'entrée 'a' est au niveau haut, et par conséquent, la sortie 'op' est portée au niveau bas, comme illustré dans le graphe associé. Lorsque l'entrée complémentaire 'ab' est au niveau haut, le même courant $I_1$ traverse Q2, et par conséquent, la sortie 'op' est portée au niveau haut. Ainsi, ce circuit fonctionne comme un inverseur.

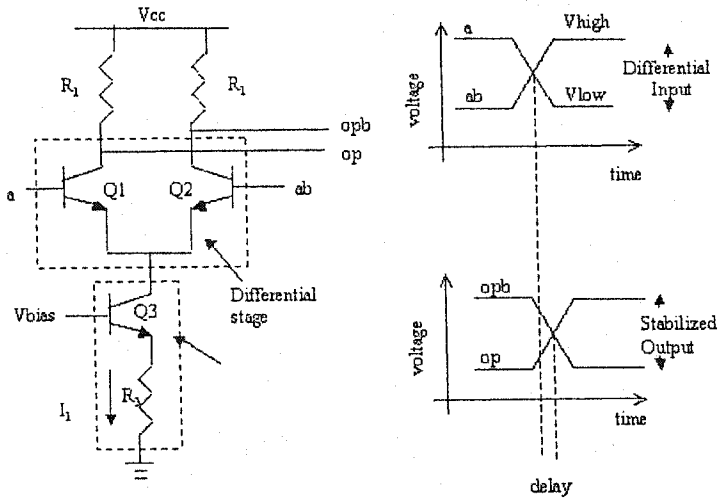


**Figure 1. La porte tampon-inverseur en CML et sa réponse temporelle**

Certains défauts peuvent transformer la nature différentielle de la porte. En effet, lorsqu'un court circuit de basse impédance, est inséré entre les entrées complémentaires 'a' et 'ab' ou 'b' et 'bb', d'une porte à 2-entrées, les deux lignes d'entrée ne sont plus

complémentaires l'une à l'autre. Cette défectuosité a fait l'objet d'études intensives tout au long de ce mémoire.

**Technique de modification du gain par réduction de la polarisation (BAS)**

La modification du gain par réduction de la polarisation est une technique qui consiste en l'application d'une phase de stress à un circuit en mode de test, par réduction de la polarisation qui lui est appliquée, afin de détecter des défauts de fabrication. La réduction de la polarisation appliquée à une porte réduit son gain (voir la figure 2.1 pour la courbe de gain). Par conséquent, une porte sans défaut produit une marge de bruit réduite. Par contre, lorsqu'un tel stress est imposé à un circuit défectueux, il rend plusieurs classes de pannes observables, ce qui se traduit par une forte dégradation de l'amplitude du signal de sortie. Lorsque plusieurs portes sont reliées en série pour former un environnement de simulation comme celui de la figure 2, les portes suivantes dans la chaîne n'ont pas assez de gain pour régénérer le rendement produit par une porte défectueuse. Dans ce cas, l'environnement de simulation commence à présenter le comportement d'un collage. Cependant, ces portes peuvent amplifier un signal de sortie de faible amplitude, produit par une porte sans défaut. Les détecteurs insérés à intervalles réguliers et qui sont conçus pour avoir un seuil approprié, peuvent identifier la présence d'un défaut de fabrication. Ainsi, cette technique identifie efficacement une porte défectueuse de celle sans défaut.

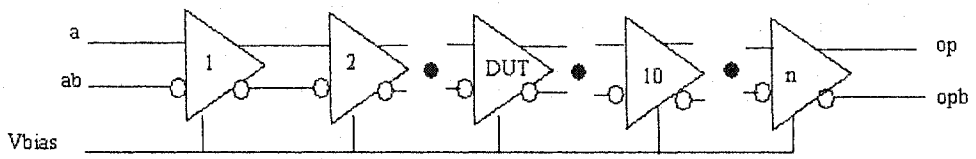


**Figure 2. Environnement de simulation pour l'étude de la réduction de la polarisation (DUT: *Device Under Test*)**

Lorsque la polarisation appliquée est trop faible, les portes n'ont pas assez de gain pour régénérer le signal de sortie produit par la porte sans défaut. Par contre, lorsque la polarisation appliquée est suffisamment élevée, les portes ont assez de gain pour régénérer même un signal de sortie de très faible amplitude produit par une porte défectueuse. Ceci est illustré à l'aide du circuit de la figure 3 pour une chaîne de tampon de grade 0 (la famille logique étudiée est disponible en 7avec un court circuit de 100 ohms à l'entrée de la 6ème porte.

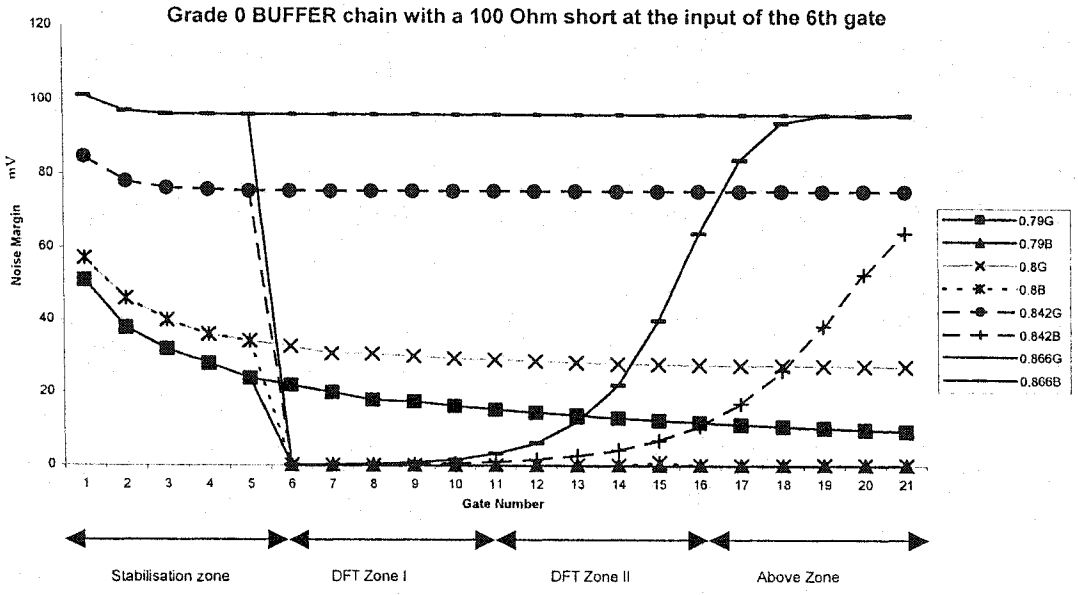


**Figure 3. Amplitude à la sortie à travers une chaîne de tampon de classe 0 pour différentes polarisations**

Dans la figure 3, l'amplitude à la sortie de chaque porte de l'environnement de simulation est tracée pour différentes polarisations, aussi bien pour les chaînes défectueuses que celles sans défaut. G désigne une chaîne sans défaut (Good) et B désigne une chaîne défectueuse (Bad). L'amplitude de sortie change avec la tension de polarisation. Alors qu'une bonne chaîne fournit une amplitude faible, due à une polarisation réduite dans les premiers niveaux; une chaîne défectueuse produit, soit une amplitude très faible, soit une sortie nulle. Le signal se dégrade rapidement à l'entrée du dispositif sous test (DUT). Quatre zones peuvent être identifiées dans la figure 3 pour la technique de BAS. Dans la zone de stabilisation, le signal d'entrée est passé à travers quelques tampons avant de se stabiliser. La différence dans la marge de bruit restante entre les portes défectueuses et celles sans défauts est élevée dans la zone 'DFT Zone I', ce qui rend cette zone très utile

pour la détection de défauts. Cependant, la différence dans la marge de bruit restante entre les bonnes et les mauvaises chaînes est basse dans la zone 'DFT Zone II', car les portes tendent à amplifier, dans cette zone, des signaux de faible amplitude. Dans la zone 'Above Zone', le signal produit par la chaîne défectueuse est entièrement régénéré. Le nombre de portes dans la chaîne qui se collent dans chacune de ces zones, dépend de la profondeur de la chaîne, du type et du temps de réponse de la porte, ainsi que de la tension de polarisation appliquée.

Cette technique a été étudiée pour des tampons, des portes ET, et des XOR. Avec les contraintes utilisées et la méthodologie adoptée, la gamme utilisable de la marge de bruit de toutes les portes était simplement de 2 mV. Cette valeur est susceptible de changer en raison des variations de procédé. Cette amplitude restante est insuffisante, et par conséquent, elle ne peut pas être utilisée pour identifier une porte défectueuse. Plusieurs méthodes ont été exploitées afin d'améliorer la marge de bruit restante utilisable, mais n'ont pas fourni de résultats satisfaisants. Par conséquent, notre recherche démontre que cette méthode n'est pas pratique pour tester les portes CML bipolaires.

**Le test de débalancement (ITT)**

Pour assurer une couverture complète de tous les défauts possibles dans des portes CML, une méthode de test, proposée pour ECL par Anderson [29] et breveté par GERSBACH, E. de J., et MOSER, J.J., [19], est étudiée. Elle porte le nom de `méthode de test de déséquilibre' (Imbalance Testing Technique, ITT). Cette méthode de test consiste en

l'application d'une phase de stress au circuit entier, afin de provoquer son déséquilibre, et par conséquent, tous les signaux marginaux sont suffisamment dégradés de façon à causer des erreurs logiques. La méthode de test de déséquilibre pour la famille CML bipolaire est étudiée dans cet ouvrage.

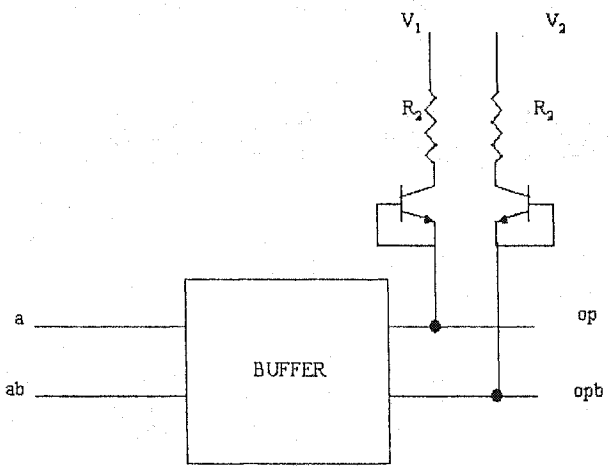


**Figure 4. La circuiterie pour le test de débalancement**

La figure 4 montre les circuits de test de déséquilibre connectés à chacune des lignes de sortie du tampon. En mode normal, $V_1$ et $V_2$ sont reliés à $V_{cc}$. En effet, la sortie de l'étage différentiel est déséquilibrée seulement si l'une des lignes de test est portée à un potentiel inférieur à $V_{cc}$. Lorsque $V_1$ ou $V_2$, est inférieur à $V_{cc}$, un courant traverse la diode, ce qui entraîne une réduction de la tension de sortie, et par conséquent, la diminution de la marge de bruit restante en sortie. Avec un déséquilibre convenablement appliqué, et pour le banc d'essai représenté à la figure 5, un circuit défectueux présente le comportement d'un collage.

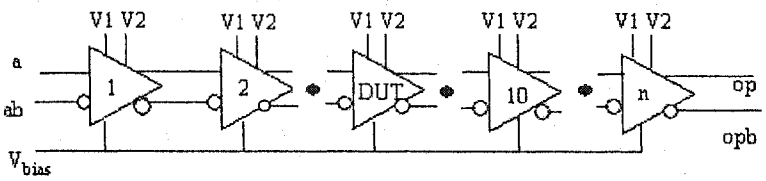


**Figure 5. Environnement de simulation pour l'étude du test de débalancement**

Lorsqu'un déséquilibre élevé est appliqué, une porte ET sans défauts présente le comportement d'un collage. Ce phénomène est appelé « accumulation de débalancement » ou « accumulation de stress ». Il a été démontré que la dissymétrie dans le schéma au niveau transistor de la porte ET, en est la cause. Afin de surmonter le problème d'accumulation, les portes placées à intervalles réguliers dans la chaîne ne doivent pas être déséquilibrées. Par conséquent, leurs gains demeurent inchangés, et elle sont capables de régénérer un signal de faible amplitude sur leurs entrées. Ceci est montré à la figure 6, où une porte normale est placée à la fin de chaque groupement de 5 portes. Ainsi, l'ITT parvient à identifier efficacement les éléments avec des défauts de fabrication. Le fait de soumettre, simultanément, la ligne de sortie et les lignes d'entrée multiples d'une porte à une contrainte de déséquilibre contribue aussi à une accumulation de débalancement. Un certain groupe de lignes déséquilibrées simultanément ne provoque pas l'accumulation, alors que d'autres la provoquent. Ces deux groupes sont identifiés, et des règles de conception sont présentées pour surmonter l'accumulation.

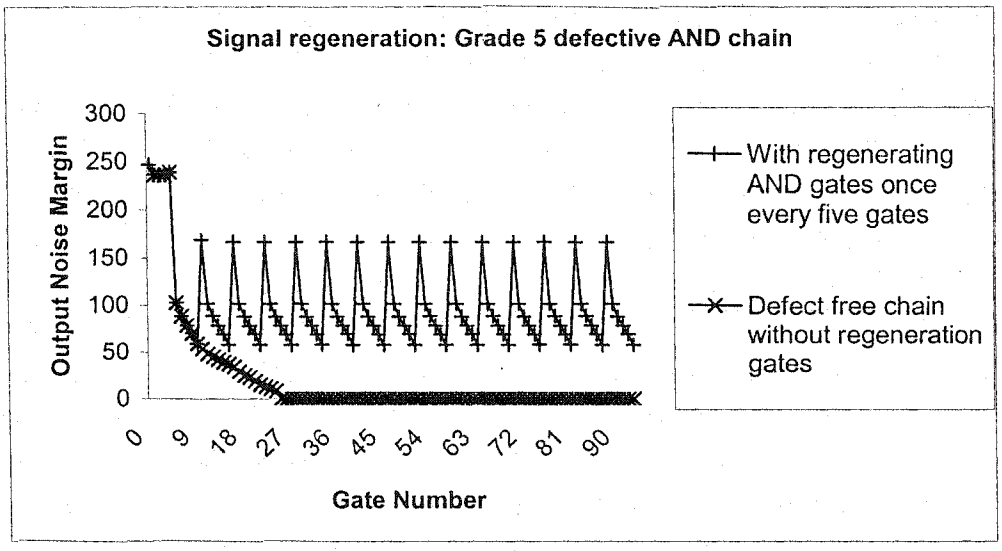


**Figure 6. Processus de récupération: La sortie est sensible à l'entrée 'b'**

## Analyse de sensibilité

Les effets de variation de plusieurs paramètres tels que la résistance, la température, etc., sur l'ITT, et par conséquent, sur les portes CML bipolaires, sont analysés en détail. Une recherche dans ce sens a montré que le fait d'insérer deux diodes dans le banc de test de déséquilibre, peut minimiser l'impact de l'accumulation de débalancement. (Voir les tableaux 3.5 à 3.8 au chapitre 3). Ainsi, l'équation en tension est donnée par,

$$V_{cc} - I_1 R_1 - (n.V_{be}) - I_1 R_2 - V_1 = 0$$

La sensibilité de $V_{out}$, relativement aux variations dans $V_{be}$, $R_1$ et $R_2$, respectivement, est donnée par les équations suivantes:

$\partial V_{out}^{\Delta} = n \cdot \frac{R_1}{R_1 + R_2} \partial V_{be}^{\Delta}$, où 'n' est le nombre de diodes, $\partial V_{be}^{\Delta}$ est la variation de la tension de diode.

$\partial V_{out} = I_1 \cdot \frac{R_2}{R_1 + R_2} \cdot \partial R_1$, où $\partial R_1$ est la variation de $R_1$.

$\partial V_{out} = I_1 \cdot \frac{R_1}{R_1 + R_2} \cdot \partial R_2$, où $\partial R_2$ est la variation de $R_2$.

Dans tous les cas cités ci-dessus, $R_2$ doit être augmentée ou diminuée, afin de minimiser l'impact des variations sur la tension de sortie. C'est au concepteur de choisir le nombre approprié de diodes ainsi que les bonnes valeurs pour $R_2$ et $V_1$. Avec un degré de liberté si élevé, cette technique peut facilement être modifiée afin d'être compatible avec les contraintes d'utilisation, afin d'obtenir une meilleure couverture des défauts.

**Testabilité du boîtier de test**

Une puce de test qui implémente les méthodes de testabilité a été proposée et conçue par Patenaude et Antaki. Cette puce de test est composée de deux principaux blocs: une matrice de portes comportant les structures de DFT proposées et le bloc des commandes de test, qui sont intercalés afin de former une architecture matricielle, tel qu'illustré à la figure 7 ci-dessous. Les deux blocs forment les lignes et les colonnes de la matrice, respectivement (voir les figures 5.2 et 5.3). Cette architecture permet de tester facilement n'importe quelle porte choisie

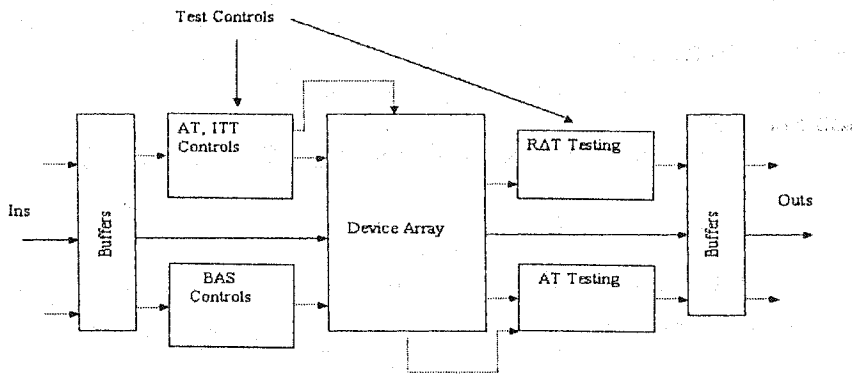


**Figure 7. Diagramme bloc de la puce d'évaluation**

Le matrice de cellules est composée de portes logiques de différents temps de réponse, connectées entre elles de façon à former des fonctions logiques très simples. Des chaînes des tampons, des blocs combinatoires composés de XOR et de ET, et des machines d'états re-configurables sont présentes dans la matrice de cellules. Les méthodes de test : 'Amplitude Testing' (AT), 'Imbalance Testing Technique' (ITT), 'Bias Alteration Stressing' (BAS), et 'Reduced Delta Testing' (RΔT) sont implémentées dans la puce de test.

Les tests appliqués à la puce sont suffisamment simples pour permettre de tester complètement les fonctions de toutes les portes. Ils exploitent la structure des commandes des méthodes DFT, lesquelles permettent l'identification de plusieurs défauts dans la puce. Les structures de test sont réalisées avec des modèles de test faits sur commande et générés par l'outil de flot de Nortel. Un vecteur de test se compose de deux parties: a) les stimulus qui sont appliqués aux entrées de la puce, et b) les valeurs désirées aux sorties de la puce. Chaque ligne de la matrice du dispositif possède un générateur de polarisation

programmable dédié (Programmable Bias Generator, PBG), qui permet l'étude de chaque ligne possible, d'une façon indépendante.

Les éléments défectueux sont identifiés en utilisant (a) des modèles fonctionnels et/ou (b) les techniques de DFT proposées. Les différents tests effectués sur la puce de test, sont énumérés comme suit: le test de continuité, le test de tension, le test de propagation du délai, le test d'amplitude, le test de déséquilibre, et finalement le test de BAS. Le test de propagation de délai est utilisé comme une référence par rapport aux techniques de DFT proposées, afin d'identifier les éléments défectueux. L'objectif est de comparer leur couverture respective, et d'identifier les défauts correspondants afin d'évaluer leur signification qualitative.

De tous les tests effectués avec les vecteurs de test que nous avons développé, 11.4% des éléments manufacturés ont été trouvés défectueux. Quand les résultats de quelques tests seront disponibles, d'autres analyses seront nécessaires afin de tirer des conclusions finales sur l'efficacité des méthodes de test proposées, et ceci est laissé pour des travaux futurs.

**Conclusion**

Nos travaux ont porté sur les validations de méthodes de DFT pour des portes CML bipolaires. Ils sont concluants dans la mesure où les techniques de DFT proposées parviennent à identifier avec succès les éléments défectueux d'un lot manufacturé. Un

ensemble de règles de conception est aussi présenté pour la méthode de test de déséquilibre. La sensibilité de la tension de sortie provoquée par les circuits de test dans l'ITT, due à des divers facteurs environnementaux, est aussi discutée. Une des méthodes de test proposées par une équipe précédente a été considérée invalide à cause de la limitation de l'environnement de test. Ce travail constitue une contribution au domaine du test des portes CML bipolaires. Ce travail peut servir de base pour des travaux futurs sur le sujet.

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| | |
|---|---|
| AT | Amplitude Testing |
| ATE | Automatic Test Equipment |
| ATPG | Automatic Test Pattern Generation |
| B | Bad |
| BAS | Bias Alteration Stressing |
| BSU | Basic Step Unit |
| CML | Current Mode Logic |
| CMOS | Complementary Metal Oxide Semiconductor |
| DFT | Design For Testability |
| DUT | Device Under Test |
| ECL | Emitter Coupled Logic |
| G | Good |
| IC | Integrated Circuit |
| IFA | Inductive Fault Analysis |
| i/p | input |
| ITT | Imbalance Test Technique |
| NM | Noise Margin |
| o/p | Output |
| PBG | Programmable Bias Generator |
| RΔT | Reduced Delta Testing |
| RNM | Remaining Noise Margin |
| TPG | Test Pattern Generation |
| VCD | Value Change Dump |
| VLSI | Very Large Scale Integration |

## LIST OF APPENDICES

# INTRODUCTION

Historically, MOS logic families have dominated due to their high density and low power consumption characteristics. However, ECL and CML logic families implemented with bipolar technologies have continuously occupied lucrative niches such as very high-speed circuits. The evolution of technology has lead to the realisation of high-speed circuits. Switching speeds up to 50 Gb/s and gate delays far below 1ns have been reported in [33]. CML gates are used in high-speed applications like telecommunications, transmitters, receivers, microwave digital processing, satellite communications, etc.

CML gates have maintained their popularity owing to their high speed and high gain characteristics. In order to successfully use these gates for complex VLSI circuits, it is imperative to test them for manufacturing defects. Very little specific literature exists on the testability of bipolar CML gates, as discussed in chapter 1. The dominance of MOS technologies has had for consequence that ECL and CML technologies have received little attention. Due to the technological evolution, area of bipolar devices has decreased significantly, and the dynamic power dissipation of bipolar gates favourably compares with CMOS in very high-speed applications [27]. Several testability techniques suitable for CMOS families are less appropriate for bipolar CML gates [4, 29]. Since both ECL and CML are non-saturating logic families, some of the testing techniques proposed for ECL may be applicable to bipolar CML as well.

The microelectronic division of Nortel Networks was studying the testability of bipolar CML gates, for their technology. NT25™ [1] design kit is based on a high performance bipolar process. In the first phase of the project, Patenaude and Antaki studied the possible defects with bipolar CML gates, and also proposed DFT methods to detect such defects. This master thesis is a continuation of their work. Monté is also presently studying complementary related issues.

The main purpose of the work reported here is to determine how defects propagate in this logic family, and also to study how these defects degrade the performance of bipolar CML gates. We also study some of the potential testing techniques proposed by Patenaude and Antaki, as applicable to Bipolar CML gates. Certain testing techniques used in combination to improve fault coverage, were analysed in a test chip designed by Patenaude and Antaki [4, 29, 28]. One of the main ideas behind devising testing techniques for Bipolar CML gates was to obviate the need for expensive at-speed testers and use dc-testing to detect manufacturing defects [9].

The first chapter of the thesis presents the basic concepts of bipolar CML gates and briefly describes the NT25™ VersArray technology. Some of the benefits of these gates are listed, and the importance of testing and design-for-testability is highlighted. Possible faults with these gates are also listed. This chapter also reviews some relevant literature. We also give a notion of the testing techniques that have been studied in this work.

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1 NT25 is a trademark of Nortel Networks.

The second chapter studies one of the testing techniques, called the Bias Alteration Stressing (BAS) technique in detail. This testing technique enables the study of fault propagation in bipolar CML gates and also helps analyse the performance degradation of these gates. With this knowledge, it becomes easier to understand the characteristics of these gates and further devise suitable testing techniques for them. The results obtained for some of the gates studied are presented and analysed.

In the third chapter, we extend a testing technique studied for ECL gates to bipolar CML gates. We call this the Imbalance Testing Technique (ITT). Our analysis of this technique uncovers performance degradations in bipolar CML gates. The limitations imposed by these gates due to their design on ITT are also studied. We also present some useful methods to overcome the uncovered limitations. We finally present a set of design rules to avoid the limitations.

The fourth chapter discusses the sensitivity of the test circuitry proposed in chapter three to various parameters like noise, temperature, process variations, etc. These are some of the important factors to be taken care of while implementing the testing technique in an actual circuitry.

The fifth chapter discusses the test vectors generated for testing the test chip that implements some of the testing techniques studied by the previous team in the project. We also present some results obtained using these vectors. This chapter analyses the

efficiency of the testing techniques, and the fault coverage obtained by independent and combined study of different test techniques.

# CHAPTER 1

# BACKGROUND INFORMATION AND LITERATURE REVIEW

## 1.1 Introduction

Complementary Metal Oxide Semiconductor (CMOS) technologies posses several advantages that largely stem from the low static power dissipation of some logic families they allow to integrate. It became the dominant technology and its testability was deeply studied. However, the testability of bipolar logic gates received very little attention from the scientific community due to their low density and high power consumption characteristics. Current Mode Logic (CML) devices using bipolar technology has long been the technology of choice in applications requiring logic functions at multi-gigahertz rates, where switching speed is more important than power dissipation and cost [4, 29, 19, 30, 32, 26, 27]. With the achievement of low power, high speed and high density, CML can find a variety of applications [27, 35]. In today's world, there is a strong interest in high-speed electronic technologies [26, 27].

In order to successfully use bipolar CML gates in circuits, it becomes imperative to study their testability. Their testability is a rarely studied topic. In order to fill this gap, and to be able to use these gates, we studied the testability of Nortel Networks' NT25$^{TM}$ bipolar CML technology combined with the VersArray technology that comprise a cell library and a set of technology files [6]. This bipolar CML logic family is similar to Emitter

Coupled Logic (ECL) families [4, 29]. Hence, we first briefly discuss ECL logic families, before focusing on CML.

## 1.2 Emitter Coupled Logic

Emitter Coupled Logic (ECL) is a non-saturated digital logic family. ECL is based on the use of a multi-input differential amplifier to amplify and combine digital signals, and emitter followers to adjust the dc voltage levels. They operate by diverting the current from one path to another rather than by switching the transistors 'on' and 'off'. The transistors remain entirely within their active operating regions at all times. Hence, the transistors have a much reduced charge storage time to contend with, and can change states much more rapidly. Therefore, it is possible to achieve propagation delays of 300 ps [27, 11]. Thus, the main advantage of this type of logic gates is their extremely high speed.

## 1.3 Bipolar CML gates

Bipolar CML gates are low power, high gain, and high-speed gates, operating in the low GHz frequency range. Like ECL, bipolar CML families operate by switching current between conducting and non-conducting branches of the gates. Bipolar CML gates are purely differential; using low voltage swings (250 mV) that lead to faster circuits and reduced power consumption [6]. Differential signalling reduces EMI (electromagnetic interferences), and is also less sensitive to cross talk, and offers high noise immunity.

In order to study the testability of a particular logic, it is important to understand its functionality. To orient the reader, in this section, we describe how bipolar CML logics are implemented in the VersArray NT25$^{TM}$ technology and also explain the operation of a simple inverter [6]. Then we also explain the operation of a two-level OR gate. Antaki [4] developed a set of Boolean equations for the outputs of Nortel's bipolar CML logic gates.

### 1.3.1 Inverter

Bipolar CML inverter is a simple logic gate using only one differential transistor pair as shown in the figure below. The output waveform of the inverter and its truth table are presented.

**Table 1.1 Truth table of an inverter**

| A | ab | op | Opb |
|---|---|---|---|
| High | Low | Low | High |
| Low | High | High | Low |

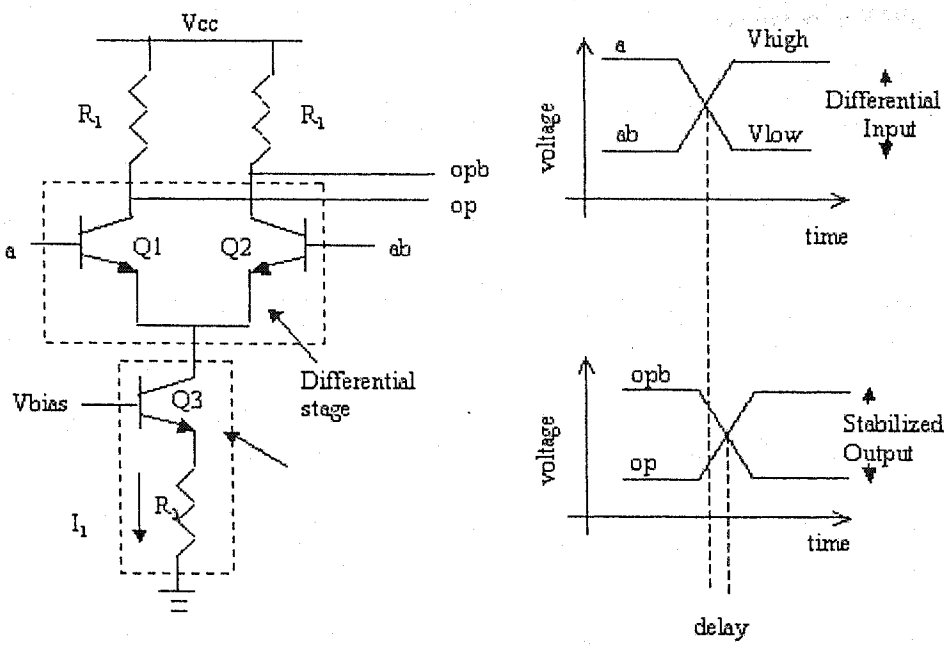


**Figure 1.1 Bipolar CML Inverter**

In figure 1.1, $V_{bias}$ is the bias voltage applied to the gate. The current $I_1$ is supplied using a current source transistor. Input 'ab' is the complement of input 'a'. Similarly, outputs 'opb' and 'op' are complementary.

- When input 'a' is high, current $I_1$ flows through Q1, lowering the output voltage 'op'. On the other hand, no current flows through Q2, and therefore, 'opb' is high. Thus, when 'a' is high, 'op' is low; 'opb' is high, and the gate functions as an inverter.
- When 'ab' is high, the current $I_1$ flows through the transistor Q2, lowering the voltage 'opb'. When 'a' is low, being the complement of 'ab', no current flows through transistor Q1. Hence, 'op' is high and again the gate functions as an inverter.

The same circuit can be used as a buffer by simply switching the differential output lines, 'op' and 'opb' [4, 29, 6].

### 1.3.2 Bipolar CML OR gate

In this thesis, we also focus our attention on gates like OR, AND, and XOR. Bipolar CML AND gates and OR gates have received special attention in our study, for reasons that will become evident in chapters 2, 3 and 4 of this thesis. The operation of the OR gate is explained here, and the schematic of the XOR gate is given in figure 2.3.

Figure 1.2 shows the schematic of a bipolar CML OR gate. The two input OR gate has two differential transistor pairs, one for each set of complementary inputs. The number of differential pairs in a circuit is equal to the number of complementary input signals [4, 6]. Each of the additional differential pairs uses level shifters to avoid saturation. In this schematic Q3 and Q4 are used for level shifting. For a two input circuit to function as an OR gate, when both the inputs are low, the output should be low, and it should be high otherwise [19]. In the schematic of figure 1.2,

- When the inputs 'a' and 'b' are high, the current flows through transistors Q1 and Q5, driving 'opb' low and 'op' high.
- When 'a' is high, and 'b' is low, the current flows through transistors Q1 and Q6, driving 'opb' low and 'op' high.

- When both 'a' and 'b' are low, the current flows through Q6 and Q2, driving 'op' low and 'opb' high.
- When 'a' is low and 'b' is high, the current flows through Q5, and the upper differential pair receives no current, even though the transistor Q2 can conduct. Thus, 'opb' is driven low and 'op' is driven high.

The truth table of bipolar CML OR gate is given below. This table lists the transistors that conduct for a given signal value.

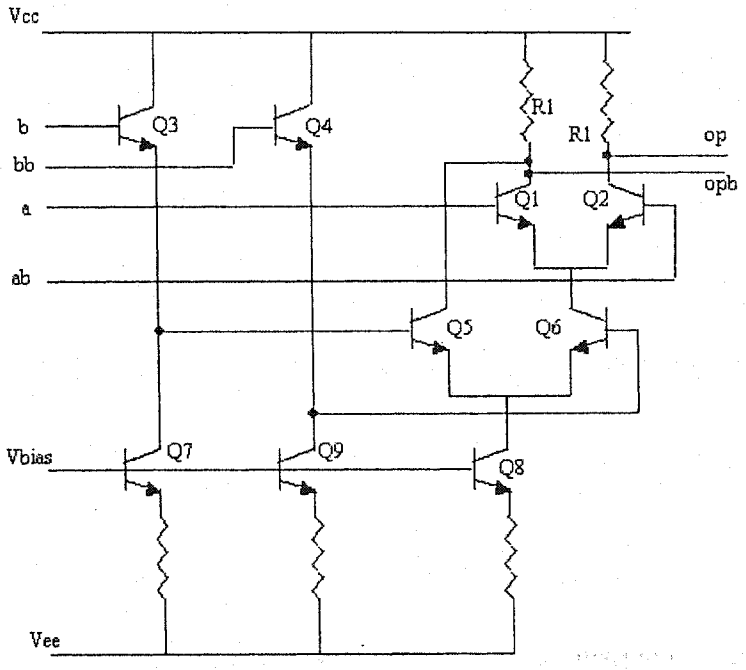


**Figure 1.2 Schematic of bipolar CML OR gate**

Figure 1.3

Table 1.2 Truth table of bipolar CML OR gate

| A | ab | b | bb | Conducting transistors | op | opb |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | Q2, Q6 | 0 | 1 |
| 1 | 0 | 1 | 0 | Q1, Q5 | 1 | 0 |
| 1 | 0 | 0 | 1 | Q6, Q1 | 1 | 0 |
| 0 | 1 | 1 | 0 | Q5, Q2 | 1 | 0 |

## 1.4 VersArray Technology

Nortel Networks' VersArray technology is a gate array technology [6]. It consists of an array of Basic Step Units (BSU). Each basic step unit consists of two transistors and a resistor. These transistors and resistors are then connected together to form the desired logic. This technology offers seven speed grades by varying the value of the resistor $R_1$ and the applied bias. The right speed grade can be chosen based on the speed/power requirements. The functionality and architecture of NT25$^{TM}$ bipolar CML has been discussed so far. The following sections discuss the importance of testing, different design for testability methods and fault modelling for bipolar CML.

## 1.5 The importance of testing

During the fabrication of an IC, physical defects could occur [34]. Examples of physical defects are: improper contact windows, oxide breakdown, surface impurities, thin metal wire, etc. Testing of a system is an experiment in which the system is exercised and its

resulting response is analysed to ascertain whether it behaved correctly [2]. Testing is used to isolate the defective parts from a manufactured lot. Testing is important to ascertain the quality of a manufactured part. An undetected defect may fail the chip later on in the field due to various factors like high current, voltage, or environmental attributes. Detecting and discarding a defective chip at an early stage is more economic than detecting a defective board used in a system, in spite of the testing costs involved.

## 1.6 Design For Testability

Design For Testability (DFT) techniques are design methods specifically employed to ensure that a device is testable. *Controllability, observability* and *predictability* are the three most important factors that determine the complexity of deriving a test for a circuit.

- **Controllability** is the ability to establish a specific signal value at each node in a circuit by setting values on circuit's inputs.
- **Observability** is the ability to determine the signal value at any node in a circuit by controlling the circuit's inputs and observing its outputs.
- **Predictability** is the ability to obtain known output values in response to a given input stimuli.

DFT is used to reduce test generation costs and enhance the quality (fault coverage) of tests. For structured DFT techniques, tests are generated automatically, increasing the quality and substantially decreasing the test development time. This significantly affects the time to market of a product and hence its commercial success. Hence, it is important

to have a structured DFT methodology in place for any type of logic family. References [2] and [8] are excellent textbooks on testing and DFT.**Significance of developing DFT methods for bipolar CML**

In conventional digital testing, the Automatic Test Equipment (ATE) applies test vectors at the primary inputs of the circuit, measures the signals at the primary outputs of the circuit, and compares this against the expected output values to determine if the chip is defective. Due to the high gain of bipolar CML gates, these gates tend to mask noise margin faults, as reported in [4, 29, 19, 31, 32]. Classical digital testing techniques do not detect a good proportion of these faults, as the faults are not propagated to the primary outputs of the circuit (not *observable*). Therefore, it is important to develop DFT methods to detect such defects. This is the main objective of our study. We study two DFT techniques in detail to determine their suitability for bipolar CML. Proper modelling of the faults is essential to obtain high fault coverage. The following sections discuss the difference between defects and faults, their coverage, and modelling. The studied DFT techniques are also briefly described in this chapter.

## 1.8 Faults and Defects

A defect in an electronic system is the unintended difference between the implemented hardware and its intended design. Examples are: unintended shorts between nets, an open in a net, etc. A representation of a 'defect' at the abstract function level is called a fault. The difference between a defect and a fault is that they are imperfections in the hardware and function, respectively.

Fault coverage is defined as the ratio of the number of detected faults to that of faults in the initial fault list. Defect coverage is the probability with which the test detects any defect that occurs on the chip.

## 1.9 Fault modelling & Defect modelling for bipolar CML

In order to design bipolar CML gates for their testability, it is important to understand the defects possible with this logic family. Patenaude [29] and Antaki [4] carried out an extensive study of the defects possible in bipolar CML. They developed a fault dictionary for CML gates and also proposed a few DFT techniques to detect some of these defects [5, 30]. They developed fault models for bipolar CML gates, and developed tools for Inductive Fault Analysis (IFA) and also to test CML gates [30, 31, 32]. In the following sections, we discuss the different types of fault modelling and defect modelling relevant to bipolar CML.

### 1.9.1 Fault modelling

Physical faults do not allow direct mathematical testing and diagnosis. Logical faults are a convenient representation of the effect of the physical faults on the operation of the system. A fault is detected by observing the error caused by it. The basic assumptions regarding the nature of logical faults are referred to as a "fault model". Fault models are used to provide a fault list for test generation and test verification [2, 8]. Therefore, the

fault list, and hence the fault model used to generate it, play a key role in determining what test set is generated and its perceived effectiveness [12].

Esonu et al. [10] have reported a detailed study of fault models for shorts, stuck-at, truth table, delay, and Iddq faults for bipolar ECL. Some of the relevant fault models available in the literature are briefly described in table 1.3. While most of the fault models are described in [2, 8], additional references are provided for each model in the table. Menon et al. [26, 21, 23] analysed faults in simple logic circuits and suggested that transistor level testing provides a higher coverage of faults compared to that at the gate level. It is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [1]. The major fault models at transistor level are stuck-at faults, and bridging faults [7]. Bridging faults are reported to be the major failure modes in ICs in [27]. Certain bridging faults manifest as stuck-at faults [15]. Bridging faults are reported to be up to 30% of all the faults in [12] and up to 50% of all the faults in [20].

**Table 1.3 Fault model definitions**

| Fault model | Definition | References |
|---|---|---|
| Bridging fault | A physical short between two signal lines is referred to as a bridging fault. | 18, 19, 20, 31 |
| Delay fault | These faults cause the combinational delay of a circuit to exceed the clock period. Specific delay faults are transition faults, gate-delay faults, line-delay faults, segment-delay faults, and path-delay faults. | 18, 30, 31 |
| Like fault | A fault that forces both outputs of a differential circuit to identical values for certain input combinations, without causing any of the outputs to be stuck-at. | 17, 29, 33 |
| Path delay fault | This fault causes the cumulative propagation delay of a combinational path to increase beyond some specified time duration. "Propagation delay" is defined as the propagation of a signal transition through a given path. Thus, for each combinational path there are two path-delay faults, which correspond to the rising and the falling transitions, respectively. | 21, 22, 30, 31 |
| Parametric fault | Such a fault changes the values of electrical parameters of active or passive devices from their nominal or expected values | 2, 4, 31, 32 |
| Reduced Noise Margin fault | A fault that reduces the remaining output noise margin. | 3, 4, 5, 12, 13, 14 |
| Stuck-at fault | This fault is modelled by assigning a fixed (0 or 1) value to the input or output of a logic gate. Single stuck-at faults have 2 faults per line, stuck-at-1 and stuck-at-0. | 2, 17, 18, 20, 27, 31, 32 |
| Transition fault | The gate delay of a given gate, usually an increase over the nominal value, is assumed to be large enough to prevent a passing transition from reaching any output within the clock period, even when the transition propagates through the shortest path. Possible transition faults of a gate are slow-to-rise and slow-to-fall types. | 3, 4, 14, 15, 32 |
| Truth-table fault | A fault that produces an output of a logic gate that is different from the expected value for a given input. | 3, 4, 14, 15, 31 |

The most widely used fault model is that of a single line (wire) being permanently "stuck" at a logic value. Single-stuck fault model is a classical or standard fault model,

as it has been widely studied in the literature. A non-classical fault, in general refers to a fault other than a stuck-at fault. When choosing a fault model, it is important to select a model whose faults are generally dominated by faults of other fault models, because a test set detecting the faults of the chosen model will also detect many other faults that are not even explicitly considered. The best fault model representing many different physical faults is the single-stuck fault model [2, 8]. Tests that detect classical faults detect many non-classical faults as well [2].

Stuck-at faults at the gate level are the most popular fault models in digital testing. Automatic Test Pattern Generation (ATPG) tools support classical stuck-at fault models for structured tests. ATPG tools greatly reduce the test generation time and cost. If we could model most of the defects present in the bipolar CML family as stuck-at faults, then the process of test pattern generation can be automated. Therefore, in this study we use stuck-at faults models. Anderson [3] has proposed a DFT technique for ECL that forces stuck-at behaviour in defective gates. We study this method in detail in Chapter 3.

### 1.9.2 Defects possible with bipolar CML & Defect modelling

In this section we study how the different physical defects possible with bipolar CML are mapped to fault models. A defect such as a short between a net and ground can be modelled as a 'stuck-at' fault. This 'short' is modelled by connecting a very low resistance in series between the net and the ground. Other defect models are discussed in

table 1.4, excerpted from [29]. Proper fault modelling is required to obtain high fault coverage.

**Table 1.4 Defect modelling, excerpted from [29]**

| Defect type | Definition | Model | References |
|---|---|---|---|
| Short-circuit between different transistor nodes | Used to model any defect causing an undesired interconnection between two terminals of a transistor. | Modelled using a small resistance or a direct connection between the two nodes. | 3, 13, 17, 24, 23, 10, 18 |
| Open-circuit in a transistor terminal | Used to model any defect breaking a transistor node. | Modelled using a high resistance, normally above 1Mohms (some times in parallel with a small capacitor) in series with the terminal of the transistor. | 3, 13, 17, 26, 10, 24, 18 |
| Pipe between collector and emitter | Used to model any defect causing an abnormal behaviour in a bipolar transistor (normally an abnormally high current between the collector and the emitter). | Modelled using a resistance connected in parallel between the collector and the emitter (the value of this resistance varies from 400 Ohms to a few KOhms) | 3, 13, 17, 10, 18 |
| Bridge between two nodes | Used to model any short-circuit between two unspecified nodes. | Modelled by using a resistor between 400-Ohms and a few Kohms. | 17, 27, 12, 10, 25, 18 |
| Open | Used to model any open on an unspecified node. | Modelled by using a resistor above 1MOhms (sometimes in parallel with a small capacitor) | 9, 17, 18 |

We are interested in characterising the fault propagation and the performance degradation of bipolar CML gates. In a differential circuit, when one of the two differential inputs is defective and is shorted to the other, the output signals should not complement each other, as described by Menon et al. in [27, 14]. The differential output lines will exhibit stuck-at fault. Therefore, the differential output amplitude is zero. Such a defect should

be easy to detect, and hence it is used in our study. The effect of such a defect is described in detail in Chapter 2.

### 1.10 Types of test

In general, each chip is subjected to two types of tests, parametric and functional tests, as described below. These tests are further discussed in Chapter 5.

**Parametric tests:** *DC parametric* tests include shorts test, opens test, maximum current test, leakage test, output drive current test, and threshold levels test. *AC parametric* tests include propagation delay test, setup and hold test, functional speed test, access time test, refresh and pause time test, and rise and fall time test. These tests are usually technology dependant.

**Functional tests:** These consist of the input vectors and the corresponding responses. They check for proper operation of a verified design by testing the internal chip nodes. Functional tests cover a very high percentage of modelled faults (e.g., stuck-type).

**Testing combinational and sequential circuits:** Combinational circuits are tested by applying a sequence of test vectors and by comparing the output response with the expected output response. The tests in the sequence may be applied in any order. Almost, all digital systems of any significant size are realised as sequential circuits [2, 8]. Testing sequential circuits is considerably more difficult than testing combinational circuits. To detect a fault a test sequence is usually required, rather than a single input vector, and the response of a sequential circuit is a function of its initial state.

## 1.11 Studied DFT techniques

Some of the testing techniques proposed by Patenaude and Antaki [4, 29] are studied in detail to determine if they can be successfully used for bipolar CML gates [5, 28, 19, 30, 31, 32]. These techniques are briefly described below. In this study, we also uncovered some roadblocks and showstoppers. We discuss means to circumvent the problems found with these techniques. Therefore, some of these DFT methods can be used for bipolar CML family, as reported in [19].

### 1.11.1 Bias Alteration Stressing Technique

The first technique that we study is called the Bias Alteration Stressing (BAS) technique, in which the bias applied to the gate is altered to stress the gate [4, 29, 16]. With reduced bias, the gain of the gate is altered and a good gate outputs low amplitude, while a defective gate outputs very low amplitude or exhibits stuck-at behaviour.

### 1.11.2 Imbalance Testing Technique

The second technique is called the Imbalance Testing Technique (ITT) and was originally proposed for ECL gates by Anderson [3, 4, 29]. In ITT, a DFT circuitry is added to each of the two output lines of the gate. The idea is to reduce the output voltage of one of the complementary signals by dropping some voltage across the corresponding test circuit shown in figure 1.3. The gate is partially imbalanced by stressing one output line at a time. When only one output line is imbalanced, the differential output amplitude is lower than in a normal gate. This is shown in figure 1.4. By contrast, defective gates are often

led to exhibit stuck-at behaviour, leading to detection of defects on the biased side of the gate. Similarly, the other output line is imbalanced, after the first one has been restored to its original state. Therefore, ITT is a two-pass testing method.

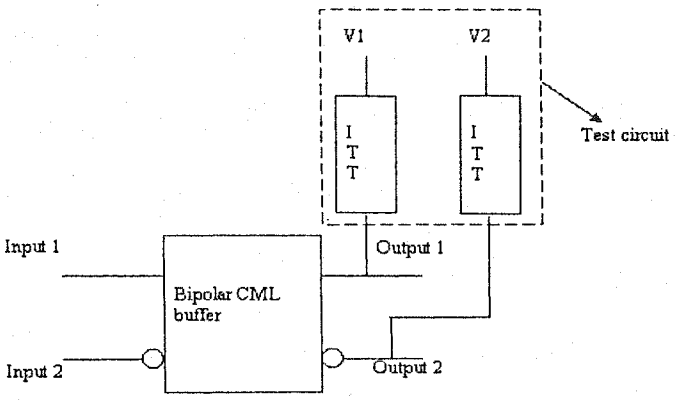


**Figure 1.4 BUFFER with Imbalance test circuitry**

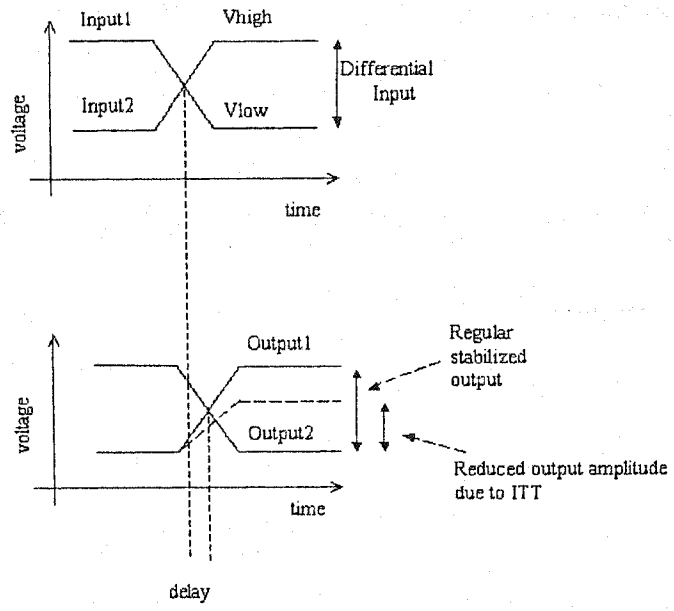


**Figure 1.5 Input and Output waveforms of a BUFFER subject to ITT**

We also study in detail the effect of variation of various parameters like resistance, temperature, etc., on the imbalance testing technique. The test chip implementing the test methods suggested by Patenaude and Antaki was fabricated [28]. We also discuss how we generated functional test patterns for this test chip. The testing of the test chip is not fully completed yet, and Ginette Monté is analysing the results available so far.

## 1.12 Summary

Evidently, very little literature exists on the testability of bipolar CML logics. Bipolar CML gates find extensive applications in high-speed digital circuits. We discussed about fault modelling and different types of faults possible with them. Bridging faults contribute to a major portion of the total faults. Bridging faults cover a wide variety of shorts. Menon's research on bipolar emitter coupled logics has been useful to successfully position our study on bipolar current mode logics. Some of the testing techniques already proposed by Patenaude and Antaki are studied in much detail in this thesis to find their suitability for the bipolar CML family.

# CHAPTER 2

# BIAS ALTERATION STRESS TECHNIQUE

## 2.1 Introduction

CML gates are growing in popularity owing to their high speed, high gain and relatively low power consumption characteristics. Due to their high gain, even a small signal output produced by a defective gate is quickly regenerated by other defect-free gates in the circuit as explained by the gate's gain coupled to their differential nature in figure 2.1 [29, 30]. The classical definition for gain, $G_{diff\text{-}diff}$ is defined as the ratio of the differential output voltage to the differential input voltage. Other gain definitions can be found in [29]. CML gates tend to mask noise margin faults due to their high gain. Such defects could be detected, by altering the gain of the gate, degrading the performance of the gate. *Bias Alteration Stressing* (BAS) is a technique in which the circuit is stressed in the test mode by reducing the bias applied to it, to detect such defects [29]. The basic principle of operation of BAS is that when the bias is altered, the gain of the gate is altered, as seen from the figure excerpted from [29]. CML gates have a lower gain when reduced bias is applied. A defective gate present in the circuit often outputs very low amplitude or exhibits stuck-at behaviour. With a suitably reduced bias, normal gates that are present at the output of a defective gate do not have enough gain to regenerate, in a few levels, the signals of amplitude lower than some target threshold.

The objective of the BAS technique is to ensure that a detector designed to detect a very low amplitude signal, even when it is several levels after the defective gate, would have the ability to differentiate a fault-free circuit from a faulty one. To study the effect of bias variation and masking, a test bench was developed as described in the following section.

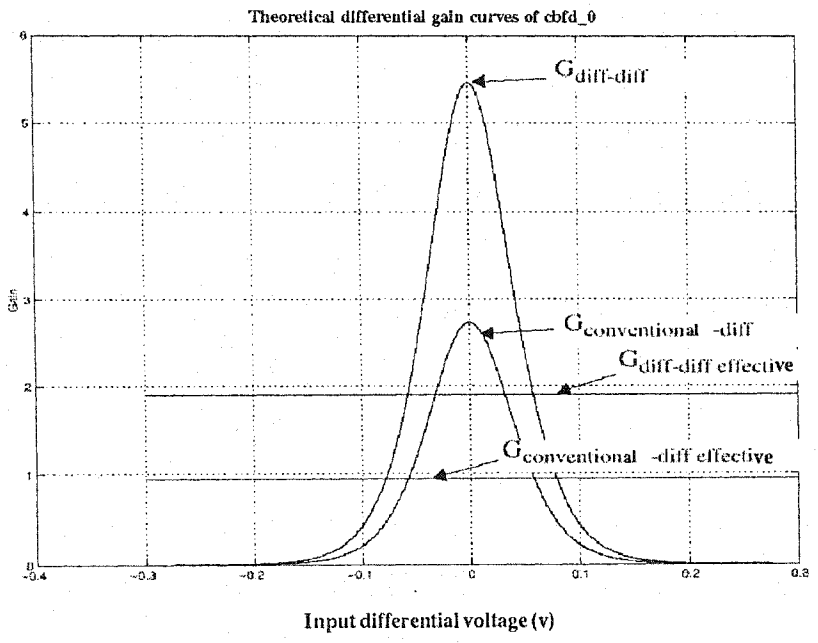


**Figure 2.1 Theoretical differential gain curve of CML grade 0 BUFFER, excerpted from [29]**

## 2.2 Test bench setup for characterising BAS technique

To study the effects of defects in bipolar CML gates, a number of gates of the same type and of the same speed grade are connected in series to form an appropriately biased chain. BUFFERs, as well as two input AND, and XOR gates are analysed. AND, and OR gates have the same schematic, (see the schematic of the bipolar CML OR gate presented in figure 1.2, chapter 1), with the exception that the input and output lines of

the OR gate are reversed to obtain an AND function, as shown in figure 2.2 [4, 6]. AND gates are analysed here. The functionality of bipolar CML OR gate is explained in chapter 1.

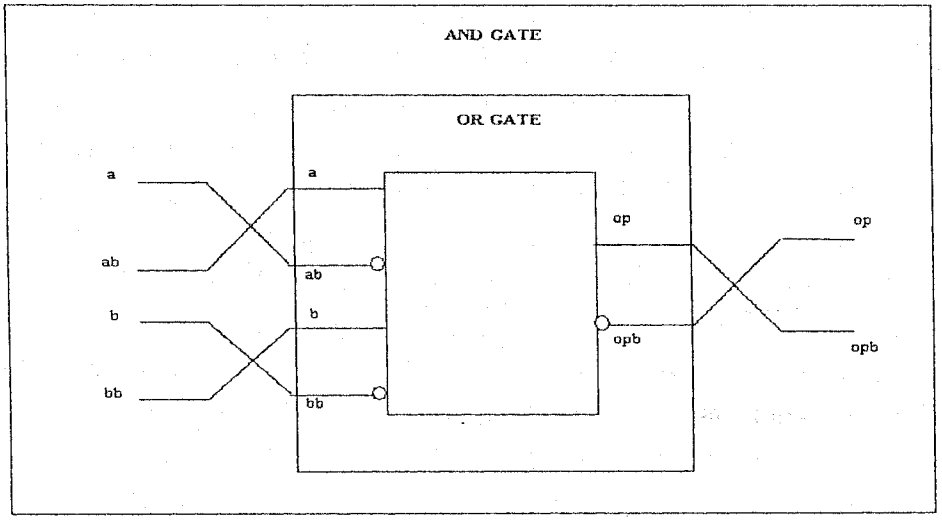


**Figure 2.2 Bipolar CML AND gate from bipolar CML OR gate**

Figure 2.3 shows the transistor level schematic of a two input XOR gate. The associated truth table shows which transistors conduct for each of the logic levels possible.

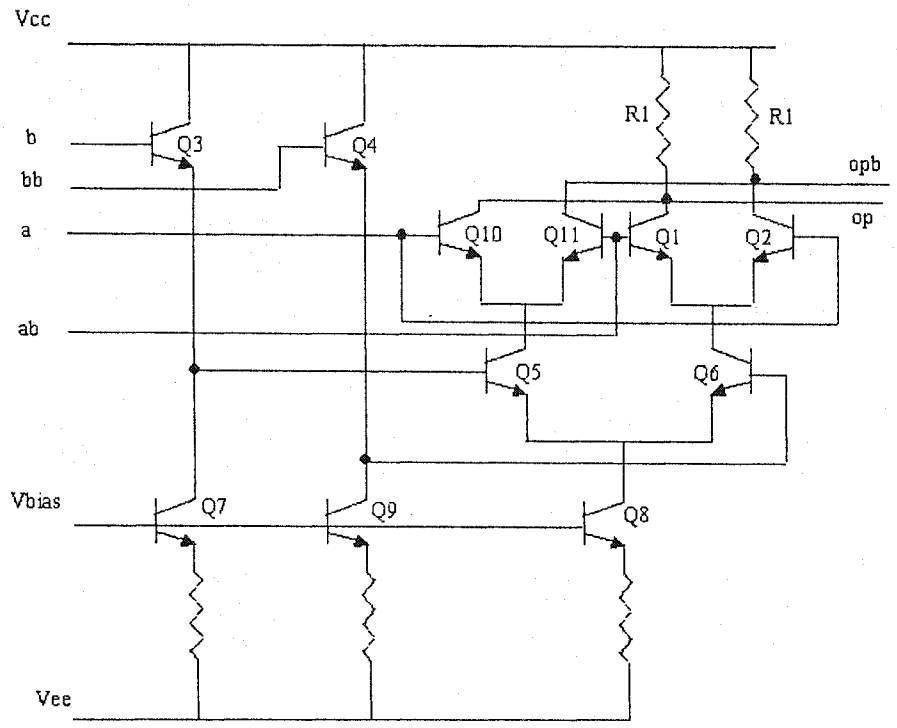


**Figure 2.3 Schematic of bipolar CML XOR gate**

**Table 2.1 Truth table of bipolar CML XOR gate**

| a | b | Transistors that conduct | Op |
|---|---|---|---|
| High | High | Q5, Q10, Q2 | Low |
| High | Low | Q6, Q10, Q2 | High |
| Low | High | Q5, Q11, Q1 | High |
| Low | Low | Q6, Q11, Q1 | Low |

A typical test bench setup for BAS test is depicted in figure 2.4. A few buffers are placed in front of the DUT to stabilise the amplitude of the input signal. Indeed, with BAS, the output amplitude produced by a normal gate changes with reduced bias. Since bias will

be varied as a controllable parameter, the natural amplitude produced by a chain of defect-free gates can automatically be computed by a circuit simulation as part of the process of characterising the signature of each fault. This is not computationally efficient, since it is repeated for each defect location for a given 'gate type - speed grade' combination, but it is a very simple and affordable method of making the test bench systematically and automatically produce realistic signals, as they would truly appear if we use a reduced bias.

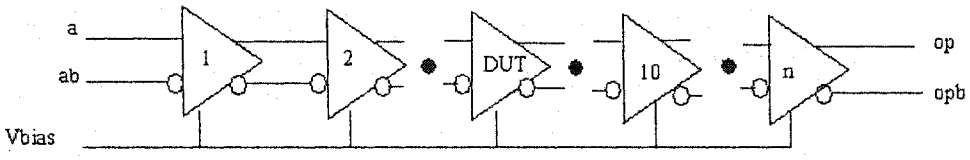


**Figure 2.4 BUFFER test bench setup for BAS Technique**

For two input AND, and XOR gates, in order to sensitise fault propagation, it becomes essential to put one input in a non-controlling value, when the fault is present at the other input. A line whose value in the test 't' changes in presence of the fault 'f' is said to be sensitised to the fault 'f' by the test 't' [2]. A path composed of sensitised lines is called a *sensitised path*. While applying a logic 1 to one input of the AND gate makes this input non-controlling, and allows fault propagation from the other input, applying a logic 0 forces its output to zero, and thus controls the output, and blocks fault propagation through the other input. Logic 0 is used in the XOR test bench for this study, even though both 1 and 0 are non-controlling values.

Input buffers are employed to stabilise the sensitising signal. Table 2.2 presents the simulation results to determine the number of buffers required to stabilise the input

signal. This table presents the output noise margin of the gates for a given bias voltage. The title of the table gives the speed grade and the type of the gate. The first row gives the bias voltage applied (in Volts), and the second row gives the input voltage (in mVolts). In the next 5 rows, the first column gives the position of the gate (rank) in the chain. This table shows that when the bias is sufficiently large, the signal converges to a steady value towards the end of the fifth gate. For instance, from table 2.2, for a bias voltage of 0.88V, the output amplitude is settling at 65mV. However, for higher bias voltages, the signal amplitude stabilises to a steady value with only few input buffers as illustrated in figure 2.5. We see that for a bias of 0.94 Volts, the amplitude remains constant at the output of all the buffers of the chain. Therefore, while more buffers are required to stabilise the input signal for lower bias voltages, only a few buffers are required for higher bias voltages. Since in this study, we vary the bias to detect defects, we use five buffers connected in series to stabilise the input signal.

**Table 2.2 Grade 3 BUFFER chain. Differential voltages representing a signal in mV as a function of the bias and rank in a defect-free chain when a 250 mV input signal is applied to the chain.**

| Bias (V) | 0.85 | 0.872 | 0.875 | 0.88 |
|---|---|---|---|---|
| i/p (mV) | 250 | 250 | 250 | 250 |
| 1 | 53.71 | 70.66 | 73.05 | 77.1 |
| 2 | 41 | 61.33 | 64.24 | 69 |
| 3 | 34.87 | 57.76 | 61 | 66.4 |
| 4 | 30.88 | 56.2 | 59.6 | 65.17 |
| 5 | 28.05 | 55.3 | 58.95 | 65 |

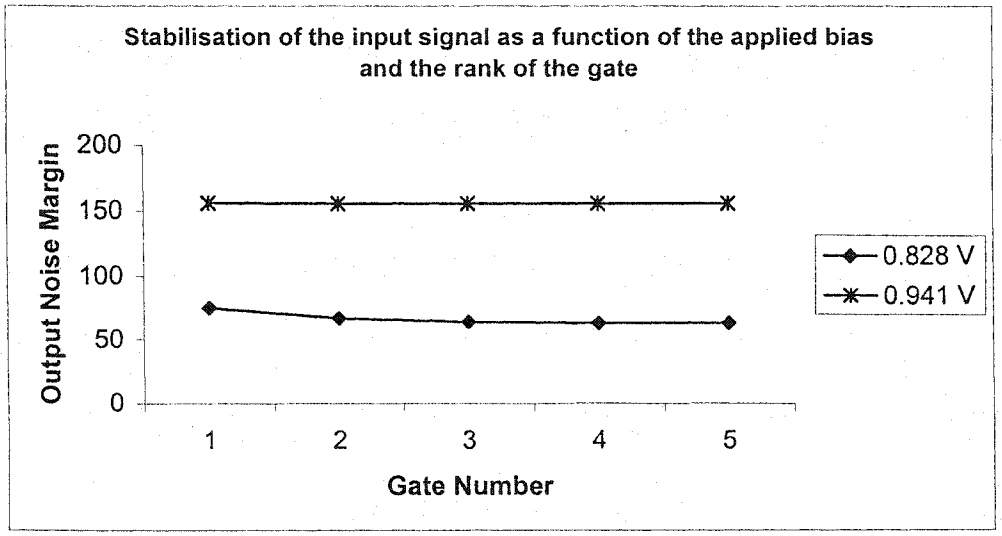


**Figure 2.5 Stabilisation of the input signal as a function of the applied bias for grade 0 BUFFERs**

The test bench setup is simulated for various bias voltages. Simulations were carried out with both defective and defect-free chains of various speed grades. We are interested in

identifying the defects that lower the output noise margin of the Device Under Test (DUT). A defect is simulated by inserting a 100-Ohm short at the input of a gate called the DUT. Such a defect is a good representative fault model for any defect that reduces the fault margin severely. Reduced noise margin faults can be detected by comparing the output amplitude against a preset threshold value, thus resulting in good defect coverage. We aim at inducing stuck-at behaviour in defective chains, by reducing the bias, to distinguish them from defect-free chains. Since two input AND, and XOR gates are considered for the analysis, we consider the following two cases for study:

- A100 Ohm short is injected between the input pair a - ab of the DUT, while the other input pair b - bb is made non-controlling.
- A 100 Ohm short is injected between the input pair b - bb of the DUT, while the other input pair a - ab is made non-controlling.

This short has a strong impact on the output amplitude produced by the gate. Such a defect either forces the DUT to exhibit stuck-at behaviour, or reduces the output amplitude of the DUT. This type of defect was chosen for the following reasons: Since bipolar CML gates are differential, 'op' and 'opb' should toggle in opposite directions in defect-free gates. But the presence of a short at the input prevents the output signals 'op' and 'opb' from crossing each other as shown in figure 2.6. This defect is also a test to the gain and the fault masking capabilities of bipolar CML gates.

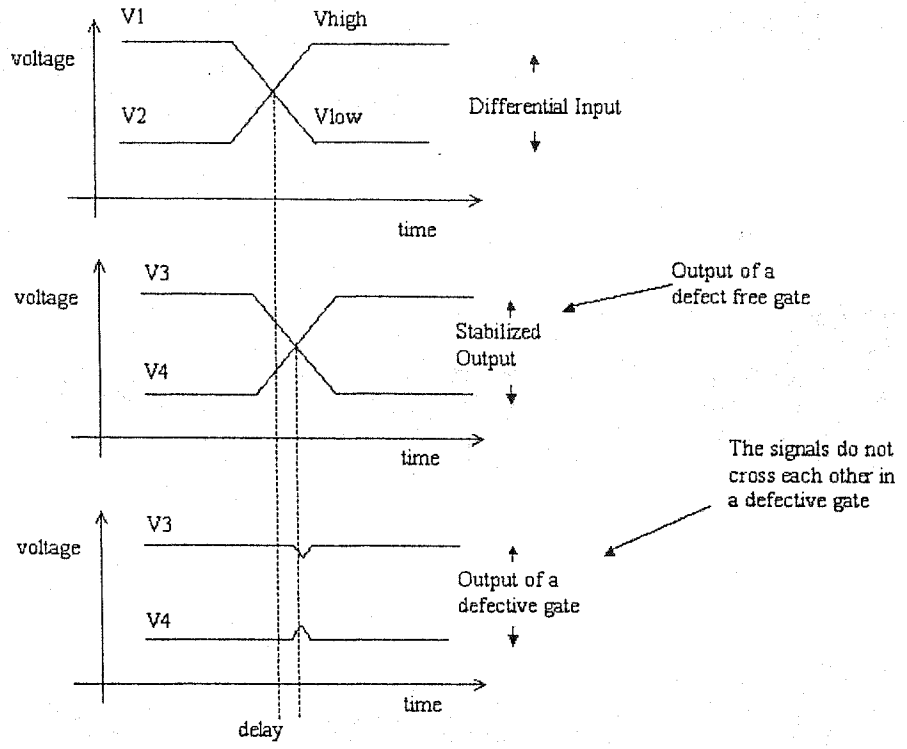


**Figure 2.6 Waveforms depicting the input and output values of the defect-free and defective gates**

A typical simulation output for a bias of 0.83V for a grade 0, defective AND chain is shown in figure 2.7. The output waveform shows that indeed in the presence of such a defect, the output signals do not cross each other. While gates of speed grades 0 to 3 use the same type of bias generator that produces 1.104 V, grades 4 to 6 use a different type of bias generator that produces 1.1653 V. The values of the applied signals and bias voltages are presented in Appendix I.

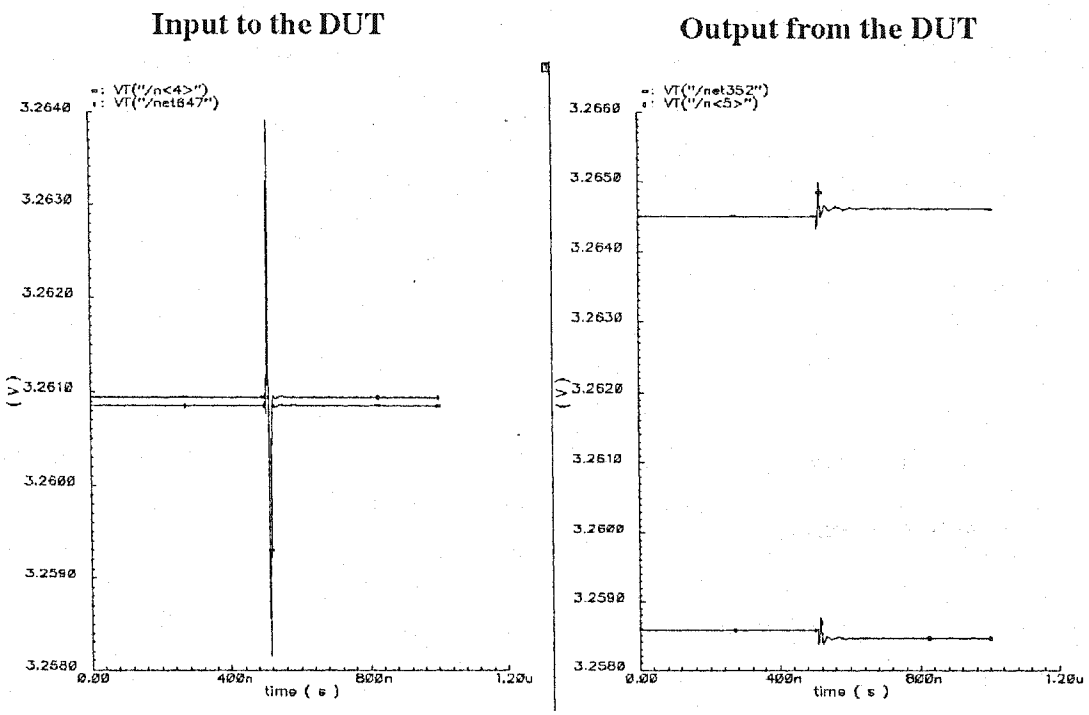


**Figure 2.7 Response of a grade 0 AND chain with a 100 Ohm short at the a-ab input**

In the test bench, while five buffers are placed before the DUT to stabilise the signal, thirty-four gates of the same type as the DUT are placed after the DUT, in order to study the effect of a defect (fault propagation) for a considerable depth of the chain. In the NT25™ technology, since the buffers have a fan-out of five for gates of the same speed grade, chains of certain number of buffers are used to drive every set of five 2-input gates connected in parallel on their respective non-controlling input line. Recall from table 2.2 that five buffers are needed to stabilise the input signal. Figure 2.8 shows the response of a grade 0 BUFFER chain subjected to BAS testing, for different bias voltage values.

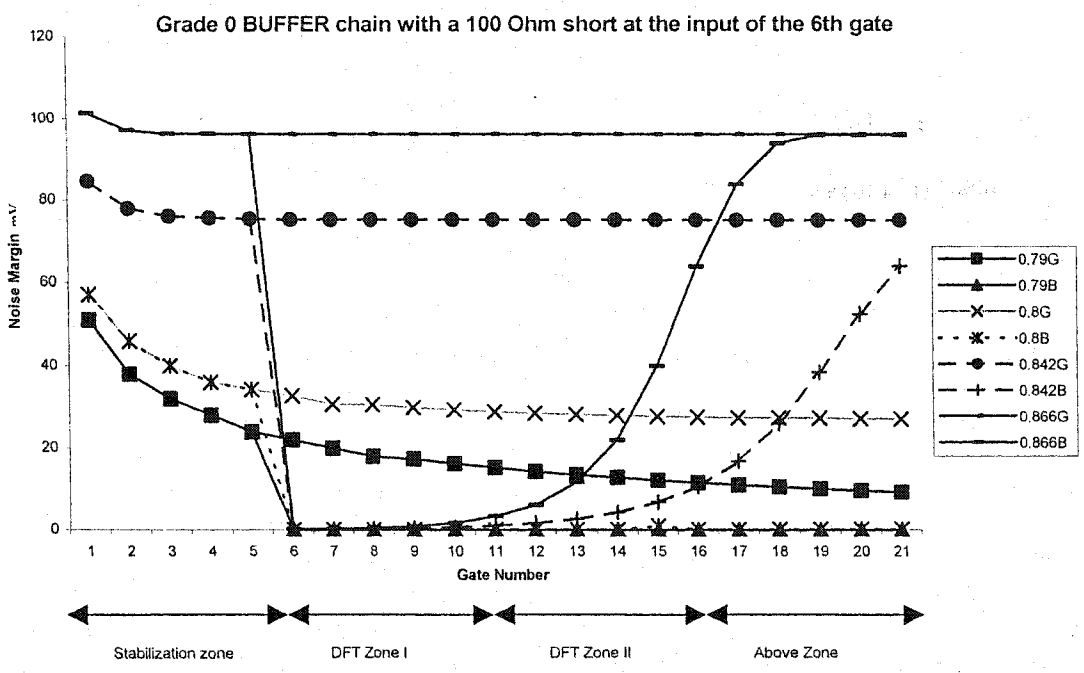


**Figure 2.8 Output amplitudes of defective & defect-free BUFFER chain for different bias voltages**

The output amplitude of each gate of the chain is plotted for different bias values, for both defective and defect-free chains. G denotes a defect-free (Good) chain and B denotes a defective (Bad) chain. We see that the output amplitude is different for different bias voltages. While a defect-free chain (Good chain) exhibits low amplitude due to reduced bias in the first few levels, a defective chain either outputs very low output amplitude or no output amplitude. The signal falls steeply at the input of the DUT. Four zones can be derived from figure 2.8 for BAS technique. In the 'stabilisation zone', the input signal is passed through a few BUFFERs to be stabilised. The difference in the remaining noise margin between defective and defect-free gates is high in 'DFT Zone I', and hence it is very useful for detection. However, the difference in remaining noise margin between good and bad chains is low in 'DFT Zone II', as the gates tend to

amplify low amplitude signals in this zone. In the 'Above Zone', the signal from the defective chain is fully regenerated. The number of gates in the chain that fall in each of these zones depends upon the depth of the chain, the type and speed grade of the gate, and the applied bias voltage.

## 2.3 Simulation results

So far, we have seen the response of bipolar CML BUFFERs to BAS testing. Now let us study the response of bipolar CML AND, and XOR gates. An XOR test bench is presented in figure 2.9. BUFFERs are single input gates. Whereas AND, and XOR gates have two inputs. For a two input gate, one input has to be made non-controlling, to study fault propagation through the other input. Sensitisation can be achieved by applying the following voltages:

- The inputs 'b' and 'bb' of the AND gate are connected to $V_{high}$ (3.3V dc) and $V_{low}$ (3.05V dc) respectively (logic 1). The input pair 'a' and 'ab' are connected to 'high' signal (input1 in Appendix I) and 'low' signal (input2 in Appendix I) respectively, or 'a' is connected to input2 and 'ab' is connected to 'input1'. Thus, one input is always at logic 1, forcing the output to depend upon the other input, making the gate transparent, reducing it to a buffer. Note that the output of AND gate = a AND b = a, when b = 1.

- Similarly, the inputs 'b' and 'bb' of the XOR gate are connected to $V_{low}$ (3.05V dc) and $V_{high}$ (3.3V dc) respectively (logic 0). The input pair 'a' and 'ab' is connected to input1 and input2 respectively, or 'a' is connected to input2 and 'ab' is connected to 'input1'. Note that the output of XOR gate = (a AND bb) OR (b AND ab) = a, when b = 0.

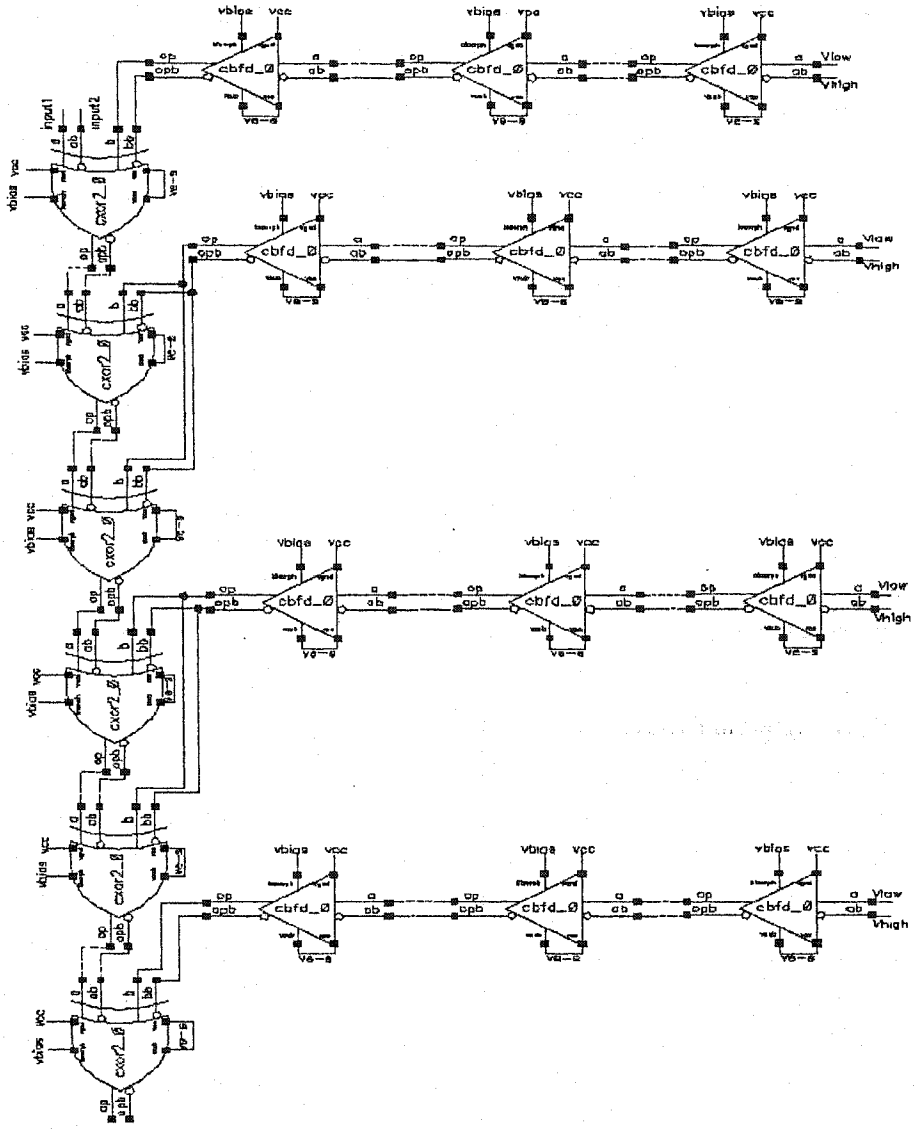


**Figure 2.9 A segment of the test bench employed for the XOR chain.**

Simulations showed that an output NM in the range of 35 to 50 mV would better discriminate a fault free chain and a faulty one. However, this is still not valid for all gates types and speed grades. There are cases where the faulty chain outputs a fully regenerated signal for this bias voltage. However, reducing the threshold below this value will increase the errors due to noise signal. Our objective is to have one threshold voltage for all gate types and speed grades. The following section presents some of the results obtained by simulating a chain of gates that are subjected to BAS testing. These results help to understand BAS technique.

## 2.4 Observations

Table 2.3 presents the results obtained by subjecting a grade 0 AND chain to BAS testing. The test bench is the same as that of XOR, except that the XORs are replaced with the ANDs. As the title of the table suggests, a 100-ohm short is inserted at the a-ab input of the $6^{th}$ device called the DUT. The first row gives the applied bias in Volts. G denotes a fault-free chain (Good), and B denotes a faulty chain (Bad). The second row gives the input voltage in mV. The first column gives the rank of the gates with respect to the DUT in the chain. -1 is the gate before the DUT, -2 is 2 gates before the DUT and so on. Likewise, 1 is the gate after the DUT, 5 is five gates after the DUT, and so on. The rest of the cells in the table give the output amplitude in mV. All similar tables have the same format as that of table 2.3, unless indicated otherwise.

**Table 2.3 Output amplitude (in mV) produced by a grade 0 AND chain with a 100 Ohm short at the a-ab input of the DUT**

| Bias V | 0.828G | 0.828B | 0.941G | 0.941B | 0.942G | 0.942B |
|---|---|---|---|---|---|---|
| i/p | 250 | 250 | 250 | 250 | 250 | 250 |
| -4 | 75.12 | 75.12 | 156 | 156 | 157 | 157.1 |
| -3 | 66.95 | 66.95 | 155.6 | 155.6 | 156.4 | 156.7 |
| -2 | 64.15 | 64.15 | 155.6 | 155.6 | 156.4 | 156.7 |
| -1 | 63.05 | 63.05 | 155.6 | 147.9 | 156.4 | 156.4 |
| DUT | 61 | 0.085 | 155.6 | 0.21 | 156.4 | 0.213 |
| 1 | 56 | s-@-f[2] | 152.4 | 0.2 | 153.6 | 0.224 |
| 3 | 50.98 | s-@-f | 152.2 | 0.15 | 153.4 | 0.33 |
| 5 | 47.97 | s-@-f | 152.2 | s-@-f | 153.4 | 1.17 |
| 6 | 46.97 | s-@-f | 152.2 | s-@-f | 153.4 | 3 |
| 11 | 43 | s-@-f | 152.2 | s-@-f | 153.4 | 151.4 |
| 16 | 36.97 | s-@-f | 152.2 | s-@-f | 153.4 | 153 |
| 21 | 25.97 | s-@-f | 152.2 | s-@-f | 153.4 | 153 |
| 26 | 2.72 | s-@-f | 152.2 | s-@-f | 153.4 | 153 |
| 31 | 0.034 | s-@-f | 152.2 | s-@-f | 153.4 | 153 |

From table 2.3, when the bias voltage is 0.942V, a defective chain produces an output, which is the same as that of the defect free chain only after 14 gates. Clearly, when the

[2] s-@-f denotes stuck-at fault

bias voltage is reduced below a particular limit, (0.828V in this example) the gain of the gate is very low, and the output amplitude is negligible for a fault-free chain, for the considered depth. Thus, the useful range for detection is determined by both the defect-free and the defective chains, with the defect-free chain determining the lower bound of the range (since the output signals do not cross each other in a defect-free chain for very low bias voltages) and the defective chain determining the upper bound of the range (since the signal is fully regenerated in a defective chain). Also, the useful voltage range depends on various other parameters as discussed later in this chapter.

Simulations show that the chain can be very sensitive to bias when close to the threshold, where it starts (or ends) exhibiting stuck-at fault behaviour, even for a change in the bias voltage by a mV. In table 2.3, the defective chain exhibits a stuck-at fault when the applied bias is 0.941 V, but behaves normally, producing the same output amplitude as that of the defect-free chain when the bias is 0.942 V. This signal regeneration is shown in figure 2.10. It implies that after a particular bias value, the output amplitude varies widely even for a very small variation in the applied bias. Thus, the grade 0 AND chain BAS tested for the injected fault exhibits a strict upper boundary at 0.941 V, under the set constraints.

Figure 2.10 represents a typical response obtained by subjecting the defective grade 0 AND chain to a bias of 0.942 V. It clearly illustrates in stages, for a sufficiently high bias voltage applied to the chain, the regeneration of a very low amplitude signal as the signal

passes through a few gates in the chain, leaving no trace of the defect at the output of the chain. Thus, after a few levels, the defect is completely masked. Hence, it becomes imperative to place a detector once in every few gates in order to successfully detect such defects, before the signal is fully regenerated. For higher applied bias voltages for BAS testing, the signal regenerates quickly. Hence, more detectors will be required when the bias voltage is high. Therefore, a choice has to be made between the number of detectors used and the applied bias. Obviously, we want to minimise the number of detectors.

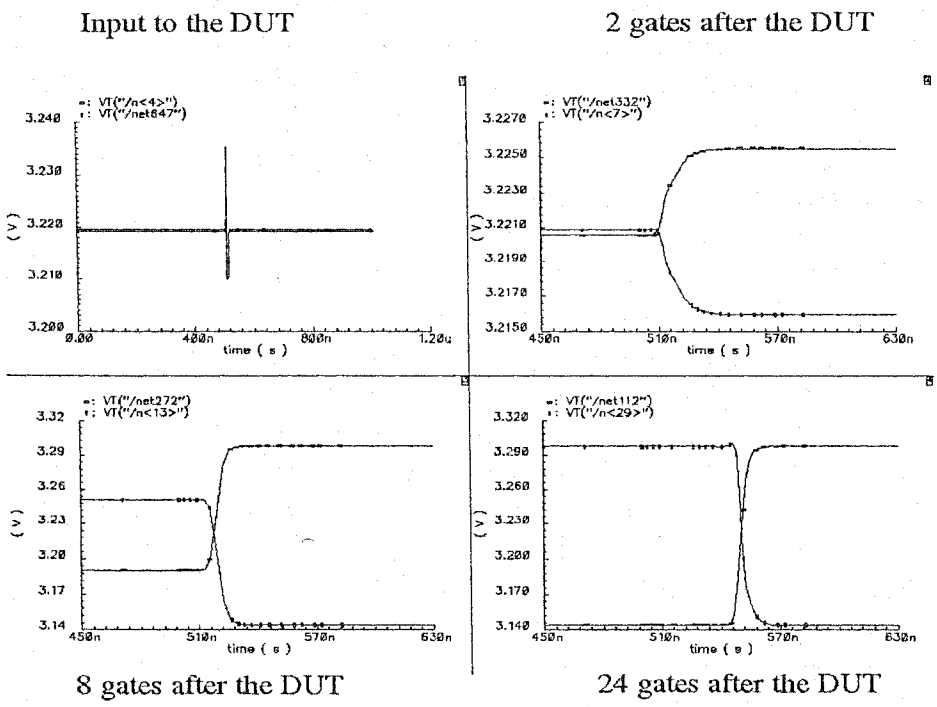


**Figure 2.10 Response of grade 0 AND chain with a defect at the a-ab input of the DUT, bias = 0.942 Volts**

Also, the response of the AND gate is found to be different according to the input line that is sensitised. This is due to the asymmetry of the gate. While table 2.3 presents the results for grade 0 AND chain, when the b - bb line is connected to a non-controlling value and the toggling inputs are connected to the a - ab line, using the same presentation format, table 2.4 presents the results obtained with a - ab line connected to a non-controlling value, when the toggling inputs are connected to the b - bb line of the AND gate.

**Table 2.4 Output amplitude (in mV) produced by a grade 0 AND chain with a 100 Ohm short at the b-bb input of the DUT**

| Bias V | 0.833G | 0.833B | 0.85G | 0.85B | 1.1G | 1.1B |
|---|---|---|---|---|---|---|
| i/p | 250 | 250 | 250 | 250 | 250 | 250 |
| -4 | 78 | 78 | 90.2 | 90.2 | 281 | 281 |
| -3 | 71 | 71 | 84.3 | 84.3 | 281 | 281 |
| -2 | 68 | 68 | 82.63 | 82.63 | 281 | 281 |
| -1 | 67.6 | 67.6 | 82.45 | 82.45 | 281 | 281 |
| DUT | 68.2 | 0.093 | 83.48 | 0.113 | 284.5 | 0.37 |
| 1 | 56 | s-@-f | 74 | s-@-f | 280.5 | s-@-f |
| 2 | 50 | s-@-f | 71 | s-@-f | 280.5 | s-@-f |
| 5 | 42 | s-@-f | 70 | s-@-f | 280.5 | s-@-f |
| 11 | 37 | s-@-f | 70 | s-@-f | 280.5 | s-@-f |
| 21 | 36 | s-@-f | 70 | s-@-f | 280.5 | s-@-f |
| 31 | 36 | s-@-f | 70 | s-@-f | 280.5 | s-@-f |

Table 2.4 shows the case of a faulty signal that is unable to recover even for an applied bias of 1.1 Volts. Recall that 1.1 V is the bias value required for the gate to operate in the normal mode. Therefore, for the set constraints, this fault can be detected in the functional mode itself.

By comparing the results shown in tables 2.3 and 2.4, we see that while in one case the chain regenerates the signal even for a bias of 0.942 Volts, in the other case the chain does not regenerate the signal even for a bias voltage of 1.1 Volts. The only difference in the test bench between the results presented in these tables is that, different input lines are sensitised in each case. The results are not symmetric. With a suitable bias, when a

defect is present at the input driving the lower differential pair of figure 1.2, the AND chain regenerates the signal. However, the fault present at the upper differential pair propagates to a greater depth even for the regular bias voltage. Also, by looking at the schematic of the OR gate presented in figure 1.2, we see that while the transistor Q6 drives a differential stage, the transistor Q5 does not. The AND (OR) gate is asymmetric by design. Thus, the asymmetry of the AND gate imposes a limit on the bias voltage for BAS based on the input line that is sensitised.

A large number of results like those shown in table 2.3 and table 2.4 were generated by manually searching for the limit points that enable or prevent the detection of a specific fault considered in the analysis. These results are summarised below. For the chain considered (30 gates after the DUT), table 2.5 presents the useful range of bias voltages (in Volts) for BAS testing, for speed grades 0 and 3, for each type of the gates studied. Results are reported for each defective input of a 2-input gate.

**Table 2.5 Useful bias voltage ranges for fault detection using BAS technique for a 30 gate deep chain**

| Gate | Grade 0 (V) | Grade 3 (V) |
|---|---|---|
| BUFFER | 0.8 - 0.815 | 0.84 - 0.85 |
| XOR (a - ab) | 0.815 - 0.825 | 0.865 - 0.875 |
| XOR (b - bb) | 0.82 - 0.83 | 0.868 - 0.875 |
| AND (a - ab) | 0.828 - 0.941 | >0.88 – 1.1 |
| AND (b - bb) | 0.8 - 1.1 | Not Available[3] |

A suitable range of bias voltages for all gates of both speed grades is given by the largest voltage in the lower end of the range listed in the table for all gates (0.88 V in the above table), and the smallest voltage of the upper end of the range listed in the table (0.815 V). Note that this table reports the case of the grade 3 AND gate, which exhibits stuck-at fault for the fault-free case itself over the whole bias range applicable to other gates. The absence of an intersection between these intervals questions the usability of BAS testing for fault detection.

Also, note that in the above table, the usable range of bias voltages for BAS testing for XORs when the input a-ab is sensitised is not the same as that when the input b-bb is sensitised. However, from the schematic of the bipolar CML XOR gate shown in figure 2.3, we would expect the gate to be more symmetrical than an AND gate. But, the

[3] Results for grade 3 AND gates were not collected because, from the table, the usable bias voltages do not overlap for grade 0 BUFFER and XOR gates.

difference arises from the fact that the current sources of the level shifting transistors are also receiving a reduced bias, thereby altering the $V_{be}$ drop of the level shifting transistors as well. Even for a very small change in the diode voltage, the diode current changes significantly. Thus altering the bias makes an otherwise symmetric gate asymmetric. This compounded to the fact that the lower and the upper differential pairs of the AND gate are not already balanced, which makes the AND gate asymmetric as well. We know that in bipolar CML technology, level shifting transistors are provided for each of the lower differential pairs. The number of differential pairs is equal to the number of inputs to the gate. The asymmetry of multiple input bipolar CML gates is exposed by BAS, making the employability of BAS for testing such gates challenging.

We do not have a common interval for the different gates shown in table 2.5. To circumvent this problem, we will explore BAS's feasibility for the considered fault as a function of gate chain. This corresponds to the insertion of detectors at regular intervals when a logic chain gets very deep. Hence, the applicability of this technique as a function of the number of gates used in the chain (depth of the chain) was determined. Table 2.6 and table 2.7 present results similar to those reported in table 2.5 but for 10 and 15 gate deep chains after the DUT.

**Table 2.6 Usable range of bias voltages for BAS testing, for a 10 gate deep chain**

| Gate | Grade 0 (Volts) | Grade 3 (Volts) |
|---|---|---|
| BUFFER | 0.79 - 0.9 | 0.85 - 0.88 |
| XOR (a - ab) | 0.812 - 0.97 | 0.867 - 0.887 |
| XOR (b - bb) | 0.816 - 0.894 | 0.869 -0.887 |
| AND (a - ab) | 0.825 - 0.941 | 0.876 - 0.917 |
| AND (b - bb) | 0.827 - 1.1 | 0.878 - 0.941 |

**Table 2.7 Usable range of bias voltages for BAS testing, for 15 gate deep chain**

| Gate | Grade 0 (Volts) | Grade 3 (Volts) |
|---|---|---|
| BUFFER | 0.8 - 0.866 | 0.85 - 0.872 |
| XOR (a - ab) | 0.816 - 0.85 | 0.87 - 0.887 |
| XOR (b - bb) | 0.82 - 0.853 | 0.872 - 0.887 |
| AND (a - ab) | 0.828 - 0.941 | 0.88 - 0.917 |
| AND (b - bb) | 0.83 - 1.1 | 0.8803 - 0.941 |

From table 2.6, for the gates studied and within the set constraints, the overlapping voltage zone useful for BAS testing is 0.878 V to 0.88 V. Thus, for a 10 gate deep chain, the overlapping voltage zone is just 2 mV, which is very critical and probably not acceptable in practice. Moreover, from table 2.7, we observe that a 15 gate deep chain has no region in common between grades 0 and 3. A few techniques described below were explored to expand the acceptable region of operation.

## 2.5 Methods attempted to increase the usable range of bias voltages

When analysing the simulation outputs, it was found that the main cause limiting BAS's region of operation is the imbalance of the AND gate at low bias, as demonstrated in tables 2.3 and 2.4. A first possibility is to amplify the signal produced by a gate with a reduced bias, by passing it through a BUFFER that keeps a symmetric behaviour. The BUFFER functions as an amplifier. Thus, for various bias voltages, DC response curves were obtained to determine how the number of gates through which a fault propagates in a detectable manner would increase (thereby increasing the coverage depth) by adding BUFFERs at regular intervals. From simulation results, inserting BUFFERs did not improve the situation much as several BUFFERs were required to obtain a small increase in the output amplitude of the circuit, and hence the usable chain depth did not improve significantly.

Since OR gates have a better gain than BUFFERs, they were connected as BUFFERs in the chain. This is achieved by applying a suitable logic value to one input of the gate, forcing the output to follow the other input i.e., the gate is made transparent to the other input. Again, this did not significantly improve the situation on hand. The outputs obtained by simulating a grade 3 AND chain with a defect at the a-ab input is presented in Appendix II for different cases.

So far we only discussed an ideal design, where the resistor values are as mentioned in the design specification. However, due to process variations, the calculated values are

expected to be different from those obtained after fabrication. Hence, to study the effect of process variations, various parameters of several gates present in the chain were varied randomly and the resulting chain was simulated as reported in the following section.

## 2.6 Simulations taking process variations into account

This section reports the simulation results for gate chains where the values of some current sources and load resistors of the gate are varied by up to $\pm 20\%$ of their nominal value. For every gate type - speed grade combination, one chain with random parametric variation is generated. The location of these variations in the chain is random. But, in all cases, the gate immediately after the DUT is always subjected to a change in one of its resistors. The variations introduced are random and no two chains are alike. Approximately 25% of the gates in the chain have such process variations modelled on different resistors, one resistor per gate chosen. The results thus obtained are presented in table 2.8 and table 2.9, where the tables hold the same format as table 2.6 and table 2.7.

**Table 2.8 Usable range of bias voltages for a 10 gate deep chain subjected to random variations**

| Gate | Grade 0 (Volts) | Grade 3 (Volts) |
|---|---|---|
| BUFFER | 0.79 - 1.1 | 0.845 - 0.89 |
| XOR (a - ab) | 0.816 - 1.0 | 0.867 - 0.9 |
| XOR (b - bb) | 0.817 - 1.1 | 0.871 - 0.91 |
| AND (a - ab) | 0.822 - 1.1 | 0.877 - 0.91 |
| AND (b - bb) | 0.827 - 1.1 | 0.8765 - 0.91 |

**Table 2.9 Usable range of bias voltages for a 15 gate deep chain subjected to random variations**

| Gate | Grade 0 (Volts) | Grade 3 (Volts) |
|---|---|---|
| BUFFER | 0.795 - 1.1 | 0.847 - 0.872 |
| XOR (a - ab) | 0.818 - 1.0 | 0.87 - 0.885 |
| XOR (b - bb) | 0.82 - 1.1 | 0.873 - 0.91 |
| AND (a - ab) | 0.8255 - 1.1 | 0.879 - 0.91 |
| AND (b - bb) | 0.8285 - 1.1 | 0.8805 - 0.91 |

These experiments produced bias voltage ranges for grade 3 gates that are subset of the corresponding grade 0 gates with same or different random perturbation for each type of gate/input combination. Thus, in these experiments, grade 3 determines the usable voltage range for testing. For a 10 gate deep chain, the usable range is found to be 0.877 V to 0.89 V, which is 13 mV. For a 15 gate deep chain, there is no voltage range in common due to grade 3 BUFFER. Thus, the imposed process variations indeed enhanced the situation, and a 13 mV range is obtained for a 10 gate deep chain. However, this improvement is not significant.

Since the variations introduced are random, it is also possible that instead of decreasing the output amplitude of a faulty chain, the variations may increase it. This situation is encountered in the grade 3 XOR chain with a defect at the b-bb input, characterised in table 2.10. This table shows that the defective chain exhibits a stuck-at behaviour initially. However, after a few gates, the signals overlap each other and give out small amplitude. If the successive gates had a large enough bias current in a long chain, this

signal would have been amplified considerably and the defect could have been masked. Since the gates were subject to a random variation, which in this case happened to worsen the weak signal, the defect was not masked. A typical response of this behaviour is depicted in figure 2.11 for a bias of 0.873 Volts. In the output from the DUT, only spikes appear to show the signal as being differential. The signals actually do not cross each other.

**Table 2.10 Output amplitude (in mV) produced by a grade 3 XOR gate chain taking process variations into account and with a defect at the b-bb input of the DUT**

| Bias V | 0.871G | 0.871B | 0.873G | 0.873B | 0.91G | 0.91B |
|---|---|---|---|---|---|---|
| i/p | 250 | 250 | 250 | 250 | 250 | 250 |
| -4 | 70 | 70 | 71.47 | 71.47 | 102.75 | 102.75 |
| -3 | 60.47 | 60.47 | 62.2 | 62.2 | 98.6 | 98.6 |
| -2 | 56.63 | 56.63 | 58.9 | 58.9 | 97.88 | 97.88 |
| -1 | 54.95 | 54.95 | 57.2 | 57.2 | 97.6 | 97.6 |
| DUT | 54.7 | 1.07 | 57.15 | 1.11 | 98.66 | 1.1 |
| 1 | 40.18 | 0.95 | 43.1 | 1.97 | 92 | 3.3 |
| 2 | 30.37 | s - @ - f | 33.73 | s - @ - f | 89.17 | s - @ - f |
| 3 | 26.6 | s - @ - f | 30.34 | s - @ - f | 90.21 | s - @ - f |
| 4 | 23.8 | s - @ - f | 27.92 | s - @ - f | 89.7 | s - @ - f |
| 5 | 20.72 | 0.63 | 24.86 | 0.35 | 88.5 | s - @ - f |
| 6 | 18.92 | 0.62 | 23.39 | 0.3 | 89.32 | s - @ - f |
| 7 | 17.36 | 0.62 | 22 | 0.3 | 89.4 | s - @ - f |
| 8 | 12.53 | s - @ - f | 17.4 | 0.4 | 88.34 | s - @ - f |
| 9 | 11.74 | s - @ - f | 16.89 | s - @ - f | 89.3 | s - @ - f |
| 10 | 11.1 | s - @ - f | 16.46 | s - @ - f | 89.6 | s - @ - f |

From the figure below, we see that the chain that exhibited stuck-at behaviour after the DUT, had a tendency to regenerate the signal after only 4 gates. The chain, being subjected to random variations, restored the stuck-at behaviour after a few levels as shown. It may also be possible that the defect be masked by the successive gates of the chain, due to the their high gain characteristics.

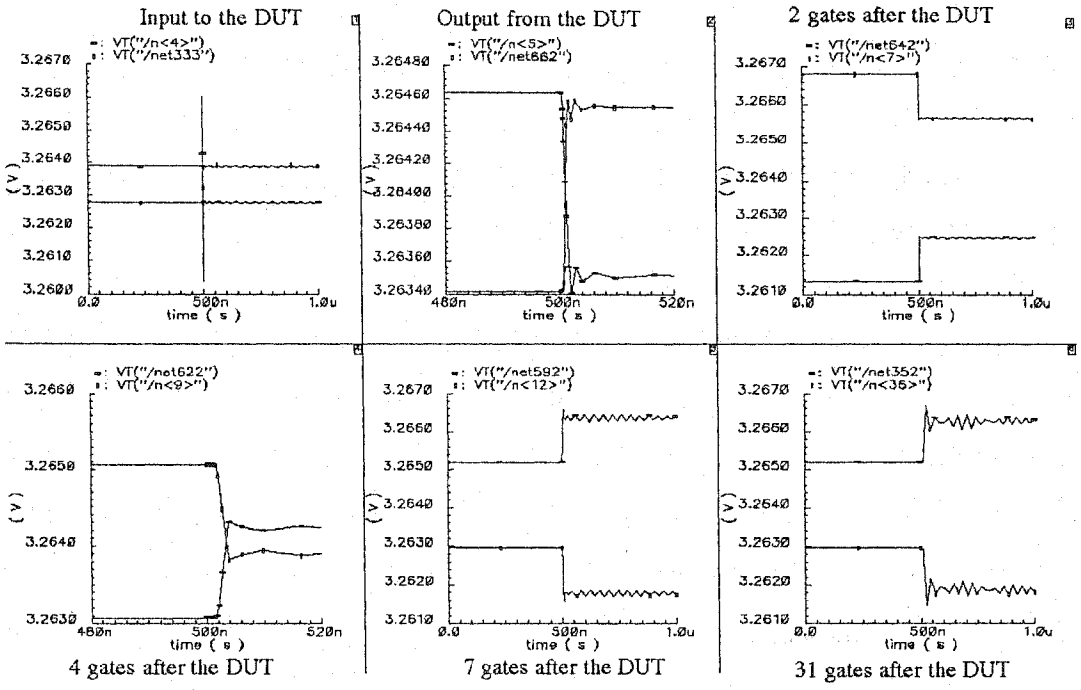


**Figure 2.11 Response of a grade 3 XOR chain with a defect at the b-bb input**

## 2.7 Summary and Conclusions on BAS testing

In this chapter, we discussed how the gain of the gate could be altered to detect manufacturing defects. We also showed how this technique makes a gate asymmetric, and discussed a few methods to overcome them. We also studied the effects of process variations on BAS testing technique. We also discussed how, with the setup used, there

is little or no usable bias voltage in common for different gates of different speed grades. In spite of our efforts, we did not succeed in finding an acceptable region of operation for the bias setting in BAS technique. The usable range of bias voltage obtained is too narrow when taking process variations into account. Also, noise signals extrinsic and intrinsic to the chip might render the testing method extremely unreliable.

# CHAPTER 3

# IMBALANCE TESTING TECHNIQUE & STRESS ACCUMULATION

## 3.1 Introduction

A variety of faults are possible with CML gates. To name a few, stuck-at faults, truth table faults, delay faults, shift of average value faults, etc., have been observed [4]. Conventional testing methods detect a good proportion of these faults. However, to ensure a complete coverage of all possible faults in CML gates, we also study a testing technique proposed for ECL by Anderson [29] and patented by GERSBACH, J. E., and MOSER, J.J., [19] that we call the DC Imbalance Test Technique (ITT).

The test method proposed by Anderson, stresses the entire circuit just enough such that the circuit is imbalanced, and all marginal signals are sufficiently degraded to cause logic errors. In this chapter, we study the imbalance testing technique as applied to bipolar CML family. We focus our attention on BUFFER, AND, and XOR gates. We explain the concept of imbalance testing technique, and show some of the results obtained. We also discuss the phenomenon of stress accumulation observed in defect-free bipolar CML AND gates, and also discuss some workarounds to overcome stress accumulation.

## 3.2 Functionality of AND gates

Figure 3.1 shows the schematic of a bipolar CML AND gate with the imbalance test circuit. Transistors Q3 and Q4 are level shifters, used to avoid saturations of the

transistors in the lower differential pair (Q5 and Q6). Q7, Q8 and Q9 are current source transistors. The output of an AND gate is high when all of its inputs are high, and low otherwise. In the schematic, when 'b' is high, transistor Q6 conducts, when 'a' is high, Q2 conducts and therefore 'op' is high; when 'b' is high and 'a' is low, Q6 and Q1 conduct, and 'opb' is high. The truth table of the AND gate is summarised in table 3.1.

**Table 3.1 Truth table of AND gate and the switching transistors4**

| a | b | Transistors that conduct | Output |
|---|---|---|---|
| 0 | 0 | Q1, Q5 | 0 |
| 0 | 1 | Q1, Q6 | 0 |
| 1 | 0 | Q2, Q5 | 0 |
| 1 | 1 | Q2, Q6 | 1 |

Note that, while the transistor Q6 drives a differential stage, the transistor Q5 does not. Also note that, two collectors are connected to the 'op' line in the schematic of the AND gate, and only one transistor's collector is connected to the 'opb' line, making the AND gate asymmetric. The consequences of this asymmetry on the proposed imbalance testing technique are studied in detail in this chapter, and in the next chapter. The following section studies the 'Imbalance Test Technique' as applied to bipolar CML gates.

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4 Note that input ab is the complement of input a, and output bb is the complement of output b. If a = 0, then ab = 1.

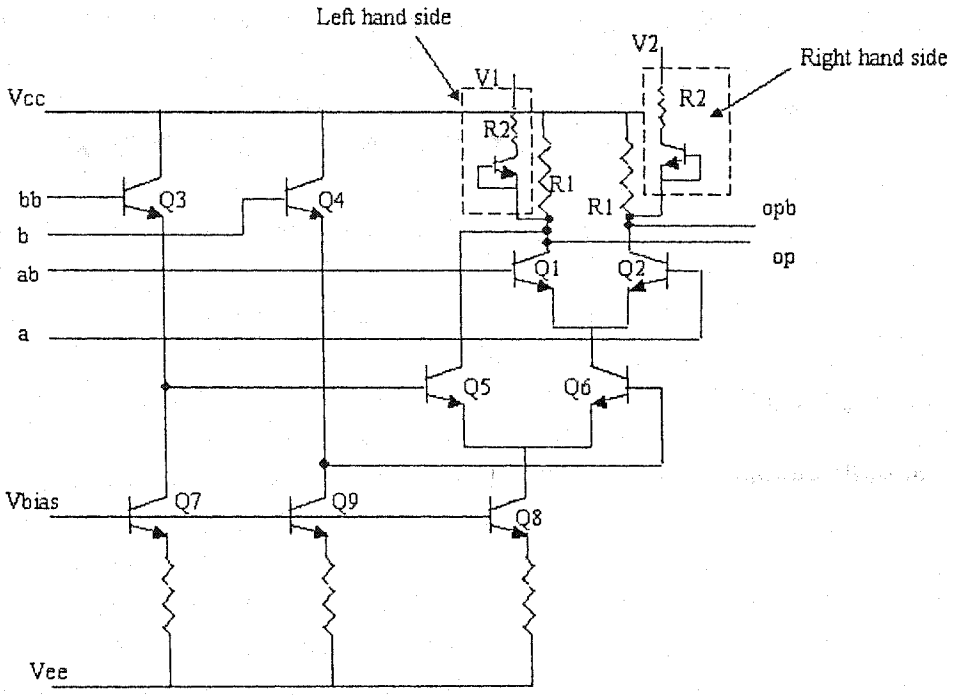



**Figure 3.1 Schematic of Bipolar CML AND gate with imbalance test circuit**

## 3.3 Imbalance Test Technique

The original imbalance testing technique reported by Anderson [3, 19] was for ECL family. It was proposed with one Schottky diode in each test branch. Imbalance Test Technique (ITT) is a two-pass testing technique. A test line is connected to each of the output lines in the differential circuit. In ITT, the voltages $V_1$ and $V_2$ (see figure 3.1) are connected to Vcc in the normal mode. In the test mode, lines $V_1$ and $V_2$ are operated independently. A differential circuit would be imbalanced only when one line has a lower voltage than the other. Thus, when either $V_1$ or $V_2$ is sufficiently lowered with respect to Vcc, the corresponding test branch conducts. The imposed drop across the

pull-up resistor $R_1$ is the imbalance ($V_{imbalance}$) applied to the gate. The drop is significantly higher when the imbalanced side is at a high logic value.

When a signal is low, stressing it moves the differential signals further apart, increasing the differential amplitude of the 'low' signal, and the remaining noise margin is high. This is not desirable for fault detection. If a signal is high, and the corresponding differential line is imbalanced, then the differential amplitude of the 'high' signal goes low. Reduced output amplitude helps in fault detection since several gates are needed after the DUT to restore this signal. Hence, in this study, we ignore the case where the low signal is imbalanced.

The following notation is used throughout the study: In the upper differential pair of the schematic, node $V_1$ is always at the reader's left hand side branch of the differential pair. Likewise, $V_2$ is on the reader's right hand side branch of the differential pair. In the schematic of figure 3.1, $V_1$ is connected to transistor Q1 and $V_2$ is connected to transistor Q2. Note that the transistor names need not be the same always. A clear distinction as to whether $V_1$ or $V_2$ is connected to 'op' or 'opb' is not possible with bipolar CML, because certain logic gates are obtained by just inverting the input and the output lines of other logic gates. For example, AND logic is obtained by inverting the inputs and outputs of the OR logic, as shown in figure 2.2 [4].

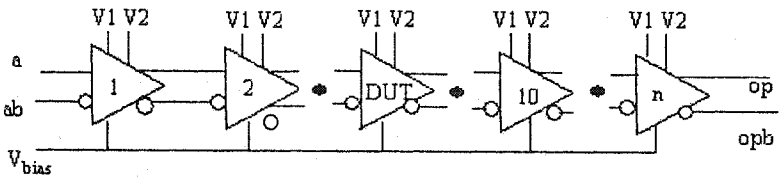



**Figure 3.2 BUFFER test bench employed for ITT**

With ITT, the gates are imbalanced to detect manufacturing defects. A typical test bench using BUFFERs, for characterising ITT is shown in figure 3.2. Here, 'n' is the total number of gates in the chain. The setup remains the same for AND, and XOR gates, except that the BUFFERs are replaced with the respective gates. BUFFERs are still used in the AND, and XOR test bench to stabilise the input signals, and to sensitise one input. If the second input of an AND gate implemented as shown in figure 3.1 is driven by a non-controlling signal, the gate as driven by its first input reduces to a buffer.

The value of $V_1$ and $V_2$ connected to the imbalance test arms dictate the amount of imbalance applied to the gate. The imbalance voltage is given by $I_1R_1$. $R_1$ is fixed in the design. Therefore, to change the current, the voltage has to be altered. It is desirable to have the same voltage for all gate types and all speed grades, as $V_1$ and $V_2$ will be brought out as external pins, connecting to all the gates. A defect-free gate should be able to withstand the applied imbalance without producing errors. The right value for all the speed grades and all the gate types has to be determined first. Thus, if we fix $V_1$, in the test mode, the current $I_1$ drops across the imbalance resistor $R_2$.

In some speed grades, for a given $V_1$ or $V_2$, the value of $R_2$ required is very high to achieve the desired imbalance level, and these resistors may become too large. But, the NT25™ technique imposes a limit on the value of the resistor. A basic step unit in VersArray consists of two transistors and one ~50 KOhm resistor. Thus, if $R_2$ is greater than this value, two BSUs are needed. In order to overcome this limitation, we propose that a second diode may be inserted in each test branch to get some additional voltage drop. In this chapter, some results are reported for test benches having one and two diodes, as required.

The purpose of ITT is to detect defective gates, but if the degree of imbalance is too strong, even defect-free gates may adopt a stuck-at behaviour. Let us first illustrate how this technique effectively differentiates between a defect-free and a defective circuit. To model the manufacturing defects in this study, a defect-free chain is made defective by shorting one of the complementary inputs 'a' and 'ab' (or, 'b' and 'bb') of the Device Under Test (DUT), the first AND gate of the chain, by a 100 Ohm resistor. The two lines being the complement of each other, they will definitely output complementary signals in the defect-free chain. However, in the defective chain, the short forces the two lines to output the same signal, as explained in chapter 2 [27, 14]. Thus, this is a serious defect, and it is used in the analysis of differential bipolar CML gates.

In the considered test bench setup, the outputs of all the gates in the chain are imbalanced. The imbalanced output of one gate is input to the next gate of the chain.

Thus, the gate receives an imbalanced input signal, while its output is already imbalanced. This is called as "double imbalance."

Table 3.2 gives the results obtained by simulating a 20 gate deep chain composed of bipolar CML grade 0 AND gates, with $V_1$ = 2.5 Volts, $R_2$ = 1.5 KOhms using one diode. In this case, five buffers were employed to stabilise the input signal. Gate #5 is the first AND gate of the chain, and it is the DUT. The first column gives the gate rank (gate's position) in the chain. The second column gives the output amplitude (in mVolts) observed on the defect-free (good) chain, and the rest of the columns give the output of the defective chain. The third column gives the output amplitude of a defective chain, not subjected to imbalance testing, where both $V_1$ and $V_2$ are connected to Vcc.

From the 3$^{rd}$ column, we see that even if the signal amplitude is extremely low after the DUT, this fault may escape, due to the high gain characteristics of the CML gates. Thus, the circuit would offer a highly unreliable operation. It is remarkable that this severely degraded signal is quickly regenerated, and the defect may be masked when the chain is not subjected to ITT. The differential signals grow in amplitude in a few levels after the DUT. The defect is masked as the signal passes through a few gates in the chain. It is important to identify such defects because even if the gate functions normally - producing a defect free output, the gate may fail in the field due to various reasons like, temperature, environmental factors, etc.

**Table 3.2 Grade 0 AND chain with a 100 ohm short at a - ab input, $R_2$ = 1.5 K**

| Gate No. | Good | Bad | V1 = 2.5Volts (Bad + ITT) | V2 = 2.5Volts (Bad + ITT) |
|---|---|---|---|---|
| i/p | 250 | 250 | 250 | 250 |
| 1 | 284.3 | 284.3 | 284.5 | 284.5 |
| 3 | 284.3 | 284.3 | 284.2 | 284.2 |
| 4 | 284.23 | 0.39 | 0.39 | 0.39 |
| 5 | 280.1 | 1.95 | s - @ - f | s - @ - f |
| 6 | 280.1 | 9.78 | s - @ - f | s - @ - f |
| 7 | 280.1 | 49.14 | s - @ - f | s - @ - f |
| 8 | 280.1 | 203.7 | s - @ - f | s - @ - f |
| 10 | 280.1 | 280.12 | s - @ - f | s - @ - f |
| 20 | 280.1 | 280.12 | s - @ - f | s - @ - f |

Now we study how ITT can propagate the fault to the last gate of the chain, instead of masking the defect by regenerating the signal. The fourth column of the table gives the output of the chain when $V_1$ is lowered, and the fifth column gives the output when $V_2$ is lowered. We see that all the gates after the DUT exhibit stuck-at behaviour. The imbalance testing technique level shifts one side of a differential signal such that the complementary signals do not cross each other in the presence of a defect, while they still cross in the absence of a defect. Also, stressing the gate sufficiently degrades any marginal signal causing the gates to fail. Thus, the imbalance test effectively forces the defective chain to exhibit stuck-at behaviour.

Table 3.2 is depicted in the chart below. When the defective chain is not subjected to imbalance testing, we see that the gates after the DUT quickly regenerate the low

amplitude signal, and produce the same output as that of the defect-free gates in a few levels. However, when subjected to ITT, the gates are not capable of regenerating the signal, and the defect is not masked. Thus, we could identify the presence of a defect by using this two-pass imbalance testing technique.

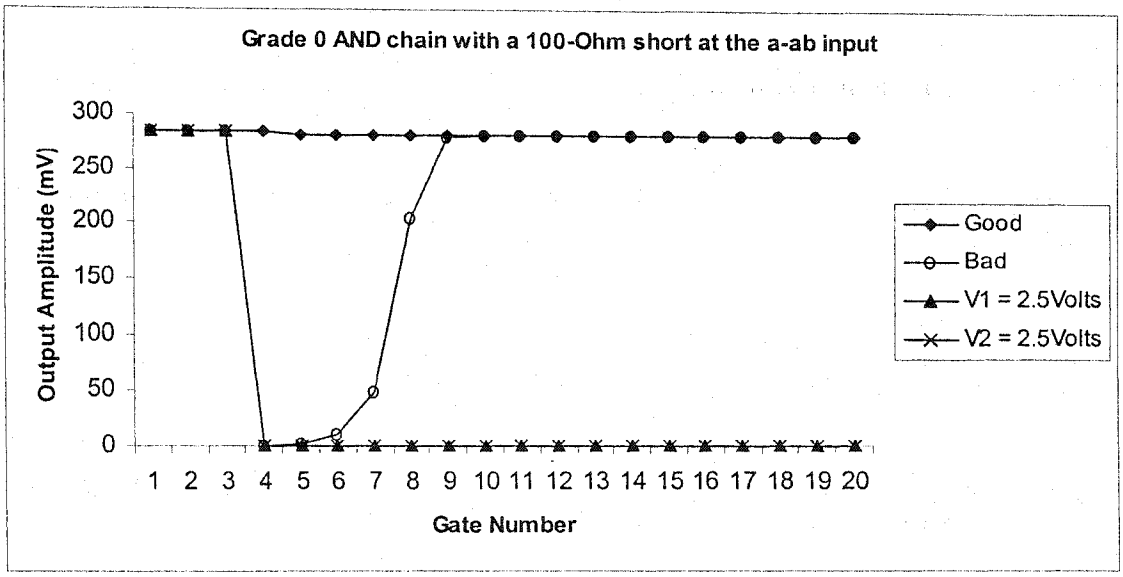



**Figure 3.3 Output of a defective chain with & without ITT**

However, in table 3.3, we see a case where the defective AND chain exhibits stuck-at behaviour even when it is not subjected to any testing. The table holds the same syntax as the previous one. In the third column, the table lists the output of a defective chain not subjected to any testing technique. The fourth and the fifth columns give the output when the chain is subjected to ITT. From tables 3.2 and 3.3, when a defect is present at the b-bb input of the AND gate, the lower differential pair in figure 3.1, it is propagated to the last gate of the chain. It is suspected that the asymmetry of the AND gate plays an important role in fault propagation and fault masking.

The input amplitude to the DUT in table 3.2 is 0.39 mV, while it is 0.388 mV in table 3.3. From tables 3.2 and 3.3, we see that the gate is sensitive to even a small variation in the input signal. Also, as with BAS testing, the AND gate is sensitive to the presence of the defect in either the upper or lower differential pairs. As seen from the table below, the defect present at the b-bb input propagates to the last gate of the chain in the absence of a testing technique itself. Hence, under the set constraints, such a defect can be detected in the functional mode itself.

**Table 3.3 Grade 0 AND chain with a 100 ohm short at b-bb, $R_2$ = 1.5 K**

| Gate No | Good | Bad | V1 = 2.5V (Bad + ITT) | V2 = 2.5V (Bad + ITT) |
|---|---|---|---|---|
| I/p | 250 | 250 | 250 | 250 |
| 1 | 285.15 | 284.16 | 284.16 | 284.16 |
| 4 | 284.2 | 284.2 | 284.2 | 284.2 |
| 5 | 286.6 | 0.388 | 0.385 | 0.389 |
| 6 | 247.5 | s - @ - f | s - @ - f | s - @ - f |
| 20 | 247.5 | s - @ - f | s - @ - f | s - @ - f |

When all the gates in a chain are imbalanced, they exhibit a reduced gain compared with normal gates, in which case they are less capable of restoring small signals on their inputs. When the output of one gate is input to the other, imbalanced gates are also subject to a phenomenon we call 'stress accumulation', which further degrades the signal as it propagates through a gate chain. The signal is progressively degraded, which may, as shown in table 3.4, cause a good chain to exhibit stuck-at behaviour.

**Table 3.4 Defect free grade 5 AND chain. $V_1 = 1.5V$, $R_2 = 3.94K$, one diode**

| Gate No. | Output (mV) | Gate No. | Output (mV) |
|---|---|---|---|
| Input | 250 | 7 | 88.55 |
| 1 | 236.5 | 8 | 78.94 |
| 2 | 236.5 | 9 | 69.84 |
| 3 | 236.6 | 10 | 58.67 |
| 4 | 236.51 | 11 | 41 |
| 5 | 239.4 | 12 | 0.0035 |
| 6 | 103.1 | 13 | s-@-f |

Table 3.4 has the same syntax as the previous tables, but the layout is different. Columns 3 and 4 are the continuations of columns 1 and 2 respectively. A few buffers are used in the chain to stabilise the input signal. The signal falls sharply when it passes the AND gate subjected to ITT. In table 3.4, the amplitude of the signal is progressively degraded by the successive gates of the chain, resulting in stuck-at behaviour in defect-free AND chain. This is also illustrated in the following figure.

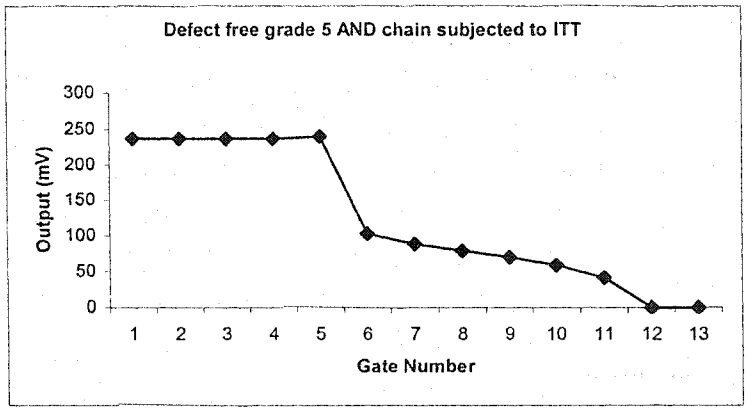



**Figure 3.4 Defect-free grade 5 AND chain outputs s-@-f when subjected to ITT**

From the above table and the figure, we see that the defect-free AND chain exhibits stuck-at behaviour when subjected to the imbalance technique. The AND chain is not able to withstand the applied imbalance. To summarise, stress accumulation leads to a progressive reduction of the propagated amplitude, which may result in stuck-at behaviour of defect-free gate chains.

The impact of this phenomenon on various gates (BUFFER, AND, and XOR) of the Nortel NT25$^{TM}$ Bipolar CML technology was carefully studied. Stress accumulation was observed in AND gates. Within the context of this study, the imposed restrictions and the methodology adopted, defect-free XOR and BUFFER cells did not adopt a stuck-at behaviour when subject to ITT. Note that since CML gates produce differential output signals from differential input signals, studying the AND covers the NAND, the OR and the NOR functions that can be derived by appropriate signal renaming. So far, we considered three cases: (a) a defect is identified by ITT (b) a defect is not masked even when the chain is not subject to ITT, and (c) a defect-free chain outputs a defective behaviour when subject to ITT, due to the accumulation of the applied stress. The following sections report on our study of the stress accumulation phenomenon.

### 3.4 Imbalance Types and Limits

So far, we discussed the results of double imbalance. The inputs and the output of a two-input gate can be imbalanced independently or together, leading to a number of

imbalance patterns. Three significant types of imbalance are possible for a two input gate. They are,

- **Single imbalance:** Only the output line of the gate is imbalanced.
- **Double imbalance:** One of the input lines and the output line are imbalanced.
- **Triple imbalance:** Both input lines and the output line are imbalanced.

In single imbalance, only one of the three lines (two input and one output line) is imbalanced. Single imbalance is possible when one gate is studied in isolation. In a chain of gates, when the outputs of all gates are imbalanced, we obtain double imbalance. Even though single and double imbalance on inputs only is possible, we will restrict our attention on cases where the output is in the set of imbalanced nodes. Indeed, input imbalance is a second order phenomenon compared to output imbalance. Thus, double imbalance will involve one of the input lines as well as the output line. In triple imbalance, both input lines and the output line are imbalanced. In an actual circuit where we wish ITT to be a two-phase test, all nodes are imbalanced in each test phase and triple imbalance is generalised. Triple imbalance occurs in a normal circuit when ITT is applied as a two-phase test (all gate outputs are imbalanced with one of the possible polarities in each test phase). Single and double imbalances are useful for modelling.

The degree of imbalance that a gate can withstand is an important design parameter. Indeed, the degree of imbalance affects the gain of each gate, but it also determines the fault coverage. The degree of imbalance that a gate can withstand can be determined by

studying the chain's behaviour for different imbalance levels. Varying the resistance $R_2$, the voltage $V_1$, and the number of diodes in the imbalance arm varies the imbalance voltage. For logic high, the voltage equation is given by,

$$V_{cc} - I_1 R_1 - n \cdot V_{be} - I_1 R_2 - V_1 = 0 \qquad \text{Eq 3.1}$$

where, $I_1R_1$ is the imbalance voltage ($V_{imb}$). For a given $V_1$, the imbalance current can be changed by changing the number of diodes and/or the value of $R_2$.

$$V_{imb} = I_1 R_1 \qquad \text{Eq 3.2}$$

$$I_1 = \frac{V_{imb}}{R_1} \qquad \text{Eq 3.3}$$

Thus, $V_{imb}$ determines the value of $I_1$, since $R_1$ is fixed for a given speed grade. The following tables list the resistor values ($R_2$) for all the speed grades, for a specified number of diodes in the imbalance arm, below which a defect-free chain exhibits stuck-at behaviour. This is given as a function of the depth of the chain. The title of each table specifies the number of diodes used in the imbalance arm and the number of gates in the chain. The 'a-ab' in the table's headers indicates that the toggling inputs are connected to these lines, while the other inputs receive a full amplitude non-controlling DC value. Likewise, the 'b-bb' in the title indicates the chain is assembled through the 'b-bb' inputs while the 'a-ab' is connected to a full amplitude non-controlling DC signal. In this experiment, $V_1$ was set to 1.5 Volts, and the imbalance voltage was 125 mV. It is

remarkable that the limit value of the resistor $R_2$ is higher with longer chains, an indication of stress accumulation.

**Table 3.5 Smallest resistance (in KOhms) that causes stuck-at behaviour in a fault free 10-gate deep chain, when one diode is used in the test circuitry.**

| Grade | AND a - ab (KOhms) | AND b - bb (KOhms) |
|---|---|---|
| 0 | 170 | 170 |
| 1 | 56.5 | 56 |
| 2 | 17.3 | 17.1 |
| 3 | 10.3 | 10.2 |
| 4 | 5.8 | 5.8 |
| 5 | 3 | 3.1 |
| 6 | 1.8 | 1.8 |

**Table 3.6 Smallest resistance (in KOhms) that causes stuck-at behaviour in a fault free 20-gate deep chain, when one diode is used in the test circuitry.**

| Grade | AND a - ab (KOhms) | AND b - bb (KOhms) |
|---|---|---|
| 0 | 175 | 175 |
| 1 | 58 | 57.5 |
| 2 | 18 | 17.5 |
| 3 | 10.6 | 10.6 |
| 4 | 6.1 | 6.1 |
| 5 | 3.2 | 3.2 |
| 6 | 1.9 | 1.9 |

**Table 3.7 Smallest resistance that causes stuck-at behaviour in a fault free 10-gate deep chain when two diodes are used in the test circuitry.**

| Grade | AND a - ab | AND b - bb |
|---|---|---|
| 0 | 15 KOhms | 14 KOhms |
| 1 | 600 ohms | 600 ohms |
| 2 | No lower limit | No lower limit |
| 3 | No lower limit | No lower limit |
| 4 | No lower limit | No lower limit |
| 5 | No lower limit | No lower limit |
| 6 | No lower limit | No lower limit |

**Table 3.8 Smallest resistance that causes stuck-at behaviour in a fault free 20-gate deep chain when two diodes are used in the test circuitry.**

| Grade | AND a - ab | AND b - bb |
|---|---|---|
| 0 | 15.5 KOhms | 15 KOhms |
| 1 | 1.1 KOhms | 1 KOhms |
| 2 | No lower limit | No lower limit |
| 3 | No lower limit | No lower limit |
| 4 | No lower limit | No lower limit |
| 5 | No lower limit | No lower limit |
| 6 | No lower limit | No lower limit |

The AND gate always had a lower limit on $R_2$ when one diode was used for all speed grades, as compared to the limit on $R_2$ only in grades 0 and 1 - when two diodes were used. When two diodes were used for AND gates of speed grades 2 to 6, stuck-at behaviour cannot be induced because the diodes are too resistive. The extra diode inserts an extra resistance. The incremental resistance of each diode is in the order of 224

Kohms to 1.8 Kohms, from grade 0 to grade 6. The diodes in NT25$^{TM}$ technology are turned on for a $V_{be}$ of 900 mV. For lower diode voltages, the current through the diode is too low. The imbalance level required for stuck-at behaviour to occur in defect-free AND chain cannot be attained when two diodes are used in the test circuitry, due to the dynamic resistance of the diodes. When two diodes were used to test BUFFER and XOR gates, they did not have any lower limit on the value of the resistor connected to the imbalance arm within the set constraints and methods. This is because these gates are symmetrical and are more robust than the AND gate, which is asymmetrical.

Testing is done to identify defective parts from defect-free ones. The test constraints set should be such that, they aid in effectively differentiating the defective parts from the manufactured lot. It is important to not declare a defect-free gate defective, as the yield will go low. Therefore, it is important to study why defect-free AND gates exhibit stuck-at behaviour when subjected to imbalance testing. From the above tables, we now know that the AND gate can withstand only a certain imbalance level. In the following sections, based on the asymmetry of the bipolar CML AND gates, we discuss why they accumulate imbalance.

### 3.5 Analysis of stuck at behaviour observed in defect-free AND gates

From the transistor level schematic of BUFFER (figure 1.1, inverter) and XOR gates (see figure 2.3 in chapter 2), we see that the gates are perfectly symmetrical i.e., the same number of transistors conduct when either input is high. However, in the case of an AND

gate (see figure 3.1), the output changes based on whether the transistor Q5 is on or transistor Q6 is on. While the transistor Q6 drives a differential stage, transistor Q5 drives none. Also, collectors of two transistors are connected to the 'op' output, while just one collector is connected to the 'opb' output of the AND gate. As discussed in the following section, it is suspected that this asymmetrical nature of the AND gates leads to stress accumulation.

In the AND gate chain, when one arm is imbalanced in the test mode, the amplitude is lowered on this side. Therefore, the remaining noise margin is much lower than 250 mV. When this signal is passed on to the next AND gate of the chain, after being level shifted by the transistors Q3 and Q4, they drive the differential amplifier pair Q5 - Q6 with almost the same reduced amplitude. With the voltages being more or less equal in the two transistors, the current flows in both arms. While the branch that should conduct current in the normal mode still conducts current, the opposite branch also conducts a current of lower amplitude. Thus, there is a leakage of current in the differential pair resulting in lower output amplitude. This signal is further reduced by the applied imbalance and passed on to the successive AND gate of the chain. Successive reduction in the output amplitude leads to stuck-at behaviour in defect-free imbalanced AND gates. It is suspected this phenomenon is observed in AND gates due to their asymmetric nature, and does not occur in XOR gate, as it is symmetrical by design. Higher imbalance levels induce current leakage and thus perturb the functioning of the gate.

However, we were not able to analytically attribute the current leakage to the asymmetry of the AND gates, as the current leaks in the XOR gates as well.

Since the waveforms of the signals 'op' and 'opb' follow that of 'a' and 'ab' respectively, the relative pull down of 'opb' with respect to 'op' is carried out in all the AND gates of the chain. The output signal 'opb' is further drifted away from the output signal 'op' in each of the gates in the chain. The amount of drift in each gate is not the same because of the varying gains in each gate of the chain. Thus, the drift in one gate is carried on to the other accumulating the shift in level. Slowly the differential amplitude decreases and the signals do not cross each other any more, leading to stuck-at fault.

### 3.6 Characterisation of ITT on one gate

We know that accumulation occurs in defect-free gates, leading to stuck-at behaviour. Since we do not want to declare a good gate defective, we are interested in studying the behaviour of imbalanced defect-free gates. In order to help understand and characterise the phenomenon of stress accumulation, a single gate was studied in detail, rather than a chain of gates [30]. Indeed, a more complete knowledge of how a single gate behaves helps understand what happens to a chain of gates or a network.

In an actual circuit, if we are successful in limiting ITT to two test modes as desired, all inputs and the outputs are imbalanced. Note that each line can be imbalanced on the true side or on the complement side. If we include cases where one or more line is not

imbalanced for reference purposes, it yields $3^3$ possibilities. It was also observed that the impact of imbalance depends on how it combines with imposed logic signals. A complete characterisation of a gate must consider $3^3 * 2^2 = 108$ cases of interest.

The process of simulating all these combinations for different imbalance levels was automated by developing a tool called "imbalance analyser". Ginette Monté developed this tool. The necessity of this tool is compounded by the need to analyse 7 speed grades for various imbalance strengths. Note that accumulation is a non-linear phenomenon, and before developing the tool, it was not clear which combination produced the worst accumulation. Figure 3.5 illustrates the test bench setup. The inputs of the DUT, an AND gate, can receive a regular or an imbalanced signal, and its outputs can also be regular or imbalanced.

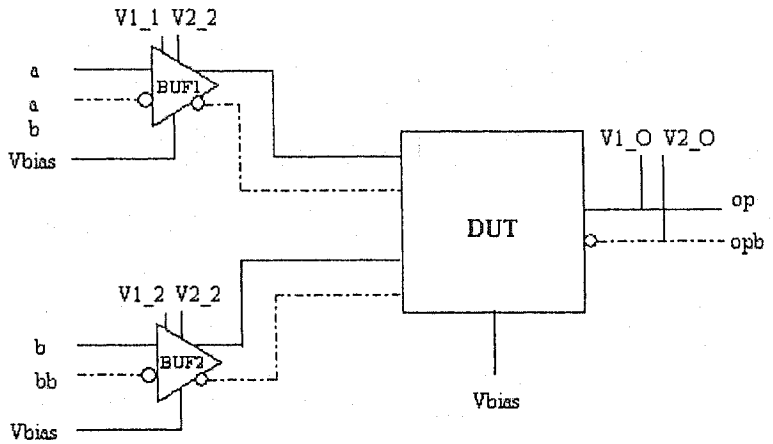



**Figure 3.5 Setup employed to characterise the ITT on one gate**

The "Imbalance analyser" tool exhaustively analyses all possible ways in which a gate can be imbalanced, to study the imbalance patterns that lead to accumulation. The tool ranks the K patterns that give rise to largest and smallest accumulation. Based on these

ranks, we can determine which patterns must be considered in the determination of a safe imbalance limit. A sample of the results obtained for a CML grade 5 AND gate for 125mV nominal imposed imbalance is listed below [30]. A complete table is presented in Appendix III.

**Figure 3.6 Imbalance Analyser simulation results**

```
What simulator would you prefer (Spectre=1, Spice=0)?
File name listing cells to analyse:
List of stimuli file name:
Test bench file name: Beginning of simulation -- gold
CELL: andITT_grad5
RESULTS
Presentation order: Stress-vectors, logical levels, op, opb, abs(NM), NM, diff, NM1, rank
stress_vectors: v1w1 v2w1 v1w2 v2w2 v1wo v2wo
logical levels: vin1 vin2
Definition of the different variables:
Stress vectors
      v1w?: is the stress input on the left side of the gate
      v2w?: is the stress input on the right side of the gate
      v?w1: is the buffer connected to the A line of the following DUT
      v?w2: is the buffer connected to the B line(level shifted) of the following DUT
      v?wo: is the DUT output, ie gate studied
So v2w2 is the stress input on the op line of the buffer connected to the B line of the DUT
Definition of the logical levels:
      vin1: nominal value on the true line of the buffer connected to the A line of DUT
      vin2: nominal value on the true line of the buffer connected to the B line of DUT
Definition of the ouput values:
      op: voltage on the op line of DUT
      opb: voltage on the opb line of DUT
      abs(NM): absolute NM
      NM: op - opb
      diff: remaining NM
      NM1: Noise margin at the following buffer after DUT
      rank1: rank of the value of abs(NM) (beginning with the lowest value)
      rank2: rank of the value of abs(NM) (beginning with the highest value)
Calculated stress:
Nominal value of voltage applied at the stressing inputs: 1.5V
nb combinations: 108
Cell GRADE      #of diodes      Resistor Value (KOhms)
```

| | | |
|---|---|---|
| G 0 | 2 | 49.83 |
| G 1 | 2 | 11.5 |
| G 2 | 1 | 28.13 |
| G 3 | 1 | 17.04 |
| G 4 | 1 | 6.61 |
| G 5 | 1 | 3.23 |
| G 6 | 1 | 1.58 |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 0 0 0 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000000 | -0.254137 | | |
| 2 | 0 0 0 0 0 0 | 3.05 | 3.30 | 3.046746 | 3.296750 | 0.250005 | -0.250005 | 0.003362 | -0.254129 | | |
| 3 | 0 0 0 0 0 0 | 3.30 | 3.05 | 3.043437 | 3.296753 | 0.253315 | -0.253315 | 0.000051 | -0.254137 | | |
| 4 | 0 0 0 0 0 0 | 3.30 | 3.30 | 3.296723 | 3.046773 | 0.249951 | 0.249951 | 0.003416 | 0.254128 | | |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 21 | 0 0 0 1 1 0 | 3.05 | 3.05 | 2.934553 | 3.296778 | 0.362225 | -0.362225 | -0.108858 | -0.254194 | | 2 |
| 22 | 0 0 0 1 1 0 | 3.05 | 3.30 | 2.937382 | 3.296751 | 0.359369 | -0.359369 | -0.106003 | -0.254194 | | |
| 23 | 0 0 0 1 1 0 | 3.30 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 8 |
| 24 | 0 0 0 1 1 0 | 3.30 | 3.30 | 3.142671 | 3.053743 | 0.088928 | 0.088928 | 0.164438 | 0.226882 | 6 | |
| 45 | 0 1 0 0 1 0 | 3.05 | 3.05 | 2.934554 | 3.296778 | 0.362224 | -0.362224 | -0.108858 | -0.254194 | | 7 |
| 46 | 0 1 0 0 1 0 | 3.05 | 3.30 | 2.937350 | 3.296777 | 0.359428 | -0.359428 | -0.106061 | -0.254194 | | 16 |
| 47 | 0 1 0 0 1 0 | 3.30 | 3.05 | 2.934575 | 3.296753 | 0.362178 | -0.362178 | -0.108812 | -0.254194 | | 10 |
| 48 | 0 1 0 0 1 0 | 3.30 | 3.30 | 3.142504 | 3.053923 | 0.088582 | 0.088582 | 0.164785 | 0.226559 | 2 | |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 57 | 0 1 0 1 1 0 | 3.05 | 3.05 | 2.934553 | 3.296778 | 0.362225 | -0.362225 | -0.108858 | -0.254194 | | 1 |
| 58 | 0 1 0 1 1 0 | 3.05 | 3.30 | 2.937359 | 3.296777 | 0.359418 | -0.359418 | -0.106052 | -0.254194 | | 19 |
| 59 | 0 1 0 1 1 0 | 3.30 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 6 |
| 60 | 0 1 0 1 1 0 | 3.30 | 3.30 | 3.136815 | 3.060681 | 0.076133 | 0.076133 | 0.177233 | 0.212452 | 1 | |
| 72 | 0 1 1 0 1 0 | 3.30 | 3.30 | 3.142525 | 3.053899 | 0.088627 | 0.088627 | 0.164740 | 0.226601 | 4 | |
| 78 | 1 0 0 0 0 1 | 3.05 | 3.30 | 3.053896 | 3.142527 | 0.088630 | -0.088630 | 0.164736 | -0.226604 | 5 | |
| 79 | 1 0 0 0 0 1 | 3.30 | 3.05 | 3.043348 | 3.148641 | 0.105293 | -0.105293 | 0.148073 | -0.238749 | | |
| 80 | 1 0 0 0 0 1 | 3.30 | 3.30 | 3.296751 | 2.937373 | 0.359378 | 0.359378 | -0.106011 | 0.254194 | | 20 |
| 81 | 1 0 0 0 1 0 | 3.05 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 5 |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 93 | 1 0 0 1 1 0 | 3.05 | 3.05 | 2.934553 | 3.296778 | 0.362224 | -0.362224 | -0.108858 | -0.254194 | | 4 |
| 94 | 1 0 0 1 1 0 | 3.05 | 3.30 | 2.943347 | 3.289687 | 0.346340 | -0.346340 | -0.092973 | -0.254188 | | |
| 95 | 1 0 0 1 1 0 | 3.30 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 3 |
| 96 | 1 0 0 1 1 0 | 3.30 | 3.30 | 3.142693 | 3.053717 | 0.088976 | 0.088976 | 0.164390 | 0.226927 | 7 | |
| 101 | 1 0 1 0 0 1 | 3.05 | 3.05 | 3.043622 | 3.148571 | 0.104949 | -0.104949 | 0.148417 | -0.238558 | | |
| 102 | 1 0 1 0 0 1 | 3.05 | 3.30 | 3.053898 | 3.142525 | 0.088627 | -0.088627 | 0.164739 | -0.226601 | 3 | |
| 103 | 1 0 1 0 0 1 | 3.30 | 3.05 | 3.050219 | 3.143008 | 0.092789 | -0.092789 | 0.160577 | -0.230262 | 9 | |
| 104 | 1 0 1 0 0 1 | 3.30 | 3.30 | 3.296777 | 2.937351 | 0.359426 | 0.359426 | -0.106060 | 0.254194 | | 18 |

The tool allows the user to choose between *spectre* and *spice* simulators. Since the effect of imbalance accumulation on a fault free gate is of interest, the tool simulates a gold (fault free) gate. In the above figure, the type and the grade of the gate are given under the heading CELL. The table lists the following: The line number, the stimulus vectors, the logical values at the inputs, the output of the gate and its complement, the absolute value of the noise margin (NM) and the NM itself; the remaining NM (diff) that is the difference between the normal noise margin and the present value; the amplitude signal of the buffer present at the output of the DUT (NM1); then the ranks in ascending and descending orders of the absolute noise margin. The 6 columns under the label 'stimulus-vectors' are loaded with 1s and 0s: a 1 means that the corresponding line is imbalanced (with the values described in the first part of the listing, 125 mV in this case.) and 0 means that line is not imbalanced. The orders of the 6 columns, referring to the labels shown in figure 3.6 are V1_1, V2_1 (first buffer, BUF1); V1_2, V2_2 (BUF2); V1_O, V2_O (DUT). Vin1 and Vin2 are the voltages applied to the true input lines of the two buffers driving the DUT. NM1, the differential output voltage of the buffer following the DUT (not shown in figure 3.5) gives an idea of how the signals are regenerated in just one stage. The last two columns rank the absolute noise margin. From the lowest to the $Kth_{highest}$ value (where K is a parameter given when running the 'imbalance analyser') and from the highest to the $Kth_{lowest}$ value.

Table 3.9 ranks the lowest eight NMs for a 125 mV imbalance level of the CML AND gate for all grades. The first row gives the rank number and the first column gives the

speed grade of the gate. The cells of the table give the line number of the stimulus that lead to the corresponding rank in ascending order of NM. Note the mapping of ranks to stimulus pattern is uniform throughout the experiment.

**Table 3.9 Eight imbalance patterns resulting in very low output noise margins**

| Grade | Rank 1 | Rank 2 | Rank 3 | Rank 4 | Rank 5 | Rank 6 | Rank 7 | Rank 8 |
|---|---|---|---|---|---|---|---|---|
| 0 | 60 | 90 | 24 | 48 | 72 | 96 | 78 | 102 |
| 1 | 60 | 90 | 24 | 96 | 48 | 72 | 78 | 102 |
| 2 | 60 | 90 | 24 | 96 | 48 | 102 | 72 | 78 |
| 3 | 60 | 90 | 24 | 96 | 48 | 78 | 102 | 72 |
| 4 | 60 | 48 | 72 | 78 | 90 | 102 | 24 | 96 |
| 5 | 60 | 48 | 72 | 102 | 78 | 90 | 24 | 96 |
| 6 | 60 | 48 | 72 | 102 | 78 | 24 | 96 | 90 |

The lowest resulting amplitude was always obtained with the same stimulus pattern, irrespective of the grade of the gate, and the applied stress. This corresponds to pattern #60, which is 010110, where all three lines are imbalanced with a polarity that influences the branch that drives the 'op' line. The logical levels at the input of the DUT are 1 1. When the logical levels at the input are 1 1 ('a' and 'b' are high), Q2 and Q6 conduct (see figure 3.1), making 'opb' low and 'op' high. But the transistors, Q1 and Q5 receive imbalanced inputs, and $V_1$ is imbalanced in the pattern '010110', lowering the amplitude of the 'high' signal. Thus, the differential output is low in this case.

On the other hand, certain imbalance patterns can be used to reinforce a signal as well. For example, consider the case where the logical levels at the inputs are 1 1 again. If the imbalance pattern is such that 'a', 'b' and 'opb' are imbalanced, then 'opb' is further lowered while 'op' is high, lowering the amplitude of the 'low' signal. Thus the noise margin increases, reinforcing the signal.

It is also important to note that the same set of eight patterns always produce the top eight ranks, not necessarily in the same order always. While some combinations lead to very low output noise margins, some do not. For instance, the output noise margin with pattern 60 is 76 mV, and with pattern 57 is 362 mV, while the expected noise margin is 125mV. Now, having given a clear idea of accumulation, why it occurs, and how sensitive it is to the imbalance patterns, let us study the means to overcome accumulation.

### 3.7 Overcoming stress accumulation

Several methods to overcome accumulation were studied in detail. Only those found fruitful are described here. We briefly introduce here the methods that have some potential, and develop the most effective ones in the following sections. The most effective ones are marked with a star in the beginning.

1. Choosing the imbalance patterns that do not lead to the lowest output amplitudes avoids worst-case accumulation. If care is taken to avoid the patterns that lead to the lowest resulting output amplitudes throughout the circuit, then accumulation

can be overcome. The "imbalance analyser" tool ranks these patterns. See Appendix IV.

2. *Inserting one balanced gate (a normal gate) once in every few gates in a chain restores or regenerates weak signals. The gain of this gate is not reduced, and hence can amplify the small input signal.

3. *Inserting one buffer once in every few gates regenerates the signal. Since the buffers do not suffer from accumulation effects, this method overcomes accumulation. This is a potential method and has been left for future work. Therefore, this method is not discussed here.

4. *Increasing the remaining noise margin (or, in other words, reducing the degree of imbalance) helps overcome accumulation. If the imbalance is sufficiently small, good gates do not exhibit stuck-at behaviour. At low imbalance, good gates have a gain large enough to prevent accumulation. Also, if the minimum input signal required for a gate to operate is known, then stress accumulation can be overcome by keeping the input signal to all gates above this value. The input signals can be kept above this value by choosing the right amount of imbalance.

5. *Another alternative would be to imbalance the two arms to two different levels. The worst case is when b - bb has a defect and when $V_1$ is imbalanced. Reducing

the imbalance in this arm, and applying a significantly larger imbalance on the other improves coverage, at least for a fraction of the defects.

Having outlined the methods studied and/or proposed so far, let us explore the potential of the most promising methods in detail in the following sections.

### 3.7.1 Signal regeneration

Accumulation can be overcome by not stressing one AND gate once in every few gates of the chain. In other words, inserting one balanced (normal) gate in every few gates of the chain regenerates the signal to the value it had a few stages before, effectively increasing the depth of the chain. This is possible because the gate is balanced; its gain is not altered. Hence, it has the strength to restore small signals on its input. The balanced gate used here is an AND gate. However, it is conjectured that a balanced buffer too can perform the task.

The test bench setup is the same as before, except that one gate in every 'n' number of gates is normal. Let us study using the normal AND gate for signal restoration. The normal gate amplifies the signal on its input to the value observed a few gates before, say 'n1', in the chain - and inputs this signal to the next gate in the chain. Thus, with respect to the attainable depth, a gain of 'n1' gates is obtained. This prevents the good chain from exhibiting stuck-at behaviour, while the defective one still does. In some cases, this method delays the stuck-at behaviour in these gates, thereby increasing the feasible depth of the chain. This method can be used to overcome stress accumulation.

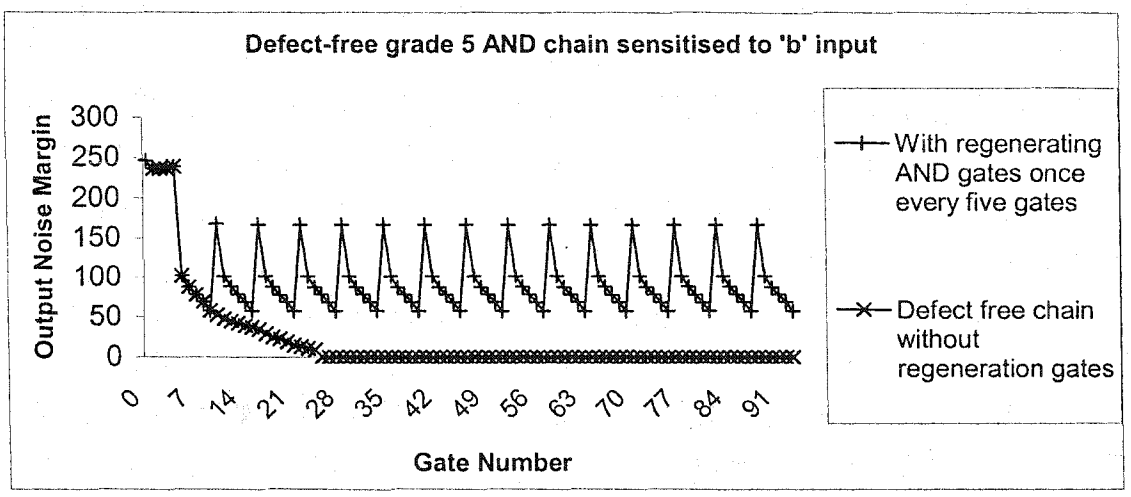



**Figure 3.7 Signal regeneration: Output amplitude with & without regenerating gates**

Figure 3.7 illustrates the case of a 100 gate deep grade 5 AND chain, with and without normal gates. When no special gates are employed to regenerate the output amplitude, a defect-free chain of AND gates containing only imbalanced gates exhibit a stuck-at behaviour at a depth of 27 gates.

The figure also illustrates the same chain where one un-imbalanced (normal) AND gate is placed once in every five gates of a 100 gate deep chain. A 3K resistor is connected to the imbalance test circuit and the toggling signal is connected to the b-bb line of the AND gate. The first five gates of the chain are buffers, used to stabilise the input signal. Gate #6 is the 1st AND gate in the chain. While each imbalanced AND gate degrades the signal, the normal AND gate amplifies it. This is seen in the figure by a steep rise in the output noise margin.

From the figure, the input to the normal gate is around 57.7mV and the output is around 167mV. This can be observed for all the normal gates. This shows that the behaviour of such a set up is cyclic i.e., the input to all the normal gates in the chain is approximately 58mV and the output is always 167mV approximately. Inserting one balanced gate once in every five gates of the chain, in this case, leads to a gain of five gates i.e., in each cases, the signal has been restored to its value before five gates in the chain. Each normal gate increases the attainable depth by 5 more imbalanced AND gates, in this case. This method can be used to overcome stress accumulation.

### 3.7.2 Low imbalance levels

Imbalance level plays an important role in stress accumulation. When high levels of imbalance are applied, the gains are sharply reduced, which gradually degrades the signal leading to stuck-at behaviour in the chain. If the imbalance level is decreased, then the good chain does not exhibit stuck-at behaviour, as the gate is capable of regenerating the signal amplitude. This is discussed in the following sections.

Table 3.10 illustrates the effect of remaining noise margin on the circuit studied in figure 3.7. The first column gives the gate number in the chain and the second column gives the output amplitude in mV. While all others remain the same as in the previous set up, the resistance connected to the imbalance arm was changed to 2.5K to obtain a remaining noise margin of approximately 80mV (81.7). The circuit is found to exhibit stuck-at behaviour even before the signal was input to the balanced gate (gate #9, marked

with a star *) - which may have restored the signal amplitude; but the signal collapsed before reaching that gate.

**Table 3.10 One normal AND gate once in every five imbalanced AND gates, $V_1$=1.5 V, $R_2$=2.5 K**

| Gate No. | Output amplitude (mV) | Gate No. | Output amplitude (mV) |
|---|---|---|---|
| 0 | 236.63 | 5 | 81.7 |
| 1 | 236.5 | 6 | 51.7 |
| 2 | 236.5 | 7 | 0.007 |
| 3 | 236.5 | 8 | s-@-f |
| 4 | 239.42 | 9* | s-@-f |

To further illustrate the effect of imbalance level, consider the following figure. The remaining noise margin is 130 mV. One balanced AND gate is placed once in every 10 imbalanced AND gates of the 100 gate deep chain, only 25 gates are shown in the figure here. The circuit outputs approximately 123 mV throughout. Periodic behaviour can be observed in the figure.

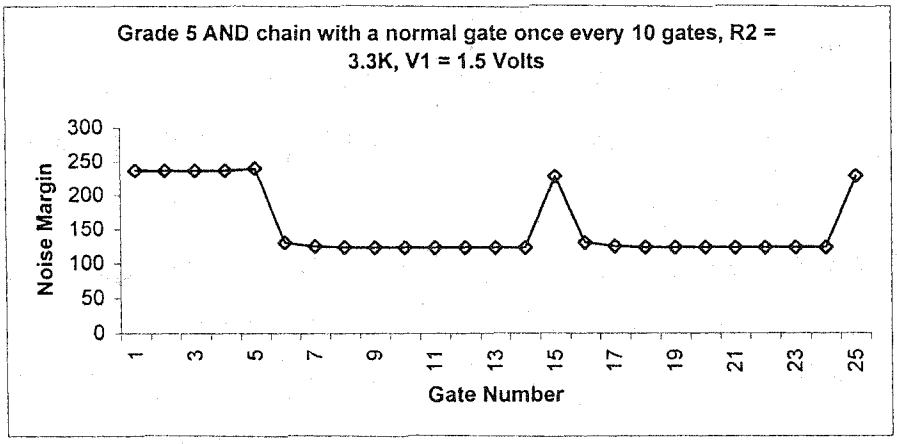



**Figure 3.8 Periodic behaviour of the AND chain during signal restoration**

We see that the output noise margin remains fairly uniform throughout, despite placing one balanced gate every 10 gates - for an imbalance level of 120 mV (remaining noise margin is 130 mV). Simulations were carried out with no normal gate in the chain, i.e., all the gates in the chain were imbalanced. Figure 3.9 shows that stress accumulation saturates to insignificant levels when the remaining noise margin is sufficiently high - or when the imbalance level is low. Thus, the imbalance applied to the gate plays an important and non-linear role in stress accumulation. This finding can also be leveraged to control stress accumulation.

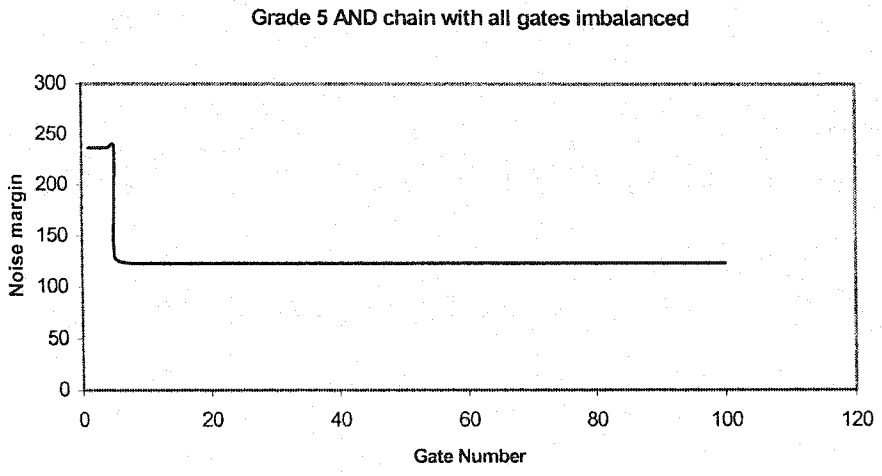



**Figure 3.9 Steady output of defect-free AND chain for low imbalance voltages**

The effect of applied imbalance was studied for different imbalance levels. It was found that when the remaining noise margin was greater than 125 mV, signal restoration was not required, as the studied gate did not suffer from stress accumulation. Thus, when the imbalance level is above a particular value, stress accumulation can be prevented.

However, the exact imbalance for safe operation cannot be generalised as it varies according to the speed grade of the gate, the type of the gate itself, the technology used, etc.

### 3.7.3 Different imbalance levels

So far, we have considered the cases where the nodes $V_1$ and $V_2$ were connected to the same voltage levels. But, we know the AND gate is asymmetric, and we suspect that this leads to imbalance accumulation in these gates. Therefore, it is conjectured that the voltages $V_1$ and $V_2$ need not necessarily be the same. From table 3.9, worst stress accumulation occurs when 'a' and 'b' of the AND gate are high, and $V_1$ is imbalanced. The imbalance level on this arm can be decreased to a safe value where a good gate does not exhibit stuck-at behaviour and the imbalance level in the other arm can be increased, thus increasing fault coverage on this side.

## 3.8 Conclusions

In this chapter, we studied the imbalance testing technique as applied to bipolar CML family. We studied three type of imbalance techniques namely, single, double and triple imbalance, reported by the 'imbalance analyser' tool. While this technique is quite effective in degrading any marginal signals, it also leads to imbalance accumulation in defect-free AND gates if the imbalance level is not carefully chosen. We also discussed the importance of choosing the right design parameters for both the functional mode and the test mode: we do not want to disturb the functional parameter $R_1$. Therefore, we

change the test parameters like $V_1$, $R_2$ and 'n' to suit our requirements. We studied ITT as applied to one gate in order to better understand the phenomenon of stress accumulation. From the above discussions, it is clear that stress accumulation occurs due to excessive imbalance of the asymmetric AND gate. In order to overcome this effect, the imbalance level should be reduced. Other techniques like adding one normal gate once in every few gates, adding a buffer once in every few gates, etc., are also useful in overcoming stress accumulation. Using two different imbalance levels for the two test branches may increase the defect coverage and overcome stress accumulation. This method is yet to be studied, and is left as a future work.

# CHAPTER 4

# SENSITIVITY ANALYSIS

## 4.1 Introduction

One of the potential techniques proposed for testing bipolar CML family is the "Imbalance Testing Technique", discussed in the previous chapter. In this technique, a test circuitry is added to each of the output lines of the gate, to imbalance the gate. The applied imbalance degrades any marginal signals, causing the defective gate to exhibit stuck-at behaviour. This imbalance test circuitry consists of a resistor and a transistor-diode connected to external voltage supplies $V_1$, $V_2$. This chapter analyses the effect of varying several parameters like resistance, temperature, etc., on the testing technique proposed, and hence on the bipolar CML gates.

## 4.2 Overview of the proposed testing technique

The Imbalance Testing Technique (ITT) imbalances each gate just enough so that any marginal signals are sufficiently degraded to cause logic errors. The circuit is shown in figure 4.1. When subjected to this technique, a good circuit outputs low amplitude, and defective circuit exhibits stuck-at behaviour. It is suspected that the asymmetry of bipolar CML AND gates influences the threshold imbalance level, where good gates subjected to ITT exhibit stuck-at behaviour. Successive gates in the chain accumulate the applied imbalance, resulting in stuck-at behaviour of defect-free gates. Research showed that inserting two diodes in the imbalance arm could reduce the impact of imbalance

accumulation. See tables 3.5 to 3.8 in chapter 3. It is important to study the consequences of using a given number of diodes in the test circuitry. We also wish to study how the variations in $V_{be}$ affect the output voltage and the imbalance voltage. The sensitivity of $V_{out}$ with respect to $V_{be}$, $R_1$ and $R_2$ is studied in detail in this chapter.

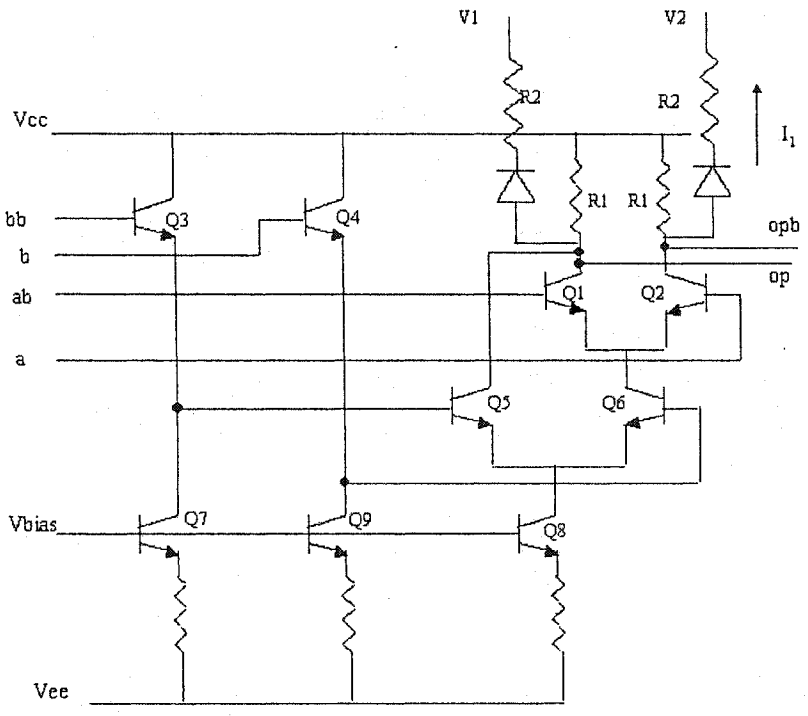



**Figure 4.1 ITT as applied to a bipolar CML AND gate**

## 4.3 Deriving the sensitivity of $V_{out}$ to various parameters

### 4.3.1 Sensitivity of the output voltage to $V_{be}$ variations

In this section, we discuss how the change in the diode voltage affects the output voltage. A voltage equation from $V_{cc}$ to $V_1$ gives,

$$V_{cc} - I_1 R_1 - (n.V_{be}) - I_1 R_2 - V_1 = 0 \qquad \text{Eq 4.1}$$

where, 'n' is the number of diodes.

From Eq 4.1, the equation for the current $I_1$ can be given by,

$$I_1 = \frac{V_{cc} - (n \cdot V_{be}) - V_1}{R_1 + R_2} \qquad \text{Eq 4.2}$$

We know that the output voltage is given by,

$$V_{out} = V_{cc} - I_1 R_1 \qquad \text{Eq 4.3}$$

Substituting for $I_1$ (Eq 4.2) in the first voltage equation (Eq 4.3), we get

$$V_{out} = V_{cc} - \left( R_1 \cdot \frac{V_{cc} - (n \cdot V_{be}) - V_1}{R_1 + R_2} \right) \qquad \text{Eq 4.4}$$

Multiplying throughout by $R_1 + R_2$, we get,

$$V_{out}(R_1 + R_2) = V_{cc}(R_1 + R_2) - R_1(V_{cc} - n \cdot V_{be} - V_1) \qquad \text{Eq 4.5}$$

Let us assume that the voltage drop across the diode varies for some reasons. For example, the variations may be due to temperature or process variations. Such variations can be expressed by $\Delta$ as in $V_{be}^{\Delta}$. The effect of this variation on the output voltage $V_{out}$ is denoted by $V_{out}^{\Delta}$, and is given by the following equation:

$$V_{out}(R_1 + R_2) + V_{out}^{\Delta}(R_1 + R_2) = V_{cc}(R_1 + R_2) - R_1(V_{cc} - n \cdot V_{be} - (n \cdot V_{be}^{\Delta}) - V_1) \qquad \text{Eq 4.6}$$

Subtracting Eq 4.5 from Eq 4.6, we get

$$V_{out}^{\Delta} \cdot (R_1 + R_2) = n \cdot R_1 \cdot V_{be}^{\Delta} \quad \text{Eq 4.7}$$

Rearranging Eq 4.7,

$$V_{out}^{\Delta} = n \cdot \frac{R_1}{(R_1 + R_2)} \cdot V_{be}^{\Delta} \quad \text{Eq 4.8}$$

Partially deriving Eq 4.8 with respect to $V_{be}^{\Delta}$,

$$\frac{\partial}{\partial V_{be}^{\Delta}} V_{out}^{\Delta} = n \cdot \frac{R_1}{R_1 + R_2} \quad \text{Eq 4.9}$$

Rewriting the above equation,

$$\partial V_{out}^{\Delta} = n \cdot \frac{R_1}{R_1 + R_2} \partial V_{be}^{\Delta} \quad \text{Eq 4.10}$$

From the above equation, we see that any change in $V_{be}$ linearly affects the output voltage. Further, the number of diodes used in the test circuitry augments the change in diode voltage. Hence, to minimise the effect of variations in $V_{be}$ on the output voltage, it is desirable to have only one diode in the circuit. The increase in $V_{be}$ can be compensated by adjusting the coefficient, $R_1/(R_1 + R_2)$. $R_1$ cannot be modified, as it is a part of the library. However, $R_2$ can be changed in the design stage. Therefore, increasing $R_2$ helps reduce the effect of $V_{be}$ variations. Thus, 'n' should be small and $R_2$ should be high.

### 4.3.2 Sensitivity of the output voltage to $R_1$

In this section, we discuss the effect of change in the resistance $R_1$ on the output voltage. We know that the output is given by,

$$V_{out} = V_{cc} - I_1 R_1 \quad \text{Eq 4.11}$$

The sensitivity of the output voltage to $R_1$ can be obtained by taking partial derivative of Eq 4.11:

$$\frac{\partial V_{out}}{\partial R_1} = -I_1 - \left( R_1 \cdot \frac{\partial I_1}{\partial R_1} \right), \text{ as } V_{cc} \text{ is a constant} \qquad \text{Eq 4.12}$$

From Eq 4.2, we know that $I_1$ is given by,

$$I_1 = \frac{V_{cc} - (n \cdot V_{be}) - V_1}{R_1 + R_2} \qquad \text{Eq 4.13}$$

Substituting the value of $I_1$ in the second part of equation 4.12, and differentiating, we get

$$\frac{\partial V_{out}}{\partial R_1} = -I_1 + R_1 \cdot \frac{V_{cc} - (n \cdot V_{be}) - V_1}{(R_1 + R_2)^2} \qquad \text{Eq 4.14}$$

Grouping out $I_1$ in the above equation, we get

$$\frac{\partial V_{out}}{\partial R_1} = -I_1 + I_1 \cdot \frac{R_1}{R_1 + R_2} \qquad \text{Eq 4.15}$$

Rearranging the above equation,

$$\frac{\partial V_{out}}{\partial R_1} = I_1 \cdot \frac{R_2}{R_1 + R_2} \qquad \text{Eq 4.16}$$

Therefore,

$$\partial V_{out} = I_1 \cdot \frac{R_2}{R_1 + R_2} \cdot \partial R_1 \qquad \text{Eq 4.17}$$

From the above equation (Eq 4.17), in order to minimise the change in the output voltage, $V_{out}$ due to the change in $R_1$, it is desirable to lower the ratio $R_2/(R_1 + R_2)$. This is always smaller than 1. If $R_2$ goes high, then the above ratio increases. Hence, it is desirable to

have a lower value for $R_2$ to reduce the effect of variations in the resistance $R_1$ on the output voltage.

### 4.3.3 Sensitivity of the output voltage to $R_2$

So far, we studied the effect of change in the diode voltage and change in the resistance $R_1$ on the output voltage. Now, let us study the effect of change in the resistance $R_2$ on the output voltage. The output voltage is given by,

$$V_{out} = V_{cc} - I_1 R_1 \qquad \text{Eq 4.18}$$

Substituting for $I_1$ in the above equation,

$$V_{out} = V_{cc} - \left( R_1 \cdot \frac{V_{cc} - (n \cdot V_{be}) - V_1}{R_1 + R_2} \right) \qquad \text{Eq 4.19}$$

Partial derivative of the above equation with respect to $R_2$ gives,

$$\frac{\partial V_{out}}{\partial R_2} = (V_{cc} - (n \cdot V_{be}) - V_1) \cdot \frac{R_1}{(R_1 + R_2)^2} \qquad \text{Eq 4.20}$$

$$\frac{\partial V_{out}}{\partial R_2} = I_1 \cdot \frac{R_1}{R_1 + R_2} \qquad \text{Eq 4.21}$$

Rewriting the above equation, we get

$$\partial V_{out} = I_1 \cdot \frac{R_1}{R_1 + R_2} \cdot \partial R_2 \qquad \text{Eq 4.22}$$

From the above equation, to minimise the effects of variations in $R_2$ on the output voltage, it is desirable to keep $R_2$ as low as possible. At the same time, the ratio $R_1/(R_1+R_2)$ will be low only when $R_2$ is high.

### 4.3.4 Power Consumption

So far, we discussed the effects of variations in the resistances on the output voltage. Now, we discuss the power consumed in the test mode. From figure 4.1, the equation for power is given by,

$$(V_{cc} - V_1)I_1 = I_1^2(R_1 + R_2) + n \cdot V_{be} \cdot I_1 \qquad \text{Eq 4.23}$$

Rearranging,

$$V_{cc}I_1 - I_1^2R_1 - n \cdot V_{be} \cdot I_1 - I_1^2R_2 = V_1I_1 \qquad \text{Eq 4.24}$$

Dividing Eq 4.24 by $I_1$, we get the voltage equation,

$$V_{cc} - I_1R_1 - (V_{be} \cdot n) - I_1R_2 = V_1 \qquad \text{Eq 4.25}$$

In the above equation, $V_{cc}$ and $R_1$ are fixed; $V_1$ is an external parameter that can be controlled; $R_2$ can be selected at the design stage. Thus, the above voltage equation can be written as,

$$V_1 \propto -I_1R_2 \qquad \text{Eq 4.26}$$

From the above equation, for a given imbalance voltage level, lowering $V_1$ results in a high value for $R_2$ - which is desirable in many ways. However, lowering $V_1$ increases the power consumed in the test mode. From Eq 4.24, when $V_1$ is lowered, $I_1$ goes high, increasing the power consumed in the test mode. On the contrary, higher values of $V_1$ may lead to decreased power consumption in the test mode. Thus, $R_2$ should be lower.

## 4.4 Analysis

The sensitivity of the output voltage to variations in $R_1$, $R_2$ and the diode voltage were discussed. We also discussed the effect of $R_2$ and $V_1$ on the power consumed in the test mode. In all the above cases, we had to either increase or decrease $R_2$ to minimise the impact of their variations on the output voltage. To summarise, $R_2$ should be

- High to minimise the impact of $V_{be}$ on the output voltage
- Low to minimise the impact of $R_1$ on the output voltage
- Low to minimise the impact of $R_2$ on the output voltage
- Low to reduce the power consumed in the test mode

The following approximations were made in the analysis for the effect of variation of $R_1$ or $R_2$ on the output voltage: Any change in either $R_1$ or $R_2$ changes the current $I_1$ flowing through the test circuitry. Change in the current $I_1$, changes the diode voltage $V_{be}$. A small change in the diode voltage leads to a large change in current in the diode curve. In other words, for a large change in diode current, the change in diode voltage is quite small. Hence, $V_{be}$ can be assumed almost constant. Recall from equation 4.10 that the output voltage is directly proportional to the change in the diode voltage. Since the change in diode voltage is negligible even for a large change in current, the effect of $V_{be}^{\Delta}$ on the output voltage is small.

Once the chip has been fabricated, it is not possible to alter the value of $R_2$. $I_1R_1$ is the imbalance voltage. When either $R_1$ or $R_2$ varies, $I_1$ changes, which affects the imbalance

voltage, $V_{imb}$. $R_2$ should be high to minimise the effect of change in $V_{be}$. However, $R_2$ should be low to minimise the effects of $R_1$ and to reduce the power consumed in the test mode. Hence, we need to compromise on an optimum value for $R_1$ and $R_2$, to not affect the output amplitude.

## 4.5 Case study

The above concepts can be best understood with the aid of an example. We present a case study to illustrate the concepts:

Let us consider a grade 5 gate in the numerical examples given below. Let, $R_2$ = 3.96 K Ohm, $V_1$ = 1.5 V, n = 1, $R_1$ = 500 Ohm, Vcc = 3.3 V. Output voltage = 130mV. Let, $V_{imb}$ = 120 mV, and $I_1 = 2.06 \times 10^{-4}$ Amps; $V_{be}$ = 0.885 V.

### 4.5.1 Sensitivity of the output voltage to Vbe variations

Let us assume that $V_{be}$ varies from 0.885 V to just 0.890 V. Then from Eq 4.10, the output voltage changes by,

$$\partial V_{out} = 0.56mV$$

### 4.5.2 Variation in $R_1$

Let us assume that $R_1$ varies by 5% i.e., $R_1$ varies by 25 Ohm. Then from Eq 4.17, the output voltage changes by,

$$\partial V_{out} = 4.57mV, \text{ when } R_2 = 3.96 \text{ Kohm.}$$

If $R_2$ was low by design, say $R_2$ = 2.96 Kohm , then the same variation in $R_1$ would affect the output voltage by,

$$\partial V_{out} = 4.41mV \text{, when } R_2 = 2.96 \text{ Kohm}$$

On the other hand, if $R_2$ was high by design, say $R_2$ = 4.96 Kohm, then the same variation in $R_1$ would affect the output voltage by,

$$\partial V_{out} = 4.67mV \text{, when } R_2 = 4.96 \text{ Kohm}$$

Therefore, when $R_2$ is low, the effect of change in $R_1$ on the output voltage is low.

### 4.5.3 Variation in $R_2$

Let us assume that $R_2$ varies by 5%

From Eq 4.22,

$$\partial V_{out} = 4.57mV \text{, when } R_2 = 3.96 \text{ Kohm \& } \partial R_2 = 198 \text{ Ohm}$$

$$\partial V_{out} = 4.67mV \text{, when } R_2 = 4.96 \text{ Kohm \& } \partial R_2 = 248 \text{ Ohm}$$

$$\partial V_{out} = 4.41mV \text{, when } R_2 = 2.96 \text{ Kohm \& } \partial R_2 = 148 \text{ Ohm}$$

Thus, we see that the change in output voltage is low when $R_2$ is designed to be low.

### 4.5.4 Power consumed in the test circuit

From equation 4.23, the power consumed in the test mode is:

= 0.37 mW, when $V_1$ = 1.5 V

= 0.47 mW, when $V_1$ = 1.0 V

= 0.26 mW, when $V_1$ = 2.0 V

Obviously, when $V_1$ is high, power consumed in the test circuitry is low. For a given imbalance voltage, when $V_1$ increases or decreases, $V_{be}$ and $R_2$ should vary. From Eq 4.25, $R_2$ is given by,

$$R_2 = \frac{Vcc - V_1 - n \cdot Vbe}{I_1} - R_1 \qquad \text{Eq 4.26}$$

If $R_2$ alone had to be varied to compensate for the change in $V_1$, then

$R_2$ = 3.96 Kohm, when $V_1$ = 1.5 V

$R_2$ = 6.36 Kohm, when $V_1$ = 1.0 V

$R_2$ = 1.51 Kohm, when $V_1$ = 2.0 V

## 4.6 Environmental factors

So far, we discussed the effects of variations in the resistors and the diodes on the output voltage. These variations may be caused by temperature, process or other environmental factors. In this section, we discuss other factors that might affect the output voltage.

### 4.6.1 Impact of chip warming up

When a chip is powered up, its temperature rises above the room temperature. If the test is carried out during this period, then the results may not be correct. This is because the diode characteristics are subject to temperature variations.

### 4.6.2 Effect of cooling

Absence of cooling may also affect the performance of the technique, as the applied imbalance may not be the same as the expected one. If the applied imbalance is greater than expected, then stress accumulation may occur. If the applied imbalance is lesser than the expected imbalance, the coverage is reduced. $V_{be}$ increases with rise in temperature. Referring to equation 4.10, we see that $V_{out}$ increases in direct proportion to $V_{be}$.

### 4.6.3 Other factors

Information on the following factors will be of significant value in estimating how the technique performs under process and temperature variations.

- Temperature gradient
- Temperature gradient in the test time context i.e., in a short duration
- Expected die temperature
- Average temperature across the die

## 4.7 Conclusions

We have modelled the effect of variations in $R_1$, $R_2$, and $V_{be}$ on the output voltage. These effects can be alleviated. It is the designer's choice to use the appropriate number of diodes and to chose the right value for $R_2$ and $V_1$. With such a high degree of freedom, this technique can easily be modified to suit the design on hand and still obtain good defect coverage.

# CHAPTER 5

# THE TESTING OF THE TEST CHIP

## 5.1 Introduction

The DFT techniques developed for bipolar CML gates were implemented in a test chip in order to study their performance in an actual circuit. This chapter describes the various DFT structures implemented in the test chip designed by Patenaude and Antaki [4, 29]. It also presents the custom test pattern generation process for this test chip. Some of the available test results are presented.

The chip was designed using the NT25™ technology of Nortel Networks. It was manufactured in sufficiently large quantities to ensure we would find enough fabrication defects to verify the proposed DFT techniques. The purpose of this chapter is to describe the test strategies, and how the corresponding test vectors were generated. Due to a number of practical problems, the test chip is yet to be fully analysed, and most of test results are not available at the time of completing this document. Only the available results are discussed in this master thesis. The following section briefly describes the architecture of the test chip.

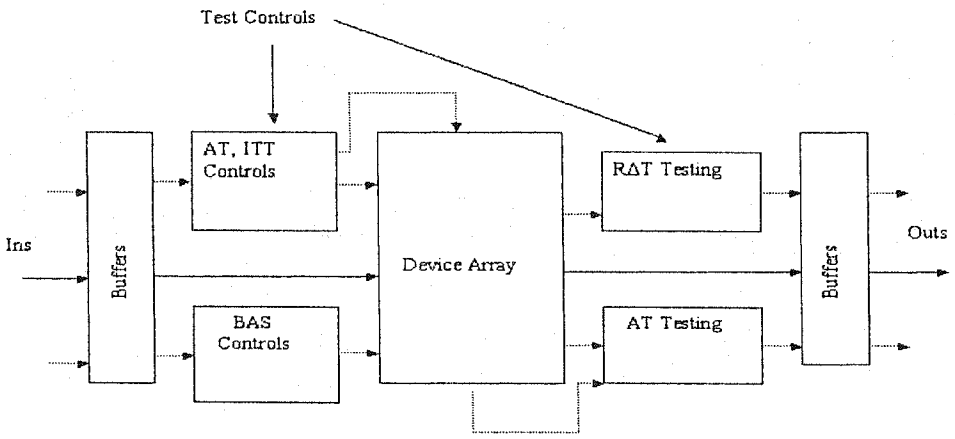



**Figure 5.1 Block Diagram of the Test Chip**

## 5.2 The Test Chip

Figure 5.1 shows the block diagram of the test chip, which comprises two main blocks: (i) the device array block (see figure 5. 2) and (ii) the test control block. The two blocks are interleaved to form the architecture of a matrix – intersecting device rows and test columns, as shown in figure 5.3. This architecture allows for the easy testability of any particular selected gate. The signals and the structure of the gates will become clearer as we progress through this chapter. The two blocks are discussed in the following sections.

## 5.3 Device Array Block

This section briefly describes the various elements of the device array [4]. Figure 5.2 shows the block diagram of the device array. The device array block consists of the logic gates to be tested. Gates of different speed grades are connected to form very simple logic functions. Chains of BUFFERs, AND, and XOR combinational blocks, as well as level sensitive shift registers with re-configurable state machines are present in the device

array. Though the test chip circuitry was designed to resemble an actual chip, it was kept simple to ease the validation of the testing methodologies.

In the matrix architecture, the chains form the rows of the matrix, and the test controls follow the columns of the matrix. A series of logic gates are connected together in tandem to form a chain. The device array has the following rows: BUFFER chain (grade 0, grade 6, and mixed grades), two input AND gate chain with input 'a' sensitised, and with input 'b' sensitised (each in grade 0 and grade 6), latches (grade 0 and grade 6), two input half XOR tree - part A and part B (each in grade 0 and grade 6), and shift register (grade 0 and grade 6). Their structure is discussed below.

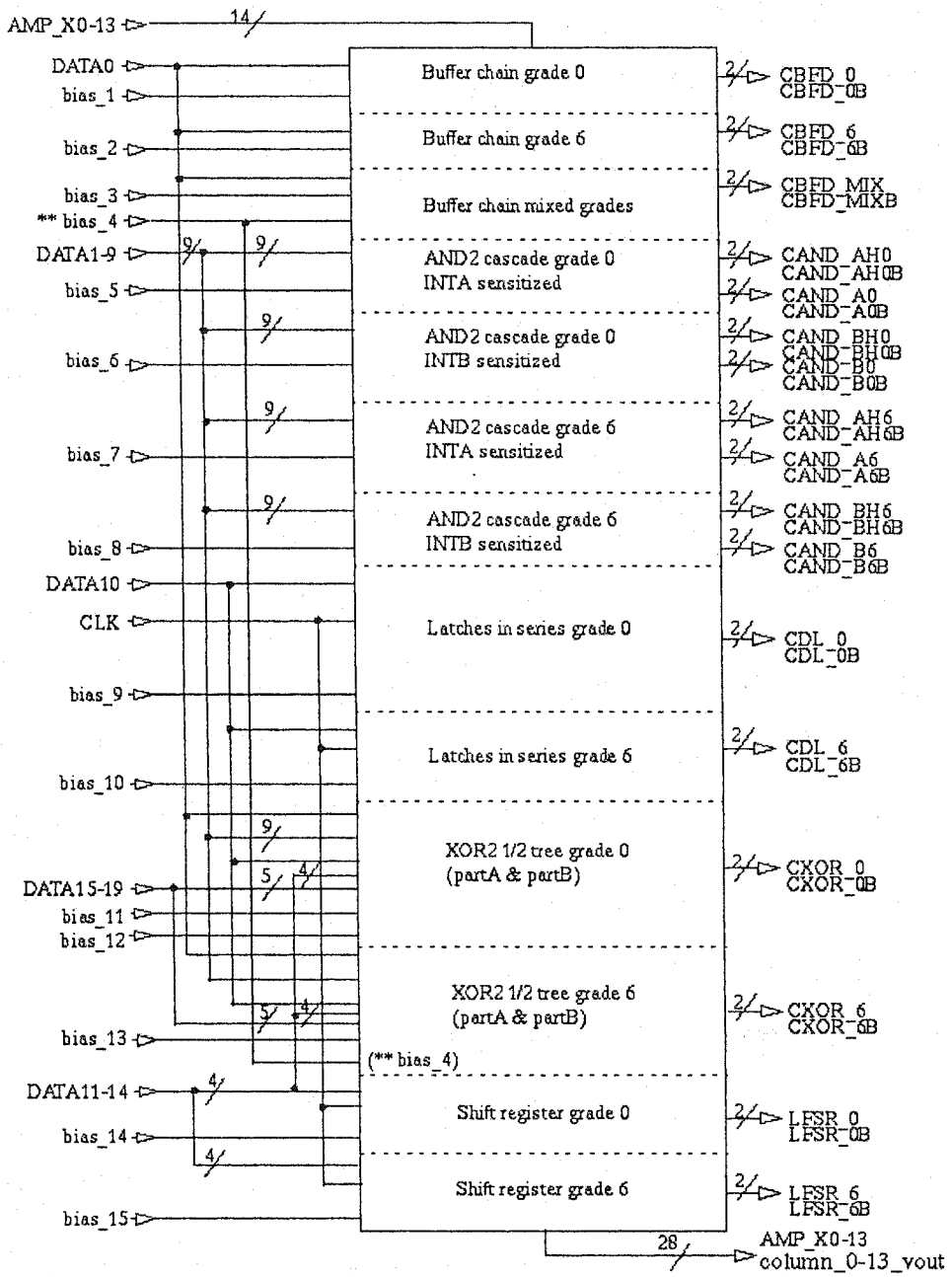



**Figure 5.2 Block diagram of the device array**

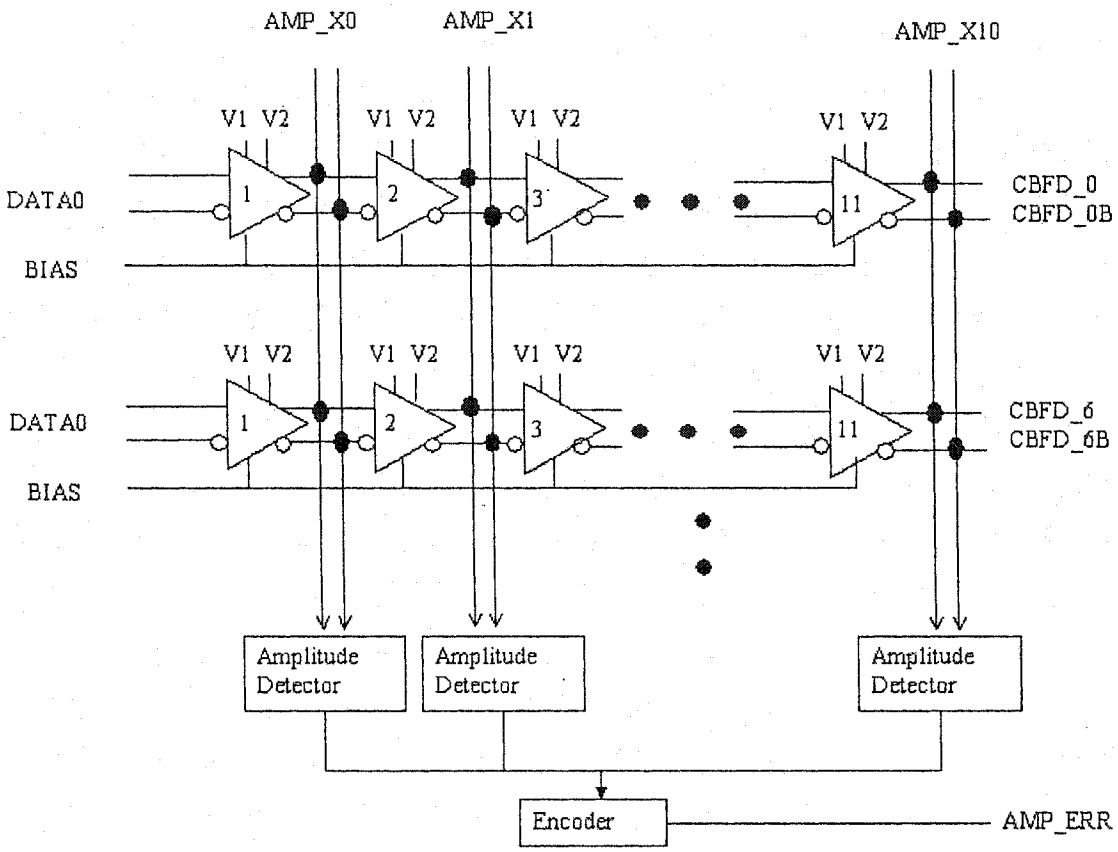


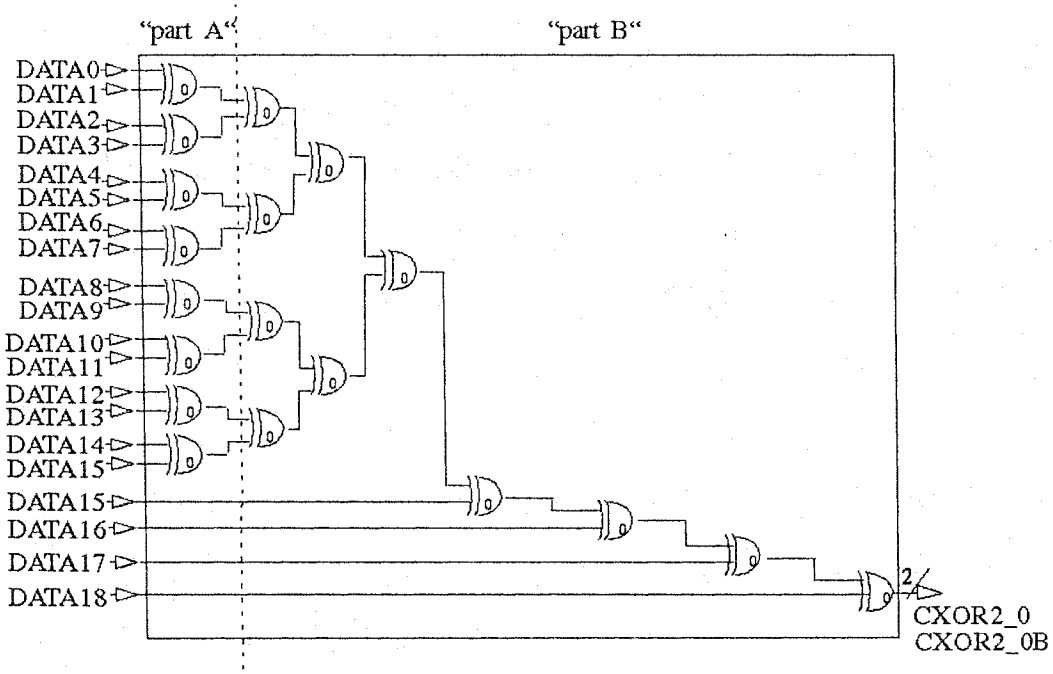

**Figure 5.3 Matrix architecture**

### 5.3.1 BUFFER

The buffer chain is made up of 11 gates connected in series. Grade 0 and grade 6 buffer chains each have one bias supply line. The mixed grade buffer chain consists of gates in the following pattern of grades 0, 1, 2, 4, 6, 0, 1, 2, 4, 6 and 0 (11 gates in total). Since this chain has mixed speed grades, two different bias lines are provided for this row. Recall that grade 0-3 gates on the one hand and grade 4-6 on the other hand use a different bias generator.

### 5.3.2 XOR

The XOR half-tree row is an eight gate deep combinational circuit. As the name implies, the first four columns of the row (half the depth of the chain) have a tree structure, and the other 4 gates are just cascaded. The figure below shows the architecture of the XOR row.




Total logical depth is 8.

**Figure 5.4 XOR half tree**

### 5.3.3 AND

The AND gate cascade rows can be made depth sensitive, with a total logical depth of 8 gates. Since the transistor level structure is different for 'input a' and 'input b', both versions are implemented in both grades 0 and 6. For all the versions, the signal at half the depth is also made available on the output pins.

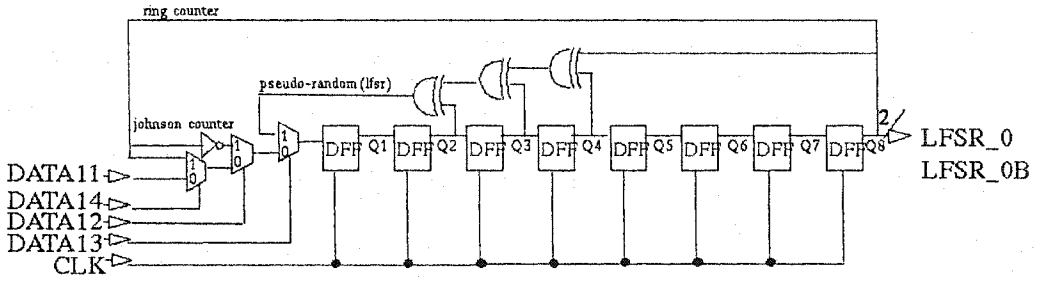
### 5.3.4 LATCH

The re-configurable shift register implements a re-configurable finite state machine. This row can be operated in four modes - (a) eight bit shift register with one input, (b) ring counter, (c) Johnson counter and, (d) linear feedback shift register. Pins 'Data14-12' control the mode of operation (see table 5.1). The data pins are used as control pins here.

Data 11 is the input to the 8-bit shift register. Figure 5.5 shows the architecture of the re-configurable shift register.

**Table 5.1 Modes of operation of the re-configurable shift register**

| DATA13 | DATA12 | DATA14 | Mode of Operation |
|---|---|---|---|
| 0 | 0 | 0 | 8 bit shift register (input is Data 11) |
| 0 | 0 | 1 | Ring Counter (looping shift register) |
| 0 | 1 | X | MODULO 16 Johnson Counter |
| 1 | X | X | LFSR or Pseudo-random counter |




Total logical depth is 11.

**Figure 5.5 Re-configurable shift register**

## 5.4 Test control block

The main objective of the test chip is to validate the DFT techniques proposed for bipolar CML gates. The test control block generates the signals that exercise the DFT circuitry in the bipolar CML gates in the test chip. The testability methods incorporated in this test chip are: Bias Alteration Stressing, Amplitude testing, Reduced Delta testing and Imbalance testing. They are discussed below:

### 5.4.1 Bias Alteration Stressing (BAS) Technique

Reduced bias is applied to a circuit in the test mode to control the gain of the gate. The output amplitude is then passed through a detector to detect fabrication defects. BAS is implemented on all the rows of the test chip. To enhance detection of fabrication defects, the signal is passed through RΔT detector, designed for 'Reduced Delta Testing', further discussed in section 5.4.4.

### 5.4.2 Imbalance Testing Technique (ITT)

ITT is a two pass testing technique. Bipolar CML gates are differential and hence have a pair of output lines. Each output line of the gate is imbalanced to stress the gate sufficiently to transform any marginal signals into stuck-at faults. The induced faults are propagated to the output of the circuit and can be observed. In the test chip, ITT is implemented in all BUFFER, and AND gate chains, both grade 0 and grade 6, with the exception of the mixed grade BUFFER chain.

### 5.4.3 Amplitude Testing

Excessive output amplitudes can be detected by the specially designed Amplitude Testing circuitry that observes the differential output signal. In the test chip, AT is implemented on all the columns. Thus, all gates in the same column of the matrix share the same AT detector. A signal with a voltage of 0.4V above Vcc is applied to the test line, to activate Amplitude testing. The outputs of the 'Amplitude Test' (AT) signals of all the columns are input to a big OR gate, whose output is connected to an output pin, thereby reducing

the number of outputs of AT to one pin. When a defect is detected, AT outputs a 1, (otherwise AT outputs a 0). Since the outputs from all the columns of the matrix are ORed, a defect in any column would output a '1'. This just flags the presence of a defect in the circuit. However, the defective column can be located by turning only one AT signal 'ON' at a time, thereby testing only one column at a time. Thus, when the output goes high, some gate in the column that was tested at that time is defective.

### 5.4.4 Reduced Delta Testing (RΔT)

RΔT technique detects faults that cause the absolute output voltage swing to remain below a given value, during a given time interval 't', where 't' is long enough to allow switching in defect-free gates without triggering detection of this defect type. A reduced delta detector is connected to the output of each row of the device array. When the output of the last gate of the chain is passed through the detector, it checks this amplitude against a preset threshold, to detect any low remaining output noise margins. This method tests only the last gate of the chain. Though RΔT is present in the test chip, no specific test vectors are applied to characterise its dynamic features. RΔT is used in conjunction with BAS to enhance the detection of fabrication defects. BAS induces the propagation of local fault effects through the logic and allows the detection of such fault effects by means of voltage tests that target standard stuck-at faults. In the test chip, a RΔT detector is implemented in all the Buffer, Latch, XOR, AND, and LFSR rows.

Each of the above DFT techniques is used to observe a subset of the fabrication defects in bipolar CML gates. While AT identifies the column of a defective gate in the matrix, RΔT and BAS identify the row of a defective gate in the matrix. Thus, if both AT, and one of RΔT, BAS or regular voltage testing detect a defect, then the defective gate can be located precisely, by combining the failing row and column numbers.

Some DFT methods have been studied in much more detail, since the time the test chip was designed. Although our understanding of the DFT techniques under study has increased and the methods have been refined since then, the basic concepts remain the same. For instance, the ITT implemented in the test chip has only one Schottky diode, whereas in a recent study we used also a resistor and sometimes two diodes to reduce sensitivity to parasitic elements and process variations.

### 5.5 Test pattern generation flow and the Testing process

This section describes Nortel's design flow for generating the test patterns. We also discuss the different tests carried out on the test chip, including the standard tests. The chip can be tested using standard methods like voltage testing, continuity testing, etc., to ensure connectivity between the die's IO ports and the package pins through the pads. The chips are then tested for their functionality to isolate the defective ones. The functional test is used as a reference against the proposed DFT techniques in identifying the defective parts. The objective here is to compare their respective coverage and to find related defects to assess their qualitative significance.

The test pattern generation for this test chip was done manually, no ATPG tool was used. The tests for the test chip are simple enough to test the functions of the gates. They exploit the structure of the DFT controls, which is expected to help locate many defects in the chips. Test vectors are generated using Verilog and Anvil. 'Anvil' is a C Macros language, proprietary to Nortel Networks. A test vector consists of two parts: a) the stimuli applied to the inputs of the chip, and b) the values expected at the outputs of the chip. The stimuli are specified in the Verilog test bench. This is simulated as applied to a simple model of the test chip. The Verilog circuit model has no timing information, and it is expressed only with conventional digital signals, i.e. not the differential signals that stimulate CML gates on the tester. This Verilog simulation produces the expected values at the outputs. Both the input stimuli and the simulation outputs are saved in different files. Verilog simulation also produces a dump file called Value Change Dump (VCD), which has the values of the applied inputs and the simulated outputs, for the length of the simulation. The signals can be viewed using a waveform viewer called Signal Scan.

All the timing information for the waveforms is included in Anvil. User patterns created by Anvil are placed in the 'datahub' by 'dhio', datahub input output. A datahub is a database directory for storing test related information of the chip. Figure 5.6 below illustrates the relationships between these various tools and data representations. The datahub contains the timing information, the test patterns (input stimulus), and also the expected output values, all in binary format. The datahub directory is passed on to the

test engineer, who then extracts the test information from it and applies it to test the chip. The expected outputs of chip will be used on the tester to verify the observed outputs at specified time points (for example, any time an event is expected to occur according to the test bench). Sptran extracts an spdata file from the datahub. The waveforms in the spdata file can be viewed using a Nortel Networks proprietary tool called Shadow. Based on this brief introduction to the tool flow for test pattern generation and verification, let us now discuss how each test is carried out.

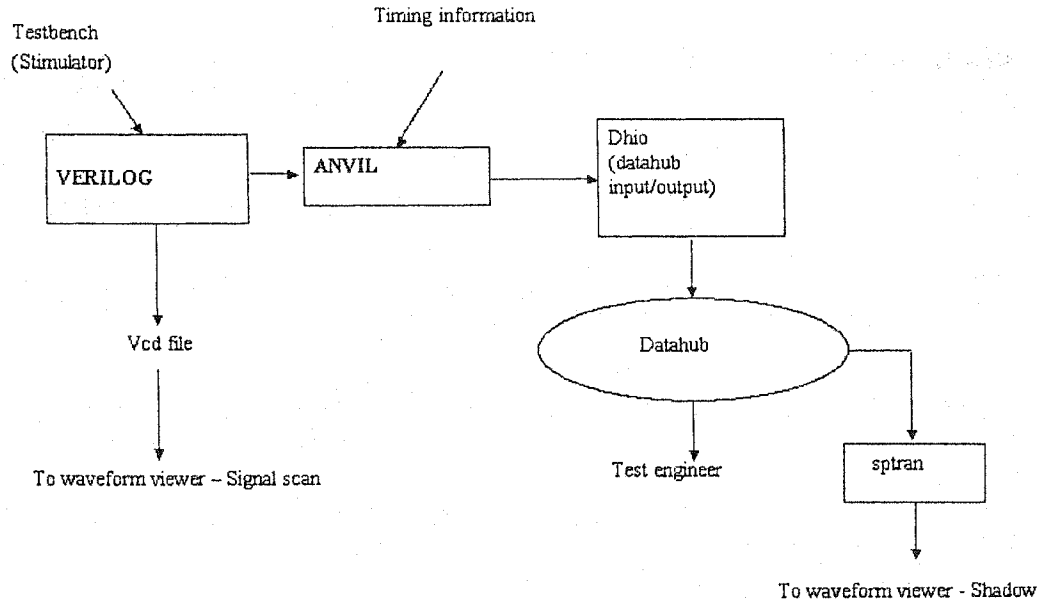



**Figure 5.6 Test pattern generation tool flow**

## 5.6 Test pattern generation and the testing of the test chip

This section describes how test vectors were generated for both the functional tests (propagation delay tests) and the proposed DFT methods. We also discuss how these vectors are applied to the chip.

Antaki developed a first skeleton of the test vector sets for the test chip. This only exercised the voltage test. The test vector sets have been extensively upgraded since then, in order to exercise all the DFT structures, and to make the tests suitable for the tester. If a defect flag output is triggered when activating a DFT technique, then such defects can be detected. Note that none of the testing techniques used offer complete coverage of all possible physical defects. During the revision process, 'Amplitude testing' was included in the test vector set, to allow locating precisely the column where parts of the defects are. By contrast, the BAS technique targets the rows (See figure 5.1). ITT was included in the test vector set, and the test chip allows imposing various degrees of imbalance to characterise their impact on coverage and on test robustness (noise margins of defect-free devices can be reduced to zero with excessive imbalance).

Immediately after power up, the switching times of the gates on the chip may change while the device is warming up. In order to avoid spurious compare failures, immediately after power up, the data input pins of the chip are toggled for a time sufficient to warm up the chip, and stabilise the functionality of the gates. Then, the tests are executed one at a time in the following order: voltage testing, amplitude testing, imbalance testing and BAS testing.

Each row of the device array has a dedicated Programmable Bias Generator (PBG), making independent study of each row possible. The desired PBG can be selected with the address pins PBG_ADD3-0. Address 'zero' connects the output of a PBG directly to

the output pin PBG_MON, to monitor the functionality of the PBG directly. There are three modes of operation for the Programmable Bias Generator (PBG). Pins PBG_VAL [1-0] are used to choose one of the three modes of operation. Bits 00 on PGB_VAL is for normal functional mode, 01 is for test mode, and 10 is for OFF mode. Pattern 11 is not used. Pins PBG_ADD [3-0] are used to specify the address of the row to receive the bias. Each PBG needs to be initialised first before testing can start. The PBG of each row can be in any one of the three modes, independent of the other PBGs. The PBGs are configured one at a time. After power up, it is required that each PBG be configured into one of the three modes. After this is done, each PBG can remain configured in that way throughout the remainder of the test, or, if desired, it can be reconfigured into a different mode from time to time.

While in the normal mode of operation, all the chains receive the regular bias voltage, 1.104V for speed grades 0-3 and 1.194 for speed grades 4-6. The test mode is used for BAS technique, and is set in the rows having a RΔT detector. While in the test mode, the rows receive a bias of 0.88V for speed grades 0-3 and 1.023V for speed grades 4-6. The bias voltage is low enough to turn off the gates it drives in the OFF mode and the unused mode. In the vectors we generated, after power-up, we set only two PBGs in the normal mode, and all the others in the OFF mode. These two PBGs correspond to the PBG_MON signal and the grade 0 buffer row. DATA0, input to the grade 0 Buffer chain, is toggled for a few cycles to warm up the chip, and then various tests are executed, as discussed below.

### 5.6.1 Voltage test

This tests looks for the presence of classic stuck-at faults and ensures that I/Os function properly.

### 5.6.2 Propagation Delay test

Twenty-two propagation delay test vectors were generated for the test chip. Propagation delay is measured from each input of a chain to the output of the chain. The propagation delay from an input to an output is defined as the time it takes for the output to reflect any change in the input. If a chain has many inputs, only one input at a time is toggled for a particular propagation delay test.

Since the test chip is only made up of simple logic gates connected in series to form a chain, propagation delay tests can be carried out with relatively few test patterns. Delay faults are one of the fault models considered in comparative analysis. Propagation delay tests serve two purposes. Firstly, they ensure that the gates operate at the proper speed. Thus, this test is used to identify the slow devices. Such chips can be used to gauge the effectiveness of the proposed DFT techniques. If these chips are also identified as defective by the proposed techniques, then we are successful in isolating the slow devices from the lot, without using at-speed testing. On the other hand, if the new DFT techniques fail to identify such slow devices, then they may still be very effective in detecting other defects that don't induce slow speed behaviour.

Secondly, propagation delays play a very important role in monitoring the outputs of the device array elements. Once the propagation delays are obtained for all the device arrays, the measurement of outputs from the test structures are done 'propagation delay' time units after the input is applied, to avoid miscompares. Such events may occur if this delay is not properly accounted for, thus declaring a defect free chip as defective.

Now, having discussed functional testing, let us discuss the test pattern generation and the execution of the test itself for the proposed testing techniques – AT, RΔT, BAS and ITT. The tests are done at low frequencies. The proposed DFT techniques on the chip are activated one at a time to make the analysis simple, and to ease fault location. It is important to make the most of the limited tester time, but still carry out different tests independently.

### 5.6.3 Amplitude test

To ease fault location, one amplitude test signal is turned on at a time (one per gate column) and the test stimuli for voltage testing are applied. The output goes to an 'Amplitude detector' which compares the obtained output with that of the present threshold value. When the test for a column has been completed, the amplitude-testing (AT) signal for this column is turned off and the AT signal for the next column is turned on simultaneously. The process is repeated 14 times, once for each column. The outputs of amplitude detectors are ORed together to reduce the number of output pins. The pin

AMP_ERR goes high when a defect is detected. After all the columns have been tested, all the amplitude-testing signals are deactivated.

### 5.6.4 Imbalance test

Imbalance Testing is done simultaneously on all the device rows implementing this technique. Two pins of the test chip, $V_1$ and $V_2$, are used to imbalance the device. Bipolar CML gates are differential, and hence have two input and two output lines. $V_1$ applies an imbalance voltage to one of the output lines, and $V_2$ imbalances the other output line. The voltage applied on either $V_1$ or $V_2$ lowers the remaining output noise margin. For imbalance testing, only $V_1$ or $V_2$ is activated at a time. Varying the voltages on $V_1/V_2$ varies the imbalance level. The outputs for different imbalance levels, viz., 100mV, 120mV, and 130mV are studied. The objective is to find an optimum imbalance level that is strong enough to provide a high coverage of defects in the circuit, but weak enough to avoid declaring good circuits defective. This optimum imbalance level varies with the speed grade and the type of logic gate.

In a direct test, test vectors are applied at the inputs, and the results are observed at output pins. In ITT, the immediate results are only available at the output of the gates. The analog voltages resulting from the tests are not passed on output pins. However, the combined effect of a defect and the applied imbalance causes a defective gate to exhibit stuck-at behaviour, thus causing all the following gates in the chain to propagate this

condition. This stuck-at behaviour can be observed as a digital signal at the output pin of the chain.

### 5.6.5 BAS test

Rows implementing the BAS technique are then tested. Programmable bias generators (PBG) are used to activate the required rows for BAS testing. Like ITT, BAS testing does not have dedicated output test pins. When a low bias is applied, a defective gate may exhibit a stuck-at behaviour or output a very low remaining noise margin. The gates following the defective gate tend to propagate and degrade this condition, which makes the presence of defect causing this behaviour observable at the output. BAS is also based on a detector designed by Patenaude [29], which detects the defects by comparing the obtained noise margin with a preset threshold value. Both ITT and BAS stress the gates enough to translate marginal signals into stuck-at behaviours or into low amplitude conditions that propagate through multiple gate levels.

## 5.7 Test results

The test chip was tested on a tester with the test methods discussed thus far. For various reasons outside our control, the test process has not been fully completed at the time of writing this thesis. While most of the proposed tests have been carried out, detailed results for propagation delay tests are available now and partial results are available for the other tests. The available results are discussed in this section.

The test chip was tested for continuity test, voltage test, AT, BAS, ITT and propagation delay. 44 defective parts were identified on a total of 500 parts that were tested. These

44 defective parts will be referred to as the tester-failed group. The breakdown of the failures is as follows:

- 7 failed continuity (3 shorts and 4 opens)
- 10 parts had excessive supply current (IDD)
- 18 parts failed the propagation delay test (the output did not change during the test)
- 5 grade 0 AND chain failures
- 1 grade 0 XOR row failure
- 2 grade 6 AND row failure
- 1 grade 0 latch row failure

In order to gain more insights into these 44 failing parts, we decided to retest these devices. After analysing the propagation delay data, we selected an additional 13 parts that would be worth retesting. A total of 57 parts has been retested.

Propagation delay data for all the 500 parts and all 402 different paths was available. This information was analysed by Monté, and is discussed here. Parts that have delays much greater than the mean propagation delay are identified (slow parts), and are selected as suitable candidates for retesting.

The test chip does not have just one propagation delay. There are a number of chains of different gate types, and different speed grades, and each such chain has its own propagation delay value for both the rising and the falling transitions. This value is measured across all the 500 parts and an average is obtained. Some of these values are listed in the following table:

**Table 5.2 Propagation delay – mean and sigma values**

| | LFSR_0B – Falling edge | CAND_A0 – Rising edge | CAND_A6B – Rising edge | CXOR_0B – Rising edge |
|---|---|---|---|---|
| Mean | 34.4 ns | 11.7 ns | 1.25 ns | 50.6 ns |
| Standard deviation | 1.151 ns | 3.159 ns | 0.0257 ns | 0.91 ns |

Twenty-four parts had at least one zero delay value, i.e., the output did not change during the test. Thus, these parts did not function at all in the test. These 24 parts are also in the tester-failed group. These 24 parts were not included in the list of 500 to calculate the mean and standard deviation for each delay path. However, these parts were included in the rest of the analysis. For each delay path, parts deviating by a multiple (10x, 5x, 4x) of sigma from the actual sigma value were identified. The results are summarised below:

- 36 parts deviated from the mean propagation delay by 10 sigma. All of them except two were in the tester-failed group.
- 44 parts deviated from the mean propagation delay by more than 5 sigma. 6 such parts were not in the tester-failed group.
- 49 parts deviated from the mean propagation delay by more than 4 sigma. 13 such parts were not in the tester-failed group.

The figure below illustrates the relationship between the two groups of parts: the tester-failed group and the greater than 4-sigma deviation category in the form of a Venn diagram. The left circle shows the number of slow devices (with delays exceeding the average delay by more than 4 times the standard deviation), and the right circle shows the number of parts in the tester-failed category. 36 slow devices were also in the tester-failed group, whereas 8 tester-failed parts appeared to have normal delays. This is the

intersection shown in the figure. The union of the two groups is 57 parts – the parts that were retested on the tester in order to better understand the failures.

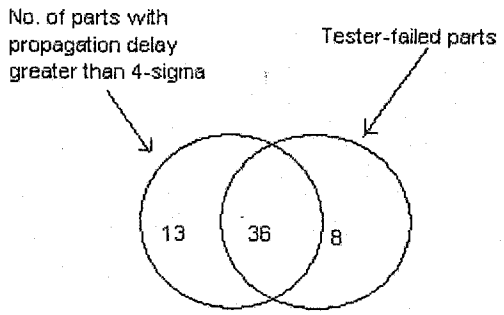



**Figure 5.7 Venn diagram of the tester-failed and sigma deviation parts**

In the retest, some of the parts failed many tests (massive failures) and some of the parts failed only a few tests (limited failure). We do not have sufficient information about which parts failed what tests, and hence is not discussed here. The results have to be analysed, and further testing of the test chip is required.

We've discussed the test results available so far. Once we successfully isolate all the defective parts using the proposed DFT techniques and locate the defective gate/chain, engineers at Nortel could use "microanalysis" to find out the actual cause of the defects. Using microanalysis it is possible to physically look at the die and locate the spots with manufacturing defects. With this result, we could confirm that the fabrication defects we aim at identifying with the proposed DFT techniques are not trivial, and the proposed test

techniques identify defective parts that could fail in the field, even if they pass conventional voltage testing.

## 5.8 Summary

This chapter discussed how the different test structures implemented in the test chip are exercised with the custom test patterns that were generated using Nortel's tool flow. Defective parts were identified using (a) functional patterns and/or (b) using the proposed DFT techniques. The available test results were presented in this chapter. While some results available so far are quite impressive, further study is required to draw conclusive results on the effectiveness of the proposed test methodologies and this is left for future work.

# CONCLUSION

In this thesis, the importance of testing bipolar CML gates, and the lack of relevant literature were explained. We studied fault propagation in bipolar CML gates. A defect that has a strong impact on the behaviour of CML gates was chosen for the purpose of this study. Performance degradation of bipolar CML gates in the presence of manufacturing defects has been reported in detail. We also studied some of the Design For Testability techniques for Bipolar CML gates in detail.

In the second chapter, we showed that though Bias Alteration Stressing technique effectively distinguishes a defect-free gate from a defective one, the remaining output noise margin is very low for a chain of gates. We also showed that the noise margin for which a detector was designed by a previous team would not be able to successfully differentiate a defect-free circuit from a defective one. It is conjectured that the noise margin available for testing would go down further for different speed grades, and different gates, in different circuits. This is compounded by the variations in the manufacturing process itself, as demonstrated in chapter 2. Hence, this technique is not suitable for bipolar Current Mode Logic gates.

In the third chapter, we studied a two-pass test technique. In Imbalance Testing Technique, the gate is sufficiently imbalanced leading any marginal signals to cause stuck-at behaviour. The test circuit has been modified from the originally proposed

version, which had just one diode. It was demonstrated that the amount of imbalance applied is an important factor for the performance of the defect-free bipolar CML AND gates. Solutions to circumvent the problem of imbalance accumulation were presented along with a set of design guidelines for testability. This is indeed a significant achievement in the literature that relate to the testability of bipolar CML gates. It is easier to test a logic family, when a thorough understanding of its behaviour in the presence of defects is available.

In the fourth chapter, we characterised the performance of bipolar CML gates in the test mode due to variations in the process and environmental factors. We discussed in detail the sensitivity of the output voltage to variations in each component of the imbalance circuitry. Importantly, design guidelines to minimise these variations were presented.

Also, we discussed the test generation process for the test chip that implements some of the testing techniques studied. The fifth chapter showed that generating test patterns for the test chip implemented by a previous team was not a simple task. These patterns made it possible to effectively distinguish the chips with manufacturing defects from the defect-free ones. The testing is yet to be fully completed, and some of the available results were presented in this chapter.

We believe that this thesis has provided a better understanding of the performance of the studied bipolar logic family in the presence and absence of defects. With this knowledge,

testing becomes easier as the expected behaviour is known beforehand. Also, a promising structural DFT method, the ITT has been studied in great detail. We are convinced that this work lays a solid foundation for further research on the testability of bipolar CML logic circuits.

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# APPENDIX I

Values of the applied signals and bias voltages

1. input 1: 3.3 V to 3.05 V toggling signal with a frequency of 1 MHz
2. input 2: 3.05 V to 3.3 V toggling signal with a frequency of 1 MHz
3. vcc: 3.3 V dc
4. vbias: variable dc
5. vhigh: 3.3 V dc
6. vlow: 3.05 V dc
7. vee and vsub: Connected to the substrate
8. A tie-down was added to establish a link between the substrate and vee and vsub.

# APPENDIX II

In this appendix, we show the limitation imposed on the usable range of bias voltage for BAS testing and discuss the various methods that we attempted to improve the usable range of bias voltages for BAS testing.

When insufficient bias is applied, a defect-free chain does not have enough gain to amplify a very low noise margin input signal, and hence the output dies. This is shown in the following figure. Where applicable, a 100-Ohm short is present at the a-ab input of the DUT.

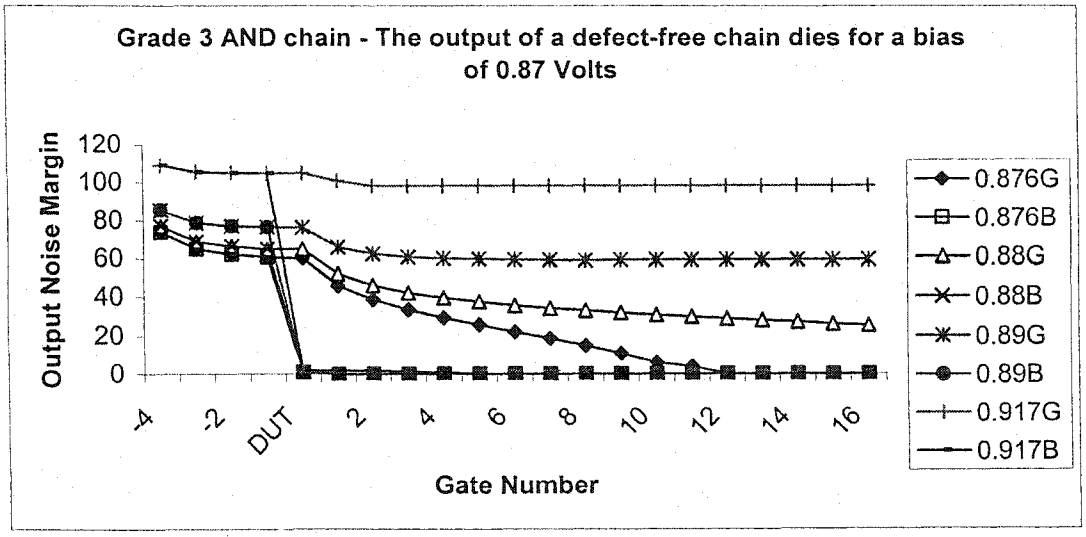


**Figure II.1. The output of a defect-free grade 3 AND chain dies when the bias voltage is low (0.876 G in the figure)**

## OR Gate Used As A Buffer In The AND Chain

The following figure illustrates how an OR gate is used as a buffer to regenerate the signal. As before, the test bench is grade 3 AND chain. 'Buffer1' is the input to the first buffer, and 'Buffer2' is the input to the second buffer. As seen from the figure, for a bias

of 0.876 Volts, the defect free chain is differentiable from the defective chain. The buffer tries to restore the signal amplitude. However, this improvement is not significant. Similar results are obtained when XOR gate is used a buffer.

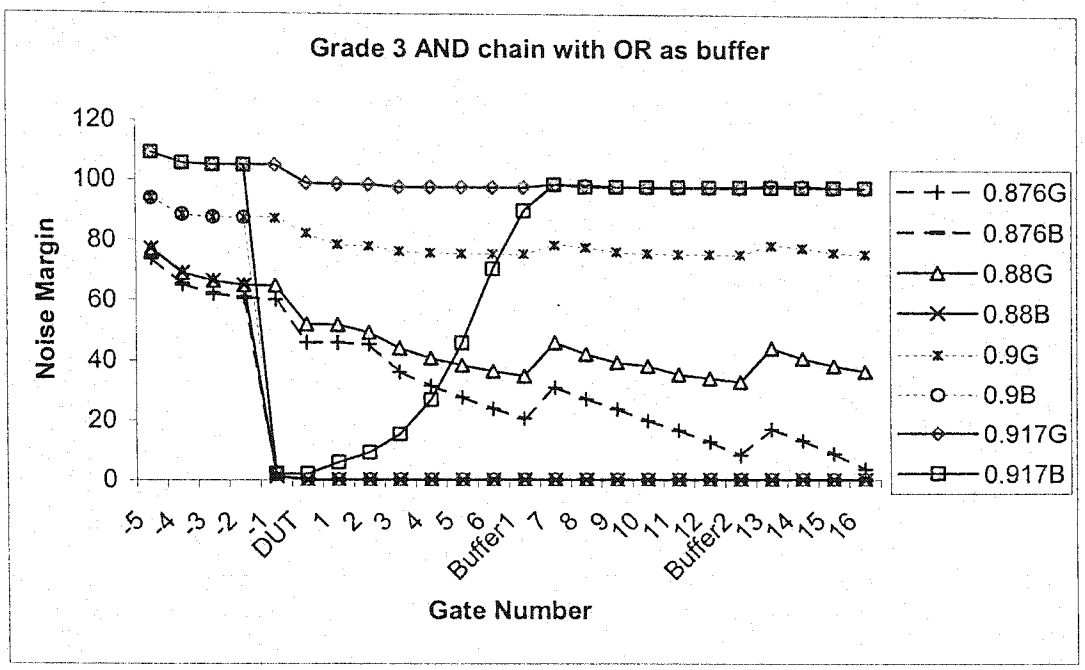


**Figure II.2. AND gate (grade 3) with OR as a buffer and a 100-ohm short at a – ab**

# APPENDIX III

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What simulator would you prefer (Spectre=1, Spice=0)?
File name listing cells to analyse:
List of stimuli file name:
Test bench file name: Beginning of simulation -- gold
CELL: andITT_grad5
RESULTS
Presentation order: Stress-vectors, logical levels, op, opb, abs(NM), NM, diff, NM1, rank
stress_vectors: v1w1 v2w1 v1w2 v2w2 v1wo v2wo
logical levels: vin1 vin2
Definition of the different variables :
Stress vectors
v1w?: is the stress input on the left side of the gate
v2w?: is the stress input on the right side of the gate
v?w1: is the buffer connected to the A line of the following DUT
v?w2: is the buffer connected to the B line(level shifted) of the following DUT
v?wo: is the DUT output, ie gate studied
So v2w2 is the stress input on the op line of the buffer connected to the B line of the DUT
Definition of the logical levels:
vin1: nominal value on the true line of the buffer connected to the A line of DUT
vin2: nominal value on the true line of the buffer connected to the B line of DUT
Definition of the ouput values:
op: voltage on the op line of DUT
opb: voltage on the opb line of DUT
abs(NM): absolute NM
NM: op - opb
diff: remaining NM
NM1: Noise margin at the following buffer after DUT
rank1: rank of the value of abs(NM) (beginning with the lowest value)
rank2: rank of the value of abs(NM) (beginning with the highest value)

Calculated stress: 125mV
Nominal value of voltage applied at the stressing inputs: 1.5V
nb combinations: 108

| Cell GRADE | #of diodes | Resistor Value(KOhms) |
|---|---|---|
| G 0 | 2 | 49.83 |
| G 1 | 2 | 11.5 |
| G 2 | 1 | 28.13 |
| G 3 | 1 | 17.04 |

| | | |
|---|---|---|
| G 4 | 1 | 6.61 |
| G 5 | 1 | 3.23 |
| G 6 | 1 | 1.58 |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 0 0 0 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000000 | -0.254137 | | |
| 2 | 0 0 0 0 0 0 | 3.05 | 3.30 | 3.046746 | 3.296750 | 0.250005 | -0.250005 | 0.003362 | -0.254129 | | |
| 3 | 0 0 0 0 0 0 | 3.30 | 3.05 | 3.043437 | 3.296753 | 0.253315 | -0.253315 | 0.000051 | -0.254137 | | |
| 4 | 0 0 0 0 0 0 | 3.30 | 3.30 | 3.296723 | 3.046773 | 0.249951 | 0.249951 | 0.003416 | 0.254128 | | |
| 5 | 0 0 0 0 0 1 | 3.05 | 3.05 | 3.043322 | 3.148662 | 0.105340 | -0.105340 | 0.148027 | -0.238774 | | |
| 6 | 0 0 0 0 0 1 | 3.05 | 3.30 | 3.046645 | 3.148649 | 0.102004 | -0.102004 | 0.151362 | -0.236842 | 15 | |
| 7 | 0 0 0 0 0 1 | 3.30 | 3.05 | 3.043348 | 3.148641 | 0.105293 | -0.105293 | 0.148073 | -0.238749 | | |
| 8 | 0 0 0 0 0 1 | 3.30 | 3.30 | 3.296723 | 2.937396 | 0.359327 | 0.359327 | -0.105960 | 0.254194 | | |
| 9 | 0 0 0 0 1 0 | 3.05 | 3.05 | 2.934554 | 3.296778 | 0.362224 | -0.362224 | -0.108858 | -0.254194 | | 9 |
| 10 | 0 0 0 0 1 0 | 3.05 | 3.30 | 2.937373 | 3.296750 | 0.359376 | -0.359376 | -0.106010 | -0.254194 | | |
| 11 | 0 0 0 0 1 0 | 3.30 | 3.05 | 2.934575 | 3.296752 | 0.362177 | -0.362177 | -0.108811 | -0.254194 | | 12 |
| 12 | 0 0 0 0 1 0 | 3.30 | 3.30 | 3.148627 | 3.046671 | 0.101955 | 0.101955 | 0.151411 | 0.236812 | 12 | |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 13 | 0 0 0 1 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000000 | -0.254137 | | |
| 14 | 0 0 0 1 0 0 | 3.05 | 3.30 | 3.046756 | 3.296751 | 0.249996 | -0.249996 | 0.003371 | -0.254128 | | |
| 15 | 0 0 0 1 0 0 | 3.30 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000001 | -0.254137 | | |
| 16 | 0 0 0 1 0 0 | 3.30 | 3.30 | 3.289570 | 3.053936 | 0.235635 | 0.235635 | 0.017732 | 0.254075 | | |
| 17 | 0 0 0 1 0 1 | 3.05 | 3.05 | 3.043322 | 3.148662 | 0.105340 | -0.105340 | 0.148027 | -0.238774 | | |
| 18 | 0 0 0 1 0 1 | 3.05 | 3.30 | 3.046654 | 3.148650 | 0.101996 | -0.101996 | 0.151371 | -0.236836 | 13 | |
| 19 | 0 0 0 1 0 1 | 3.30 | 3.05 | 3.043323 | 3.148662 | 0.105339 | -0.105339 | 0.148027 | -0.238774 | | |
| 20 | 0 0 0 1 0 1 | 3.30 | 3.30 | 3.289569 | 2.943452 | 0.346117 | 0.346117 | -0.092750 | 0.254187 | | |
| 21 | 0 0 0 1 1 0 | 3.05 | 3.05 | 2.934553 | 3.296778 | 0.362225 | -0.362225 | -0.108858 | -0.254194 | | 2 |
| 22 | 0 0 0 1 1 0 | 3.05 | 3.30 | 2.937382 | 3.296751 | 0.359369 | -0.359369 | -0.106003 | -0.254194 | | |
| 23 | 0 0 0 1 1 0 | 3.30 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 8 |
| 24 | 0 0 0 1 1 0 | 3.30 | 3.30 | 3.142671 | 3.053743 | 0.088928 | 0.088928 | 0.164438 | 0.226882 | 6 | |
| 25 | 0 0 1 0 0 0 | 3.05 | 3.05 | 3.043605 | 3.296778 | 0.253173 | -0.253173 | 0.000194 | -0.254136 | | |
| 26 | 0 0 1 0 0 0 | 3.05 | 3.30 | 3.046746 | 3.296750 | 0.250004 | -0.250004 | 0.003363 | -0.254128 | | |
| 27 | 0 0 1 0 0 0 | 3.30 | 3.05 | 3.050358 | 3.290025 | 0.239667 | -0.239667 | 0.013699 | -0.254091 | | |
| 28 | 0 0 1 0 0 0 | 3.30 | 3.30 | 3.296750 | 3.046747 | 0.250003 | 0.250003 | 0.003364 | 0.254128 | | |
| 29 | 0 0 1 0 0 1 | 3.05 | 3.05 | 3.043515 | 3.148662 | 0.105147 | -0.105147 | 0.148219 | -0.238668 | | |
| 30 | 0 0 1 0 0 1 | 3.05 | 3.30 | 3.046645 | 3.148649 | 0.102004 | -0.102004 | 0.151363 | -0.236841 | 16 | |
| 31 | 0 0 1 0 0 1 | 3.30 | 3.05 | 3.050218 | 3.143008 | 0.092790 | -0.092790 | 0.160576 | -0.230263 | 10 | |
| 32 | 0 0 1 0 0 1 | 3.30 | 3.30 | 3.296749 | 2.937374 | 0.359375 | 0.359375 | -0.106008 | 0.254194 | | |
| 33 | 0 0 1 0 1 0 | 3.05 | 3.05 | 2.934717 | 3.296777 | 0.362061 | -0.362061 | -0.108694 | -0.254194 | | 14 |
| 34 | 0 0 1 0 1 0 | 3.05 | 3.30 | 2.937374 | 3.296750 | 0.359376 | -0.359376 | -0.106009 | -0.254194 | | |
| 35 | 0 0 1 0 1 0 | 3.30 | 3.05 | 2.940449 | 3.289997 | 0.349547 | -0.349547 | -0.096181 | -0.254188 | | |
| 36 | 0 0 1 0 1 0 | 3.30 | 3.30 | 3.148649 | 3.046646 | 0.102003 | 0.102003 | 0.151363 | 0.236841 | 14 | |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 37 | 0 1 0 0 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000000 | -0.254137 | |
| 38 | 0 1 0 0 0 0 | 3.05 | 3.30 | 3.046718 | 3.296778 | 0.250060 | -0.250060 | 0.003307 | -0.254129 | |
| 39 | 0 1 0 0 0 0 | 3.30 | 3.05 | 3.043437 | 3.296753 | 0.253317 | -0.253317 | 0.000050 | -0.254137 | |
| 40 | 0 1 0 0 0 0 | 3.30 | 3.30 | 3.289368 | 3.054119 | 0.235249 | 0.235249 | 0.018118 | 0.254073 | |
| 41 | 0 1 0 0 0 1 | 3.05 | 3.05 | 3.043322 | 3.148662 | 0.105340 | -0.105340 | 0.148027 | -0.238774 | |
| 42 | 0 1 0 0 0 1 | 3.05 | 3.30 | 3.046618 | 3.148672 | 0.102054 | -0.102054 | 0.151312 | -0.236872 | 20 |
| 43 | 0 1 0 0 0 1 | 3.30 | 3.05 | 3.043347 | 3.148641 | 0.105294 | -0.105294 | 0.148072 | -0.238749 | |
| 44 | 0 1 0 0 0 1 | 3.30 | 3.30 | 3.289335 | 2.943635 | 0.345700 | 0.345700 | -0.092333 | 0.254188 | |
| 45 | 0 1 0 0 1 0 | 3.05 | 3.05 | 2.934554 | 3.296778 | 0.362224 | -0.362224 | -0.108858 | -0.254194 | 7 |
| 46 | 0 1 0 0 1 0 | 3.05 | 3.30 | 2.937350 | 3.296777 | 0.359428 | -0.359428 | -0.106061 | -0.254194 | 16 |
| 47 | 0 1 0 0 1 0 | 3.30 | 3.05 | 2.934575 | 3.296753 | 0.362178 | -0.362178 | -0.108812 | -0.254194 | 10 |
| 48 | 0 1 0 0 1 0 | 3.30 | 3.30 | 3.142504 | 3.053923 | 0.088582 | 0.088582 | 0.164785 | 0.226559 | 2 |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 49 | 0 1 0 1 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000000 | -0.254137 | | |
| 50 | 0 1 0 1 0 0 | 3.05 | 3.30 | 3.046729 | 3.296778 | 0.250049 | -0.250049 | 0.003318 | -0.254128 | | |
| 51 | 0 1 0 1 0 0 | 3.30 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000001 | -0.254137 | | |
| 52 | 0 1 0 1 0 0 | 3.30 | 3.30 | 3.282507 | 3.060991 | 0.221516 | 0.221516 | 0.031850 | 0.253988 | | |
| 53 | 0 1 0 1 0 1 | 3.05 | 3.05 | 3.043322 | 3.148662 | 0.105340 | -0.105340 | 0.148027 | -0.238774 | | |
| 54 | 0 1 0 1 0 1 | 3.05 | 3.30 | 3.046628 | 3.148672 | 0.102044 | -0.102044 | 0.151323 | -0.236866 | 18 | |
| 55 | 0 1 0 1 0 1 | 3.30 | 3.05 | 3.043323 | 3.148662 | 0.105339 | -0.105339 | 0.148027 | -0.238774 | | |
| 56 | 0 1 0 1 0 1 | 3.30 | 3.30 | 3.282474 | 2.949443 | 0.333031 | 0.333031 | -0.079664 | 0.254181 | | |
| 57 | 0 1 0 1 1 0 | 3.05 | 3.05 | 2.934553 | 3.296778 | 0.362225 | -0.362225 | -0.108858 | -0.254194 | | 1 |
| 58 | 0 1 0 1 1 0 | 3.05 | 3.30 | 2.937359 | 3.296777 | 0.359418 | -0.359418 | -0.106052 | -0.254194 | | 19 |
| 59 | 0 1 0 1 1 0 | 3.30 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 6 |
| 60 | 0 1 0 1 1 0 | 3.30 | 3.30 | 3.136815 | 3.060681 | 0.076133 | 0.076133 | 0.177233 | 0.212452 | 1 | |
| 61 | 0 1 1 0 0 0 | 3.05 | 3.05 | 3.043605 | 3.296778 | 0.253174 | -0.253174 | 0.000193 | -0.254136 | | |
| 62 | 0 1 1 0 0 0 | 3.05 | 3.30 | 3.046719 | 3.296778 | 0.250059 | -0.250059 | 0.003308 | -0.254128 | | |
| 63 | 0 1 1 0 0 0 | 3.30 | 3.05 | 3.050218 | 3.290164 | 0.239946 | -0.239946 | 0.013420 | -0.254092 | | |
| 64 | 0 1 1 0 0 0 | 3.30 | 3.30 | 3.289393 | 3.054095 | 0.235299 | 0.235299 | 0.018068 | 0.254073 | | |
| 65 | 0 1 1 0 0 1 | 3.05 | 3.05 | 3.043514 | 3.148663 | 0.105148 | -0.105148 | 0.148218 | -0.238668 | | |
| 66 | 0 1 1 0 0 1 | 3.05 | 3.30 | 3.046618 | 3.148672 | 0.102054 | -0.102054 | 0.151313 | -0.236872 | | |
| 67 | 0 1 1 0 0 1 | 3.30 | 3.05 | 3.050079 | 3.143125 | 0.093046 | -0.093046 | 0.160320 | -0.230472 | 11 | |
| 68 | 0 1 1 0 0 1 | 3.30 | 3.30 | 3.289360 | 2.943614 | 0.345746 | 0.345746 | -0.092379 | 0.254187 | | |
| 69 | 0 1 1 0 1 0 | 3.05 | 3.05 | 2.934717 | 3.296778 | 0.362061 | -0.362061 | -0.108695 | -0.254194 | | 13 |
| 70 | 0 1 1 0 1 0 | 3.05 | 3.30 | 2.937351 | 3.296777 | 0.359427 | -0.359427 | -0.106061 | -0.254194 | | 17 |
| 71 | 0 1 1 0 1 0 | 3.30 | 3.05 | 2.940331 | 3.290137 | 0.349805 | -0.349805 | -0.096439 | -0.254188 | | |
| 72 | 0 1 1 0 1 0 | 3.30 | 3.30 | 3.142525 | 3.053899 | 0.088627 | 0.088627 | 0.164740 | 0.226601 | 4 | |
| 73 | 1 0 0 0 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000001 | -0.254137 | | |
| 74 | 1 0 0 0 0 0 | 3.05 | 3.30 | 3.054092 | 3.289395 | 0.235303 | -0.235303 | 0.018064 | -0.254074 | | |
| 75 | 1 0 0 0 0 0 | 3.30 | 3.05 | 3.043437 | 3.296753 | 0.253315 | -0.253315 | 0.000051 | -0.254137 | | |
| 76 | 1 0 0 0 0 0 | 3.30 | 3.30 | 3.296751 | 3.046745 | 0.250006 | 0.250006 | 0.003361 | 0.254129 | | |
| 77 | 1 0 0 0 0 1 | 3.05 | 3.05 | 3.043323 | 3.148662 | 0.105339 | -0.105339 | 0.148027 | -0.238774 | | |
| 78 | 1 0 0 0 0 1 | 3.05 | 3.30 | 3.053896 | 3.142527 | 0.088630 | -0.088630 | 0.164736 | -0.226604 | 5 | |
| 79 | 1 0 0 0 0 1 | 3.30 | 3.05 | 3.043348 | 3.148641 | 0.105293 | -0.105293 | 0.148073 | -0.238749 | | |
| 80 | 1 0 0 0 0 1 | 3.30 | 3.30 | 3.296751 | 2.937373 | 0.359378 | 0.359378 | -0.106011 | 0.254194 | | 20 |

| Line# | stress_vec | vin1 | vin2 | op | opb | abs(NM) | NM | diff | NM1 | rank1 | rank2 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 81 | 1 0 0 0 1 0 | 3.05 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 5 |
| 82 | 1 0 0 0 1 0 | 3.05 | 3.30 | 2.943612 | 3.289362 | 0.345750 | -0.345750 | -0.092383 | -0.254188 | | |
| 83 | 1 0 0 0 1 0 | 3.30 | 3.05 | 2.934575 | 3.296752 | 0.362177 | -0.362177 | -0.108811 | -0.254194 | | 11 |
| 84 | 1 0 0 0 1 0 | 3.30 | 3.30 | 3.148649 | 3.046644 | 0.102006 | 0.102006 | 0.151361 | 0.236843 | 17 | |
| 85 | 1 0 0 1 0 0 | 3.05 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000000 | -0.254137 | | |
| 86 | 1 0 0 1 0 0 | 3.05 | 3.30 | 3.053779 | 3.289720 | 0.235941 | -0.235941 | 0.017426 | -0.254076 | | |
| 87 | 1 0 0 1 0 0 | 3.30 | 3.05 | 3.043412 | 3.296778 | 0.253366 | -0.253366 | 0.000001 | -0.254137 | | |
| 88 | 1 0 0 1 0 0 | 3.30 | 3.30 | 3.289597 | 3.053909 | 0.235687 | 0.235687 | 0.017679 | 0.254075 | | |
| 89 | 1 0 0 1 0 1 | 3.05 | 3.05 | 3.043322 | 3.148662 | 0.105340 | -0.105340 | 0.148027 | -0.238774 | | |
| 90 | 1 0 0 1 0 1 | 3.05 | 3.30 | 3.053587 | 3.142796 | 0.089209 | -0.089209 | 0.164158 | -0.227141 | 8 | |
| 91 | 1 0 0 1 0 1 | 3.30 | 3.05 | 3.043323 | 3.148662 | 0.105339 | -0.105339 | 0.148027 | -0.238774 | | |
| 92 | 1 0 0 1 0 1 | 3.30 | 3.30 | 3.289596 | 2.943430 | 0.346166 | 0.346166 | -0.092799 | 0.254187 | | |
| 93 | 1 0 0 1 1 0 | 3.05 | 3.05 | 2.934553 | 3.296778 | 0.362224 | -0.362224 | -0.108858 | -0.254194 | | 4 |
| 94 | 1 0 0 1 1 0 | 3.05 | 3.30 | 2.943347 | 3.289687 | 0.346340 | -0.346340 | -0.092973 | -0.254188 | | |
| 95 | 1 0 0 1 1 0 | 3.30 | 3.05 | 2.934554 | 3.296777 | 0.362224 | -0.362224 | -0.108857 | -0.254194 | | 3 |
| 96 | 1 0 0 1 1 0 | 3.30 | 3.30 | 3.142693 | 3.053717 | 0.088976 | 0.088976 | 0.164390 | 0.226927 | 7 | |
| 97 | 1 0 1 0 0 0 | 3.05 | 3.05 | 3.043713 | 3.296669 | 0.252956 | -0.252956 | 0.000411 | -0.254135 | | |
| 98 | 1 0 1 0 0 0 | 3.05 | 3.30 | 3.054095 | 3.289394 | 0.235299 | -0.235299 | 0.018067 | -0.254073 | | |
| 99 | 1 0 1 0 0 0 | 3.30 | 3.05 | 3.050358 | 3.290024 | 0.239666 | -0.239666 | 0.013700 | -0.254091 | | |
| 100 | 1 0 1 0 0 0 | 3.30 | 3.30 | 3.296777 | 3.046719 | 0.250058 | 0.250058 | 0.003308 | 0.254128 | | |
| 101 | 1 0 1 0 0 1 | 3.05 | 3.05 | 3.043622 | 3.148571 | 0.104949 | -0.104949 | 0.148417 | -0.238558 | | |
| 102 | 1 0 1 0 0 1 | 3.05 | 3.30 | 3.053898 | 3.142525 | 0.088627 | -0.088627 | 0.164739 | -0.226601 | 3 | |
| 103 | 1 0 1 0 0 1 | 3.30 | 3.05 | 3.050219 | 3.143008 | 0.092789 | -0.092789 | 0.160577 | -0.230262 | 9 | |
| 104 | 1 0 1 0 0 1 | 3.30 | 3.30 | 3.296777 | 2.937351 | 0.359426 | 0.359426 | -0.106060 | 0.254194 | | 18 |
| 105 | 1 0 1 0 1 0 | 3.05 | 3.05 | 2.934809 | 3.296668 | 0.361858 | -0.361858 | -0.108492 | -0.254193 | | 15 |
| 106 | 1 0 1 0 1 0 | 3.05 | 3.30 | 2.943614 | 3.289361 | 0.345747 | -0.345747 | -0.092380 | -0.254187 | | |
| 107 | 1 0 1 0 1 0 | 3.30 | 3.05 | 2.940450 | 3.289995 | 0.349546 | -0.349546 | -0.096179 | -0.254188 | | |
| 108 | 1 0 1 0 1 0 | 3.30 | 3.30 | 3.148672 | 3.046618 | 0.102053 | 0.102053 | 0.151313 | 0.236871 | 19 | |

# APPENDIX IV

In chapter three, we discussed a two-pass testing technique, called the 'Imbalance Testing Technique'. From table 3.9, certain imbalance patterns lead to stress accumulation in defect-free gates. In this appendix, we show in detail how certain imbalance patterns lead to the accumulation of the applied stress. We also identify certain imbalance patterns that do not lead to the lowest output amplitudes, avoiding worst-case accumulation. A few best and worst ranking patterns were studied to analyse their employability. These patterns were analysed by the 'imbalance analyser' tool, also discussed in chapter three. Some of the imbalance patterns ranked by this tool are studied in detail in this appendix.

Pattern numbers that led to worst-case accumulation were ranked in table 3.9, chapter three. The 'imbalance analyser' tool used just one gate instead of a chain of gates. It is easier to analyse one gate with such imbalance patterns than to apply this imbalance pattern for a chain of gates, as it becomes hard to control the imbalance pattern in a chain of gates. For instance, when the output of the first gate has to be imbalanced on one line - either the actual signal or its complement, the input of the second gate, connected to the output of the first gate, may have to be imbalanced on the opposite line. It is not possible to achieve this unless the input is cross-wired which changes the functionality of the gate.

For example, consider the imbalance pattern "010110" for the AND gate, pattern 60 listed in Appendix III. Bit '1' denotes that a line is imbalanced and a '0' denotes that the

line is not imbalanced, not their logical values. The first two bits denote if 'ab' or 'a' input is imbalanced, the second two bits denote if 'bb' or 'b' input is imbalanced, and the last two bits denote if $V_1$ or $V_2$ line is imbalanced. Note that $V_1$ is on the left hand side of the differential pair and $V_2$ is on the right hand side of the differential pair. Also, note that the bit '1' only indicates that the line is imbalanced, but does not say by how much. However, this information can be found at the beginning of the table.

In the "010110" pattern, 'a', 'b' and $V_1$ lines are stressed. When the 'b-bb' input is sensitised, 'b' is connected to 'op' and 'bb' is connected to 'opb' of the previous gate in the chain. But we know that $V_1$ ('op' line) is imbalanced in all the gates of the chain. But, if 'op' is connected to the 'b' input, then the imbalance pattern is no longer the same as that of the previous one. However, this can still be achieved in the test mode, by cross connecting the wires in the test mode only. But the process is complicated and needs careful handling, for a long chain of gates.

According to the results obtained from the 'imbalance analyser' tool, the same set of eight patterns always gave rise the top eight ranks, varying in order among different speed grades. We aimed at finding out why these combinations of imbalance at the input and the output lead to accumulation. A number of stress patterns were studied to find how the output was affected in the chain.

**Pattern 010110 (Rank #1)**

For all speed grades, the lowest resulting amplitude was always obtained with the same stimulus pattern "010110" for an AND gate. This pattern corresponds to all lines in the gate being imbalanced on the left side of the differential pair. Thus the pattern 010110 for the AND gate denotes that 'a', 'b', and 'op' are stressed while 'ab', 'bb' and 'opb' are normal. Q2 and Q6 conduct when both 'a' and 'b' are high. 'opb' is low and 'op' is high. Also, note that two collectors are connected to the output line at this side and hence the load is high. When 'a', 'b' and $V_1$ are all imbalanced, 'op' and the 'opb' signals are reduced in amplitude. This reduces the remaining noise margin for a logic '1' signal. Thus this pattern leads to the worst-case behaviour.

The first AND gate in the chain was designed to follow this imbalance pattern. Since gates were connected in series, it becomes tedious to follow the same pattern throughout the chain, without flipping the input and the output lines. Therefore the rest of the chain followed "011010" pattern, for ease of connection.

When one diode was employed in the imbalance arm and when the circuit was designed for a remaining noise margin of 110 mV, the circuit exhibited stuck-at behaviour after 20 gates in the chain, as illustrated by the following table. The title of the table gives the speed grade of the gate, the type of the gate studied, the number of diodes used, the value of the resistor in the imbalance arm, and the input to which the toggling signals are

connected. The other input is connected to dc signal. The first column gives the gate number and the second column gives the output (in mV) of each gate in the chain.

**Grade 5 AND chain with toggling input on b – bb; Diodes = 1, $R_2$ = 3.5K**

| Gate no. | V1 = 1.5 Volts, Defect-free chain | Gate no. | V1 = 1.5 Volts, Defect-free chain |
|---|---|---|---|
| Input | 250 | 7 | 97 |
| 0 | 238 | 10 | 92 |
| 1 | 238 | 15 | 85 |
| 2 | 238 | 20 | 78 |
| 3 | 238 | 22 | 70 |
| 4 | 124 | 25 | 20 |
| 5 | 110 | 28 | s-@-f |
| 6 | 103 | 40 | s-@-f |

Signal degradation can be observed with successive gates of the chain. Thus, if this imbalance pattern is used in the test mode, when the gate is already weak due to the applied imbalance, the defect-free chain exhibits stuck-at behaviour. This is an undesirable aspect of testing. Therefore, this imbalance pattern should be avoided.

***Hypothesis:*** From the above discussion, we see that the imbalance applied on each line of the gate by pattern 010110 reinforces signal degradation, leading to the failure of the chain. Since the AND gates are asymmetrical, reversing the stress polarity should not lead to stress accumulation. If we take a bit-wise complement of this pattern and apply it to the AND gate, then this imbalance should be such that the gate is not weakened, and hence the chain should not exhibit stuck-at fault.

**Pattern 101001**

The pattern "101001" is the bit-wise complement of the above pattern, "010110." According to this pattern, all the lines are imbalanced on the right hand side of the differential pair. To verify if this pattern avoids accumulation, the test bench was set-up with the first AND gate in the chain to be imbalanced according to the above pattern. The rest of the chain followed "100101". The results obtained for this pattern is tabulated below. The table holds the same syntax as the previous one.

**Grade 5 AND chain with toggling input at b – bb; Diodes = 1, $R_2$ = 3.5K**

| Gate no. | V2 = 1.5 Volts, Defect-free chain |
|---|---|
| Input | 250 |
| 0 | 238 |
| 1 | 238 |
| 2 | 238 |
| 3 | 238 |
| 4 | 124 |
| 5 | 117 |
| 6 | 115 |
| 7 | 114 |
| 39 | 114 |

The chain does not exhibit stuck-at behaviour for the above pattern. The output of each gate of the chain remains the same. Also, this pattern does not lead to stuck-at behaviour in fault free gates. Hence, this combination can be used in the test mode without causing stress accumulation.

**Pattern 011010 (rank 4)**

Pattern 011010 ranks four in the table. Two lines are imbalanced on the left side of the differential pair, and one line on the right side. The table holds the same syntax as the previous one.

**Grade 5 AND chain with toggling input at b-bb; D = 1, R = 3.5K**

| Gate no. | V1 = 1.5 V Good gate |
|---|---|
| Input | 250 |
| 0 | 238 |
| 1 | 238 |
| 2 | 238 |
| 3 | 238 |
| 4 | 124 |
| a - ab i/p | 178.41 |
| 5 | 110 |
| 6 | 99 |
| 7 | 94 |
| 10 | 86 |
| 15 | 80 |
| 20 | 71 |
| 25 | 33 |
| 26 | s-@-f |

The table clearly illustrates signal degradation with successive gates of the chain. Upon applying this pattern, the signal is degraded to the point where a defect-free chain exhibits stuck-at behaviour. Therefore, it is important to select the right imbalance pattern type.