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Published in:
The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)

DOI (link to publication from Publisher):
10.1049/icp.2021.0989

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Citation for published version (APA):
Niazi, K. A. K., Yang, Y., & Séra, D. (2021). Architecture for Parallel PV Strings using the Switched- Capacitor-Based Differential Power Processing Technique. In *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)* (pp. 603-607) https://doi.org/10.1049/icp.2021.0989

Architecture for Parallel PV Strings using the Switched-Capacitor-Based Differential Power Processing Technique

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Keywords: PHOTOVOLTAIC (PV), MISMATCH, SWITCHED-CAPACITOR, DIFFERENTIAL POWER PROCESSING (DPP), PARALLEL-CONNECTED

Abstract

Mismatch effects are common in photovoltaic (PV) systems, which affect the overall system performance and the PV module life. A mismatch causes an imbalance in the PV module voltages, and therefore, it is not recommended to connect PV modules in parallel due to increased power losses and stresses. To mitigate the effect of mismatch, module-level power electronics converters are considered as an effective solution. Accordingly, this paper introduces a differential power processing (DPP) converter based on switched-capacitors (SCs) for parallel-connected PV strings. The proposed DPP converters are connected across each PV module, which equalizes the PV module voltages. The technique can help to generate more output power regardless of mismatch between PV modules and make the parallelization of PV strings possible. The proposed architecture is analyzed through simulations and compared with parallel-connected PV strings using Schottky diodes.

1 Introduction

Energy production from non-renewable sources like coal and other fossil fuels causes environmental threats. Therefore, the development of clean and green energy is important. The energy yield from renewable sources like solar and wind has significantly increased in the past years [1]. Especially, the solar photovoltaic (PV) energy has grown with the highest rate. It is predicted that the installed capacity will reach up to 600 GWp by 2023 [2, 3].

In the PV system, the output power from PV modules is sensitive to non-ideal conditions such as shadows, dirtiness, and manufacturing tolerances. All these non-idealities cause a power mismatch in the PV system, which affects the overall performance and life of the system. To reduce the mismatch issues, PV modules are preferred to connect them in series instead of parallel because mismatch effects are more severe in parallel, e.g., voltage imbalance between the PV strings.

Mismatch in PV strings is severe and causes power losses. The mismatch characteristics in PV modules vary with the irradiance level. During mismatch, the shaded PV modules generate lesser currents than the un-shaded PV modules. Therefore, an extra current from the un-shaded PV modules flows through a bypass diode connected in parallel with the other series-connected shaded PV modules, as demonstrated in Fig. 1. In Fig. 1, a mismatch occurs in a PV module comprising of three PV submodules (*SM1*, *SM2*, and *SM3*), where D_1, D_2, and D_3 are the bypass diodes connected across *SM1*, *SM2*, and *SM3*, respectively. The mismatch issue can further be explained as follows. In no shade conditions, bypass diodes remain *OFF* and the same current I_m flows from all submodules, as shown in Fig. 1(b). During shading, there is a significant decrease in the power generation of the entire PV string, because the shaded PV submodule is bypassed by a bypass diode, as shown in Fig. 1(c) [4]. The shaded PV submodule has no power contribution due to the conduction of the bypass diode. According to the latest research, partial shading on 10% of the area of a PV string installed on a residential rooftop causes a reduction of annual energy yield up to 20%-30% [5]. In addition, multiple maximum power points (MPPs) that consist of local MPP(s) and a global MPP (GMPP) appear in the power-voltage (*P-V*) characteristics of PV strings under partial shading or mismatch, as shown in Fig. 2(a). In this situation, the conventional MPP tracking (MPPT) algorithms may malfunction and the string works at a local MPP instead of operating at the GMPP [6].

To solve mismatch issues, power electronic techniques have been proposed. The differential power processing (DPP) converters [7–12] are proven effective to mitigate the mismatch issues. DPP converters are used to process the

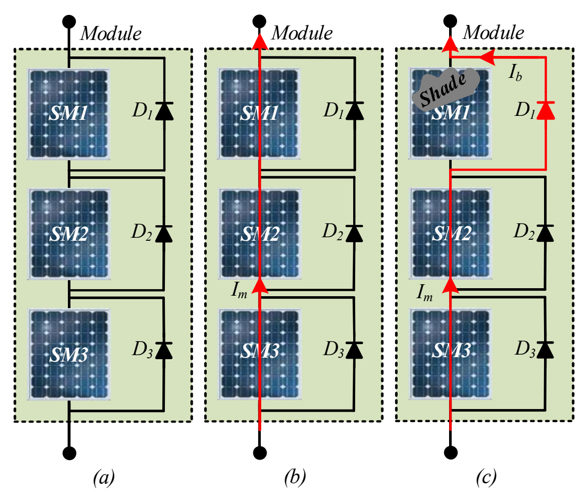

Fig. 1. A PV module with three series-connected submodules (*SM1*, *SM2*, and *SM3*): (a) general representation, (b) there is no mismatach, and (c) *SM1* is shaded. Here, D_1, D_2, and D_3 are the bypassing diodes connected in parallel to *SM1*, *SM2*, and *SM3*, respectively, I_m and I_b are the submodule and bypassing currents, respectively.

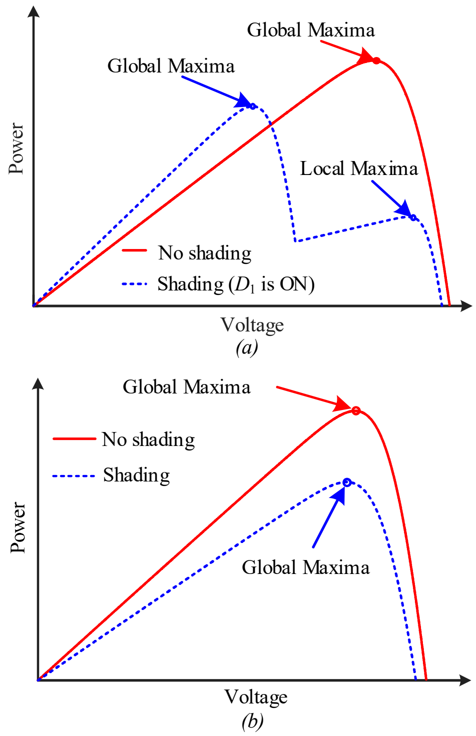

Fig. 2. Power-Voltage (*P-V*) characteristics of PV modules during mismatch and no mismatch: (a) traditional bypass diode technique and (b) parallel-connected DPP converter.

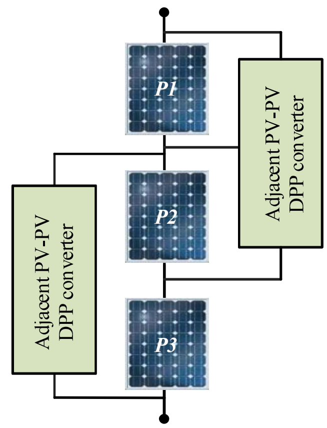

Fig. 3. General structure of mismatch mitigation with the module-to-module (PV-PV) DPP converter.

mismatched power between the adjacent PV module instead of processing the full power. In addition, the PV module characteristics are virtually unified by the charge distribution through the DPP converter. Therefore, local MPPs disappear, and only there is a GMPP, as shown in Fig. 2(b). Therefore, the power yield by using DPP converters is dramatically increased. In all, the DPP converters can extract the maximum power, leading to easy power tracking algorithms, and they significantly enhance the power yield in comparison to the bypass diodes. Despite the increase in power yield under partial shading conditions, DPP converters require more switches with complicated control circuitry, which increases the system complexity along with the system cost [13, 14].

Nevertheless, more power electronics are integrated into PV modules due to its considerable improvements over existing solutions in terms of efficiency, reliability, and cost. The structure of a PV-PV-based DPP converter is shown in Fig. 3. In DPP systems, the common power between the PV modules is directly processed by the central converter. However, the mismatch or differential power is only processed by the DPP converters between series-connected PV modules. As the mismatched power is just a small fraction of the overall power. Therefore, the system can achieve high efficiency with a small size and low power rating components [15].

In this paper, a switched-capacitor (SC)-based DPP methodology is thus adopted for parallel-connected PV strings. The proposed architecture is compared with the conventional parallel-string structure, where the modules are connected in parallel with bypass diodes. The rest of this paper is organized as follows. Firstly, the proposed methodology is explained in Section 2. In Section 3, a loss analysis is presented. Simulations are provided to verify the analysis and discussion in Section 4. In the end, the conclusion is presented in Section 5.

2. Proposed solution

The proposed methodology uses the concept of voltage equalization, which was employed in series-connected batteries [16]. In this paper, this concept is used for the parallel-connected PV strings at a module-level. During this work, mismatched power between PV modules (*P1* and *P2*) are processed through the capacitor *C*, as shown in Fig. 4. The transfer of energy depends on the severity of the mismatch. The operational principle of the SC-based DPP converter is explained in [17]. During mismatch, *P1* is producing less power. Firstly, S_2 and S_4 are turned *ON*, which allows the charging of *C*, as shown in Fig. 4(b). Similarly, in the next duty cycle, S_1 and S_3 are turned *ON*, while S_2 and S_4 are turned OFF, which can be seen from Fig. 4(c). During this operation, charges stored in capacitor *C* start to redistribute and the operation continues. Both transistors S_2 and S_4 operate together and alternatively to S_1 and S_3 with a duty cycle of 50%. Therefore, the voltage across the capacitor rises in one cycle and falls in the other.

To extend the SC topology for parallel-connected PV strings, capacitors (C_1 and C_2) are switched continuously between the PV modules (*P1*, *P2*, *P3*, and *P4*), as shown in Fig. 5(a). For this purpose, C_1 switched between *P1* and *P2*, while C_2 is between *P3* and *P4*. Transistors $S_{1\text{-}4}$ are used for the continuous switching of C_1 between *P1* and *P2*. Similarly, $S_{11\text{-}44}$ transistors are used for the continuous switching of C_2. Transistors $S_{1,\,3}$ and $S_{11,\,33}$ switched together and alternatively to transistors $S_{2,\,4}$ and $S_{22,\,44}$. These switches are operated with a duty cycle of 50% (for equal distribution of charges between PV modules during mismatching) at a high frequency for better charge distribution and lower capacitor losses. The proposed methodology in Fig. 5(a) makes it possible to achieve the same voltages for all PV modules in a system. Due to the same voltages, the *P-V* characteristics for the proposed methodology appear with one power peak, as demonstrated in Fig. 2(b). Therefore, voltage equalization is achieved for parallel-

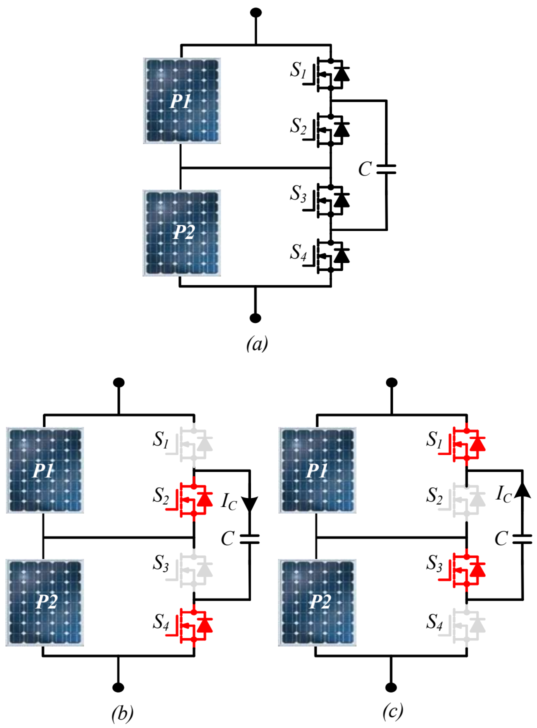

Fig. 4. General diagram for the switched-capacitor (SC)-based DPP converter containing two series-connected PV modules *P1* and *P2* [18]: (a) no shading, (b) mismatch situation, S_1, S_3 are in OFF-state and S_2, S_4 are ON-state, and (c) mismatch situation, S_1, S_3 are in ON-state and S_2, S_4 are OFF-state. Here, C is the charge distribution capacitor during mismatch.

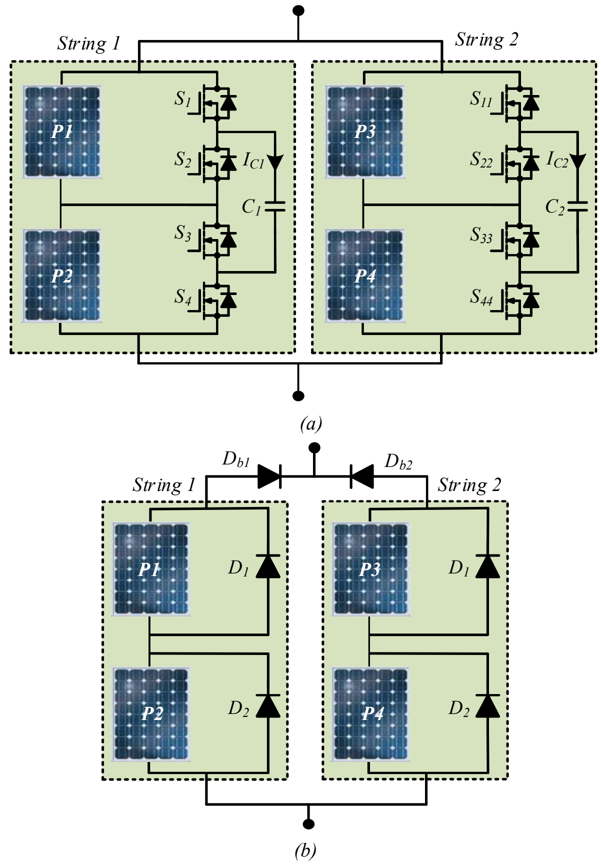

Fig. 5. Two parallel-connected PV strings (*string 1* and *string 2*) each containing two PV modules (*P1*, *P2*, *P3*, and *P4*) with: (a) switched-capacitor (SC)-based differential power processing (DPP) topology and (b) traditional bypass diode (D_1, D_2, D_3, and D_4) topology. Here, D_{b1} and D_{b2} are the blocking diodes for the *string 1* and *string 2*, respectively.

connected PV modules. Hence, the proposed methodology eliminates the voltage unbalance problem in the parallel-connected PV strings.

3 Power loss analysis

The power losses are briefly calculated for the proposed methodology. The main power losses in the proposed methodology consist of switching losses, conduction losses, losses in energy storage devices, and leakage losses [18]. Leakage losses are not taken into account. On the other hand, the performance has been evaluated from the rest of the losses. Initially, the ON-state power losses (P_{on}) can be found as

$$P_{on} = 2\sum_{i=1}^{2} I_{Ci}^2 R_{on} \tag{1}$$

where R_{on} is the ON-state resistance of the MOSFETs, I_{Ci} is the mismatch current passing through the switches, and i can be 1 or 2, which depends on the string. The ON-state losses are multiplied by a factor of 2 because two MOSFETs are *ON* in each cycle.

The capacitor size decreases by increasing the switching frequency f_{sw}. However, switching losses increase with f_{sw}. At any switching instance, two switches are involved for each parallel-connected string, switching power losses (P_{sw}) can be estimated as

$$P_{sw} = 2\sum_{i=1}^{2} V_{DS}\left[I_{Ci(tson)} \times t_{on} + I_{Ci(tsoff)} \times t_{off}\right] f_{sw} \tag{2}$$

where $I_{Ci(tson)}$ is the turn-ON current and $I_{Ci(tsoff)}$ is the turn-OFF current during the rise t_{on} and t_{off} fall time of the switch, respectively.

In Fig. 5(a), I_{Ci} is flowing through C_i. Hence, the power losses (P_{Closs}) for the capacitors can be found by

$$P_{Closs} = \sum_{i=1}^{2} I_{Ci}^2 R_C\left(f_{sw}\right) \tag{3}$$

where $R_{C(fsw)}$ is the effective series resistance of C_i at f_{sw}. The capacitors are designed large enough for better charge distribution during mismatch and reduce the $R_{C(fsw)}$, which comes in series.

The overall power losses can be found by adding (1)-(3), which appears as

$$P_t = 2P_{on} + 2P_{sw} + P_{Closs} \tag{4}$$

where P_t is the total power loss.

The loss estimation for the proposed SC-based DPP methodology for parallel-connected PV strings in Fig. 5(a) can be achieved by using (1)-(4).

Table 1 Ratings of the PV module under test

Parameter	Value
Rated Maximum Power (P_{max})	60 W
Voltage at maximum power (V_{mp})	17.10 V
Current at maximum power (I_{mp})	3.50 A
Open-Circuit Voltage (V_{oc})	21.10 V
Short-Circuit Current (I_{sc})	3.80 A

Table 2 Partial shading cases for the architectures shown in Fig. 4

Irradiance (W/m^2)	Case 1	Case 2	Case 3	Case 4	Case 5
E_1	500	500	1000	500	500
E_2	1000	500	500	500	500
E_3	1000	1000	500	500	500
E_4	1000	1000	1000	1000	500

4 Simulation Results

Simulations are performed to assess the performance of the proposed methodology in PSIM for different mismatch cases. For this purpose, two PV strings consisting of two series-connected PV modules per string are connected in parallel, as revealed in Fig. 5. The proposed SC-based DPP architecture is shown in Fig. 5(a). It consists of eight MOSFET switches ($S_{1\text{-}8}$) and the capacitors (C_1 and C_2) for charge distribution. This proposed architecture is compared with the traditional bypass diode methodology, which is shown in Fig. 5(b). For simulations, the forward conduction voltages are set at 0.5 V for bypass diodes and capacitors at 50 µF. The MOSFETs are operated at the frequency of 100 kHz at a 50% duty cycle to minimize the effective series resistance of capacitors. The PV module parameters are given in Table 1.

Five mismatch cases (i.e., Case 1-5) are developed to evaluate techniques in Fig. 5 by varying the irradiances ($E_{1\text{-}4}$) over the PV modules. E_1, E_2, E_3, and E_4 are the irradiances over *P1*, *P2*, *P3*, and *P4*, respectively. Mismatch cases are given in Table 2. In these cases, the irradiance level is varied to generate the mismatch effect. The simulation results under these cases are presented in Fig. 6. In Fig. 6(a), the output power from the proposed architecture is higher than the traditional bypass diode architecture. During mismatch Case 1, the output power is 209 W for the SC-based DPP topology and 183 W for the traditional bypass diode. Overall, the results in Fig. 6(a) shows the maximization of power yield by using the proposed methodology as compared to the modules with parallel-connected bypass diodes. In addition, Fig. 6(b) shows the *P-V* characteristics for the proposed DPP architecture. It can be seen from Fig. 6(b), the proposed DPP technique has only a GMPP instead of local maxima's. Hence, the proposed architecture can use the traditional MPPT algorithm to extract the maximum power out of the system.

Besides, the power loss distribution across each component in the proposed SC-based DPP methodology is shown in Fig. 7. For loss calculation R_{on} is 16.5 mΩ, R_c is 1 mΩ, t_{on} is 137 ns, and t_{off} is 40 ns. These losses are calculated for Case 3 given in Table 2. It can be seen from Fig. 7, the ON-state power losses

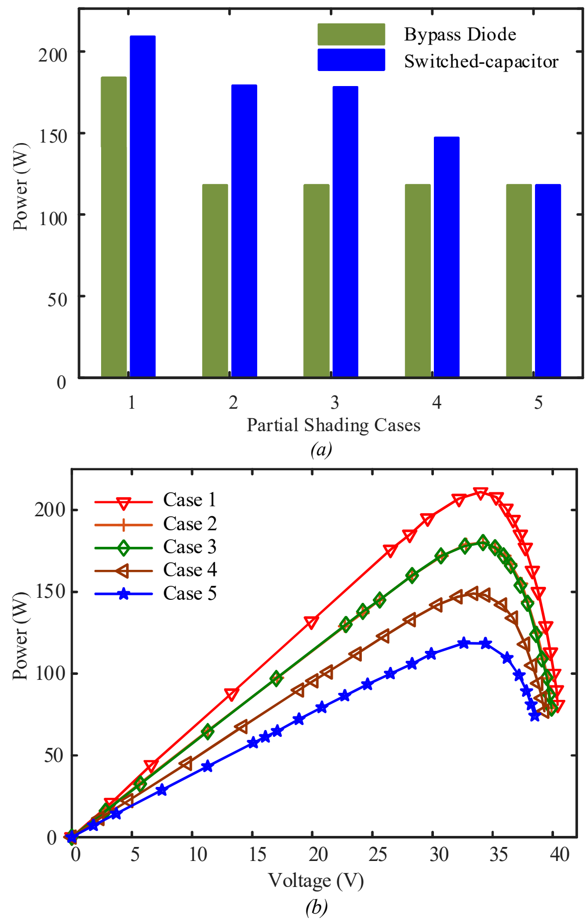

Fig. 6. Simulated results: (a) output power of the modules with traditional (Schottky diode) and proposed mismatch mitigation technique and (b) power-voltage (*P-V*) curves for the proposed architecture for the cases defined in Table 2.

are the maximum, i.e., 63.40%. However, the switching and capacitor losses are 34.70% and 1.9%, respectively.

The proposed SC-based DPP methodology can help to achieve the identical voltage across each PV module in the system shown in Fig. 5(a) during mismatch. The PV module voltages are shown in Fig. 8 for the mismatch Case 1 given in Table 2. It can be seen from Figs. 8(a), the voltages across the PV modules are almost similar for the DPP methodology. However, the voltages are different for traditional bypass diode methodology, as shown in Fig. 8(b). Therefore, the proposed methodology makes it possible to avoid the parallelization problems in the PV system. This work discussed in this paper is specifically for the applications, which require low power and high current, e.g., battery charging and other small rooftop setups. The presence of multiple paths for the power flow makes the system more reliable. Moreover, the DPP supports each PV module in a string to work at its MPP or near it. Hence, it makes the parallel connection possible. The size of the proposed DPP-based architecture is small due to the presence of four switches per topology. Therefore, it is possible to integrate it into a PV module junction box. In addition, the cost of the overall system becomes high due to the presence of more components, which is a major concern to substitute the bypass diode architecture.

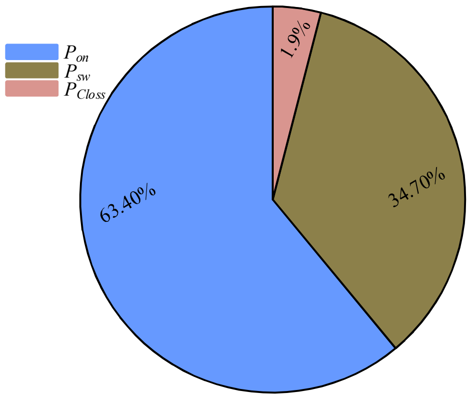

Fig. 7. Power loss distribution among various components in the proposed SC-based DPP methadology when one of the PV modules is half-shaded from each parallel connected PV string in Fig. 5(a).

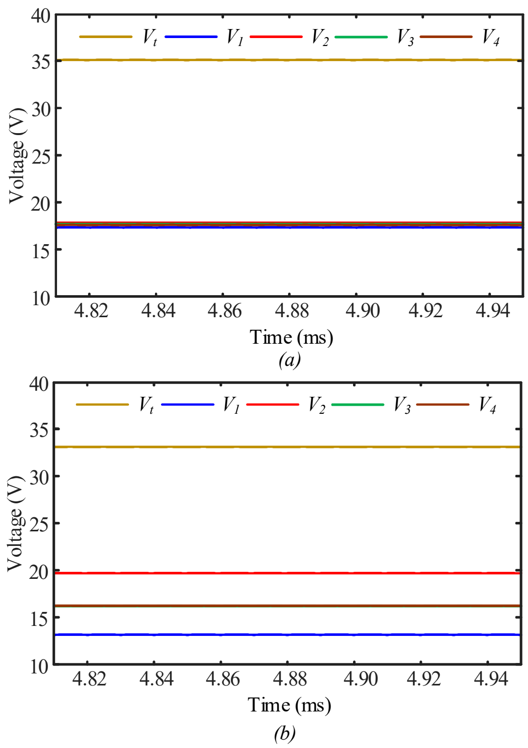

Fig. 8. Voltages across PV modules for the mismatch Case 1 mentioned in Table 2: (a) proposed SC-based DPP methodology and (b) traditional bypass diode methodology. Here, V_1, V_2, V_3, and V_4 are the voltages across *P1*, *P2*, *P3*, and *P4*, respectively.

However, they are reasonable in comparison to other power electronic-based available solutions, e.g., DC optimizers, which process the full power. In all, they are valuable because of higher power outputs along with with better system performance by processing only the mismatch power.

5 Conclusion

In this work, a switched-capacitor-based DPP architecture has been proposed for parallel-connected PV strings subjecting to mismatch. The proposed methodology allows each PV module in the system to operate at or near the maximum power point. In addition, the voltage across each PV module in a parallel-connected PV string has almost similar values, which helps to eliminate the voltage balancing issues in the parallel connections. The performance significance of the proposed concept is achieved by comparing it with the traditional bypass diode technique. The results have shown that the proposed architecture yields more power. Besides, this concept can also be applied to a sub-module level to further investigate the performance and lifetime of PV modules.

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