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An Improved Submodule Capacitor Voltage Measuring Algorithm for MMC with Reduced Sensors

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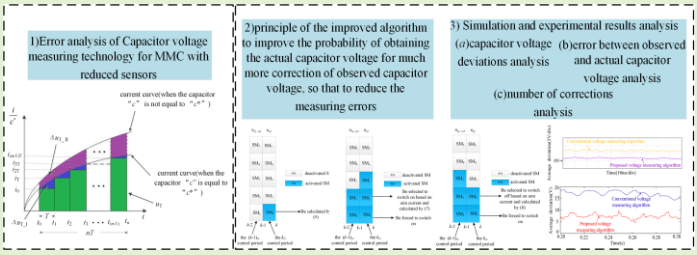
***Abstract*— The nearest level modulation (NLM) based submodule capacitor voltage measuring technology for a modular multilevel converter (MMC) with reduced sensors can effectively reduce the costs of the data acquisition system of MMC and simplify the operation system. One of the technical challenges of this submodule capacitor voltage measuring technology is to reduce the measurement errors of submodule capacitor voltage. This paper proposes an improved submodule capacitor voltage measuring algorithm to overcome this challenge. In the proposed algorithm, by keeping the operation states of submodules unchanged during the continuous control period, the probability of obtaining the actual capacitor voltage is increased, and then the number of corrections of observed capacitor voltage is significantly increased. Thus, the proposed algorithm can effectively reduce the measuring errors. More significantly, the proposed algorithm can also improve the measurement accuracy even in the capacitance deviation situation. Finally, both simulation and experimental results are provided to verify the feasibility and effectiveness of the proposed voltage measuring algorithm.**



***Index Terms*—MMC, submodule capacitor voltage measurement, reduced sensors, measurement errors reduction**

I. Introduction

MODULAR multilevel converter (MMC) adopts the form of cascading connection of distributed submodules (SMs), which has advantages of high output voltage level, low device stress, good output voltage waveform, and the elimination of cumbersome power frequency transformers and filters [1-2]. It has received extensive attention in the fields of flexible ac transmission systems [3] and high-voltage direct current (HVDC) systems [4]. To accommodate high voltage grades in HVDC, it normally requires a large amount of SMs. For example, the Trans Bay Cable Project has more than 200 SMs for each arm-bridge [5]. As the distributed SM cascade structure with an energy storage capacitor is adopted in MMC, the capacitor voltage of the SM needs to be controlled to ensure the voltage balance of each SM [6]. Currently, most of the voltage balancing methods are based on the sampling of the capacitor voltage of each SM with a voltage sensor, which needs a lot of voltage sensors. Thus, it not only increases the costs of the data acquisition system but also complicates the implementation of MMC.

Consequently, to reduce the burden of data acquisition and the implementation complexity of MMC, many studies have been conducted, in which the proposed strategies can be mainly classified into the following two categories.

1） Adopting advanced modulation, unique control structure, or advanced observer to reduce the data processing burden and complexity [7-11,14-15,19].

2） Using modulation-based strategies to reduce the number of voltage sensors or remove sensors [12-13,16-17,20-22].

Various control structures are adopted to reduce the processing time and the data transmission burden at the implementation level, such as disturbed control [7], hierarchical control [8], closed-loop voltage balance control [9], pulse rotation technique [11], and simplified nearest level control [19]. Several advanced observer-based strategies, such as adaptive observers [10,14] and discrete-time sliding-mode observer [15], are also used for the reduction of communication complexity. However, these strategies don't reduce the number of capacitor voltage sensors.

In order to reduce the number of capacitor voltage sensors or even eliminate the adoption of capacitor voltage sensors, several strategies based on advanced carrier-based modulation techniques are proposed, such as the phase disposition (PD) modulation technique combined with fixed switching pattern

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[12], hierarchical permutation cyclic coding [13], phase-disposition PWM based capacitor voltage periodic update algorithm [16], and adaptive linear neuron algorithm [17]. Strategies proposed in [12-13] eliminate the adoption of capacitor voltage sensors, while the stability of MMC is compromised due to the open-loop operation. The technology presented in [16] reduces the number of capacitor voltage sensors by adopting a predictor model to observe capacitor voltages and uses the periodic update algorithm to obtain an actual value of capacitor voltage, while the bandwidth of the voltage sensors and their voltage isolation needs to be higher because of the adoption of pulse-width modulation. The strategy in [17] also reduces the adoption of capacitor voltage sensors, while this method requires accurate measurements of arm inductor voltages.

As the MMC usually consists of a large number of SMs when applied for the HVDC system, the nearest level modulation (NLM) is considered as a more suitable modulation strategy for the MMC applied for the HVDC system than the carrier-based modulation [18] because of its advantage of smaller switching loss and simpler control system. Some studies have been conducted about NLM-based methods to reduce or eliminate the capacitor voltage measurement [20-22].

In [20], a predictive sorting algorithm is proposed to manage the charge and discharge of capacitors. The capacitor voltage measurement can be eliminated, but there will occur a divergence of SM capacitor voltages due to the difference between the predicted and the actual voltage values. In [21], a modified square wave NLM method is proposed to eliminate the capacitor voltage measurement, but the stability may not be guaranteed due to the open-loop operation. In [22], a SM capacitor voltage measuring technique based on NLM and observation is proposed to reduce voltage sensors, and a compensation method is proposed for the delay of the actual sampling circuit. However, the equivalent model of the actual sampling circuit has a strong dependence on the parameters, which leads to poor robustness, and the implementation of this method is relatively complex. With the reduction of the amount of SM voltage sensors in the MMC, the cost and complexity of the MMC data acquisition stages can be decreased. However, designing an algorithm to decrease the voltage measurement errors becomes a challenge[23] and the measurement error reduction in NLM-based SM capacitor voltage measuring technology of MMC with reduced voltage sensors is few.

Therefore, for the NLM-based SM capacitor voltage measuring technology of MMC with reduced voltage sensors, this paper proposes an improved SM capacitor voltage measuring algorithm to improve the measurement accuracy of SM capacitor voltages. The principle of the proposed algorithm is illustrated, and the proposed algorithm is compared with the conventional NLM-based algorithm in detail to show its merits. Finally, the effectiveness of the proposed algorithm is verified in both simulation and an established MMC experimental test bench.

This paper is organized as follows. The basic principle of NLM-based capacitor voltage measuring technology for MMC with reduced sensors is presented in Section II. In Section III, the proposed voltage measuring algorithm is analyzed and compared with the conventional algorithm in detail. Simulation and experiment results are given in Section IV and Section V, respectively. Finally, the main contributions of this paper are summarized in Section VI.

II. Basic Principle of NLM-Based Voltage Measuring Technology for MMC with Reduced Sensors

A. The basic principle of NLM-based capacitor voltage measuring technology for MMC with reduced sensors

The general topology of one phase leg of MMC with reduced sensors is shown in Fig.1.

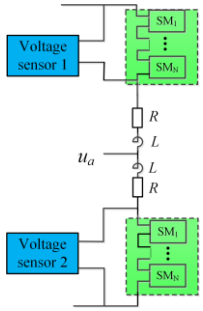


Fig. 1. The general topology of one phase leg of MMC with reduced sensors.

In Fig. 1, the SMs in one arm are divided into several groups (or even one group), and each group is equipped with one voltage sensor. Based on the NLM and the configuration in Fig. 1, the voltage of each SM can be obtained by direct measurements and observation, which is analyzed as follows.

The output of the voltage sensor at the k_{th} control period equals the sum of voltages of all SMs in on-state in the group.

$$u_{kT} = \sum_{i=1}^{N} s(i)_{(k-1)} u_c(i)_{kT} \tag{1}$$

Where kT is the k_{th} control period, $u_c(i)$ is the voltage of the i_{th} SM, and $s(i)_{(k-1)}$ is the state of the i_{th} SM at the k_{th} control period. When the i_{th} SM is in on-state, $s(i)$=1; otherwise $s(i)$=0.

At the $(k\text{-}1)_{th}$ control period, the measured value from the sensor is:

$$u_{(k\text{-}1)T} = \sum_{i=1}^{N} s(i)_{(k-2)} u_c(i)_{(k\text{-}1)T} \tag{2}$$

According to the V-I characteristic of capacitors, the voltage of SM at the beginning of the k_{th} control period can be expressed by,

$$u_c(i)_{kT} = u_c(i)_{(k-1)T} + \frac{1}{c}\int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T} dt \tag{3}$$

Where c is the capacitance and $i_{(k-1)T}$ is the arm current at the $(k\text{-}1)_{th}$ control period.

Substituting (3) into (1), it can be obtained,

$$u_{kT} = \sum_{i=1}^{N} s(i)_{(k-1)} \left[u_c(i)_{(k-1)T} + \frac{1}{c}\int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T} dt \right] \tag{4}$$

Supposing Δu_k is the difference between the measured values at the k_{th} and $(k\text{-}1)_{th}$ control period, which is expressed by,

$$\Delta u_k = u_{kT} - u_{(k-1)T} \tag{5}$$

Substituting (2) and (4) into (5), it can be obtained,

$$\Delta u_k = \sum_{i=1}^{N} s(i)_{(k-1)} u_c(i)_{(k-1)T} - \sum_{i=1}^{N} s(i)_{(k-2)} u_c(i)_{(k-1)T} + \frac{1}{c}\sum_{i=1}^{N} s(i)_{(k-1)} \int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T} dt \quad (6)$$

Based on the charging or discharging state of the capacitor, the simplification of equation (6) is discussed below.

State 1: if only the i_{th} SM has its state changed at the k_{th} control period and the state changes from an off-state to an on-state, the voltage of the i_{th} SM can be expressed by,

$$u_c(i)_{kT} = \Delta u_k - \frac{1}{c}\sum_{i=1}^{N} \int_{(k-1)T}^{kT} s(i)_{(k-2)} i_{(k-1)T} dt \quad (7)$$

State 2: if only the i_{th} SM has its state changed at the k_{th} control period and the state changes from an on-state to an off-state, the voltage of the i_{th} SM can be expressed by,

$$u_c(i)_{kT} = -\Delta u_k + \frac{1}{c}\sum_{i=1}^{N} \int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)} dt \quad (8)$$

State 3: if only the i_{th} SM is switched on at the k_{th} control period, the measured value is the actual voltage of the i_{th} SM. Its voltage can be expressed by,

$$u_c(i)_{kT} = u_{kT} \quad (9)$$

In other states, the voltages of SMs are obtained through an observer.

Given the state of the i_{th} SM $s(i)_{(k-1)}$ and the arm current $i_{(k-1)T}$, the capacitor voltage is normally obtained[24] by,

$$\tilde{u}_c(i)_{kT} = \tilde{u}_c(i)_{(k-1)T} + \frac{1}{c^*} \int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T} dt \quad (10)$$

where the superscript "~" denotes the observed values, c^* is the rated capacitance value.

Therefore, the capacitor voltage of SM is mostly obtained by the observer and probabilistically obtained by direct measurement when the operating conditions of SMs meet the above states 1-3. Following this estimation, SM voltage balancing is performed utilizing the estimated SM voltages and directly measured SM voltages with a conventional sorting algorithm[25].

B. Analysis of submodule capacitor voltage measuring errors

Assuming the i_{th} SM is in the on-state for n consecutive cycles starting from the k_{th} control cycle and its actual voltage has not been directly measured, the capacitor voltage of the i_{th} SM is normally obtained according to (10):

$$\tilde{u}_c(i)_{(k+n)T} = \tilde{u}_c(i)_{(k-1)T} + \frac{1}{c^*}\sum_{i=1}^{n} i_{(i+k-2)T} T \quad (11)$$

However, the real voltage value of the SM after n control periods is,

$$u_c(i)_{(k+n)T} = u_c(i)_{(k-1)T} + \frac{1}{c}\int_{(k-1)T}^{(k-1+n)T} i dt \quad (12)$$

where $u_c(i)_{(k-1)T}$ denotes the real value of the SM voltage measured in the $(k\text{-}1)_{th}$ control period, c is the actual capacitance value

If the real voltage value of the SM is directly measured at the $(k\text{-}1)_{th}$ control period or the observed value of the SM is corrected at the $(k\text{-}1)_{th}$ control period, then,

$$\tilde{u}_c(i)_{(k-1)T} = u_c(i)_{(k-1)T} \quad (13)$$

Comparing the second term of (11) and (12), it can be observed that the measuring errors come from two aspects, including the cumulative error caused by the observer discretization and the error caused by the capacitance deviation. Fig. 2 shows these two kinds of errors. Take t_0 to t_1 as an example for explanation. Firstly, if there is no capacitance deviation (i.e. the actual submodule capacitance "c" is equal to the rated capacitance "c*"), the observer discretization will cause a cumulative error(Δu_{T_I}) as highlighted by the blue color in Fig. 2. However, there exists the capacitance deviation in the practical applications (i.e. the actual submodule capacitance "c" is not equal to the rated capacitance "c*"). This capacitance deviation will cause another kind of error (Δu_{T_II}) as highlighted by the purple color in Fig. 2. With the increase of operation time, the errors generated by the observer dispersion and capacitance offset will accumulate, thereby making the total error larger, corresponding to the sum of all the blue and purple squares in Fig.2.

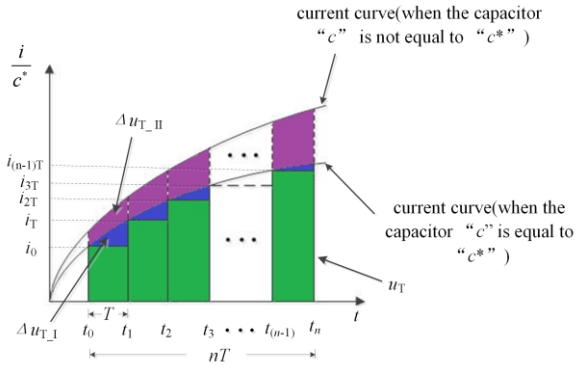


Fig. 2. Diagram of measuring errors caused by observation.
Note: The areas with green color represent the value of SM capacitor voltage obtained by the observer discretization according to equation (11); the areas with blue color are cumulative errors; the areas with purple color are errors caused by capacitance deviation.

III. Conventional and Proposed Voltage Measuring Algorithm for MMC with Reduced Sensors

Just as the real-time correction of the control object in the closed-loop control system, the obtained actual value of SM capacitor voltages based on direct measurable states 1-3 can be used to correct the SM capacitor voltage from the observer to reduce the measurement errors[26-27]. It is obvious that the more correction times the observed capacitor voltage is corrected by the actual capacitor voltage obtained by direct measurement, the higher the accuracy of the capacitor voltage measurement (If the actual value of the SM capacitor voltage can always be obtained in real-time, the operation effect of the MMC with reduced sensors will achieve the operation effect of the MMC with each SM connected to a sensor).

A. Conventional NLM-based voltage measuring algorithm of MMC with reduced sensors

The conventional NLM-based measuring algorithm adopts the natural sorting algorithm, which leads to a low likelihood of direct measurement, a small number of correction times, and a considerable measurement error in MMC with reduced sensors. Taking the upper bridge arm of phase A as an example. Supposing all SMs are put into operation, based on the principle of conventional NLM-based algorithm, the relationship between the direct measurement times for SM capacitor voltages and the state of SMs is shown in table I (when the submodule is selected for charging).

TABLE I
RELATIONSHIP BETWEEN THE TIMES OF DIRECT MEASUREMENT FOR SM CAPACITOR VOLTAGES AND THE STATE OF SMS

The number and the state change of on-state SMs	0 to 1	1 to 2	…	(N-2) to (N-1)	(N-1) to N
The times of direct measurement for SM capacitor voltages	1	$\frac{N-1}{C_N^2}\times 1$	…	$\frac{2}{C_N^{N-1}}\times 1$	1

The sum of the direct measurement times n_{sum} can be expressed as,

$$n_{sum}=1+\frac{N-1}{C_N^2}\times 1+\cdots+\frac{2}{C_N^{N-1}}\times 1+1 \tag{14}$$

Approximating (14) by excluding the first and the last two items in (14), the combinations can be expressed as,

$$\frac{N-2}{C_N^3}\times 1\le\frac{2}{N},\cdots,\frac{3}{C_N^{N-2}}\times 1\le\frac{2}{N} \tag{15}$$

Substituting (15) into (14) n_{sum} can be expressed by,

$$n_{sum}\le 2+\frac{2}{N}\times(N-2) \tag{16}$$

Usually, the number of SMs on a bridge arm is large, so $N\approx N-2$. Formula (16) can be further expressed by,

$$2\le n_{sum}\le 4 \tag{17}$$

Given the symmetry of the bridge arm current direction, when the SM is selected for discharging, the sum of direct measurement times is equal to n_{sum}. The sum of direct measurement times in one power frequency cycle includes the number of direct measurements during SM charging progress and discharge progress, which thus can be expressed by,

$$N_{sum}=2n_{sum} \tag{18}$$

Substituting (17) into (18) N_{sum} can also be expressed by,

$$4\le N_{sum}\le 8 \tag{19}$$

Based on the above analysis, it can be obtained that there is a small probability of direct measurement and a few corrections when adopting the conventional NLM algorithm in the MMC with reduced sensors. In addition, as time increases, the observation errors will become large, especially considering the capacitance deviation, which will reduce the stability of the MMC operation. Therefore, the number of corrections (i.e., the number of direct measurements) may need to be increased to reduce observation errors.

B. Proposed voltage measuring algorithm for MMC with reduced sensors

The proposed algorithm aims to increase the probability of direct measurement for improving the measuring accuracy.

To simplify the following illustration of the proposed algorithm, it is assumed that the bridge arm has only five SMs, and SM_1, SM_2 are in the on-state during the $(k\text{-}1)_{th}$ control period. If the number of the on-state SMs increases at the k_{th} control period, i.e., the number of SMs in the on-state becomes three at the k_{th} control period. There will be ten possibilities of having three SMs in the on-state under the conventional algorithm, as shown in Table II.

TABLE II
POSSIBILITIES OF THE THREE SMS IN THE ON STATE

Possibilities	SMs in the on-state	Possibilities	SMs in the on-state
Possibility1	SM_1,SM_2,SM_3	Possibility6	SM_1,SM_4,SM_5
Possibility2	SM_1,SM_2,SM_4	Possibility7	SM_2,SM_3,SM_4
Possibility3	SM_1,SM_2,SM_5	Possibility8	SM_2,SM_3,SM_5
Possibility4	SM_1,SM_3,SM_4	Possibility9	SM_2,SM_4,SM_5
Possibility5	SM_1,SM_3,SM_5	Possibility10	SM_3,SM_4,SM_5

However, the direct measurement can occur only under possibility1, possibility2, and possibility3. Thus, the probability of direct measurement is only 30% by using the conventional algorithm. When adopting the proposed algorithm, the operation states of SM_1 and SM_2 is kept unchanged during the $(k\text{-}1)_{th}$ and the k_{th} control period, and the other SM is selected to put into operation, which means SM1 and SM2 are still in the on-state at the k_{th} control period and the other third SM can be calculated by the formula (7), corresponding to state 1. Then the capacitor voltage of the third SM can be directly measured. Therefore, the probability of direct measurement under this situation can be increased to 100%, which would thus increase the number of corrections of observed submodule capacitor voltage. The principle of the proposed algorithm to improve the probability of the direct measurement is illustrated in Figs. 3– 5

In Fig. 3, if there is no SMs in the on-state at the $(k\text{-}1)_{th}$ control period in a certain group, the capacitor voltage is achievable as (9) for correction when one more SM needs to be switched on at the beginning of the k_{th} control period (i.e. only one SM is activated at the k_{th} control period).

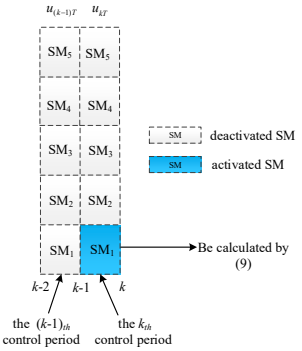


Fig. 3. The principle diagram of the proposed algorithm: only one SM is activated at the k_{th} control period.

In Fig. 4, if there are some SMs in the on-state at the $(k\text{-}1)_{th}$ control period, the activated SMs are forced to stay

switched-on, and one of the deactivated SMs inside this group is selected to be switched on based on the arm current at the $(k\text{-}1)_{th}$ control period when one more SM needs to be switched on at the beginning of the k_{th} control period. Then, the capacitor voltage for correction can be obtained by (7).

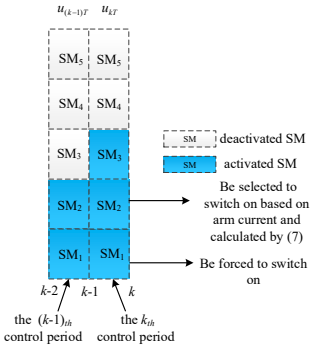


Fig. 4. The principle diagram of the proposed algorithm: the deactivated SM at the $(k\text{-}1)_{th}$ control period is selected to switch on.

In Fig. 5, when the number of SMs that need to be switched on decreases by one at the beginning of the k_{th} control period, the SM that needs to be deactivated should be selected from the activated SMs at the $(k\text{-}1)_{th}$ control period based on the arm current. Then, the capacitor voltage can be calculated by (8) for correction.

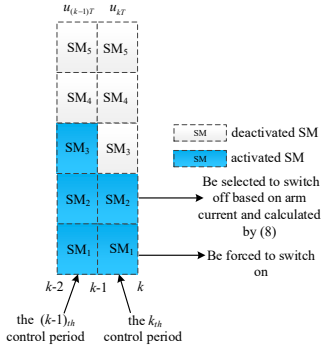


Fig. 5. The principle diagram of the proposed algorithm: the activated SM at the $(k\text{-}1)_{th}$ control period is selected to switch off.

To better implement the proposed algorithm, the implementation conditions need to be considered. Take the upper arm in one phase for illustration:

From the reference [28], the required number of activated SMs in the upper arm can be expressed by,

$$n_{act} \le N - N_i + 1 \tag{20}$$

where n_{act} is the number of the activated SMs, N is the number of SMs in the upper or lower arm, and N_i represents the number of SMs within one group. The essence of the formula (20) is that: in order to implement the proposed method shown in Fig. 3 (i.e., there is no SMs in the on-state at the $(k\text{-}1)_{th}$ control period in a certain group and only one SM is activated at the k_{th} control period), the number of activated SMs in one group of the upper arm needs to be zero, otherwise, the proposed method shown in Fig.3 cannot be implemented.

If the number of activated SMs during system operation satisfies (20), the principle shown in Fig. 3 can be implemented.

Normally, there is a link between the reference voltage of the arm and the modulation ratio. The reference voltage of the upper arm in one phase can be expressed by,

$$u_{up} = \frac{U_{dc}}{2} - \frac{m}{2} U_{dc} \cos(\omega t) \tag{21}$$

where u_{up} is the reference voltage of the upper arm, m is the modulation ratio. The max u_{up} can be expressed by,

$$u_{up\max} = \frac{U_{dc}}{2} + \frac{m}{2} U_{dc} \tag{22}$$

Dividing the SM capacitor voltage U_c into both sides of (22), the maximum number of the activated SMs can be expressed by,

$$n_{\max} = \frac{u_{up\max}}{U_c} = \frac{N}{2} + \frac{m}{2} \cdot N \tag{23}$$

If

$$n_{\max} \le N - N_i + 1 \tag{24}$$

then

$$m \le \frac{N - 2N_i + 2}{N} \tag{25}$$

If the modulation ratio satisfies equation (25), it means that: the number of active SMs in all the control periods is small, (20) can be satisfied throughout the operation of MMC, and the principle shown in Fig. 3 can be implemented. If the modulation ratio does not satisfy (25) while the number of activated SMs in the upper (or lower) arm satisfies (20) at one control cycle, it means that: the number of SMs needing to be active for the operation of MMC is large, but in this control period the number of activated SMs in the upper (or lower) arm is small. Thus, the principle shown in Fig. 3 can be implemented in this control period. If the modulation ratio does not satisfy (25) and the number of activated SMs in the upper (or lower) arm does not satisfy (20) at one control period, it means that: in this control period the number of SMs needing to be active in the upper (or lower) arm is large. Thus, the principle shown in Fig. 3 cannot be implemented. It needs to be mentioned that the implementation of the principle shown in Fig. 4 and Fig. 5 are not limited by the number of the activated SMs and the modulation ratio.

Based on the above analysis, the three direct measuring states can be fully utilized in the proposed measuring algorithm to increase the number of corrections for observed SM capacitor voltages. When the number of SMs on the upper bridge arm is N and the SMs on the bridge arm are all included in one group, the number of corrections (i.e. the times of direct measurements) under the proposed algorithm is about 2N, which is much higher than that under the conventional algorithm (N_{sum}).

Taking the upper bridge arm of phase A as an example, the flow chart of the implementation process of the proposed method is shown in Fig. 6. In Fig. 6, n is the number of SMs in the on-state at the k_{th} control period, *nold* is the number of SMs in the on-state at the $(k\text{-}1)_{\text{th}}$ control period, and i_{pa} is the upper arm current. Firstly, detect the number of SMs that need to be activated at the k_{th} control period. Then, compare the detected number with the number of SMs that are activated at the $(k\text{-}1)_{\text{th}}$ control period. If such number is increased by one, 1) when i_{pa} is greater than 0, keep the states of SMs at the $(k\text{-}1)_{\text{th}}$ control period unchanged and then switch on the off-state SM with the

lowest voltage at $(k\text{-}1)_{\text{th}}$ control period, 2) when i_{pa} is less than 0, keep the states of SMs at the $(k\text{-}1)_{\text{th}}$ control period unchanged and then switch on the off-state SM with the highest voltage at $(k\text{-}1)_{\text{th}}$ control period. If such number is reduced by one, 1) when i_{pa} is greater than 0, keep the states of SMs at the $(k\text{-}1)_{\text{th}}$ control period unchanged and switch off the on-state SM with the highest voltage at $(k\text{-}1)_{\text{th}}$ control period, 2) when i_{pa} is less than 0, keep the states of SMs at the $(k\text{-}1)_{\text{th}}$ control period unchanged and then switch off the on-state SM with the lowest voltage at $(k\text{-}1)_{\text{th}}$ control period. If the above two conditions (i.e., $|n\text{-}nold|=1$) are not satisfied, maintain the pulse signal generated by the natural sorting algorithm. After judging the conditions, the new pulses of each group of SMs are allocated to the corresponding submodule. Finally, based on the pulse signal of the SM and the equations (7) - (9), the actual submodule capacitor voltages can be obtained for correcting the observed capacitor voltages and reducing the measurement errors.

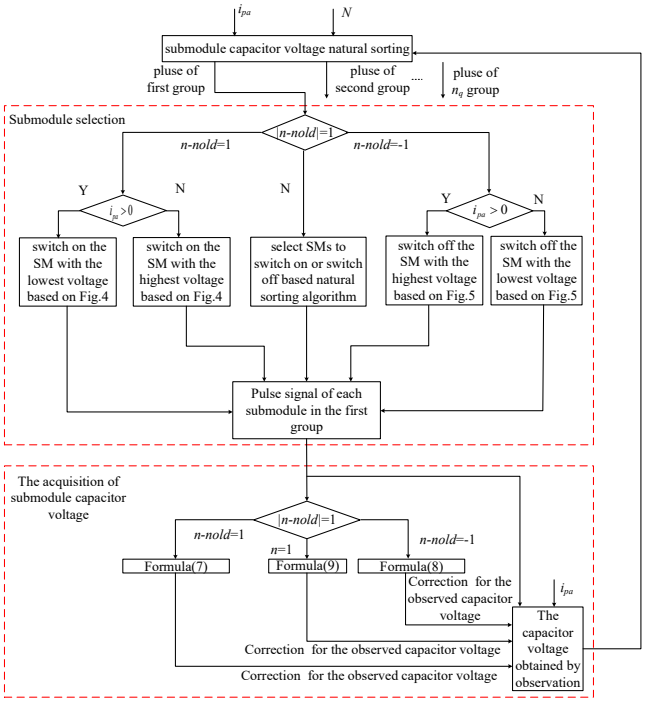


Fig. 6. The flow chart of the implementation process of the proposed method

C. The effect of the proposed algorithm on the switching frequency

From the voltage measuring technology for MMC with reduced sensors in Section II of this paper, it can be known that the capacitor voltage can be measured directly by the three measurable states.

Effect on switching frequency in state 1: When only the i_{th} SM changes its state from off-state to on-state at the k_{th} control period, the number of activated SMs changes from n to $(n+1)$. Based on the proposed algorithm, the states of the n SMs in the $(k\text{-}1)_{\text{th}}$ control period are not changed, and one SM changes the state in the k_{th} control period. Thus, the number of submodule switch actions is 1 in the k_{th} control period. However, the conventional NLM-based voltage measuring algorithm of MMC with reduced sensors does not keep the states of SMs unchanged, so the number of submodule switch actions is greater than 1 or equal to 1 in the k_{th} control period.

Effect on switching frequency in state 2: When only the i_{th} SM changes its state from on-state to off-state at the k_{th} control period, it is similar to "state1". The number of submodule switch actions is 1 in the k_{th} control period under the proposed method but the number of submodule switch actions is greater than 1 or equal to 1 when adopting the conventional NLM-based voltage measuring algorithm of MMC with reduced sensors.

Effect on switching frequency in state 3: When only the i_{th} SM is switched on at the k_{th} control period, the state of the i_{th} SM changes from "0" to "1", which is changed one by one. Thus, only one SM has switch action in this control cycle. In this case, the switching frequency of the MMC is the same as that of using the conventional NLM-based voltage measuring algorithm of MMC with reduced sensors.

Based on the above analysis, it can be concluded that the proposed method will reduce the switching frequency of the MMC.

D. The effect of the proposed algorithm on the balance of MMC

The main advantage of using the sorting algorithm in NLM is eliminating the capacitor voltage imbalance caused by the dynamic or static process. During the operation of MMC, only a small part of the control periods have a level step, and most of the control periods have no step. The proposed algorithm is applied into the period having the level step, and the natural sorting algorithm is adopted in other control periods. This means that one execution of the proposed algorithm would be accompanied by multiple executions of the natural sorting algorithm. Therefore, the influence of the proposed algorithm on capacitor voltage balance can be ignored.

IV. Simulation Results

To verify the correctness and effectiveness of the proposed algorithm, an MMC model with 30 SMs in each arm is established in MATLAB/Simulink, whose parameters are given in Table III.

TABLE III
SPECIFICATIONS OF SIMULATION MODEL

Parameters	Value
Rated frequency (Hz)	50
Rate voltage of SM (V)	600
Capacitor of SM (μF)	4700
Rated DC voltage (V)	18000
Arm inductance (mH)	4.6
Load inductance (mH)	50
Load resistance (Ω)	120
Modulation ratio	0.9
Control frequency (kHz)	5
Number of SMs per arm	30

A. Comparison simulation results when having no capacitance deviation

Fig.7 shows the simulation results when each submodule is equipped with one sensor. As shown in Fig.7(i.e., when each submodule is equipped with one sensor), 1)the capacitor voltage waveforms of SMs are very consistent, which means the error between the waveforms is very small; 2)the THD of the output current is 1.96%, which is obtained by FFT analysis.

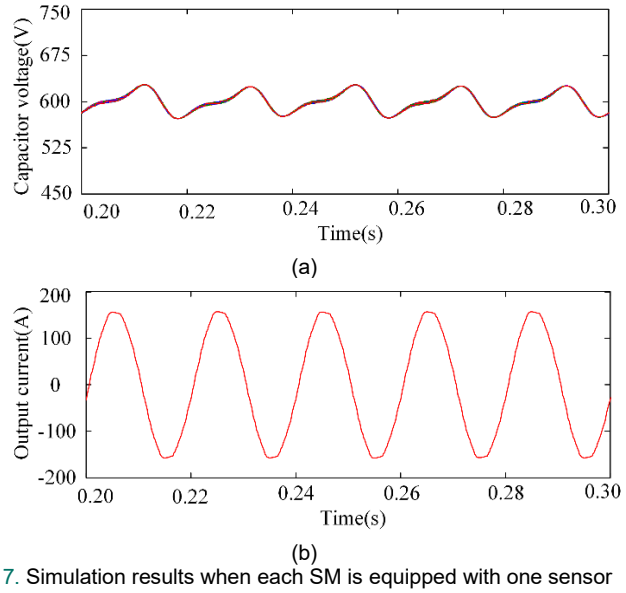
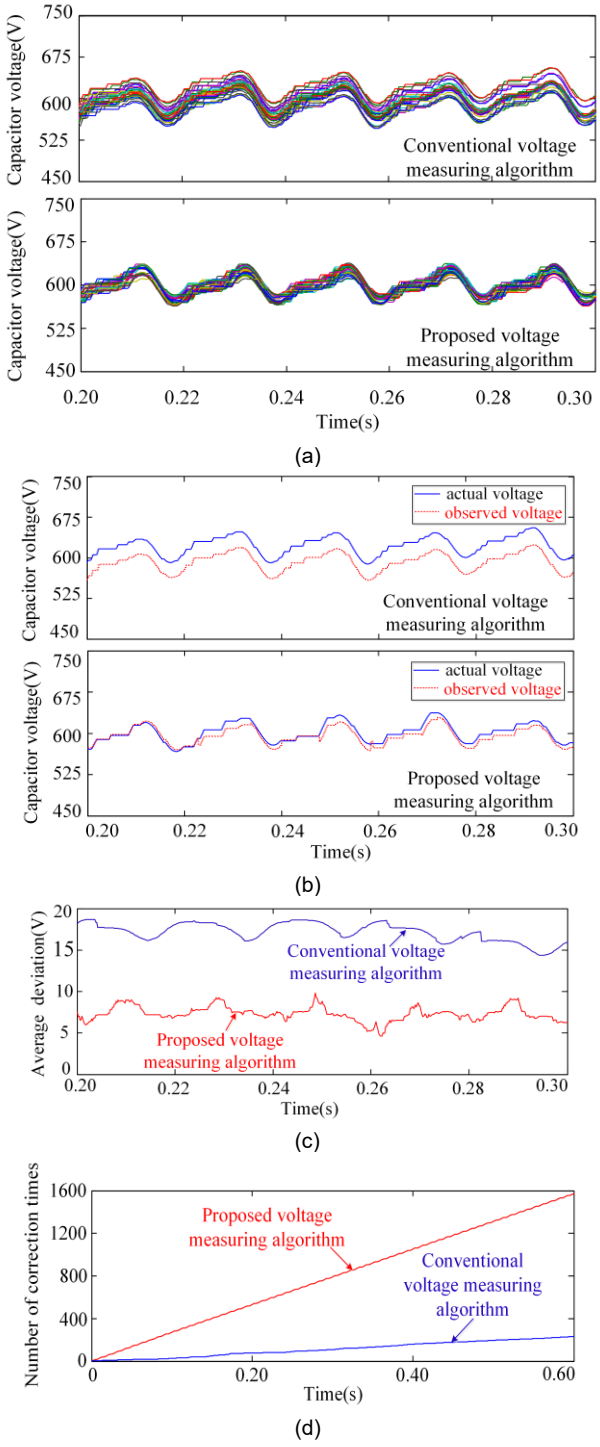
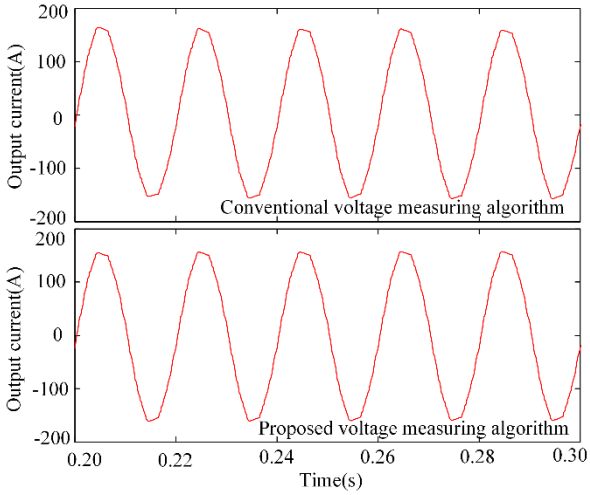


Fig. 7. Simulation results when each SM is equipped with one sensor (i.e.,30 sensors are used). (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC.

Fig. 8 shows comparison simulation results between the conventional NLM-based voltage measuring algorithm and the proposed algorithm when SMs in the upper or lower bridge are combined into one group only. As seen in Fig. 8(a), the capacitor voltages under the conventional algorithm show more dispersion than those under the proposed algorithm. The actual and observed capacitor voltage of SM are illustrated in Fig. 8(b). From Fig. 8(b), it can be seen obviously that the error between observed capacitor voltage and the actual capacitor voltage under the conventional algorithm is larger than that under the proposed algorithm. The average deviation between the actual capacitor voltage and observed capacitor voltage is shown in Fig. 8(c). It can be seen that the average deviation under the conventional algorithm is 17.2V, but it can be decreased to 7.8V by adopting the proposed algorithm. The number of corrections for the SMs capacitor voltages on the upper arm of phase A is shown in Fig. 8(d). From Fig.8(d), it can be observed that: 1) there is only a small number of corrections in 0.6s under the conventional algorithm, which is 229, and the number of corrections in average in a power frequency cycle is only 7.6, which agrees with the analysis in (19); however, 2) by utilizing the proposed algorithm, the number of corrections in average in a power frequency cycle increases to 53. Because the SMs in the upper or lower bridge are divided into one group only, the SMs could only be selected one by one to be activated or deactivated based on the basic principle of the conventional algorithm, which leads to the small probability of direct measurement and the small number of corrections for observed submodule capacitor voltage. After adopting the proposed algorithm, the probability of direct measurement can be greatly increased. Correspondingly, the number of corrections can be increased, which would thus decrease the measuring errors. The output current of MMC under the two methods are shown in Fig.8(e). The THD of the output current is 3.29% when adopting the conventional algorithm and 2.61% by using the proposed algorithm, which are obtained from FFT analysis.

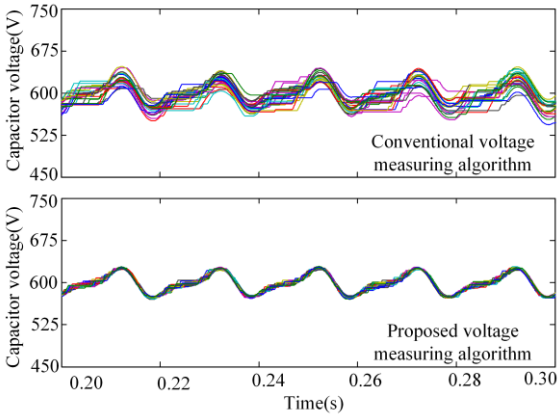




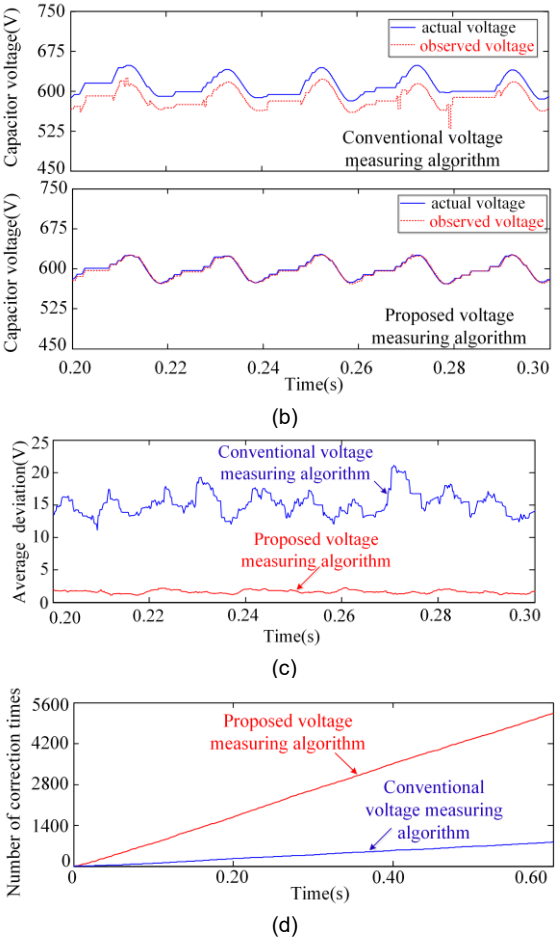
(e)

Fig. 8. Simulation results when SMs on the upper or lower bridge are combined into one group. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage. (d) The number of SM capacitor voltage corrections on the upper arm of phase A.(e)The output current of MMC

It needs to be mentioned that the probability of the occurrence of direct measurement will be further increased if SMs are divided into more groups and the direct measurement may occur in each group. The simulation results are given in Fig. 9 when SMs in the upper or lower bridge are divided into five groups. The average number of corrections in a power frequency cycle increases to 28.6 and 177 under the conventional and proposed algorithms, respectively, which are shown in Fig. 9(d). The error between the actual capacitor voltage and the observed capacitor voltage decreases and the average deviation decreases to 14.8V and 1.91V under the conventional and proposed algorithm, as shown in Fig. 9(b) and (c), respectively. As seen in Fig. 9(a), increasing the groups cannot completely eliminate the capacitor voltage deviations, but it can make the deviations smaller. Based on the results in Fig. 9 and Fig. 8, it can be concluded that the appropriate increase in the groups can increase the measurement accuracy, especially under the proposed algorithm.



(a)



(b) (c) (d)

Fig. 9. Simulation results when SMs on the upper or lower bridge are divided into five groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage. (d) The number of SM capacitor voltage corrections on the upper arm of phase A.

B. Comparison simulation results when having capacitance deviations

In order to demonstrate the effectiveness of the proposed algorithm under capacitance deviations, several simulation studies are performed when having different SM capacitances. The rated capacitance of the capacitor of SMs in MMC is set to 4700μF. Normally, the capacitance of the capacitor is not expected to lower than 50% of its nominal value [16], thus the capacitance of SM_1, SM_2, SM_7, and SM_8 are set to 4200μF, 3700μF, 3200μF, and 2900μF, respectively, (i.e. there has a deviation of 10.6%, 21.3%, 31.9%, and 38.3% compared to their corresponding rated values).

Fig. 10 presents the related simulation results when the SMs on the upper or lower arm bridge are divided into one group. As seen in Fig. 10(a), the capacitor voltages under the conventional algorithm have more dispersion than those under the proposed algorithm. It is because the three measurable states are all applied in the proposed algorithm, which greatly increases the probability of direct measurement. Correspondingly, when using the proposed algorithm, the average number of corrections in a power frequency cycle is 52, while it is only 7.59 under the conventional algorithm, as shown in Fig. 10(d). As seen in Fig. 10(b) and (c), the error between the actual

capacitor voltage and the observed capacitor voltage is also decreased by adopting the proposed algorithm, and the average deviation is decreased from 28.6V (under the conventional algorithm) to 9.7V (under the proposed algorithm).

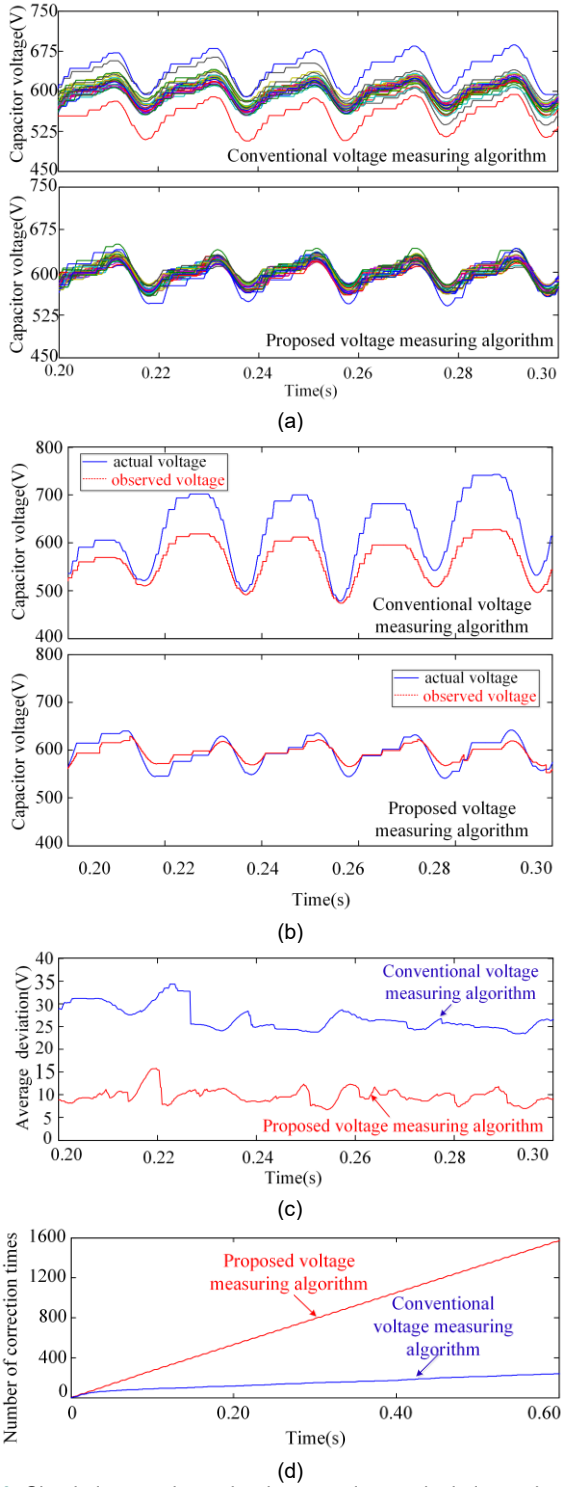


Fig. 10. Simulation results under the capacitance deviations when SMs on the upper or lower bridge are combined into one group. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage. (d) The number of SM capacitor voltage corrections on the upper arm of phase A.

The related simulation results are shown in Fig. 11 when SMs on the upper or lower bridge are divided into five groups. The obtained results are similar to those as above, which include that: under the proposed algorithm, 1) the capacitor voltages have less dispersion and 2) the average deviation and the average number of corrections are lower and larger, respectively. Additionally, comparing the results in Fig. 11(a) and 9(a), it can be obtained that there still have unbalanced capacitor voltages and certain dispersion among the SMs when adopting the proposed algorithm, which is due to the capacitance parameter deviations.

Based on the simulation results in Fig. 10 and Fig. 11, it can be concluded that the proposed algorithm is still effective in the situation of capacitance deviations.

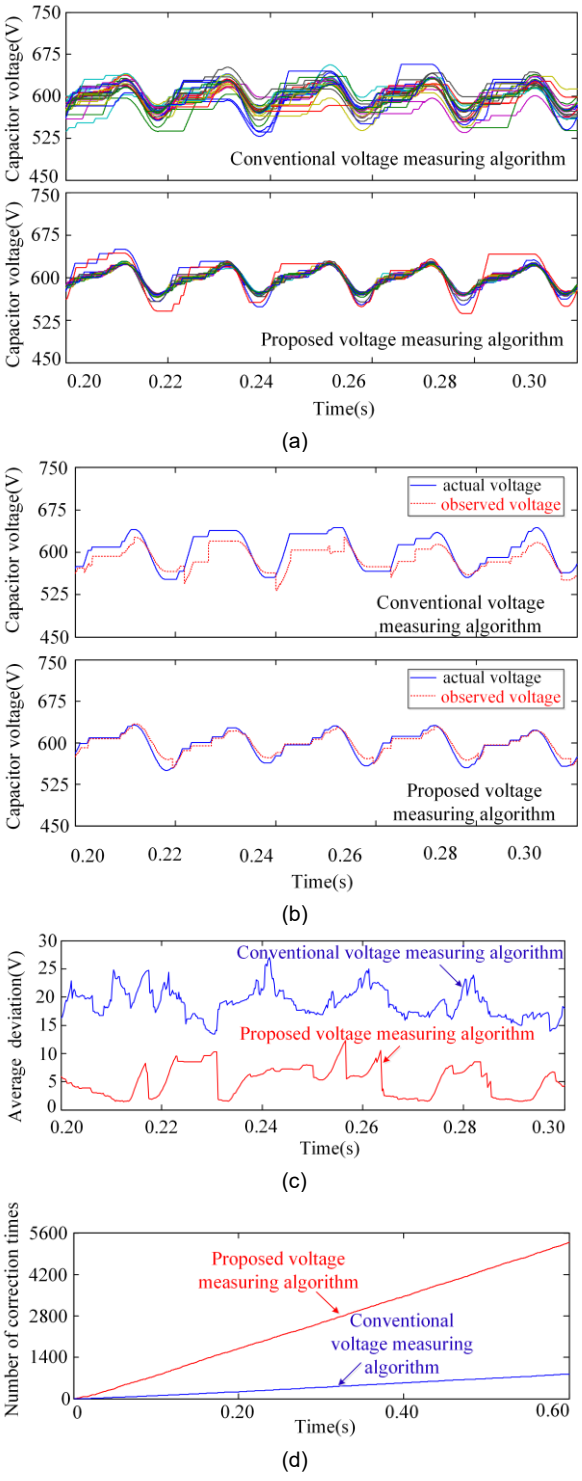
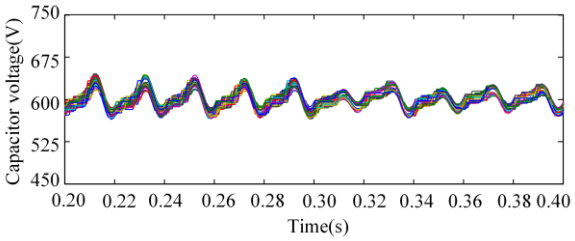


Fig. 11. Simulation results under the capacitance deviations when SMs on the upper or lower bridge are divided into five groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage. (d) The number of SM capacitor voltage corrections on the upper arm of phase A.

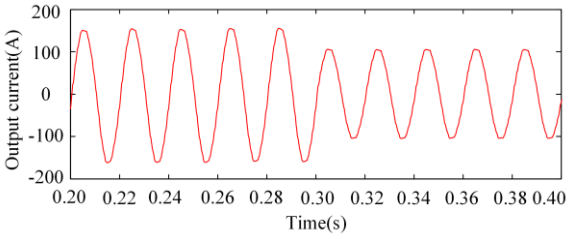
C. Simulation results when the load changes

In order to verify the effectiveness of the proposed method under dynamic conditions, the load resistance changes from 120Ω to 180Ω at 0.3s, and the proposed method is adopted.

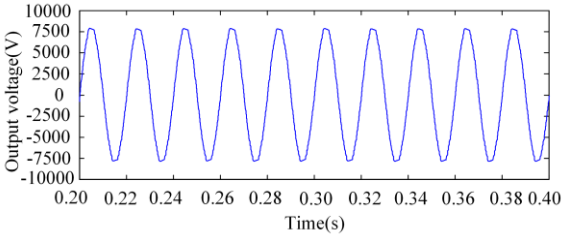
Fig. 12 and Fig. 13 show the simulation results when the SMs in the upper or lower bridge are divided into one group and five groups respectively. From Figs. 12 -13, it can be obtained that: 1) the capacitor voltages of the SMs change at 0.3s and then quickly reach a stable state, as shown in Figs. 12(a) and 13(a); 2) the amplitude of the output current has a drop and then becomes stable, as shown in Figs.12(b) and 13(b); 3) the amplitude of the output voltage maintains constant in the whole period, as shown in Figs. 12(c) and 13(c). Accordingly, it can be concluded that the proposed method is effective under dynamic conditions based on the simulation results in Figs. 12-13.



(a)

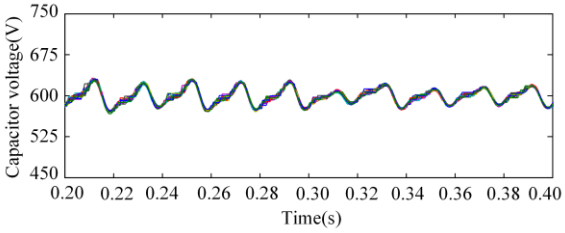


(b)

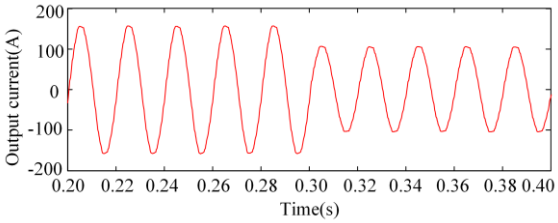


(c)

Fig. 12. Simulation results under dynamic conditions when SMs on the upper or lower bridge are combined into only one group. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC. (c) The output voltage of MMC.



(a)



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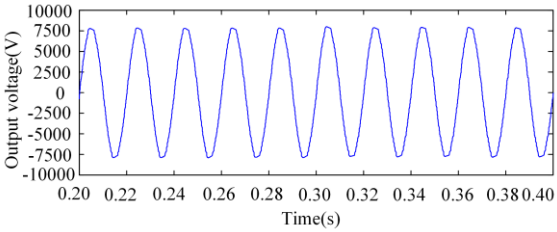
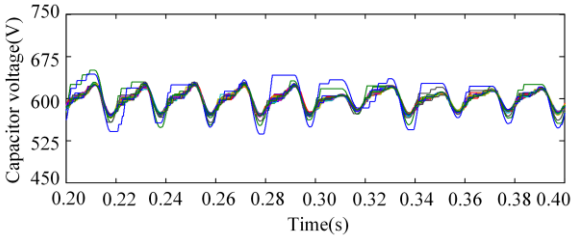


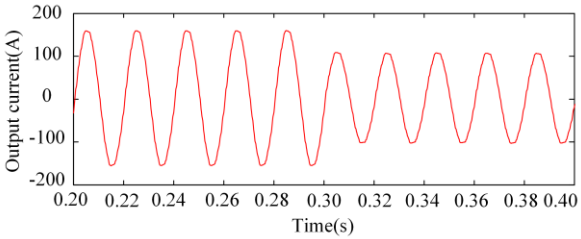
(c)

Fig. 13. Simulation results under dynamic conditions when SMs on the upper or lower bridge are divided into five groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC. (c) The output voltage of MMC.

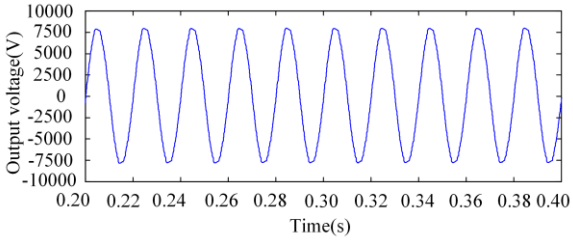
Fig. 14 shows the simulation results when the SMs in the upper or lower bridge are divided into five groups and capacitances have deviations. Similar observed results to that in Figs. 12-13 can be obtained from Fig. 14, which means that the robustness of the proposed method is also good in the condition of capacitance deviations.



(a)



(b)



(c)

Fig. 14. Simulation results under dynamic conditions when SMs on the upper or lower bridge are divided into five groups and capacitances have deviations. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC. (c) The output voltage of MMC.

V. Experimental Results

A down-scale single-phase 9-level MMC experimental platform is set up, as shown in Fig. 15. The parameters of the experimental platform are given in Table IV.

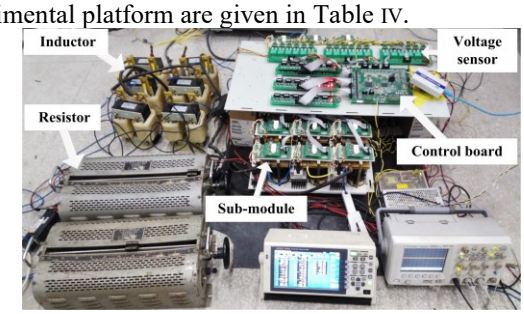


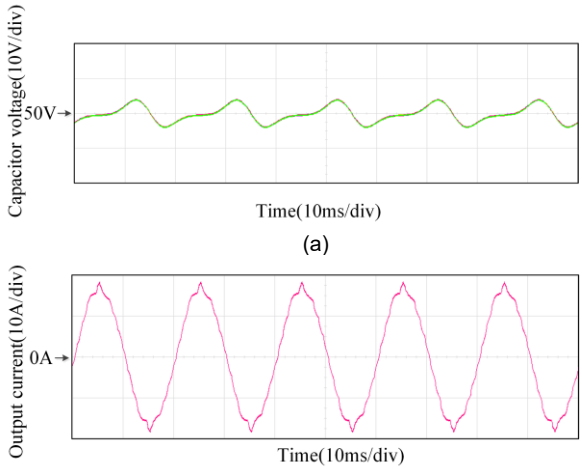
Fig. 15. Experimental set-up of single-phase 9-level MMC

TABLE IV
PARAMETERS OF THE EXPERIMENTAL PLATFORM

Parameter	Values
Number of SMs on the upper or lower arm	8
Rate voltage of SM (V)	50
Capacitance of SM(μF)	4700
Rate DC voltage (V)	400
Inductance on each arm(mH)	2
Load resistance (Ω)	10
Load inductance (mH)	5
Modulation ratio	0.9
Control frequency (kHz)	5

A. Experimental results when having consistent capacitance parameters

Fig. 16 shows the experimental results when each submodule is equipped with one sensor. The experimental results are consistent with the simulation results. As seen in Fig. 16, the capacitor voltage waveforms of SMs are consistent and the THD of the output current is 5.62% when every SM has a sensor.

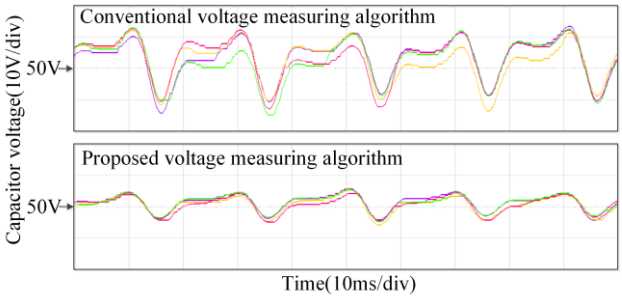


(a)

(b)

Fig. 16. Experimental results when each SM is equipped with one sensor(8 sensors are used). (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC.

Fig. 17 shows the comparison experimental results between the conventional NLM-based voltage measuring algorithm and the proposed algorithm when SMs in the upper or lower bridge are combined into one group. The capacitor voltages under the conventional algorithm have more dispersion than those under the proposed algorithm, as shown in Fig. 17(a). The actual and observed capacitor voltage of one SM are presented in Fig. 17(b). From Fig. 17, it can be observed that the error between observed capacitor voltage and the actual capacitor voltage under the conventional algorithm is larger than that under the proposed algorithm. As shown in Fig. 17(c), The average deviation between the actual capacitor voltage and observed one is 2.76V under the conventional algorithm, while the average deviation decreases to 0.78V by using the proposed algorithm. The average number of corrections in a power frequency cycle is 5.4 and 35.2 under the conventional and proposed algorithm, which are acquired by a counter implemented in the DSP. The THD of the output current is 12.67% when adopting the conventional algorithm and 8.93% when using the proposed algorithm, which can be obtained from Fig.17(d) by FFT analysis.



(a)

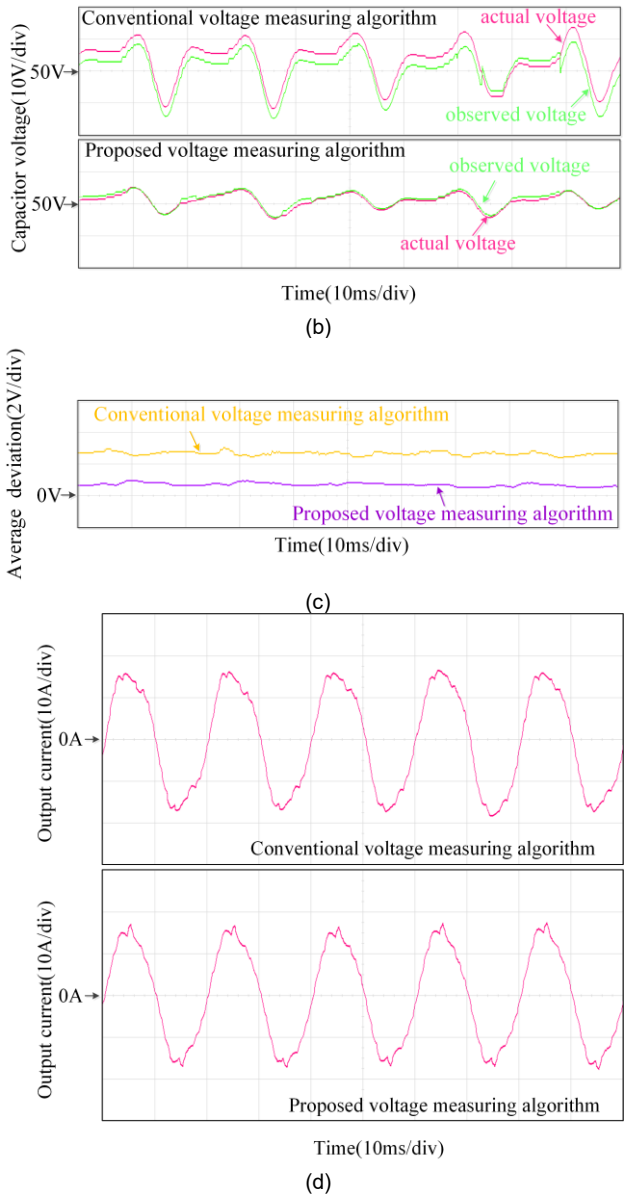


Fig. 17. Experimental results when SMs on the upper or lower bridge are combined into one group. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage. (d) The output current of MMC.

Fig. 18 presents experimental results under the conventional and proposed algorithm when the SMs on the upper or lower bridge are divided into two groups. As seen in Fig. 18(a), the capacitor voltages under the proposed algorithm present a smaller dispersion than those under the conventional algorithm. The error between the observed capacitor voltage and the actual capacitor voltage under the proposed algorithm is smaller than that under the conventional algorithm, as shown in Fig. 18(b). From Fig. 18(c), it can be seen that the average deviation under the proposed and conventional algorithms is 0.63V and 2.35V, respectively. The average number of corrections in a power frequency cycle under the proposed and conventional algorithm is 48.5 and 13.2, respectively, which are acquired by a counter implemented in the DSP. Comparing the results in Fig. 18 and Fig. 17, it can be obtained that the appropriate increase of sensor groups can increase the number of corrections and thus decrease the measuring errors.

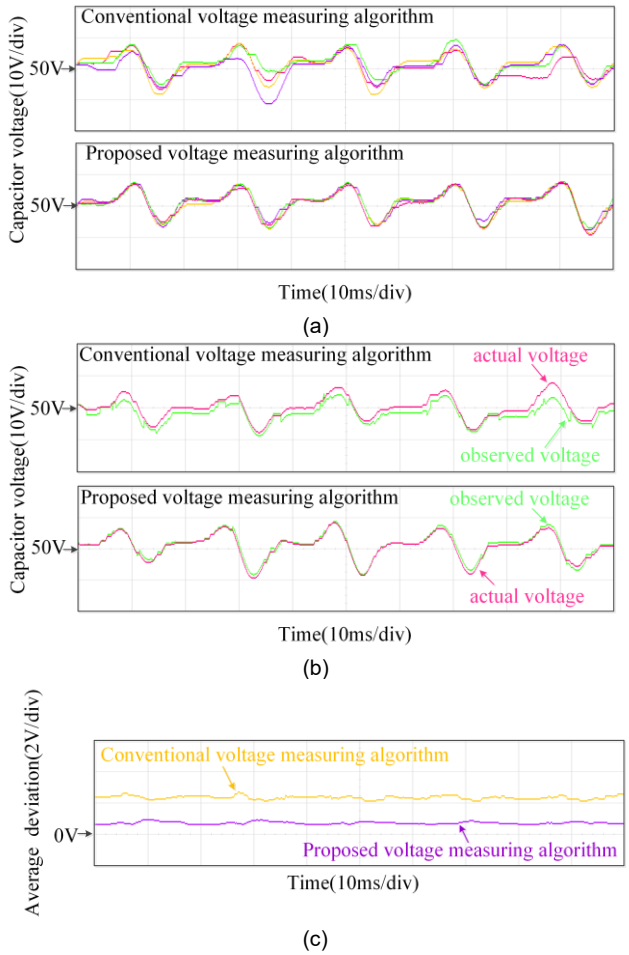


Fig. 18. Experimental results when SMs on the upper or lower bridge are divided into two groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage.

B. Experimental results when having capacitance parameter deviations

In the following experiments, the capacitance of SM_1, SM_2, SM_7 and SM_8 is 4100uF, 3873uF, 3400uF, and 3197uF, i.e. with a deviation of 12.8%, 17.6%, 28.7%, and 34% respectively compared to its rated value(4700uF).

Fig. 19 presents the experimental results when SMs on the upper or lower bridge are combined into one group. As seen in Fig. 19(a), there have large deviations of capacitor voltages under the conventional algorithm while the deviations are decreased by adopting the proposed measuring algorithm. The error between the observed capacitor voltage and the actual capacitor voltage under the proposed measuring algorithm is smaller than that under the conventional algorithm, as shown in Fig. 19(b). In Fig. 19(c), the average deviation under the proposed and conventional measuring algorithms are 1.53V and 3.88V, respectively. The average number of corrections in a power frequency cycle under the proposed and conventional algorithm is 35.1 and is 5.1, respectively. Additionally, it needs to be mentioned that the capacitor voltages in Fig. 19 have more deviations than those in Fig. 17 due to the capacitance parameter deviations.

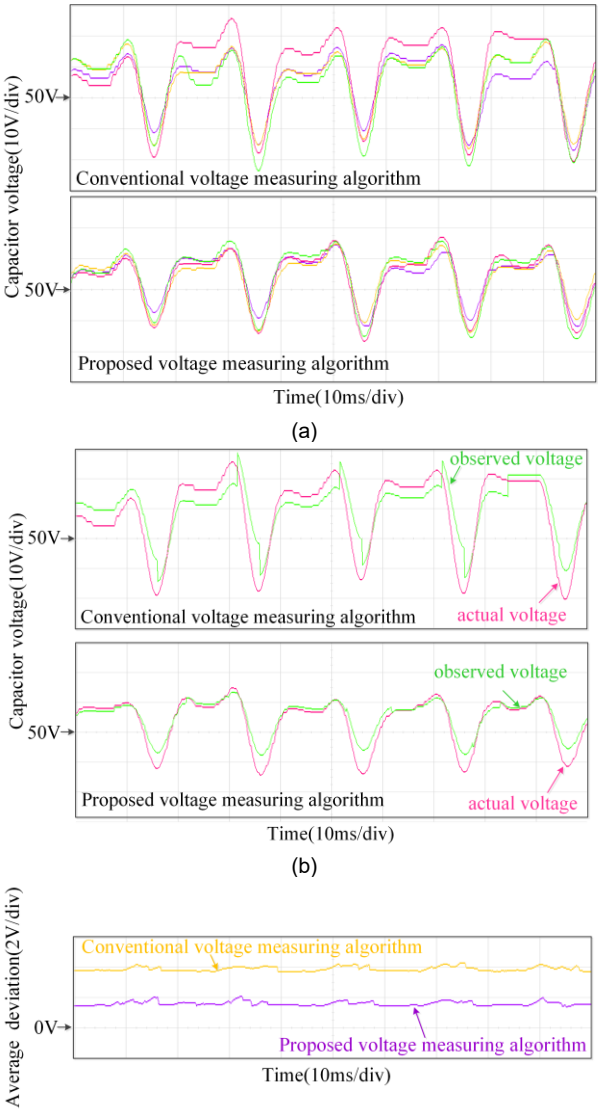


Fig. 19. Experimental results under capacitance deviations when SMs on the upper or lower bridge are combined into one group. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage.

Fig. 20 shows the experimental results when the SMs on the upper or lower bridge are divided into two groups and there have capacitance deviations. As shown in Fig. 20(a), under the conventional algorithm, the capacitor voltage balance is not particularly good and there exist deviations among capacitor voltages. However, by adopting the proposed algorithm, the capacitor voltages become almost balanced, and they have less dispersion because the average number of corrections in a power frequency cycle is increased from 13.5 (under the conventional algorithm) to 47.9. Correspondingly, the error between the actual capacitor voltage and the observed one is decreased under the proposed algorithm, as shown in Fig. 20(b). The average deviation under the proposed and conventional algorithm are 1.08V and 3.06 V, respectively, as shown in Fig. 20(c).

Based on the experimental results in Figs. 19- 20, it can be concluded that the proposed algorithm is still effective when having the capacitance deviations.

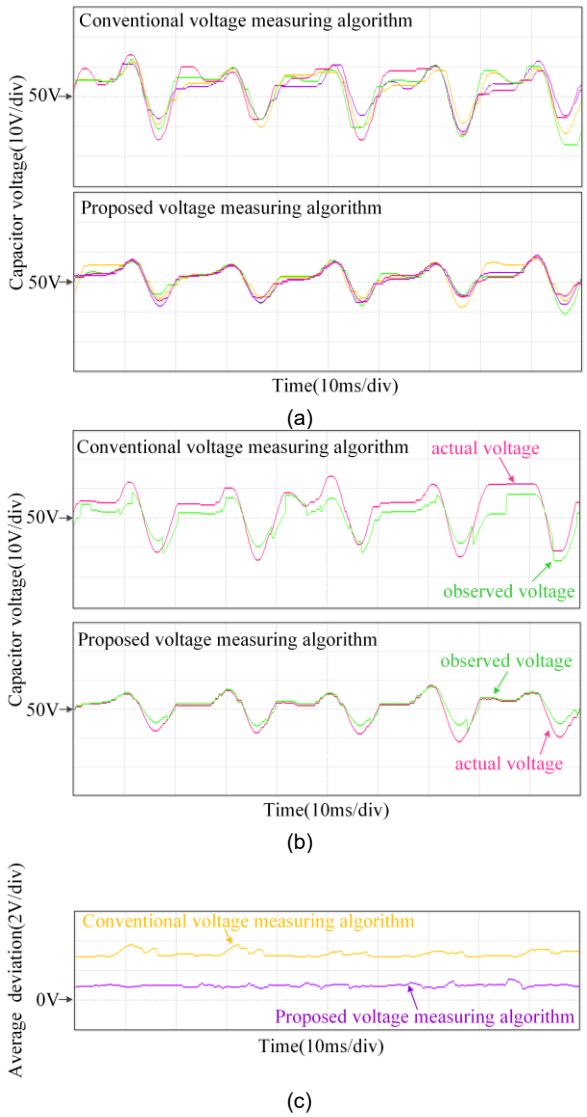


Fig. 20. Experimental results under capacitance deviations when SMs on the upper or lower bridge are divided into two groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The actual and observed capacitor voltage of one SM. (c) The average deviation between the observed value and the actual value of capacitor voltage.

C. Experimental results when the load changes

Figs. 21 - 23 presents the experimental results to verify the effectiveness of the proposed method under dynamic conditions. In the experiments, the load resistance changes from (10Ω+5mL) to(20Ω+5mL) at 0.2s.

Fig.21 shows the experimental results when the SMs in the upper or lower bridge are combined into only one group. As seen in Fig.21(a), the capacitor voltages have a short distortion at 0.2s, and then become stable quickly. The amplitude of the output current drops from17.8A to 9.1A, and then the output current becomes stable, as shown in Fig.21(b). As seen in Fig.21(c), the output voltage remains constant at about 188V before and after load changes. From Fig.21, it can be concluded that the proposed method is still effective when the load changes.

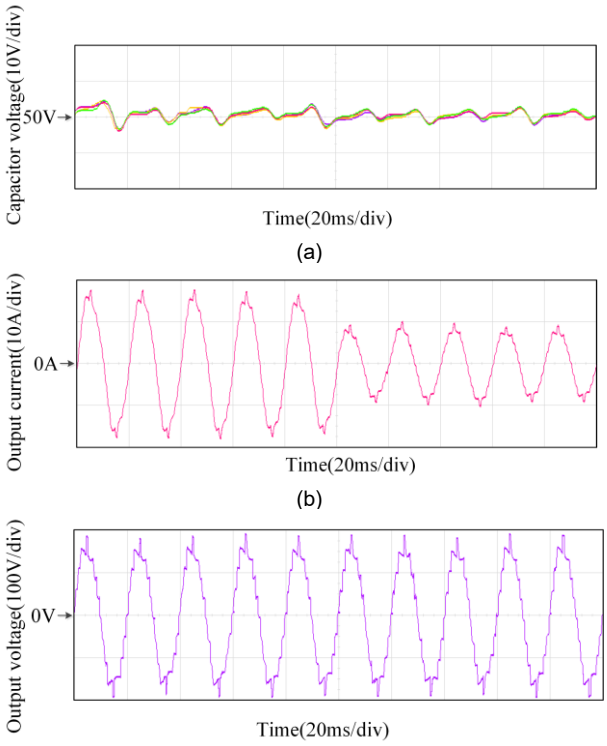
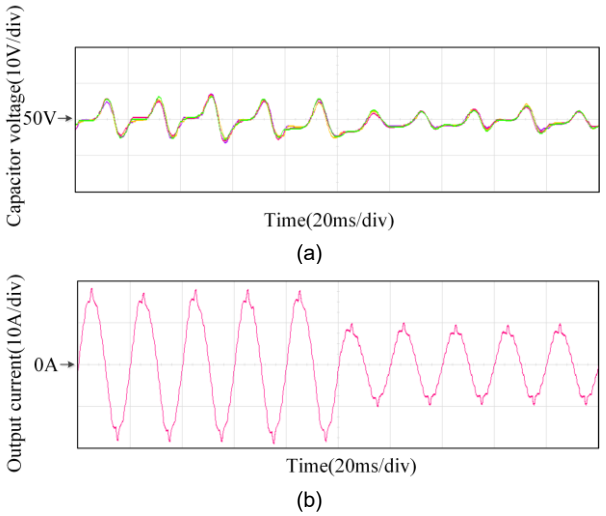


Fig. 21. Experimental results under dynamic conditions when SMs on the upper or lower bridge are combined into only one group. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC. (c) The output voltage of MMC.

Fig. 22 presents experimental results when the SMs on the upper or lower bridge are divided into two groups. The results are similar to those in Fig.21. The capacitor voltages show a little distortion at 0.2s and then become stable quickly. The output current after 0.2s is reduced to about half of that before 0.2s, and the current always remain stable before and after 0.2s. The output voltage of MMC is constant during the whole operation.



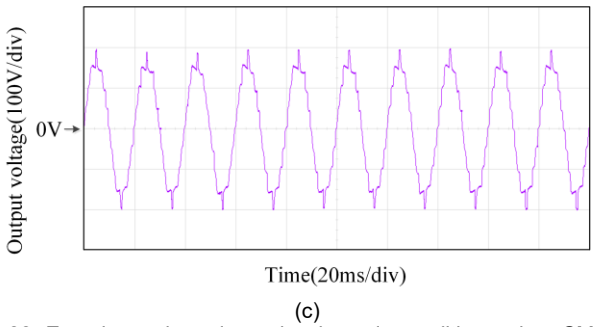


Fig. 22. Experimental results under dynamic conditions when SMs on the upper or lower bridge are divided into two groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC. (c) The output voltage of MMC.

Fig. 23 shows the experimental results when the SMs on the upper or lower bridge are divided into two groups and there have capacitance deviations. As shown in Fig.23, the capacitor voltages are still stable after 0.2s. The output current decreases at 0.2s and then becomes stable. The output voltage of MMC maintains constant during the whole operation. Based on the experimental results in Fig.23, it can be obtained that the proposed method has great robustness even in the situation of having capacitor deviations.

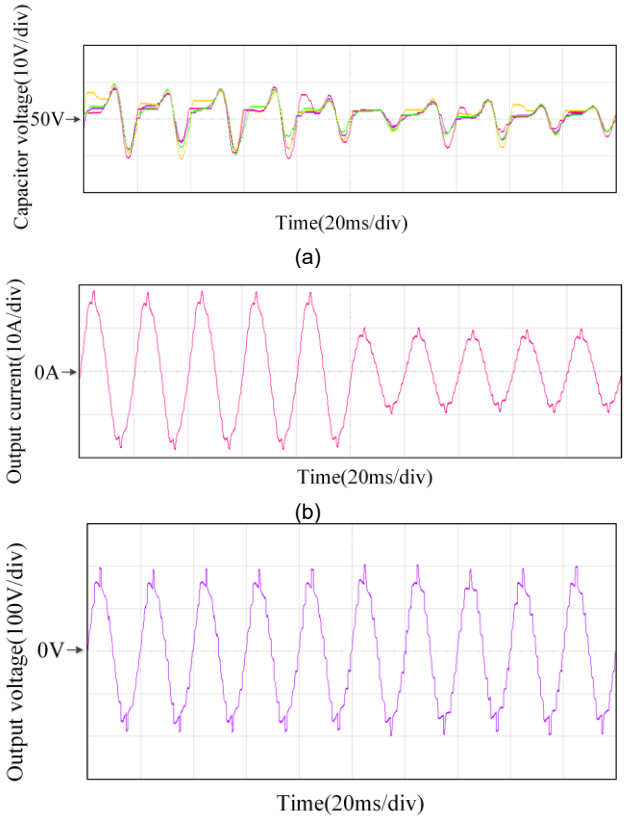


Fig. 23. Experimental results under capacitance deviations and dynamic conditions when SMs on the upper or lower bridge are divided into two groups. (a) The capacitor voltages of SMs in the upper arm of phase A. (b) The output current of MMC. (c) The output voltage of MMC.

VI. Conclusion

In this paper, an improved SM capacitor voltage measuring algorithm for MMC with reduced sensors proposed. The major advantage of the proposed measuring algorithm is reducing the

number of capacitor voltage sensors but with an acceptable system performance in comparison with the conventional capacitor voltage measuring method (i.e., one sensor for each SM capacitor). Besides, compared with the reduced-sensor-based MMC operation with the conventional NLM, the proposed algorithm can effectively increase the number of corrections about dozens of times and thus greatly reduce the capacitor voltage measurement errors. Even in the situation with capacitance variation of capacitors, the proposed algorithm is still effective. Finally, the effectiveness and feasibility of the proposed algorithm are verified by both simulation and experimental results.

APPENDIX

On page 3, $s(i)$ represents the state of a switch. For a detailed explanation, the formulas and the figures in the following derivation are renumbered (i.e., their numbers are not the same as that above).

The output of the voltage sensor at the k_{th} control period is equal to the voltage sum of all SMs in the on-state.

$$u_{kT} = \sum_{i=1}^{N} s(i)_{(k-1)} u_c(i)_{kT} \tag{1}$$

where kT is the k_{th} control period, $u_c(i)$ is the voltage of the i_{th} SM, and $s(i)_{(k-1)}$ is the state of the i_{th} SM at the k_{th} control period ($s(i)_{(k-1)}$ is a switch, if $s(i)_{(k-1)}$ is changed at the beginning of the k_{th} control period, the state of the i_{th} SM at the whole k_{th} control period will be equal to the changed $s(i)_{(k-1)}$. It is shown in Fig. a or Fig. b). When the i_{th} SM is in on-state, $s(i)$=1; otherwise $s(i)$=0. At the $(k\text{-}1)_{th}$ control period, the measured value of the sensor is:

$$u_{(k-1)T} = \sum_{i=1}^{N} s(i)_{(k-2)} u_c(i)_{(k-1)T} \tag{2}$$

According to the capacitor charging model, at the beginning of the k_{th} control period, the voltage of SM can be expressed by the integration of bridge arm current which flows through submodule capacitor at $(k\text{-}1)_{th}$ control period, as:

$$u_c(i)_{kT} = u_c(i)_{(k-1)T} + \frac{1}{c}\int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T}\, dt \tag{3}$$

Where c is the capacitance and $i_{(k\text{-}1)T}$ is the arm current at the $(k\text{-}1)_{\text{th}}$ control period.

Substituting (3) into (1), it can be obtained,

$$u_{kT} = \sum_{i=1}^{N} s(i)_{(k-1)} \left[u_c(i)_{(k-1)T} + \frac{1}{c}\int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T}\, dt \right] \tag{4}$$

Supposing Δu_k is the difference between the measured values at the k_{th} and $(k\text{-}1)_{th}$ control period, which is expressed by,

$$\Delta u_k = u_{kT} - u_{(k-1)T} \tag{5}$$

Substituting (2) and (4) into (5), it can be obtained,

$$\begin{aligned} \Delta u_k &= \sum_{i=1}^{N} s(i)_{(k-1)} u_c(i)_{(k-1)T} \\ &+ \frac{1}{c}\sum_{i=1}^{N} s(i)_{(k-1)} \int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T}\, dt \\ &- \sum_{i=1}^{N} s(i)_{(k-2)} u_c(i)_{(k-1)T} \end{aligned} \tag{6}$$

State1: If only the i_{th} SM changes its state from off-state to on-state at the k_{th} control period, the switch state change of the i_{th} SM is shown in Fig. a,

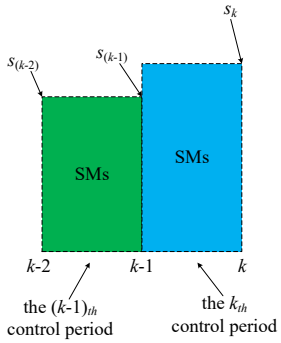


Fig. a: the diagram of switch state change when the i_{th} SM changes from off-state to on-state

The statuses of the SMs at the $(k\text{-}1)_{th}$ and k_{th} control periods are expressed by,

$$\begin{cases} [s(1)_{(k-1)}, \cdots, s(i)_{(k-1)}, \cdots, s(N)_{(k-1)}] = [*, \cdots, 1, \cdots, *] \\ [s(1)_{(k-2)}, \cdots, s(i)_{(k-2)}, \cdots, s(N)_{(k-2)}] = [*, \cdots, 0, \cdots, *] \end{cases} \tag{7}$$

Thus, Δu_k can be expressed by,

$$\begin{aligned} \Delta u_k &= u_c(i)_{(k-1)T} + \frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-1)} i_{(k-1)T}\, dt \\ &= u_c(i)_{(k-1)T} + \frac{1}{c}\int_{(k-1)T}^{kT} i_{(k-1)T}\, dt \\ &\quad + \frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-2)} i_{(k-1)T}\, dt \\ &= u_c(i)_{kT} + \frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-2)} i_{(k-1)T}\, dt \end{aligned} \tag{8}$$

In this case, the voltage of the i_{th} SM can be expressed by,

$$u_c(i)_{kT} = \Delta u_k - \frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-2)} i_{(k-1)T}\, dt \tag{9}$$

State2: If only the i_{th} SM changes its state from on-state to off-state at the k_{th} control period, the switch state change of the i_{th} SM is shown in Fig. b,

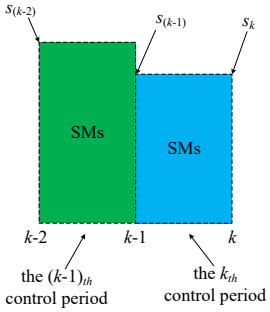


Fig. b: the diagram of switch state change when the i_{th} SM changes from on-state to off-state

The statuses of the SMs at the $(k\text{-}1)_{th}$ and k_{th} control periods are expressed by,

$$\begin{cases}[s(1)_{(k-1)},\cdots,s(i)_{(k-1)},\cdots,s(N)_{(k-1)}]=[*,\cdots,0,\cdots,*] \\ [s(1)_{(k-2)},\cdots,s(i)_{(k-2)},\cdots,s(N)_{(k-2)}]=[*,\cdots,1,\cdots,*]\end{cases} \tag{10}$$

And $u_c(i)_{(k-1)T}$ can be equal to $u_c(i)_{kT}$, then Δu_k can be expressed by,

$$\begin{aligned}\Delta u_k &= -u_c(i)_{(k-1)T}+\frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-1)}i_{(k-1)T}dt \\ &= -u_c(i)_{kT}+\frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-1)}i_{(k-1)T}dt\end{aligned} \tag{11}$$

In this case, the voltage of the i_{th} SM can be expressed by,

$$u_c(i)_{kT} = -\Delta u_k+\frac{1}{c}\sum_{i=1}^{N}\int_{(k-1)T}^{kT} s(i)_{(k-1)}i_{(k-1)T}dt \tag{12}$$

State3: If only the i_{th} SM is switched on at the k_{th} control period, the measured value is the actual voltage of the i_{th} SM, which can be expressed by,

$$u_c(i)_{kT} = u_{kT} \tag{13}$$

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