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Published in:
IEEE Transactions on Power Electronics

DOI (link to publication from Publisher):
[10.1109/TPEL.2021.3078182](https://doi.org/10.1109/TPEL.2021.3078182)

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

Citation for published version (APA):
Hashemzadeh, E., Aghamohammadi, M. R., Asadi, M., Moghaddam, J. Z., & Guerrero, J. M. (2021). Secondary Control for a D-STATCOM DC-Link Voltage under Capacitance Degradation. *IEEE Transactions on Power Electronics*, 36(11), 13215-13224. [9426407]. <https://doi.org/10.1109/TPEL.2021.3078182>

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Secondary Control for a D-STATCOM DC-link Voltage under Capacitance Degradation

Ehsan Hashemzadeh, Mohammadreza Aghamohammadi, Mehdi Asadi, Javad Zahedi Moghaddam and Josep M. Guerrero, *Fellow, IEEE*

Abstract- Degradation of the DC link Capacitance due to aging, cell failure, and fuse failure has a negative impact on the AC-side current THD of a D-STATCOM and power quality. These variations noticeably increase the modulation index and DC-link voltage ripple leading to growing the AC-side current THD of the D-STATCOM. To solve this problem, this paper proposes a modification mechanism as a secondary control layer added to the common control structure, nested control loops. This upper-hand layer regulates DC-link voltage set-point based on modulation index magnitude to remain the current THD in the standard range indirectly. This method works in steady-state modes and does not change the primary controllers. Simulation and experimental results show that this mechanism properly controls the device and regulates the THD and improve power quality in the network under DC-link capacitance variations.

Index Terms— D-STATCOM, DC-link capacitance variations, Secondary modification mechanism, THD regulation, Power quality

I. INTRODUCTION

Distribution static compensator (D-STATCOM) is a shunt custom power device installed at the sensitive points in distribution networks for voltage stabilizing, flicker suppressing, and power quality modifying at the point of the common coupling (PCC) through reactive power control [1]–[3]. A D-STATCOM is a voltage source converter (VSC) that can work in two reactive power compensation modes: injection (capacitive) and absorption (inductive). The effective operation of a D-STATCOM is highly dependent on its physical parameters—including DC-link voltage, capacitance of the DC-link capacitor bank (CB), power switches [4], and the impedance of the AC-side filter [5]. It is indicated that the good performance of D-STATCOM are highly degraded under occurrence of faults in these components and the physical structure of the converter.

The capacitance of DC-link CB generally specifies the full compensation rate, compensation speed, and DC-link voltage ripple, and thus, it has noticeably impacts on the dynamic

response of the system and power quality at PCC. This parameter should not be chosen small or large owing to safety issues, and the right half plane (RHP) zero in DC link voltage dynamic [6]. In addition, the DC-link CB size of the power converters usually has high capacitance in practical application [7]. Capacitors are recognized as the most fragile components so that they are responsible for 30% of the failures occurred in the converters [8]. The capacitance of DC link CB also vulnerable to be degraded from its nominal value due to aging, cell failure, and fuse failure in CB [8]. DC-link CB size degradation from nominal value can cause negative effects on the power system that prompt the unstable modes and active the protection devices and boards that disconnect the D-STATCOM from the grid. As a result, this leads to decrease of the power quality and voltage stability at PCC. Accordingly, engineers and experts have been dedicating a great deal of their attention to make converters more resilient against the CB failures [8]. With this in mind, three factors—including analytical physics [9]; design and verification [10]; and control and monitoring [11]—are specified as the main elements in the analysis of the reliability in converters. In DC-link capacitors, Analytical physics addresses the understanding of the failure mechanisms and types of the failures. This piece of information is highly important in prediction of the lifetime and reliability enhancement of the all power electronic components, especially capacitors [8]. Design and verification stages deal with finding an efficient structure for the DC-link CB to manage electric shocks such as current and voltage stresses and decrease them to improve the reliability of the system [12]. In spite of analytical physics, design and verification that consider the reliability of DC-link before implementation and operation, control and monitoring focus on online operational conditions [9]. Monitoring methods anticipate the system's behavior in the upcoming events, while control explores the design of fault-tolerant methods for sub-optimal operation of the system under faulty situations. Control approaches such as passivity-based theorem [13], nonlinear differential-algebraic [14], a combination of H_∞ and feedback linearization (FL) [15], and FL [16] have been adopted to assure meeting of control demands in a D-STATCOM. However, these approaches have not considered the fault events in CB and add complexity to the control structure system. Additionally, considering the similarity in the control structure of grid-connected converters, especially DC-link voltage controller, some methods including a Proportional-Integral (PI) controller in conjunction with a feed-forward controller [17], direct power control (DPC) [18], robust PI controller [19], and adaptive algorithms [20] have

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been suggested to enhance the reliability of DC link against sudden changes and disruptions. However, to address the above-mentioned challenges, these techniques have some drawbacks to be implemented on the D-STATCOM in practical applications. To be more precise, the designed control system prompts high fluctuation in grid currents, depends on the nominal conditions [17], and causes variable switching frequency resulting in introducing current harmonic components to the network [18]. Control methods used in [20] have properly produce reliable responses under sudden load variation; however, their gain tuning procedures are dependent on the CB capacitance, so capacitor variations or fault occurrence in DC-link CB will have adverse effects on their operation. Therefore, designing a control system that can alleviate these negative impacts on the device will be an obligation for a D-STATCOM under faulty conditions.

Without changing the basic controllers in the primary cascaded control structure, this paper proposes a regulation algorithm that monitors the power quality parameters, such as AC-side current THD and designates the DC-link voltage set-point to avoid entering to the over-modulation region under variations of DC-link capacitance.

The rest of the paper is organized as follows. In the Section 2, the relation between capacitance and the THD is described. Section 3 explores the D-STATCOM's model and the effects of capacitance reduction on the operational condition in comparison to a normal situation and proposes a control approach guaranteeing power quality criteria. The applicability of this approach is justified by simulation and experimental studies in Section 4 and Section 5, respectively. Finally, the paper concludes in Section 6.

II. EFFECT OF CAPACITANCE DEGRADATION ON THD

Fig. 1 shows the DC-link current (I_c) that is composed of switching and 6th components that have impact on the DC-link capacitance. A main constraint in designing of the converters is providing the proper AC-side current in the permissible THD zone that is specified by IEEE519 standard. To show the relation between the DC-link capacitance and AC-side current, one can calculate I_c as follows:

$$I_c = \sum_{k=1}^{\infty} I_{(6k)} + \sum I_{sw} \quad (1)$$

where $I_{(6k)}$ and I_{sw} show the 6th components and the switching current, respectively. The 6th components of this current are

$$I_{(6k)}(t) = C \frac{dV_{(6k)}(t)}{dt} \quad (2)$$

where $V_{(6k)}$ are the 6th components of voltage, and when connect to the AC terminal through the converter, they turn to $6k \pm 1$ components. In AC/DC converters, it could be shown that the 6th current components are calculated as [21]

$$I_{(6k)} = I_{rms} \frac{6|\cos\varphi|}{\pi(36k^2-1)} \sqrt{1+36k^2 \tan^2\varphi} \quad (3)$$

where $\cos\varphi$ is power factor and $I_{rms} = I_{peak}/\sqrt{2}$. Ignoring the ohmic loss of the converter, the power factor for a STATCOM could be approximately equal to 1, i.e. $\varphi \approx 90^\circ$. Hence, the 6th components of the AC current become

$$I_{(6k)} \approx I_{rms} \frac{1}{k\pi} \quad (4)$$

The 6th components of the DC-link voltage are built based on the 6th components of the DC-side current. Fig. 2 displays the AC-side voltage terminal of the converter that is composed of fundamental, switching harmonic, and $6k \pm 1$ harmonic components. The AC-side voltage terminal of a STATCOM is

$$V_t = V_1(t) + \sum V_{sw}(t) + \sum_{k=1}^{\infty} V_{(6k\pm 1)}(t) \quad (5)$$

where the 6th components are calculated as

$$\frac{I_{rms}}{k\pi} \sin(6k\omega t) = C \frac{dV_{(6k)}(t)}{dt} \Rightarrow |V_{(6k)}| = \frac{I_{rms}}{6k^2\omega\pi C} \quad (6)$$

Then, the terminal voltage will be

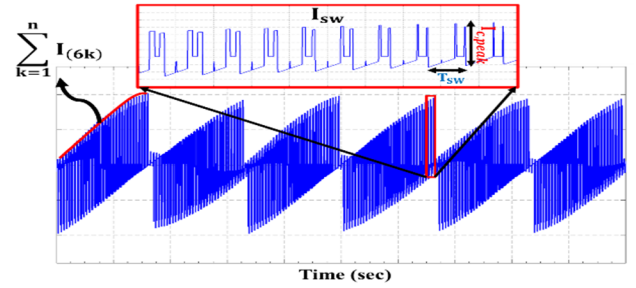


Fig. 1 DC-link current waveform with 10 kHz switching frequency

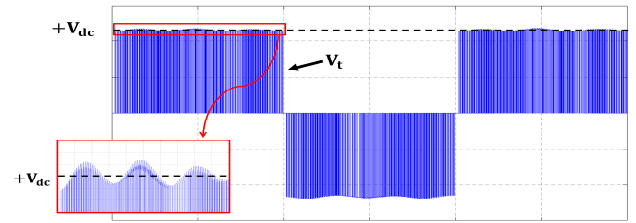


Fig. 2 D-STATCOM terminal voltage waveform

$$V_t = V_{(1)} + \sum V_{sw} + \sum_{k=1}^{\infty} \frac{I_{rms}}{6k^2\omega\pi C} \quad (7)$$

and the switching harmonic components are given by [22]

$$f_h = jf_{sw} \pm kf \quad (8)$$

when k is even, j is odd, and vice versa. The third term in the AC-side voltage terminal is stemmed from the equivalent load current at the DC-side. Considering the AC-side voltage terminal, the THD in the healthy situation is as follows:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} (V_{(h)}^2)}}{V_{(1)}} = \frac{1}{V_{(1)}} \sqrt{\sum V_{sw}^2 + \sum V_{6k}^2} \quad (9)$$

and in the faulty situation as:

$$THD = \frac{1}{V_{(1)}} \sqrt{\sum V_{sw}^2 + \sum \hat{V}_{6k}^2} \quad (10)$$

where $|\hat{V}_{(6k)}| = \frac{I_{rms}}{6k^2\omega\pi\hat{C}}$ and $\hat{C} = C - \Delta C$ is the DC-link equivalent capacitance under the degradation fault. Hence, if the DC-link capacitance is decreased (due to fault occurrence, aging, etc.), the amplitude of \hat{V}_{6k}^2 will be increased, and this will

lead to the increase of the AC-side current THD. The increase of the current THD from healthy to faulty situation is

$$\frac{\hat{V}_{6k}}{V_{6k}} = \frac{c}{\hat{c}} = \frac{c}{c-\Delta C} = \frac{1}{1-\frac{\Delta C}{C}} = \frac{1}{1-\alpha\%} \quad (11)$$

where α is the variation percentage in the capacitance. This paper proposes a new method that can maintain the THD in the standard zone through manipulating the modulation index and DC-link voltage, and is described in the next section.

III. MODIFICATION MECHANISM FOR A D-STATCOM

Considering the D-STATCOM structure in Fig. 3, the exchange active and reactive powers at PCC in a dq-frame calculated as follows [23]:

$$P = \frac{3}{2}(V_{sd}i_d + V_{sq}i_q) \quad (12)$$

$$Q = \frac{3}{2}(V_{sq}i_d - V_{sd}i_q) \quad (13)$$

where V_{sd} , V_{sq} , i_d , and i_q indicate direct and the quadrature components of the PCC voltage and current, respectively. The control system should provide a proper voltage at the VSC's terminals, V_t , through generating suitable voltage references for the pulse width modulation (PWM) modules. In a dq-frame [23], V_{td} and V_{tq} are calculated as:

$$V_{td} = L \frac{di_d}{dt} + Ri_d - L\omega i_q + V_{sd} \quad (14)$$

$$V_{tq} = L \frac{di_q}{dt} + Ri_q + L\omega i_d + V_{sq} \quad (15)$$

where L , R , and ω are the coupling inductance, coupling resistance, and angular frequency. Fig. 3 shows the prevailing control configuration, basic layer, used in a D-STATCOM. In this structure, the outer loop generates reference signals for the inner loop by regulating DC-link voltage (V_{dc}) and reactive power (Q), and the inner loop generates reference signals for the PWM by regulating i_d and i_q . Regarding the steady-state conditions ($V_{sq} = 0$), these set points will be as follows

$$i_d^* = I_{Loss} \quad (16)$$

$$i_q^* = -\frac{2}{3V_{sd}}Q^* \quad (17)$$

Additionally, i_d and i_q are equal to their set-points under steady-state; thus, in static mode, V_{td} and V_{tq} will be as follows

$$V_{td} = V_{sd} + \frac{2L\omega}{3V_{sd}}Q^* + RI_{Loss} \quad (18)$$

$$V_{tq} = \frac{-2R}{3V_{sd}}Q^* + L\omega I_{Loss} \quad (19)$$

If power loss is waived, modulation index ($m = \frac{V_t}{V_{dc}/2}$) in steady-state is calculated as follows:

$$m = \frac{4}{3V_{dc}^*V_{sd}} \sqrt{\left(\frac{9}{4}V_{sd}^2 + L\omega Q^*\right)^2 + R^2} \quad (20)$$

Since $L\omega$ is larger than R in practical application, we can ignore R and (20) becomes

$$m = \frac{6V_{sd}^2 + 4L\omega Q^*}{3V_{dc}^*V_{sd}} \quad (21)$$

It is obvious in (21) that the larger Q^* the larger modulation index when V_{dc}^* and V_{sd} are assumed to be a constant value. In this case, the D-STATCOM just regulates the exchangeable reactive power at the PCC, and the effect of both load and D-STATCOM on the PCC voltage is negligible. That being said, a linear model showing in (22) designates the relation between the modulation index and Q^* as follows:

$$m = \frac{2V_{sd}}{V_{dc}^*} + \frac{4L\omega}{3V_{sd}V_{dc}^*}Q^* \quad (22)$$

where $\frac{V_{sd}}{V_{dc}^*}$ and $\frac{L\omega}{V_{sd}V_{dc}^*}$ are constant. Regarding sinusoidal pulse width modulation (SPWM) technique, $m_{max} = 1$; thus, the maximum reactive power compensation is obtained by

$$Q_{max}^* = \frac{3V_{sd}(V_{dc}^* - 2V_{sd})}{4L\omega} \quad (23)$$

Note that (23) is more accurate if DC-link voltage, V_{dc} , is used instead of its set-point, especially when there is a considerable DC-link voltage ripple. It could be shown that DC-link voltage ripple has a great impact on the CB size installed in DC-link. Under VAR-compensation and in static and ideal mode, DC-link current could be calculated as follows:

$$i_c = C \frac{dV_{dc}}{dt} \quad (24)$$

where i_c and C are DC-link current and the equivalent capacitance of CB. In this inverter, the DC-link current variations is equal to the maximum current, $i_{c,peak}$, in half of a switching period [22]. Since AC current's peak is equal to reactive current component (reactive current reference) under VAR-compensation and static modes; hence, the relation between DC-link characteristics and demanding reactive power will be as follows:

$$i_c = \frac{C\Delta V_{dc}}{T_{sw}/2} \xrightarrow{i_{c,peak}=i_q^*} i_q^* = 2Cf_{sw}\Delta V_{dc} \quad (25)$$

Eq.(19)

$$\rightarrow |Q^*| = 3V_{sd}f_{sw}C\Delta V_{dc}$$

where f_{sw} is the switching frequency. In (27), V_{sd} and f_{sw} are constant, and therefore, Q^* is a function of CB capacitance and DC-link voltage ripple. More specifically, Q^* has a direct relationship with the multiplication of C and ΔV_{dc} . What is more, the envelope of the DC-link current displayed in Fig. 1 has a frequency that is six times that of the grid, and this envelope causes to generate the six harmonic component in the DC-link current, $I_{(6)}$. Using (17) and (24), $I_{(6)}$ becomes

$$I_{(6)} = C \frac{dV_{dc}}{dt} \xrightarrow{f_{(6)}=6f} I_{(6)} = 12Cf\Delta V_{dc} \quad (26)$$

$$\rightarrow |Q^*| = 18V_{sd}fC\Delta V_{dc}$$

Once Q^* is a constant value, the D-STATCOM's DC-link voltage ripple will increase as some of the capacitors in the CB fail because of aging, fuse failure, cell failure, etc. DC-link voltage ripple also has a direct relationship with AC side current ripple and current THD so that if it raises more than a specified value, the THD will be increased, and this lead to lessening the power quality compared with normal conditions [24], [25]. PI controllers is the most common controllers used in cascaded control structure, Basic layer, depicted in Fig. 3, and these controllers are highly reliant on the system's nominal

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conditions [26]. Hence, they cannot properly work on the degradation of CB capacitance (DCBC) from its nominal value. As a result, designing an advanced control system avoiding lessening of power quality, here the current THD, would be necessary.

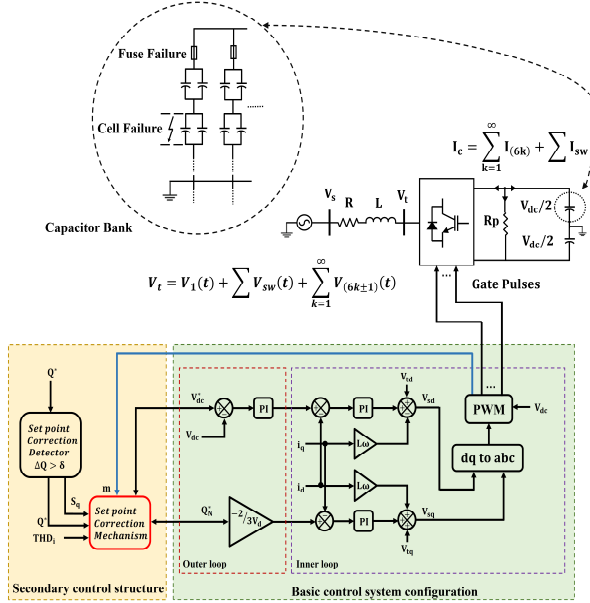


Fig. 3 Proposed Control Structure (Secondary and Basic layers)

Indicated in (21) and (25), both modulation index and DC-link voltage ripple could be regulated by Q^* in static modes. For $m=1$, one can obtain using (23), (25), and (26)

$$\Delta V_{dc,max} = \max \left\{ \frac{V_{dc}^* - 2V_{sd}}{3f_{sw}CL\omega}, \frac{V_{dc}^* - 2V_{sd}}{24fCL\omega} \right\} \quad (27)$$

In (27), the maximum DC-link voltage ripple, $\Delta V_{dc,max}$, is obtained under a normal condition, with no occurrence of DCBC. This indicates larger values of the Q^* results in increasing the DC-link voltage ripple, and this could then increase the normalized ripple current at the AC side, and thereby raise the current THD injected to the network at PCC [27], [28]. In addition, DC-link voltage ripple could be raised by the occurrence of the DCBC under a constant compensation rate, and thereby, the power quality indices, here the current THD, will be aggravated. Furthermore, the modulation index should not go to the over-modulation zone, $m > 1$, since this leads to distortion of the AC voltage profile at VSC's terminals, and this drastically increases the THD of the injected current to the grid. This usually occurs when D-STATCOM is forced to work in overload mode.

This secondary control system does not change the basic PI controllers and it only designates a new V_{dc}^* using Q^* and modulation index, DC-link voltage, and AC current THD, THD_i , measurements as shown in Fig. 3. The flowchart of the DC-link set-point modification mechanism is displayed in Fig. 4 that f and δ are the network frequency and detection level (2-5% nominal compensation rate). This upstream control system works based on static measurements of the system and it is slower than the downstream ones. In a static view, (21), (25) and (26) states that Q^* plays a key role in the amount of THD_i

through changing the $C\Delta V_{dc}$ and m . When THD_i gets more than an acceptable threshold in operational mode, the modification mechanism sets $V_{dc,1}^*$ to a new value bigger than the previous one, $V_{dc,0}^*$, and this leads to decreasing the modulation index in (21) and the DC-link voltage ripple that result in returning the THD_i in the standard range. Using this modification mechanism, the D-STATCOM continues compensating the reactive power and maintaining THD_i in the permissible value [29] to be connected to the network although it increases the switching loss and decreases the converter performance rate. Regarding this, the performance degradation should not be considered, that is, the new DC-link voltage set-point should not be chosen conspicuously larger than the previous one. This procedure guarantees the operation of the system under the DCBC fault until the next maintenance routine and avoids disconnecting of the system and emergency shut-down risen from the power quality lessening. To adjust $V_{dc,1}^*$, this algorithm indirectly uses the dependency of the DC-link voltage set-point, modulation index, and Q^* indicated in (21). Precisely, this mechanism starts correction of the DC-link voltage set-point using this fact that V_{td} and V_{tq} have fixed value under a fixed reactive power reference as indicated in (18)-(20). In fact, this algorithm measures Q^* in each operation period of itself ($\tau = 1/f$) and calculate the regulation constant, $K_{m,V_{dc}}$, using (21) as follows:

$$K_{m,V_{dc}} = mV_{dc}^* = \frac{6V_{sd}^2 + 4L\omega Q^*}{3V_{sd}} \quad (28)$$

where $K_{m,V_{dc}}$ has a fixed value for a fixed reactive power reference. In this case, m_{max} is considered to be unit and m_{min} is calculated in the no load operation, $Q^* = 0$, as follows

$$m_{min} = \frac{2V_{sd}}{V_{dc,N}^*} \quad (29)$$

where $V_{dc,N}^*$ is the DC-link voltage set-point in the healthy conditions. In a healthy scenario, where the modulation index and the measured THD_i are in the admissible values, the modification mechanism does not change V_{dc}^* , and the modulation index varies from m_{min} to unit to compensate the required Q^* . In this case, the command $V_{dc,1}^* = V_{dc,N}^*$ is sent to the DC-link voltage regulation loop. If the modulation index gets bigger than unit and THD_i violates the standard, then the DC-link voltage set-point correction mechanism designates $V_{dc,1}^*$ based on $m = 1$ (maximum permissible modulation index). If $m_f = 1 + \Delta m$, the modulation index in faulty case, then $V_{dc,1}^*$ is calculated as follows:

$$V_{dc,1}^* = k(1 + \Delta m)V_{dc,0}^* \quad (30)$$

Where k is a design factor and Δm is the difference of modulation index from the unit, and $V_{dc,0}^*$ is the previous DC-link voltage set-point. Furthermore, D-STATCOM should have a fast dynamic to provide desired demanding reactive power at transient modes, so this algorithm also prioritizes this function to its basic function so that if the new Q^* is bigger than the previous one in the capacitive mode, it does not change the corrected DC-link set-point for this new Q^* and tries to regulate the THD_i after the reactive power regulation transient modes. If

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not, this algorithm sets the DC-link voltage reference to the DC-link voltage set-point in the healthy mode and then tries to check THD_i and regulate V_{dc}^* after the transient modes. This operation is activated by the detection level, δ . The modification block stops the running functions as soon as reactive power reference changes touch the detection level, and designates $V_{dc,1}^* = V_{dc,0}^*$ for increasing of the compensation rate and $V_{dc,1}^* = V_{dc,N}^*$ for the decreasing scenario in 25 cycles (25τ). In this time interval, the THD_i might not be in the acceptable range. Note that the modification procedure returns to its basic function after the specified time for transient modes in the reactive power reference change.

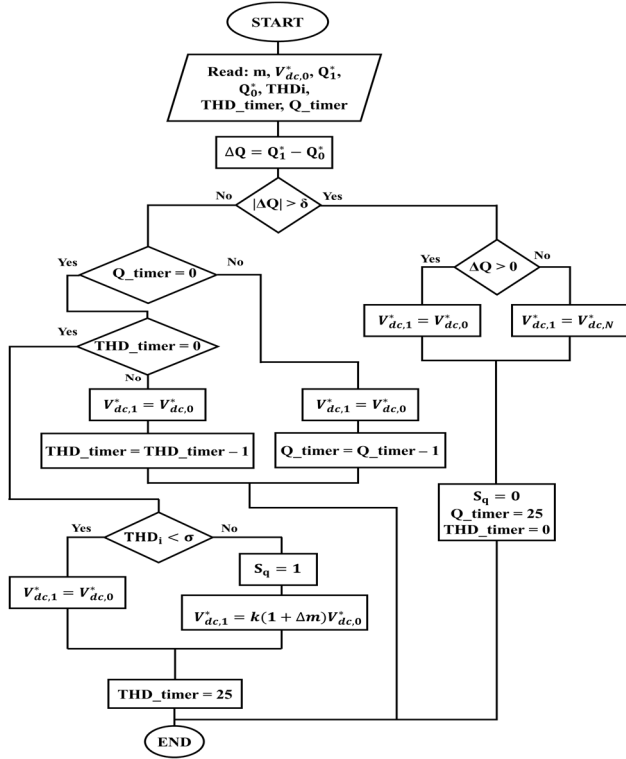


Fig. 4 Modification mechanism in each operation cycle (τ)

IV. SIMULATION RESULTS

The proposed method was tested and compared with a common basic structure using Matlab/SimPowerSystem. In the simulation studies, it is assumed that a variable reactive load is connected to the 400 V distribution lines, and a 5 kVAr D-STATCOM was installed at PCC to provide the demanding reactive power. Based on the D-STATCOM's full compensation rate and requiring power quality criteria, the parameters of this equipment are designed and shown in Table I. Two scenarios were considered to analyze the behavior of the proposed control system and the primary one. In the first scenario, it was assumed that the inductive load starts absorbing of 4.5kVAr reactive power from the network at $t = 1s$, then increases to 5kVAr at $t = 2s$ and finally decreases to 4kVAr at $t = 4s$. In the second scenario, the reactive load has the same behavior in the first, and it is only assumed half of the capacitors in one of the CB legs, shown in Fig. 3, suddenly failed at $t =$

0.5s, and thereby 33 percent of the CB capacitance is reduced compared with the scenario 1.

In the rest of this paper, scenario 1 and scenario 2 are specified by \mathcal{H}_0 (healthy) and \mathcal{H}_1 (faulty), respectively. For both healthy and faulty scenarios, tuning of the PI controllers' coefficients is based on criteria mentioned in literature [26] so the proportional and integral gains are 8 and 800 for the inner loops, and 0.1 and 10 for outer loop.

Shown in Fig. 5-a, the D-STATCOM tracks properly the demanding reactive power set-point, and the THD_i , Fig. 5-d, is less than 5% throughout the \mathcal{H}_0 experiment.

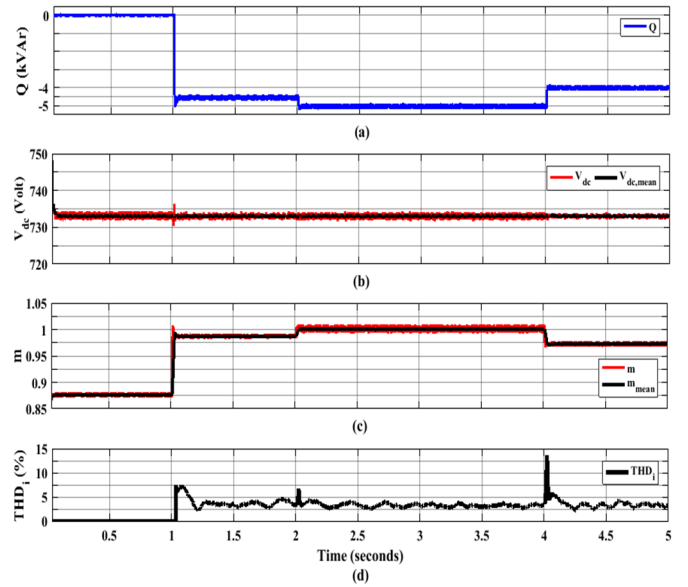


Fig. 5 a) Reactive power; b) DC-link voltage ripple; C) modulation index; and d) THD_i ; under the healthy scenario

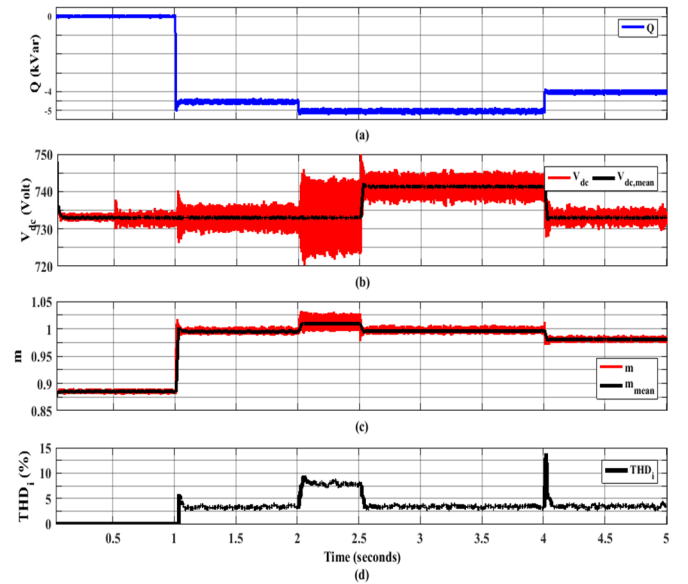


Fig. 6 a) Reactive power; b) DC-link voltage ripple; C) modulation index; and d) THD_i ; under the faulty scenario

TABLE I
THREE PHASE D-STATCOM SYSTEM PARAMETERS

Symbol	Value	Description
S_n	5kVA	Rated Power
V	400V	Nominal Bus Voltage (line-to-line)
F	50Hz	Fundamental Frequency
f_{sw}	10kHz	Switching Frequency
$V_{dc,0}^*$	733V	DC-link Voltage
L	12.8mH	Inductance of Output Filter
R	0.4Ω	Resistance of Filter inductance
C	150μF	Capacitance of DC-link

TABLE II
SYSTEM PARAMETERS IN FAULTY SCENARIO

Compensation rate (VAr)	4500	5000	5000	4000
Set-point change (S_q)	0	0	1	1
Modulation index	0.994	1.009	0.996	0.981
DC Voltage ripple (V)	10	30	12	8
THD_i (%)	3.33	7.67	3.61	3.34

Note that when the reactive power set-point is changed, the THD_i gets bigger than the admissible threshold ($\sigma = 5\%$) [29] in Fig. 5-d, and this is a normal behavior because of transient modes in these times. Slightly obvious in Fig. 5-b, the DC-link voltage ripple gets bigger when the system must inject higher values of reactive power to the network and the capacitance of the CB is a fixed value.

The controlled variable of the D-STATCOM under the \mathcal{H}_1 scenario are displayed in Fig. 6. Similar to the healthy experiment, the system appropriately follows the reactive power variations, indicated in Fig. 6-a. Shown in Fig. 6-b, DC-link voltage ripple starts increasing as soon as the fault occurs in the CB at $t = 0.5s$, and its amplitude gets bigger under reactive compensation modes. Conspicuously observable, the DC-link voltage under the faulty scenario ripple gets much bigger than that of under the healthy scenario. In addition, the modulation index slightly increases in the faulty modes compared to healthy ones indicated in Fig. 5-b and Fig. 6-b. Indicated in Table II, these two phenomena occurred under the \mathcal{H}_1 experiment cause to drastically increase the THD_i from 2s to 2.5s while the D-STATCOM provides 5kVAr at PCC. At $t = 2.5s$, the modification mechanism assigns a bigger DC-link voltage reference value according to (31), and therefore, this leads to decreasing the modulation index and the DC-link voltage ripple. This set-point changing procedure rises the switching loss slightly, but this increment rate is negligible since the difference between the new DC-link voltage set-point and the previous one is approximately 8V as shown in Fig. 6-b, and this could be ignored in return of favorable outcomes that are gained by applying the modification mechanism. This secondary control, in addition, decreases the DC-link voltage ripple considerably, and this is in favor of the D-STATCOM's protection under the faulty cases. Displayed in Fig. 6-b, the DC-link voltage set-point returns to the nominal reference at $t = 4s$ because the reactive power set-point is decreased, and the modification mechanism checks that the system can provide the demanding reactive power with the nominal DC voltage, $V_{dc,N}^* = 733V$, to decrease the switching loss and increase the converter efficiency. The THD_i waveform in Fig. 6-d experiences some instantaneous impulses at $t = 1s, 2s, \text{ and } 4s$

because of the variations in the reactive power set-point and the associated transient modes.

V. EXPERIMENTAL VALIDATION

A. Laboratory D-STATCOM Prototype

To validate the proposed method experimentally, a 5kVAr three-phase two-level D-STATCOM is implemented as shown in Fig. 7. The D-STATCOM's parameters are designed and given in Table I, similar to the simulation section. A simulator has been designed using ATmega32 to artificially implement the occurrence of the degradation in DC-link capacitance. Depicted in Fig. 8, one can cut off everywhere of CB, in both levels. Similar to the simulation results, here we implement the healthy and faulty scenarios, and the only difference between the simulation and implementation sections is the time length of the experiments. Indeed, the load variations occur at $t = 10s, 20s, \text{ and } 40s$ for 4.5kVAr, 5kVAr, and 4kVAr, respectively. Since the lowest sampling rate of THD_i in the power analyzer is equal to 1s, we consider 250 cycles for set-point changing step in the reactive power and 250 cycles for the current THD correction stage to show the different stages in the algorithm operation clearly, while this algorithm can operate in lower time zones similar to the Simulink results.

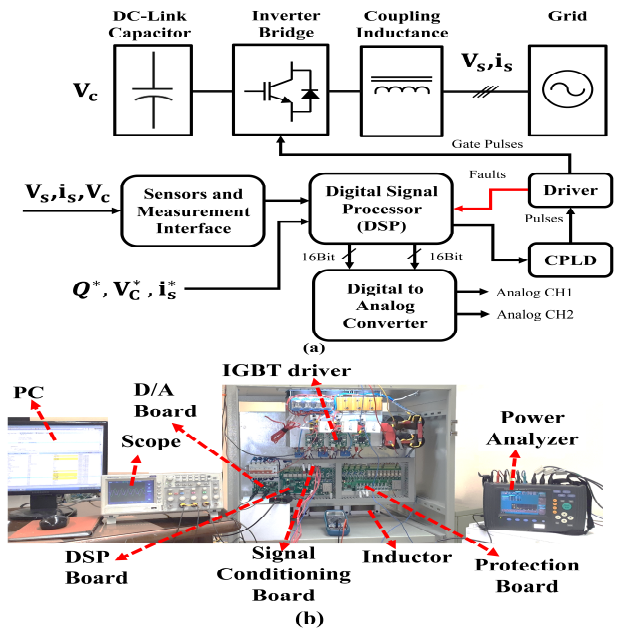


Fig. 7. D-STATCOM-5kVAr a) Block diagram b) Experimental setup

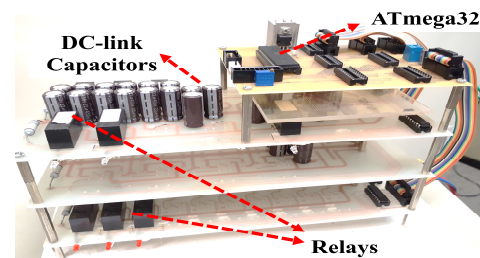


Fig. 8 CB and Simulator for capacitance variations

B. Experimental Results

Fig. 9 shows the injected reactive power to the grid in the steady-state mode for healthy mode. The control system rapidly tracks the set-point changes and the modification mechanism does not change the compensation rate of the system even though the THD_i is in the permissible zone, displayed in Fig. 10. Indicated in Table III, the harmonic components under different load set-points is less than 5% and acceptable according to the IEEE519 standard [29]. Shown in Fig. 11, the modulation index for 5kVAr approximately reaches its maximum value and has a higher ripple than the others. Even though these variations, near to the maximum modulation index, prompt the converter to operate in the over-modulation region, the THD_i is not increased conspicuously and the D-STATCOM properly provides the demanding reactive power. This also justifies the simulation section results and the relation between the demanding reactive power and DC-link voltage ripple in (27). To evaluate the operation of the modification mechanism under DCBC fault, the scenario \mathcal{H}_1 is implemented on the set up using the DSP microcontroller and the ATmega32 board. The profile of the compensated reactive power is displayed in Fig. 13. Shown in Fig. 13, similar to the healthy scenario, the control system tracks the reactive power reference and prioritizes the variation of the set-point over the current THD correction. As shown in Fig. 14, the THD_i is in the allowable zone, less than 5%, for 4.5kVAr; hence, the modification mechanism does not change the DC-link voltage reference. In 5kVAr compensation, this adjustment algorithm firstly lets the system to follow the reactive power reference, for 5s. Then, it activates the current THD correction procedure

to decrease the THD_i , and return it to the allowable values. Clearly obvious, setting the new set-point for DC-link voltage decreases not only the THD_i but also the DC-link voltage ripple displayed in Fig. 15. Indeed, such a ripple had been 40V before the THD correction mechanism started its operation, and it got 20V after applying this mechanism through the modification mechanism.

Fig. 16 indicates that the ripples got bigger at $t = 5s$, when half of the capacitors in one arm were disconnected from the CB of the DC link, compared to the time zone before $t = 5s$, and the voltage ripple profile also shows this ripple is increased compared to the healthy scenario shown in Fig. 12. Once the reactive power set-point changes from 5kVAr to 4kVAr, the DC-link set-point modification mechanism immediately change the DC-link voltage reference to the normal reference, $V_{dc,N}^* = 733V$, since the new Q^* is decreased from the previous one, and the algorithm wants to check the possibility of a lower DC-link set-point to achieve the control and power quality standards. In fact, this function causes to decrease the switching loss of the converter in order to enhance its performance when a decrease occurs in the compensation rate. The current THD profile in Fig. 14 indicates that applying $V_{dc,N}^*$ under 4kVAr compensation rate guaranteed being of the THD_i in the admissible zone; hence, this decrease in the V_{dc}^* has improved the converter efficiency under the \mathcal{H}_1 scenario.

Similar to the healthy scenario, the modulation index profile also shows in Fig. 16 for the faulty experiments. Displayed in Figs. 15-16 and, Table IV, the modification mechanism tries to decrease the modulation index by raising the DC-link voltage reference to maintain the current THD in the standard zone.

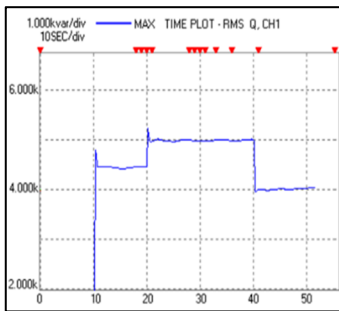


Fig. 9 Injected reactive power at the PCC under \mathcal{H}_0 scenario

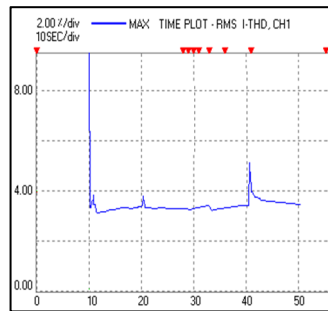


Fig. 10 THD_i profile under \mathcal{H}_0 scenario

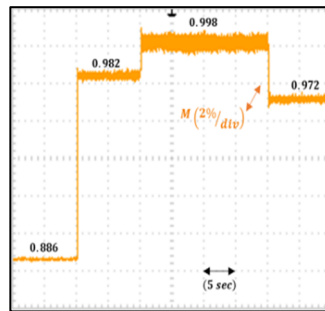


Fig. 11 Modulation index profile under \mathcal{H}_0 scenario

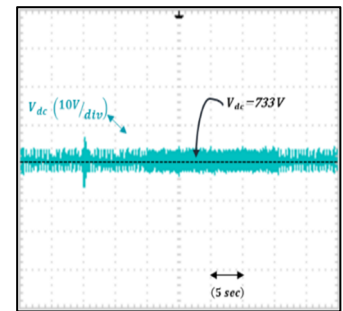


Fig. 12 DC-link voltage ripple under \mathcal{H}_0 scenario

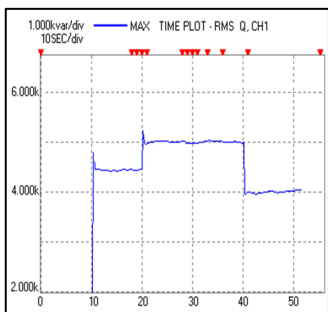


Fig. 13 Injected reactive power at the PCC under \mathcal{H}_1 scenario

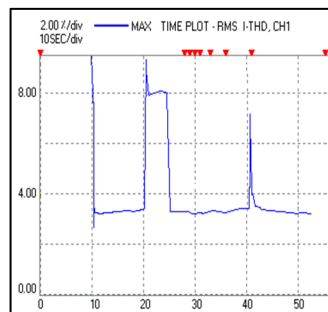


Fig. 14 THD_i profile under \mathcal{H}_1 scenario

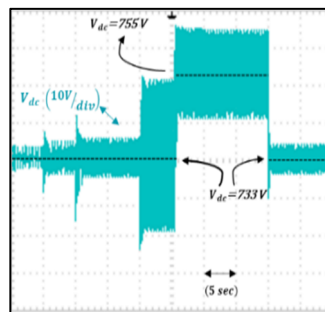


Fig. 15 DC-link voltage ripple under \mathcal{H}_1 scenario

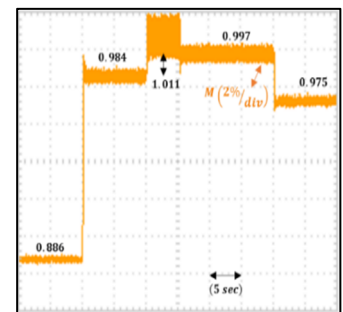


Fig. 16 Modulation index profile under \mathcal{H}_1 scenario

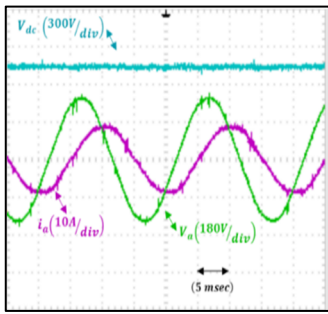


Fig. 17 DC-link voltage (blue), voltage (green) and current of phase a (purple) in 4.5kVAr compensation and \mathcal{H}_1 scenario

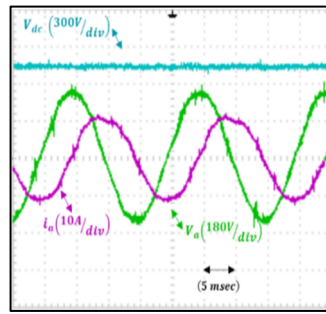


Fig. 18 DC-link voltage (blue), voltage (green) and current of phase a (purple) in 5kVAr compensation and \mathcal{H}_1 scenario, before starting the mechanism

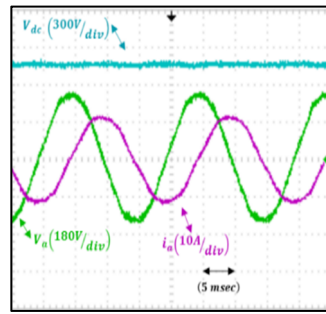


Fig. 19 DC-link voltage (blue), voltage (green) and current of phase a (purple) in 5kVAr compensation and \mathcal{H}_1 scenario after starting the mechanism

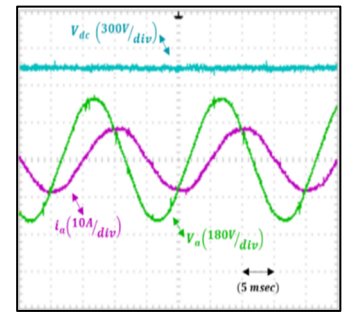


Fig. 20 DC-link voltage (blue), voltage (green) and current of phase a (purple) in 4kVAr compensation and \mathcal{H}_1 scenario

TABLE III
SYSTEM PARAMETERS IN HEALTHY SCENARIO

Compensation rate (VAr)	4500	5000	4000
DC-link set-point change	0	0	0
Modulation index	0.982	0.998	0.972
DC-link voltage ripple (V)	15	18	15
THD _i (%)	3.6	3.6	3.8

TABLE IV
SYSTEM PARAMETERS IN FAULTY SCENARIO

Compensation rate (VAr)	4500	5000	5000	4000
DC-link set-point change	0	0	1	1
Modulation index	0.984	1.011	0.997	0.975
DC-link voltage ripple (V)	22	56	30	14
THD _i (%)	4.1	8.0	4.8	3.9

Figs. 17-20 show the voltage and current waveforms of the system under different compensation and the faulty scenario. The distort current waveform in Figs. 17-18 and the corrected one in Figs. 19-20 show the impact of modification mechanism in decreasing of the THD_i by increasing the DC-link voltage.

VI. CONCLUSION

This paper explores the adverse effects of the decline in the capacitance of the capacitor bank of the DC-link of a D-STATCOM. It shows that occurrence of such a fault causes to increase DC-link voltage ripple and modulation index that basic control system cannot properly manage the power quality indices. To address this issue, this paper proposes a secondary control system augmented to the basic one and changes the DC-link voltage set-point so that the current THD returns to the permissible zone. It was shown that this system does not change the basic controllers, keeps the compensation rate of the D-STATCOM at its nominal rate, and just works in steady modes. The simulation and experimental results verified the applicability of this algorithm under capacitance degradation fault while the common structure suffer from regulating the current THD and power quality indices. These results also show that the proposed secondary control layer tries to provide the reactive power and satisfy the THD criteria through minimizing the DC-link voltage ripple and modulation index through choosing the lowest DC-link voltage reference.

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