AALBORG UNIVERSITY

DENMARK

A Simplified On-state Voltage Measurement Circuit for Power Semiconductor Devices

Peng, Yingzhou; Wang, Huai

Link to publication from Aalborg University

A Simplified On-state Voltage Measurement Circuit for Power Semiconductor Devices

Yingzhou Peng, *Member, IEEE*, Huai Wang, *Senior Member, IEEE*

Abstract—**This letter proposes a simplified converter-level on-state voltage measurement circuit for power semiconductor devices, without an external power supply and self-power circuit. It has a reduced component count and circuit complexity, and retains the plug-and-play feature, comparable measurement accuracy, and dynamic response as recently reported methods. A proof-of-concept prototype is developed and tested for a three-phase inverter application.**

Index terms— Power semiconductor, condition monitoring, converter-level, on-state voltage, reliability.

I. INTRODUCTION

The on-state voltage is considered as a critical parameter for power semiconductors (e.g., $V_{CE,sat}$ of IGBT, $V_{ds,on}$ of MOSFET, and V_F of Diode). It is widely used as an indicator for device junction temperature estimation [1] and health monitoring [2].

Various circuits have been proposed to measure the on-state voltage of power semiconductor devices. They can be divided into component-level [2–5] and converter-level methods [6, 7]. The component-level circuits are connected to the two power terminals of individual power semiconductor devices, i.e., the collector-emitter of an IGBT, the drain-source of a MOSFET, or the anode-cathode of a power diode. For a typical three-phase inverter as shown in Fig.1(a), six sub-circuits are required to obtain the on-state voltages of the six power switches and six diodes. Moreover, in [2–5], a power supply in the range of several volts is needed for voltage clamping. It implies that three isolated bipolar power supplies are needed for a three-phase inverter application. Converter-level methods are recently proposed to overcome the challenge in complexity and accessibility. They are demonstrated by a single-phase inverter and three-phase inverter, respectively, in [6] and [7]. The measurement circuit in [6] is connected to the middle-point of each phase-leg only. It has a single bipolar power supply and a reduced component count compared to the methods in [2–5]. Moreover, its voltage rating is scalable by changing the number of depletion MOSFETs and diodes connected in series, respectively. A self-power scheme is proposed in [7], to replace the bipolar power supply, enabling a plug-and-play

Y. Peng and H. Wang are with the Department of Energy Technology, Aalborg University, Aalborg, Denmark (email: ype@et.aau.dk, hwa@et.aau.dk). (*Corresponding author: Huai Wang*)
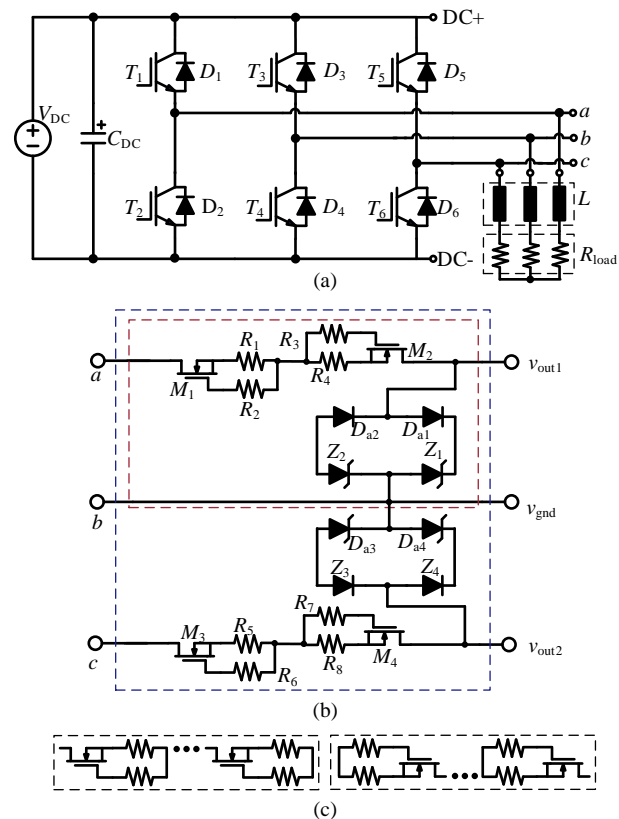

Fig. 1. Implementation of the proposed circuit: (a) three-phase inverter; (b) topology of the proposed on-state voltage measurement unit: for a single-phase inverter (red dash rectangle) and a three-phase inverter (blue dash rectangle); (c) voltage scalability.

solution. Nevertheless, the main component count, excluding the replaced power supply, is increased by 50% compared to the circuit in [6].

As a continuous research of [6, 7] for exploring solutions to eliminate the external power supply and self-power circuit, it is found that a component-level power-supply-less on-state voltage measurement circuit is given in [8]. The method is implemented for a single device application. It would be possible for the three-phase inverter application by extending the circuit. Nevertheless, there are two drawbacks: 1) the circuit complexity is still comparable to that of [2] and [7], as discussed later in Section II; and 2) the maximum voltage that can be measured is limited by the voltage capability of the depletion MOSFET, which cannot be scaled up by connecting multiple depletion MOSFETs in series.

This letter discloses part of a patent application [9] on a new converter-level on-state voltage measurement circuit without any external power supply and self-power scheme. It has the following advantages: 1) significantly simplified circuit and reduced input-output terminals compared to [6, 7]; and 2) retains the plug-and-play feature and voltage scalability of the method in [7], and comparable measurement accuracy of the method in [2].

II. PROPOSED MEASUREMENT CIRCUIT

A. Function analysis

Fig.1(b) shows the proposed on-state voltage measurement circuit. For three-phase inverter application, it has four depletion MOSFETs (M_1 - M_4), which are mA-level normally-on devices and exhibit different impedance by controlling its source-connected and gate-connected resistors when it is in operation. The bipolar clamping voltage is obtained through Zener diodes Z_1 - Z_4, instead of power supply or self-power circuit. The diodes D_{a1} - D_{a4} are used to protect these Zener diodes from forward conduction. For the sake of simplicity, the following analysis is for half of the measurement circuit in the red dash-rectangle shown in Fig.1(b).

When the input voltage is higher than V_Z+V_{D1}, Z_1 operates at reverse-clamping mode and its leakage current forms a voltage drop in R_1, which makes M_1 to operate at high-impedance mode. Then, v_{out1} is clamped to:

$$v_{out1} = V_Z + V_{D_{a1}} \qquad (1)$$

When the input voltage is within the range between $-V_Z$-V_{Da2} and V_Z+V_{Da1}, D_{a1}, D_{a2}, Z_1 and Z_2 are all blocked. At this moment, there is only the reverse leakage I_{Leak} of Zener diodes flowing through this circuit, which is a μA-level current. Therefore, the voltages across R_1 and R_4 are in mV-level, which means M_1 and M_2 are in on-state. As a result, the voltage drops of MOSFETs and resistors can be neglected, and v_{out1} equals to v_{ab} at this situation as:

$$v_{out1} = v_{ab} - I_{Leak}(2R_{dson} + R_1 + R_4) \approx v_{ab} \qquad (2)$$

When the input voltage is lower than $-V_Z$-V_{Da2}, Z_2 operates at reverse-clamping mode. Similarly, the leakage current of Z_2 leads to a voltage drop in R_4, and forces M_2 to operate at high impedance-mode. Therefore, v_{out1} is clamped to:

$$v_{out1} = -V_Z - V_{D_{a2}} \qquad (3)$$

To sum up, the function of the proposed circuit is to block the voltage higher than V_Z+V_{Da1} and lower than $-V_Z$-V_{Da2}, while passing the voltage within the boundaries.

In practical implementation, the input voltage ranges of the measurement circuit are scalable by connecting different number of depletion MOSFETs in series as shown in Fig.1(c).

TABLE I
NUMERIC COMPARISON BETWEEN EXISTING SOLUTIONS AND PROPOSED
CIRCUIT FOR A THREE-PHASE INVERTER APPLICATION.

Items	Ref.[2]	Ref.[8]	Ref.[6]	Ref.[7]	Proposed
Depletion MOSFET	6	6	4	6	4
Diode	18	12	8	12	8
Resistor	6	6	8	10	8
Power supply	3	0	1	0	0
Output signal	6	6	4	4	2
Floating ground	3	3	1	1	1

Note: the circuits in [2] and [8] are extended to a three-phase inverter application for the purpose of comparison.

B. Implementation in Three-Phase Inverter

The proposed circuit is demonstrated by connecting to the middle-point of each phase-legs in the three-phase inverter shown in Fig.1. According to the detailed explanations in [7], the output voltages v_{ab} and v_{cb} retain the on-state voltage information of all the six IGBTs and six diodes with both SPWM and SVPWM schemes. Taking the devices in phase a and b as an example, the output voltage v_{ab} includes the on-state voltages of T_1-T_4 and D_1-D_4. Likewise, the situations for the devices in other bridges can also be derived. In the rest of this paper, $V_{CE,satx}$ denotes the on-state voltage of T_x, V_{Fx} denotes the forward voltage of D_x.

In conclusion, with the proposed circuit, the positive and negative DC-link voltages in v_{ab} or v_{cb} can be clamped to V_Z+V_{D2} and $-V_Z$-V_{D1}, respectively. Therefore, the on-state voltage can be measured at the outputs. Here the clamping voltage can be changed by using the Zener diode with different zener voltages to meet the demand of different applications.

C. Comparisons with existing solutions

Fig.2 compares the number of input and output terminals between the proposed circuit and those in [2–8] applied for the three-phase inverter. v_{T1}-v_{T6} contain the on-state voltage information of T_1-T_6, respectively. v_{gnd}, v_{gnd1}-v_{gnd3} are the floating grounds in the respective solution. As discussed in [6, 7], each of the outputs v_{o1}-v_{o4} contains the on-state voltage information of two IGBTs and two diodes. It can be noted that the proposed circuit reduces the total number of input and output terminals to six only. It is the simplest solution for a three-phase inverter application to our best knowledge. The specific comparisons listed in Table I shows that the total component count of the proposed circuit is the lowest. In practical applications, Analog-to-Digital Conversion (ADC) or galvanic isolation may be required. It implies that the proposed circuit requires the least ADC channels and signal isolations, which are additional merits in terms of circuit complexity and cost.

III. EXPERIMENTAL VERIFICATION

The physical realization of the proposed circuit is shown in Fig.3(a). The size of the circuit inside this prototype is 3.5*3.5 cm with one-side PCB design. The specifications of the used components are listed in Table II and the component selection is discussed later.
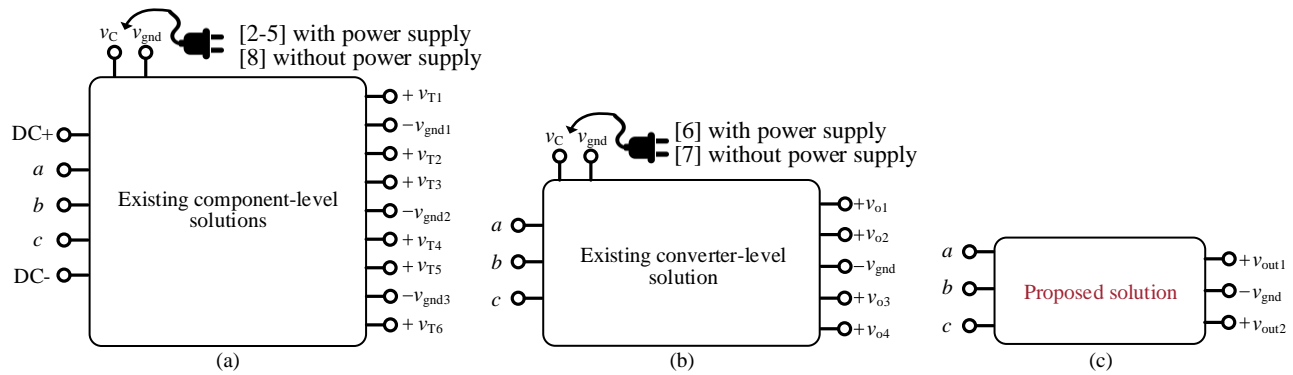
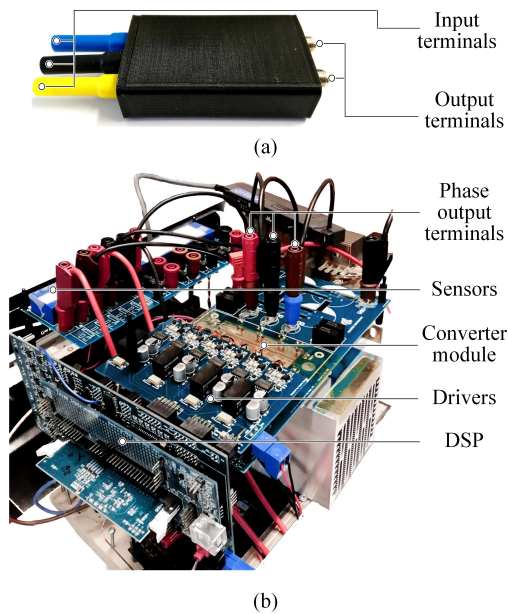Fig. 2. Circuit comparison of the existing solutions and the proposed solution for a three-phase inverter.

Fig. 3. Experimental setup: (a) prototype of the proposed on-state voltage measurement circuit; (b) three-phase inverter demonstrator.
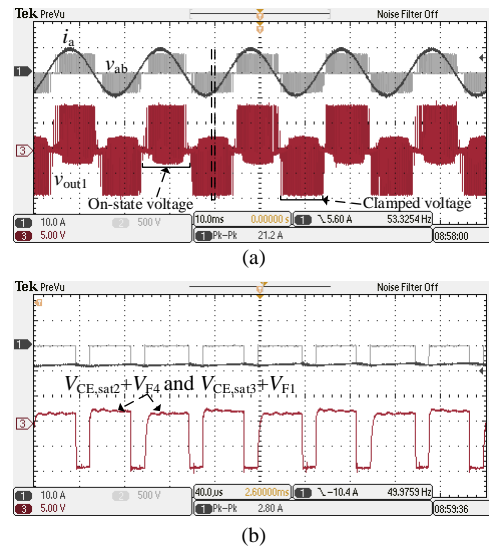

Fig. 4. Measured waveforms from the three-phase inverter and proposed circuit: (a) v_{out1} along with output current i_a and voltage v_{ab} from phase a and b; (b) zoom-in of the dash rectangle part in Fig.4(a) .

TABLE II
SPECIFICATION OF THE PROPOSED CIRCUIT FOR A 400 V THREE-PHASE INVERTER CASE STUDY.

Components	Product	Rating	Package
$R_{1,4,5,8}$	3.3 kΩ	1/8 W	SMD (0805)
$R_{2,3,6,7}$	1 kΩ	1/8 W	SMD (0805)
D_{a1-a4}	BAS70-04	70 V/70 mA	SOT-23
Z_{1-4}	1SMA4739 R3G	1.25 W	SMA
M_{1-4}	BSS126	600 V/21 mA	SOT-23

A three-phase inverter demonstrator is developed as shown in Fig.3(b), with DC-link voltage by 400 V, peak output current by 10 A, and switching frequency by 10 kHz. For simplification, only the on-state voltages of T_1-T_4 and D_1-D_4 extracted from v_{ab} are given in this letter as shown in Fig.4, including the output currents i_a, output voltage v_{ab}, and v_{out1}. It can be seen that the measured on-state voltage shows variation with the sinusoidal i_a. Further, the zoom-in of the dash-rectangles

area in Fig.4(a) is presented in Fig.4(b), showing that the $+V_{dc}$ and $-V_{dc}$ in v_{ab} are clamped to $V_Z + V_D$ and $-V_Z - V_D$, respectively. While, the on-state voltages of T_1-T_4 and D_1-D_4 are retained in v_{out1}. Overall, the on-state voltages of all power semiconductors in this three-phase inverter are detectable in two signals (v_{out1} and v_{out1}) separately. It should be noted that the $V_{CE,sat3} + V_{F1}$ and $V_{CE,sat2} + V_{F4}$ alternatively exist in Fig.4(b), for example. They can be separated by processing the measured results further, which is not covered by this letter.

The measured transient of on-state voltage is given in Fig.5(a), implying that the proposed circuit can follow the change of v_{ab} from negative DC-link voltage to on-state voltage very well. It should be noted that the response time of the proposed circuit is dependent on the charging process of the parasitic capacitances of D_{a1}-D_{a4} and Z_1-Z_4. In addition, since the MOSFETs have a fixed gate voltage when they operate in high-impedance mode, which means the lower source-connected resistances $R_{1,4,5,8}$ can cause higher operating cur-
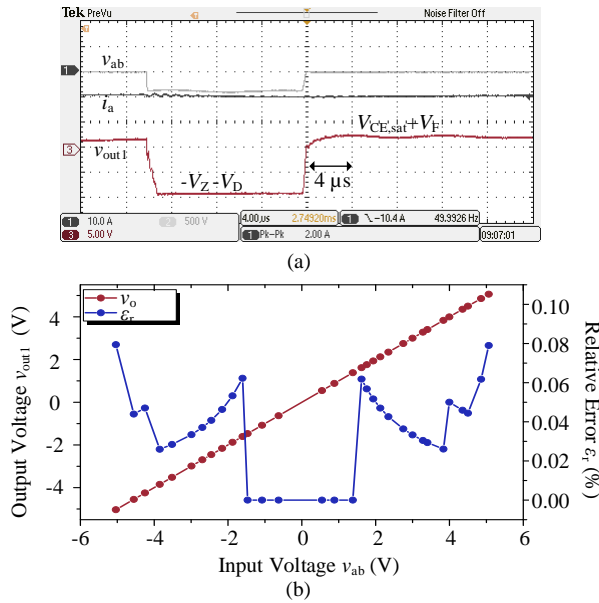
Fig. 5. Performance testing of the proposed circuit: (a) dynamic response testing in the three-phase inverter; (b) accuracy testing with an input voltage from -5 V to +5 V.

Fig. 6. Response time testing of the proposed circuit with different source-connected resistances in response to a step-change input voltage from -5 V to +5 V: (a) step-up; and (b) step-down.

rent I_M and hereby faster dynamic response. However, it can also lead to higher power consumption when the MOSFETs are bearing DC-link voltage. Thus, there is a trade-off between response time and power consumption. For example, in this case study, the gate voltage of the selected MOSFETs is -1.1 V in high-impedance mode according to experimental test. If $R_{1,4,5,8}$ are selected as 3.3 kΩ, 1.8 kΩ, or 1 kΩ, I_M (i.e., the charging current) is 333 μA, 611 μA, or 1.1 mA, respectively. At the same time, the corresponding response time in response to a step-change input signal from -5 V to +5 V is about 800 ns, 500 ns, or 300 ns, respectively, according to the experimentally

measured results as shown in Fig.6. In conclusion, with a 3.3 kΩ source-connected resistance and 400 V DC-link voltage in this case study, the response time and power consumption are 800 ns and 133 mW, respectively. In addition, the gate-connected resistances $R_{2,3,6,7}$ can affect the switching time of the applied MOSFETs as well as the response time of the proposed circuit. Therefore, they can be reduced further if the response time is not short enough for a specific application.
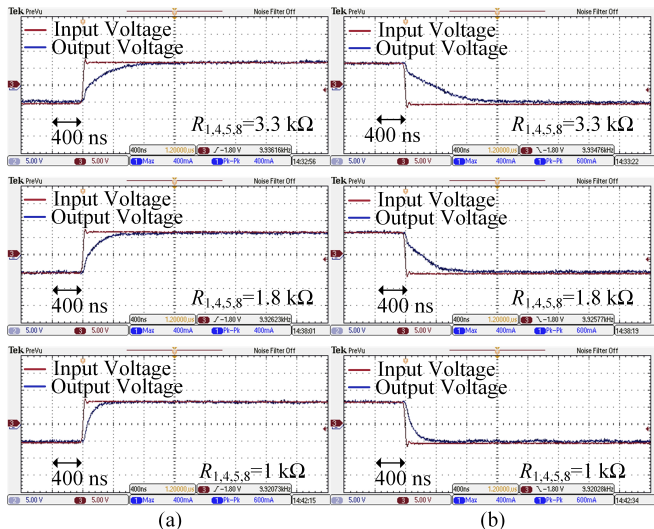
Fig.5(b) gives the accuracy performance of the proposed circuit tested with a DC input voltage from -5 V to +5 V. The maximum error is limited to 0.08% with an absolute error by 4 mV, which is much lower than the method in [7] ($\leq \pm 2\%$), and comparable with the method in [2] ($\leq \pm 0.1\%$) based on the experimental test with a DC input voltage from 0 V to +5 V. With the selected Zener diodes, the reverse leakage current is less than 0.5 μA. Also, It is known that R_{dson} of MOSFETs $\leq$ 700 Ω and $R_{1,4,5,8}$ = 3.3 kΩ, the maximum measurement error is 4 mV in this case study. Meanwhile, higher input voltage can cause higher leakage current, and thereby higher error, which agrees with the results shown in Fig.5(b). Moreover, Due to such low operating current and the extreme low temperature-dependency of resistance (e.g., less than ± 100ppm/K), the impact of the temperature-dependency of MOSFET on the measurement accuracy of the proposed circuit can be neglected.

A 14-bit ADC is used to acquire the on-state voltages of T_1-T_4 and D_1-D_4 with 10 kHz sampling frequency, as shown in Fig.7. The data acquisition is carried out once the inverter operates at current freewheeling mode. As such, the on-state voltage can be exactly obtained, and the clamped voltage is excluded. Over one fundamental period, $V_{CE,sat}$ and V_F appear with different combinations at different time instants, and alter along with the sinusoidal current. It can be derived that the proposed solution can obtain the on-state voltage of all power devices in a three-phase converter over one fundamental period. As discussed in [6], depending on the purpose of using the measured data, the separation of the on-state voltages between the pairs of IGBT and diode shown in Fig.7 may be needed for some specific applications (e.g., junction temperature estimation). It is a further data processing step based on the measured raw data and software algorithm, which is not covered in this letter.

Thereafter, in every fundamental period, the on-state voltages under the peak current are extracted at three different heatsink temperature-levels T_h as shown in Fig.8. During the operation, the peak current of inverter may fluctuate at a range (e.g., 9.9-10.1 A), instead of a fixed value. Therefore, there is a variation by about 10 mV in the extracted results. The measured on-state voltage is linearly increased with the increasing T_h, which verifies that the proposed circuit can sense the change of on-state voltages. It is worth mentioning that the isolation is a common requirement in practical applications. In this letter, since the focus is to present the proof-of-concept of the proposed method, the isolation stage is not demonstrated.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2021.3070698, IEEE Transactions on Power Electronics
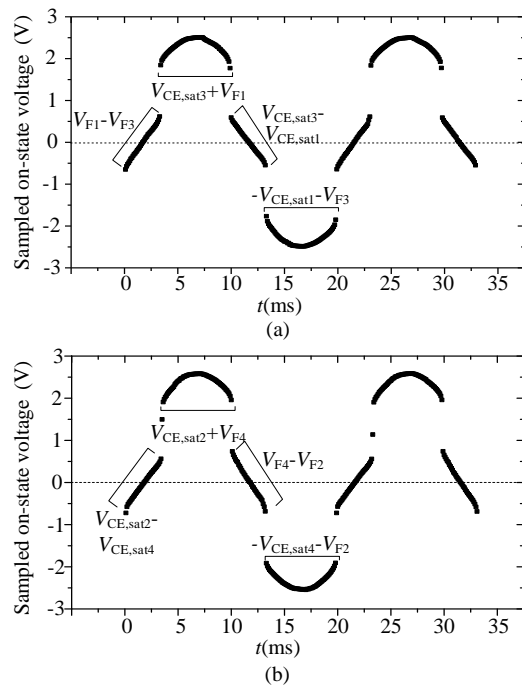
IEEE POWER ELECTRONICS LETTER 5

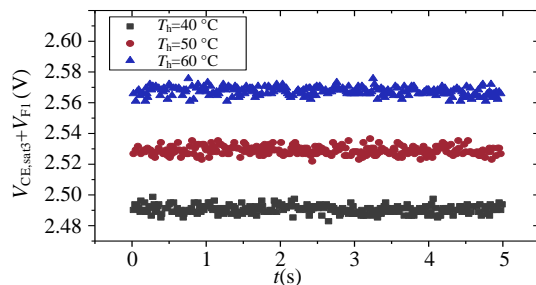Fig. 7. Sampled on-state voltages of T_1-T_4 and D_1-D_4.

Fig. 8. Extracted the peak point of the measured on-state voltage in Fig.7(a) at different heatsink temperature levels.

IV. CONCLUSIONS

This letter proposes a converter-level power-supply-less circuit to measure the on-state voltages of power semiconductor devices. It reduces the total connecting terminals from eight to six, the number of output signals by 50%, and the component count by 50% compared to a recently reported method in [7]. By far, it is the simplest on-state voltage measurement circuit for the six IGBTs and six diodes in a typical three-phase inverter, to our best knowledge. Moreover, it retains the advantages of the circuit in [7] with a plug-and-play feature and scalable voltage rating. The experiment results verify that it has fast dynamic response and its measurement error is within 0.08% in response to the input voltage within ± 5 V. It should be noted that half of the proposed circuit can be applied for a single-phase inverter or a half-bridge leg with two switches.

REFERENCES

[1] U. Choi, F. Blaabjerg, and S. Jørgensen, "Junction temperature estimation for an advanced active power cycling test," in *Proc. International Confer-
ence on Power Electronics and ECCE Asia*, 2015, pp. 2944–2950.
[2] U. Choi, F. Blaabjerg, S. Jorgensen, S. Munk-Nielsen, and B. Rannestad, "Reliability improvement of power converters by means of condition monitoring of IGBT modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7990–7997, Oct. 2017.
[3] S. Beczkowski, P. Ghimre, A. R. de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thøgersen, "Online Vce measurement method for wear-out monitoring of high power IGBT modules," in *Proc. European Conference on Power Electronics and Applications.*, 2013, pp. 1–7.
[4] M. Denk and M.-M. Bakran, "IGBT gate driver with accurate measurement of junction temperature and inverter output current," in *Proc. PCIM Europe*, 2017, pp. 1–8.
[5] V. Smet, F. Forest, J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of Vceon monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2760–2770, Jul. 2013.
[6] Y. Peng, Y. Shen, and H. Wang, "A converter-level on-state voltage measurement method for power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1220–1224, Jul. 2021.
[7] Y. Peng and H. Wang, "A self-power method for a converter-level on-state voltage measurement concept," *IEEE Transactions on Power Electronics*, pp. 1–1, 2021.
[8] N. Springett, "Voltage limiter and use of a voltage limiter to determine values of a power semiconductor element," Jan. 2015, US Patent App. 14/333,537.
[9] Y. Peng and H. Wang, "Non-invasive front-end for power electronic monitoring," Patent, 2020.