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A Self-Power Method for A Converter-level On-state Voltage Measurement Concept

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***Abstract*—This paper discloses part of an invention on plug-and-play converter-level on-state voltage measurement methods for power semiconductor devices. To exclude the external power supply required in on-state voltage measurement circuits, a self-power solution is proposed to provide the required bidirectional low-voltage power sources. The application of the measurement circuit with the proposed self-power solution is demonstrated for a single-switch, a single-phase inverter, and a three-phase inverter.**

***Index Terms*—Power semiconductor, converter-level, reliability, condition monitoring, self-power.**

I. Introduction

On-state voltage in this paper refers to the voltage stress of a power semiconductor during its fully-conducted operation mode. For example, the $V_{\mathrm{CE,sat}}$ of an IGBT, $V_{\mathrm{ds,on}}$ of a MOSFET, and V_{F} of a diode [1]–[3]. It is a parameter widely used for degradation prediction, junction temperature estimation, and protection implementation of power semiconductor devices [3]–[6]. Particularly for those safety-critical applications (e.g., train traction) and availability-critical applications due to high maintenance cost (e.g., off-shore wind turbine), the on-line measurement of on-state voltage is of importance in realizing condition monitoring. Compared to the gate-related parameters, such as the threshold voltage [7], gate-emitter voltage [8], and the turn-off delay time [9], on-state voltage has the following outstanding features: 1) it is noninvasive to the gate driver; 2) it has relative low-frequency, which simplifies the measurement significantly; 3) it is relevant to the three typical failure mechanisms (e.g., bond-wires lift-off [3], solder layer degradation [10], and gate-oxide layer wear-out [11]) of power devices.

On-state voltage typically ranges from sub-volt to few volts. It needs to be measured from signals including also the off-state voltage stresses up to the rated voltage of the semiconductor of interest. Cost, complexity, and accuracy are three important aspects to be considered for the measurement solutions. To achieve this, various solutions have been proposed and summarized in [12]. Nevertheless, they still reveal limited performances: 1) they are component-level measurement circuit and require one isolated power supply for each power device or phase-leg, which leads to the increased circuit complexity, size, cost, and complex connection to monitor a three-phase converter for example; 2) they are connected to the two power-terminals of individual power switch, which requires multiple connecting terminals for the application of three-phase converters; 3) they require one reference ground for each phase-leg, which makes the data sampling equipment more complicated. Recently, a converter-level measurement circuit is presented in [13] for a single-phase inverter application. It has the advantage of significantly reduced cost and complexity. Nevertheless, the reported converter-level method in [13] and existing component-level methods require the power supply for generating low-voltage references. Two practical issues exist: 1) the isolated power supply is the most expensive component in the circuit proposed in both component-level and converter-level methods. 2) even though the converter-level method enables a better accessibility to existing power electronic converters, it has not yet fully decoupled from the converters to be measured due to the power supply requirement. This paper aims to realize a plug-and-play converter-level on-state voltage measurement solution with further reduced cost by a self-power method.

Different self-power solutions are presented for other applications [14]–[16]. However, these methods require high-voltage capacitor to withstand most part of the DC-link voltage when the MOSFET/IGBT is in off-state, and an inductor-capacitor energy storage. Another self-power circuit is proposed in [17] to supply gate driver, which takes the rising DC-link voltage during the turn-off transient of MOSFET/IGBT to charge the energy-storage capacitor and needs a specific design for the selected MOSFET, polarization diode, and avalanche diode to achieve the required performance. It is modified in [18] by replacing the polarization diode with a high-voltage resistor to avoid complex design. In addition, the transformer/coupled-inductor is used to extract the required power supply in different converters, e.g., power factor correction (PFC) converter and modular multilevel converter (MMC) [19]–[21]. However, the transform/coupled-inductor is usually bulky. Besides, all of the above solutions are not able to withstand bi-directional high-voltage and provide bi-directional reference voltage. Therefore, a suitable self-power solution for the on-state voltage measurement circuits is not investigated yet and still missing.

This paper discloses one of the methods filed in the invention [22]. The contributions of the presented study are: 1) a self-power method is proposed to enable a plug-and-play solution; and 2) the converter-level measurement concept refers to the measurement of on-state voltage from the output terminal of inverter, which is firstly introduced in [13]. In this paper, it is extended to a three-phase inverter application, which represents a wider range of relevant industry applications. Furthermore, its design principle is elaborated to achieve high-

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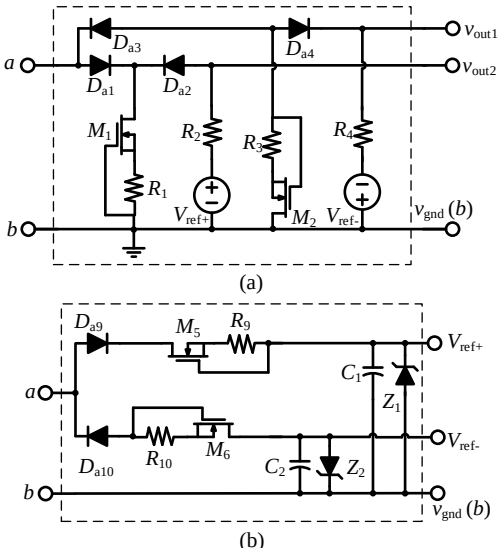


Fig. 1. Topology of the proposed health indicator monitoring circuit: (a) on-state voltage monitoring circuit; (b) self-power circuit to replace the voltage sources $V_{\mathrm{ref}+}$ and $V_{\mathrm{ref}-}$ shown in Fig.1(a).

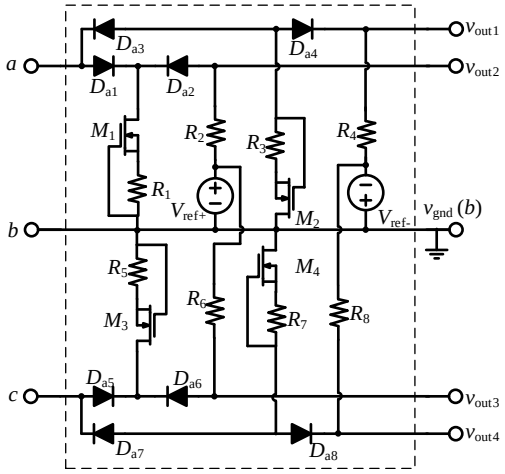


Fig. 2. Topology of the proposed on-state voltage measurement circuit for three-phase inverter.

accuracy and fast-response. In Section II, the proposed self-power circuit is introduced firstly. Subsequently, the application of the converter-level on-state voltage measurement circuit with the proposed self-power solution in a three-phase inverter is discussed in Section III. The hardware realization, circuit design principle, and experimental verification are, thereafter, presented in Section IV. Section V concludes this paper with an overall summary.

II. Proposed Self-Power Circuit for On-State Voltage Monitoring Circuit

A. Configuration of the converter-level on-state voltage measurement circuit

The basic configuration of the converter-level on-state voltage measurement circuit is depicted in Fig.1(a). $D_{\mathrm{a}1}$-$D_{\mathrm{a}4}$ are normal diode. M_1 and M_2 are signal N-channel depletion MOSFET. $V_{\mathrm{ref}+}$ and $V_{\mathrm{ref}-}$ are the bidirectional reference voltages. The basic function of this circuit is elaborated in Table I, where $V_{\mathrm{Da}1}$-$V_{\mathrm{Da}4}$ are the forward voltage of $D_{\mathrm{a}1}$-$D_{\mathrm{a}4}$, $V_{\mathrm{M}1}$ and $V_{\mathrm{M}2}$ are the voltage across M_1 and M_2, respectively. The detail of the operation principle can be referred to [13].

B. Configuration of the proposed self-power circuit

The proposed self-power circuit is depicted in Fig.1(b). It can replace the external power supply and provide the bi-directional reference voltages. More importantly, it does not affect the normal operation of the power converter.

$D_{\mathrm{a}9}$ and $D_{\mathrm{a}10}$ are normal diode, Z_1 and Z_2 are zener diode with 6.2 V zener voltage in this case study, M_5 and M_6 are depletion MOSFET. Based on this, when the input voltage of the self-power circuit is positive, $D_{\mathrm{a}9}$ is conducted and $D_{\mathrm{a}10}$ is blocked. M_5 operates in the linear mode due to the voltage drop in R_9 and withstands the high-voltage. Then, C_1 is charged until its voltage reaches at 6.2 V. Likewise, when the input voltage is negative, C_2 starts to charge until its voltage reaches at -6.2 V. Accordingly, the bidirectional reference voltage $\pm$6.2 V is obtained. Moreover, the proposed on-state voltage measurement circuit and self-power supply can share the common ground, which excludes the requirement of electrical isolation. It is noted that R_9 (R_{10}) are used to control the impedance of M_5 (M_6) and the charging current of C_1 (C_2). The higher R_9 is selected, the less charging current and the higher impedance of M_5 can be induced. Then, the charging time is increased, and further the reference voltage may not be able to reach the preset zener voltage. However, if the R_9 is too low, the higher current can cause the power losses of M_5 exceeds its maximum limitation.

III. Application of the Proposed Self-Powered On-State Voltage Measurement Circuit

A. Implementation

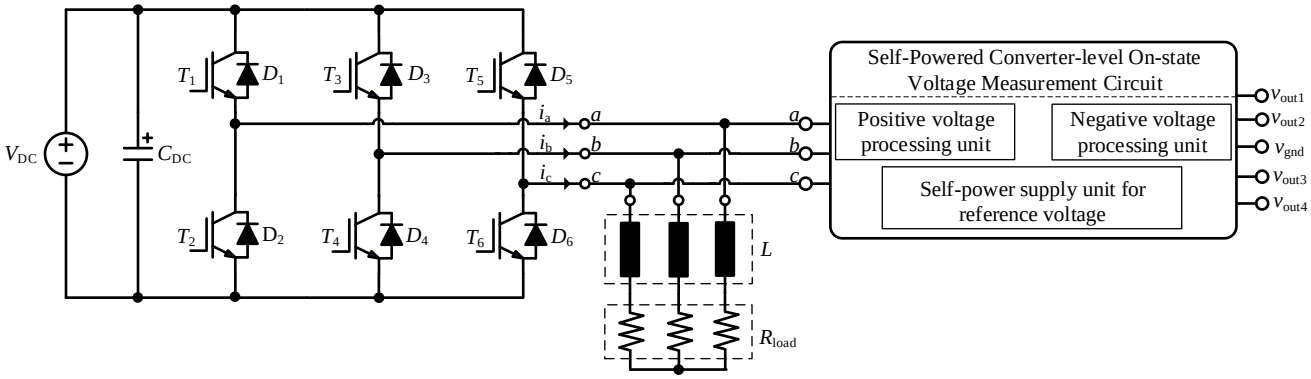
1) Three-phase inverter: The configuration depicted in Fig.1(a) is designed for single-phase converters as discussed in [13], which is replicated partially (the reference voltage can be shared due to the common ground) for three-phase inverter as shown in Fig.2.

Fig.3(a) shows that the measurement circuit is connected to the three-phase inverter through the three output terminals, which achieves plug-and-play and shows non-invasive to the converter. Also, the number of input and output terminals is halved from 16 in conventional methods (including 5 input terminals, 2 power supply terminals, and 9 output terminals) for three-phase inverter application.

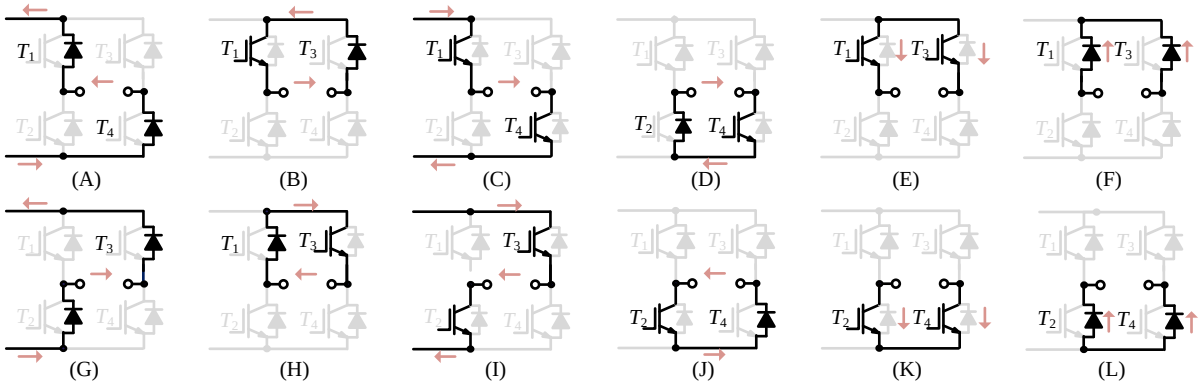
To make it simple and understandable, the operation modes of three-phase inverter are analyzed in terms of phase-legs a and b (phase c and b can be derived similarly). According to the direction of phase current and the on-off state of switches, the operation modes can be drew as Fig.3(b). Based on this, one of the output line voltages of the inverter, v_{ab} for example, presents different values in different modes, as listed in Table II. Among these modes, the v_{ab} can be the sum of the on-state voltages of one IGBT and one diode, and the difference of the on-state voltages of two IGBTs or two diodes, which

TABLE I
BASIC FUNCTION OF THE PROPOSED ON-STATE VOLTAGE MONITORING CIRCUIT.

$v_{\rm ab}$	$v_{\rm out1}$	$v_{\rm out2}$
$v_{\rm ab} > V_{ref+}$	$\frac{R_4}{R_4+R_3}(V_{\rm ref-}+V_{\rm Da4}+V_{M2})+V_{\rm ref-}$	$V_{\rm ref+}$
$0 \le v_{\rm ab} \le V_{\rm ref+}$	$\frac{R_4}{R_4+R_3}(V_{\rm ref-}+V_{\rm Da4}+V_{\rm M2})+V_{\rm ref-}$	$v_{\rm ab}-V_{\rm Da1}+V_{\rm Da2}\approx v_{\rm ab}$
$V_{\rm ref-} \le v_{\rm ab} \le 0$	$v_{\rm ab}+V_{\rm Da3}-V_{\rm Da4}\approx v_{\rm ab}$	$V_{\rm ref+}-\frac{R_2}{R_2+R_1}(V_{\rm ref+}-V_{\rm Da2}-V_{M1})$
$v_{\rm ab} < V_{\rm ref-}$	$V_{\rm ref-}$	$V_{\rm ref+}-\frac{R_2}{R_2+R_1}(V_{\rm ref+}-V_{\rm Da2}-V_{\rm M1})$



(a)



(b)

Fig. 3. Implementation of the proposed circuit in three-phase inverter: (a) connection to the three-phase inverter; (b) operation models of phase-legs a and b in the three-phase inverter with SPWM modulation.

TABLE II
VALUE OF THE OUTPUT VOLTAGE OF THE THREE-PHASE INVERTER IN DIFFERENT OPERATION STATES.

Operation states	Output voltage $v_{\rm ab}$
A	$V_{\rm DC}+V_{\rm F1}+V_{\rm F4}$
B	$-V_{\rm CE,sat1}-V_{\rm F3}$
C	$V_{\rm DC}-V_{\rm CE,sat1}-V_{\rm CE,sat4}$
D	$-V_{\rm CE,sat4}-V_{\rm F2}$
E	$V_{\rm CE,sat3}-V_{\rm CE,sat1}$
F	$V_{\rm F1}-V_{\rm F3}$
G	$-V_{\rm DC}-V_{\rm F3}-V_{\rm F2}$
H	$V_{\rm CE,sat3}+V_{\rm F1}$
I	$-V_{\rm DC}+V_{\rm CE,sat3}+V_{\rm CE,sat2}$
J	$V_{\rm CE,sat2}+V_{\rm F4}$
K	$V_{\rm CE,sat2}-V_{\rm CE,sat4}$
L	$V_{\rm F4}-V_{\rm F1}$

are existed in the converters with both SPWM and SVPWM modulations.

$V_{\rm CE,sat1}-V_{\rm CE,sat4}$ are the on-state voltages of T_1-T_4; $V_{\rm F1}-V_{\rm F4}$ are the forward voltages of freewheeling diodes (FWD) D_1-D_4. It can be seen from Table II that the on-state voltage of T_1-T_4 and D_1-D_4 are included in v_{ab}. Likewise, it can be reasoned that the on-state voltage of T_3-T_6 and D_3-D_6 are included in $v_{\rm cb}$. In conclusion, the output voltages $v_{\rm ab}$ and $v_{\rm cb}$ contain the positive and negative DC-link voltage, the sum of $V_{\rm CE,sat}$ and $V_{\rm F}$, and the difference of two $V_{\rm CE,sat}$ or two $V_{\rm F}$. Considering the functions of the proposed circuit, the positive and negative DC-link voltage can be clipped into the preset reference voltages, while $V_{\rm CE,sat}$ and $V_{\rm F}$ become detectable.

2) Single-phase inverter: For the single-phase inverter with unipolar SPWM or hybrid SPWM modulations, the operation modes are same with that of three-phase inverter excluding the modes (E), (F), (K), and (L) in Fig.3(b), which is detailed in [13].

3) Individual power semiconductor: With the self-power function, the plug-and-play is realized, and the circuit size and cost of the proposed method is still lower than that of existing

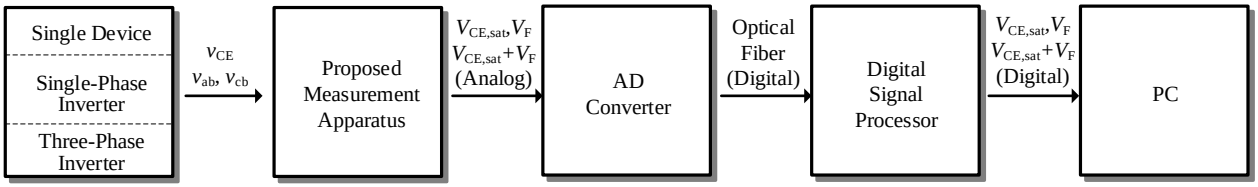


Fig. 4. Implementation process.

TABLE III
DESCRIPTION OF THE COMPONENTS USED IN THE PROPOSED CIRCUIT.

Components	Description	Value
M_1-M_6	Signal depletion MOSFETs	17 mA/600 V
D_{a1}-D_{a10}	ES1JR2	600 V/1 A
Z_1-Z_2	Zener diodes	6.2 V
R_1, R_3, R_5, R_7	SMD resistors	200 Ω
R_2, R_4, R_6, R_8	SMD resistors	1.2 k/1.8 k/6.8 kΩ
C_1-C_2	SMD capacitors	10 μF

component-level methods even it is applied to an individual power semiconductor.

B. Selection of components

The selection of components is discussed to make the measurement circuit has much better performance. Take the half circuit in Fig.1(a) (M_1, R_1, R_2, D_{a1}, and D_{a2}) and the self-power circuit as example:

- D_{a1} and D_{a2} must have the same rating voltage with the DC-link voltage of the converter and share identical electrical characteristics as much as possible. As such, V_{Da1} and V_{Da2} can be canceled with each other to a large degree, leading to a small measurement error.
- The depletion MOSFETs M_1 also must has the rating voltage higher than the DC-link voltage of the converter since it needs to withstand the DC-link voltage when D_{a1} is conducted.
- $R_1 - R_2$ can be SMD resistor due to the mA-level current during operation (e.g., 1.5 mA in this cast study). Among them, R_1 and R_2 are used to control the current flowing through D_{a1} and D_{a2}, respectively. So as to adjust the measurement error, which is discussed in Section IV, Part C.
- Z_1 and Z_2 are used to provide the bidirectional reference voltage. Their zener voltage should be higher than the maximum $V_{CE,sat} + V_F$.
- D_{a9} and D_{a10} are same with D_{a1} and D_{a2} except for the requirement of identical characteristic.
- M_5 and M_6 are the same with M_1.
- R_9 and R_{10} are the same with R_1.
- C_1 and C_2 are used to stabilize the reference voltages.

IV. EXPERIMENTAL VERIFICATION

A. Hardware realization

The implementation process of the proposed circuit for a single device, single-phase inverter, and three-phase inverter is discussed as summarized in Fig.4, including the power converter stage, monitoring circuit, Analog-Digital converter, digital signal processor, and data storage in computer.

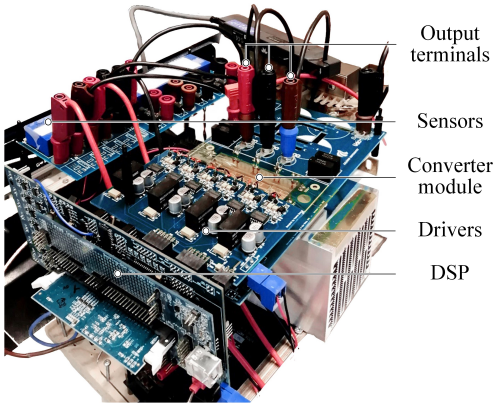


Fig. 5. Demonstrator of three-phase inverter.

TABLE IV
SPECIFICATIONS OF THE DEVELOPED INVERTER PLATFORM.

Parameters	Value
DC-Link voltage	400 V
Switching frequency	10 kHz
Dead time	2 μs
Inductance	2 mH
AC capacitance	10 μF

1) Inverter stage: Firstly, the specifications of the three-phase inverter are listed in Table IV, along with its hardware realization as shown in Fig.5. The modulation method for the three-phase inverter is SPWM.

2) Prototype of the proposed circuit: A 600 V prototype of the proposed circuit is designed as shown in Fig.6. The size of this prototype is 3.5 cm×4.5 cm×3 cm, which can be smaller further if the housing and connecting terminals are well-deigned and manufactured. The three input terminals are used to connect the output terminals of the three-phase inverter as shown in Fig.5. Due to the SMD (Surface Mount Device) package of the required components and the negligible power losses (e.g., about 0.5 W in this case study), the proposed circuit can be designed as a compact double-layer PCB (e.g., 2.5*3 cm^2 in this case study). In field applications, the size can be different due to the different requirements of insulation-distance between input terminals.

3) AD converter and data communication: Once the analog on-state voltage are obtained, they are converted into digital data by using a 14-bit dual channel AD converter and transmitted into a digital signal processor through the optical fiber. Then, the digital on-state voltage information can be processed further and used to assess the health condition of the power semiconductors.

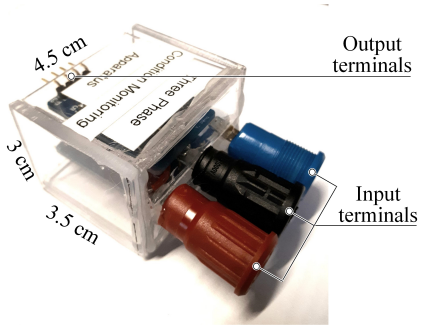


Fig. 6. 600 V prototype of the proposed condition monitoring apparatus.

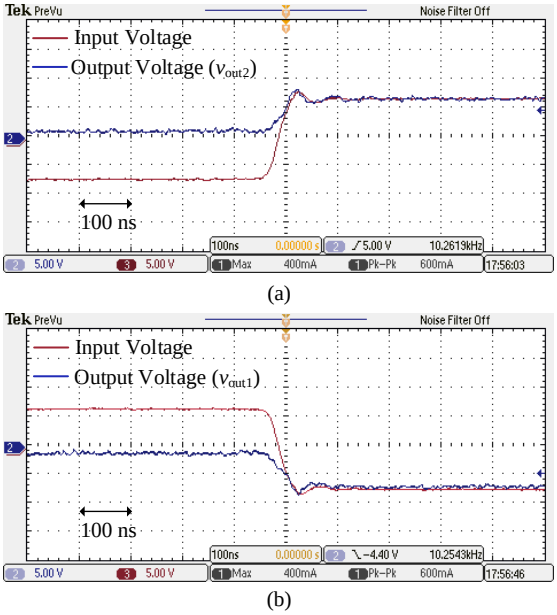


Fig. 7. Dynamic response of the proposed measurement circuit with a step-change input voltage: (a) from -7.5 V to 6.5 V; (b) from 7.5 V to -6.5 V.

B. Dynamic response testing of the proposed circuit

A fast dynamic response is mandatory for the on-line monitoring of on-state voltage considering the short measurement window during operating converter. The dynamic performance of the proposed circuit is verified with a step-change voltage signal. Fig.7 shows that, in principle, the proposed circuit can follow the step-change input voltage very well, no matter it increases from -7.5 V to 6.5 V or decreases from 7.5 V to -6.5 V. In an operating converter, the overshoot and oscillation are existed in the measured result due to the parasitic parameters of converter and connecting wires as shown in Fig.8. It can be seen that the setting time is around 4 μs. Therefore, based on the case study in this paper, the maximum operating frequency is around 250 kHz, which can be increased further by reducing the parasitic parameters.

C. DC accuracy calibration of the proposed circuit

With the selected components in Table III, the accuracy of the proposed circuit is tested with DC input voltage. One of the corresponding results are depicted in Fig.9, illustrating the relative error $\varepsilon_{\rm r}$ from a DC input voltage $v_{\rm in}$ to a DC output

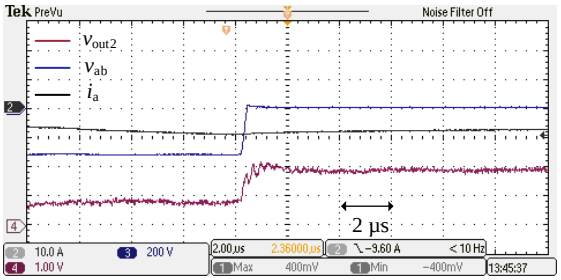


Fig. 8. The on-state voltage measurement transient in the converter by using the proposed circuit.

voltage $v_{\rm o}$ in the range from 1 V to 5 V. $\varepsilon_{\rm r}$ is limited to $\pm 2\%$ with an absolute maximum error 80 mV when $v_{\rm in}$ is 4 V and an absolute minimum error less than 5 mV when $v_{\rm in}$ is within 1.5 V and 1.9 V.

The change trend of $\varepsilon_{\rm r}$ can be roughly analyzed with the help of the circuit in Fig.1. If the input voltage is from 1 V to 5 V and the $V_{\rm ref+}$ is 9 V, the voltage drop in R_2 ranges from 8 V to 4 V by roughly assuming $V_{\rm Da1}$ and $V_{\rm Da2}$ can be canceled with each other. Consequently, the current flowing through $D_{\rm a2}$ ($I_{\rm Da2}$) decreases from 8/6.8 k=1.2 mA to 4/6.8 k=0.6 mA. On the other side, as the input voltage increases from 1 V to 5 V, the voltage drop in M_1 and R_1 increases from 0.5 V to 4.5 V by assuming a constant 0.5 V drop in $D_{\rm a1}$. However, it is difficult to quantitatively determine the specific voltage drop in M_1 or R_1 due to the variable impedance of M_1. Thus, the voltage drop in R_1 is measured experimentally and it increases from 0.4 V to 0.9 V along with the increasing input voltage. Consequently, the current flowing through $D_{\rm a1}$ ($I_{\rm Da1}$) increases from (0.4/200-1.2)=0.8 mA to (0.9/200-0.6)=3.9 mA. To summarize, as increasing $v_{\rm in}$ from 1 V to 5 V, $I_{\rm Da1}$ and $I_{\rm Da2}$ present opposite change trend, resulting that the $\varepsilon_{\rm r}$ increases from -1.7% to 1.7%.

Based on the analysis above, $I_{\rm Da1}$ and $I_{\rm Da2}$ can be changed by adjusting R_1, R_2, and the reference voltage. Then, the variation range of $\varepsilon_{\rm r}$ can be consequently moved or narrowed.

For example, if R_2 is replaced with a 1.8 kΩ resistance, the accuracy distribution is depicted in Fig.10(a). It shows the relative error $\varepsilon_{\rm r}$ is limited to $\pm 1\%$ when the $V_{\rm in}$ is higher than 3.8 V. Especially, $\varepsilon_{\rm r}$ is zero when $V_{\rm in}$ is 4.91 V. Similarly, increasing the reference voltage can also change the accuracy distribution as shown in Fig.10(b). The point with zero $\varepsilon_{\rm r}$ is moved to $V_{\rm in}$=3.35 V and the range of $\varepsilon_{\rm r}$ less than $\pm 1\%$ is moved to $V_{\rm in} \geq$2.8 V. Therefore, based on different applications, the relative error can be limited to $\pm 1\%$ by selecting proper components. Considering the reference voltages generated by the proposed self-power circuit is $\pm$6.2 V and the monitored sum of on-state voltages to indicate the degradation level of the applied IGBT is within 4 V and 6 V in this case study, the selected components are as follows: R_1=200 Ω and R_2=1.2 KΩ, which can achieve same accuracy-level with Fig.10(a).

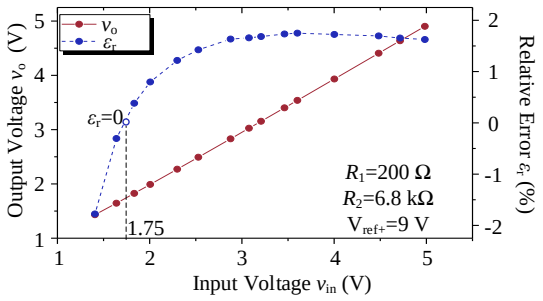


Fig. 9. Accuracy verification of the proposed circuit.

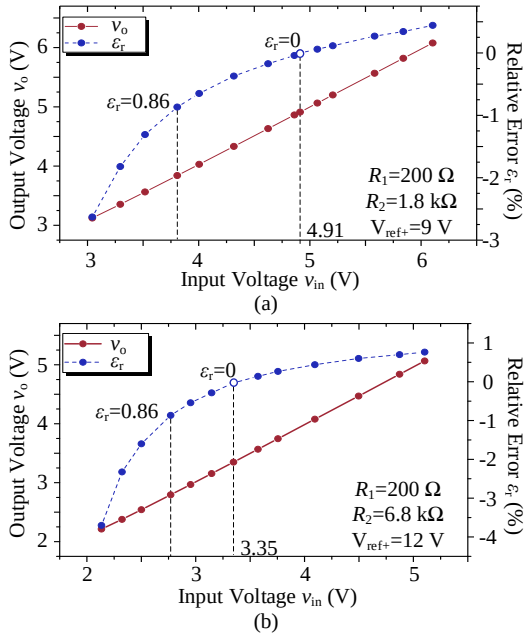


Fig. 10. Accuracy verification of the proposed circuit with different components compared to Fig.9.

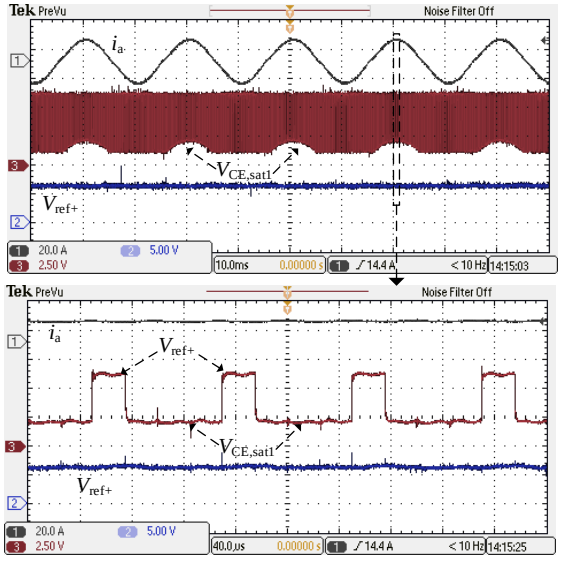


Fig. 11. Measured on-state voltage of an individual IGBT with the proposed circuit.

D. Measured on-state voltage waveforms from an individual IGBT

The proposed circuit is firstly applied to an individual IGBT in the converter. The Corresponding experimental results are given in Fig.11, including the sinusoidal output current i_a, the measured on-state voltage, and the extracted reference voltage, which verifies the effectiveness of the proposed circuit in extracting on-state voltage from the two-terminals of IGBT.

E. Measured on-state voltage waveforms from three-phase inverter

There are four output signals of the proposed circuit for monitoring a three-phase inverter as shown in Fig.3(a). $v_{\rm out1}$ and $v_{\rm out2}$, extracted from $v_{\rm ab}$, consist of $V_{\rm CE,sat1-4}$ and $V_{\rm F1-4}$. Similarly, $V_{\rm CE,sat3-6}$ and $V_{\rm F3-6}$ are included in $v_{\rm out3}$ or $v_{\rm out4}$ extracted from $v_{\rm cb}$. For simplification, only the results measured from the phase leg a and b of the three-phase inverter are given as shown in Fig.12, indicating that the bidirectional high-voltages in $v_{\rm ab}$ are clipped to the reference voltages. While the low on-state voltages are retained. The dash rectangle in Fig.12(b) is zoomed-in as shown in Fig.12(c). The low on-state voltages $V_{\rm CE,sat3}+V_{\rm F1}$ and $V_{\rm CE,sat2}+V_{\rm F4}$ are alternatively appeared in $v_{\rm out2}$. Likewise, it can be expected that $V_{\rm CE,sat1}+V_{\rm F3}$ and $V_{\rm CE,sat4}+V_{\rm F2}$ are alternatively appeared in $v_{\rm out1}$. They can be separated based on the operation modes listed in Table II. It is worth mentioning that The voltage spikes in Fig.12(c) are mainly attributed to the parasitic inductances of the module terminals, bus-bar, and the connecting wires between the inverter and the proposed circuit during the current commutation transient. they can be reduced by well designing the inverter and shorting the connecting wires, and do not impact the accuracy as only the steady-value is required during the data analysis step.

F. Result of the self-power supply

The extracted bidirectional reference voltages (e.g., ±6.2 V in this case study) are shown in Fig.13, indicating neglected impact on the inverter. Fig.14 compares the results of the measured on-state voltage waveforms from a three-phase inverter by using the self-power circuit and external power supply, indicating that there is no identical difference between them. In principle, the reference voltage is used to prohibit the high-voltage reaching at the end of the measurement circuit and only provides negligible power consumption. Thus, replacing the external power supply with the proposed self-power circuit does not affect the accuracy of on-state voltage measurement as shown in Fig.15.

G. On-line monitoring of the degradation of power semiconductors

The measured results from the three-phase inverter and single-phase inverter are similar. Therefore, the degradation testing is carried out based on a single-phase inverter for the sake of saving experimental material. The modulation of the single-phase inverter is unipolar SPWM and its specifications are same with the developed three-phase inverter (e.g., 400V

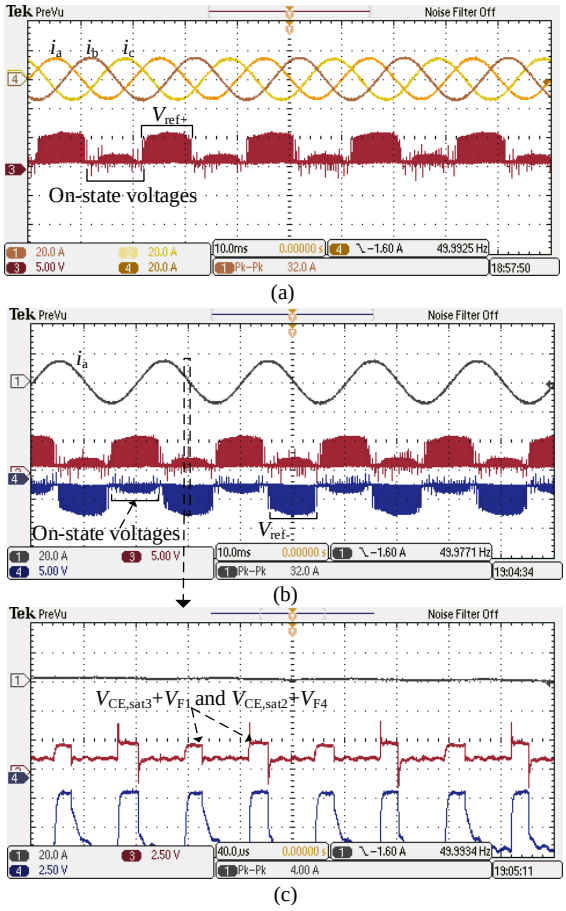


Fig. 12. Experimental results measured from the three-phase inverter: (a) CH1:i_a, CH2:i_b, CH4:i_c, CH3:v_{out2} (b) CH1:i_a, CH3:v_{out2}, CH4:v_{out1}; (c) Zoom-in of the rectangle in Fig.12(b).

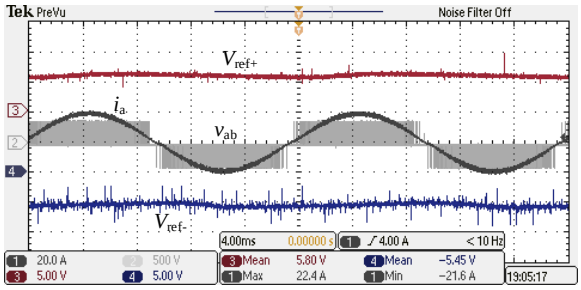


Fig. 13. Output waveforms of the proposed self-power circuit.

DC-Link voltage and 30A peak current). The device under test (DUT) is a 1200 V/50 A converter module (F4-50R12KS4). The IGBT and FWD are connected to the power terminals with 8 and 6 bond-wires, respectively as shown in Fig.16.

To verify the proposed circuit, the degradation mechanisms of IGBT are simulated by cutting off bond-wires and increasing the heatsink temperature (T_h), respectively. They are reasonable methods and have been verified in many researches [5], [23], [24]. The detail about how to cut off bond-wires is illustrated in Table V. The temperature of heatsink is controlled by a controllable heat plate at 40 °C, 50 °C, and 60 °C accordingly.

For simplification, only the bond-wires of T_4 and D_2 are cut

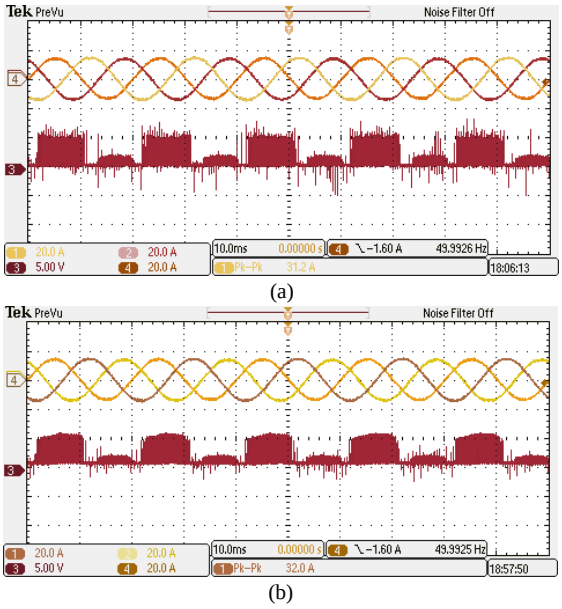


Fig. 14. Comparison of the measured on-state voltage waveforms by using: (a) external power supply (b) proposed self-power circuit.

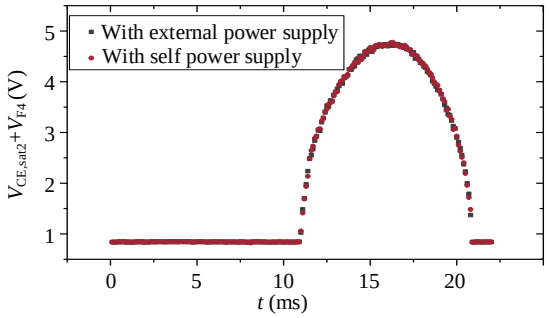


Fig. 15. Comparison of the measured on-state voltage data from a single-phase inverter by using the external power supply and the proposed self-power circuit.

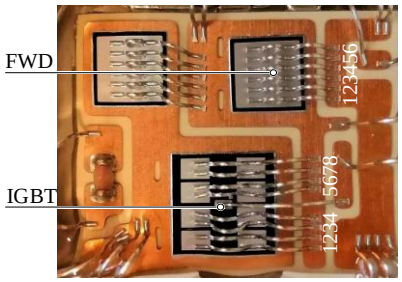


Fig. 16. Internal structure of the IGBT module under test.

TABLE V
EXECUTED ACTIONS TO SIMULATE THE BOND-WIRES LIFT-OFF OF POWER DEVICES (THE DEVICES UNDER TEST ARE THE IGBT IN T4 AND FWD IN T2).

Cases	Action
#1	New
#2	2 bond-wires of IGBT are cut off
#3	4 bond-wires of IGBT are cut off
#4	6 bond-wires of IGBT are cut off
#5	6 bond-wires of IGBT and 2 bond-wires of FWD are cut off

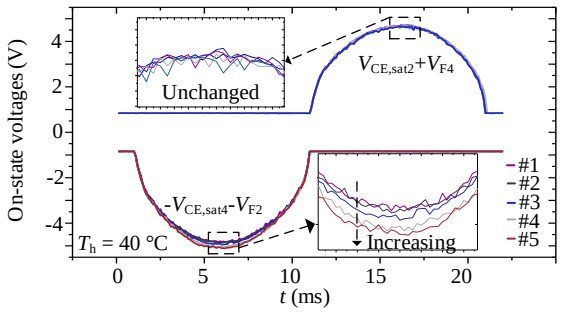


Fig. 17. Measured on-state voltage among one fundamental period when the bond-wires of T_4 and D_2 are cut off and the heat-sink temperature is 40 °C.

TABLE VI
NORMALIZED ON-STATE VOLTAGE WITH DIFFERENT HEATSINK TEMPERATURES AND NUMBERS OF BOND-WIRES CUT-OFF.

Cases	T_h=40 °C	T_h=50 °C	T_h=60 °C
#1	1(4852 mV)	1(4877 mV)	1(4898 mV)
#2	1.0050	1.0117	1.0080
#3	1.0210	1.0146	1.0180
#4	1.0445	1.0451	1.0447
#5	1.0536	1.0562	1.0566

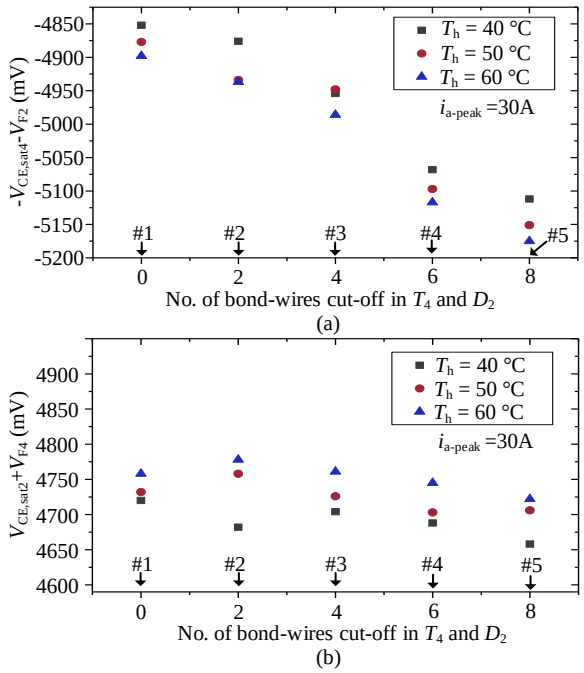


Fig. 18. Monitored on-state voltage at peak current when bond-wires are cut off and heat-sink temperature is increased: (a) -$V_{\mathrm{CE,sat4}}$-V_{F2} (v_{out1}) (b) $V_{\mathrm{CE,sat2}}$+V_{F4} (v_{out2}).

off. For comparison purpose, the on-state voltage of T_2 and D_4 is also sampled. The monitored results are summarized in Fig.17. It shows that $V_{\mathrm{CE,sat2}}$+V_{F4} keeps same when bond-wires are cut off, while -$V_{\mathrm{CE,sat4}}$-V_{F2} is increased negatively, particularly at the peak point. These bond-wires are connected in parallel and the increment of their equivalent resistance is exacerbated as more bond-wires are cut off. Thus, -$V_{\mathrm{CE,sat4}}$-V_{F2} shows slow increase at first three cases (#1, #2 and #3). Then, it shows a relative big jump when 6 bond-wires are cut off (#4). In addition, it is increased further when the two bond-wires of FWD are cut off (#5).

In practice, the change of on-state voltage caused by degradation becomes much larger at higher current. Therefore, the on-state voltage measured at the peak current is extracted as shown in Fig.18(a). It shows the measured on-state voltage is increased negatively with cutting off the bond-wires and increasing the heatsink temperature by about 270 mV and 50 mV, respectively. While, if the bond-wires is healthy, the change of the measured on-state voltage at the same temperature level is much smaller as shown in Fig.18(b). It should be noted that the data sampling is conducted once every switching period in this case study and the current during one switching period is not constant. Therefore, the measured on-state voltage at same temperature level in Fig.18(b) is not exactly same.

The monitored on-state voltages at peak point are normalized by using their initial value as shown in Table VI, indicating that after cutting off 8 bond wires (6 of IGBT and 2 of FWD), it is increased by more than 5% at each same heatsink temperature level.

V. CONCLUSION

A self-power solution is proposed for the on-state voltage monitoring circuit of power semiconductor devices in this paper. It can extract the power from the two-terminal of an individual power device or the middle-points of the phase-legs in the three-phase/single-phase inverter without influencing the operation of converter. With the proposed self-power circuit, the conventional component-level and converter-level on-state voltage monitoring circuits can exclude the external power supply and become plug-and-play application. In addition, the previously introduced converter-level on-state voltage monitoring circuit is extended to monitor a three-phase inverter, and its dynamic response and accuracy are investigated with step-change voltage and DC voltage, respectively. The measured errors are adjustable in respect to different input voltage by adjusting the selected resistances and reference voltages accordingly. For example, For the developed prototype with R_1=200 Ω, R_2=1.2 kΩ, and $V_{\mathrm{ref+}}$=6.2 V, the error is limited to ±0.5% in respect to the input voltage from 4 V to 6.2 V.

Finally, the ability of monitoring the degradation process and temperature change of power semiconductor is performed with a single-phase case study. According to the results, the on-state voltage is increased by over 5% (about 270 mV) when 6 bond-wires of an IGBT and 2 bond-wires of a Diode are cut off, and 1% (about 50 mV) when the heat-sink temperature is increased from 40 °C to 60 °C, respectively. Overall, due to the features of converter-level monitoring and self-powering, the proposed method can achieve the plug-and-play implementation, and reduced circuit complexity, size, and connecting terminals, compared to existing methods.

The limitation of the proposed circuit is that it can only be applied to those converter systems where the middle-points of the phase-legs are accessible, which, nevertheless, represents a wide range of applications. In the future work, isolation and signal processing for applications which the separation of the on-state voltage signals are necessary will be developed.

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