A CMOS RADIO-FREQUENCY FRONT-END

FOR MULTI-STANDARD WIRELESS COMMUNICATIONS

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A CMOS RADIO-FREQUENCY FRONT-END

FOR MULTI-STANDARD WIRELESS COMMUNICATIONS

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LIST OF ABBREVIATIONS

CDMA .....code division multiple access

CMOS .....complementary metal oxide semiconductor

EDGE.....enhanced data rates for GSM evolution

EVM .....error vector magnitude

FET .....field effect transistor

GaAs .....gallium arsenide

GSM .....global system for mobile communications

HBT .....hetero-junction bipolar transistors

IC .....integrated circuit

IL.....insertion loss

IMD3 .....third-order intermodulation distortion

IP3 .....third-order intercept point

LC .....inductors and capacitors

LNA .....low noise amplifier

LTCC .....low-temperature co-fired ceramic

OFDM .....orthogonal frequency division multiplexing

P1dB .....1-dB compression point

PA .....power amplifier

PAE .....power-added efficiency

PAPR .....peak-to-average power ratio

PCB .....printed circuit board

pHEMT .....pseudomorphic high electron mobility transistor

RF .....radio frequency

RL .....return loss

RX.....receive

SOI.....silicon on insulator

SP4T.....single pole four throws

SP7T.....single pole seven throw

SP9T.....single pole nine throw

SPDT.....single pole double throw

TX.....transmit

VCO .....voltage-controlled oscillator

WCDMA .....wideband code division multiple access

WiMAX .....worldwide interoperability for microwave access

WLAN .....wireless local area network

SUMMARY

The explosive growth of wireless communication market has led the development of low-cost, highly-integrated wireless communication systems. Even though most blocks in the front-end have successfully been integrated by using the CMOS technology, it is still a formidable challenge to integrate the entire front-end. Thus, the objective of this research is to demonstrate the feasibility of the integrated front-end by using improved circuit techniques as well as the improved process technologies.

This dissertation proposes an improved control scheme to enhance the high-power handling capability of an antenna switch. As a part of this research, an antenna switch controller for a GaAs antenna switch was first developed to enhance the performances of the GaAs antenna switch by using the boosted control voltage. To enhance the efficiency of the front-end, efficiency improvement techniques for the antenna switch controller has also been studied. With the suggested efficiency improvement techniques, a fully-integrated antenna switch was implemented using the SOI technology, and exceeding performances over many commercial products for watt-level high-power applications have been successfully demonstrated. As an effort to improve the efficiency of a power amplifier, a linear envelope detector was also implemented, and the results show that the envelope detector is suitable for dynamic biasing of the power amplifier.

The research presented in this dissertation, thus, provides a low-cost and high-performance solution for highly-integrated RF front-end used in various wireless communication systems.

CHAPTER 1

INTRODUCTION

1.1. BACKGROUND

Since the introduction of hand-held wireless communication devices to the public, the growth of the wireless communication industry has been explosive. Unlike the captive market in early or mid 90's when the wireless communication technology was available limitedly for the military or broadcasting companies, today's market for the public consumes greatly increased number of devices, and the consumers demand low-cost, small-sized devices with more features such as video streaming and computer-like capabilities in the devices.

The diversified demands for the multiple functionalities from the public consumers stoked the development of multiple wireless communication standards, and today's wireless communication devices easily include two or more transceivers in a single device; for example, global system for mobile (GSM), code division multiple access (CDMA), enhanced data rates for GSM evolution (EDGE), wideband CDMA (WCDMA), wireless local area network (WLAN), and worldwide interoperability for microwave access (WiMAX). For each standard, moreover, there are multiple frequency bands to support interoperability and global roaming for countries that use different frequency bands. For example, there are four different frequency bands for the GSM network, which are at 850 MHz, 900 MHz, 1800 MHz, and 1900 MHz. Even though some of the

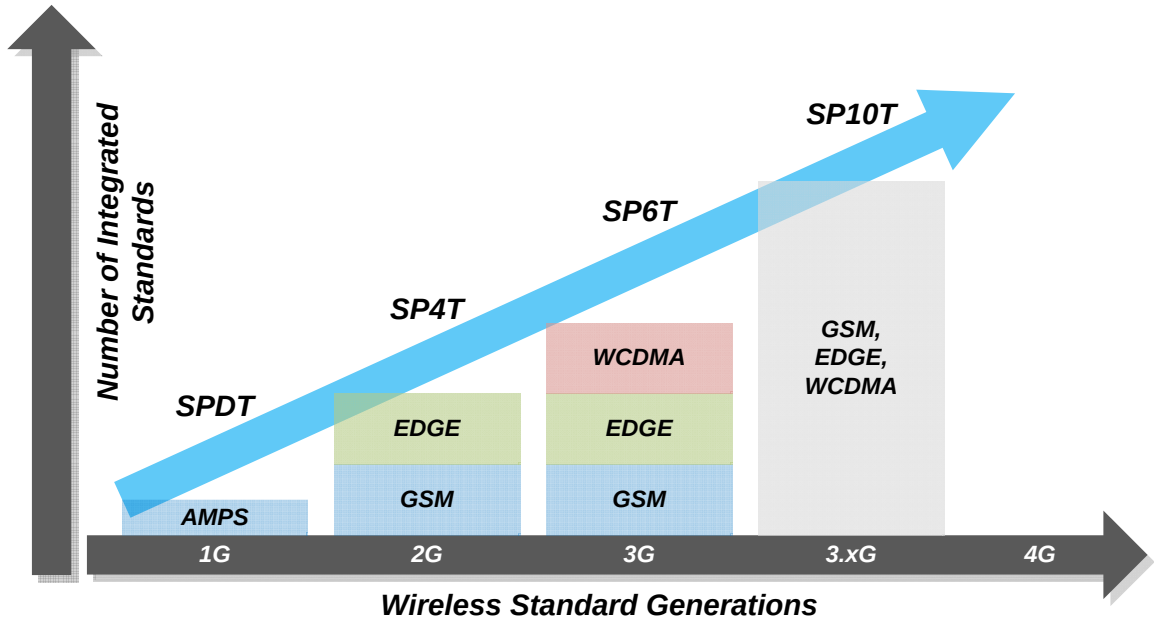


Figure 1. Integration trend of wireless communication standards.

bands can share the transceiver, the number of the transceivers integrated in one device has greatly been increased.

The trend of integration is illustrated in Figure 1. As shown in the figure, there are six wireless standards including GSM, EDGE, and WCDMA for the 3rd generation, and it is expected to be about ten standards in 3.5 or 3.9th generation. The SPDT represents a single-pole double-throw antenna switch, and SP4T, SP6T, and SP10T does a single-pole four-throw, six-throw, and ten-throw antenna switches, respectively.

While the demands for various standards lead to include multiple transceivers in one device, the competitive market forces the devices to be low cost to manufacture and time-to-the-market to be as short as possible. These additional demands from the competitive market along with the demands from the consumers brought another necessity. It became inevitable to reduce the number of components to minimize the cost and the time to

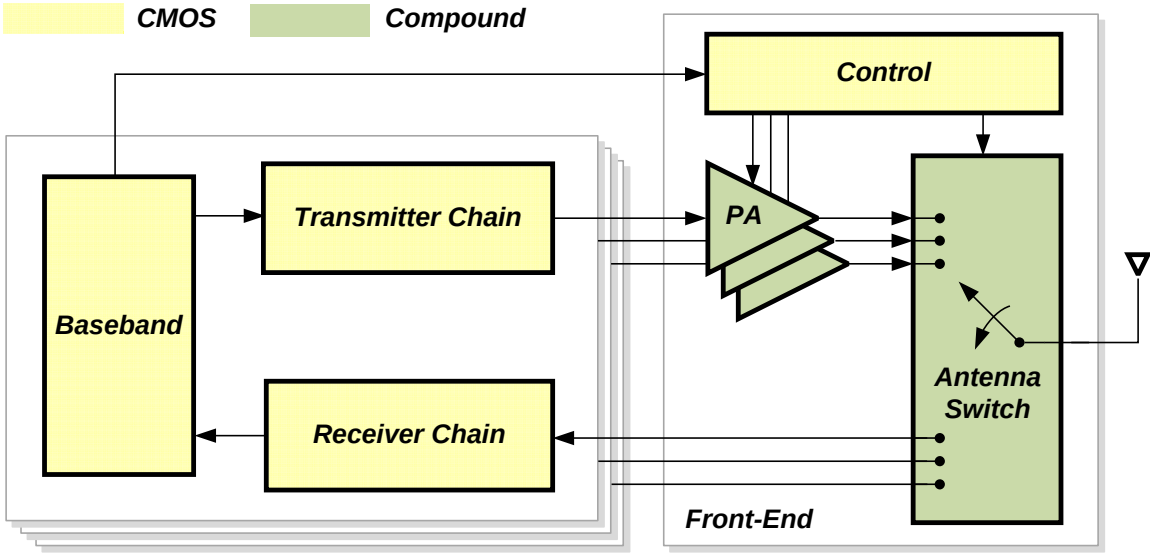


Figure 2. Front-end block diagram of a typical multi-standard and multi-band wireless communication device.

manufacture. The system-on-chip (SOC) or the system-in-package (SIP) approach became prevalent in this purpose.

To keep up with the demands for multi-functional, low-cost wireless communication devices, there has been a great effort to implement a single-chip radio. The advance of fabrication technologies, especially complementary metal oxide semiconductor (CMOS) technology, enabled the integration of the most digital and analog components in the wireless device such as a digital signal processing (DSP), a digital-to-analog converter (DAC), an analog-to-digital converter (ADC). With the achievement, the recent researches focused on the integration of radio frequency (RF) components. In fact, most of the RF components including low noise amplifiers (LNAs), mixers, and voltage controlled oscillators (VCOs), have successfully been integrated in the CMOS

technology. However, the bottleneck of the fully-integrated solution is the front-end including power amplifiers (PAs) and antenna switches.

The front-end of a typical multi-standard and multi-band wireless communication device is shown in Figure 2. Because of its low cost and versatility, the CMOS technology prevails over other semiconductor technologies such as Gallium Arsenide (GaAs) and Silicon Germanium (SiGe) technology in implementing the front-end of today's wireless communication devices. As previously mentioned, all the digital and analog components have already been integrated in the CMOS technology, and even some of the RF components have successfully been integrated, including LNAs, the mixers, and VCOs.

Nevertheless, the standard bulk CMOS technology still has physical bottlenecks to realize the full integration of all the components in the front-end of the wireless communication devices. Its limitations are originated from the intrinsic drawbacks of the standard bulk CMOS technology such as low quality (Q) factor due to the lossy substrate [1], low breakdown voltage of active devices [2], low mobility, and lots of parasitic parameters [3]. Especially, these disadvantages become more significant when the components of the front-end start dealing with watt-level high power signals. The components under this influence are the PA and the antenna switch, and the limitations of the standard bulk CMOS technology let the compound semiconductors, mostly the GaAs technology, dominate the markets for the PA and the antenna switch.

Even with the compound semiconductor technology, the PA and the antenna switch require special circuitries to control their behavior for improved performances. For example, the PA needs an adaptive bias circuitry to bias the power transistors at an

optimal bias point for higher efficiency and better linearity. The antenna switch uses a voltage higher than its nominal power supply voltage, 1.8 V or 3.3 V for instance, to ensure the linearity performance for watt-level high power signals. A boost DC-DC converter is necessary to generate the voltage higher than the power supply voltage. Due to its nature, these analog and digital control circuitries are typically implemented in the CMOS technology.

Today's general approach for the front-end design takes modules packaging one or more integrated circuits (ICs), for example: one CMOS IC and two or more compound semiconductor ICs, onto a board to perform a system function. This approach is known as SIP. For instance, one commercial front-end module consists of three different ICs and multiple off-chip passive components [4]. This approach suffers from high manufacturing cost and large die area.

Not only the integration but the performance improvement is also one of the difficulties that the current front-end modules face today. As various standards such as GSM, EDGE, and WCDMA are integrated in one device, the antenna switch becomes more complex having more ports for more standards, and it leads to a more stringent set of specifications for the antenna switch. Even more, the integration of more advanced standards for higher data rate requires the PA to be linear while maintaining high efficiency. This leads to the necessity of a special control scheme to control the PA.

1.2. MOTIVATIONS

As described in the previous section, the today's wireless communication industry is striving to integrate more standards in a single device and to integrate more components

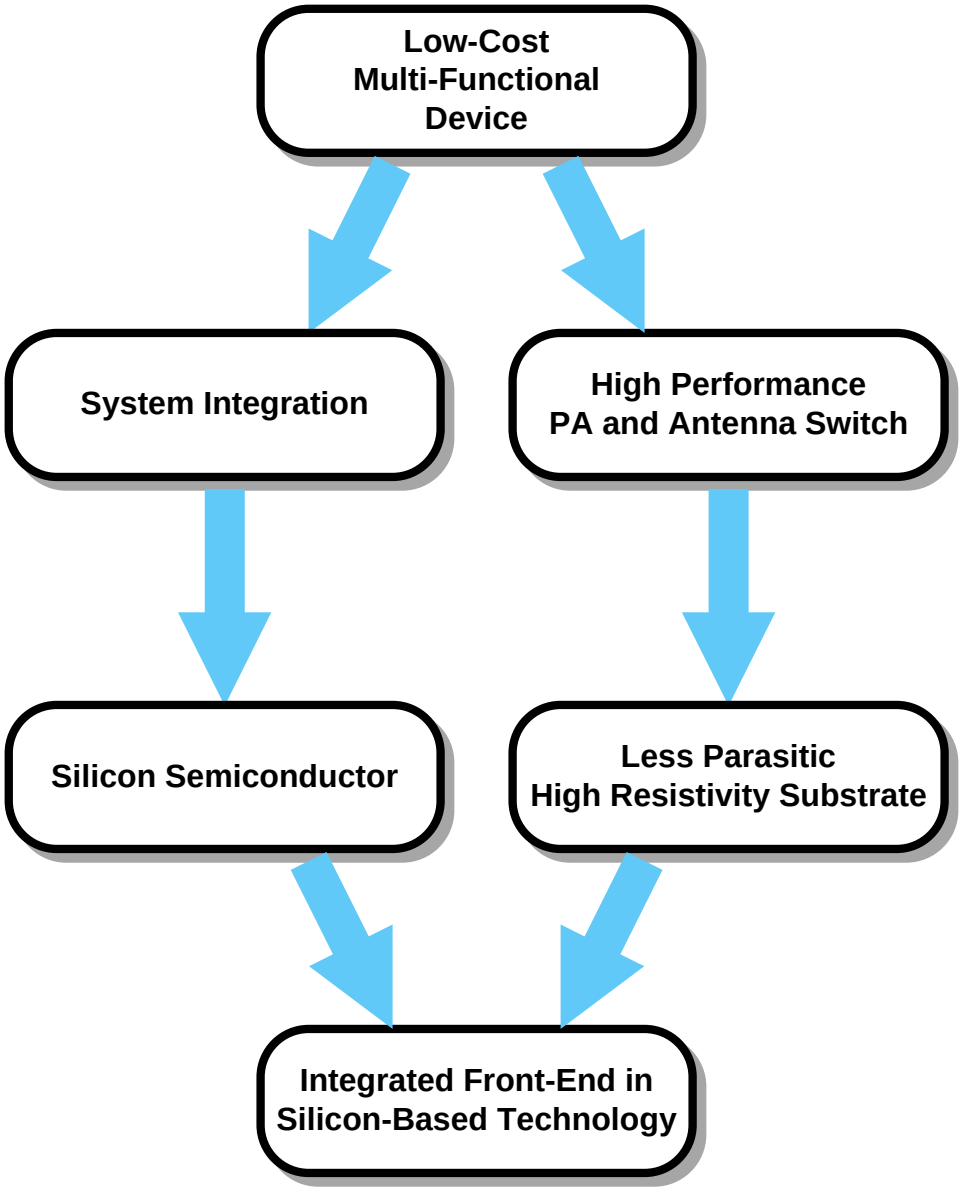


Figure 3. Approach to satisfy the needs of the current wireless communication industry.

in a single chip to perform a system function. This trend of the wireless communication industry brings two design respects.

First of all, the need for low cost, multi-functional devices drives system integration. The relatively low-cost CMOS technology allows the integration of digital components

and most RF components as previously mentioned. The CMOS technology even allows the integration of sensors such as image sensors. This integration capability is the key factor to achieve the low-cost, multi-functional devices. Secondly, the integration of multiple wireless standards necessitates the performance improvement of the front-end. For example, the power-handling capability of the antenna switch should be increased to cover high-power signals, and the linearity of the PA should be enhanced to cover non-constant envelope signals such as EDGE and WCDMA.

The approach to achieve these objectives is illustrated in Figure 3. The demand for the low-cost, multi-functional devices leads to the system integration and performance improvement. For the system integration, the silicon-based technology can be utilized to incorporate the digital components in the front-end as well as the RF components. For the performance improvement, the enhanced fabrication technology such as silicon-on-insulator (SOI) technology can be used as well as improved circuit techniques. Together, they lead to an integrated front-end design in the SOI technology to realize the low-cost, multi-functional wireless communication devices.

In this dissertation, the challenges that the current front-end design faces will be discussed first in Chapter 2. In Chapter 3,

CHAPTER 2
RADIO-FREQUENCY FRONT-END DESIGN

2.1. MULTI-STANDARD AND HIGH-POWER ANTENNA SWITCH

The challenges of designing an antenna switch are twofold. The antenna switch assumes very low insertion loss, and it is also expected to be linear while dealing with watt-level high power signal.

2.1.1. Insertion loss

The insertion loss of the antenna switch directly affects the overall performance of the front-end because it deals with very high-power signal generated by the PA. The causes of the insertion loss are shown in Figure 4. Most importantly, the insertion loss is proportionally related to the on-resistance of the ON-state transistors,

$$R_{ON} = \frac{L}{\mu C_{OX} W (V_{GS} - V_{TH})} \quad (1)$$

where L and W are the gate length and the gate width of a transistor, respectively, μ is the mobility, C_{OX} is the oxide capacitance, V_{GS} is the voltage difference between the gate and the source of the transistor, and V_{TH} is the threshold voltage. Due to its intrinsic low mobility compared to the GaAs counterpart, the antenna switch in CMOS technology generally shows higher insertion loss. Even with the antenna switch in the GaAs technology, stacking multiple transistors to handle high power over 30 dBm causes higher insertion loss because the on-resistance, R_{ON}, is increased. Increasing the width of the transistor reduces the insertion loss, but it degrades the isolation performance of the

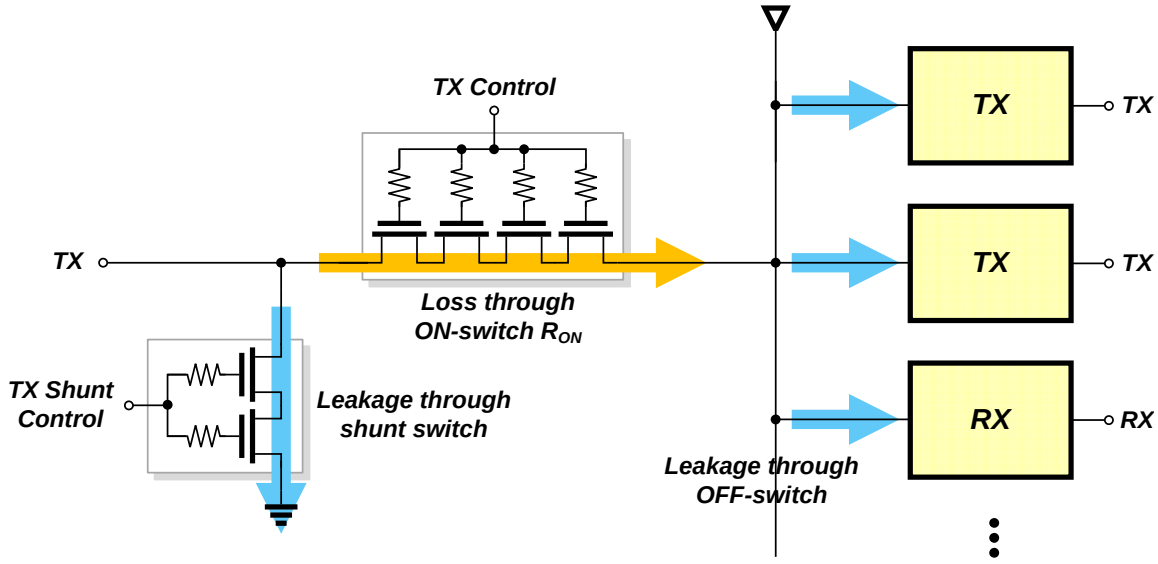


Figure 4. Insertion loss mechanisms of the antenna switch.

antenna switch because of the increased parasitic capacitance. Raising the gate-to-source voltage also helps reduce the insertion loss, but it requires an additional circuit to boost the voltage.

Other factors that affect the insertion loss of the antenna switch include the leakage through the shunt devices and that through the OFF switches as shown in the figure. The shunt devices are necessary to increase the isolation performance of the antenna switch. To reduce the insertion loss, the size of the OFF switches can be decreased. It, however, increases the insertion loss when they are turned on. So, it is necessary to be carefully determined.

2.1.2. Linearity

The antenna switch is expected to work as a passive component introducing no extra non-linearity. Since it is the last stage before an antenna, it should maintain the linearity

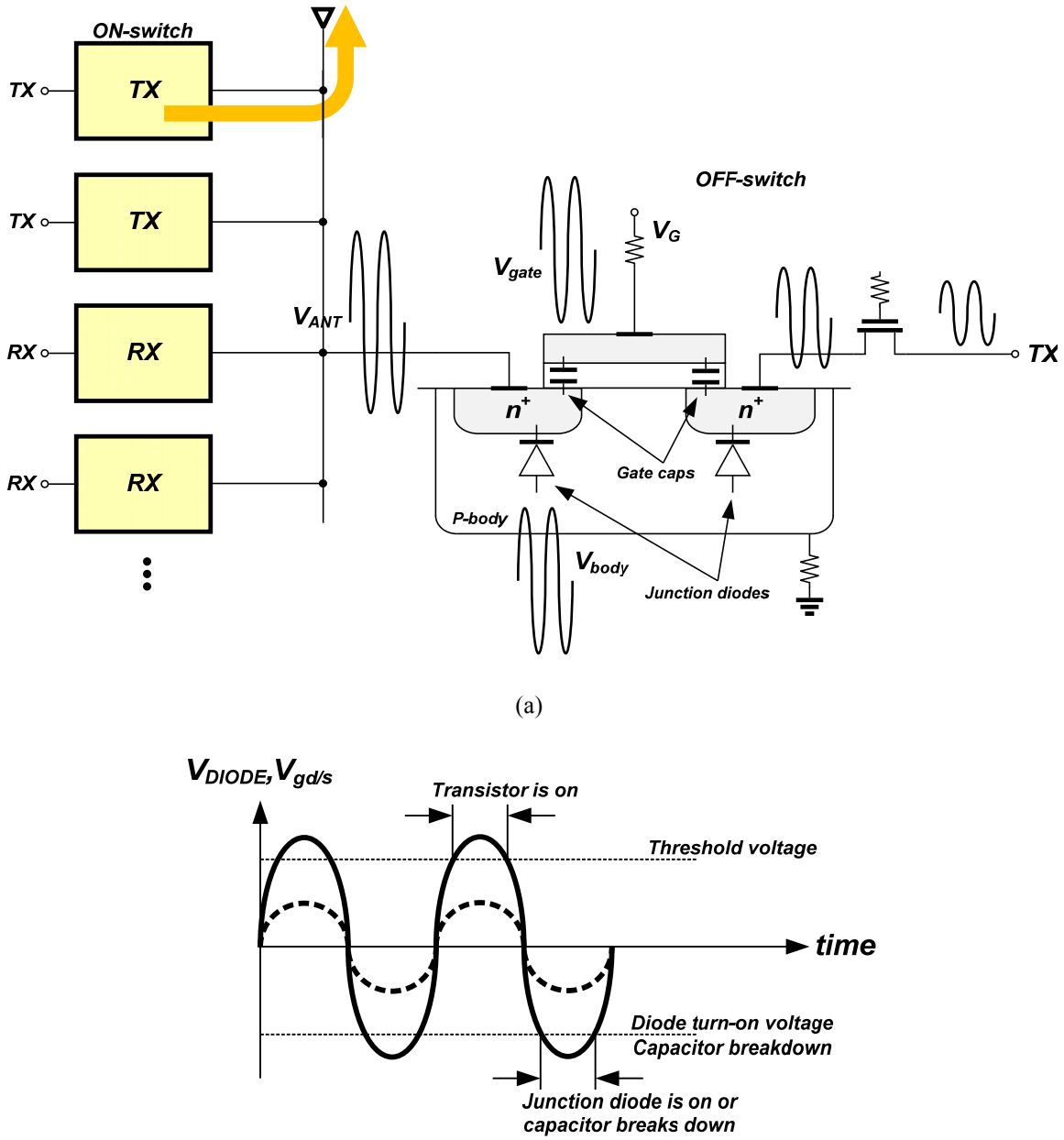


Figure 5. (a) Cross-sectional view of the OFF switch with voltage swings at each node and (b) voltage swing across the parasitic diodes and capacitors

of the signal generated by the PA to minimize the interference with other signal. However, most of the antenna switch shows active characteristic generating non-linearity.

The non-linearity mainly comes from the active device structure. Shown in Figure 5 is the active device of the CMOS technology. Figure 5 (a) shows the cross-sectional view of the OFF switch and voltage swings at each node. When the voltage swing is small as shown by the dotted line in Figure 5 (b), the junction diode does not turn on. However, when the high-power signal swing reaches negative voltage where the voltage difference across the parasitic junction diode becomes larger than the diode turn-on voltage, the junction diode turns on. This causes the output signal to be corrupted. Stacking multiple transistors to distribute the voltage swing or increasing the voltage at the gate can reduce the source of non-linearity, but they also require additional circuits. Furthermore, the low breakdown voltage of the CMOS technology prevents from using high voltage at its gate. In addition, the parasitic elements such as junction diodes and parasitic capacitances of the transistors distort the RF signal, adding non-linearity.

Table 1. Typical set of standards included in a SP7T antenna switch.

Standard	Frequency (MHz)	Typical Output Power (dBm)
GSM (850/900) TX	824-915	35
GSM 850 RX	869-894	N/A
GSM 900 RX	935-960	
DCS/PCS (1800/1900)TX	1710-1910	33
DCS RX	1805-1880	N/A
PCS RX	1930-1990	
WCDMA (UMTS)	1920-1980	27

2.1.3. Multi-standard operation

Today's wireless communication device supports many different standards including GSM, EDGE, and WCDMA, and so does the antenna switch. Shown in Table 1 is the typical set of standards included in a single pole seven-throw (SP7T) antenna switch. As the number of standards integrated in one device increases, it becomes more difficult to meet the requirements discussed above; the insertion loss and the linearity.

2.2. HIGHLY-LINEAR AND HIGHLY-EFFICIENT CMOS POWER AMPLIFIER

The disadvantages of the CMOS technology have slackened the development of the PA on a silicon substrate. The linearity and the efficiency of the CMOS PA were inferior to the GaAs counterpart. However, the advance of the CMOS technology has successfully shown its ability to support some of the standards such as GSM. By utilizing a switching amplifier such as class-E PA, the CMOS PA has shown the comparable efficiency performance to the GaAs PA [5-6]. Now, the issue on the CMOS PA is the linearity for the most part.

As more advanced modulation scheme, hybrid phase shift keying (HPSK) for example, became necessary for higher data rate, the linearity issue of the PA came to the fore. It is challenge to meet the linearity requirements while maintaining the high efficiency as achieved by the switching PA. Furthermore, there are number of parasitic elements such as variable transconductances and variable capacitances that hinder the PA from being linear. More detail about these challenges will be discussed in the following sections.

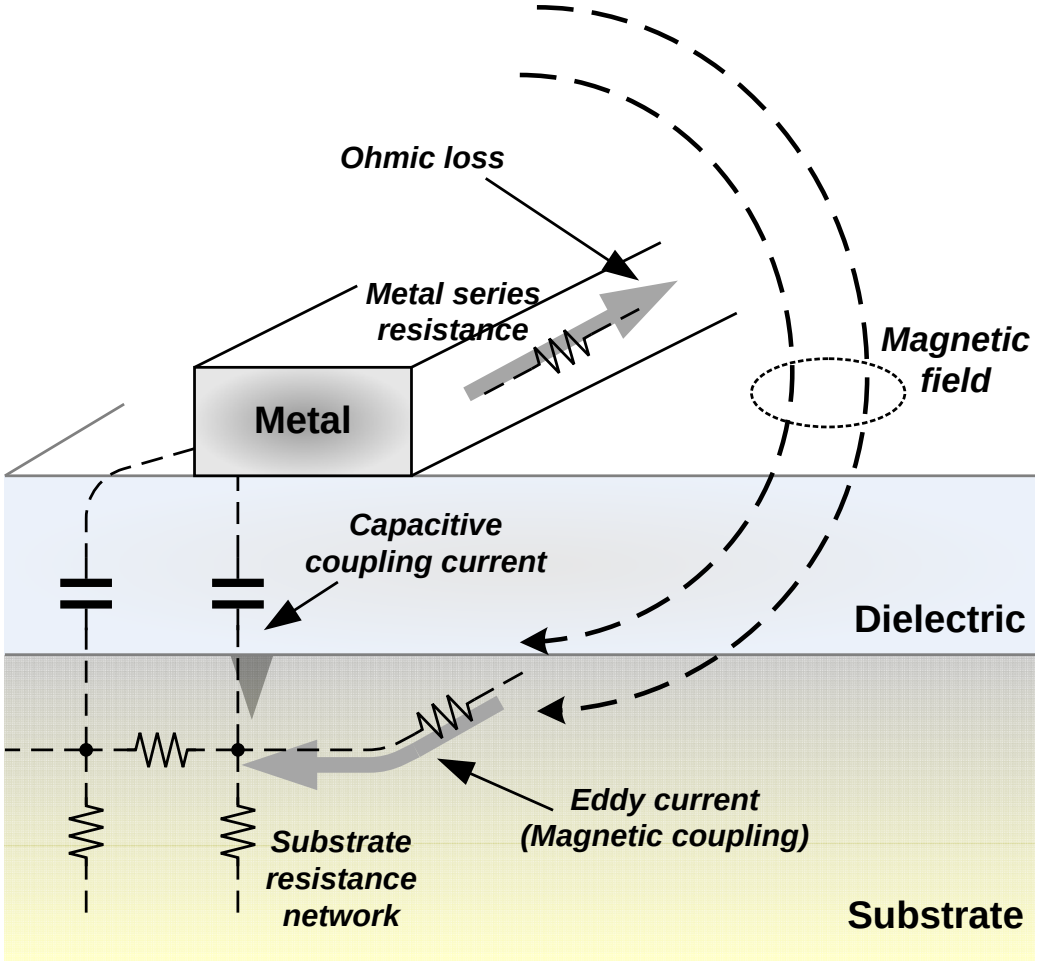


Figure 6. Loss mechanisms in the CMOS technology.

2.2.1. Reliability of the CMOS technology

The PA generates watt level of power, and its maximum voltage swing easily reaches 10 V. Unlike the GaAs hetero-junction bipolar transistor (HBT) with the breakdown voltage up to 20 V, the CMOS transistor, in general, can only endure the voltage stress up to the twice of the supply voltage [2]. The high voltage stress on the transistors may be the source of a reliability problem including the gate-oxide breakdown,

junction breakdown, and hot-carrier degradation [7]. Some of the phenomenon may be destructive and not reversible.

2.2.2. Low quality factor of passive elements

The performance of the PA is very sensitive to its output matching network which consists of passive elements such as an inductor and a capacitor, generally. Thus, a good percent of PA designs uses off-chip components for high Q factor of the passives in the matching network. Since the output power of the PA is watt level, a small different of the Q factor may cause a large difference in overall efficiency performance. The Q factor of the passive elements is mostly determined by the conductivity of the passive material for low frequency signals, DC for example, and the eddy current induced on the substrate material by the magnetic field for high frequency signals. The conceptual diagram of the loss mechanisms in the CMOS technology is shown in Figure 6. Compared to the GaAs counterpart, the CMOS technology suffers from thin metallization which results in more voltage drop in DC and lossy substrate which causes more eddy current to be generated in the substrate [8].

2.2.3. Inherent non-linearity

The CMOS technology has inherent non-linear parasitic elements, and the effect of them becomes more severe when a large signal is applied. The PA is the best example of that. In Figure 7, the non-linear parasitic elements of the CMOS technology are shown. One important factor among the sources of the non-linearity is the transconductance of the CMOS transistor as denoted by g_m. When a small signal is applied, the transconductance remains the same over the whole range of the input voltage swing.

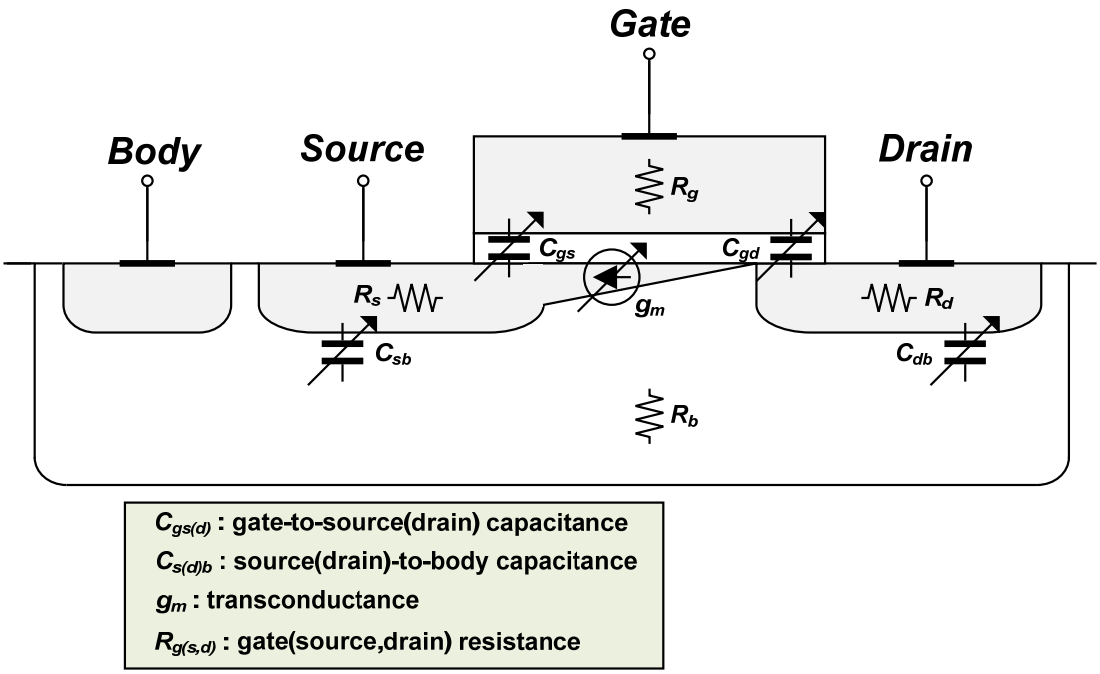


Figure 7. Non-linear parasitic elements of the CMOS technology.

However, when the signal is large, the variation of the transconductance becomes significant. Furthermore, as the frequency of operation increases, reaching gigahertz, the high order transconductances becomes considerable [9]. In addition to the variable transconductance, gate-to-source capacitance, C_{gs}, gate-to-drain capacitance, C_{gd}, and drain-to-body capacitance, C_{db}, also vary when the signal swing is large, adding non-linearity. It is very essential that the effects of these non-constant passive elements be avoided or minimized to meet the linearity requirements.

2.2.4. Multi-standard and multi-band front-end

A typical front-end consists of two major blocks: a PA and an antenna switch. Due to the disadvantages of the CMOS technology, these two blocks has usually been fabricated in the GaAs technology. Since control and power management blocks are implemented in

the CMOS technology, it is inevitable to have multiple ICs on the front-end package. Furthermore, the passive elements used in the output matching network of the PA are usually off-chip components such as low temperature co-fired ceramic (LTCC) or surface mounted technology (SMT). Having different ICs and off-chip passive components in one package increases package size and cost to build the package. So, it is desirable to integrate different components of the system into as smaller number of ICs as possible to reduce the size and the cost of the system.

2.3. PRIOR ARTS IN MULTI-STANDARD FRONT-END MODULE

Because of the disadvantages of the CMOS technology, the implementation of the PA and the antenna switch is still dominated by the GaAs technology for high performance. Typically, the PA and the antenna switch are fabricated in the GaAs HBT technology and in the GaAs pseudomorphic high electron mobility transistor (p-HEMT) technology, respectively. However, due to the fact that the depletion mode (D-mode) p-HEMT technology is lack of digital functionality, the enhancement and depletion mode (E/D-mode) p-HEMT technology emerged to integrate the digital functionality in a single die with the PA or the antenna switch. This technology, however, consumes a lot more area, compared to the CMOS technology, so the most of the control circuit is implemented in a separate die from the PA or the antenna switch.

Shown in Figure 8 is the block diagram of the front-end module that incorporates the PA and the antenna switch with associated controllers in a single module [4, 10-11]. The output matching network of the PA is implemented with off-chip passive components as well as the input matching network. The controller blocks for the PA and the antenna

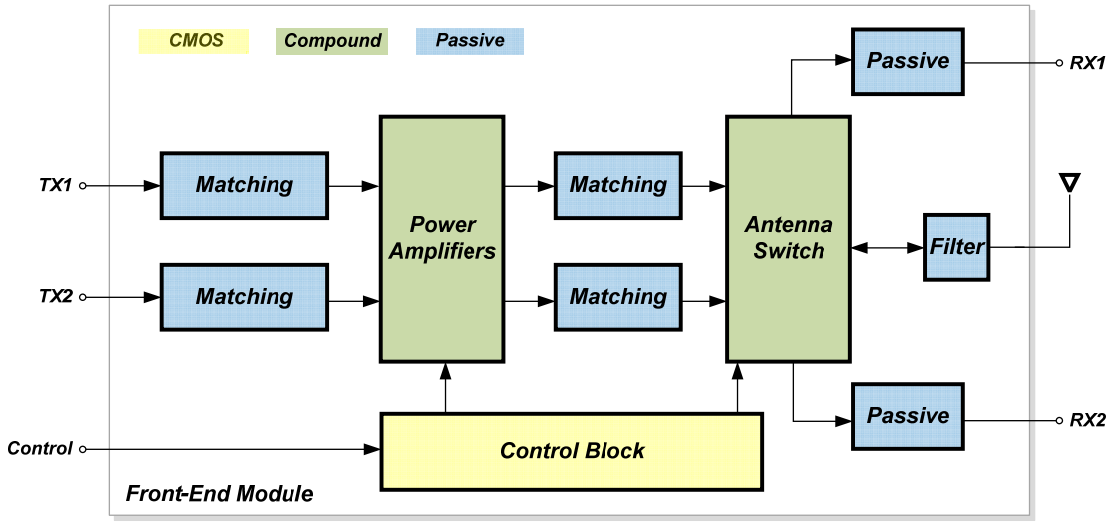


Figure 8. Block diagram of the multi-chip front-end module.

switch are implemented in the same die to reduce the number of components. However, there are still many different components that need to be assembled together, and it is directly related to the cost to build the front-end module. Furthermore, as mentioned above, the ICs are fabricated in a relatively high-cost technology, the GaAs technology.

2.3.1. Design techniques for the antenna switch

2.3.1.1. Multi-stacked FET structure

To alleviate the previously-described challenges of the antenna switch, many design techniques have been introduced. First of all, to increase the power-handling capability of the antenna switch, multiple FETs are stacked. A typical structure of the stacked FET is shown in Figure 9 as an example. As shown, the SPDT antenna switch has two RF ports and one port for the antenna. When one RF port is turned on, the other port is turned off by the control voltage at its gate. The OFF-state FETs share the voltage swing applied between its drain and source. If there is only one FET, the FET should sustain the high

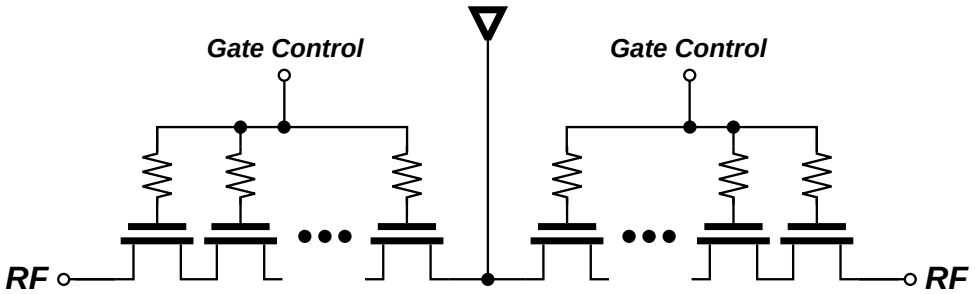


Figure 9. Typical multi-stacked FET structure for a SPDT antenna switch.

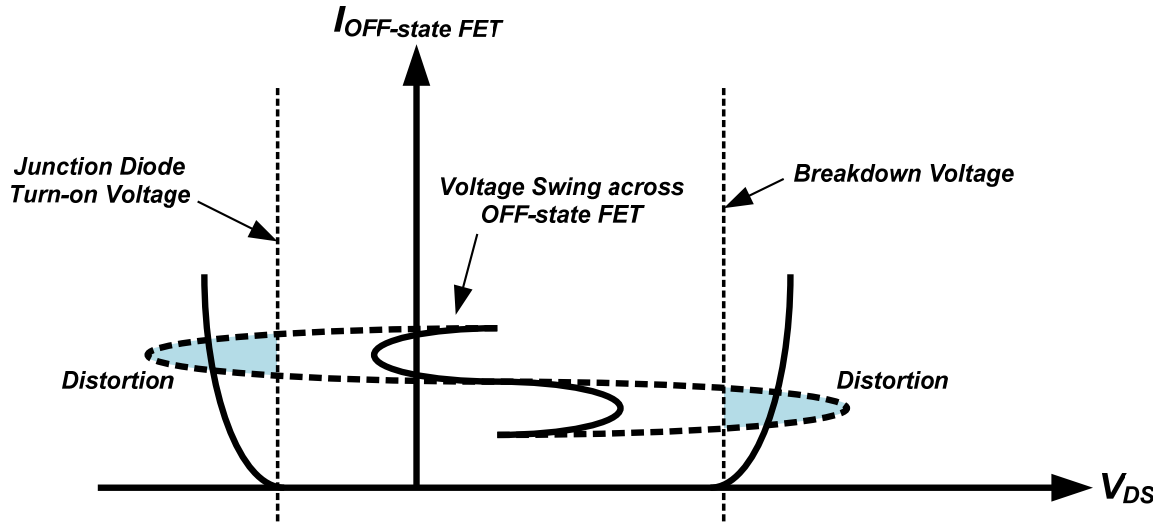


Figure 10. Illustration of the distortion caused by a large voltage swing.

voltage swing. It implies that the breakdown voltage of the FET should be at least as large as the RF voltage swing. The voltage swing can reach over 14 V when the power of the RF signal is 33 dBm in 50-ohm environment. The breakdown voltage of readily-available process technologies such as GaAs and CMOS technologies is less than this level, causing the distortion at the peak of the voltage swing as shown in Figure 10. Furthermore, the junction diodes of the FET should be kept reversely-biased at all times.

However, when the voltage swing of the RF signal gets larger, the junction diodes are turned on, allowing current flow. As shown in Figure 10, the large voltage swing across the OFF-state FET can cause the distortion at its minimum because of the current flow through the OFF-state FET. However, when multiple FETs are stacked to distribute the voltage swing, resulting in a reduced voltage swing for individual FETs, the OFF-state FETs do not turn on, minimizing the distortion caused by the effects described above. This can increase the power level that the antenna switch can handle without increasing the harmonic power levels, which is a measure of the linearity.

Nevertheless, the stacked-FET structure suffers from an increased insertion loss. Because the FETs are stacked in series, the on-resistance of the entire stacked FETs is increased. Thus, the number of the stacked FETs should be carefully considered. By increasing the width of the FETs, the insertion loss performance can be improved at the cost of the increased area of the antenna switch.

2.3.1.2. Voltage boosting method for GaAs antenna switch

The multi-stacked FET can improve the high-power handling capability, but it may be necessary to further increase the high-power handling capability of the antenna switch. This can be achieved by using the boosted voltage at its gate to control the GaAs antenna switch. Illustrated in Figure 11 is the effect of the voltage boosting method. As shown with the dotted line, the voltage swing is centered at the VGS of the OFF-state FET. With the nominal power supply voltage of 3 V, for example, the headroom between the center of the voltage swing and the threshold voltage of the D-mode p-HEMT device can not handle the large voltage swing of the watt-level RF signal. However, with the voltage boosting method, the center of the voltage swing is shifted to the left, allowing more

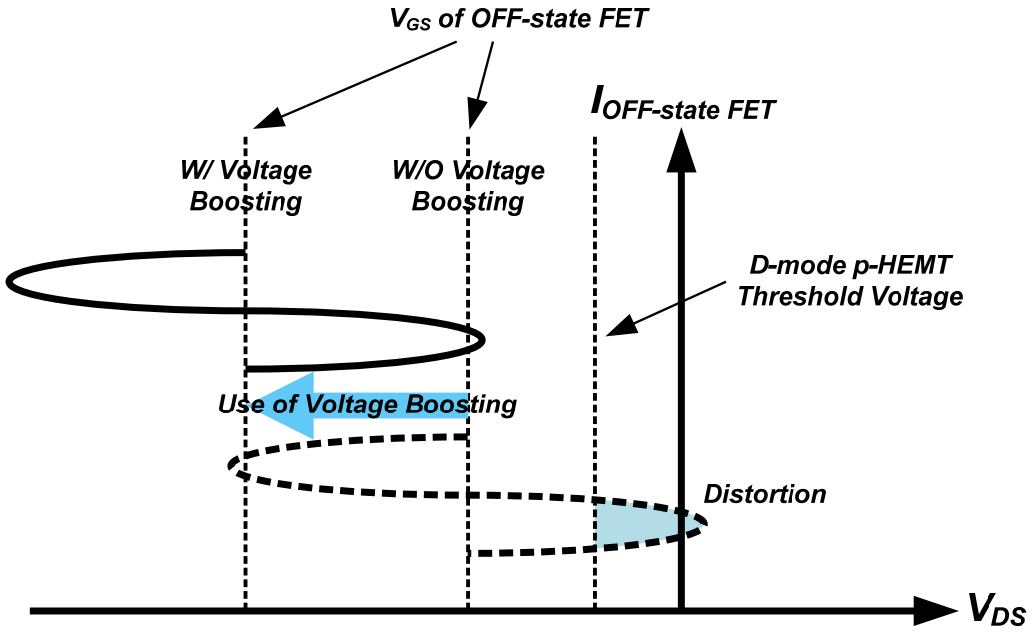


Figure 11. Illustration of the effect of the voltage boosting method.

headroom for the high-power RF signal to swing before the voltage swing reaches the threshold voltage. In this way, the power handling capability of the antenna switch can be improved further. Nevertheless, this method requires an extra circuitry to generate the high voltage to bias the FET, and this may increase the chip area the power consumption of the antenna switch.

2.3.1.3. CMOS body tuning structure

The junction diode of the CMOS technology is one of the most critical disadvantage to handle high-power signal. As shown in Figure 10, the voltage swing may go down below the junction diode turn-on voltage if the body of the CMOS FET is biased at ground. Since the turn-on voltage of the CMOS technology is very low, e.g. 0.7 V for 0.18-μm CMOS technology, the power-handling capability of the CMOS antenna switch is not able to cover watt-level RF signal.

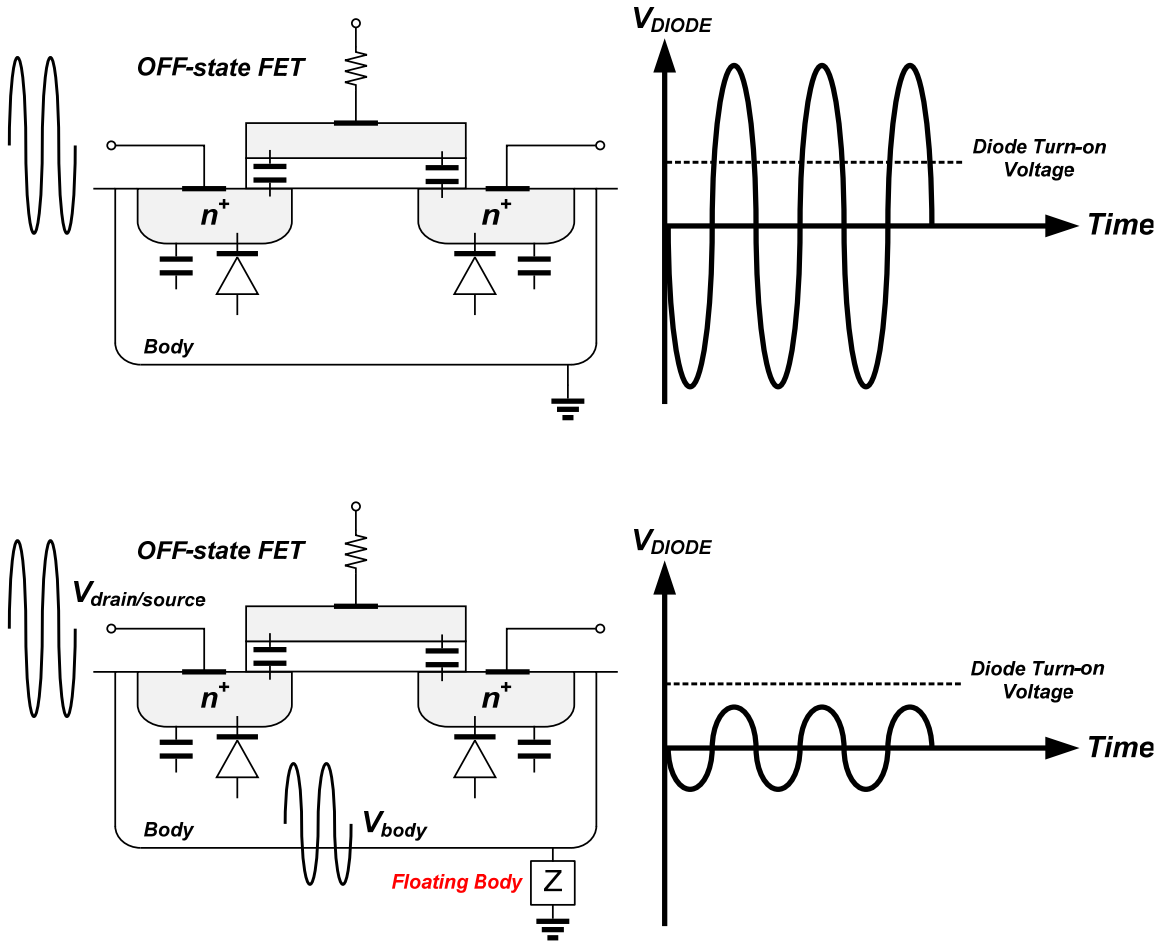


Figure 12. Voltage across the parasitic junction diode of CMOS technology.

Shown in Figure 12 is the voltage swings applied across the parasitic junction diode of the CMOS technology. When the body of the FET is biased at ground, the entire voltage swing applied at the source/drain of the FET is applied across the junction diode as previously discussed. A good portion of the voltage swing goes beyond the diode turn-on voltage, and this results in the distorted output signal through the antenna switch. To reduce the voltage swing and minimize the distortion caused by this effect, the body of

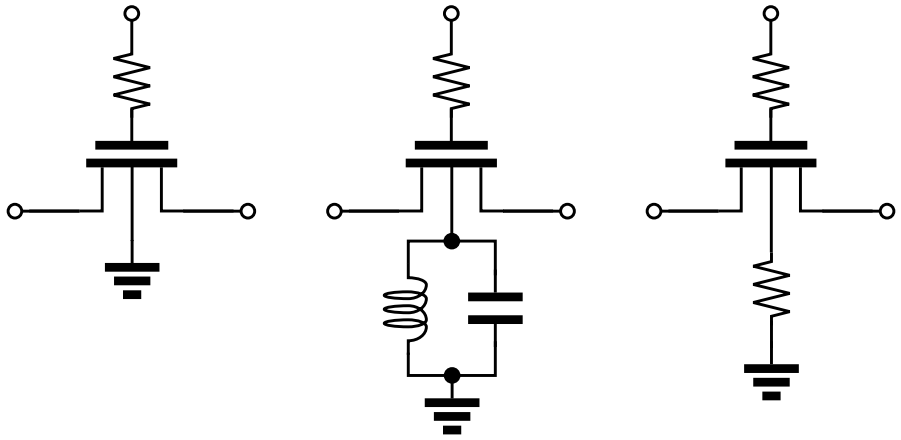


Figure 13. Implementation of body floating technique: (a) grounded body, (b) LC resonator, and (c) large resistor.

the FET can be floated as shown in the figure by using the high impedance as denoted by *Z*. With the floating body, the voltage swing across the junction diode can be the difference between $V_{drain/source}$ and V_{body}. This difference can be kept below the diode turn-on voltage.

The implementation of the high impedance can be in two ways as shown in Figure 13 [12]. Shown in Figure 13 (a) is the typical grounded body. In Figure 13 (b), the LC resonator is inserted between the body of the FET and ground to make the body float in terms of AC. Since an inductor is necessary to implement this structure, the size of this structure can be considerably large. The second way of implementation the high impedance without the increased area is shown in Figure 13 (c). Instead of using the resonator, a large resistor is placed between the body of the FET and ground. This can reduce the area greatly compared to the LC resonator implementation without performance degradation. However, this can only be implemented by using the CMOS

technology with the triple-well process available to access the body terminal of the FET. Otherwise, the body of the FET should be at global ground.

2.3.2. Design techniques for power amplifiers

2.3.2.1. Power combining techniques

The output power of the PA for cellular applications reaches watt level. The GSM application, for example, requires more than 33 dBm of output power. This is a challenging objective to achieve by using the CMOS technology due to its well-known disadvantages such as low breakdown voltage and low quality passives. Thus, it is necessary to overcome these weak points of the CMOS technology by using circuit techniques.

Depicted in Figure 14 are the typical power combining structures. The LC power combining method is popular, but it is not sutable for IC implementation because of the large size of inductors. As the frequency of operation increases reaching up to tens of gigahertz, this implementation can be a good candidate for the power combining. However, in the cellular applications, this can still be bulky. The transformer power combining method can be utilized to alleviate the issues on the increased size. As shown in the figure, the transformer power combining method can provide the impedance transformation and the power combining at the same time within comparably small area [13].

2.3.2.2. Linearity and efficiency improvement techniques

Unlike the old-generation wireless communications, today's wireless communication standards requires more advanced transmitter to increase the data rate in the given environment. For example, the GSM utilizes a constant-envelope signal so that the PA

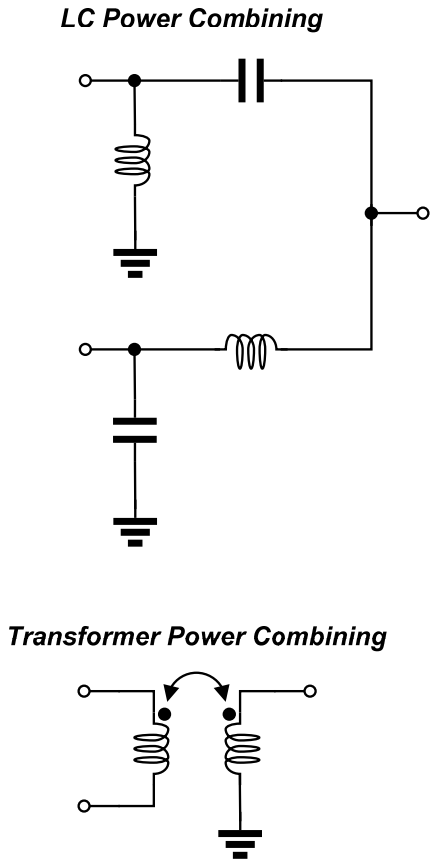


Figure 14. Typical power combining methods of power amplifiers.

does not need to be linear in generating the high-power RF signal. In contrast, the WCDMA or EDGE uses a non-constant-envelope signal. Thus, the PA should be linear to generate the high-power RF signal. By doing so, the efficiency of the PA is degraded, reducing the batter life of the wireless communication devices.

There have been a lot of researches to improve the linearity of the PA without sacrificing the efficiency performance such as Doherty PA [14] and Polar PA. These techniques have been adopted in implementing the base-station PA. The simplified illustration of the Polar PA is shown in Figure 15. The saturation PA is utilized with the

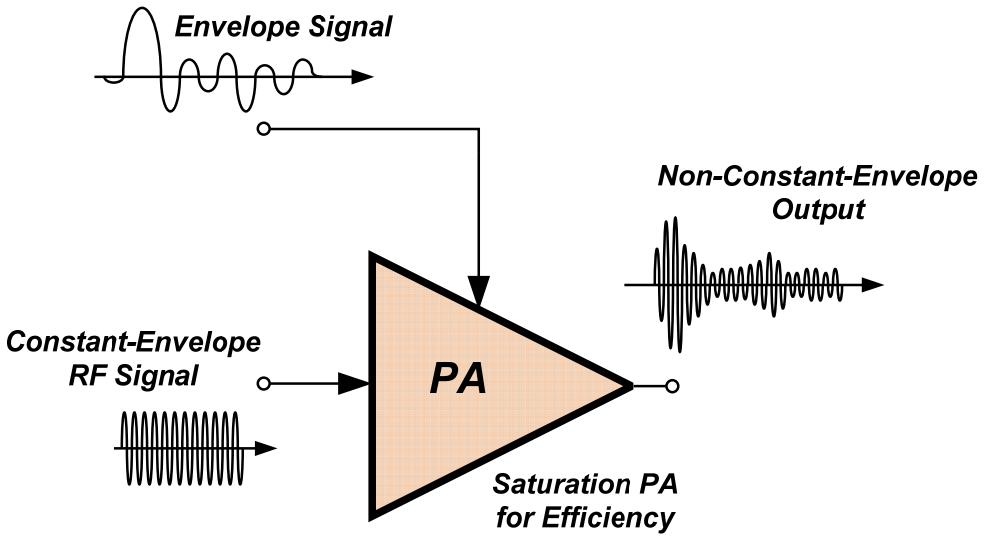


Figure 15. Simplified illustration of the Polar PA structure.

constant-envelope RF signal as an input to maximize the efficiency of the PA. The envelope information is used to vary the V_{DD} of the PA. The output of the Polar PA is now non-constant-envelop signal which has information in the envelope and the phase as well. In the mobile applications, however, these techniques have not been very successful because of the poor passive performances, difficulties to precisely align the phase and the envelope, etc.

In the mobile applications, simpler implementations such as input capacitance cancellation technique [15] and pre-distortion technique are more suitable without any necessity of complicated circuitries. As shown in Figure 16, the PMOS transistor which has the opposite characteristics of the NMOS transistor can be used to make a flat capacitance over the gate-to-source voltage range. Since the variable gate capacitance of the NMOS is one of the most critical factors in the non-linearity, it is very effective to flatten the capacitance over the gate-to-source voltage variation. Shown in Figure 17 is

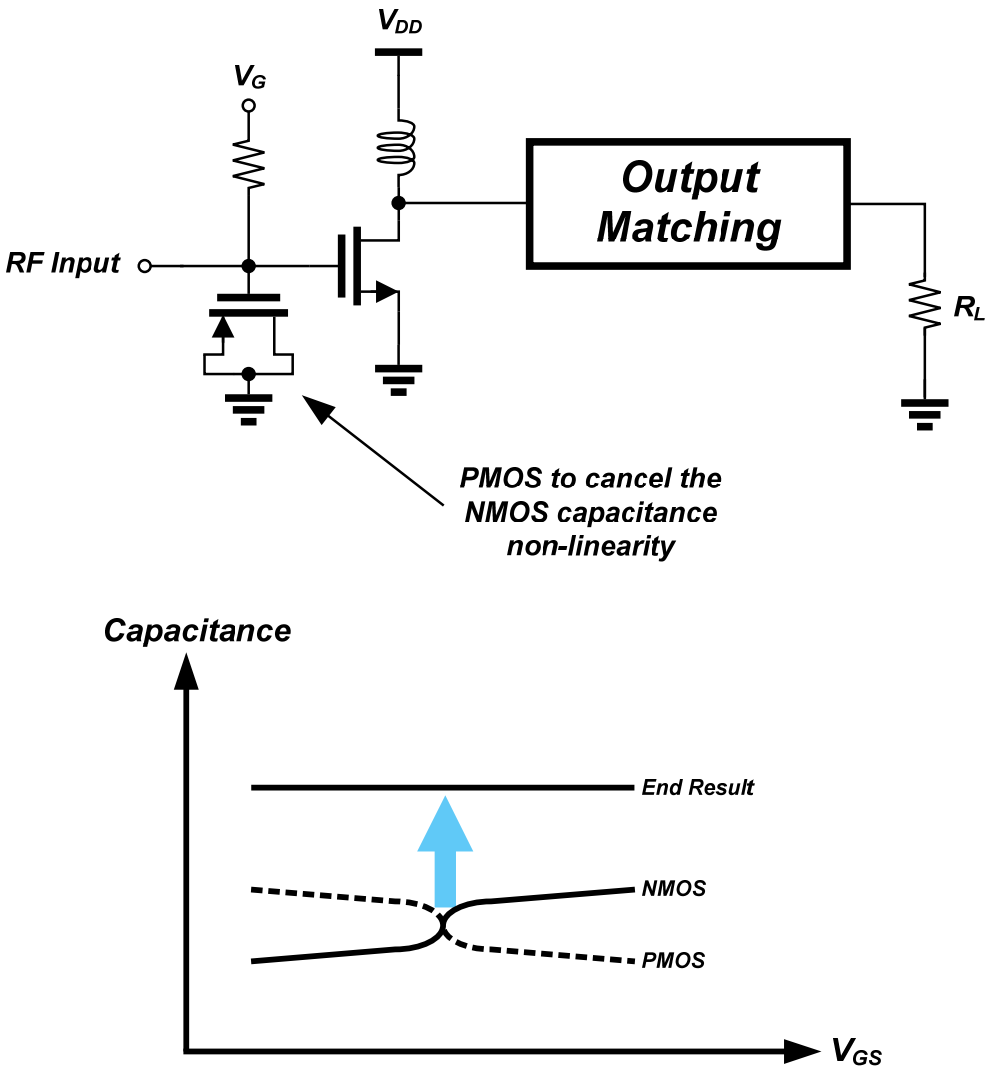


Figure 16. Capacitance cancellation technique and its effect.

the pre-distortion technique. If the transfer characteristics of the PA are known, the pre-distortion intentionally adds non-linearity to the input signal, which is the opposite to the characteristics of the PA. Then, the output becomes linear as shown in the figure. Even with these techniques, it is necessary to precisely obtain the characteristics of the NMOS transistors and the PA for the capacitance cancellation technique and the pre-distortion

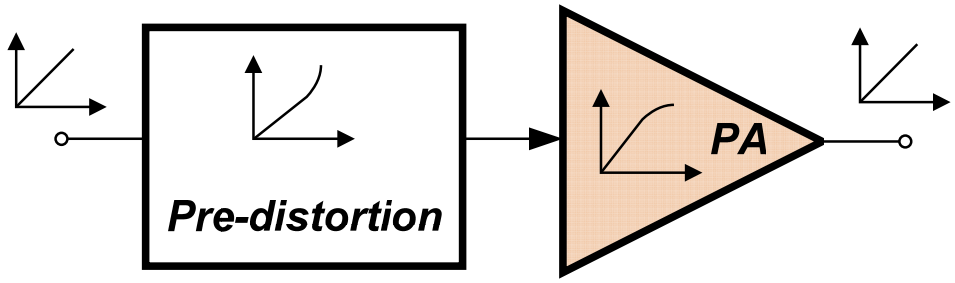


Figure 17. Pre-distortion technique.

technique, respectively. It requires great amount of time and effort to concisely extract the characteristics. Furthermore, there need to be extra circuitries to implement these techniques.

CHAPTER 3

GAAS p-HEMT ANTENNA SWITCH CONTROLLER

The research was initially focused on the implementation of the multi-standard and multi-band antenna switch and its performance improvement by revising the control scheme of the antenna switch.

The most important requirements of the antenna switch are the insertion loss and the linearity. They are closely related to the control scheme as well as the antenna switch architecture. So, the primary research was focused on the controller design to improve the antenna switch performance, especially the insertion loss and the linearity. The antenna

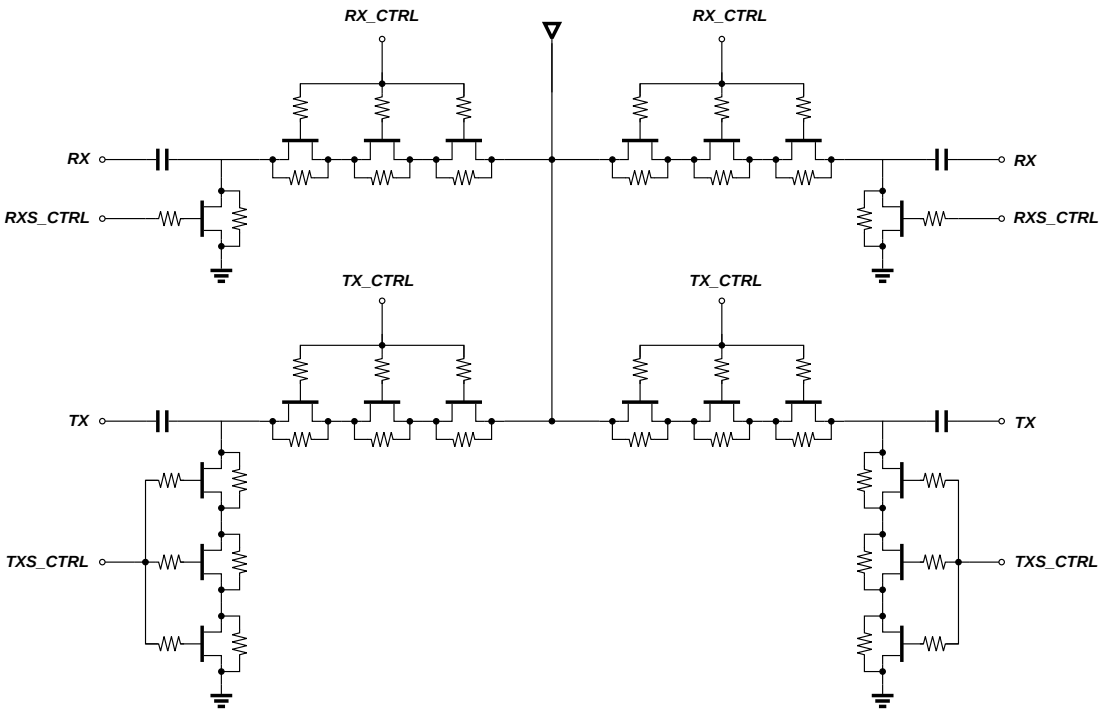


Figure 18. GaAs SP4T switch design for the multi-standard and multi-band operation.

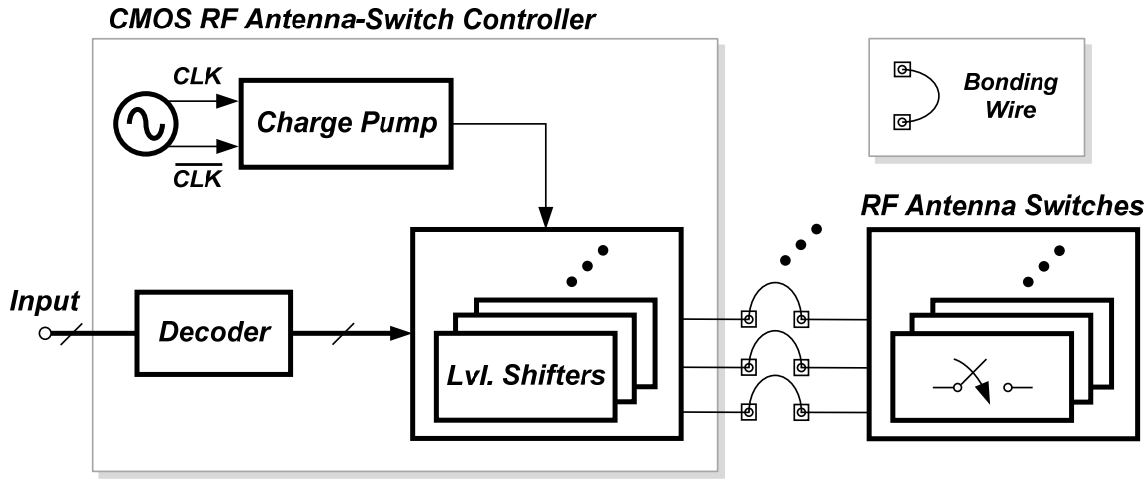


Figure 19. Block diagram of RF antenna-switch controller.

switch used in the initial research was implemented in the GaAs p-HEMT technology, and it has three stacks for each TX path to handle up to 35 dBm of power since one transistor can only handle 30 dBm of power. The circuit diagram of the antenna switch is shown in Figure 18. The number of throws of the antenna switch was chosen to be 4, covering two RX ports and two TX ports. The shunt devices were included to increase the isolation between the ports. Three devices are stacked for TX shunt devices to handle high power. To improve the linearity of high power signal without degradation of the insertion loss, the control voltage, denoted by TX_CTRL in the figure, should be higher than a power supply voltage. If the control voltage is lowered, the number of stacks of the transistors should be increased. This causes higher insertion loss. The target control voltage is above 6 V to keep the number of stacks. Thus, in the following section, the controller design will be discussed in detail.

3.1. ANTENNA-SWITCH CONTROLLER OVERVIEW

The block diagram of the antenna-switch controller that employs a charge pump is shown in Figure 19 [16-17]. The antenna-switch controller consists of four sub-blocks: an oscillator, a charge pump, a decoder, and level shifters. As shown in Figure 19, the oscillator generates two out-of-phase clock signals to drive the charge pump. Before the charge pump, there is an inverter chain as a clock buffer to provide adequate drive to the charge pump. Using the clock signals out of the buffer, the charge pump creates a voltage higher than power supply voltage. This high voltage is connected to level shifters, and the level shifter output switches between the high voltage and ground according to the decoder output. A conventional level shifter is used as in [17-18]. The decoder is utilized to reduce the number of input signals needed to control multiple antenna switches.

3.2. CHARGE PUMP

The charge pump is the most important block in the antenna-switch controller since it generates the desired voltage to the antenna switch. The first integrated charge pump to generate a voltage higher than a power supply voltage was introduced in [19]. This charge pump, however, suffers from a threshold voltage drop, resulting in a lower voltage gain and efficiency. For higher gain, many modified charge pumps have been proposed [20-35]. To avoid the threshold voltage drop of the diode-connected transistors, additional MOS switches were used with the diodes [27]. Then, the charge pump using only MOS switches was introduced to further increase the voltage gain [31]. The more complex clock scheme was also used for higher efficiency [24].

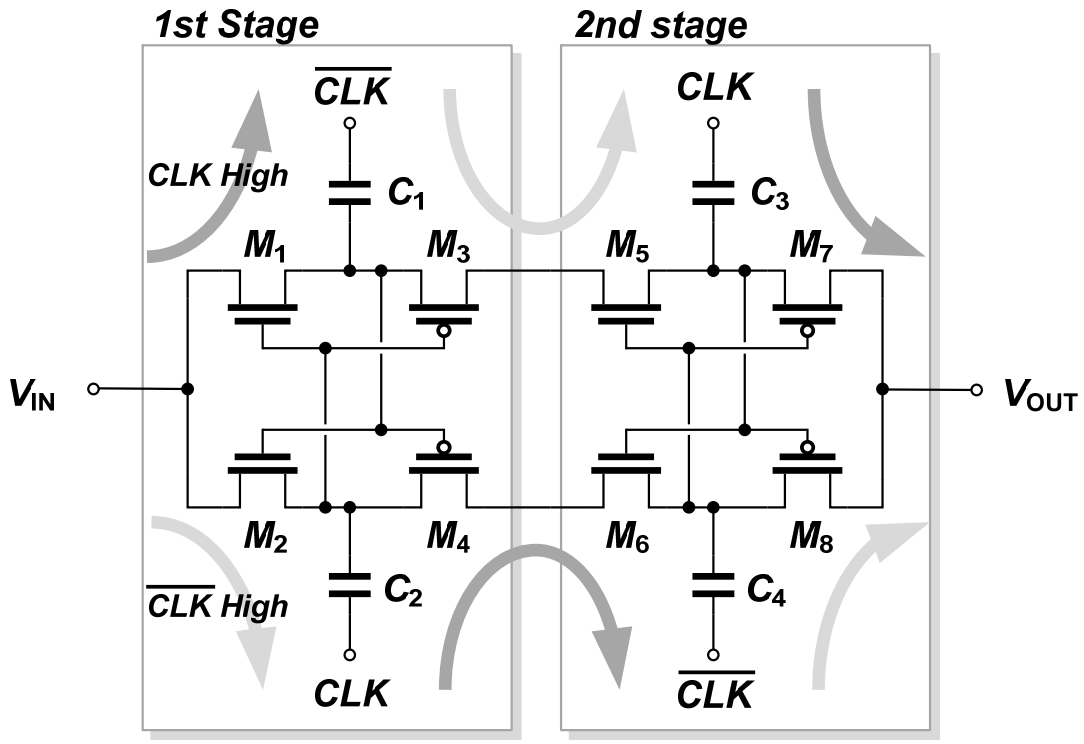
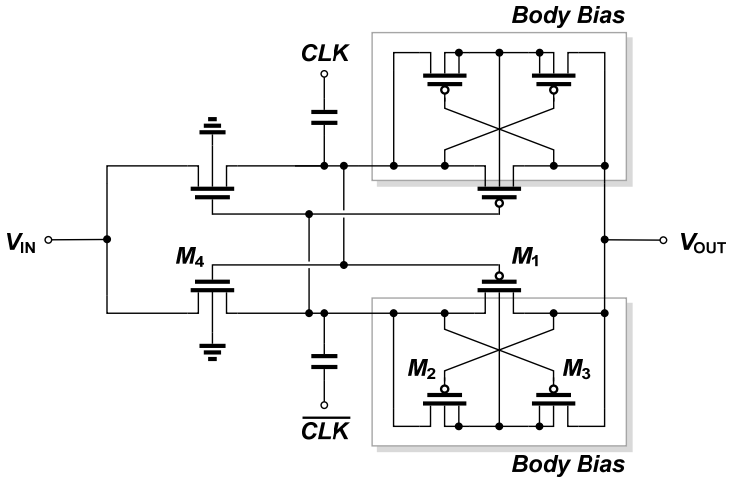


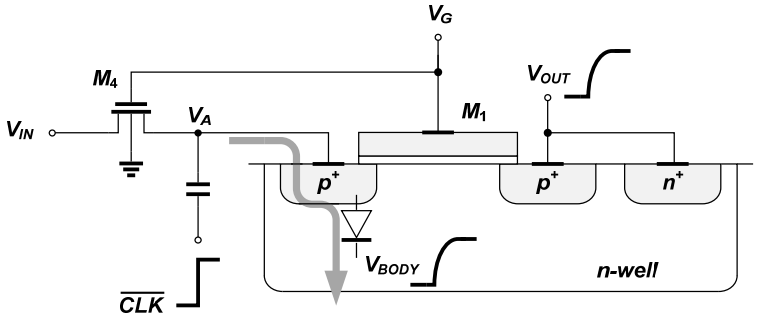
Figure 20. Circuit diagram of a two-stage charge pump with only MOS switches.

3.3. CHARGE PUMP OPERATIONS

Figure 20 is the circuit diagram of a two-stage charge pump with MOS switches only [31]. Each stage of the charge pump is composed of four MOS switches, M_1-M_4, and two charging capacitors, C_1 and C_2. In one clock period, the MOS switches connecting two stages, for example, M_4 and M_6, are closed to pump charges into the next stage while the other MOS switches, M_2 and M_8, are open to prevent the current from going back to the previous stage. In the next clock period, M_4 and M_6 are open to block the reverse current, and M_2 and M_8 are closed to charge the next stage. For instance, if CLK is low, the gate voltage of M_2 and M_4 becomes higher than its source/drain voltage because $\overline{CLK}$ is high



(a)



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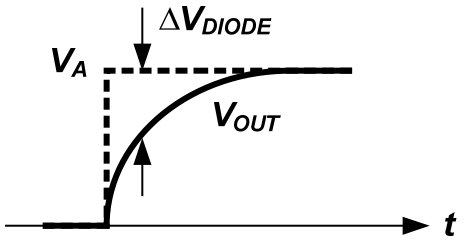


(c)

Figure 21. (a) Body biasing circuit diagram, (b) cross-sectional view of the PMOS switches, and (c) illustration of the voltage difference of the junction diode.

and the voltage across C_1 is added to $\overline{CLK}$. Since M_2 is closed and M_4 is now open, C_2 is charged until next clock cycle comes as indicated with light arrows in Figure 20. This process keeps repeating in a complementary manner as shown with arrows until all the charging capacitors are charged to the power supply voltage if there is no output current. However, if there is output current, the charge pump should keep pumping in the extra charges every period at the cost of voltage drop. Therefore, it is necessary to identify the output current prior to the charge pump design to generate a certain voltage level. The voltage drop also depends on the charging capacitance and the on-resistance of the MOS switches. Thus, it is important to choose proper values of the charging capacitance and the MOS-switch width to design the charge pump, assuming the length of MOS switches are at minimum. At the end of the charge pump, there is an output capacitor acting as a filter that reduces ripple generated by the complementary charge pumping.

3.4. BODY BIASING TECHNIQUE

In Figure 21 (a), the body biasing circuit for the PMOS switches of the charge pump is shown. The auxiliary PMOS switches, M_2 and M_3, connect the higher between the drain and the source of M_1 to the body [17, 28]. The body biasing circuit is necessary to keep the junction diodes between the drain/source and the body of the MOS switches reverse-biased at all time even before the voltage of the following stage is charged higher. As shown in Figure 21 (b), if the body of the MOS switch is tied to the output, the output voltage is lower than that of V_A, making the voltages at each node of the junction diode as shown in Figure 21 (c). This forward-biases the junction diode and allows charges to be dumped into the body as shown in Figure 21 (b). This may cause latch-up and can

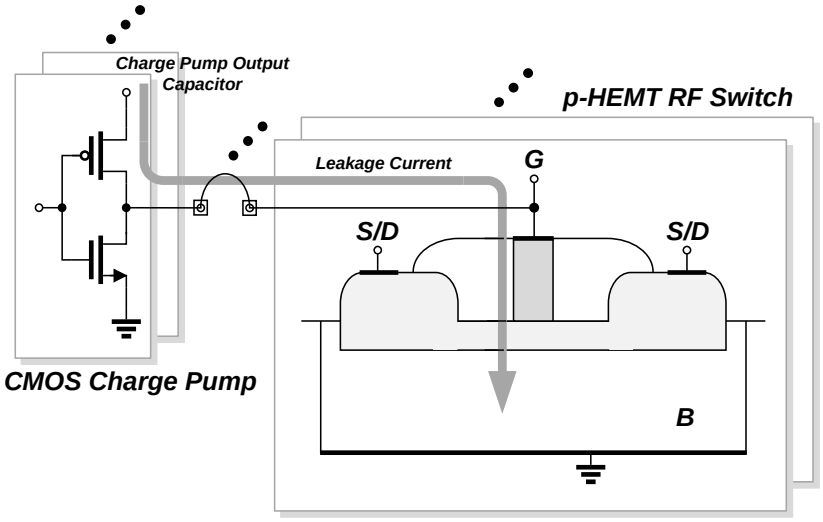


Figure 22. Illustration of the leakage current drawn from the charge pump, reducing the output voltage.

damage the device. Thus the body bias circuit is employed to prevent these problems for the charge pump circuits shown in Figure 20.

3.5. LOAD CONSIDERATIONS

The antenna switch should ideally be seen as an open to the charge pump due to the nature of the p-HEMT since the charge pump output is connected to a gate terminal. Thus, no charges can be drawn out from the output capacitor of the charge pump, resulting in no voltage drop. However, leakage current creates a current path from the charge pump to ground as shown in Figure 22 [36]. When the output voltage of the charge pump is connected to the gate of the antenna switch to turn it on, the ideal open circuit looking into the gate becomes resistive because of the leakage current, and the quantity of the current is not negligible because the antenna switch is very large in size for high RF

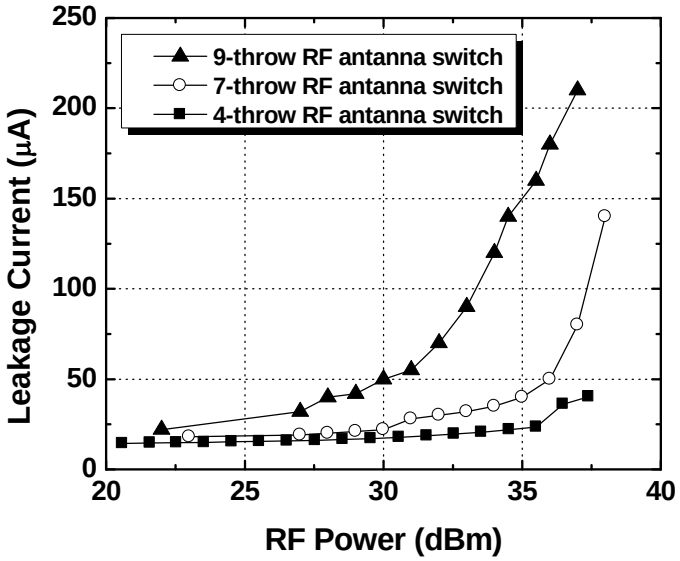


Figure 23. Measured leakage currents from the charge pump to ground with different number of antenna switch.

power. As the number of antenna switches increases to cover multiple wireless standards, the leakage current becomes larger as shown in Figure 22. Moreover, the leakage current further increases as RF power going through the p-HEMT device rises because the voltage at the gate increases with higher RF power [36-37]. This non-negligible leakage current becomes problematic in designing the antenna switch controller unlike memory or LCD applications because it decreases the output voltage of the charge pump. The measured increasing leakage current is shown in Figure 23. As shown, the leakage current depends on the number of antenna switches and RF power. This non-negligible leakage current flow lowers the output voltage of the charge pump, degrading linearity and isolation performances of the antenna switch [38]. Therefore, it is important to consider the load condition for the charge pump design, especially for multiple throw antenna switch. The design techniques described in following section take into account

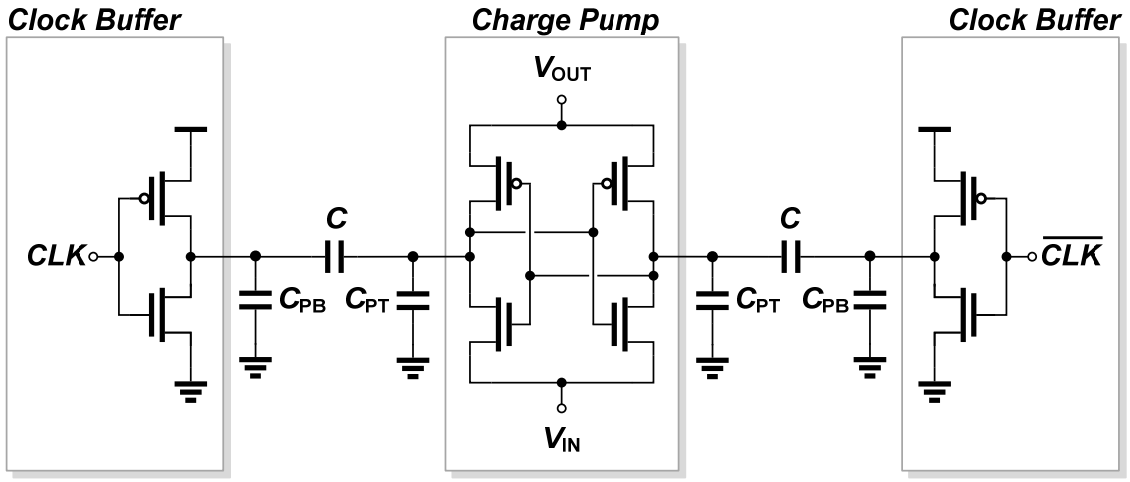


Figure 24. Circuit diagram showing one stage of a charge pump with parasitic capacitances and clock-buffer stages.

these loading effects in designing the charge pump.

3.6. CHARGE PUMP CIRCUIT ANALYSIS AND DESIGN

The circuit diagram of the charge pump with parasitic capacitances is shown in Figure 24. C is a charging capacitor, and C_{PT} and C_{PB} are parasitic capacitances at the top layer and the bottom layer of the charging capacitor, respectively. In addition, C_{PT} includes the parasitic capacitance of the charge pump MOS switches, and C_{PB} includes the parasitic capacitance of the clock buffer.

The first integrated charge pump was introduced and analyzed in [19]. The output voltage of the charge pump is given by

$$V_{OUT} = V_{IN} + NV_{GAIN} - \frac{NI_{OUT}}{(C + C_{PT})f} \tag{2}$$

where V_{IN} is the input voltage to the charge pump, V_{GAIN} is the voltage gain of each stage,

N is the number of stages, I_{OUT} is the output current, and f is the clock frequency. The input voltage and the gain of each stage are reduced because of the threshold voltage and can be written as

$$V_{IN} = V_{DD} - V_T \tag{3}$$

and

$$V_{GAIN} = \left(\frac{C}{C + C_{PT}}\right) V_{DD} - V_T, \tag{4}$$

respectively. Due to its generality, (2) has been used as a model even for different topologies using MOS switches and capacitors as the charge-pumping medium. There are, however, several aspects to be considered for a better description of the output voltage such as on-resistance of the MOS switches, especially for the topology shown in Figure 20 and Figure 24.

The output voltage of the topology shown in Figure 24 can be divided into four elements as

$$V_{OUT} = V_{IN} + N(V_{GAIN} - \Delta V_I - \Delta V_{RC}) \tag{5}$$

where ΔV_I is the voltage loss due to the output current and ΔV_{RC} is the voltage loss caused by the RC network, which is composed of the MOS-switch on-resistance and the charging capacitance including its parasitics. The first two elements, V_{IN} and V_{GAIN}, are the same as (2) except that the topology in Figure 24 does not suffer from a threshold voltage drop [31].

To provide the output current, each branch of the charge pump delivers charges of $(C+C_{PT})\Delta V_I$ for each half clock period. Thus, the voltage loss due to the output current at each stage is given by

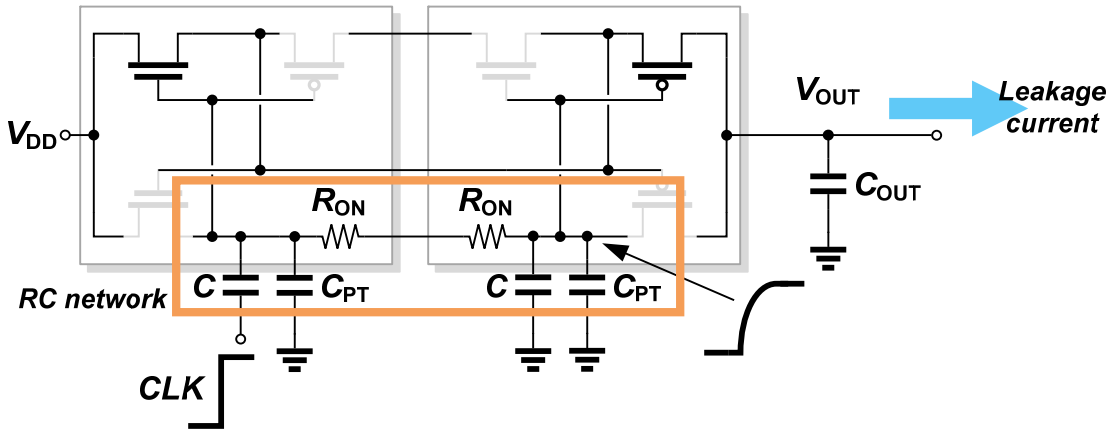


Figure 25. Parasitic RC network.

$$\Delta V_I = \frac{I_{OUT}}{2(C + C_{PT})f} \tag{6}$$

where the factor 2 reflects the parallel structure of the charge pump in Figure 24. The parasitic capacitance comes from the top-layer connections of the charging capacitors and the gate/drain capacitances of the MOS switches and is given by

$$C_{PT} = \alpha C + C'W \tag{7}$$

where α is the ratio between the charging capacitance and the top-layer parasitic capacitance, $C'W$ is the parasitic capacitance of the MOS switches, and W is the width of the MOS switches.

As the clock frequency reaches tens of mega-hertz or higher to reduce ripple of the output voltage, the on-resistance of the MOS switches and the charging capacitance with its parasitic form a relatively slow RC network, as shown in Figure 25, compared to ideal square signals, resulting in the voltage loss. The voltage loss can be written as

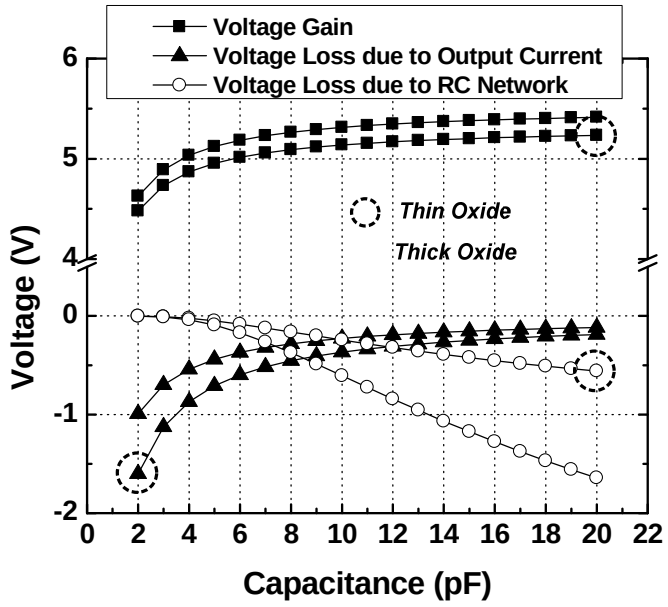
$$\Delta V_{RC} = kV_{DD}\left(\frac{C}{C + C_{PT}}\right)e^{\frac{-1}{2R_{ON}(C+C_{PT})f}} \tag{8}$$

where R_{ON} is the on-resistance of the MOS switches. The factor k in (8) is introduced to prevent the voltage loss from being over-emphasized, and this quantity depends on the output current because the increased output current further slows the charging process of the RC network. The k value tends to increase to reduce the output voltage as the size of the clock buffer decreases. Since the current level to charge the RC network is reduced with smaller buffer, it takes longer to charge the RC network, resulting in the voltage drop. The buffer size brings trade-off between the current consumption and the voltage drop as other design parameters. The effects of the buffer size will be discussed in the following section.

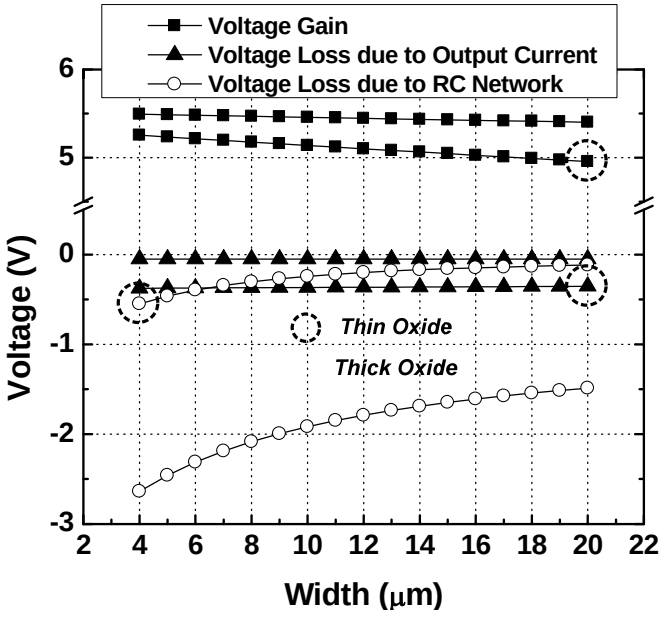
Substituting (6)-(8) into (5), the output voltage can be written as

$$V_{OUT} = V_{DD} + \left(\frac{N}{C + \alpha C + C'W}\right) \times \left(CV_{DD} - (k' + k''I_{OUT})CV_{DD}e^{\frac{-W}{2R'(C+\alpha C+C'W)f}} - \frac{I_{OUT}}{2f}\right) \quad (9)$$

where R' is the resistance per unit width of the MOS switches, and k' and k'' are experimentally determined factors to include the effects of the RC network. To provide insight on how the charging capacitance and the width of MOS devices change the output voltage, Figure 26 (a) and (b) are included. This shows the contributions toward the output voltage from each term in (5) with N being 2. It can be noted that, unlike (2), the output voltage is a function of both the charging capacitance and the width of the MOS switches. At first, the voltage gain increases as the charging capacitance increases. However, the voltage loss due to the RC network increases while the voltage gain saturates as shown in Figure 26 (a). Thick MOS devices suffer from higher voltage loss as charging capacitance increases due to more parasitic capacitance and lower



(a)



(b)

Figure 26. Simulated voltages of each term in (4) toward the output voltage with (a) different charging capacitances and (b) with different widths of MOS devices.

transconductance. The width was fixed to be 10 μm. In Figure 26 (b), increasing width helps to decrease the voltage drop due to the RC network, but it decreases the voltage gain as well. In this case, thick MOS devices suffer from the slow RC network in a lot greater degree than thin MOS devices. The capacitance was set to be 10 pF. As a result, these two parameters should be deliberately chosen to generate the higher output voltage while providing the required output current. Moreover, it can be noted that the output current in (9) has larger effect on the output voltage compared to the analysis in (2). Hence, the load considerations described in Section III should precede the charge pump design. The proposed analysis allows to precisely expect the behavior of the output voltage as the charging capacitance and the width of MOS devices vary.

The current consumption of the charge pump in Figure 24 ideally depends only on the amount of the output current. However, the parasitic capacitances increase the current consumption of the charge pump [39]. The extra current consumption includes the dynamic current to drive the parasitic capacitance at the top layer of the charging capacitors and that at the bottom layer. Considering these parasitic effects, the current consumption of the charge pump is given by

$$I_{POWER} = (N+1)I_{OUT} + N(I_{CLK} + I_{ST}) \tag{10}$$

where I_{CLK} is the current to drive the bottom-layer parasitic capacitance and I_{ST} is the current to drive the top-layer parasitic capacitance. They can be written as

$$I_{CLK} = 2\beta C V_{DD} f \tag{11}$$

and

$$I_{ST} = 2(\alpha C + C' W)\Delta V_n f \tag{12}$$

where β is the ratio between the charging capacitance and the bottom-layer parasitic

capacitance and ΔV_n is the voltage swing across the charging capacitor. ΔV_n is the same as V_{GAIN} in (5). The factor of 2 in (11) and (12) comes from the parallel structure of the charge pump. Substituting (11) and (12) in (10), the current consumption becomes

$$I_{POWER} = (N+1)I_{OUT} + N\left(2\beta C V_{DD} f + 2(\alpha C + C'W)\left(\frac{C}{C + \alpha C + C'W}\right)V_{DD} f\right) \quad (13)$$

The current consumption is also a function of the charging capacitance and the width of the MOS switches.

3.7. ANALYSIS VERIFICATION AND DESIGN STRATEGY

The proposed analysis was verified using the 0.35-μm CMOS technology. This technology does not provide a deep n-well process, so the body terminal of every NMOS device is tied together to a common substrate, which is ground. As the number of stages increases, the voltage differences between gate/drain/source and body of NMOS devices become larger than the breakdown voltage, 8-V DC between junctions. The gate, source, and drain of NMOS devices for two-stage charge pump are biased at 7 V. Three stages give that of 9.8 V, which is larger than the breakdown voltage. Thus, the number of stages can not be increased larger than two with a power supply voltage of 2.8 V. Thus, the number of stages was chosen to be two, resulting in an output voltage less than 8 V. The process parameters such as *C'* and *R'* had been determined by simulations as well as *k'* and *k''*. To validate the analysis, simulations with a wide range of different parameters have been carried out.

Shown in Figure 27 are the comparisons between the proposed analysis and

simulation results. The width of the NMOS devices was fixed to be 5 μm while the width of the PMOS devices was varied because the on-resistance of the PMOS devices is a limiting factor. In addition to the higher mobility of the NMOS devices, the threshold voltage of the NMOS devices is smaller than that of the PMOS devices since the bulk of the NMOS devices is connected to ground while the gate voltage increases. Thus, the NMOS-device on-resistance does not affect the overall on-resistance as much as that of the PMOS devices does, and the larger NMOS devices only add more parasitic capacitance. First, output voltage and current consumption of the charge pump with different charging capacitances are shown in Figure 27 (a). The power supply voltage is 2.8 V, the output current is 100 μA, the PMOS width is 10 μm, and the parasitic capacitance factors, α and β, are 0.05 and 0.15, respectively. Considering ripple of the output voltage, the frequency of the clock was set to 25 MHz.

As shown in Figure 27 (a), the output voltage falls abruptly when the charging capacitance becomes less than 6 pF, and it saturates after 10 pF. The proposed analysis successfully captured the behavior of the output voltage. To show the ability of the proposed analysis to precisely describe the output voltage behavior, the analysis without the exponential term such as (1) and the analysis in [39] is also shown. The analysis without the exponential term does not follow the simulation results after 6 pF of the charging capacitance. Figure 27 (b) shows output voltage and current consumption with different widths for the PMOS switches. The charging capacitance is 10 pF. Similarly, the proposed analysis is able to describe the dependency of the output voltage on the PMOS width. Another simulation for output voltage and current consumption was done, varying the output current. The results are shown in Figure 27 (c). The charging

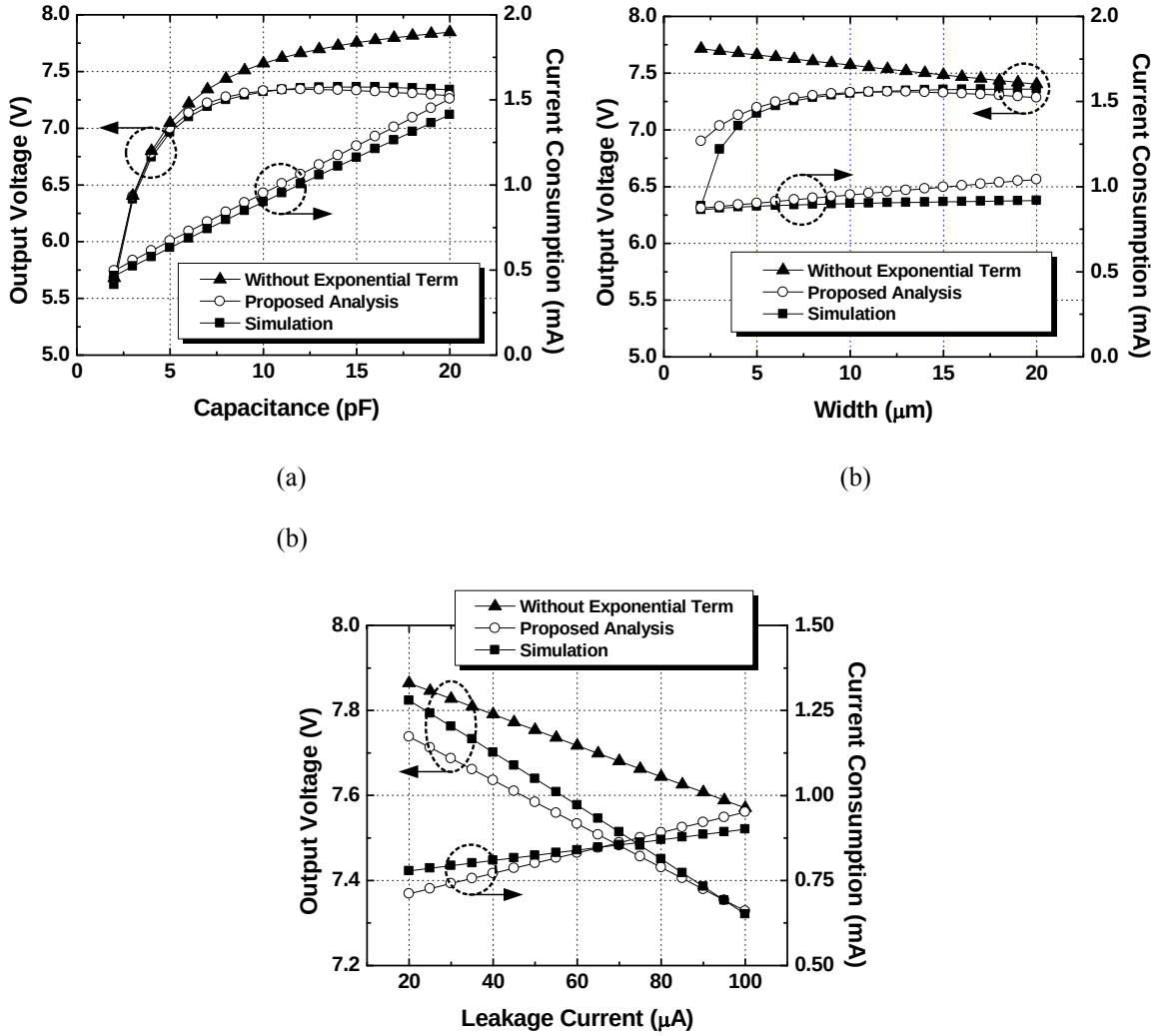


Figure 27. Comparisons of output voltage and current consumption between the analysis and simulation: (a) with different charging capacitances, (b) with different widths of PMOS switches, and (c) with different output currents.

capacitance and the width of each PMOS switch are 10 pF and 10 μm, respectively. As expected from the analysis, it was found that the output voltage is a function of both the charging capacitance and the width of the MOS switches. Both the analysis and the simulation show the same dependency on these two parameters. Compared to the analysis

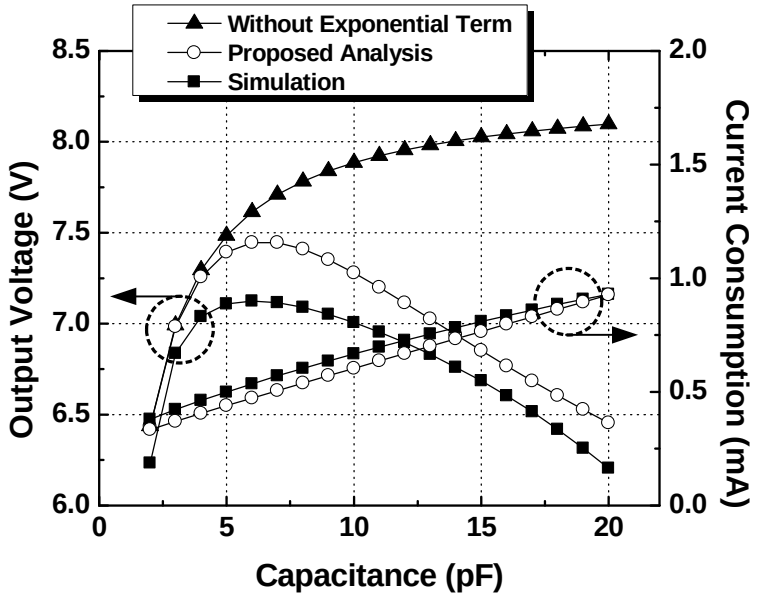


Figure 28. Comparisons of output voltage and current consumption between the analysis and simulation with different charging capacitances.

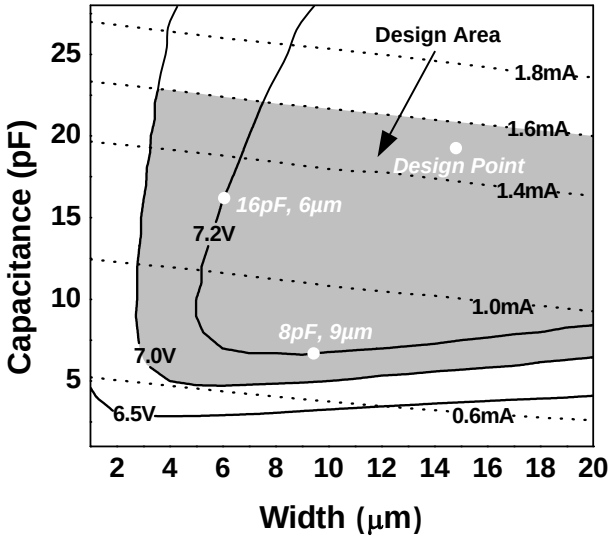
without the exponential term, the proposed analysis shows more closely matched results.

Figure 28 shows the same comparisons as Figure 27 (a) with another set of design parameters to widen the applicability of the proposed analysis. Instead of 0.35-μm MOS devices, thick-oxide MOS devices with length of 0.5 μm were used. This changes the on-resistance and the parasitic capacitance of the MOS devices. Furthermore, the size of the clock buffers was minimized to provide just enough current to drive the charge pump with the lowest output leakage current so that it can be seen the buffer size also affects the output voltage drop as expected by (9). As shown in Figure 28, the output voltage drops after 8 pF of the charging capacitance dissimilar to that shown in Figure 27 (a). There is an optimal capacitance value that gives the highest output voltage. The major difference between the results of Figure 27 (a) and Figure 28 is the size of the clock buffers. As the buffer size decreases to save current, the output voltage drops rapidly with

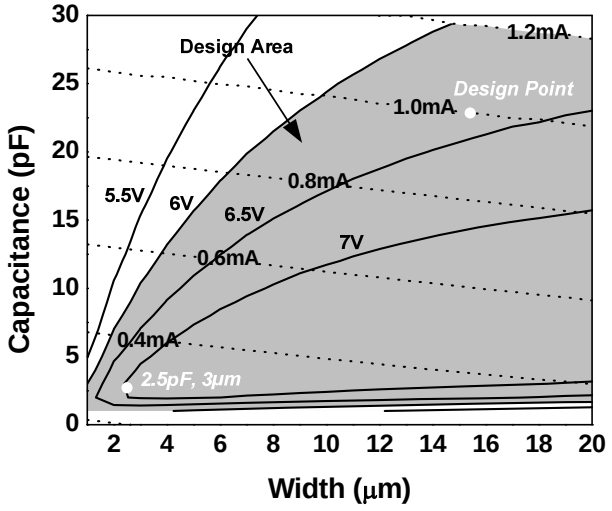
larger charging capacitances while the large enough buffer keeps the output voltage flat even with larger capacitances. Thus, it is important to size the buffer properly to keep the output voltage from dropping with larger capacitances, considering the output leakage current level to design the charge-pump based controllers.

The above analysis was applied to design a charge pump to drive the antenna switch with two different sets of design parameters detailed in Section IV. First, the target output voltage is given to be 7 V, using thin oxide MOS devices with length of 0.35 μm. Power supply voltage is 2.8 V, maximum output leakage current is 100 μA. As mentioned earlier, because the 0.35-μm CMOS technology does not support the deep n-well process, the number of stages of the charge pump was set to be two to prevent the MOS switches from breaking down. The current consumption of the charge pump is required to be less than 1.6 mA. For low ripple of the output voltage, the clock frequency was set to be 25 MHz.

In Figure 29 (a), equal-voltage and equal-current lines generated by the analysis in (8) and (12) are shown on the same plot to determine the range of the charging capacitance and the width of the PMOS switches as free design variables. The shaded area represents the design area where the output voltage is over 7 V and the current consumption is less than 1.6 mA. The charging capacitance ranges from 5 pF to 21 pF, and the width of the PMOS switches should be larger than 3 μm to meet the requirements. Since the current consumption does not strongly depend on the width of the PMOS switches but rather on the charging capacitance, it is suggested that the width of the PMOS switches be increased to lessen current consumption and area by using the smaller charging capacitance. For example, the charging capacitance should be 16 pF to generate 7.2 V



(a)



(b)

Figure 29. Design area of the charge pump for the given requirements (a) for thin oxide MOS devices and (b) for thick oxide MOS devices.

with the 6-μm PMOS switches where the charging capacitance only needs to be 8 pF with the 9-μm PMOS switches to generate the same voltage as indicated in Figure 29 (a). The current consumption and the area can be reduced by employing the latter design

strategy. In the design with the consideration of the RF antenna-switch load, however, the ripple of the output voltage is another important parameter to reduce the noise to the antenna switch. Furthermore, it was necessary to have a safe margin to guarantee the output voltage over 7 V. Thus, for fabrication, the charging capacitance was chosen to be 20 pF as shown in Figure 29 (a), where the output voltage is 7.4 V to have a margin of 0.4 V and ripple of the output voltage less than 30 mV.

The thick oxide MOS devices are used for the second set of design parameters. The length of MOS devices is 0.5 μm. The target output voltage is over 6V with power supply voltage of 2.8 V. Maximum output leakage current is 60 μA. As the first case, the number of stages is set to be two. The current consumption should be less than 1.2 mA. The design area is shown in Figure 29 (b). As shown in the first design example, the design point at the lower left corner of the equal-voltage line, e.g. 2.5 pF and 3 μm, is the optimal point at the particular output voltage in terms of the output voltage and the current consumption. However, to reduce the ripple and have a safe margin of 0.4 V, the design point with 23 pF of charging capacitance and 15 μm of MOS device width has been selected for fabrication.

3.8. MEASUREMENT RESULTS

The charge pump shown in Figure 20 was fabricated in a 0.35-μm CMOS technology, using thick oxide MOS devices. Special care was taken to prevent electromigration effects from occurring in the layout since the tens of mega-hertz clock frequency may generate a relatively heavy current level during the charging and discharing period. A die photo of the fabricated antenna switch controller is shown in

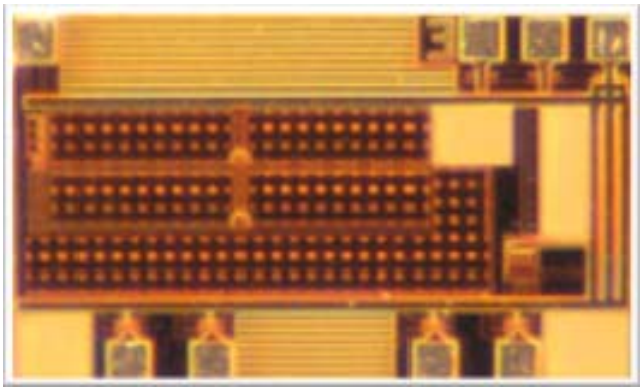
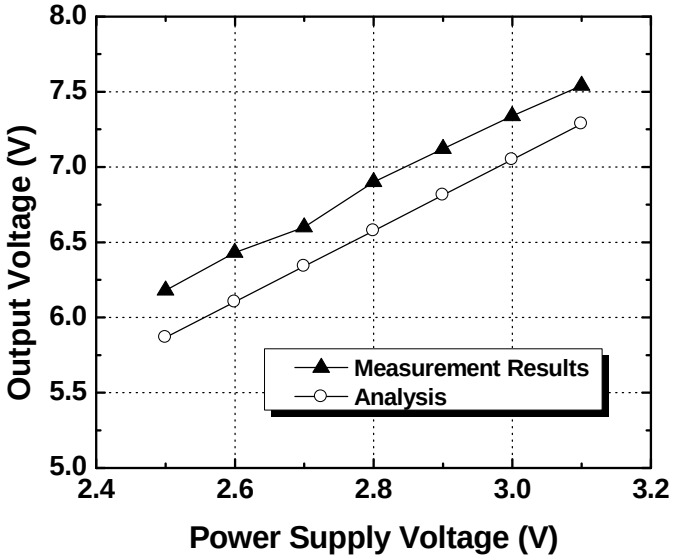


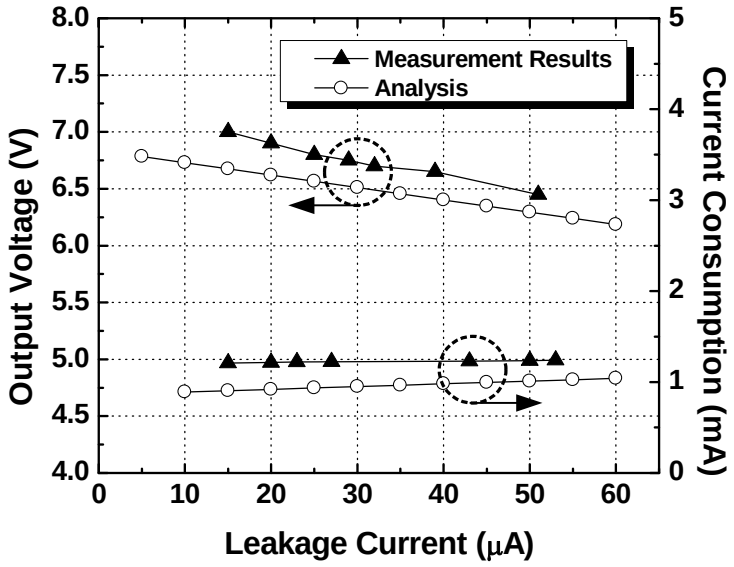
Figure 30. Die photo of the fabricated antenna switch controller.

Figure 30. The dimension of the switch controller is 1.16 mm by 0.68 mm. As mentioned in Section IV, the number of stages of the charge pump was chosen to be two. The charging capacitance is chosen to be 23 pF to reduce the ripple at the output, and the width of the MOS switches is 15 μm. Shown in Figure 31 are comparisons of the output voltage and the current consumption of analysis and measurements with different power supply voltages and output currents. The output current for Figure 31 (a) is 26 μA. The measurement results of the output voltage have a good agreement with the analysis. The ripple of the output voltage was measured to be less than 40 mV. The measured current consumption also follows the analysis. The parasitic capacitance ratio for the top-layer connections of the charging capacitor has been overly emphasized, resulting in lower voltage for the analysis than the measurements. This can be acceptable for the design to have an extra safe margin.

The performances of the antenna switch were also measured with the designed charge pump controlling the antenna switch. As mentioned earlier, the output power and



(a)



(b)

Figure 31. Comparison of the output voltage (a) with different power supply voltages and (b) with different output currents between the analysis and measurements.

the linearity requirements for the antenna switch are stringent, and the charge pump should sustain the high output voltage while providing the leakage current to the antenna

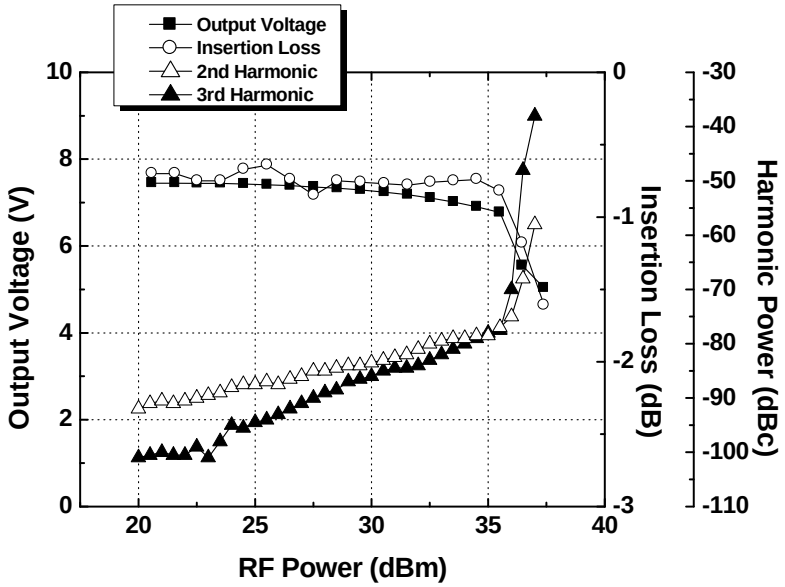


Figure 32. RF antenna-switch performance measurements: insertion loss and harmonic powers of the antenna switch with charge-pump output voltage.

switch. Shown in Figure 32 are the insertion loss and the harmonic powers of the antenna switch. The insertion loss is less than 1 dB where the RF antenna-switch controller generates the output voltage over 6.5 V with power supply voltage of 3 V. The insertion loss increases as the output voltage decreases. The linearity measure of the antenna switch is shown by looking at harmonic powers. The antenna switch that supports the various wireless standards such as GSM, PCS/DCS, and UMTS bands should support output power up to 35 dBm with less than -68 dBc of harmonics. The designed RF antenna-switch controller maintain the output voltage over 6V so that the antenna switch can output 35 dBm of power with -70 dBc of the second and the third harmonics. The designed RF antenna-switch controller was able to generate high enough voltage to drive the antenna switch while withstanding the output leakage current.

3.9. CONCLUSION

In this chapter, the analysis and the design techniques of charge-pump-based RF antenna-switch controllers have been presented. The described approach takes into consideration the effects of the loading conditions for the charge pump, which vary with the RF input power to the RF antenna switches. Furthermore, the proposed analysis newly shows that the output voltage of the charge pump depends on both the charging capacitance and the width of the MOS switches. The analysis and design techniques of the charge pump were verified with the 0.35-μm CMOS technology. The measurement results show that the analysis matches well with the measurement results and the designed controller can successfully drive the RF antenna switches while meeting the output power and the linearity requirements.

CHAPTER 4

EFFICIENCY ENHANCEMENT OF ANTENNA-SWITCH CONTROLLER

Due to the increased demand for mobile devices, power consumption has been a major concern in designing integrated circuits, especially for controller circuits to drive antenna switches, liquid crystal displays (LCDs), and memories because these components are integrated in one mobile device to satisfy the customers' demand on functionalities. The integration of these various functional blocks, mostly digital blocks, led to the ever-shrinking feature size of a complementary metal oxide semiconductor (CMOS) technology, and the scaling-down resulted in a lower power supply voltage. However, many controller circuits still need a higher voltage than a given power supply voltage [16, 20, 40-42]. To generate the high voltage, charge pumps have been commonly used [43-45] because they are small in size and consumes relatively small amount of power. However, the charge pump is still the dominant power consumer in the controller circuits.

Figure 33 shows an antenna-switch controller block diagram that utilizes the charge pump as a tool to generate the high voltage to drive antenna switches. It consists of the charge pump, level shifters, and a decoder. The high voltage generated by the charge pump is fed to the antenna switches by the level shifters, and the decoder is used to determine which antenna switch should be turned on according to input signals. Among these components, the most power-hungry block is the charge pump as previously

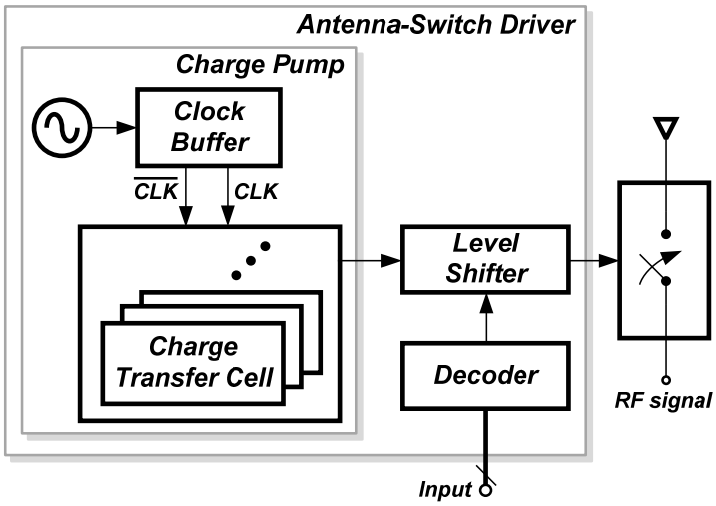


Figure 33. Antenna-switch controller block diagram including an antenna switch.

mentioned.

Many techniques have been introduced to reduce the power consumption of the charge pump. Some of the techniques focused on the efficiency of charge pumping mechanism [25, 43-45]. Other techniques introduced new clocking schemes such as a four-phase clocking scheme, which uses four different phases of a clock signal instead of two out-of-phase clock signals, to improve the efficiency of the charge pump [46-47]. However, these techniques aimed to improve the efficiency of the charge transfer cells with already-given clock signals. The efficiency of the clock generation blocks has been overlooked. The power consumed to generate the clock signals is significant and is the critical factor to design the charge pump, and it becomes more critical when the charge transfer cells utilize large capacitors or the number of charge transfer cells is increased to make higher output voltage.

In this chapter, a technique to reduce the power consumption of the antenna-switch

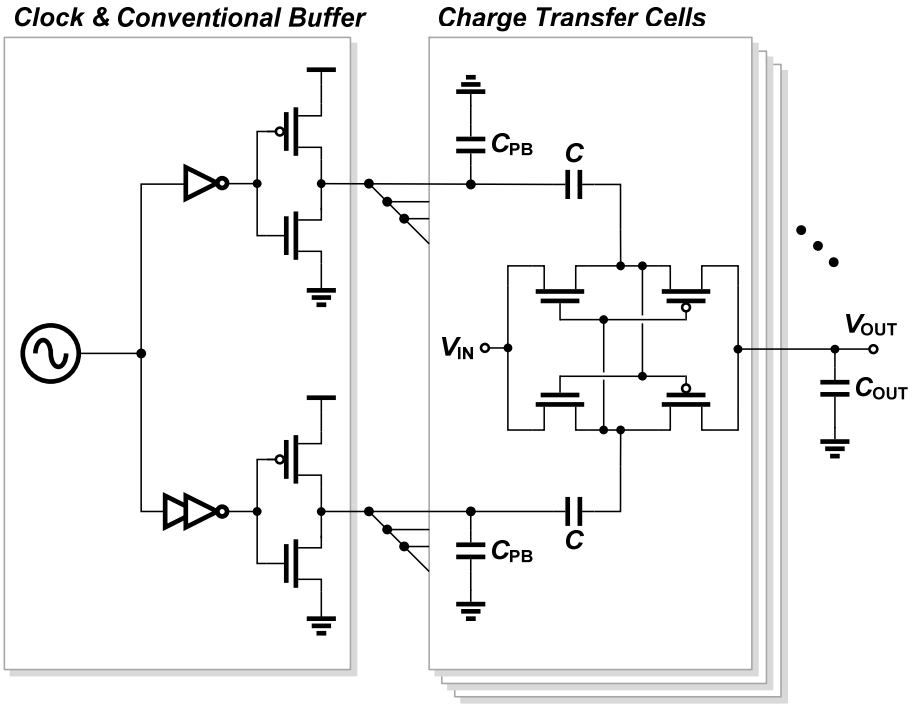


Figure 34. Conventional charge pump circuit with multiple charge transfer cells in series.

controller by recycling shared charges in the clock buffer of the charge pump is presented. The proposed technique stores the charges in parasitic capacitances without the charges being discharged, and the charges are re-used to charge other capacitors. In addition, the analysis of the relationship between the charge-recycling time and the amount of the current reduction is provided. The explanation of the detailed circuit operation and the analysis is given in Chapter 4.1 and 4.2, and the measurement results and comparisons with conventional charge pumps which use an inverter-type clock buffer are presented in Chapter 4.3.

4.1. SHARED-CHARGE RECYCLING CHARGE PUMP

4.1.1. Conventional charge pump

A conventional charge pump to generate a higher voltage than a power supply voltage using two out-of-phase clock signals is shown in Figure 34 [16, 23]. An oscillator generates a clock signal, and clock buffers make two out-of-phase signals. The clock buffers also drive charging capacitors denoted by C in Figure 34 by charging and discharging parasitic capacitances, C_{PB}. In a standard CMOS technology, the parasitic capacitances are created by the parasitic of transistors and charging capacitors, C. Since C_{PB} is the parasitic capacitance on the bottom plate of C, the capacitance of C_{PB} can be significantly large in a bulk CMOS technology.

With the clock signals generated by the clock buffers, the charge transfer cells pump charges into the output, V_{OUT}, creating a higher voltage than the power supply voltage or a negative voltage, depending on how they are configured. To maximize a voltage gain of each charge transfer cell, the charging capacitors need to be enlarged until the gain saturates or drops as described in [16], but this increased charging capacitances result in larger parasitic capacitances. Moreover, as the number of the charge transfer cells is increased to generate a higher voltage level in magnitude, the parasitic capacitances to be charged and discharged at every clock cycle are multiplied by the number of stages. The clock buffers should be able to charge these large parasitic capacitances at each clock cycle, and it requires a great amount of current. Unfortunately, the large amount of current which once used to charge the parasitic capacitances is usually dumped to ground to discharge the parasitic capacitances and wasted. The amount of current wasted by discharging the parasitic capacitances is given by

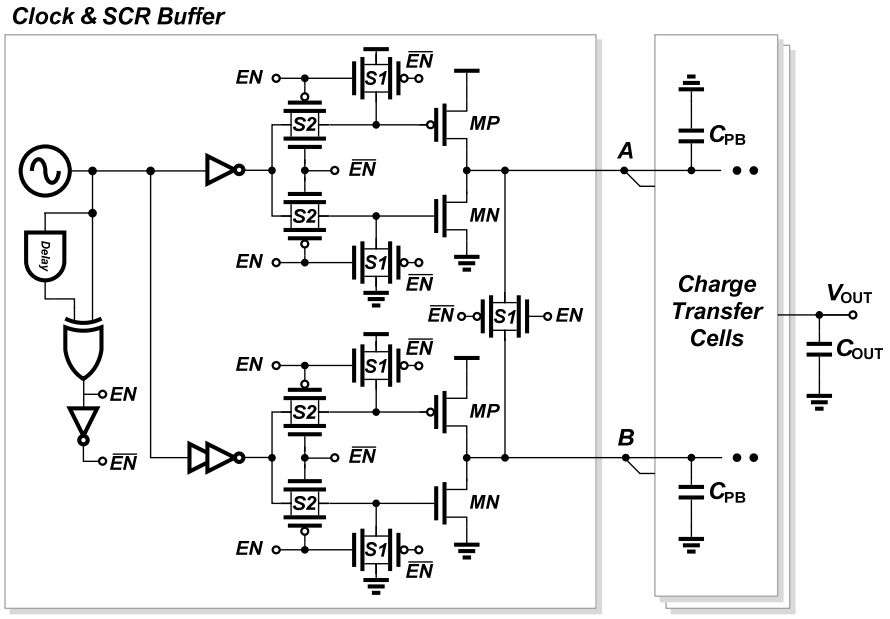


Figure 35. Proposed shared-charge recycling charge pump circuit with two charge transfer cells in series.

$$I_{waste,conv} = n \times f C_{PB} V_{DD}, \tag{14}$$

where n is the number of the charge transfer cells, f is the clock frequency, and V_{DD} is the power supply voltage. The amount of the wasted current depends on the voltage swing of the clock buffer output, which is V_{DD} in this case. Thus, it is obvious that the voltage swing of the clock buffer output should be decreased to save the current wasted in the charge pump.

4.1.2. Shared-charge recycling charge pump

Charge sharing or charge recycling concept is popular in memory applications where repeating clock signals should drive large capacitances [48-49]. The charges used to drive

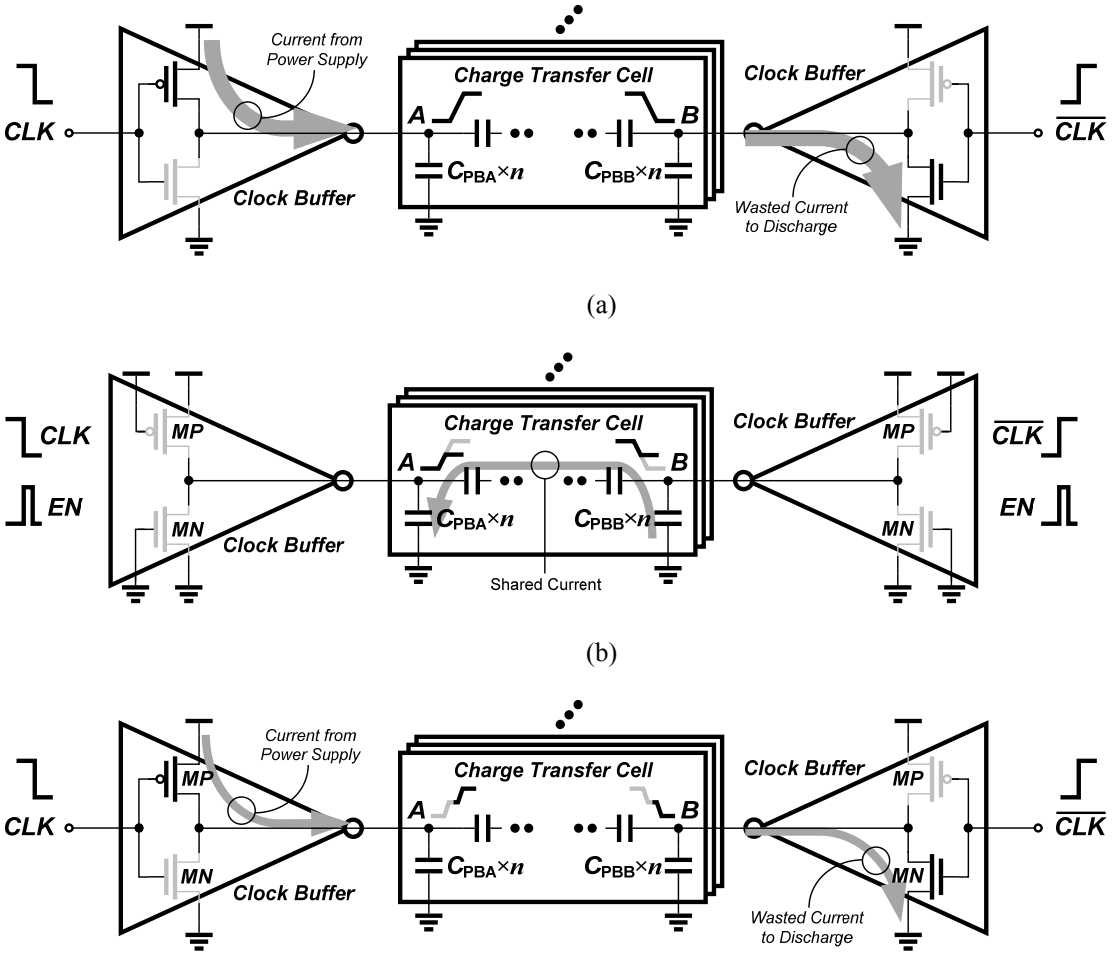


Figure 36. Conceptual description of the proposed shared-charge recycling charge pump.

a load are stored in a dummy capacitor before they are discarded to ground. Then, the charges stored in the dummy capacitor are injected to drive the load.

The circuit diagram of the proposed shared-charge recycling charge pump, based on the charge recycling concept, is shown in Figure 35. The charge-recycling enable signal, denoted by *EN* in the figure, triggers the switches, *S1*s, *S2*s, and *S3*, to isolate the buffer outputs, *A* and *B*, from the clock signals. The transistors, *MP*s and *MN*s, should be turned

off at the same time to avoid any current leakage through these transistors. The buffer outputs, then, are connected together to share the charges and the voltages of two buffer outputs become equal. The enable signal is generated at beginning of each clock edge, and the duration of the enable signal is controlled by the delay amount of the delay block shown in Figure 35. The duration of the enable signal should be sufficiently long for the buffer outputs to share the charges and to settle at half of V_{DD}. However, the duration should also be short enough not to affect the normal charge pump operation. After the charge recycling is finished, two buffer outputs are disconnected from each other, and the buffers become simple inverters as the conventional ones shown in Figure 34.

Figure 36 shows the conceptual description on how the proposed shared-charge recycling charge pump saves power. As mentioned in the previous Section, the conventional charge pumps charge the parasitic capacitances using only the current from the power supply and discharge it by dumping the charges to ground as shown in Figure 36 (a). The parasitic capacitances, C_{PB}, are multiplied by the number of the charge transfer cells denoted by n in the figure. All the charges that were used to charge $n \times C_{PB}$ are dumped to ground and wasted.

In the shared-charge recycling charge pump, on the other hand, there exists an intermediate voltage level before the clock buffer outputs, A and B, reaches V_{DD} or ground as shown in Figure 36 (b). The parasitic capacitances, $n \times C_{PB}$, are charged to half of V_{DD} by recycling the charges stored in other parasitic capacitances, which is wasted in the conventional clock buffers. Then, the current from the power supply fully charges one set of the parasitic capacitances, $n \times C_{PBA}$, raising the buffer output A to V_{DD}. The other set of the parasitic capacitances, $n \times C_{PBB}$, are discharged, and the buffer output becomes

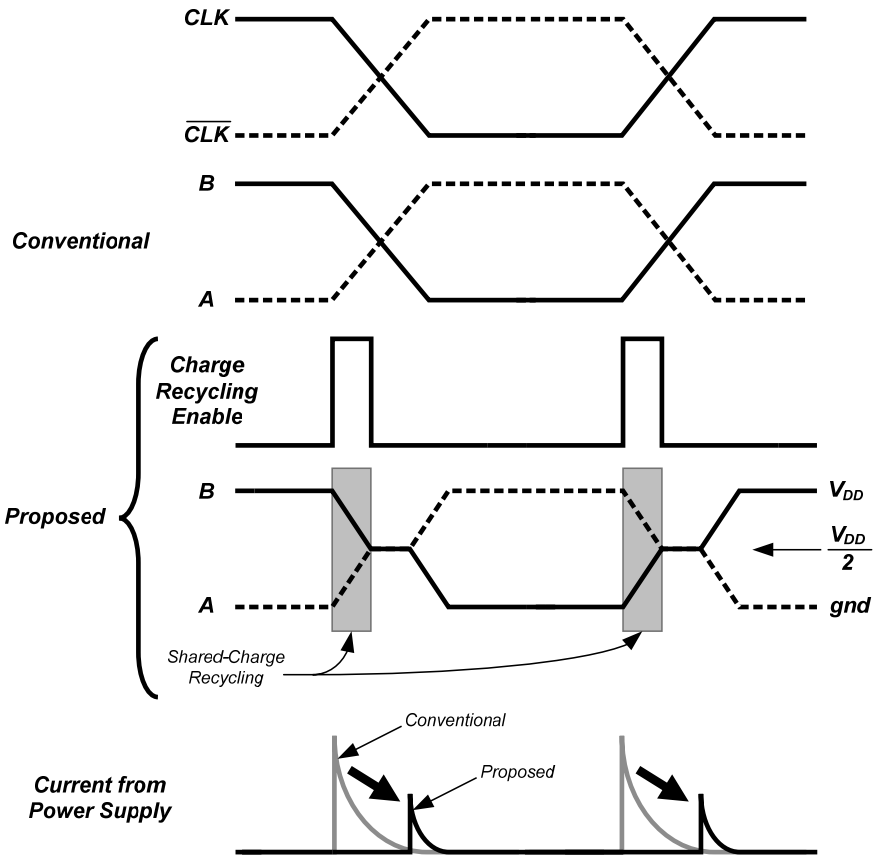


Figure 37. Voltage and current waveforms of the conventional charge pump and the proposed charge pump.

ground as illustrated in Figure 36 (c). The voltage swing of the buffer outputs charged by the current form the power supply is now cut in half, and the amount of current wasted by discharging the parasitic capacitances for the shared-charge recycling charge pump becomes

$$I_{waste,SCR} = n \times \frac{1}{2} f C_{PB} V_{DD}, \tag{15}$$

since C_{PBA} and C_{PBB} are the same and they are equal to C_{PB}. Compared to the conventional charge pump, the proposed shared-charge recycling charge pump can reduce the current consumption by 50 %, theoretically. However, in reality, there are

other factors to be included in the current calculation such as the current consumed by the control circuits and the charge-recycling time. These factors dilute the advantages of the shared-charge recycling charge pump in saving current. These diminishing effects of the shared-charge recycling charge pump is discussed in great detail in the following section.

The illustrations of the voltage and current waveforms of the shared-charge recycling charge pump are shown in Figure 37. When CLK edges occur, the buffer outputs of the conventional charge pump goes to V_{DD} or to ground at once by drawing the current from the power supply or by dumping the stored charges to ground. However, the shared-charge recycling charge pump recycles the shared charges to pre-charge the parasitic capacitances to half of V_{DD} as indicated by the shaded gray box in the figure. By this charge recycling, the level of current peaks is reduced additionally, and the duration of the current peaks is decreased as well. Then, the total area of the current becomes significantly smaller than that of the conventional charge pump as shown in the figure.

4.2. DIMINISHING EFFECTS OF SHARED-CHARGE RECYCLING

The shared-charge recycling charge pump can theoretically save 50 % of current over the conventional charge pump. However, there are diminishing effects that reduce the amount of improvement achieved by the shared-charge recycling technique. For example, the control signal that triggers switches, *S1*s, *S2*s, and *S3* in Figure 35, consumes extra dynamic power in addition to the power consumption of the conventional charge pump. Furthermore, the amount of the time delay that determines the duration of the charge recycling can be too short for the parasitic capacitances to fully share the charges and settle the voltage at half of V_{DD}. The time delay may be too long so that the

output voltage of the charge pump can be lowered due to slow RC network [16]. These effects also diminish the amount of improvement because more power should be consumed to increase the output voltage.

The amount of the current saving by the shared-charge recycling charge pump can be computed by subtracting (15) from (14) and taking the diminishing effects into account, and it can be shown as

$$I_{saving} = n \times \frac{1}{2} f C_{PB} V_{DD} - I_{dim}. \quad (16)$$

Firstly, the shared-charge recycling charge pump has additional control circuits as shown in Figure 35. The additional blocks include nine switches, one delay block, and two logic gates. At each clock cycle, these additional blocks should be driven by the current from the power supply. This current consumption diminishes the advantages of the shared-charge recycling charge pump. This quantity can be expressed as

$$I_{control} = f\left(C_{SW} + C_{logic}\right) V_{DD}, \quad (17)$$

where C_{SW} represents the total capacitance of the switches and C_{logic} is the total capacitance of the logic gates.

Secondly, the amount of the delay plays an important role to determine the amount of the current saving. As mentioned earlier, when the charge recycling time is too short, the voltage level of the clock buffer output after the charge recycling can not be as high as half of V_{DD}. Then, the voltage difference that should be charged by the current from the power supply increases. If the charge recycling time is close to zero, the shared-charge recycling charge pump becomes the same as the conventional charge pump with the extra current consumption by the control circuits, resulting in a poorer efficiency than

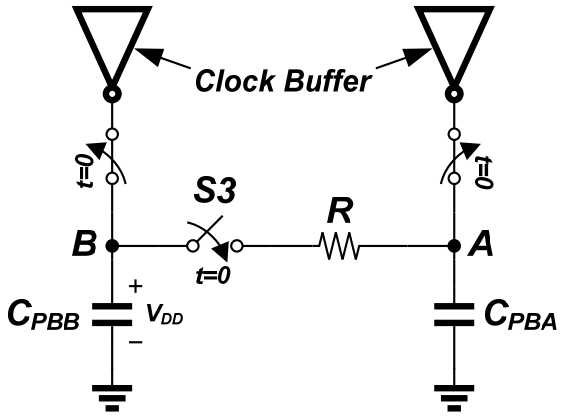


Figure 38. Circuit to describe the shared-charge recycling.

the conventional charge pump. Thus, the charge recycling time should long enough to complete the charge recycling process optimally.

The charge recycling can be described as the circuit shown in Figure 38. It can be assumed that the parasitic capacitance, C_{PBB}, holds the voltage difference of V_{DD} initially. When a new clock edge occurs (t=0), the clock buffers are disconnected from node A and B, and the shared-charge recycling begins. As the *S3* switch closes, the voltage difference between the node A and B forces current flow toward C_{PBA}, and the voltages at the node A and B changes during this time. The voltage at the node A can be expressed as

$$V_A(t) = \frac{V_{DD}}{2}(1 - e^{-\frac{2t}{RC}}), \tag{18}$$

where t is the time passed after the charge recycling begins, R is the on-resistance of the *S3* switch, and C is the parasitic capacitances, C_{PB}. As expected, the time should be long enough for the voltage at the node A to reach half of V_{DD}. For example, the time should be longer than the RC time constant for the voltage at the node A to be 90 % of half of

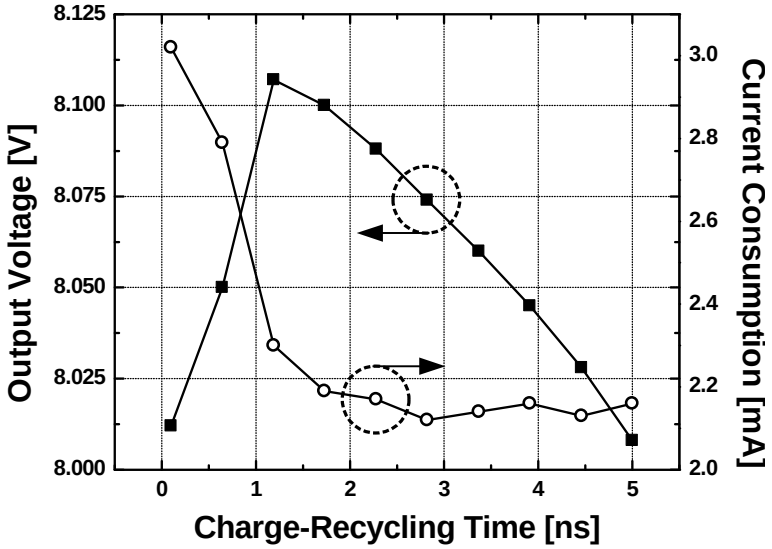


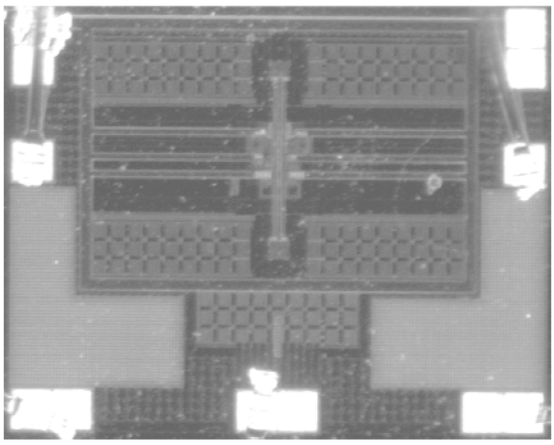
Figure 39. Simulated output voltage and current consumption of the charge pump with different charge-recycling time.

V_{DD}. If the time can not be made long, the on-resistance of *S3* should be minimized to reduce the RC time constant by increasing the width of the transistors of *S3*. However, this, in turn, increases the parasitic capacitances of node *A* and *B*, which results in increased current consumption. The trade-off between these parameters should be carefully considered to design a low-power controller.

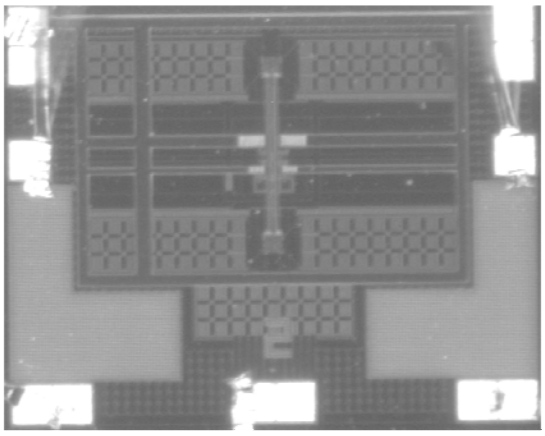
With the diminishing effects described above, the amount of the current saving now can be approximated by

$$I_{saving} = n \times \frac{1}{2} f C_{PB} V_{DD} \left(1 - e^{-2t/RC}\right) - f\left(C_{SW} + C_{logic}\right) V_{DD}. \quad (19)$$

This equation implies that the charge-recycling time should be long while the parasitic resistance and the parasitic capacitances are minimal. Also, it implies that the control circuits should be simple so that the parasitic capacitance associated with the control circuits can be minimized to save more current.



(a)



(b)

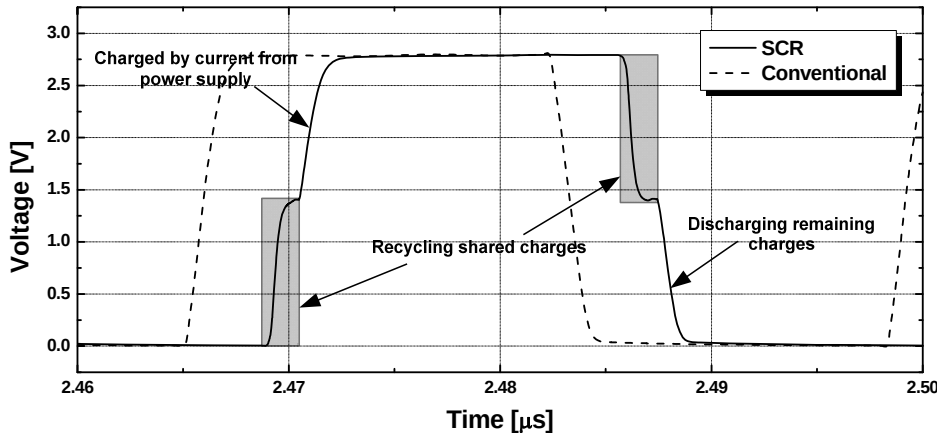
Figure 40. Die photographs of the fabricated chips (a) with the shared-charge recycling charge pump and (b) with the conventional charge pump.

Having discussed that the charge-recycling time should be long enough to complete the recycling process, it is important to note that the time should not be longer than necessary. If the charge-recycling time becomes too long, the slow RC network decreases the charge pump output [16]. Figure 39 shows the simulated results for the output voltage and the current consumption of the charge pump with different charge-recycling times. The period of the clock is 32 ns. As expected, the current consumption decreases as the

charge-recycling time is increased. When the recycling time increases from 0.1 ns to 1.8 ns, the reduction of the current consumption is about 0.8 mA. Beyond this point, the current consumption is not greatly improved. Only 0.1 mA of current is reduced when the recycling time is increased from 1.8 ns to 5 ns. This was expected by (5) because the time required for V_A to be 90 % of half of V_{DD} is one time constant, RC. Longer charge-recycling time than the RC time constant can be considered to be excessive. The output voltage of the charge pump is also as anticipated. As the recycling time is increased, the burden for the clock buffer to drive the parasitic capacitances is lessened. So, the same driving capability of the clock buffers makes the RC network, described in [16], faster, resulting in higher output voltage. However, once the recycling time goes beyond the necessary time, 1.2 ns in this case, the output voltage drops because the RC network becomes slower as previously described.

4.3. MEASUREMENT RESULTS

To evaluate the performance improvement of the antenna-switch driver utilizing the shared-charge recycling charge pump, two drivers, one with the shared-charge recycling charge pump and the other with the conventional charge pump, were fabricated by using a standard 0.35-μm CMOS technology. The die photographs of the fabricated chips are shown in Figure 40. The oscillator is implemented by using a simple inverter chain. The number of the charge transfer cells is two to ensure that the voltage across any junction of transistors is within $2V_{DD}$. This constraint can be removed when a triple-well process is available since the body of the charge transfer cells can be controlled independently from the substrate voltage, which is typically ground. The node A and B in Figure 35 are



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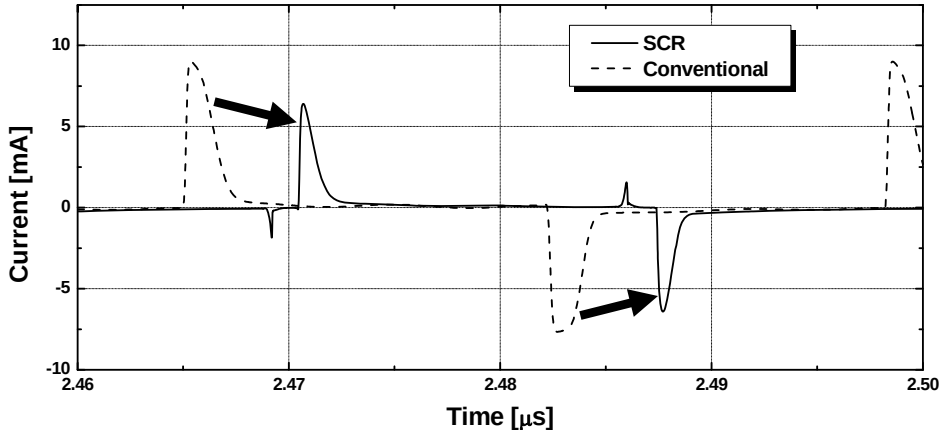


(b)

Figure 41. Simulated (a) voltage waveforms of the proposed shared-charge recycling clock buffer and the conventional clock buffer and (b) waveforms of the current drawn from the power supply.

exposed to the outside of the chip via pads to assess the effect of the increased parasitic capacitances. The charging capacitance, C, and the output capacitance, C_{OUT}, are 21 pF. The clock frequency was set to be around 30 MHz, considering the amount of the delay. The delay was implemented by inverters with a small width and a large length. Because the delay was implemented using inverters, the clock frequency should be mega-hertz range because the inverters can not generate a large delay unless inductors are used,

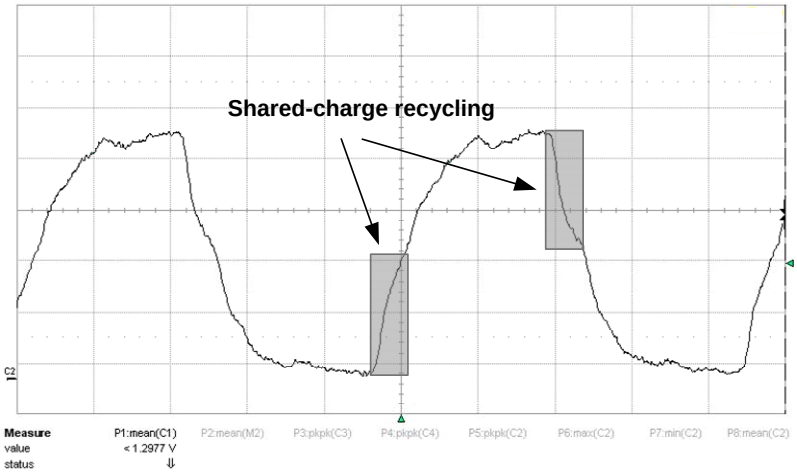


Figure 42. Measured voltage waveform of the clock buffer output of the shared-charge recycling charge pump.

which increases a chip area greatly.

Simulated voltage and current waveforms of the shared-charge recycling Charge pump and the conventional charge pump are shown in Figure 41. The charge-recycling time was chosen to be 1.2 ns. As shown in Figure 39, the output voltage of the charge pump is maximized at 1.2 ns while the current consumption is significantly reduced. As shown in Figure 41 (a), the output voltage of the shared-charge recycling charge pump has the intermediate level at half of V_{DD} before the output reaches V_{DD}. This voltage level is obtained by recycling the shared charges as described in the previous section. The conventional clock buffer output shows no intermediate level. All the charges to charge the parasitic capacitance come from the power supply. The current saving achieved by the shared-charge recycling technique can be seen in Figure 41 (b). The solid line represents the current drawn from the power supply for the shared-charge recycling charge pump while the dotted line shows the same current for the conventional charge

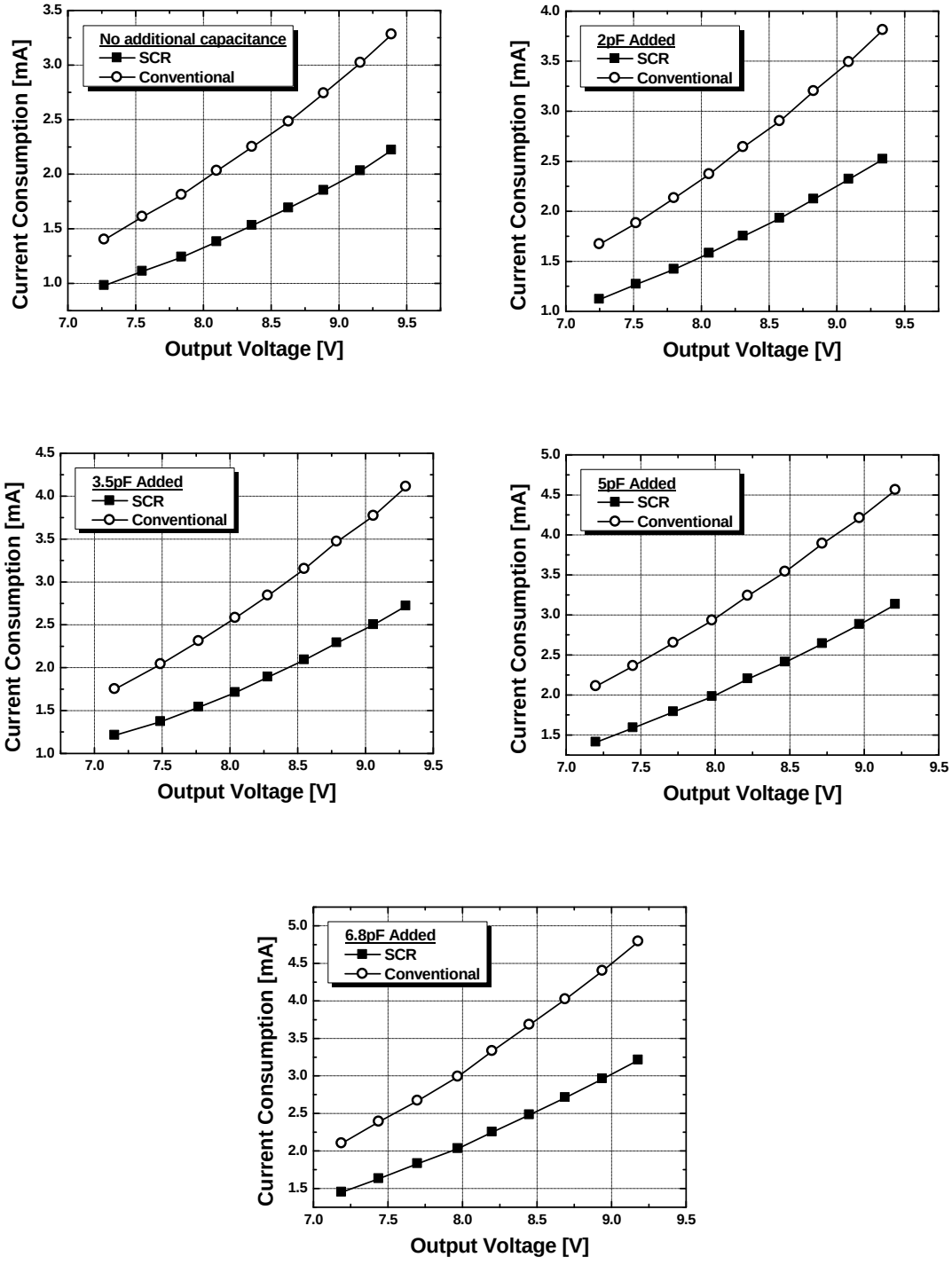
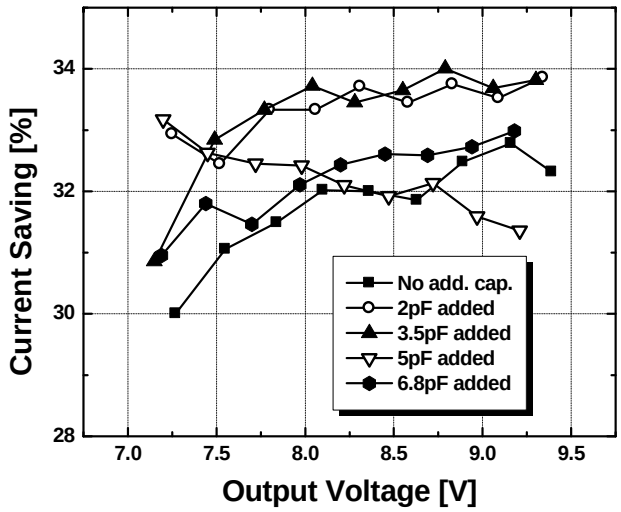


Figure 43. Measured current consumption comparisons with different output voltages and parasitic capacitances.

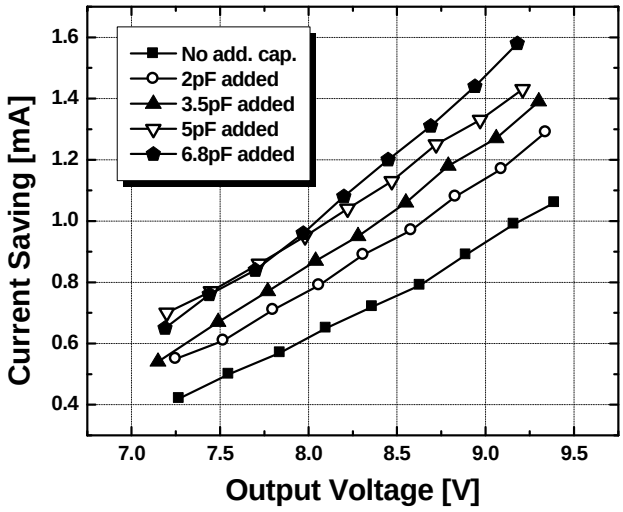
pump. The peak current level of the shared-charge recycling charge pump is lower than that of the conventional one, and the duration of the current peak is shortened as well by using the shared-charge recycling charge pump. Since the area under the current waveform represents the current consumption, the shared-charge recycling charge pump greatly reduces the overall current consumption for the switch driver. In addition, the reduced current peak level helps ease the burden of the power supply if the power supply voltage is provided by a regulator such as a low dropout regulator (LDO) as it is the case in most of commercial applications. The measured voltage waveform of the shared-charge recycling charge pump is shown in Figure 42. The intermediate voltage level at half of V_{DD} can be seen in the figure. The additional 11-pF of capacitance was added to the clock buffer outputs by oscilloscope probes.

The reduction of the current consumption by using the shared-charge recycling charge pump with different output voltages and parasitic capacitances is shown in Figure 43. The output voltage of the charge pump was set to be the same for both of the charge pumps while the current consumption was measured for fair comparisons. The additional capacitances were added at the node *A* and node *B* in Figure 35 to mimic the effects of the increased parasitic capacitances. The output voltage variation was obtained by changing V_{DD}. As shown in the figure, the shared-charge recycling charge pump consumes less current while generating the same output voltage for different parasitic capacitances and output voltages. The amount of the current saving tends to increase as the output voltage goes up. Figure 44 summarizes the current saving. The shared-charge recycling charge pump saves more current as the output voltage is raised and the parasitic capacitance is increased as shown in Figure 44 (a). Overall current saving ranges from 30

to 34 % as shown in Figure 44 (b). The diminishing effects of the shared-charge recycling charge pump decreased the amount of the current saving, which is 50 %, ideally.



(a)



(b)

Figure 44. Measured current saving of the shared-charge recycling charge pump over the conventional charge pump (a) in absolute amount of current and (b) in percentage.

4.4. CONCLUSION

In this chapter, a low-power antenna-switch driver utilizing the shared-charge recycling charge pump was proposed to reduce the current consumption of the driver. The shared-charge recycling charge pump recycles the charges stored in a capacitor, which are discharged to ground and wasted, to charge other capacitors. In this way, the shared-charge recycling charge pump theoretically saves 50 % of current, compared to the conventional charge pump. Also, the relationship between the charge-recycling time and the current saving has been analyzed, and it was used to determine the charge-recycling time. The measurements show that the current consumption is reduced from 4.79 to 3.21 mA to generate the charge pump output voltage of 9.18 V with V_{DD} of 3.3 V. This translates to be 32 % of current saving. The average current saving to generate the charge pump output voltage ranging from 7 to 9 V is over 32 %. These results show that the proposed antenna-switch driver can be a good candidate for low-power mobile applications.

CHAPTER 5

INTEGRATED SOI ANTENNA SWITCH

Recent demand for multi-standard operation of wireless devices has accelerated the integration of multiple wireless standards such as GSM, EDGE, and WCDMA in a single device. Since each standard requires its own power amplifier and LNA and they share one front-end including an antenna, there is a need for a component to control transmission and reception of a signal. Therefore, an antenna switch became one of the key building blocks in the current RF front-end circuits [16].

As more standards are integrated in a device, the complexity of the antenna switch and its control scheme increases, and the requirements of the antenna switch become more stringent. To meet the stringent requirements, gallium arsenide (GaAs) p-HEMT [50] or silicon-on-sapphire (SOS) [51] has prevailed in implementing the antenna switch. However, in recent years, a relatively low-cost silicon-on-insulator (SOI) CMOS

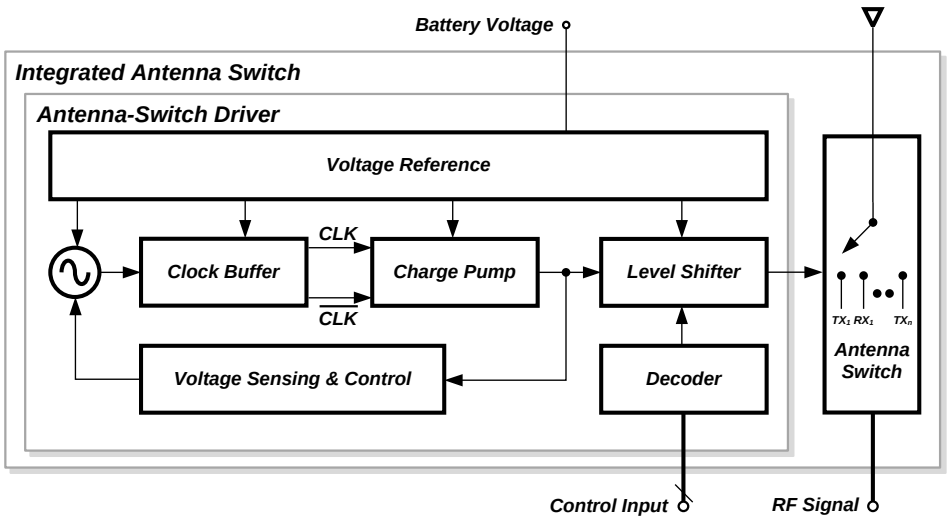


Figure 45. The integrated antenna switch block diagram.

technology has shown its ability to support high-power signals over 30 dBm [52-53].

Even though the technologies have been improved to support high-power signals, its control scheme has rarely been studied in detail. The importance of the efficient control scheme has been increased as multiple-throw antenna switches are developed to cover multiple wireless standards.

In this chapter, an efficient antenna-switch driver integrated with a multi-stacked-FET antenna switch as shown in Figure 45 is presented. The antenna-switch driver greatly reduces power consumption of the clock and the clock buffer, which are the dominant power consumer in the driver, by changing a clock frequency. The entire integrated antenna switch is also discussed in this chapter.

5.1. SILICON-ON-INSULATOR TECHNOLOGY

One of the critical challenges to implement the fully-integrated front-end in the CMOS technology is the conductive substrate. As the frequency of operation increases, reaching radio frequencies, the coupling loss through the conductive substrate became one of the main factors to degrade performance. Especially, the output network of the PA is very sensitive to a Q factor of the passives used in the network since it deals with watt-level of power. In Table 2, the comparison of some RF IC technologies is given [8]. The frequency performances of the CMOS technology including f_T and f_{MAX} are comparable to the other technologies. However, the substrate resistivity is much less, resulting in lower Q factor, compared to the GaAs counterparts. The breakdown voltage is also an issue of the CMOS technology.

Table 2. Comparison of some RF IC technologies.

Standard	CMOS	SiGe BiCMOS	GaAs MESFET	InGaAs HBT
Feature Size (μm)	0.25	0.25	0.5	3
f_T (GHz)	40	75	40	60
f_{MAX} (GHz)	45	75	40	60
Breakdown (V)	2.5	2.5	20	20
Substrate Resistivity (Ω-cm)	1	18	> 10000	> 10000
Inductor Q	4	15	25	25

The inferiority of the CMOS technology has motivated the preference of the GaAs solution for the PA and the antenna switch over the CMOS one. However, recent advance of the CMOS technology on an insulating material, so called silicon-on-insulator (SOI), has been remarkable, and the performance of the SOI technology is comparable to the GaAs technology. Recently, the SOI technology showed the high resistive substrate with the resistivity of greater than 750 Ω-cm [54]. From this point, the CMOS technology will be referred as bulk CMOS technology to distinguish it from the SOI technology. The thickness of the metallization for passives is also one of the important properties required for the high Q factor. Since the resistivity of the metal is inversely proportional to the thickness of the metal, the metal should be thick to increase the Q factor. The SOI technology mentioned above offers a thick top metal, the thickness of which is 4 μm. The Figure 46 shows the cross-sectional view of the SOI technology. Unlike the bulk CMOS

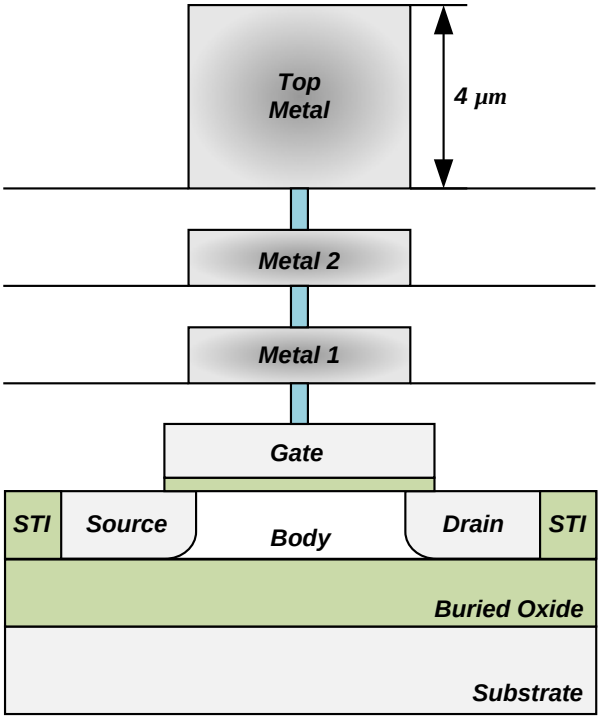


Figure 46. Cross-sectional view of the SOI technology.

technology, there exists a buried oxide layer beneath the source and the drain region, separating the body of the transistor from the substrate. The thickness of the buried oxide is in the order of micron, so the distance between the top metal and the substrate is increased to reduce the coupling. In this technology, every transistor can be separated from the other by the shallow trench isolation (STI) as shown in Figure 46. The body of the transistor is now isolated and can be biased at any voltage. So, without the triple-well process in the bulk CMOS technology, which consumes a large area, the body of the SOI transistor can be controlled freely.

5.1. EFFICIENT SOI ANTENNA SWITCH CONTROLLER

5.1.1. Negative voltage generation

Insertion loss and linearity are major requirements for the antenna switch. Using a stack of multiple FETs as shown in Figure 47 to reduce voltage stress on each FET and improve the linearity increases parasitic capacitance and on-resistance of the antenna switch. In turn, this large parasitic components increase the insertion loss. To reduce the number of stacked FETs while maintaining the linearity, a negative voltage instead of 0 V at the control terminal of the FETs becomes essential to turn the FETs off.

The necessary negative voltage is generated by using the charge pump in [16]. The same structure to generate the higher voltage than the power-supply voltage was used with NMOS and PMOS switching their positions. Now, the charges are drawn out from the output capacitor, generating the negative voltage. The circuit diagram is shown in Figure 48. The simulation result was included in Figure 49 to show the successful generation of the negative voltage. The body-contact type of transistors in the SOI CMOS technology was used, instead of floating-body type to eliminate ambiguity in the body voltage of the transistors so that the parasitic junction diodes are kept reversely biased and the threshold voltage remains the same. The body of the NMOS is connected to the output, and that of the PMOS is at the ground.

Shown in Figure 50 is the shift of the voltage swing across each OFF-state FET. Without the negative voltage, the large voltage swing goes over the threshold voltage, turning on the OFF-state FET. This, in turn, results in the distorted waveform at the antenna port. To avoid this unwanted turning-on of the OFF-state FET, the negative voltage can be used to shift the voltage swing downward as shown in Figure 50, so that

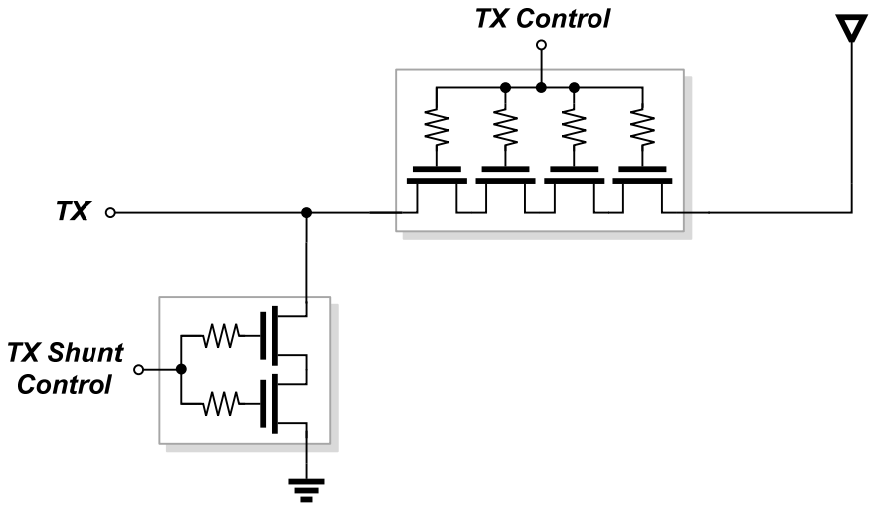


Figure 47. Multiple FETs stacked to reduce voltage stress on each FET.

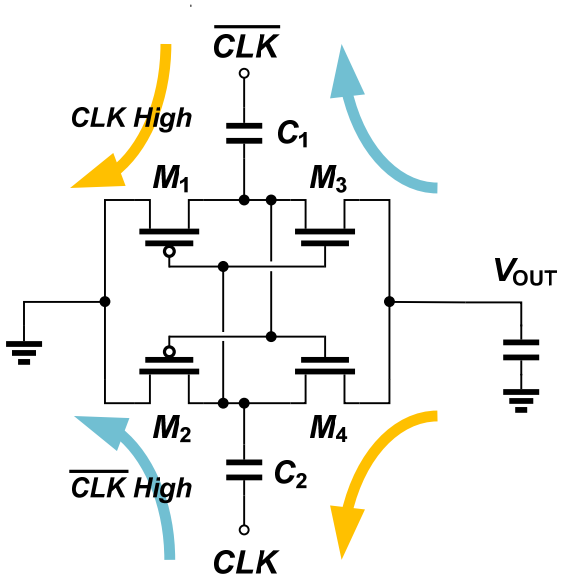


Figure 48. Negative voltage generation using the charge pump.

the large voltage swing can not go over the threshold voltage. In this way, the high-power handling capability of the antenna switch can be enhanced.

The voltage reference circuit shown in Figure 45 generates two stable voltages out of

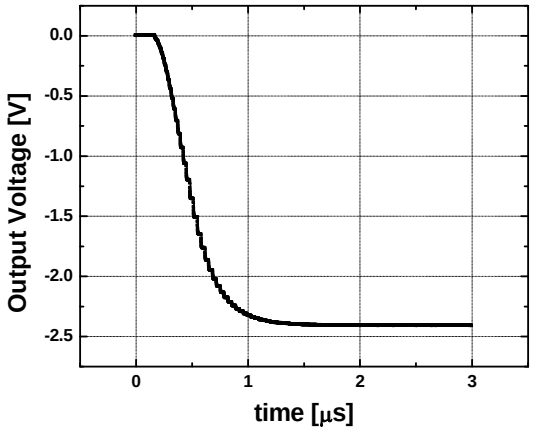


Figure 49. Simulation result of the negative voltage generation.

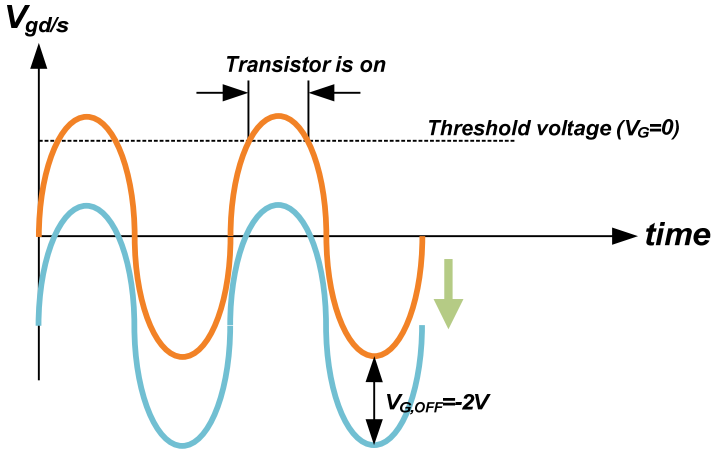


Figure 50. Voltage swing shift using the negative voltage.

the battery voltage, one for the supply voltage of the charge pump and the clock buffer and the other for the antenna-switch turn-on voltage. The turn-on voltage should be free of fluctuation to minimize noise in the RF signal, but the charge-pump supply voltage shows switching noise at every clock cycle due to the switching nature of the charge pump. Thus, the separate turn-on voltage was necessary. The voltage reference covers the battery voltage variation ranging from 2.8 V to 5 V. This range is wide enough to cover

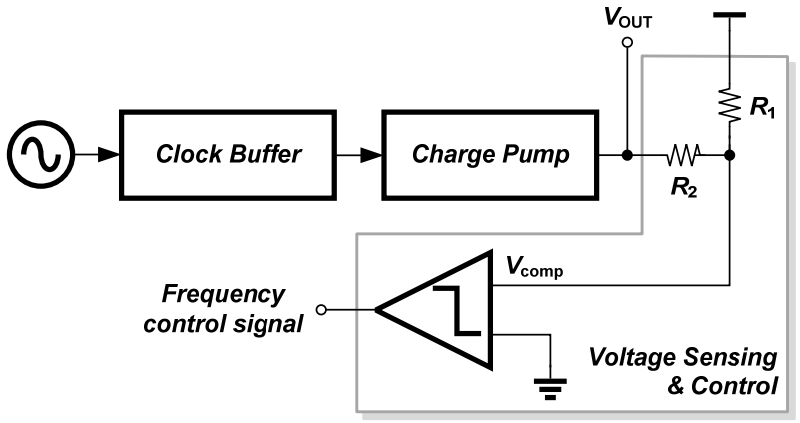


Figure 51. Voltage sensing and clock frequency control.

the variation of the battery voltage for most RF and analog circuits in front-end applications. This removes the necessity of any external regulator for the antenna switch.

5.1.2. Current reduction technique

The current consumption of the antenna-switch driver is a key parameter since it degrades the overall efficiency of a front-end, especially when the antenna switch is in a receiving mode or a stand-by mode. The dominant current consumers of the antenna-switch driver are the charge pump and the clock buffer, and the current consumption of these blocks is proportional to the clock frequency. Therefore, it is essential to reduce the clock frequency to minimize the current consumption. However, if the clock frequency is lowered, the time to generate the negative voltage is lengthened. This may cause difficulties to meet a rising time requirement of the driver for some applications. Thus, in this letter, it is proposed to lower the clock frequency once the negative voltage reaches a certain level.

The clock frequency can be controlled by the circuit shown in Figure 51. A fraction

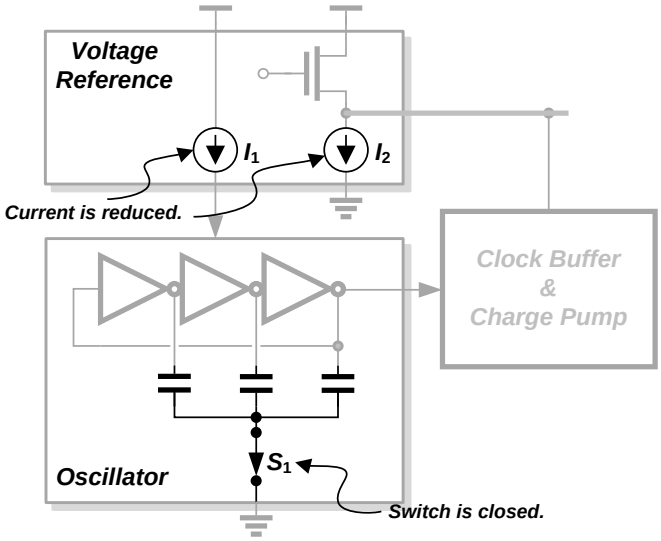


Figure 52. Methods to decrease clock frequency.

of the voltage difference, V_{comp}, between the charge-pump supply voltage and the negative voltage is compared to the reference voltage, 0 V in this case, and the comparator output is triggered when V_{comp} goes below the reference voltage. The ratio of the sensing resistors, R_1 and R_2, are determined for V_{comp} to be 0 V when the negative reaches the target negative voltage. Also, the value of the resistors should be very large to minimize the current leaking through the resistors, which may lower the level of the negative voltage.

Once V_{comp} goes below the reference voltage, the frequency control signal is set by the comparator, and the clock frequency is controlled as shown in Figure 52. The bias current for the oscillator, I_1, is reduced, and the capacitors at the output of each inverter are turned on by the switch, S_1. As the clock frequency is proportional to the bias current and inversely proportional to the capacitance, the clock frequency is lowered, reducing the current consumption. Furthermore, the bias current of the voltage buffer for the

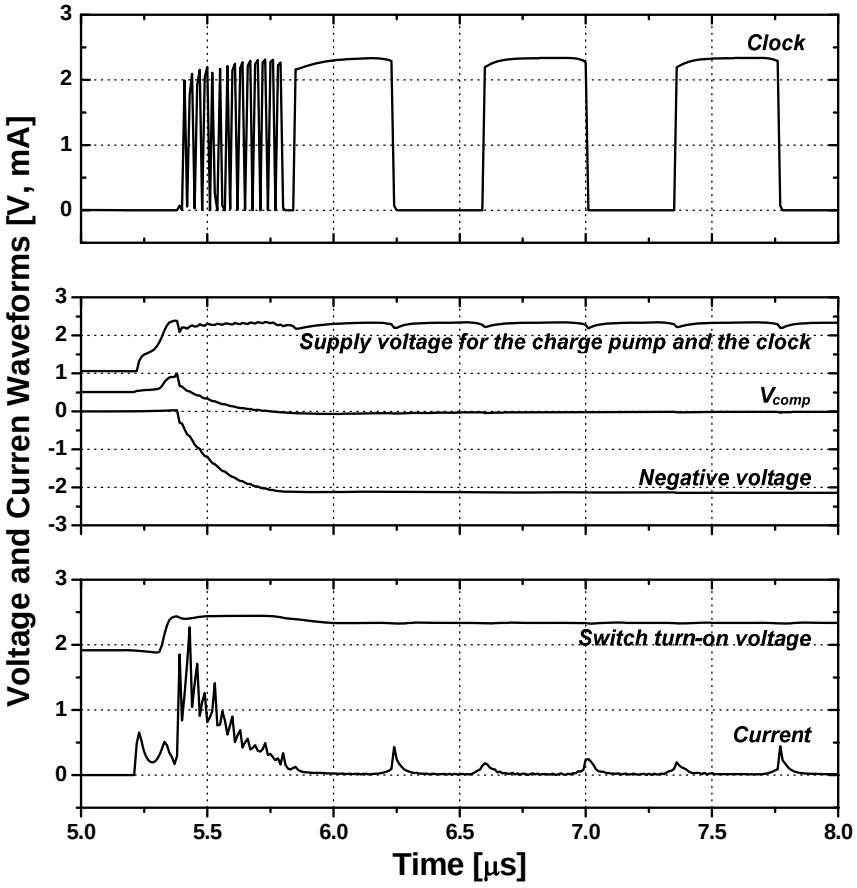


Figure 53. Simulated voltage and current waveforms.

charge-pump supply voltage is also decreased to further reduce the current consumption.

Shown in Figure 53 are the simulated voltage and current waveforms of the antenna-switch driver. The clock shows the frequency of 30 MHz from 5.4 μs to 5.8 μs before V_{comp} goes below the reference voltage, 0 V. After the comparator switches its output at 5.8 μs, the clock frequency goes down to 1.3 MHz by reducing the bias current and turning on the capacitors at the oscillator as shown in Figure 52. The current waveform shows the reduction of the current consumption after the frequency control signal is enabled. Also shown in Figure 53 are the supply voltage for the charge pump and the

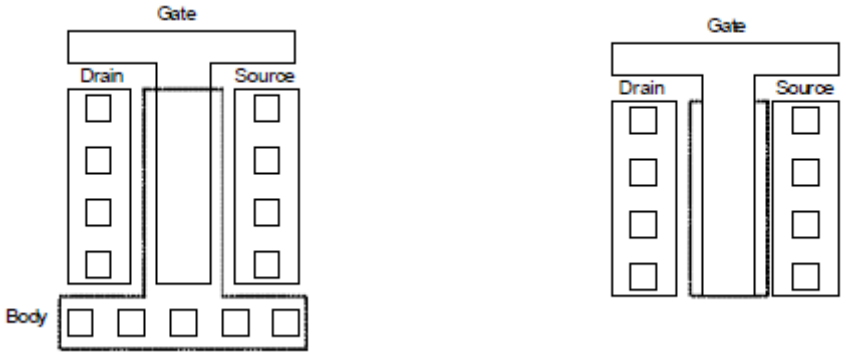
clock and the switch turn-on voltage. As previously discussed, the turn-on voltage shows significantly low voltage ripple, minimizing the noise in the RF signal.

To minimize the current consumption in the stand-by mode, all the circuits in the driver are turned off, which includes the voltage reference circuit, the charge pump, and the clock generation blocks. The decoder should remain in operation to recognize the control input change to turn the circuits back on when necessary.

5.2. SOI ANTENNA SWITCH

Many wireless communication standards such as GSM require output power level of 35 dBm at 900 MHz and 33 dBm at 1.9 GHz. Commonly, multi-stacked FETs are used to implement the antenna switch to handle watt-lever power.

The advantages of the SOI technology in designing the antenna switch can be understood in two ways. First, the SOI technology can easily integrate digital blocks with the antenna switch. Dissimilar to the GaAs pHEMT technology, the SOI technology is capable of implementing complementary transistors for digital functionalities. The digital function can be implemented by using enhancement-mode (E-mode) pHEMT technology, but the area and the cost of the E-mode pHEMT technology are much higher than that of the SOI technology. Second, the SOI technology does not suffer from the parasitic capacitances. The bulk CMOS technology is a good candidate for the integrated antenna switch, but the parasitic capacitance is the bottleneck. As the operational frequency increases and the gate width of the transistor increases to reduce the on-resistance, the loss through the parasitic capacitance becomes significant. Even with multi-stack FETs configuration, the SOI technology shows less parasitic capacitance, resulting in lower



(a) (b)

Figure 54. Two types of FETs in the SOI technology: (a) body contacted and (b) floating body.

insertion loss and better linearity than the bulk CMOS technology. So, the SOI technology was chosen for this research.

The SOI technology used in this research was a partially-depleted SOI which provides two types of FETs, a body contacted (BC) FET and a floating body (FB) FET. The layout views of these FETs are shown in Figure 54. The FB FET is advantageous in terms of the size and the ease of control because that the body terminal of the FET does not need to be controlled. However, the uncertainty of the body voltage exists with large voltage swings. Moreover, the breakdown voltage of the BC FET is higher than that of the FB FET [55]. Thus, in this research, the BC FET was chosen to implement the antenna switch.

Figure 55 shows the SOI antenna switch using the multi-stack FETs with the integrated controller. The device size of the series path to the antenna port needs to be carefully determined to meet low insertion loss and high isolation requirements, simultaneously because the increased device size, which can lower the insertion loss, may

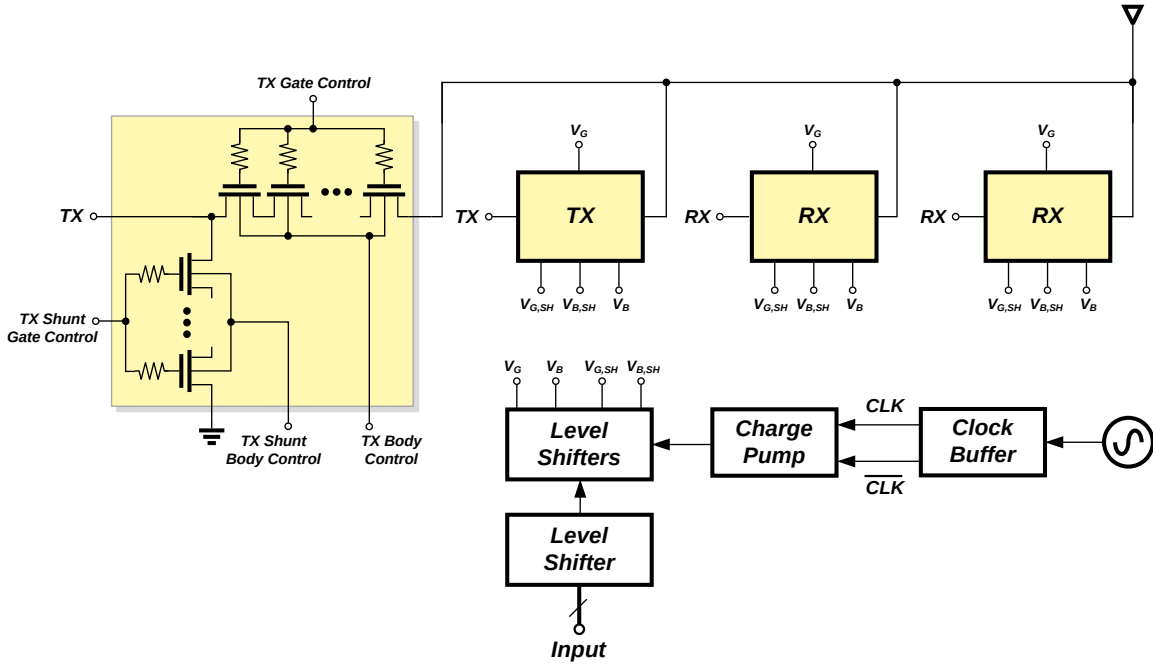


Figure 55. Integrated SOI antenna switch with its controller.

result in a degraded isolation performance. Furthermore, the increased size may cause an impedance mismatch at the antenna port due to the large OFF-state parasitic capacitance. The shunt paths are necessary to enhance the isolation performance. Since the Rx shunt path does not handle high power signals, the number of stacks in the Rx path does not have to be the same as that of the Tx path.

The circuit diagram of the SOI antenna switch is shown in Figure 56. There are 4 RF ports, 2 TX ports and 2 RX ports. The number of stacks was chosen to be 10 to handle up to 35 dBm of power. Each transistor is 4-mm wide to decrease the on-resistance. As previously mentioned, the parasitic capacitance of the SOI transistor is minimal, compared to the bulk CMOS technology. Thus, the stack of 10 transistors does not degrade the insertion loss of the antenna switch. The control voltage to turn off the

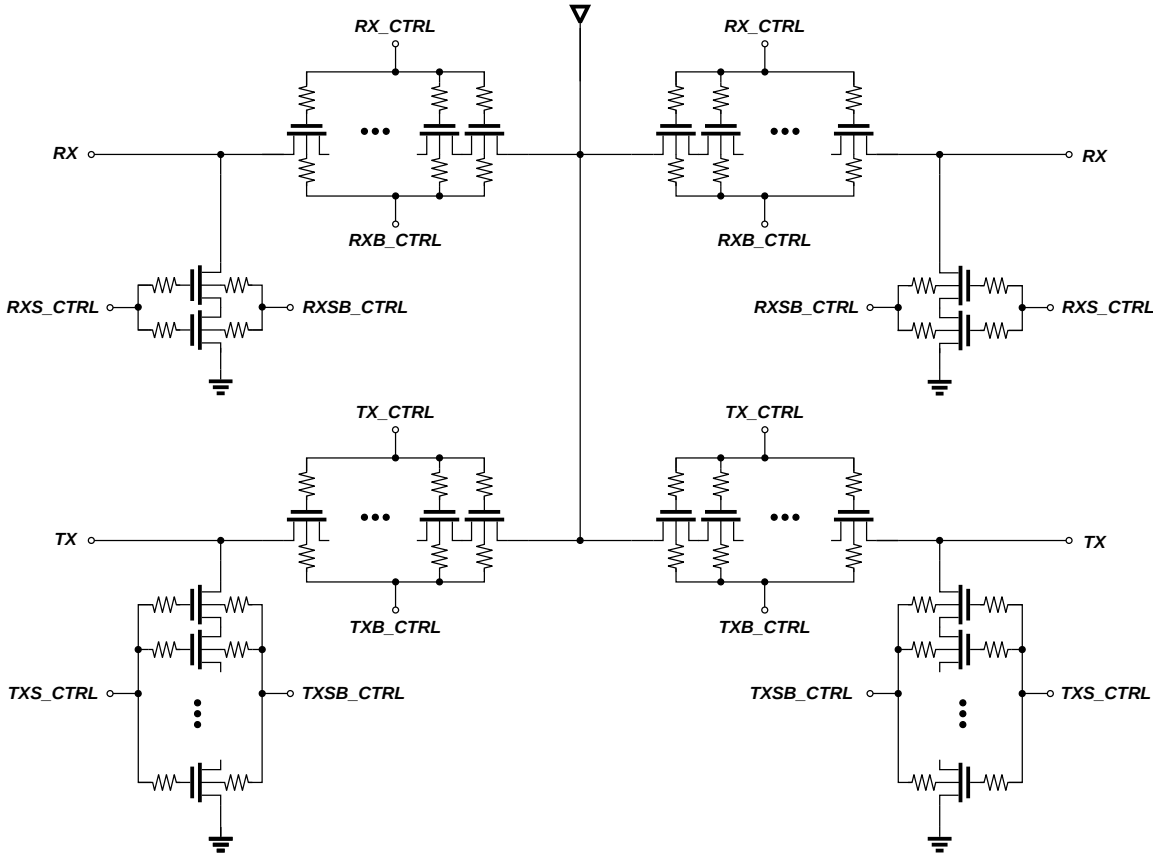


Figure 56. SOI antenna switch circuit diagram.

transistors was chosen to be -2 V instead of 0 V to increase the available voltage swing applied between the gate and the source/drain. The negative voltage is generated by the integrated controller. The control voltages for each gate of the transistors are shown in Table 3. The control voltages for TX are 2.5 V and -2 V to turn on and to turn off the switch, respectively.

Simulation results of the SOI antenna switch are shown in Figure 57. The insertion and the isolation are shown in Figure 57 (a). As expected, the insertion loss at 2 GHz of frequency is 0.3 dB and is comparable or superior, compared to the GaAs pHEMT counterpart. The isolations from RX to RX/TX port are less than -35 dBc at the frequency

Table 3. Control voltages for each transistor of the antenna switch.

Volts	TX1	TX2	TX1 shunt	TX2 shunt	RX1	RX2	RX1 shunt	RX2 shunt	TX1 body	TX2 body	TX1,2 shunt body	RX1,2 body
TX1	2.5	-2	-2	2.5	-2	-2	2.5	2.5	-2	-2	-2	-2
TX2	-2	2.5	2.5	-2	-2	-2	2.5	2.5	-2	-2	-2	-2
RX1	-2	-2	2.5	2.5	2.5	-2	-2	2.5	-2	-2	-2	-2
RX2	-2	-2	2.5	2.5	-2	2.5	2.5	-2	-2	-2	-2	-2

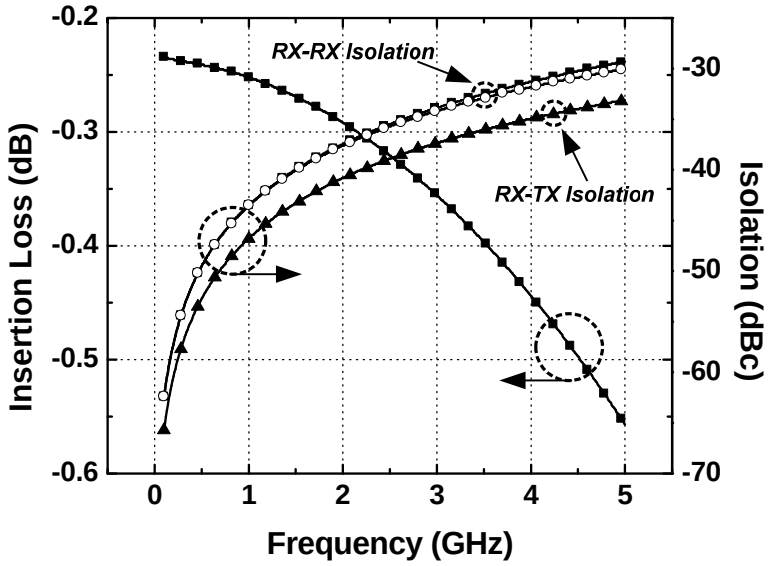
of interest. In Figure 57 (b), the linearity performance of the antenna switch is shown. The second harmonic at 35 dBm of power is less than -70 dBc, and the third and the fourth harmonics are less than -90 dBc.

5.3. MEASUREMENT RESULTS

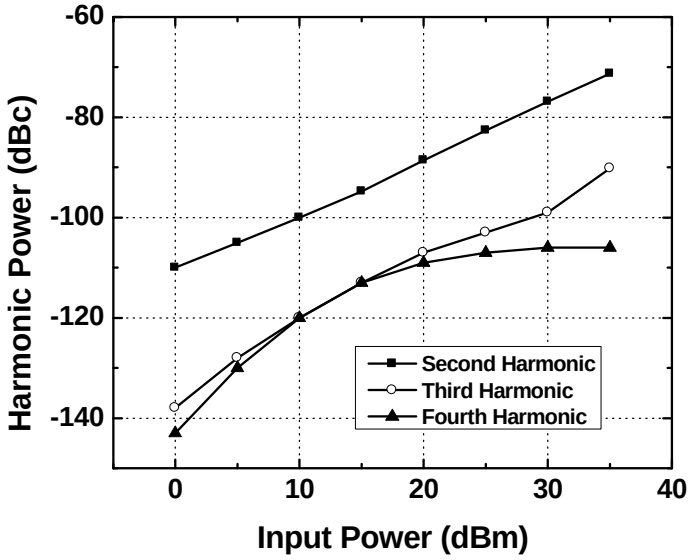
5.3.1. Controller measurement results

The die photograph of the integrated antenna switch fabricated in the SOI CMOS technology is shown in Figure 58. The entire die area is 0.88 mm × 1.15 mm, including the driver and the antenna switch. The core driver area is 0.39 mm × 1.15 mm.

In Figure 59, the measured current consumption of the antenna-switch driver with the frequency control technique to reduce the current is compared to that of the driver without the technique. Without the frequency control technique, the antenna-switch driver consumes more than 850 μA at 2.8-V supply voltage, and the current is increased to more than 950 μA at 5 V. With the frequency control, however, the current consumption is reduced to less than 100 μA and 200 μA at 2.8-V and 5-V supply voltage,



(a)



(b)

Figure 57. Antenna switch simulation results: (a) Insertion loss and isolation and (b) Harmonic power with various input power.

respectively. More than 750 μA of current can be saved in the entire supply voltage range from 2.8 V to 5 V by using the frequency control technique. The stand-by mode current is less than 5 μA over the entire battery voltage range.

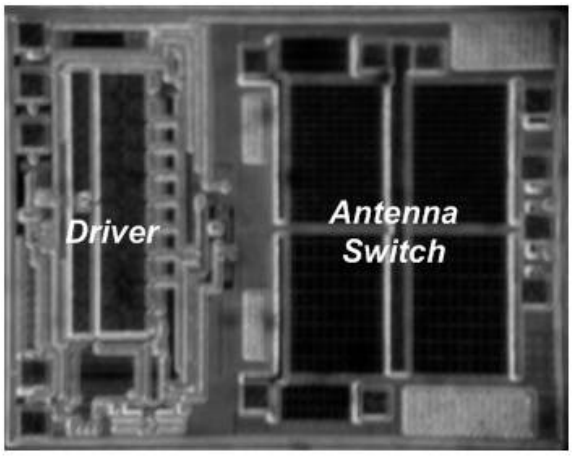


Figure 58. Die photograph of the integrated antenna switch showing the antenna-switch driver and the antenna switch

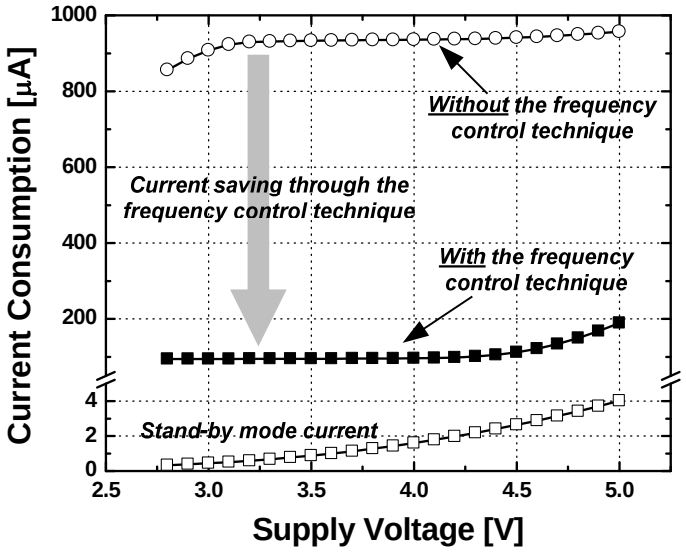


Figure 59. Measured current consumption of the antenna-switch drivers with the frequency control to reduce the current consumption and without it.

In Figure 60, the measured current consumptions and the 2nd and 3rd harmonic powers are shown with different input power levels to the integrated antenna switch. The antenna-switch controller is very vulnerable to the input power since the input level

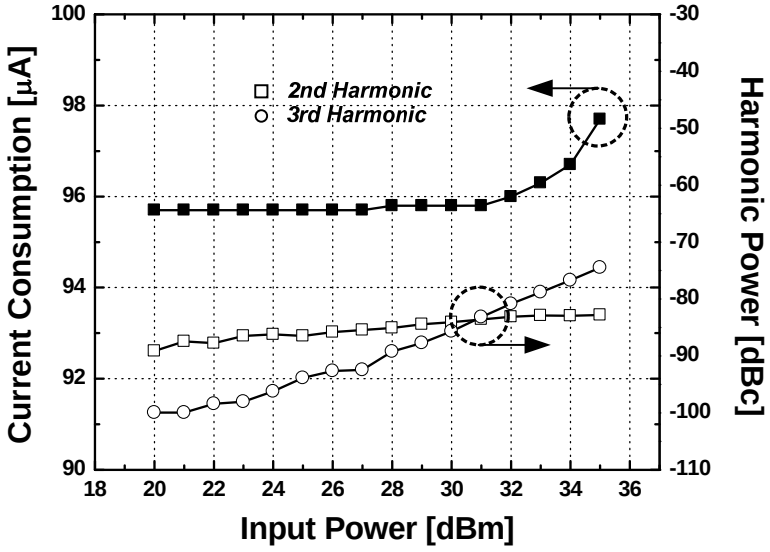


Figure 60. Measured current consumption and the harmonic powers of the antenna switch with different RF input powers.

reaches 35 dBm and the controller is located very closely to the antenna switch. The coupling from the antenna switch to the controller can affect the operation of the antenna-switch controller, resulting in the lowered negative voltage level. In turn, the lowered voltage increases the harmonic power levels abruptly. However, as shown in Figure 60, the harmonic power levels do not show the abrupt increase up to 35 dBm of input power. This implies that the negative voltage is kept even with the high-power input signals.

5.3.2. Antenna switch measurement results

As shown in previous section, the integrated SOI antenna switch was fabricated using the SOI CMOS technology, and the die photograph of the integrated antenna switch is shown in Figure 58.

The small signal performances of the antenna switch is shown in Figure 61. The insertion loss of the integrated antenna switch is shown in Figure 61 (a). The

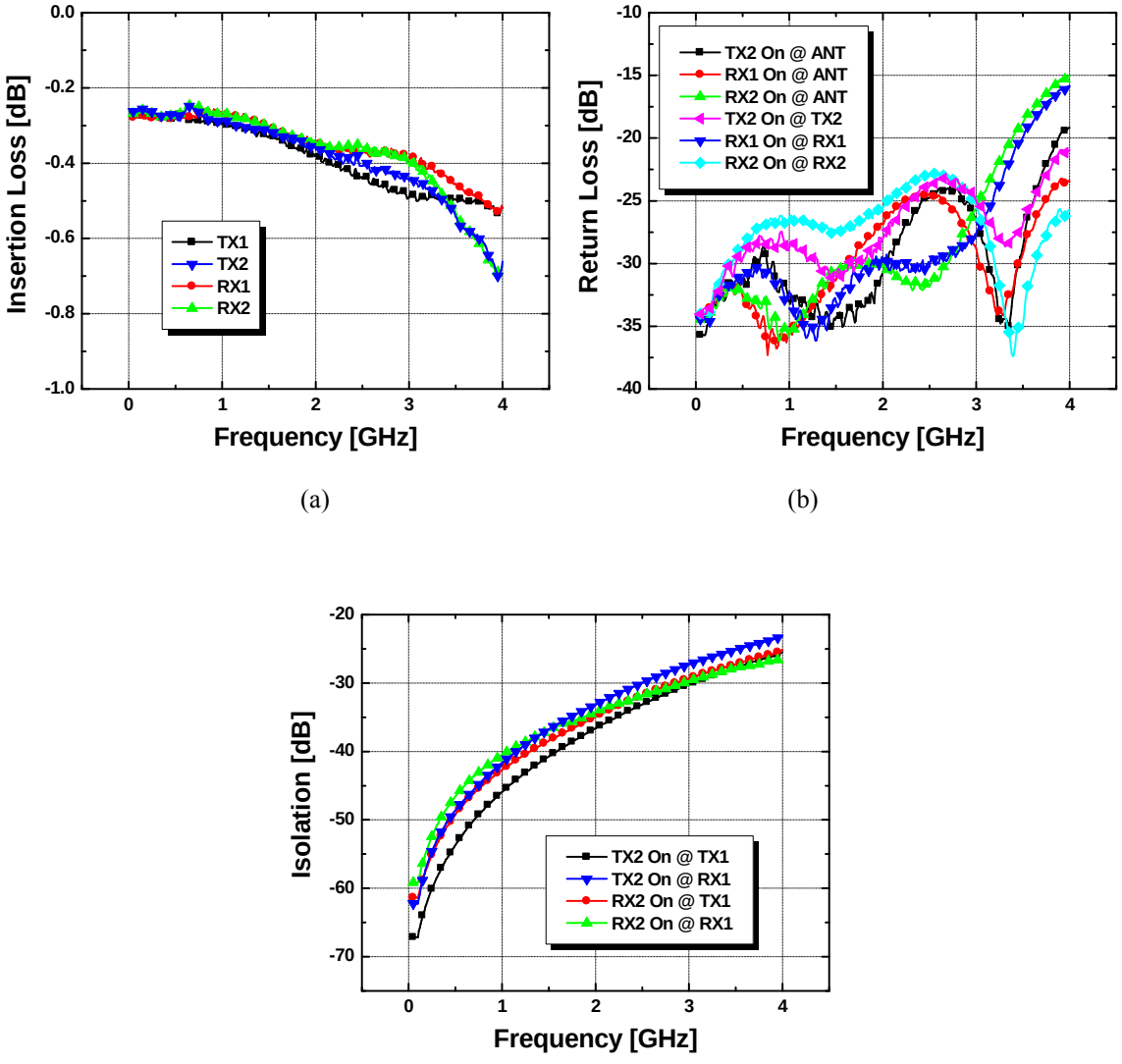


Figure 61. Measured (a) insertion loss, (b) return loss, and (c) isolation of the SP4T antenna switch.

measurement data shows that the insertion loss of the TX ports is -0.27 dB and -0.34 dB at 900 MHz and 1.9 GHz, respectively. The insertion loss of the RX ports is -0.27 dB and -0.4 dB at 900 MHz and 1.9 GHz, respectively. The return loss is shown in Figure 61 (b). The return loss was measured using chip-on-board (COB) configuration. The bonding wire was made as short as possible to minimize the effect of the bonding wire. The first

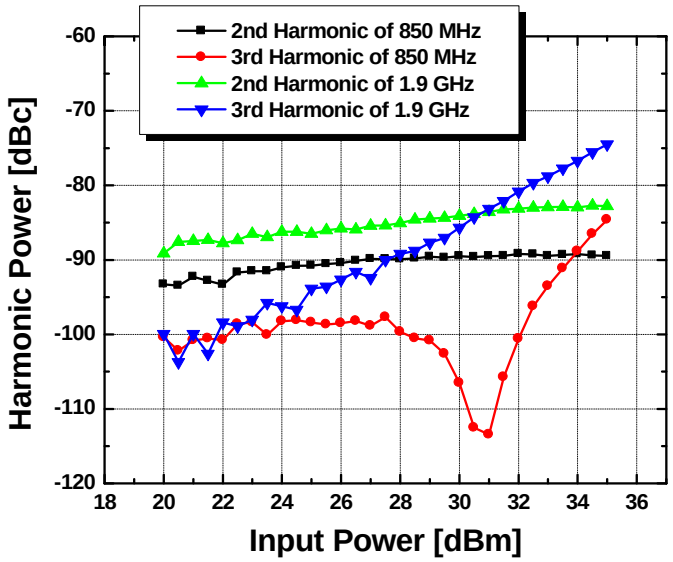


Figure 62. Measured harmonic power levels.

entry of legend represents the return loss measured at the antenna port when TX2 port is turned on, and the fourth entry shows the return loss at the TX2 port when TX2 port is on. As shown in the figure, the return loss of the integrated antenna switch is less than -20 dB up to 3 GHz. At the frequencies of interest, which are 900 MHz and 1.9 GHz, the return loss was measured to be lower than -26 dB and -24 dB, respectively. Even at 4 GHz, the return loss is less than -15 dB. The last small signal performance is the isolation as shown in Figure 61 (c). The first entry represents the isolation between the antenna port and the TX1 port when TX2 is turned on. The isolation at 900 MHz shows less than -40 dBc and that at 1.9 GHz shows less than -33 dBc.

The harmonic power levels of the antenna switch is shown in Figure 62. The measurement harmonic power levels at 850 MHz and 1.9 GHz show exceptional performance. The 2nd and 3rd harmonics of 850-MHz input signal are -90 dBc and -87 dBc with 35-dBm input power, respectively. Those of 1.9-GHz input signal are obtained

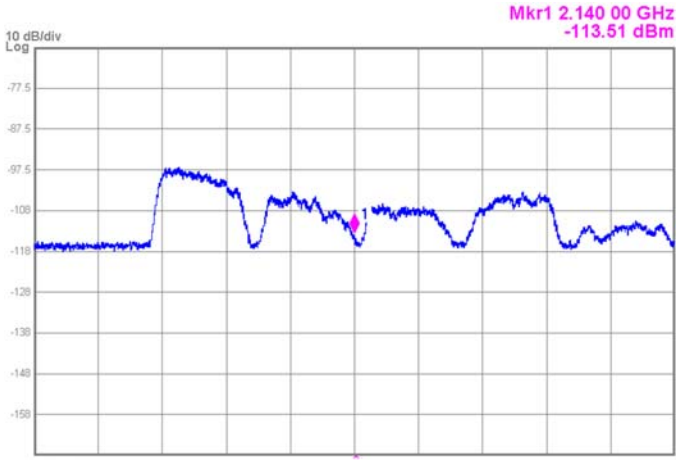


Figure 63. Measured IMD performance.

to be -84 dBc and -80 dBc with 33-dBm input power, respectively. The higher order harmonics are also measured to be less than -90 dBc. These performances show less than 10-% variation with the temperature change from -25 °C to 85 °C.

The intermodulation distortion (IMD) performance of the antenna switch was also measured, based on [56] and is shown in Figure 63. The measured IM3 is -113 dBm with -15-dBm interference signal at RX band.

5.4. CONCLUSION

In this chapter, an integrated antenna switch was implemented using the SOI CMOS technology. A low-power-consumption integrated antenna-switch controller generates a negative voltage to turn off the antenna switch. This negative voltage improves the linearity performance of the antenna switch. By sensing the generated negative voltage, the clock frequency of the controller is lowered to reduce the current consumption. The

current consumption is reduced by more than 80 % using the proposed frequency control technique. The integrated antenna switch showed superior performances compared to commercially available antenna-switch products. The insertion loss is less than -0.4 dB at 1.9 GHz, and the harmonic power level with 35-dBm input power is less than -87 dBc. The implemented antenna switch can be a great candidate for the integrated front-end solution.

CHAPTER 6
LINEAR RF ENVELOPE DETECTOR

As previously mentioned, the CMOS technology has inherent non-linear elements, and this forces the CMOS PA consumes more current the GaAs PA to maintain the same level of linearity. Thus, the efficiency of the CMOS PA is inferior to the GaAs PA on its own. However, the CMOS technology has a great advantage over the GaAs technology. That is the ability to integrate analog and digital circuits for the control. For example, the bias circuit of the CMOS technology can be very dynamic according to the input power by using the power detector, but it is not easy to incorporate the functionality into the GaAs technology. It may be possible, but the cost becomes too high. So, the initial research for the CMOS PA was focused on the PA bias control. Since the stack of transistors is typically used in the CMOS technology to avoid the breakdown, the biasing of the transistors become more important to improve the linearity and the efficiency of the CMOS PA.

In addition, the advanced modulation scheme such as HPSK uses variable envelope and the peak-to-average power ratio (PAPR) increases. To ensure that the peak power of the signal is not distorted, the PA has to be biased at a backed-off position from its peak power level. For example, the PAPR of the WCDMA signal is 3.5 dB when the maximum output power is 28 dBm. So, the PA should be biased to generate 28-dBm of output power when the maximum power of the PA is 31.5 dBm. Since the PA shows its highest efficiency at its maximum power level, it is inevitable to degrade the efficiency. To alleviate the problem, the envelope detector can be utilized. By detecting the

instantaneous power of the signal and biasing accordingly at the peak power level of the PA, the efficiency performance can be improved.

6.1. ENVELOPE DETECTOR CIRCUIT IMPLEMENTATION

High-speed envelope detectors are necessary to estimate power of RF signals and control the PA. Especially, as envelope tracking (ET) or envelope elimination and restoration (EER) techniques [57] are employed in transceivers, it became crucial for RF envelope detectors to track wide-bandwidth modulated envelope signals such as WCDMA or WiMAX in a linear fashion.

The proposed RF envelope detector improves linearity and widens bandwidth of envelope signals by employing a simple inverter-based voltage-to-current converter, denoted by VIC in Figure 64 and AC-coupling the voltage-to-current converter with a rectifier [58].

Shown in Figure 65 is a simplified circuit diagram of the current-mode full-wave rectifier followed by an integrator to filter out high-frequency components at the output voltage. It consists of two half-wave rectifiers [59], M_1 and M_3 or M_2 and M_4, in parallel, and currents from each branch are combined at a current mirror, M_5 and M_6. Differential current inputs generated by the voltage-to-current converter turns on and off diode-connected input transistors, M_1 and M_2, in terms of AC. To handle RF carriers, widths of the transistors were minimized. When current flows in, the current goes through M_1 or M_2 since M_3 and M_4 are biased to flow a certain amount of current. The output current flowing through M_5 and M_6 remains the same. By contrast, when current flows out, the current is drawn from M_5 through M_3 or M_4, keeping the current in M_1 and M_2 the same.

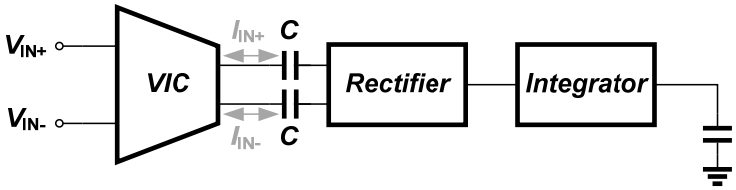


Figure 64. RF envelope detector block diagram.

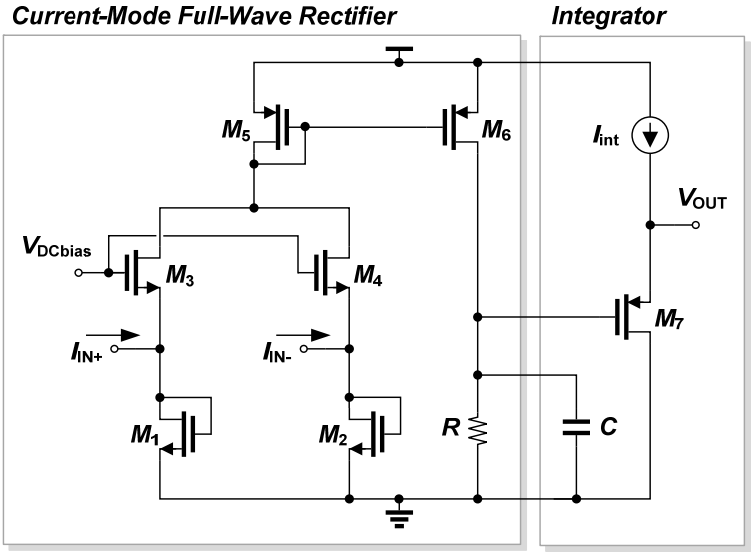


Figure 65. Simplified circuit diagram of the current-mode full-wave rectifier with the integrator.

This results in half-wave rectified output current in each branch. As mentioned previously, the half-wave rectified output currents are summed in M_5 and M_6, generating full-wave rectified output currents. Following the rectifier, the integrator smoothes out ripples caused by the radio frequency carrier.

Bias currents flowing in M_1 through M_4 sets the lower limit that the rectifier can successfully rectify. The current waveforms of the rectifier output are shown in Figure 66. As the bias current decreases, the rectifier can successfully rectify smaller variations. For instance, if the bias current is set to be 100 μA, the rectifier is not able to rectify the

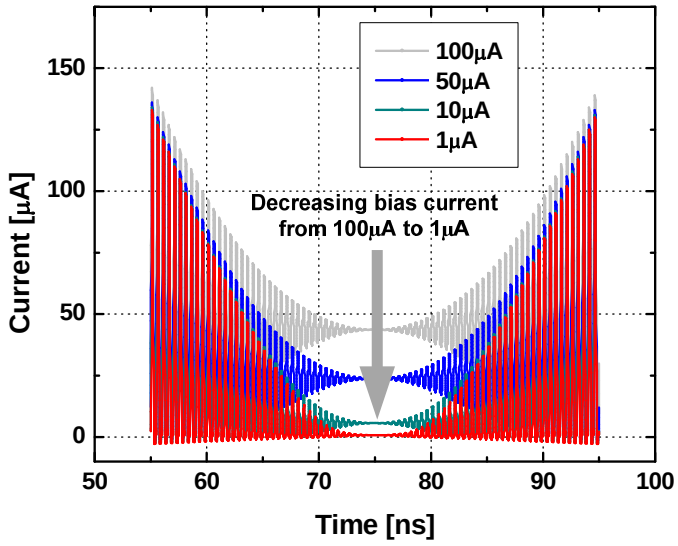


Figure 66. Simulated output current waveforms of the rectifier with different bias currents.

variation whose magnitude is less than 45 μA so that the input variation less than 45 μA gives the same output level, which, in turn, results in an error. Reducing the bias current is the key in improving linearity of the rectifier output. In addition, it was necessary to AC-couple the voltage-to-current converter with the rectifier to block a large DC current from the voltage-to-current converter as shown in Figure 64.

Due to the small size of the transistors and the small bias current of the rectifier, impedance looking into the rectifier is relatively large. To flow RF currents into the rectifier, impedance looking into the voltage-to-current converter should be much larger than that into the rectifier. However, to provide current swing of hundreds of micro-Ampere to drive the rectifier, size and bias current of the converter should be much larger than those of the rectifier. Thus, it is difficult to achieve such high impedance at RF with the conventional operational transconductance amplifier in [59-61].

To achieve such high impedance, an inverter was employed as shown in Figure 67.

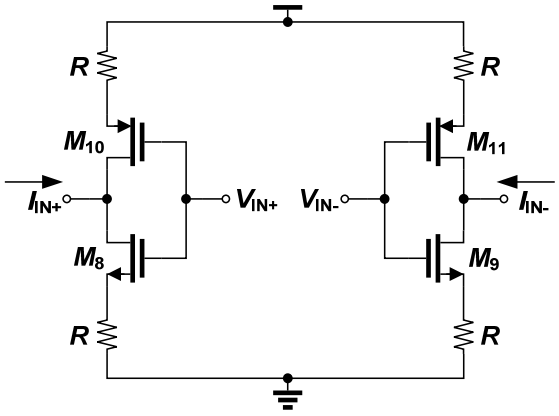


Figure 67. Simplified circuit diagram of the voltage-to-current converter.

The input voltages, V_{IN+} and V_{IN-}, partially turn off the transistors that are not conducting current, resulting in high impedance. For instance, when V_{IN+} goes high, M_8 turns on, and M_{10} turns off. Looking into a drain of the off transistor, M_{10}, the impedance is relatively large compared to that looking into the rectifier. Thus, current is drawn from the rectifier and flows into the converter. If the impedance looking into the drain of M_{10} becomes small when V_{IN+} goes low, the current flowing down through M_8 is drawn from M_{10} instead of the rectifier. To maintain the linear relationship between the input voltage and the output current, however, degeneration resistors, R, are used. The degeneration resistors prevent the inverter from acting as a digital inverter so that the envelope information can be preserved.

6.2. MEASUREMENT RESULTS

To verify performances, the proposed RF envelope detector was fabricated using a standard 0.18-μm CMOS technology. The die photo of the fabricated chip is shown in

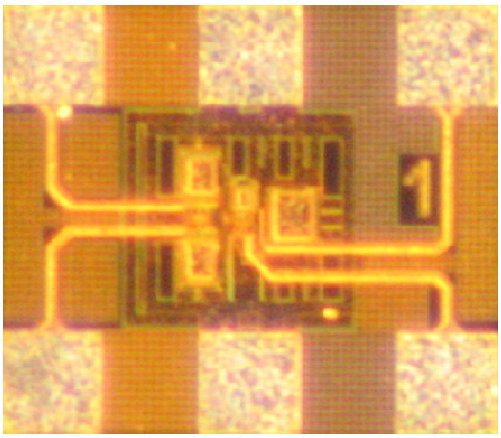


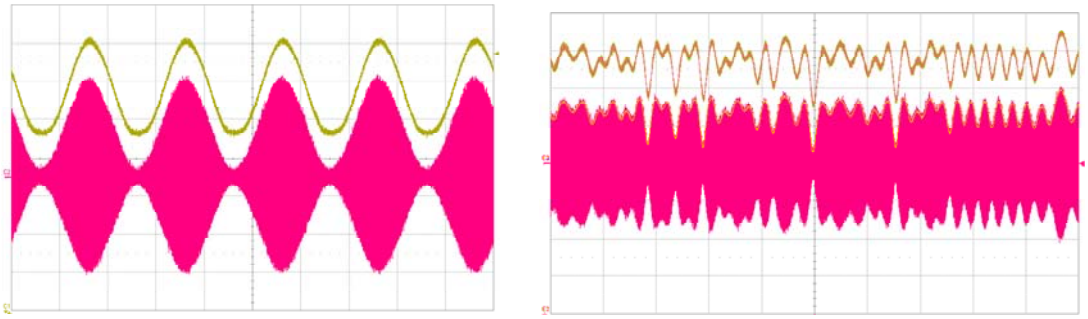
Figure 68. Die photo of the fabricated RF envelope detector.

Figure 68. The active area is 0.12 × 0.12 mm^2, and it consumes 1.8 mW of power with 1.8-V power supply voltage. Including 6 pads, the area is 0.12 mm^2.

Figure 69 shows the measured input and output of the RF envelope detector, where the carrier frequency is 1.95 GHz and the envelope is 1-MHz sinusoidal and 3.85-Mcps WCDMA uplink signal. It can be seen that the output is successfully tracking the input.

The static characteristic of the proposed RF envelope detector was evaluated using 1.9-GHz RF carrier and is shown in Figure 70. The static input dynamic range of the proposed RF envelope detector is 35 dB.

However, more important performance measure of the RF envelope detector is dynamic characteristic because the detector should provide, in real time, linear envelope information at its symbol rate to control output power of EER or ET transceivers. Thus, the proposed RF envelope detector was further evaluated using several different envelope informations including sine waves, WCDMA, and WiMAX, where the carrier frequency of the sine waves and WCDMA is 1.95 GHz and that of WiMAX is 2.4 GHz. The



(a) (b)

Figure 69. Measured input and output waveforms of the RF envelope detector (a) with 1.95-GHz RF carrier and 1-MHz sinusoidal envelope and (b) with 1.95-GHz RF carrier and 3.85Mcps WCDMA uplink envelope.

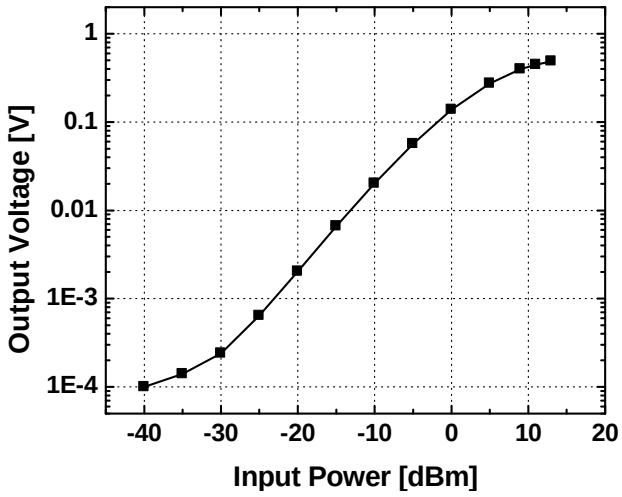


Figure 70. Measured static transfer characteristic of the proposed RF envelope detector.

dynamic transfer characteristics of the proposed RF envelope detector are shown in Figure 71. Inputs and outputs were normalized to its amplitude. For different envelope informations, the proposed RF envelope detector gives linear response over the whole range of the input signal.

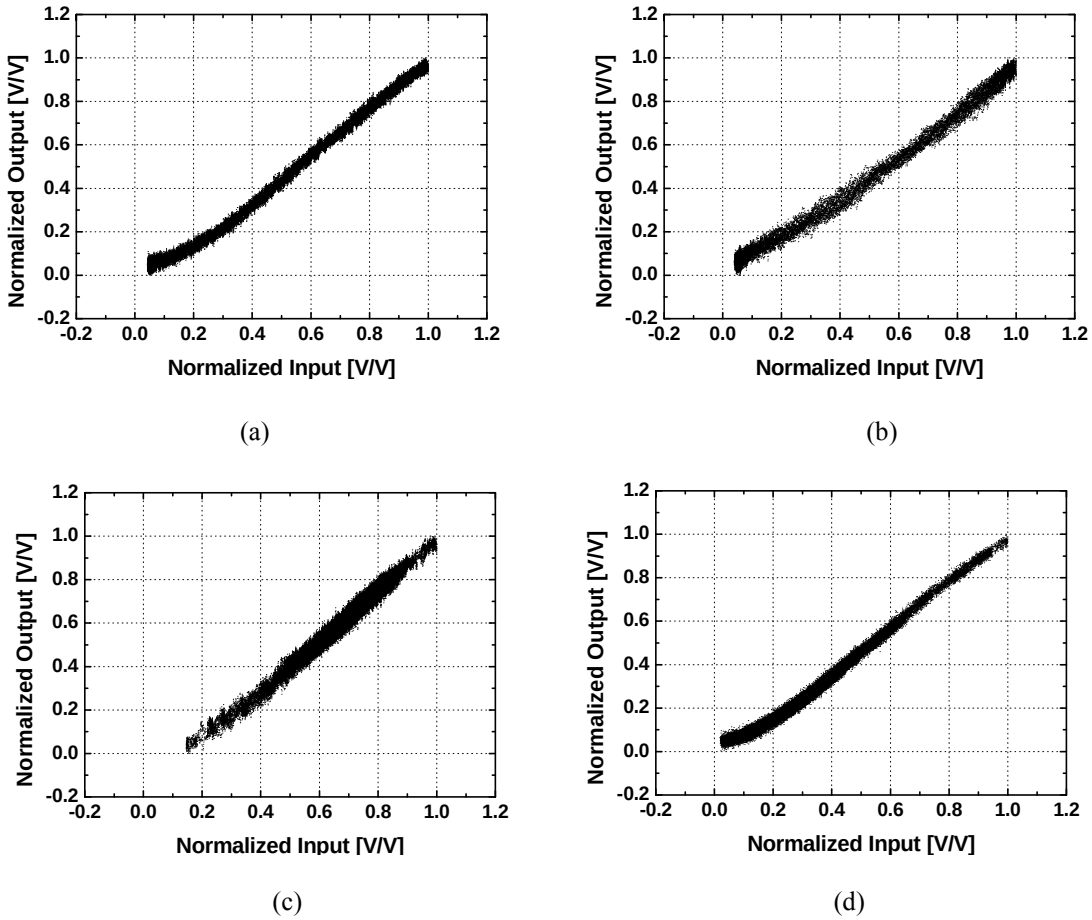


Figure 71. Measured dynamic transfer characteristics of the proposed RF envelope detector with (a) 1-MHz sine envelope, (b) 5-MHz sinusoidal envelope, (c) WCDMA uplink envelope, and (d) WiMAX uplink envelope.

The summary for performances of the proposed RF envelope detector and the comparisons with previously published works are shown in Table 4.

6.3. APPLICATION

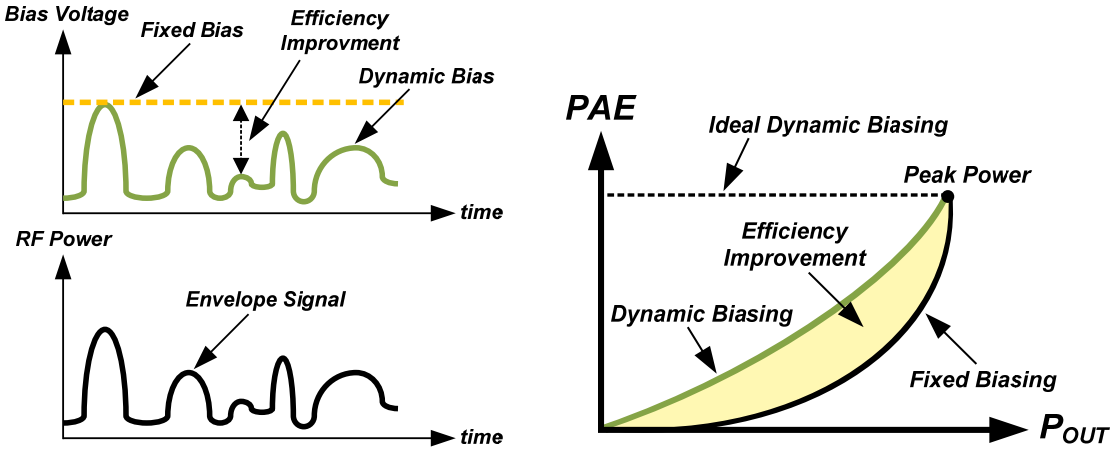
Since the advanced modulation schemes were employed to increase the date rate in the given bandwidth, the necessity of linear amplifiers has emerged. For the advanced

Table 4. Summary of performances and comparisons

	This work	Work in [59]	Work in [60]
Technology	0.18-µm CMOS	0.35-µm CMOS	0.18-µm CMOS
Carrier Bandwidth	1 GHz ~2.4 GHz	~10 MHz	100 Hz ~1.6 GHz
Envelope Bandwidth	5 MHz (Linear)	n/a (Square)	5 kHz (Square)
Power	1.8 mW	1.98 mW	6.3 mW

modulation schemes, information is contained in envelope as well as in phase. The PA should amplify the varying envelope signal in a linear fashion to preserve the information contained in the envelope. The varying envelope signals have PAPR, and the amount of back-off is determined, based on the PAPR of the signal. The PAPR of HPSK, for example, is about 3 dB, and that of 128 quadrature amplitude modulation (QAM) is about 8 dB. Thus, the PA should back off by the amount shown above to maintain the linearity of the signal by sacrificing the efficiency. As the PAPR increases, the efficiency degradation becomes significant.

There have been researches on the efficiency improvement for the varying envelope signals such as polar transmitters and linear amplification with nonlinear components (LINC). However, the complexity of the above approaches is very high. A simple approach to improve the efficiency is to bias the PA dynamically. As previously mentioned, the efficiency of the PA is maximized at the maximum power level. So, it is very effective to bias the PA at its maximum power level at all time.



(a) (b)

Figure 72. (a) Conceptual ideal of the dynamic biasing schem and (b) efficiency curves of dynamic biasing scheme and fixed biasing scheme.

The concept of the dynamic biasing scheme is shown in Figure 72 (a). The dynamic biasing uses varying bias voltage which follows the envelope signal. As the instantaneous power is reduced, the bias voltage, as shown in green, is lowered to save power, enhancing the efficiency. As opposed to the dynamic biasing scheme, the fixed biasing scheme, as drawn in yellow, uses a fixed voltage which is determined for the maxim power level. Thus, the PA consumes the same amount of DC current even when the RF power is reduced. The efficiency curves of the dynamic biasing scheme and the fixed biasing scheme are shown in Figure 72 (b). The ideal power added efficiency (PAE) curve of the dynamic biasing scheme follows the dotted line. Since the PA is biased at its maximum power level at all times, the PAE is always at maximum. However, the physical size of the PA is fixed, and the output matching network is designed for the maximum power level. Because of these non idealities, the actual PAE follows the green curve. As shown in black, the typical PAE curve shows a rapid drop as the output power

decreases from the peak power level. The effect of the back-off in the typical fixed biasing scheme is much more severe, compared to the dynamic biasing scheme. The yellow shade represents the amount of efficiency improvement by using the dynamic biasing scheme.

6.4. CONCLUSION

A highly-linear RF envelope detector has been proposed. The RF envelope detector utilizes an inverter with degeneration for a voltage-to-current converter and a current-mode full-wave rectifier with an integrator for detecting wide-bandwidth modulated envelope signals. The proposed RF envelope detector generates linear response over the whole range of the input signals of 5-MHz sine envelope, WCDMA uplink, and WiMAX uplink. This RF envelope detector allows precise amplitude modulations and amplitude error corrections of various wireless standards. The fabricated envelope detector only takes 0.12×0.12 mm^2 of area and 1.8 mW of power.

CHAPTER 7
CONCLUSION AND FUTURE WORK

7.1. TECHNICAL CONTRIBUTIONS AND IMPACTS OF THE DISSERTATION

Over the past decade, the RF front-end has been incredibly improved in terms of performance and integration. The increasing demand of customers for higher data rate and more functionalities within a small form factor has driven this trend for the decade. For instance, today's wireless communication devices should be able to support multiple wireless standards such as GSM, EDGE, WCDMA, and so on. Even non-cellular standards such as WLAN and Bluetooth became standard features of wireless communication devices.

In realizing commercially-available products that satisfy the customers' demand, the manufacturing cost is one of the most critical factors. To reduce the cost, the industry has been trying to include as many components in the front-end as possible, and the CMOS technology has been the spearhead of the integration because of its advantages over other process technologies such as GaAs. In fact, most of the components in the today's front-end including all the digital blocks and most of the RF blocks has been successfully integrated in one chip. Only bottlenecks holding up the entire integration includes the PA and the antenna switch as discussed in Chapter 1.

The difficulties to integrate the PA and the antenna switch are originated from the inferior characteristics of the CMOS technology to deal with large signals. The output power of the PA reaches 33 or 35 dBm for the GSM applications, it is very difficult to

maintain the linearity of the signal while maintain the relatively high efficiency performance. Thus, the GaAs products prevail in the market. However, the GaAs products necessitate the external control circuitries to control its behavior such as the voltage boosting circuitry for the GaAs antenna switch as mentioned in Chapter 2. Furthermore, as the wireless standards advance to increase the data rate, it becomes much more difficult to meet the linearity requirements even with the GaAs products which have higher breakdown voltage compared to the CMOS technology.

In this dissertation, various design aspects of the RF front-end, especially the antenna switch design, are addressed to overcome the limitation mentioned above and in the previous chapters. The technical contributions of this dissertation can be summarized as follows.

- A CMOS antenna switch controller to improve the high-power handling capability of the GaAs antenna switch has been developed. The antenna switch controller generates the output voltage over 7 V to bias the GaAs antenna switch by utilizing the charge pump. The comprehensive controller design has been discussed, and the critical factors to design the controller have been identified and incorporated in the design procedure. These factors include the body biasing technique and the leakage current effect. The precise model of the output voltage has also been developed to describe the output voltage behavior of the charge pump. The developed controller successfully drives the GaAs antenna switch up to over 35 dBm of RF power.
- An efficiency improvement technique of the charge pump has been developed. The developed technique utilizes charge sharing to save the

current consumption of the charge pump which is embedded in the antenna switch controller. The charge-sharing time, which is the key parameter to implement the charge sharing, has been analyzed and incorporated in the design procedure. The developed charge pump can save up to 34 % of the current consumption of the charge pump. The current consumption was reduced from 4.5 mA to 3 mA while generating 9.2-V output voltage.

- The current reduction technique for the SOI antenna switch controller has been developed. By varying the frequency of the oscillator in the charge pump, the developed antenna switch controller can save 90 % of current. The current is reduced from 850 to 100 μA and from 950 to 200 μA at 3-V power suppy voltage and 5-V power supply voltage, respectively. The entire controller has been integrated in the SOI die with the antenna switch core.
- A fully-integrated SOI antenna switch has been developed. This antenna switch integrates all the necessary control blocks with the antenna switch by using the SOI technology. The antenna switch controller integrated in this design generates negative voltage to bias the antenna switch, and this improved the high-power handling capability of the antenna switch. The integrated antenna switch can handle 35 dBm of input power with less than -85 dBc of 2nd and 3rd harmonic power levels. The insertion loss of the antenna switch is less than -0.4 dB at 2 GHz. The entire current consumption of the antenna switch is less than 100 μA. The performance of the developed antenna switch exceeds the performances of many commercially-available products.

- A linear envelope detector has been developed by using 0.18-μm CMOS technology. To realize the efficiency improvement of the linear PA, the dynamic biasing can be utilized. The developed envelope detector is the key block to realize the dynamic biasing. The developed linear envelope detector successfully extracts the envelope information out of the modulated RF signal including AM, WiMAX, and WCDMA. The envelope detector only consumes 1 mA of current at 1.8-V power supply voltage, and the size is 0.0144 mm^2.

7.2. SCOPE OF FUTURE RESEARCH

In this dissertation, the research focus was on developing the integrated antenna switch with improved performances. For the purpose, the antenna switch controllers have been developed to decrease the power consumption and to increase the power handling capability of the antenna switch. The integrated SOI antenna switch has also been developed, and the linear envelope detector has been developed to improve the efficiency of the linear PA. Even with this achievement, challenges remain to implement the fully-integrated RF front-end.

First of all, the linearity of the CMOS PA should be improved. Even though there have been a lot of research that showed promising results to improve the linearity of the CMOS PA, it is still a long way to catch up with the GaAs PA. Due to the limitations of the CMOS technology, it is very difficult to meet the linearity and the efficiency requirements at the same time. Thus, the future research should be focused on devising a smart way to improve the linearity without sacrificing the efficiency performance.

Secondly, the PA should be effectively isolated from other circuitries such as analog or digital circuit blocks. Since the PA of the cellular standards generate watt-level output power, of which voltage swing can be up to 15 V, the large voltage swing coupled to adjacent circuitries can make the adjacent control circuits malfunction. This effect is relatively minimized in the SOI technology because of the high-resistive substrate. However, in the bulk CMOS technology, it should be carefully considered to keep the coupling from affecting other circuits. Layout techniques may be involved to alleviate this effect.

Finally, the passive components of the CMOS technology should be improved. Even a small resistance in the output path of the front-end may degrade the output power level and the efficiency performance critically since the output power level reaches up to 35 dBm. Circuit techniques to improve the passive components should be paralleled with technology improvement to achieve the goal.

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