GEORGIA INSTITUTE OF TECHNOLOGY — OFFICE OF CONTRACT ADMINISTRATION

PROJECT ADMINISTRATION DATA SHEET

[X] ORIGINAL [ ] REVISION NO. _____

Project No. E-21-640 (Subproject of B-10-601) GTRI/~~GTX~~ DATE 5 / 16 / 83

Project Director: John W. Hooper/ Robert K. Feeney School/~~Lab~~ OIP

Sponsor: Lockheed-Georgia Company

Type Agreement: P. O. #CA31303

Award Period: From 4/1/83 To 12/31/83 (Performance) 12/31/83 (Reports)

Sponsor Amount:	This Change	Total to Date
Estimated:	$ 25,000	$ 25,000
Funded:	$ 25,000	$ 25,000

Cost Sharing Amount: $ N/A Cost Sharing No: _____

Title: Lockheed/Georgia Tech Cooperative VLSI Program

ADMINISTRATIVE DATA

OCA Contact Frank H. Huff x-4820

1) Sponsor Technical Contact:

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Marietta, GA 30063

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Defense Priority Rating: N/A Military Security Classification: N/A

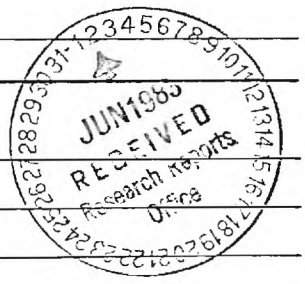
(or) Company/Industrial Proprietary: _____

RESTRICTIONS

See Attached N/A Supplemental Information Sheet for Additional Requirements.

Travel: Foreign travel must have prior approval – Contact OCA in each case. Domestic travel requires sponsor approval where total will exceed greater of $500 or 125% of approved proposal budget category.

Equipment: Title vests with N/A; None proposed



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GEORGIA INSTITUTE OF TECHNOLOGY OFFICE OF CONTRACT ADMINISTRATION

SPONSORED PROJECT TERMINATION/CLOSEOUT SHEET

Date 4/21/86

Project No. B10-601 School/~~XXX~~ OIP

Includes Subproject No.(s) E-21-640

Project Director(s) Hooper & Feeney - E-21-640/Hooper & Feeney - B-10-601 GTRC / ~~XXX~~

Sponsor Lockheed-Georgia Co.

Title Lockheed/Georgia Tech Cooperative VLSI Program

Effective Completion Date: 12/31/83 (Performance) _____ (Reports)

Grant/Contract Closeout Actions Remaining:

- [ ] None
- [XX] Final Invoice or Final Fiscal Report
- [ ] Closing Documents
- [ ] Final Report of Inventions
- [ ] Govt. Property Inventory & Related Certificate
- [ ] Classified Material Certificate
- [ ] Other _____

Continues Project No. _____ Continued by Project No. _____

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FORM OCA 69.285

E-21-6T

Monthly Letter Report No. 1-3

LOCKHEED/GEORGIA TECH COOPERATIVE VLSI PROGRAM

Purchase Order Number: CA 31 303

Performance Period: 1 April to 30 June 1983

Submitted to:

Lockheed-Georgia Company
A Division of Lockheed Corporation
Marietta, Georgia 30063

by:

Georgia Tech Microelectronics Research Center
and
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting Through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

10 July 1983

Monthly Letter Report No. 1-3

This is the first Monthly Letter Report, covering the period 1 April to 30 June 1983. Since the actual project did not start until 30 May, a single report for the indicated period is appropriate.

The cooperative program between Lockheed-Georgia and Georgia Tech is directed toward the design and development of a VLSI chip or set of chips for use in automatic test equipment. The envisioned system will connect to a unit under test through a connector having pins with programmable functions. The multiple functions of each pin will be implemented by what is called the Peripheral Pin Electronics (PPE). The objective of this cooperative effort is to create the PPE using as few components, mainly VLSI, as possible.

The cooperative effort has been tentatively organized according to the outline presented as Table I. The table summarizes an early estimate of the steps leading to a prototype PPE. However, it is anticipated that only about the first seven steps could be accomplished during the initial nine-month period of cooperative effort.

At the time of this report, the first three tasks are nearing completion. For example, it is tentatively planned to use the IEEE-488 instrument bus to connect the PPE to the host computer. This choice, together with the current, voltage, and frequency response requirements of the tester are sufficient to begin a reasonably detailed design of the PPE.

Tasks IV and V are receiving attention concurrently with the other work. Some very preliminary study indicates that CMOS technology might be appropriate for a significant portion of the PPE. It is attractive because voltage levels can be fairly high and both analog and digital functions can be implemented with the same technology. One of the EE faculty, who is potentially available to work on this program, has initiated a CMOS linear circuit design program. It is possible that this work may be of direct use to the cooperative effort.

By the end of the summer it is planned to have completed a detailed functional schematic diagram of the PPE and to have tabulated the electrical specifications of all component modules. At that time the decisions relating to semiconductor technology summarized in tasks IV through VI should be tentatively completed.

Table I. Outline of Project Tasks

I. Establish general specifications of the PPE.

II. Define the modules/functions that make up the PPE.

III. Generate reasonably detailed specifications of each module and prepare an overall functional schematic diagram.

IV. Survey the state-of-the-art to determine how much of each module can be integrated onto a VLSI chip. Consider all processes and ignore cost considerations.

V. For those parts of the PPE that can, in theory, be integrated:

a) What semiconductor device processes are applicable?

b) Is one process common to several modules?

c) Can various processes be combined? Does any semiconductor house routinely combine them?

VI. Specify processing details of those modules that can be integrated (in principle).

VII. Considering cost, yield, and delivery, which modules should be integrated?

VIII. Do a high level (logic, black box) design of each integratable module. Simulate the system at this level. Will it perform as required? Revise the design. Note: some of the design at this level was accomplished very early in tasks II and III.

IX. Design each module at the circuit level. Simulate circuit performance and revise the design.

X. Design each integratable module according to the design rules of the applicable processes. Simulate circuit performance at this (chip) level and revise as necessary. Steps IX and X would probably be done concurrently.

XI. Decide whether to implement the design in silicon.

XII. If an affirmative decision is made, generate masks and fabricate devices for testing. Test and modify the design as required.

E-21-670

Monthly Letter Report No. 4

LOCKHEED/GEORGIA TECH COOPERATIVE VLSI PROGRAM

Purchase Order Number: CA 31 303

Performance Period: 1 July to 31 July 1983

Submitted to:

Lockheed-Georgia Company
A Division of Lockheed Corporation
Marietta, Georgia 30063

by:

Georgia Tech Microelectronics Research Center
and
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Atlanta, Georgia 30332

Contracting Through

Georgia Tech Research Institute
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Atlanta, Georgia 30332

8 August 1983

Monthly Letter Report No. 4

This is the fourth Monthly Letter Report, covering the period 1 July 1983 to 31 July 1983.

Efforts during this period have been directed toward refining the specifications of the Peripheral Pin Electronics (PPE) and continuing the evaluation of candidate semiconductor technologies.

As indicated in the previous report, the IEEE 488 instrument bus was under consideration as the interface between the PPE and the host computer. However, since the tester may be required to communicate simultaneously with more than 100 pins, it was decided that the bit-parallel, byte-serial organization of the IEEE 488 bus might be too slow. If the IEEE 488 bus cannot be used, an obvious next candidate is the bus structure, or a derivative of the bus structure, of a commonly used microprocessor. Since the host computer must be quite powerful, it will probably be one of the 16-bit units made by Motorola or Intel.

CMOS continues to be a favorable candidate for implementing the PPE. A preliminary check of manufacturer's data indicate that 12-bit A/D and 12-bit D/A converters have been successfully fabricated using the CMOS process. Operational amplifiers and analog switches are also routinely made with CMOS. The power dissipation and current sinking capabilities of CMOS are limited, but it was never anticipated that high power functions could be integrated.

As part of an academic project, the MRC is designing and fabricating a CMOS operational amplifier. It is anticipated that this work will be of significant benefit to the joint Lockheed-Georgia Tech project.

Our objectives for the next reporting period include 1) the preparation of a detailed functional specification of the PPE, 2) an extensive investigation of D/A and A/D converter technology, and 3) a decision regarding the PPE bus structure.

Monthly Letter Report No. 5

LOCKHEED/GEORGIA TECH COOPERATIVE VLSI PROGRAM

Purchase Order Number: CA 31 303

Performance Period: 1 August to 31 August 1983

Submitted to:

Lockheed-Georgia Company
A Division of Lockheed Corporation
Marietta, Georgia 30063

by:

Georgia Tech Microelectronics Research Center
and
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting Through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

12 September 1983

Monthly Letter Report No. 5

This is the fifth Monthly Letter Report, covering the period 1 August 1983 through 31 August 1983.

Considerable progress has been made toward defining the specifications of the PPE. Work during this period has concentrated on the analog measurement subsystem. The analog-related functions of the PPE include:

1. DC Voltage Measurement
2. DC Voltage Source or Power Supply
3. DC Current Measurement
4. DC Current Source or Sink
5. Programmable Load Resistance with Pull-Up and Pull-Down Capability
6. Threshold Detection of Digital Signals
7. Adjustable Amplitude Digital Driver
8. Analog Signal Generation From Pre-Stored Digital Data
9. Analog Signal Capture.

A summary of the preliminary analog subsystem specifications is presented in Appendix I.

Figure 1 is a block diagram of the analog measurement system that implements the above functions. Analog switches are used to configure the various components as required for a particular function. For example, to operate as a DC power source with current monitoring, switches S3, S9, S11, S13, and S20 could be closed. The host computer would command the value of output voltage at the D/A converter and amplifier K1 would establish that value at the pin. By closing S8 the voltage could be verified with the A/D converter. All other functions can be similarly implemented by proper positioning of the various switches. In addition, extensive self-testing

is possible by appropriately configuring the switches. For example, the gain of amplifier K1 can be checked by properly setting switches S1, S3, S7, S8 and S20.

As seen from the figure, these analog measurement functions are accomplished with two operational amplifiers K1 and K2. The amplifier K2 is a true differential instrumentation amplifier, while K1 is a device capable of providing the maximum required current of 300 mA. K1 will probably require a VMOS or similar output stage that is off-chip.

It is readily seen from the figure how K1 acts as a voltage source and how K2 measures current. The two amplifiers are used together when the current source/sink or programmable resistor functions are required. Figure 2 is a simplified circuit showing how this is accomplished. Note that having amplifiers with adjustable gain is the key to this realization. These additional functions are obtained with little increase in chip complexity.

A breadboard prototype of the circuit was constructed and tested. Performance was as predicted. A simulation of the circuit using the SPICE program is now underway.

Work over the next period will concentrate on (1) refining the overall block diagram of the PPE including both analog and digital functions, and (2) beginning the detailed description of each functional block of the analog system including device technology and circuit implementation.

Appendix I

Analog Subsystem Specifications

I. DC Power Supply

1. Maximum Current: ± 300 mA
2. Maximum Voltage: ± 15V
3. Settling Time: 10 ms

II. DC Current Source/Sink

1. Maximum Current: ± 300 mA
2. Settling Time: 10 ms

III. DC Voltage and Current Measurement

1. Precision: 12-bits
2. Maximum Voltage: ± 15V
3. Maximum Current: ± 300 mA
4. Conversion Time: 100 µs
5. Input Impedance (Voltage): 22 Meg ohms
6. Offset: No more than ±1 bit for current measurement, ±½ bit for voltage measurement
7. Minimum Current for Full Resolution: 150 µA

IV. Programmagle Load with Pull-Up and Pull-Down Capability

1. Maximum Current: ± 300 mA
2. Minimum Resistance: 10 ohms
3. Maximum Resistance: 100 k ohms
4. Maximum Voltage: ± 15V
5. Resistance Tolerance: ± 10%

V. Threshold Detection of Digital Signals

1. Precision: 5 bits
2. Speed: Schottky TTL
3. Comparison: Simultaneous upper and lower limit check.

VI. Adjustable Amplitude Digital Driver

1. Precision: 12-bits

2. Speed: Schottky TTL unless full 300 mA drive needed.

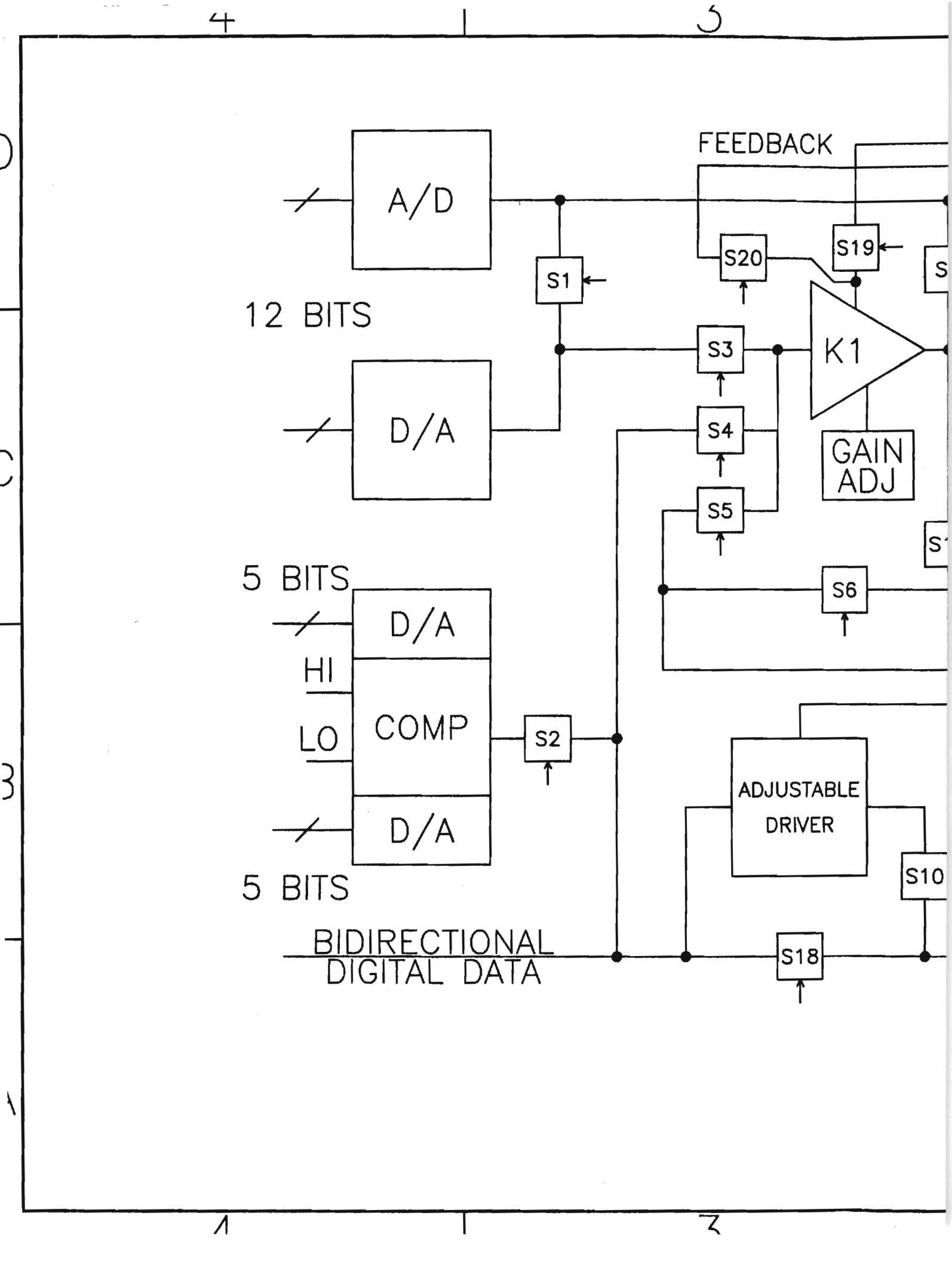
VII. Analog Signal Generation

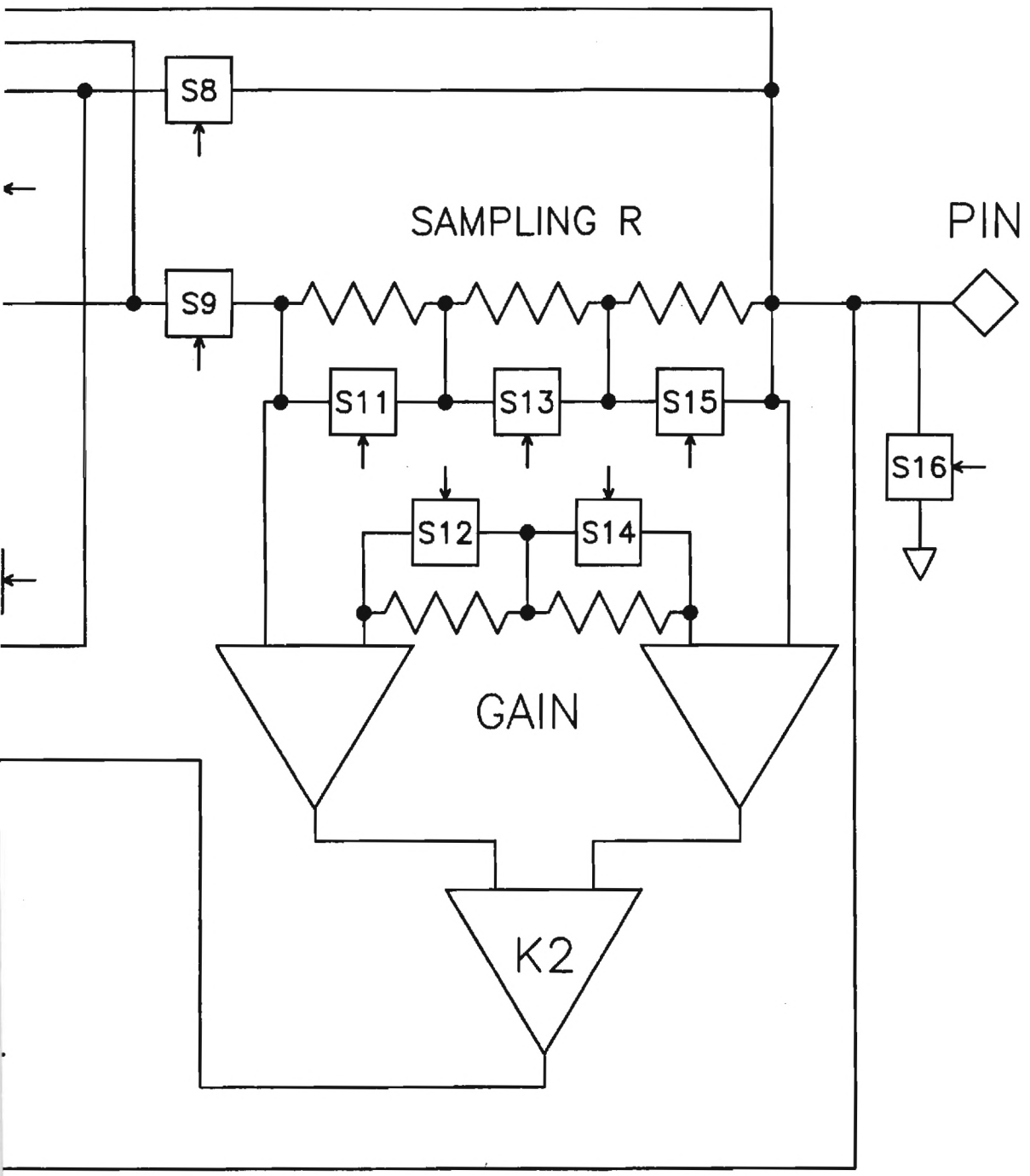
1. Maximum Bandwidth: Limited by D/A converter and output amplifier; 50 kHz is goal.

2. Maximum Current: 300 mA.

VIII. Analog Signal Capture

1. Maximum Bandwidth: Limited by A/D converter; 50 kHz is goal.

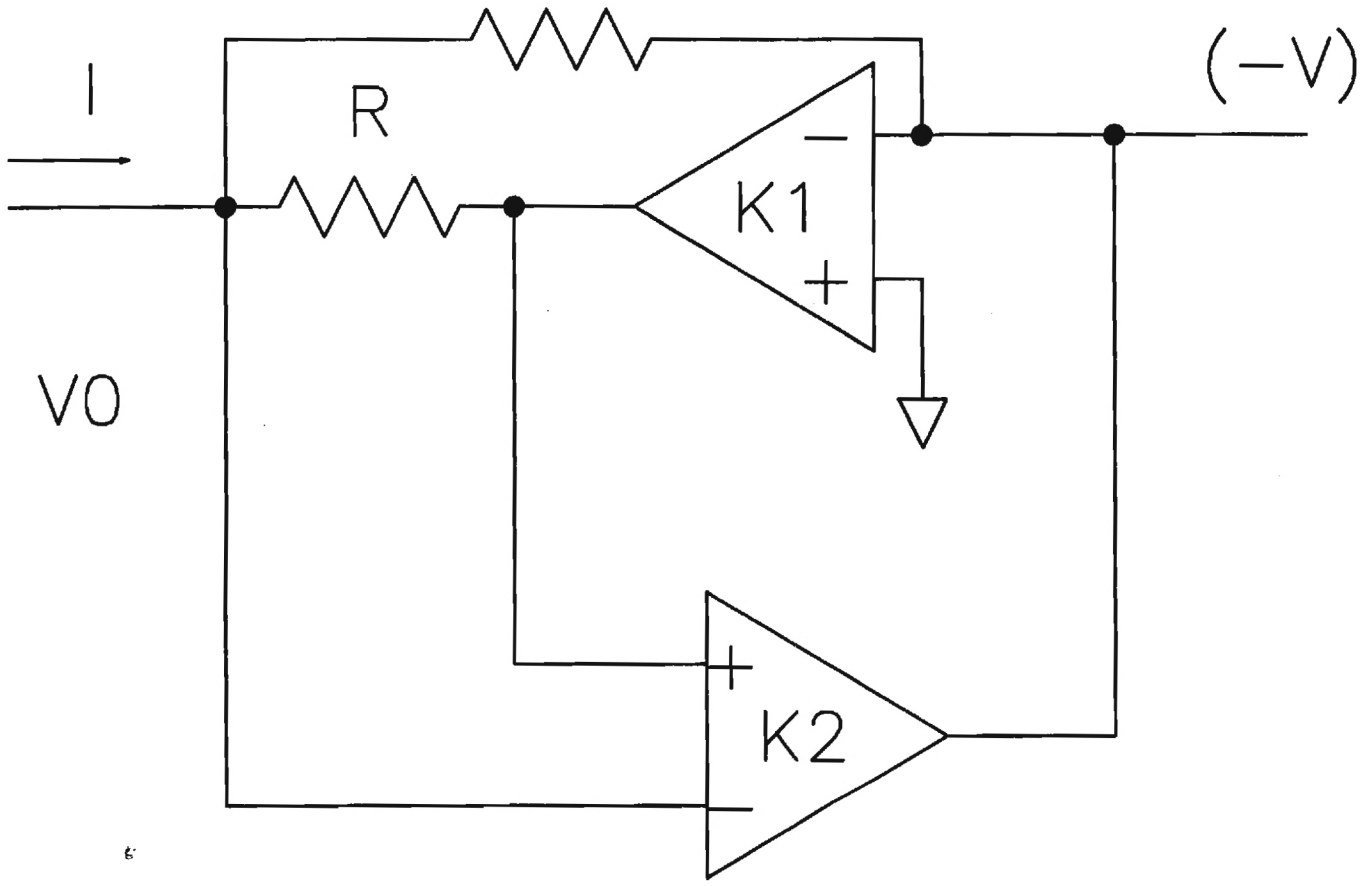

FEEDBACK
A/D
12 BITS
D/A
S1
S20
S19
S3
K1
S4
GAIN
ADJ
S5
S6
5 BITS
D/A
HI
COMP
LO
D/A
5 BITS
S2
ADJUSTABLE
DRIVER
S10
BIDIRECTIONAL
DIGITAL DATA
S18



GEORGIA TECH MICROELECTRONICS RESEARCH CENTER

ANALOG MEASUREMENT SYSTEM

FIGURE 1



PROGRAMMABLE RESISTOR

$$V0 = IRK1K2 + K1V$$

$$REQ = RK1K2$$

CURRENT SOURCE/SINK

$$I = (V0 - K1V)/RK1K2$$

IF K1 IS VERY LARGE

$$I = -V/(K2R)$$

FIGURE 2. PROGRAMMABLE RESISTOR/CURRENT SOURCE REALIZATION.

E-21-640

Monthly Letter Report No. 6

LOCKHEED/GEORGIA TECH COOPERATIVE

VLSI PROGRAM

Purchase Order Number: CA 31 303

Performance Period: 1 September to 30 September 1983

Submitted to:

Lockheed-Georgia Company
A Division of Lockheed Corporation
Marietta, Georgia 30063

by:

Georgia Tech Microelectronics Research Center
and
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

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Georgia Tech Research Institute
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Atlanta, Georgia 30332

12 October 1983

Monthly Letter Report No. 6

This is the sixth Monthly Letter Report, covering the period 1 September 1983 through 30 September 1983.

Work during this period has concentrated on (A) simulating some of the key concepts of the analog measurement subsystem, and (B) defining the digital measurement subsystem.

As indicated in the previous report, the programmable resistor/current source is a key component of the analog measurement subsystem. This subsystem contains several operational amplifiers along with analog switches. The performance of the subsystem is determined primarily by the operational amplifiers. The programmable resistor would often act as a load for a digital device and therefore operate in the large signal regime. The large sifnal capabilities of an operational amplifier are determined by the non-linear parameters of the amplifier circuit. These non-linear aspects are not amenable to simple analyses, but require computer-aided modeling. Some initial efforts at modeling the programmable resistor have been undertaken using the well-known SPICE circuit analysis package. Some of these results are presented in Figures 1 and 2. Figure 1 shown the programmable resistor acting as a pull-up for a single transistor. The circuit is excited with a voltage pulse on the base and the resulting collector waveform calculated. These results show that the ordinary 741-like opamps are capable of doing a reasonable job in the programmable resistor circuit. In conjunction with this effort, a "macromodel" of a generic operational amplifier has been developed. This model takes date sheet type parmeters (gain bandwidth, slew rate, etc.) as inputs and simulates the specified opamp. Such a model will be of significant use in the development of the detailed specifications of the analog portions of the PPE.

Figure 3 is a preliminary block diagram of the digital measurement subsystem. A digital bit stream is either received from or sent to the pin under test. The data are stored in 4096 bit bidirectional register. Such a register is capable of bidirectional transfer of both serial and parallel data. Serial data are clocked in from the pin under test with a clock rate determined by the host computer. The computer sets the desired data transfer rate by setting the programmable clock rate generator to the required value. The system can transmit a unique serial bit stream of up to 4096 bits long. However, a repetition counter allows the same bit stream to be set a predetermined number of times or for an indefinite period.

This is a very preliminary definition of the digital measurement subsystem. It is possible that other features, for example inter-pin communication, will be added to the system.

Work during the next work period will concentrate on refining and expanding the digital and analog subsystem functional description.

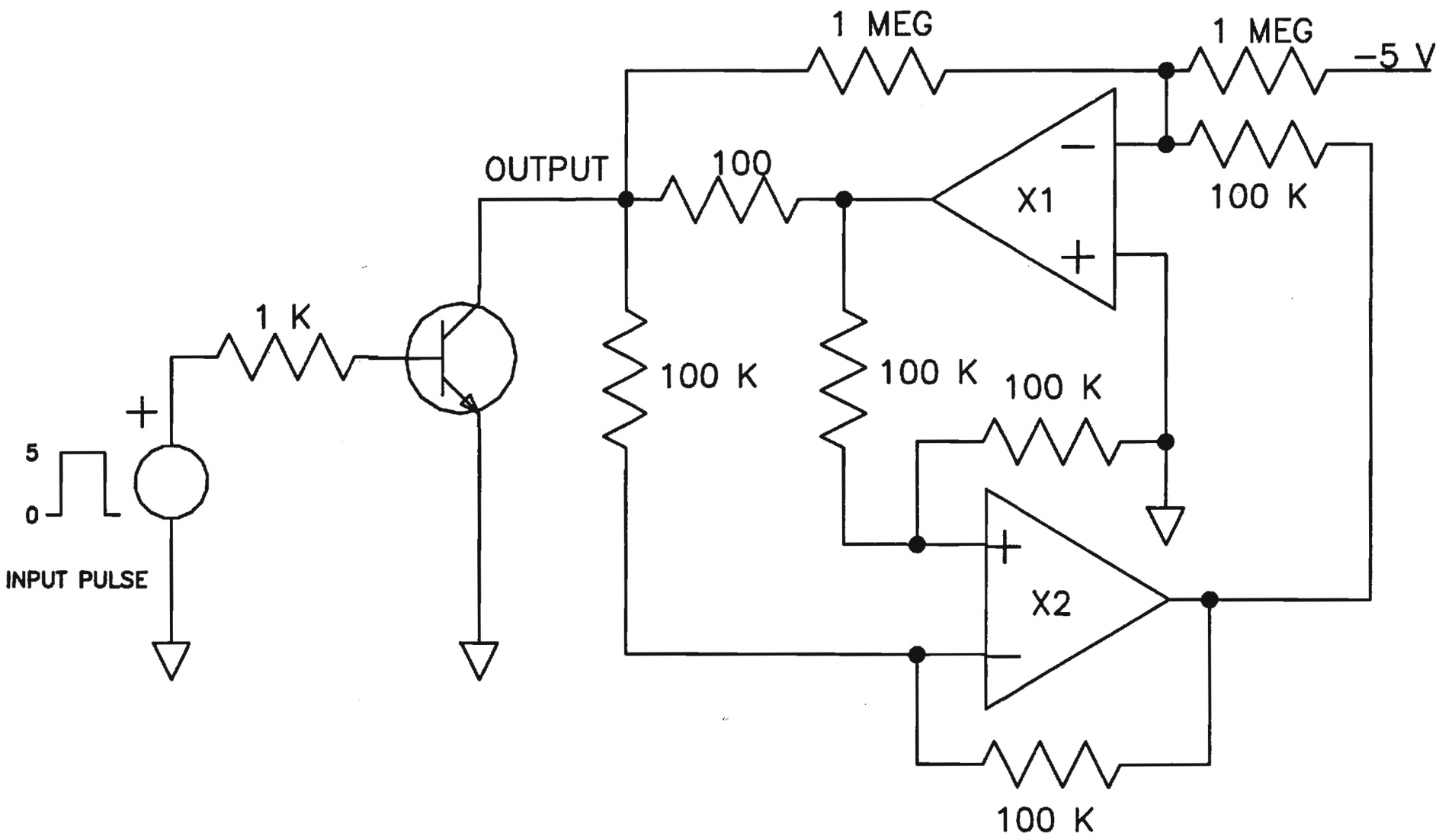
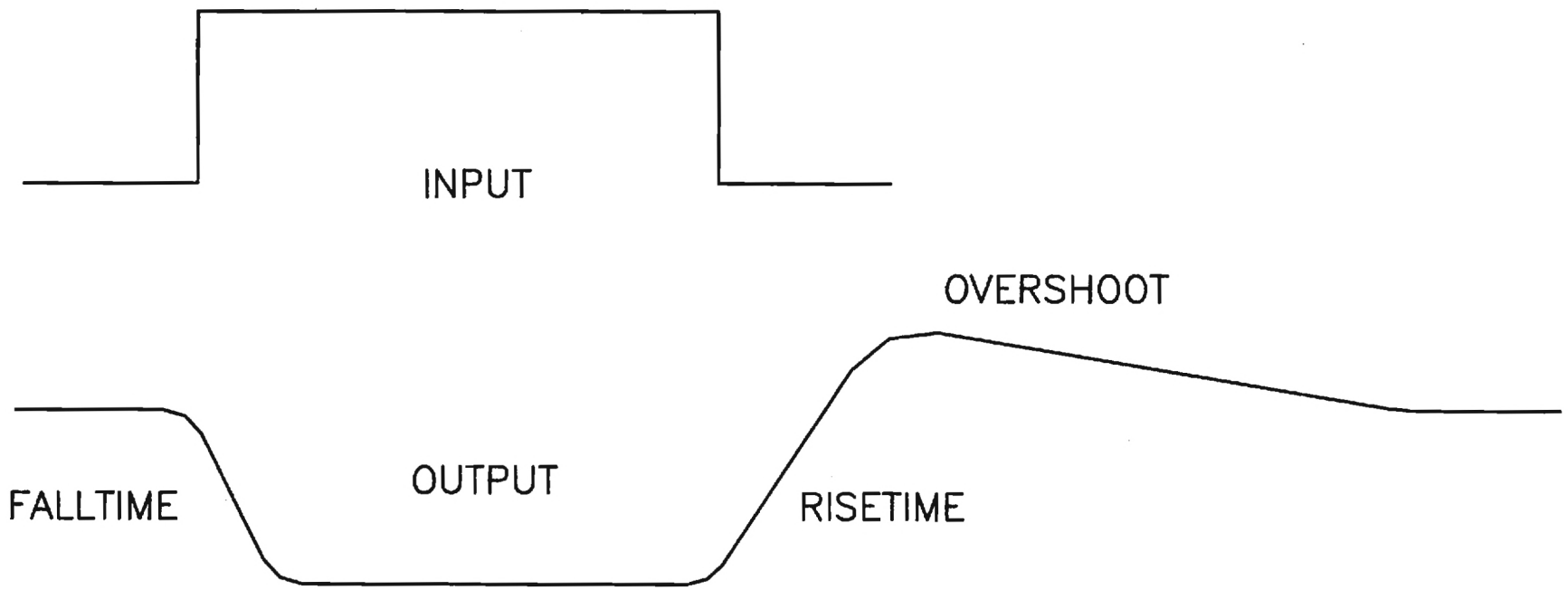


FIGURE 1

PROGRAMMABLE RESISTOR TRANSIENT RESPONSE TEST	
LOCKHEED/GEORGIA TECH	10/11/83



PROPERTY	DETERMINED BY	CALCULATED VALUES
FALL TIME	TRANSISTOR	10 NS
RISETIME	TRANSISTOR AND OPAMP	40 NS
OVERSHOOT	OPAMP	10 PERCENT

FIGURE 2 RESULTS OF SPICE SIMULATION

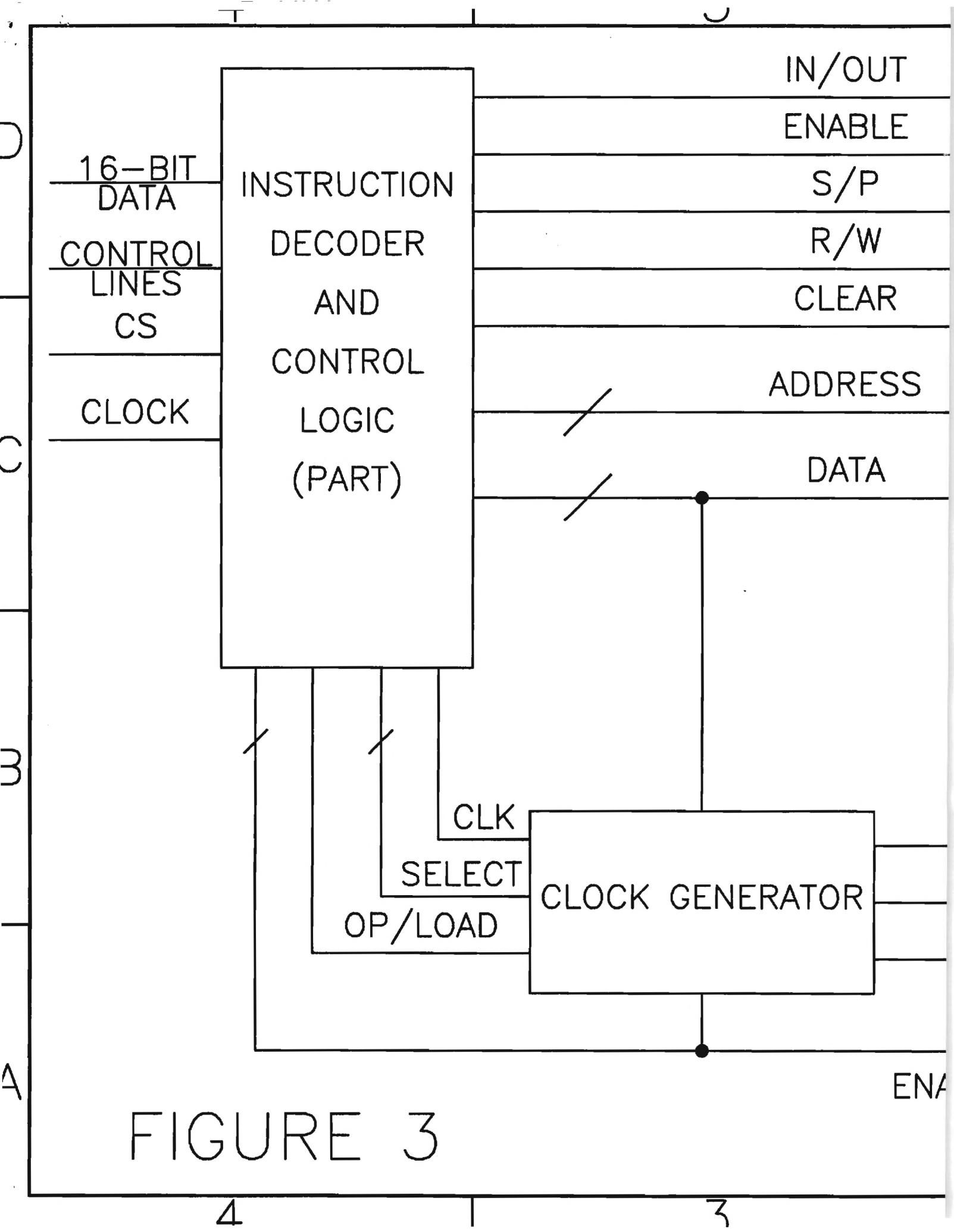
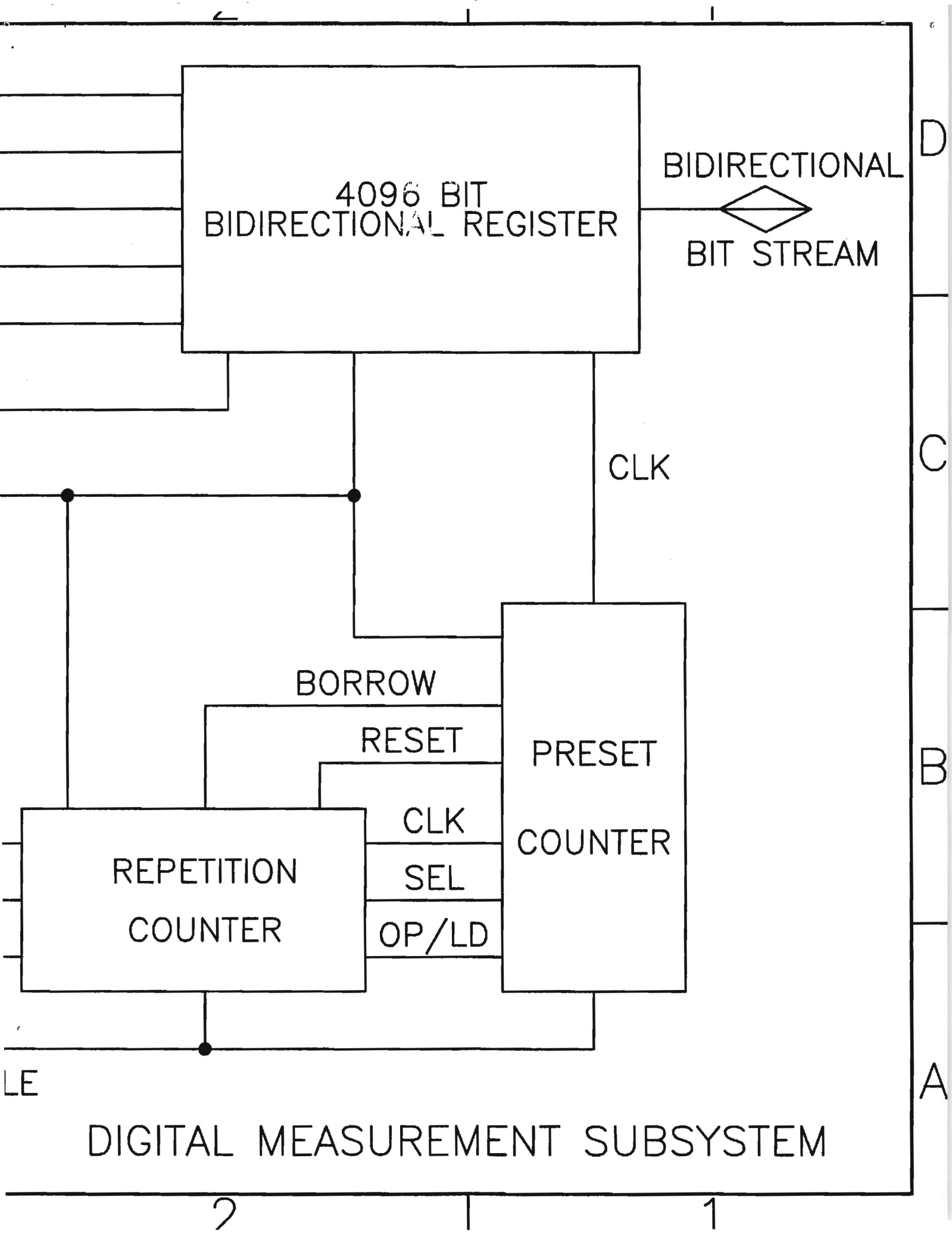

16-BIT DATA
CONTROL LINES
CS
CLOCK
INSTRUCTION DECODER AND CONTROL LOGIC (PART)
IN/OUT
ENABLE
S/P
R/W
CLEAR
ADDRESS
DATA
CLK
SELECT
OP/LOAD
CLOCK GENERATOR
ENA

FIGURE 3



DIGITAL MEASUREMENT SUBSYSTEM

E-21-640

Monthly Letter Report Nos. 7-9

LOCKHEED/GEORGIA TECH COOPERATIVE

VLSI PROGRAM

Purchase Order Number: Ca 31 303

Performance Period: 1 October to 30 November 1983

Submitted to:

Lockheed-Georgia Company
A Division of Lockheed Corporation
Marietta, Georgia 30063

by:

Georgia Tech Microelectronics Research Center
and
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

Contracting Through

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332

16 December 1983

Monthly Letter Report Nos. 8-9

This monthly letter report covers the period 1 October 1983 through 30 November 1983. Portions of the work done during this period were summarized in the presentation made by Lockheed and Ga. Tech personnel to Mr. Paul Losleben of DARPA. Only material not covered in that presentation will be presented here.

Most of the work done in this period was directed toward completing black-box level simulations of the analog measurement subsystem using the SPICE circuit analysis program. At this time, all components of the analog measurement subsystem except the high power output driver have been simulated as individual blocks. Work is underway to combine all the blocks into the complete system. When that is done, the entire analog measurement system will be modeled for all conditions of operation. Efforts have been made to obtain representative SPICE parameters for high current MOS devices from several manufacturers. If the needed quantities cannot be obtained in this way, it is planned to measure actual devices and use our MOSFIT analysis program to extract the model parameters. This will facilitate modeling of the high current output driver.

Since the analog subsystem relies upon operational amplifiers for its functioning, it is very important that we properly specify the characteristics of the amplifiers that will be eventually integrated in the PPE chip. In the initial black-box level simulation, we have been using a macromodel of the operational amplifier. Such a model takes data sheet type parameters as its input and simulates the device having those characteristics. If a particular macromodel gives a satisfactory simulation, then the properties of that macromodel define the device requirements for the circuit under simulation.

We have tested the macromodel concept by constructing a prototype programmable resistor circuit, measuring its performance and then simulating the circuit using the macromodel. The results of the test are presented in Figures 1-3. Figure 1 shows the test circuit, while Figs. 2 and 3 present the results of the measurements and simulations. Note that the agreement is very good even to predicting the asymmetries and "glitches" in the waveforms. Note that the input waveform is not shown on the oscilloscope photographs. Obviously, a 741-like opamp will not be used in the PPE; this simulation is only for the purpose of evaluating the macromodel concept.

The annual report will summarize all work done to the present as well as present additional background material.

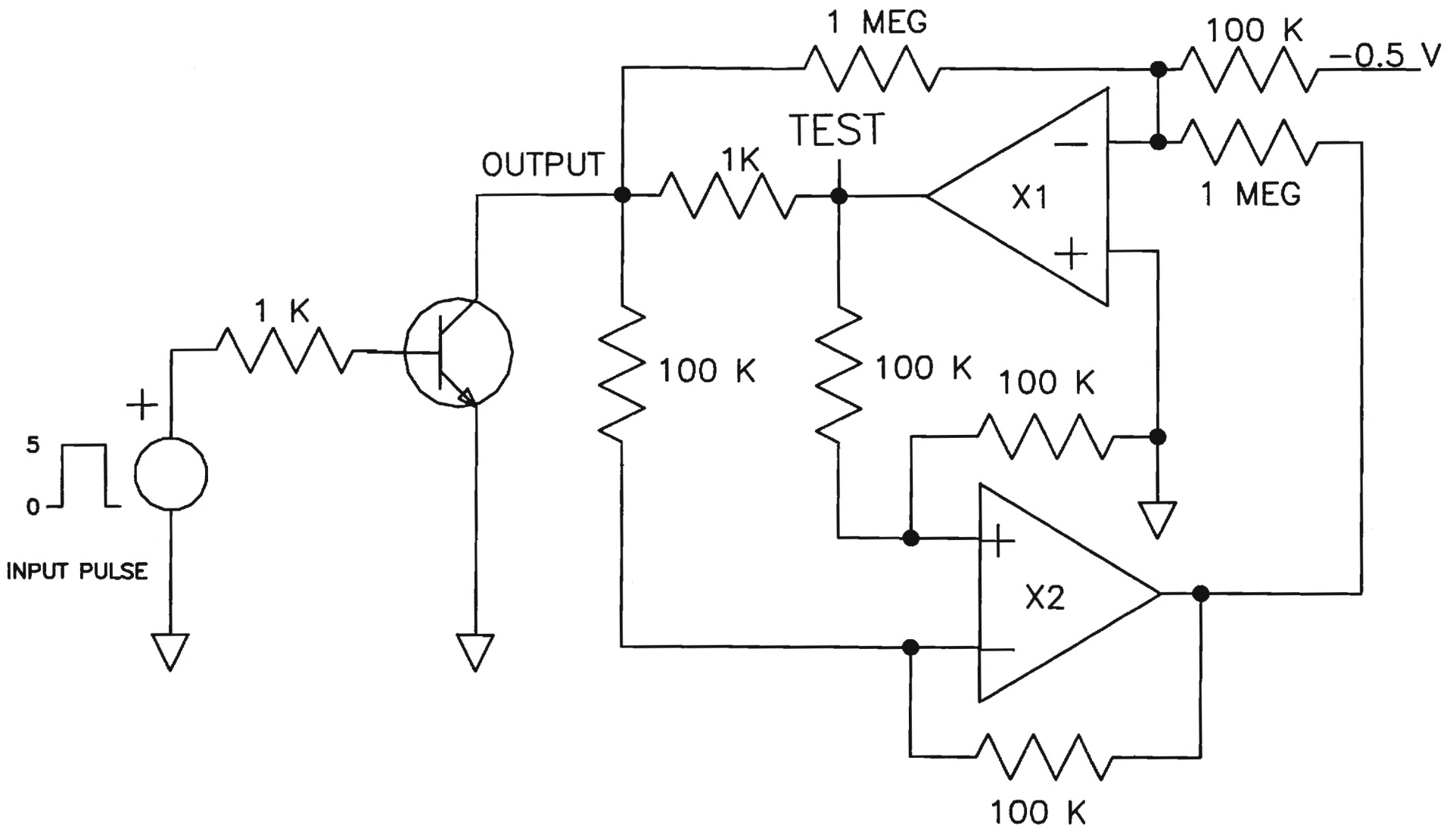
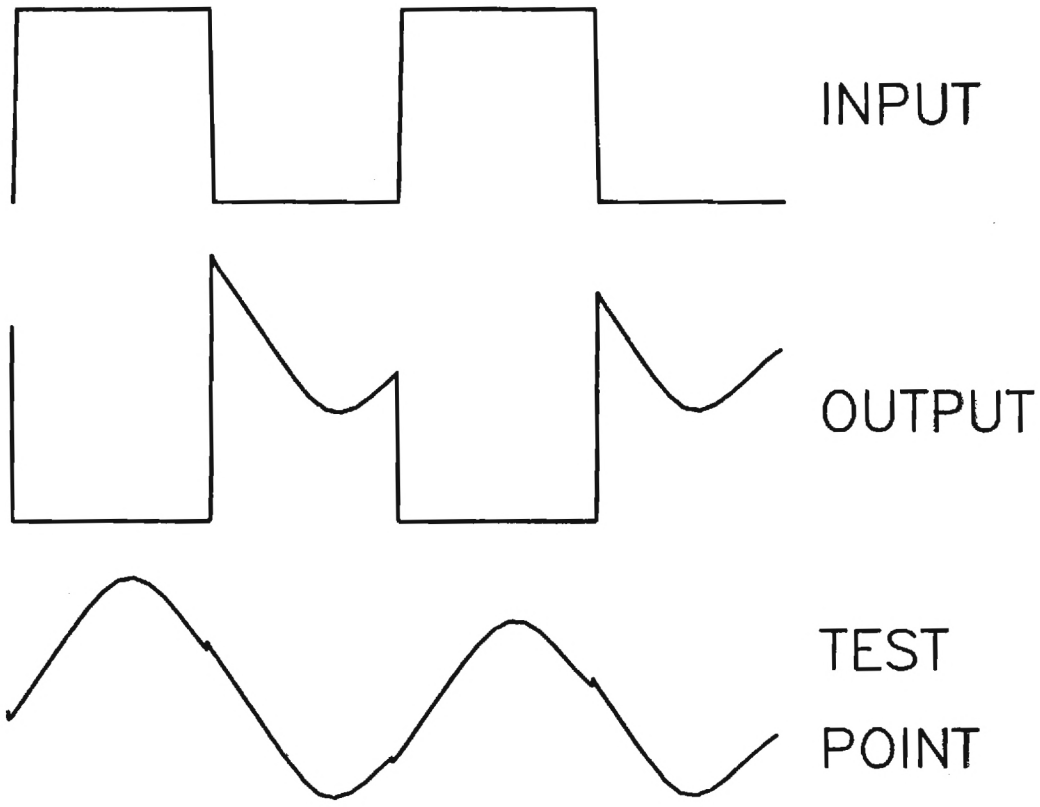
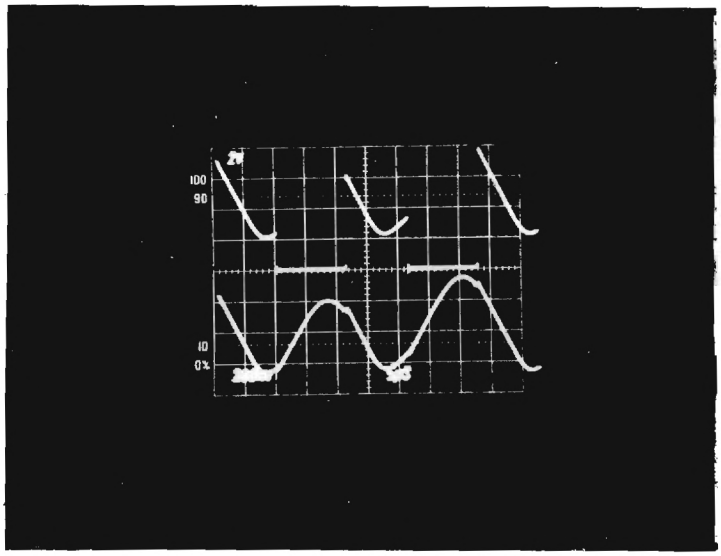


FIGURE 1

PROGRAMMABLE RESISTOR TRANSIENT RESPONSE TEST	
LOCKHEED/GEORGIA TECH	10/11/83
SCH_PROG_RES_P2	

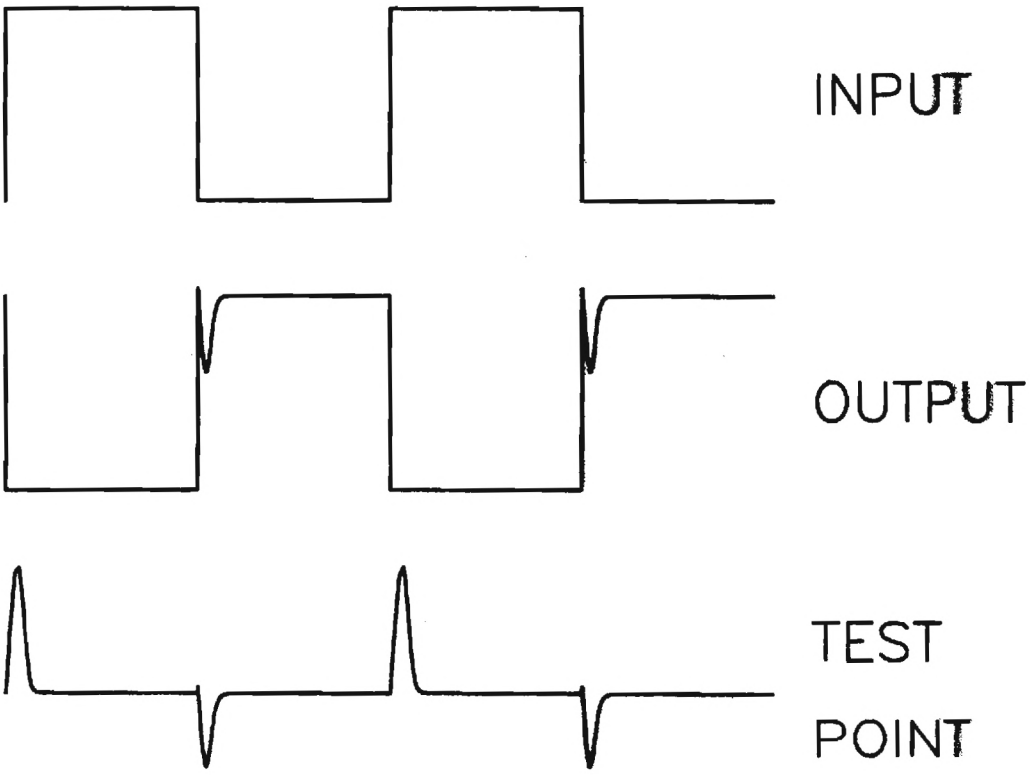


SIMULATED RESPONSE

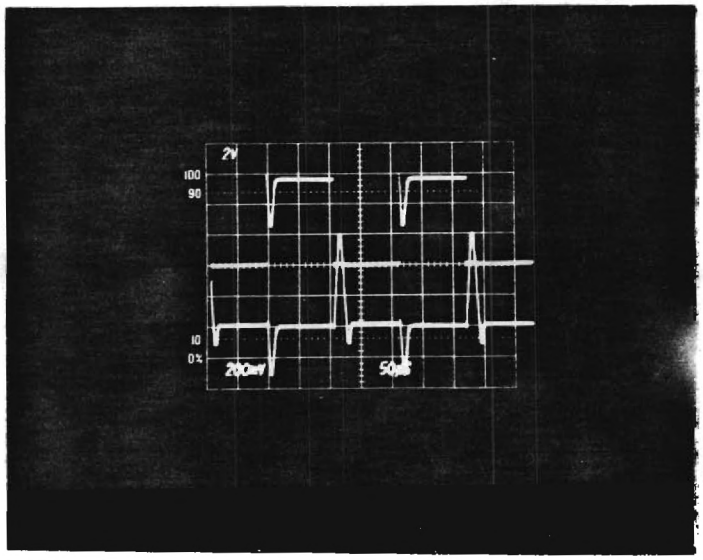


MEASURED RESPONSE

FIGURE 2. COMPARISON OF MEASURED AND CALCULATED RESPONSES TO 10 MICROSECOND PULSE.



SIMULATED RESPONSE



MEASURED RESPONSE

FIGURE 3. COMPARISON OF MEASURED AND CALCULATED RESPONSES TO 100 MICROSECOND PULSE.