ORGANIC-INORGANIC HYBRID THIN FILM TRANSISTORS AND ELECTRONIC CIRCUITS

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[This dissertation is dedicated to my wife, Myungeun, and my family in Korea for their love and endless support during my Ph. D. study.]

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Thin-film transistors (TFTs) capable of low-voltage and high-frequency operation will be required to reduce the power consumption of next generation electronic devices driven by microelectronic components such as inverters, ring oscillators, and backplane circuits for mobile displays. To produce high performance TFTs, transparent oxide-semiconductors are becoming an attractive alternative to hydrogenated amorphous silicon (*a*-Si:H)- and organic-based materials because of their high electron mobility values and low processing temperatures, making them compatible with flexible substrates and opening the potential for low production costs. Practical electronic devices are expected to use *p*- and *n*-channel TFT-based complementary inverters to operate with low power consumption, high gain values, and high and balanced noise margins. The *p*- and *n*-channel TFTs should yield comparable output characteristics despite differences in the materials used to achieve such performance. However, most oxide semiconductors are *n*-type, and the only high performance, oxide-based TFTs demonstrated so far are all *n*-channel, which prevents the realization of complementary metal–oxide–semiconductor (CMOS) technologies.

On the other hand, ambipolar TFTs are very attractive microelectronic devices because, unlike unipolar transistors, they operate independently of the polarity of the gate voltage. This intrinsic property of ambipolar TFTs has the potential to lead to new paradigms in the design of analog and digital circuits. To date, ambipolar TFTs and their circuits, such as inverters, have shown very limited performance when compared with that obtained in unipolar TFTs. For instance, the electron and hole mobilities typically found in ambipolar TFTs (ATFTs) are,

typically, at least an order of magnitude smaller than those found in unipolar TFTs. Furthermore, for a variety of circuits, ATFTs should provide balanced currents during *p*- and *n*-channel operations. Regardless of the selection of materials, achieving these basic transistor properties is a very challenging task with the use of current device geometries.

This dissertation presents research work performed on oxide TFTs, oxide TFT-based electronic circuits, organic-inorganic hybrid complementary inverters, organic-inorganic hybrid ambipolar TFTs, and ambipolar TFT-based complementary-like inverters in an attempt to overcome some of the current issues. The research performed first was to develop low-voltage and high-performance oxide TFTs, with an emphasis on *n*-channel oxide TFTs, using high-*k* and/or thin dielectrics as gate insulators. A high mobility electron transporting semiconductor, amorphous indium gallium zinc oxide (*a*-IGZO), was used as the *n*-channel active material. Such oxide TFTs were employed to demonstrate active matrix organic light emitting diode (AMOLED) display backplane circuits operating at low voltage.

Then, high-performance hybrid complementary inverters were developed using unipolar TFTs employing organic and inorganic semiconductors as *p*- and *n*-channel layers, respectively. An inorganic *a*-IGZO and pentacene, a widely used organic semiconductor, were used as the *n*- and *p*-channel semiconductors, respectively. By the integration of the *p*-channel organic and *n*-channel inorganic TFTs, high-gain complementary inverters with high and balanced noise margins were developed. A new approach to find the switching threshold voltage and the optimum value of the supply voltage to operate a complementary inverter was also proposed.

Furthermore, we proposed a co-planar channel geometry for the realization of high-performance ambipolar TFTs. Using non-overlapping horizontal channels of pentacene and *a*-

IGZO, we demonstrate hybrid organic-inorganic ambipolar TFTs with channels that show electrical properties comparable to those found in unipolar TFTs with the same channel aspect ratios. A key characteristic of this co-planar channel ambipolar TFT geometry is that the onset of ambipolar operation is mediated by a new operating regime where one of the channels can reach saturation while the other channel remains off. This allows these ambipolar TFTs to reach high on-off current ratios approaching 10^4. With the new design flexibility we demonstrated organic-inorganic hybrid ambipolar TFT-based complementary-like inverters, on rigid and flexible substrates, that show a significant improvement over the performance found in previously reported complementary-like inverters. From a materials perspective, this work shows that future breakthroughs in the performance of unipolar *n*-channel and *p*-channel semiconductors could be directly transposed into ambipolar transistors and circuits. Hence, we expect that this geometry will provide new strategies for the realization of high-performance ambipolar TFTs and novel ambipolar microelectronic circuits.

CHAPTER 1 INTRODUCTION

The primary goal of this work is to develop the technology to enable high performance complementary or complementary-like inverters based on thin-film transistors that are produced at low temperatures and are compatible with flexible substrates. These complementary technologies require developing high performance *p*-channel and *n*-channel transistors based on organic or oxide semiconducting materials. Chapter 1 provides an overview of thin-film transistors (TFTs) and oxide TFT-based TFTs. The properties of several multicomponent oxide semiconductors including zinc oxide (ZnO), indium zinc oxide (IZO), gallium zinc oxide (GZO) and indium gallium zinc oxide (IGZO) and the progress in the development of oxide TFTs are reviewed. Next, the progress of organic-inorganic hybrid complementary inverters is reviewed, and the challenges and the current issues during the development are listed. Then, the progress of all-organic or organic-inorganic hybrid ambipolar TFTs and ambipolar TFT-based inverters are reviewed, and the challenges and the current issues are also described. Finally, the objectives and the organization of the research dissertation are specified. Here, the motivation for the current research is described, and particular issues of interest related to the current research are identified.

1.1 Introduction: Thin-film transistors

In 1962, P. K. Weimer [1] fabricated the first *n*-type thin-film transistors (TFTs) employing a top gate staggered structure with microcrystalline CdS deposited by evaporation as the channel layer. Thermally evaporated silicon monoxide (SiO) and Au were used as the gate

dielectric and gate and source/drain electrodes, respectively. The TFTs exhibited field-effect mobility values of 1.1 cm^2/Vs and an on-off current ratio of 10. Since Weimer's work, TFTs based on various channel materials, including CdS, CdSe, and amorphous and polycrystalline silicon, have been developed. Currently, hydrogenated amorphous silicon (*a*-Si:H) based TFTs are commonly used as circuit components in active matrix liquid crystal displays (AMLCDs). Amorphous Si-based TFTs achieved field-effect mobility values of around 1.5 cm^2/Vs at a relatively high processing temperature of 300 ºC [2]. On the other hand, other classes of TFTs employ organic or oxide materials as the channel layers.

Organic or oxide TFTs are of great interest as a potential alternative to amorphous Si (*a*-Si) TFTs due to their low processing temperatures, which allows the use of flexible substrates. With remarkable progress in the synthesis and purification of organic semiconductors and processing of these materials into devices, the mobility of the best OFETs has surpassed that of *a*-Si TFTs [3]. In addition, organic TFTs can be processed at much lower temperatures using various simple, low-cost techniques, including vacuum thermal evaporation, spin-coating, vapor deposition, microcontact printing and screen printing. Compared to *a*-Si technology which provides only high performance *n*-channel TFTs, the versatility of synthetic organic chemistry enables the engineering of both *n*- and *p*-channel semiconductors, giving rise to many potential candidates for circuit designs based on CMOS technology. However, high mobility *n*-channel organic semiconductors typically have a high sensitivity to oxygen and moisture compared to their *p*-channel counterparts such as pentacene. Furthermore, the low work-function metals required for electron injection in *n*-channel TFTs are also reactive and oxidize instantly in air [4]. On the other hand, oxide semiconductors, such as ZnO and *a*-IGZO, show

better air stability and higher electron mobility. However, oxide-based TFTs so far provide only high-performance *n*-channel TFTs, which prevents the realization of complementary technologies. Therefore, organic-inorganic hybrid complementary structures comprised of *n*-channel oxide semiconductor and *p*-channel organic semiconductor channels could be potential candidates for complementary circuit design [5-8].

1.2 Review of progress in oxide TFTs and oxide TFT-based electronic circuits

Oxide semiconductors such as zinc oxide (ZnO) [9-12], zinc tin oxide (ZTO) [12-15], indium zinc oxide (IZO) [12, 16-20], indium gallium oxide (IGO) [21-23], indium oxide (In_2O_3) [10, 11, 24] and indium gallium zinc oxide (IGZO) [25-27] are an interesting class of materials for transparent electronic device applications because they often exhibit a high optical transparency (> 80%) in the visible spectra as a result of a large band gap (> 3.0 eV) and show high electron mobility values (> 10 cm^2/Vs). Among oxide semiconductors, ZnO [9, 28], IGZO [25, 29], and IZO [16-18, 30] are more attractive because they can be processed at low temperatures, making them compatible with flexible substrates and opening the potential for low production costs.

Fortunato *et al.* [9] fabricated transparent ZnO TFTs on ITO/glass substrates at room temperature, exhibiting a saturation mobility of about 20 cm^2/Vs, a threshold voltage of 21 V, a subthreshold slope of 1.24 V/decade, and an on-off current ratio of 2×10^5. More recently, Kang *et al*. [31] demonstrated ZnO-TFTs using high-*k* Mg-doped $B_{0.6}S_{0.4}TiO_3$ as a gate insulator on flexible PET substrate. This room temperature processed ZnO-TFTs exhibited a field effect mobility of 16.3 cm^2/Vs, an on-off current ratio of 6.4×10^4, a threshold voltage of 2.8 V, and a

subthreshold slope of 0.4 V/decade at a voltage of below 7V. However, ZnO films are polycrystalline even when deposited at low temperature. This may lead to channels with grain boundaries that deteriorate the TFT mechanical stability, uniformity, and performance of its electrical characteristics [32]. On the other hand, IGZO and IZO films deposited by physical vapor deposition or rf-magnetron sputtering at room temperatures show amorphous nature and still achieve high electron mobility values (> 10 cm^2/Vs) [17, 18, 25, 29]. The amorphous structure of the IGZO films is stable up to 500°C in air [33]. For this reason, IGZO and IZO are particularly attractive for microelectronic circuits on flexible substrates.

In 2004, Nomura *et al.* [25] first demonstrated transparent and flexible amorphous IGZO (*a*-IGZO) TFTs ($InGaZnO_4$) processed at room temperature and using a Y_2O_3 gate insulator on 200 μm-thick polyethylene terephthalate substrates. This TFT showed a channel mobility of 8 cm^2/Vs, a threshold voltage of 1.6 V, and an on-off current ratio of 10^3, respectively. In 2006, Yabuta *et al.* [29] demonstrated improved *a*-IGZO ($InGaZnO_4$) TFTs with a channel mobility value of 12 cm^2/Vs, a low threshold voltage value of 1 V, and a high on-off current ratio of 10^8. The IGZO and Y_2O_3 used as channel and insulator layers in this TFT, respectively, were deposited by rf magnetron sputtering without intentional substrate heating at low processing temperature (< 140 ºC). In 2007, Fortunato *et al.* [17] demonstrated transparent IZO TFTs processed at room temperature with the use of amorphous binary In_2O_3-ZnO oxides used simultaneously as an active channel layer and as source/drain electrodes. The oxide layers were deposited by rf sputtering on the ATO (Al_2O_3-TiO_2)/ITO/glass substrates. The TFTs exhibited saturation mobility higher than 100 cm^2/Vs, a threshold voltage lower than 6 V, a subthreshold slope of 0.8 V/decade, and an on-off current ratio of 10^7.

Oxide TFT-based electronics is now approaching commercialization in display applications. Ito *et al.* [34] fabricated 4-inch VGA IGZO TFT-based pixel array on glass with an electrophoretic display, used in an electronic paper application. In 2009, Jeong *et al.* [35] demonstrated a full-color 12.1 inch WXGA active matrix organic light-emitting diode (AMOLED) display using *a*-IGZO TFTs as an active backplane. The *n*-channel *a*-IGZO TFTs exhibited a field-effect mobility of 17 cm^2/Vs, a threshold voltage of 1.1 V, an on-off current ratio > 10^9, and a subthreshold slope of 0.28 V/decade.

In addition, other electronic components (inverters and ring oscillators) based on oxide-TFTs have also been demonstrated. In 2007, Ofuji *et al.* [36] fabricated five-stage ring oscillators using 10-μm channel-length *a*-IGZO TFTs with an oscillation frequency of 410 kHz and a propagation delay of 240 ns per stage at a supply voltage of 18 V. The discrete TFTs exhibited a channel mobility and threshold voltage of ~ 3 cm^2/Vs and 7 V, respectively. In 2008, Sun *et al.* [37] have demonstrated ring oscillators using ZnO films deposited by atomic layer deposition process at a temperature of 200 °C. Discrete TFTs exhibited field-effect mobility values of > 15cm^2/Vs. Seven-stage ring oscillators operated at a frequency as high as 2.3 MHz at supply voltages of 25 V, corresponding to a propagation delay of 31 ns per stage.

However, to date, most high mobility oxide semiconductors are *n*-type. Charge mobility of *n*-type oxide semiconductors is much larger than that of *p*-type because their electron transport paths, the conduction band minima, are made mainly of spatially spread *s* orbitals of metal cations. On the other hand, the hole transport paths, the valance band maxima, are made mainly of rather localized O 2*p* orbitals, which leads to the low hole mobility due to hopping conduction. Currently, *p*-channel oxide semiconductors that match the electrical properties and

low processing temperatures of their *n*-channel counterparts are proving difficult to realize[25][38]. Therefore, oxide-based TFTs so far provide only high performance *n*-channel TFTs, which prevents the realization of complementary metal–oxide–semiconductor (CMOS) technologies.

1.3. Review of progress in organic-inorganic hybrid complementary circuits

Recently organic TFT-based electronic components such as inverters and logic circuits have attracted much attention because they have the potential of low-temperature and large-area microelectronic circuit applications on glass or flexible substrates. Practical complementary electronic devices require both *p*- and *n*-channel TFTs. Complementary inverters are preferred compared to only *n*- or *p*-channel inverters because they allow low power consumption, higher gain, and low noise margin. Currently reported complementary inverters on glass or flexible substrates are mostly composed of organic TFTs for both *p*-channel and *n*-channel [39-44]. Relatively large electron mobility values up to 6 cm^2/Vs [44-46] using C_{60} as active channels have been reported in *n*-channel organic TFTs. However, compared to their *p*-channel counterparts *n*-channel organic semiconductors typically have high sensitivity to oxygen and moisture. Furthermore, the low work-function metals, required for electron injection in *n*-channel TFTs, are also reactive and oxidize instantly in air [4]. In contrast, *n*-channel oxide semiconductors, such as ZnO and *a*-IGZO, are attractive due to their better air stability and higher electron mobility values. As described previously, it is hard to achieve high mobility *p*-channel oxide TFTs. Therefore, *p*-type organics are a better alternative due to their relatively large hole mobility values [47] and better stability in air [4,

48-50]. Among organic semiconductors pentacene, with hole mobility values of 0.1 ~ 1 cm^2/Vs, has been the material of choice to realize *p*-type TFTs. Hybrid organic-inorganic complementary structures comprising *n*-channel oxide semiconductor and *p*-channel organic semiconductor channels are then potential candidates for circuit design based on CMOS technology.

However, only a few groups have reported hybrid complementary circuits [5-8]. In 2007, pentacene- and ZnO-based hybrid complementary inverters using 200 nm-thick AlO_X gate dielectrics processed at low temperature below 100 ºC on glass substrate were first demonstrated by Oh *et al* [5]. Since the *p*-channel TFT showed field-effect mobility and threshold voltage of 0.11 cm^2/Vs and -1.1 V compared with those of the *n*-channel device (0.75 cm^2/Vs and 1.45 V), the hybrid inverters exhibited a transition voltage (V_M) of ~ 3 V and a DC gain of 21 at a voltage of 7 V. A short time later, Oh *et al.* [51] demonstrated complementary inverters on flexible polyethersulfone (PES) substrates using *n*-ZnO and *p*-pentacene channels, showing a high DC gain of ~ 100 and comparable *n*- and *p*-channel saturation mobilities of 0.9 and 0.4 cm^2/Vs, respectively, at a voltage of 7 V. However, since the ZnO film was deposited on nonstoichiometric AlO_X by rf sputtering, the current voltage characteristics of the ZnO-TFT showed large hysteresis, resulting significant initial threshold voltage variations from 0.1 to 4.0 V after 4 runs. Furthermore, ZnO films are polycrystalline even when deposited at room temperature [32], leading to channels with grain boundaries that deteriorate the TFT stability, uniformity, and performance as described in previous section.

1.4 Review of progress in ambipolar TFTs and complementary-like circuits

Complementary circuits based on ambipolar TFTs are also attracting a great interest for integrating CMOS-like logic gates such as NOR or NAND gates, adders, and multipliers [52]. Different from unipolar inverters operating in only one quadrant regime, ambipolar inverters allow operations in both the first and third quadrant regimes independently of the sign of the gate voltage, which is a unique feature of employing ambipolar TFTs [53, 54]. Therefore, they can simplify CMOS circuit design by reducing the number of control lines and enabling multifunctional circuits [52].

All-organic or organic-inorganic ambipolar TFTs have been realized following different material approaches that can be categorized into three major groups [55, 56] with respect to their semiconductor layers;

- Pure semiconductors [54]
- Blends of n- and p-type semiconductors [53]
- Bilayer of n- and p- channel semiconductors [57]

The main challenge for the realization of ambipolar transistors using a pure or blended semiconductor as a channel layer relates to achieving efficient charge injection of hole and electrons into the semiconductor. Pure organic semiconductors with ambipolar transport can be observed, provided that the barrier for electron injection is reduced by choosing low-work function metals as electrode material [58, 59] or employing small bandgap semiconductors [40, 56, 60, 61]. However, achieving balanced electron and hole injection, and subsequently balanced transport characteristics has proved a challenging enterprise [55].

Furthermore, transport in organic semiconductors is particularly susceptible to energetic and/or positional disorder at the bulk and at the critical interfaces of a TFT [53, 56, 62]. In the work by Meijer *et al*. [53] poly(2-methoxy-5-(3,7-dimetnyloctyloxy))-p-phenylene vinylene) (OC1C10-PPV), a *p*-channel semiconductor, and [6,6]-phenyl-C61-butyric acid methylester (PCBM), an *n*-channel semiconductor, showed mobility values of about 10^{-2} cm^2/Vs when each was used as an unipolar transistor. However, with a mixture of OC1C10-PPV and PCBM, maximum ambipolar carrier mobilities were on the order of 10^{-5} cm^2/Vs (for both electrons and holes) for narrow band gap based polymeric organic TFTs, and 10^{-5} cm^2/Vs (electron) and 10^{-3} cm^2/Vs (hole) for organic TFTs based on polymer-small molecule interpenetrating networks. Dodabalapur *et al.* [62] have observed that the electron mobility in ambipolar TFTs employing an organic heterostructure of C_{60}/α-6T is decreased by a factor of 16 compared to pristine C_{60} organic TFTs. Preserving the relatively large mobilities obtained in unipolar TFTs is important to produce ambipolar TFTs with high on-off current ratios and complementary circuits operating at high frequencies.

In blended or vertically integrated bilayer ambipolar TFTs, the large surface area introduced by the *pn*-heterojunction, tends to result in much lower mobility values than in unipolar devices, and most likely leads to charge trapping and contact resistance effects which up-to-date have been less studied in ambipolar TFTs than in their unipolar counterparts.

Inverters based on all organic [40, 53, 54, 61, 63-67] or organic-inorganic hybrid [68] ambipolar TFTs have been demonstrated. In 2004, Anthopoulos *et al*. demonstrated complementary-like inverters comprised of two identical ambipolar TFTs based on solution processable methanofullerene [6,6]-phenyl-C61-butyric acid methylester (PCBM), exhibiting a

DC gain of 20 V/V at an operating voltage of 60 V. However, in the *p*-channel regime transistor operation is severely contact limited due to the presence of a large injection barrier for holes at the Au/PCBM interface. Anthopoulos *et al.* [40] also demonstrated air stable complementary-like circuits, such as inverters and ring oscillators, using ambipolar TFTs based on a nickel dithiolene derivative. In these derivatives, the electron and hole mobilities are on the order of 10^{-4} cm^2/Vs with the highest value of around 10^{-3} cm^2/Vs at a voltage of 30 V. The switching speed of their complementary circuits was limited by their low carrier mobilities, which leads high power dissipations with large operation voltages.

In 2006, Wang *et al*. [69] fabricated a bottom-contact organic TFT and inverter based on a heterostructure of C_{60} on pentacene, showing relatively large electron and hole mobilities of 0.23 and 0.14 cm^2/Vs, respectively, at a voltage of 100 V. However, in an air environment the *n*-channel C_{60} is completely degraded whereas the *p*-channel pentacene keeps working. In addition, the mismatch between the lowest unoccupied molecular orbital (LUMO) level of C_{60} and the highest occupied molecular orbital (HOMO) level of pentacene creates a barrier for electron injection from pentacene to C_{60}, leading to a non-linear increase of drain current at low drain voltages.

In 2007, hybrid ambipolar TFTs employing organic-inorganic hybrid heterostructures were first demonstrated by Nakanotani et al. [70] using the air-stable and high mobility *n*-channel IZO semiconductor and a *p*-channel semiconductor pentacene. These TFTs were fabricated with a bilayer geometry on silicon wafer. The mismatch between hole (0.14 cm^2/Vs) and electron mobilities (13.8 cm^2/Vs) in this ambipolar TFTs vertically integrated were large, which led to unbalanced *on*-current characteristic. In 2008, Pal *et al.* [71] obtained balanced *on*-

currents in hybrid ambipolar TFTs employing solution processed ZnO *n*-channel and pentacene *p*-channel semiconductors with comparable hole and electron mobilities of 6.33×10^{-3} and 7.58×10^{-3} cm^2/Vs, respectively. However, the switching performance of the TFTs was limited by the low mobilities and low on-off current ratio, around 10^2. A short time later, Dhananjay *et al.* [68] demonstrated complementary inverters using two identical ambipolar TFTs employing a bilayer of In_2O_3 and pentacene vertically distributed, showing a dc gain of 10 V/V. Again, while these ambipolar TFTs exhibited balanced electron and hole transport, the low field-effect mobilities of 0.07 and 0.02 cm^2/Vs for *n*- and *p*-channels, respectively, limited the inverter performance.

Therefore, achieving balanced large *on*-currents using all organic or organic-inorganic hybrid semiconductors in vertically distributed ambipolar TFTs and complementary circuits is still challenging due to either unmatched or low mobilities.

1.5 Objectives and organization of the dissertation

The first objective is to develop low-voltage and high-performance oxide TFTs suitable for AMOLED display backplane applications. The second objective is to develop high-performance organic-inorganic hybrid complementary inverter compatible with flexible substrates using unipolar TFTs employing organic and inorganic semiconductors as *p*- and *n*-channel layers, respectively. The third objective is to develop high-performance organic-inorganic hybrid ambipolar TFTs and complementary-like inverters compatible with flexible substrates using two identical ambipolar TFTs employing organic and inorganic *p*- and *n*-channel layers, respectively.

According to the objectives outlined above, the organization of the dissertation is structured as follows. Chapter 2 introduces experimental details and methods regarding device structure and operation, device fabrication, and electrical characterization and testing in the area of TFTs. Chapter 3 presents the results pertinent to the development of high performance oxide semiconductor *n*-channel TFTs operating at low-voltage using amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ and Al_2O_3 gate dielectrics. The effects of the dielectric properties on device performance and stability as well as channel and contact resistances are presented. The fabrication and operation of an AMOLED circuit operating at low voltage is also described in this chapter. Chapter 4 describes the development of flexible organic-inorganic hybrid complementary inverters with high gains and high and balanced noise margins using *p*-channel pentacene and *n*-channel amorphous InGaZnO (*a*-IGZO) semiconductors. A new method to find the switching threshold voltage and the optimum supply voltage of complementary inverters is also presented in this chapter. Chapter 5 describes a co-planar channel geometry for the realization of high-performance ambipolar TFTs. A generalized description of the operation of ambipolar transistors is presented and the realization of high performance complementary-like inverters in rigid and flexible substrates is also described. Chapter 6 summarizes the conclusions drawn from these studies and presents recommendations for future work.

CHAPTER 2 TFT FABRICATION AND CHARACTERIZATION

This chapter provides a detailed description of the theory and experimental methods used to characterize oxide or organic thin film transistors (TFTs). It starts with the illustration of device structures and operation, followed by its electrical characterization. The operation of TFTs with an *n*-channel oxide semiconductor is systematically analyzed and illustrated. The current-voltage characteristics and the extraction of electrical performance in the linear and saturation regimes of TFTs are explained and the analytical method for evaluating contact resistance is introduced. The thin film processing steps involved in the fabrication of oxide TFT are presented, including the deposition and patterning of metal electrodes, dielectrics, and semiconductors. The deposition methods followed for the fabrication of organic TFTs are also presented. The last section of this chapter describes the experimental setup for the electrical characterization.

2.1 Device structures and operation of thin-film transistors

2.1.1 Device structures of TFTs

Four possible TFT device structures, determined by the position of the gate, source, and drain contacts relative to the organic semiconductor film, are shown in Fig. 2.1 [72]. The basic structures are either coplanar or staggered. In a staggered structure, also called top-contact structure, the gate contact is on the opposite side of the semiconductor film from the source and drain contacts, as shown in Figure 2.1(a) and (c). In such an arrangement, the source-drain contacts are in direct contact with the induced channel. In a coplanar structure, also called

bottom-contact structure, the gate, source, and drain contacts are all located on the same side of the semiconductor film, as shown in Figure 2.1(b) and (d).

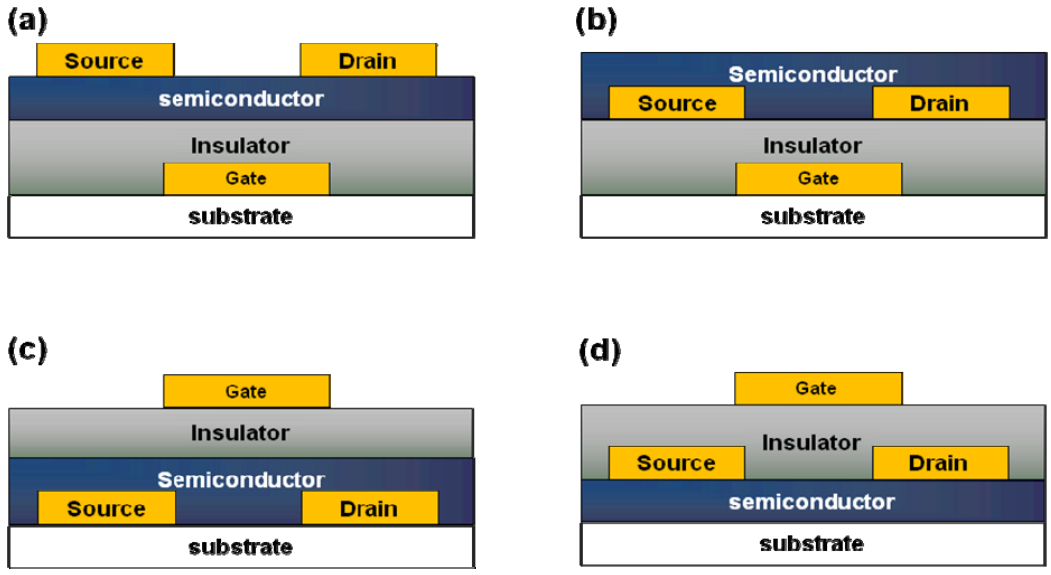

Figure 2.1: Cross-sections of simplified TFT device configurations: (a) Bottom-gate staggered structure (top-contact); (b) Bottom-gate coplanar structure (bottom-contact); (c) Top-gate staggered structure; (d) Top-gate coplanar structure.

In addition to coplanar and staggered configurations, TFTs can be classified as either bottom-gate or top-gate devices. A bottom-gate TFT, which is sometimes referred to as an inverted TFT, has the gate insulator and gate electrode located beneath the semiconductor, as shown in Figs. 2.1(a) and 2.1(b). A top-gate TFT, as shown in Figs. 2.1(c) and 2.1(d), has the gate and insulator located on top of the semiconductor. Therefore, there are four basic device configurations based on the definitions above as summarized in Figure 2.1: (a) bottom-gate coplanar structure, (b) bottom-gate staggered structure, (c) top-gate coplanar structure, and (d)

top-gate staggered structure. In the coplanar structure, the TFTs generally suffer from large contact resistance between source/drain and semiconductor, which can limit the TFTs to operate at high frequency. However, in the staggered structure, the contact resistance can be reduced due to the large contact area. In the top-gate structure, the semiconductor is covered by a gate insulator so that the property of the semiconductor can be degraded during the deposition process of the gate dielectric and the top electrodes, and the film growth can be disturbed at the interface of semiconductor/metal contact. In this work, we used an inverted-staggered (bottom gate top source/drain contact) structure for the fabrication of TFTs as shown in Fig. 2.1.

2.1.2 Device operation of *n*-channel TFTs

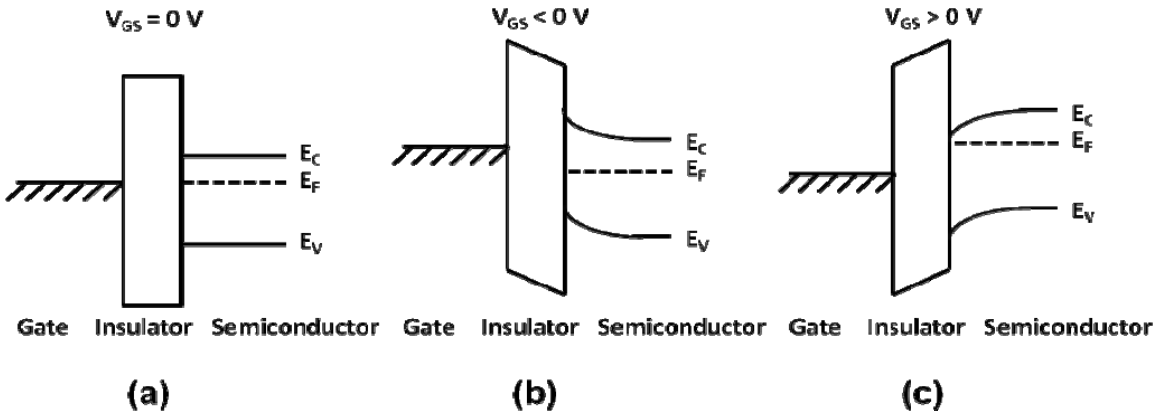

Figure 2.2: Energy band diagrams of a bottom gate top contact oxide TFT as viewed through the gate for several biasing conditions: (a) equilibrium, (b) $V_{GS} < 0$ V, and (c) $V_{GS} > 0$ V.

The basic operation of an *n*-channel TFT can be explained using a coplanar structure as shown in Figure 2.1(b) and (d). Different from metal oxide semiconductor field-effect transistor (MOSFET) operations using an inversion-mode, organic or oxide semiconductor TFTs are operated in accumulation-mode [73, 74]. Figure 2.2 shows several energy band diagrams as viewed through the gate of an *n*-channel TFT operating in such mode. For simplicity, hereafter the operation of TFTs will be reviewed by assuming an oxide semiconductor channel. A similar description applies to the case of TFTs that use organic semiconductors.

An oxide TFT device can be considered as two capacitor plates separated by an insulator between source/drain contacts and gate contact. To better understand how an oxide TFT works, we can analyze the energy band diagrams of a metal insulator semiconductor (MIS) structure based on two different modes with an *n*-channel oxide semiconductor. Figure 2.2(a) shows an energy band diagram of the device in equilibrium, with 0 V applied to the source, drain, and gate. Figure 2.2(b) shows an energy band diagram with the gate negatively biased. The applied negative bias repels mobile electrons from the semiconductor, leaving a depletion region near the insulator-semiconductor interface. When compared to Fig. 2.2(a), this biasing condition has a reduced conductance due to the reduced number of mobile electrons in the semiconductor. Figure 2.2(c) shows an energy band diagram with the gate positively biased. The applied positive bias attracts mobile electrons, forming an accumulation region near the insulator-semiconductor interface. These excess mobile electrons lead to an increase in the conductance.

2.1.3 Current voltage characteristics of *n*-channel TFTs

The TFT electrical characteristics are based on gradual channel approximation [73, 75-78], where x is the direction perpendicular to the channel and y is parallel to the channel, and the carrier density per unit area in the channel depends on y, which means that the channel formation depends on the potential $V(y)$ caused by the drain potential V_D as shown in Figure 2.3. The gate-to-source voltage (V_{GS}) and the drain-to-source voltage (V_{DS}) are the external parameters controlling the drain (channel) current I_{DS}. The gate-to-source voltage is set to be larger than the threshold voltage V_T to create carriers in the semiconducting channel layer between the source and drain. The y-coordinate origin (y=0) is at the source end of the channel. The channel voltage with respect to the source will be denoted by $V(y)$. Now assume that the threshold voltage V_T is constant along the entire channel region, between y=0 and y=L. In reality, the threshold voltage changes along the channel since the channel voltage is not constant. Next, assume that the electric field component E_y along the y-coordinate is dominant compared to the electric field component E_x along the x-coordinate. This assumption will allow us to reduce the current-flow problem in the channel to the y-dimension only. Note that the boundary conditions for the channel voltage $V(y)$ are as follow.

$$V(y=0) = V_S = 0$$
$$V(y=L) = V_{DS} \qquad \text{Eq. (2-1)}$$

Also, it is assumed that the entire channel region between the source and the drain is accumulated, i.e.,

$$V_{GS} \geq V_T$$
$$V_{GD} = V_{GS} - V_{DS} \geq V_T \qquad \text{Eq. (2-2)}$$

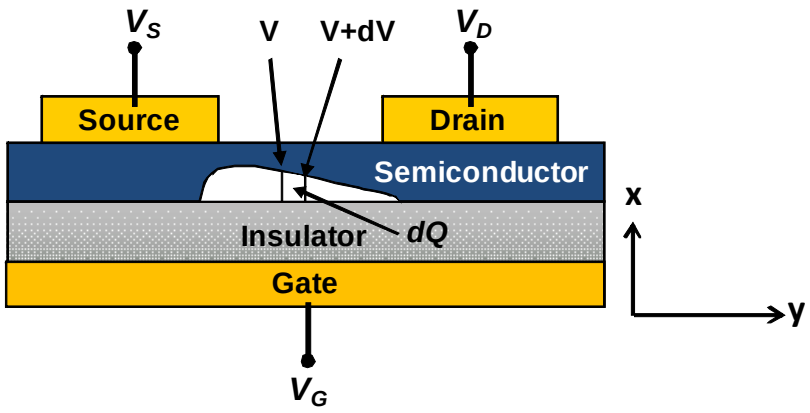

Figure 2.3: Cross-sectional view of the channel region of oxide TFT used to derive the gradual channel approximation.

When the gate potential (V_G) is higher than the threshold voltage (V_T), the charge density Q in the channel is related with the gate potential V_{GS} via

$$Q = -C_i\left(V_{GS} - V_T\right) \qquad \text{Eq. (2-3)}$$

where C_i is the capacitance per unit area of the gate insulator. In Eq. (2-3) the channel potential V_C is assumed to be zero.

Let $Q_I(y)$ be the total mobile electron charge in the surface accumulation layer. The charge can be expressed as a function of the gate-to-source voltage V_{GS} and of the channel voltage $V_C(y)$ as follows:

$$Q = -C_i\left(V_{GS} - V_T - V_C(y)\right) \qquad \text{Eq. (2-4)}$$

Note that the incremental resistance dR of the differential channel segment dy and the corresponding differential charge is dQ. Assuming that all mobile electrons in the accumulation layer have a constant mobility, the incremental resistance can be expressed as follows:

$$dR = -\frac{dy}{W\mu Q_I(y)}dy \qquad \text{Eq. (2-5)}$$

where W is the channel width, μ is the field-effect mobility, and E_y is the electric field at y.

Note that the minus sign is due to the negative polarity of the accumulation layer charge Q_I. We will assume that the channel current density is uniform across the segment. According to one-dimentional model, the channel (drain-to-source) current, I_{DS}, flows between the source and drain regions in the y-coordinate direction. Applying Ohm's law for this segment yields the voltage drop along the incremental segment dy in the y-direction:

$$dV_C = I_{DS}dR = -\frac{I_{DS}}{W\mu Q_I(y)}dy \qquad \text{Eq. (2-6)}$$

The equation can now be integrated along the channel from y=0 to y=L, using the boundary conditions given in Eq. (2-1).

$$\int_0^L I_{DS}dy = -W\mu\int_0^{V_{DS}} Q_I(y)dV_C \qquad \text{Eq. (2-7)}$$

The left-hand side of this equation is simply equal to $I_{DS}L$. The integral on the right-hand side is evaluated by replacing $Q_I(y)$ with Eq. (2-5). Thus,

$$I_{DS}L = WC_i\mu\int_0^{V_{DS}} (V_{GS} - V_T - V_C)dV_C \qquad \text{Eq. (2-8)}$$

Assuming that the channel voltage V_C is the only variable in Eq. (2-7) that depends on the position y, the drain current is as follows:

$$I_{DS} = \frac{WC_i\mu}{L}((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2})) \qquad \text{Eq. (2-9)}$$

In the linear region ($V_{DS} \ll V_{GS}$) the drain current can be written as

$$I_{DS} = \frac{WC_i\mu}{L}(V_{GS} - V_T)V_{DS} \qquad \text{Eq. (2-10)}$$

The gate field-induced carrier density at the drain disappears as the drain potential increases. Eventually, when $V_{DS} = V_{GS} - V_T$, the channel becomes completely pinched off, and the drain current saturates. For the saturation region ($V_{DS} > V_{GS} - V_T$), Eq. (2-9) is no longer valid. The saturation drain current can be obtained by substitution of $V_D = V_G - V_T$ into Eq. (2-9), yielding

$$I_{DS} = \frac{WC_i\mu}{2L}(V_{GS} - V_T)^2 \qquad \text{Eq. (2-11)}$$

The gradual channel approximation assumes that the field-effect mobility is independent of the gate voltage and that the source/drain contacts have a negligible resistance [73, 75, 76]. Therefore, the expression above does not account for the non-linear behavior of drain current at low drain bias generally observed in organic or oxide TFTs due to resistive contacts.

2.2 Device characterization of *n*-channel TFTs

2.2.1 Device structure and operation

In this work, TFTs employ common or patterned bottom-gate and top-source/drain contact device architectures, whereby the source and drain electrodes are deposited on top of the semiconductors, as shown in Figure 2.4(a) and (b).

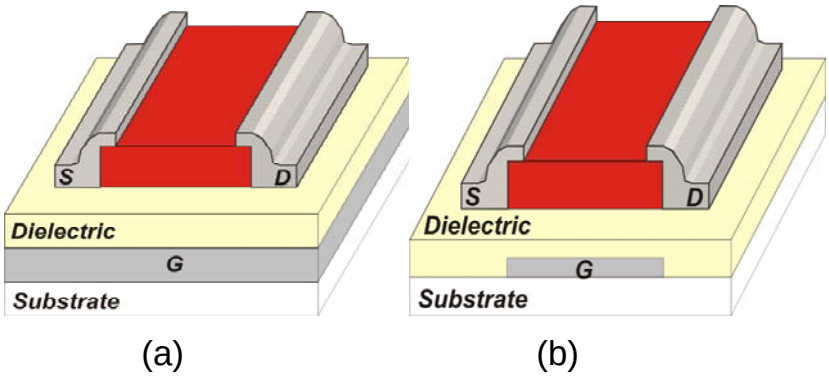

Figure 2.4: Device diagrams of bottom-gate top-contact TFTs: common bottom-gate (a) and patterned bottom-gate (b).

Oxide or organic TFTs differ from MOSFETs in their mode of operation: MOSFETs operate in the depletion or inversion mode, while oxide and organic [4, 74] TFTs generally operate in the accumulation mode [79, 80]. Since most oxide TFTs exhibit an *n*-channel behavior within an *n*-channel oxide semiconductor, the following section will focus on the operation of oxide TFTs with *n*-channel oxide semiconductor in the accumulation mode. Figure 2.5 shows the mobile carrier distributions and output characteristics of a bottom-gate and top-contact *n*-channel TFT structure under different operating conditions. In the channel layer of the TFT structures, "-" symbols represent negative mobile carriers which upon applying a gate voltage, are accumulated between the dielectric and the channel layer in the semiconductor (localized positive counter ions are not shown here for simplicity).

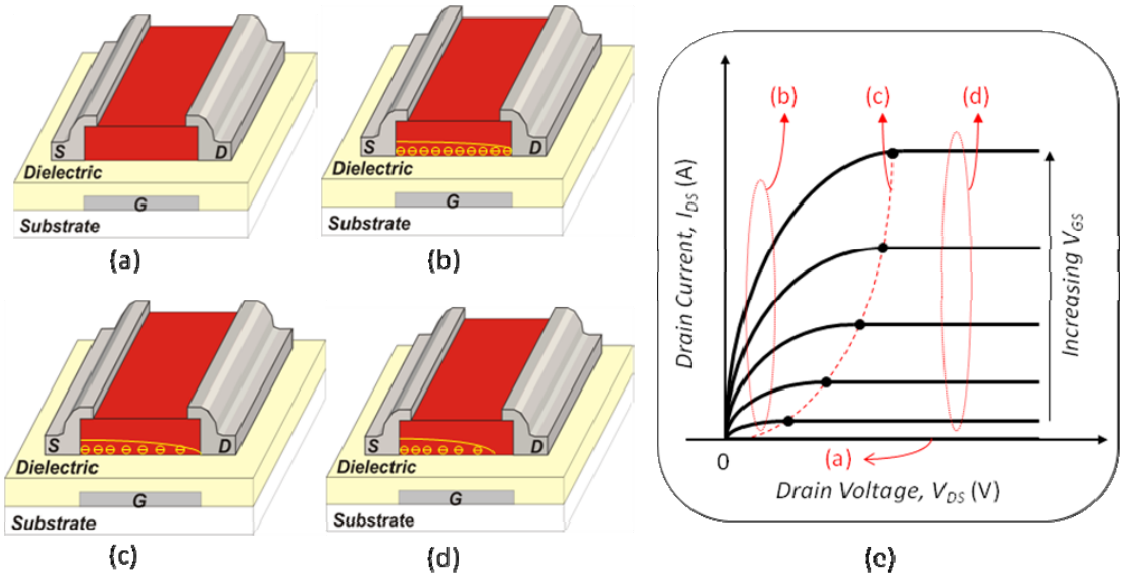

Figure 2.5: Charge carrier distributions ((a) off region (b) linear region (c) pinch off points (d) saturation region) and corresponding output characteristics (e) in a bottom-gate top-contact oxide TFT.

When the gate voltage is below the threshold voltage ($V_{GS} < V_T$), there is no accumulation of electrons between the source and drain as shown in Figure 2.5(a). The channel resistance can be considered infinite and the drain current is negligible. This operation mode is called the "off-region", which corresponds to the region (a) in Figure 2.5(e). When the drain current in the off region is high, it is referred to as leakage current, of which there are two types: source-drain leakage and gate leakage. Source-drain leakage in a TFT is strongly affected by the thickness of the intrinsic semiconductor layer. Gate leakage refers to any current which flows through the gate electrode. It is primarily determined by the quality of the gate dielectric layer.

As the gate voltage is increased beyond the threshold voltage ($V_{GS} > V_T$), a positive gate voltage will attract electrons to the interface between the gate dielectric and the active

semiconductor layer, forming a highly conductive accumulation layer as shown in Figure 2.5(b). If a small voltage ($V_{DS} < V_{GS}$-V_T) is applied across the source-drain contacts, electrons, assisted by the electric field, enter the accumulation layer and drift through the channel. This operation mode is called the "linear region", which is corresponding to the region (b) in Figure 2.5(e). As the value of the drain-source voltage is further increased, the electrons at the drain are depleted and the conducting channel disappears as shown in Figure 2.5(c). This happens when $V_{DS} = V_{GS}$-V_T, which is called the "pinch-off point", which corresponds to region (c) in Figure 2(e). Beyond the pinch-off point ($V_{DS} < V_{GS}$-V_T), a depleted surface region form adjacent to the drain, and this depletion region grows toward the source with increasing drain voltages as shown in Figure 2.5(d). This operation mode is called the "saturation region", which corresponds to the region (d) in Figure 2.5(e).

2.2.2 Extraction of performance parameters

Using an *n*-channel oxide semiconductor as an example, *n*-channel TFT operation can be described using a square-law model developed from MOSFET [77, 78]. The regions are usually determined by the values of applied voltages V_{GS} and V_{DS} in the MOSFET modeling. As described in Section 2.2.1, the device is operated in the linear regime for $V_{DS} < V_{GS} - V_T$ and is operated in the saturation regime for $V_{DS} > V_{GS} - V_T$. Here, V_T is the threshold voltage. The output characteristics (drain current I_{DS} vs. drain-source voltage V_{DS} at multiple constant gate-source voltages V_{GS}) and transfer characteristics (I_{DS} vs. V_{GS} at fixed V_{DS}) of the TFTs are measured using an Agilent E5272A medium-power source/monitor unit connected to a probe station. By measuring the output and transfer characteristics, many important TFT performance

parameters such as field-effect mobility (μ_{FE}) in the linear regime, saturation mobility (μ_{SAT}) in the saturation regime, threshold voltage (V_T), on-off current ratio ($I_{ON/OFF}$), and subthreshold slope (S) can be obtained.

2.2.2.1 Field-effect mobility (μ_{FE}) in the linear regime

For small values of V_{DS}, the field-effect mobility (μ_{FE}) in the linear regime can be determined by calculating the transconductance g_m which is the change of I_{DS} with V_{GS} for a small drain voltage V_{DS}.

From eq. (2-10), it is given by

$$g_m = \left(\partial I_{DS} / \partial V_{GS}\right)\Big|_{V_{DS}=small\ const.} = \frac{W\mu_{FE} C_i}{L} V_{DS} \qquad \text{Eq. (2-12)}$$

Therefore, the linear mobility (μ_{FE}) solved from Eq. (2-12) is given as:

$$\mu_{FE} = g_m \frac{L}{W}\frac{1}{C_i}\frac{1}{V_{DS}}\Bigg|_{V_{DS}=small\ const.} \qquad \text{Eq. (2-13)}$$

2.2.2.2 Field-effect mobility (μ_{SAT}) and threshold voltage (V_T) in the saturation regime

The field-effect mobility (μ_{SAT}) in the saturation regime is also extracted from the transfer characteristics (I_{DS} vs. V_{GS}) for the device biased as $V_{DS} > V_{GS}$-V_T. Equation (2-11) shows that the square root of the saturation current is linearly dependent on gate voltage. The field-effect

mobility in saturation can be extracted from the slope of the curve which plots the square root of the saturation current as a function of gate voltage V_{GS} and the threshold voltage V_T can be determined by extrapolating this linear region to the horizontal *x*-intercept, as shown in Figure 2.6.

$$Slope = \frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} = \sqrt{\frac{\mu_{SAT} C_i W}{2 L}} \qquad \text{Eq. (2-14)}$$

$$\mu_{SAT} = 2 \frac{L}{W} \frac{1}{C_i} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad \text{Eq. (2-15)}$$

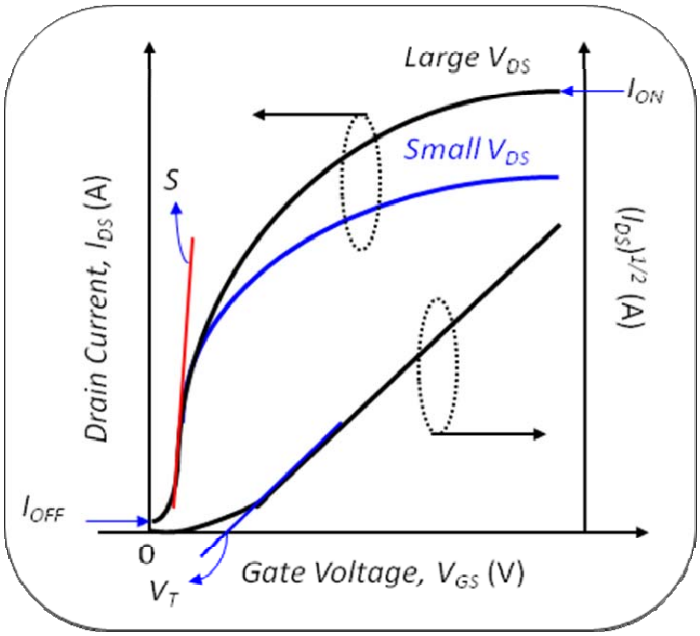

Figure 2.6: Transfer characteristics of a TFT.

2.2.2.3 On-off current ratio ($I_{ON/OFF}$) and subthreshold slope (S)

On-off current ratio ($I_{ON/OFF}$) and the subthreshold slope (S) are also extracted from the transfer characteristics. The on-off current ratio was determined by the ratio between the highest on-current measured (I_{ON}) and the minimum leakage current measured when the TFT is off (I_{OFF}). The subthreshold slope (S) was estimated as the minima on a $\left(\partial(\log I_{DS})/\partial V_{GS}\right)^{-1}$ vs. V_{GS} graph and should be kept small in order to minimize switching time and power consumption. The subthreshold slope (S) can be used to estimate upper limits to the bulk and semiconductor/gate dielectric interface density of states (DOS) by using the equation and a maximum interfacial trap density ($N_{trap}^{\max}$) can be estimated from the following equation [81-83]:

$$S = \frac{d|V_{GS}|}{d\log|I_{DS}|} = (k_B T/q)\log 10\left[\left(qN_{trap}^{\max}/C_i\right)+1\right] \qquad \text{Eq. (2-16)}$$

where k_B is the Boltzmann constant, T is temperature, q is the electronic charge, C_i is the capacitance density of the gate insulator, and $qN_{trap}^{\max}$ is the equivalent capacitance density contributed by subgap states in the bulk and at the semiconductor/dielectric interface, and S is the subthreshold slope in V/decade.

2.3 Calculation of contact and channel resistances

Contact and channel resistances limit the operation speed due to charging, and discharging of the capacitor (C) associated with the device. The switching frequency of TFTs is expressed as $f \propto \frac{\mu V}{L^2}$ [84], where f is frequency, μ is mobility, V is applied voltage and L is channel length. High mobility and short channel length at a given operating voltage in a TFT

are desirable to achieve high switching speed. Channel resistance can be reduced by using high mobility oxide semiconductors. However, device performance in short channel devices can be degraded due to the contact effect at the interface of metal/oxide semiconductor. In organic TFTs, source-drain contact resistance, R_c, effects have been reported with short channel devices, which limits the electrical performance [85]. In short channel *a*-IGZO TFTs, contact resistance effects can also limit the electrical performance by decreasing the field-effect mobility (μ_{FE}) [86][87, 88]. Therefore, it is important to quantify the influence of R_c on the overall electrical performance. The source-drain contact resistance effectively limits the maximum transconductance $g_m = \partial I_{DS} / \partial V_{GS}$ attainable at a given mobility and channel length, increasing the subthreshold slope $S = \left(\partial(\log I_{DS}) / \partial V_{GS}\right)^{-1}$ and decreasing the cutoff frequency $f_T = g_m / 2\pi C_i$. Hence, R_c is the limiting factor to achieve high frequency TFT operation [89].

Contact resistance in oxide TFTs is much higher than that in poly-Si TFTs, limiting the ability of oxide TFTs to achieve high speed operation. Therefore, it is very important to understand the physical mechanism of contact resistance in TFTs and its relevance to the gate voltage, device structure, and the interface properties between source/drain metal electrodes and semiconductors. In this work, a top contact configuration was employed to oxide TFTs due to its lower contact resistance compared to that of oxide TFTs with a bottom contact configuration. As discussed earlier, the lower contact resistance in a top contact configuration is associated with the increased effective contact area. On the other hand, the bottom contact configuration is limited by the film morphology near contacts. The extraction of contact resistances in this work follows a transmission line method (TLM) which was also applied to amorphous silicon TFTs [90]. Recently, this model has been applied to extract the contact resistance from organic or

oxide TFTs [85, 87-89, 91, 92]. In this method, the current-voltage characteristics are measured in devices with different channel length.

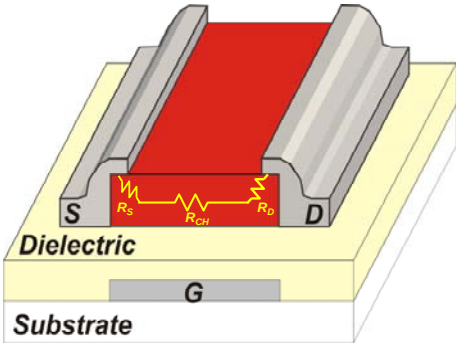

Figure 2.7: Contact and channel resistances of a TFT.

A schematic of a top contact oxide TFT in Figure 2.7 shows equivalent resistance corresponding to a source contact resistance (R_S), channel resistance (R_{CH}), and drain contact resistance (R_D). The overall device resistance, R_{ON}, can be considered as the sum of the channel resistance, R_{CH}, and a total contact resistance, R_C, which can be expressed as:

$$R_{ON} = \frac{\partial V_{DS}}{\partial I_{DS}}\bigg|_{V_{DS}\to 0}^{V_{GS}} = R_{CH} + R_C \qquad \text{Eq. (2-17)}$$

$$R_{ON}W = R_{SH}\frac{L}{W} + R_C W \qquad \text{Eq. (2-18)}$$

$$R_{SH} = \frac{1}{\mu C_i (V_{GS} - V_T)} \qquad \text{Eq. (2-19)}$$

where R_{SH}, μ, and V_T are the sheet channel resistance, the effective mobility and threshold voltage, respectively.

By plotting R_{ON} vs. L at different gate voltages using a transmission line method (TLM), R_C can be estimated as the ordinate extrapolated for a zero channel length [85, 91, 93]. Total width-normalized contact resistance (R_CW) is extracted by plotting the width-normalized total resistance ($R_{ON}W$) as a function of L for different gate voltages. By extrapolating $R_{ON}W$ to $L = 0$ μm, the y intercept of the least squares fit yields R_CW and the slopes correspond to the sheet channel resistance R_{SH}.

2.4 TFT fabrication

2.4.1 Introduction

Most devices and circuits are fabricated on 1713 Corning glass, ITO-coated glass, silicon, or flexible polyethersulfone (PES) substrates (*i*-Components Co. Ltd.). The preparation of the devices is mostly done in the Microelectronics Research Center (MiRC) at the Georgia Institute of Technology (GT). Cleaning, spin-coating, photolithography, lift-off and wet etching processes are mainly used for bottom-gate top-contact oxide TFTs. Gate and source/drain metallization are made with a CVC E-beam evaporator. Several gate dielectric layers were deposited with the following equipment:

- PVD75 RF sputterer
- Unaxis PECVD
- CVC e-beam evaporator and PVD thermal evaporator
- Atomic layer deposition (ALD) system

The PVD 75 RF sputterer was used to coat several gate dielectric materials such as BST, Si_3N_4, SiO_2, and AlN. Oxide-based semiconducting channel layers such as ZnO and InGaZnO

were also deposited by the RF sputterer. An ALD system from Cambridge Nanotech was used to deposit Al_2O_3 films as gate insulators, which allows high quality and defect-free films. The Heraeus Vacuum Oven was used to heat samples up to 350 ºC in air. The oven has a controller, allowing the user to program in a recipe that includes multiple ramping times, dwelling steps, and cooling steps. Thermal evaporation is an alternative method for depositing metal electrodes and is usually used for the deposition of organic films. Organic films such as pentacene were deposited using a Spectros high-vacuum PVD thermal evaporation system (Kurt J. Lesker Company). This system is equipped with four organic and two metal sources and has the capability to carry out co-depositions of several materials. Several photo or shadow masks were used to pattern gate and source/drain metal, gate dielectric materials, oxide layers, and organic layers for the fabrication of TFTs.

2.4.2 Thin-film deposition and processing

This section covers deposition and processing techniques that were used for this research. Many other processing techniques are available, as explained in detail elsewhere [94].

2.4.2.1 Sputtering

Sputtering is a common thin-film deposition technique, where the source target material is bombarded by energetic ions, generally argon ions. Radio frequency (rf) sputtering is performed by accelerating ions of argon or an argon oxygen mixture into the surface of a sputter target, which is made of the material to be applied to the sample. The gas ions cause atoms to be knocked off of the target and deposited on the sample being coated. Radio frequency (rf) sputtering can be used to deposit various oxide semiconductors including ZnO,

IZO, GZO, and IGZO as *n*-channel layers in oxide TFTs. The rf sputtering also allows coating with dielectric materials such as BST, silicon dioxide (SiO_2), and silicon nitride (SiN_X) as insulating layers in TFTs. Metal coatings are usually performed with a DC sputterer or with the CVC E-Beam evaporator. However, dielectric materials must be deposited by the rf sputtering or some other way, such as chemical vapor deposition (CVD) using a machine such as a Plasma Enhanced Chemical Vapor Deposition (PECVD) or an atomic layer deposition (ALD) system. In this work, the rf sputtering was used to deposit various dielectric materials such as BST, indium tin oxide (ITO), zinc oxide (ZnO), and indium gallium zinc oxide (IGZO).

2.4.2.2 Plasma enhanced chemical vapor deposition

Chemical vapor deposition (CVD) techniques employ gas-phase sources to form a thin film. Unaxis plasma enhanced chemical vapor deposition (PECVD) system is used to deposit dielectric materials such as SiO_2 or low-stress SiN_X as gate insulating layers in TFTs. The PECVD system reacts gases in a radio frequency (RF) induced plasma to deposit materials such as SiO_2 and SiN_X. The PECVD system operates at 13.56MHz and has one chamber that is used for all depositions. This system is designed to control the stress of deposited films by adjusting the ratio of $He:N_2$. The PECVD can process a wide range of sample sizes. The number of samples depends on the size of the samples. A typical run can process anywhere from one to four 5 inch wafers, and deposition will be uniform regardless of any through-wafer or through-sample holes. Typical deposition rates range from 80Å/min to 400Å/min, depending mainly on power and temperature. At the MiRC, this system was used primarily for depositing low-stress

silicon nitride films, silicon dioxide, and silicon carbide layers. It can be used for depositing silicon oxynitride and thin layers of amorphous silicon.

2.4.2.3 Evaporation

The CVC e-beam evaporator 1 and 2 were used to deposit metal electrodes in the TFTs fabricated here. E-beam evaporators can be used to coat samples with various metals including Cr, Ti, and Au. The E-beam evaporators were also used to deposit dielectric films such as SiO_2, Al_2O_3, and TiO_2. A high-intensity beam of electrons is focused on the center of a crucible containing the material to be evaporated. The energy from the electron beam melts a region of the source metal. Material evaporates from the source and covers the sample with a thin layer. Unlike sputtered films, evaporators only coat the surface facing away from the substrate. E-beam evaporators provide very little coating to the sides of any features that are perpendicular to the surface of the substrate. In a typical process, the chamber is pumped down to a pressure of 5×10^{-7} Torr to increase the mean free path. The mean free path of a gas molecule is the average distance the molecule travels before it collides with another molecule. This prevents air molecules from interrupting metal atoms as they travel from the evaporation source to the substrate. Then, the metal is heated to the point of vaporization by a high-intensity beam of electrons. This causes the metal to evaporate, and the metal molecules travel in a straight line to be deposited on the substrate. Typical deposition rates range from two to five angstroms per second.

A PVD 75 filament thermal evaporator manufactured by Kurt J. Lesker Company (KJLC) in the MiRC was also used to deposit various metals like the e-beam evaporators. The filament

evaporator also provides very little coating to the sides of any features that are perpendicular to the surface of the substrate. Unlike the e-beam evaporators, the filament evaporator is used to deposit only metals. It is ordinarily used for gold, nickel, chromium, aluminum, and copper coatings. However, it can be used to evaporate most other metals as well. In a typical process the chamber is pumped down to a pressure of 5 x 10^{-7} Torr to prevent air molecules from interrupting metal atoms as they travel from the evaporation source to the substrate. Then the metal evaporation source is heated to a high temperature by a tungsten filament. This causes the metal to evaporate and be deposited on the substrate. Typical deposition rates range from two to five Å/second. In most cases metal depositions are performed in the CVC electron beam evaporator or in the CVC DC sputterer. However, the filament evaporator is a good choice for samples that need to be evaporator coated (to avoid coating the sides of rough topologies) and are sensitive to x-ray radiation that may be emitted by the electron beam gun in the e-beam evaporator.

2.4.2.4 Atomic layer deposition

Compared with previously discussed techniques such as evaporation, PECVD, and sputtering, an atomic layer deposition (ALD) is a powerful technique that produces high-quality and defect-free thin films with excellent step coverage and few defects at a relatively low processing temperature [95-97]. Dielectric films grown by ALD have a high resistivity and good barrier properties, and therefore are excellent candidates for gate insulators. To produce high performance TFTs operating at a low voltage, small threshold voltage (V_T), small subthreshold slope (S), and high on-off current (I_{on-off}) ratio need to be achieved. Consequently,

TFTs that exhibit high-mobility with a high capacitance density are desirable. Therefore, in addition to the high mobility semiconductors, the gate dielectric materials should have a high dielectric constant and should be able to be processed into defect-free thin-films to form such TFTs. In this work, a high-*k* and thin Al_2O_3 layer grown by ALD and a high mobility rf-sputtered amorphous InGaZnO was used as a gate insulator and a channel semiconductor, respectively, to develop a high-performance TFT operating at a low voltage with a low leakage current.

The basic principle of ALD is as follows. Two sequential surface reactions produce the ALD thin-film growth. Because there are only a finite number of chemical species on the surface, both reactions are self-limiting. The chemical species are exchanged during each surface reaction. Therefore, ALD is a special modification of chemical vapor deposition (CVD) with the distinct feature that film growth takes place in a cyclic manner. Normally one growth cycle consists of four steps: 1) Exposure of the first precursor, 2) purging of the reaction chamber, 3) exposure of the second precursor, and 4) a further purging of the reaction chamber. The growth cycles are repeated as many times as required for the desired film thickness. Depending on the process and the reactor being used, one cycle can typically take time from 0.5 s. to a few seconds, and may deposit between 0.1 and 3 angstrom of film material.

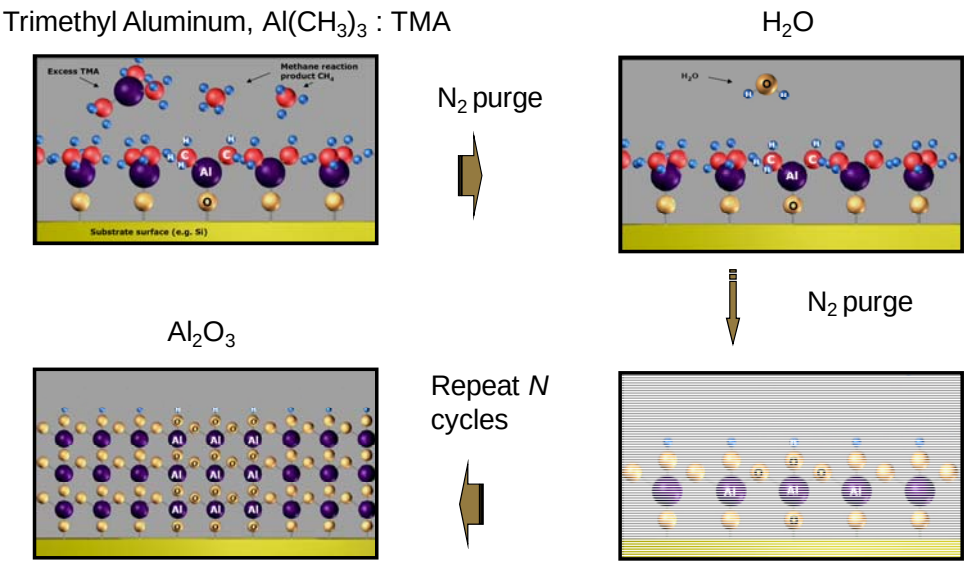

Figure 2.8: ALD example cycle for Al_2O_3 deposition. (Cambridge NanoTech Inc.)

Al_2O_3 can be used to describe ALD thin-film growth. An example of the ALD cycle for Al_2O_3 deposition from Cambridge NanoTech Inc. is illustrated in Figure 2.8. In air, water (H_2O) vapor is adsorbed on the Si surface, forming hydroxyl groups. With silicon this forms: Si-O-H (s). The deposition process involves alternate exposure of two precursors, trimethylaluminum (TMA) and H_2O. First, TMA is pulsed into the reaction chamber. The TMA reacts with the adsorbed hydroxyl groups until the surface is passivated. TMA does not react with itself, terminating the reaction to one layer. This causes the perfect uniformity of ALD. Next, the excess TMA is pumped or carried away with the methane reaction product. The same process is then repeated with H_2O, the gas phase precursor. After the TMA and methane reaction product are pumped or carried away, H_2O vapor is pulsed into the reaction chamber and reacts with the dangling methyl groups on the new surface, forming aluminum-oxygen (Al-O) bridges and

hydroxyl surface groups that are waiting for a new TMA pulse. Again, methane is the reaction product. The excess H_2O vapor and reaction product methane are pumped or carried away. Excess H_2O vapor does not react with the hydroxyl surface groups, again causing perfect passivation to one atomic layer. This completes one cycle that deposits approximately 0.1 nm-thick monolayer of Al_2O_3. These cycles are repeated to achieve the desired Al_2O_3 film thickness.

2.4.2.5 Thermal annealing

Post-deposition annealing of oxide semiconductors is often employed to improve the desired properties of thin films. For example, post-deposition annealing of oxide semiconductors in an inert ambient often increases the conductivity because oxygen vacancies are a possible source of intrinsic donor defect in oxide semiconductors. For oxide TFTs, post-deposition annealing strongly influences the conductivity of the semiconductor channel layer which affects the turn-on voltage, threshold voltage, and mobility of TFTs. A Heraeus Vacuum Oven is used to heat samples up to 350 ºC in air. The oven has a controller, allowing the user to program in a recipe that includes multiple ramping times, dwelling steps, and cooling steps. In this work, the Vacuum Oven was used to anneal *n*-channel oxide semiconductors including InGaZnO in air.

2.4.3 Deposition of organic semiconductors

Deposition of the organic semiconductors was made with a SPECTROS vacuum thermal evaporation system from Kurt J. Lesker Company (KJLC). Depositions were performed under high vacuum (lower than 10^{-7} Torr) by heating the source material with

resistive heaters until it sublimes or evaporates and deposits on the substrates. Shadow masks in close proximity to the substrates can be used to define the pattern of the deposited materials. The system has four organic sources and two high current sources, which can be used for evaporation of some metals and oxides. Additionally, the system is capable of co-depositions with two materials. To prevent exposure of deposited organic films to ambient atmosphere, the system is integrated with an N_2-filled glove box from MBRAUN so that samples can be directly loaded from the glove box into the deposition system and vice-versa. Deposition rates and thicknesses are measured by calibrated quartz crystal monitors and can be controlled by adjusting the power applied to the sources. The deposition conditions can have a significant influence on the ordering and the packing of the molecules and the morphology of the organic films and must be monitored closely. In the experiments presented in this work, 40-60 nm thick pentacene layers were thermally evaporated at a rate of 0.4-1 Å/s onto the substrates held at room temperature.

2.4.4 Thin-film and metal patterning techniques

Two methods were used in this work to pattern thin films: wet etching and lift-off processes. Etching is the preferred process since the photoresist is spun on after the film has been deposited, which does not affect any of the deposition parameters. There are also fewer chances of contaminating the interface between the two films when etching is employed. Several chemical etchants were used to pattern gate dielectrics and semiconductor channel layers in the oxide TFTs and circuits described in this work. For example, amorphous BST (*a*-BST) film as a gate dielectric is etched with hydrofluoric acid (HF) diluted with DI water and a

buffered oxide etch 6:1 (BOE 6:1) was used to pattern SiO_2 and SiN_X films. On the other hand, a hydrochloric (HCL) acid diluted with DI water was used to pattern the amorphous InGaZnO film as a semiconductor layer.

Lift-off is a preferable technique used to remove unwanted material that cannot be etched. This technique requires pattering of the photoresist prior to the deposition of the film. After the film was deposited, the photoresist and unwanted film were removed by submersing the substrate in a solvent such as acetone. Therefore, lift-off is a simple, easy method for making metallic patterns on a substrate, especially for those noble metal thin films such as platinum, tantalum, nickel or iron which are difficult to etch with conventional methods. The general lift-off process was as follows. First, a pattern was defined on a substrate using photoresist. A film, usually metallic, was deposited all over the substrate, covering the photoresist and areas in which the photoresist have been removed. During the lift-off process, the photoresist under the film was removed with solvent, removing the film, and leaving only the film which was deposited directly on the substrate. In this work, metal gate or source/drain electrodes in oxide TFTs were usually patterned by photolithography and lift-off processes. Note that during film deposition, the deposition temperature should be controlled not to degrade the property of the photoresist.

2.5. Setup for electrical and thin-film surface characterization

The electrical measurements were performed with a Lucas-Signtone H100 series probe station in an MBraun Labmaster N_2-filled glovebox. The current-voltage characterization and capacitance-voltage characterization were carried out with an Agilent E5272A 2 channel

source-monitor unit (± 100 V DC range, 200 mA current limit) and an Agilent 4284A precison LCR meter (20 Hz to 1 MHz), respectively. All measurements and data acquisition were automated using Labview software. Programs like OriginLab, Microsoft Excell, and Matlab, were used for data analysis. AutoCAD is used for mask design and drawing. The film thickness was measured and calibrated by a profiler (Veeco Instrument), which is located in the Kippelen's lab at GT. A Scanning Probe Microscope (SPM) from Veeco in MiRC at GT was used to inspect the morphology of films. The crystalline structures of the films were analyzed using x-ray diffraction (XRD). The system was available in the School of Materials Sciences and Engineering at GT.

CHAPTER 3 OXIDE SEMICONDUCTOR DEVICES

Transparent oxide-based thin-film transistors (TFTs) have attracted much attention because of their high electron mobilitiy values (> 10 cm^2/Vs) and because they can be processed at low temperature to produce large-area displays with the potential of low production costs [9]. However, large operating voltages are often required to achieve high mobility and high on/off current ratio in such TFTs. For circuit applications, such as inverters, ring oscillators, and backplane circuits for mobile displays, low-voltage and high frequency operations are desirable. For low-voltage operation, small threshold voltage (V_T), small subthreshold slope (S), and high on-off current ($I_{on\text{-}off}$) ratio need to be achieved. Consequently, TFTs that exhibit high mobility with a high capacitance density are desirable. Therefore, the research focused on the development of low-voltage and high-performance n-channel oxide TFTsusing high-k and/or thin dielectrics as gate insulators. We select amorphous indium gallium zinc oxide (*a*-IGZO), as semiconductor for *n*-channel transistors. In this chapter, the first and second sections focus on the fabrication of *n*-channel *a*-IGZO TFTs with a high-k, amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ (*a*-BST) or a thin Al_2O_3 grown by ALD as gate insulators. Such oxide TFTs are employed to demonstrate AMOLED display backplane circuits operating at low voltage, which is described in the last section of this chapter.

3.1. InGaZnO TFTs with high-k amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ gate insulator

Recently, a ZnO-based TFT using a high-k Mg-doped $Ba_{0.5}Sr_{0.5}TiO_3$ (BST) gate insulator on a PET substrate was fabricated at low temperature [31]. This TFT showed a field

effect mobility of 16.3 cm^2/Vs, sub-threshold slope of 0.4 V/decade, and an on/off current ratio of 6.4×10^4 at 6 V. However, ZnO films are polycrystalline even when deposited at room temperature. This leads to channels with grain boundaries that deteriorate the TFT stability, uniformity, and performance of its electrical characteristics [32]. In contrast, indium gallium zinc oxide (IGZO) films, deposited by physical vapor deposition or rf-magnetron sputtering, show an amorphous morphology. Using high-k Y_2O_3, [25, 29] as gate dielectric, high performance amorphous-IGZO-based TFTs have been reported, with electron mobility values over 10 cm^2/Vs, V_T = 1.4 V and S = 0.20 V/decade. Despite operating below 6 V, the low V_{DS} region on these TFTs shows strong nonlinear effects that are commonly associated with a source-drain contact resistance (R_c) limited behavior. The source-drain contact resistance effectively limits the maximum transconductance, attainable at a given mobility and channel length, consequently, increasing the subthreshold slope and decreasing the cutoff frequency. Therefore, it is desirable to reduce the contact resistance R_c since it is the limiting factor to achieve low voltage and high frequency TFT operation.

3.1.1 Experimental details

The TFTs employ a common bottom-gate and top-contact geometry and were fabricated using the following steps: first, ITO on a glass substrate was used as the common gate electrode; a 170 nm-thick *a*-BST gate dielectric layer was deposited onto the ITO on glass substrate by rf-sputtering without substrate heating, using a power of 150 W, a working pressure of 5 mTorr, and an O_2/Ar (6/4) atmosphere. A 30 nm-thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) active layer was then deposited by rf-sputtering at room temperature and using a

power of 125 W, a working pressure of 5 mTorr, and an O_2/Ar (1/10) atmosphere. After deposition of the *a*-IGZO layer, the device was annealed at 325 °C for 30 minutes in air. To define the channel *a*-IGZO layer was patterned by wet-etching process using hydrochloric acid (HCl: H_2O = 100:1) diluted in DI water. To provide access to the gate electrode, *a*-BST was selectively patterned using hydrofluoric acid (HF: H_2O = 10:1). Then, Ti (6 nm) and Au (120 nm) were sequentially e-beam deposited and patterned by lift-off process to form the source and drain electrodes, creating a total overlap area of 1.5×10^{-3} cm^2 with the gate electrode.

3.1.2 Dielectric properties of *a*-BST

Although BST is a well-known high-k dielectric in its polycrystalline phase, the voltage-dependent dielectric constant characteristics that make it attractive for dynamic random access memories and tunable microwave devices [98] is less desirable to achieve low-voltage and high-frequency operating TFTs. In contrast with its polycrystalline phase, which requires high deposition temperatures, *a*-BST films can be fabricated using rf-sputtering at room temperature. Figure 3.1 shows x-ray diffraction (XRD) patterns confirming the amorphous nature of the BST films right after room temperature deposition, and after annealing for 1 hr at 325 ^oC in air. While the dielectric constant of the amorphous phase ($\varepsilon_r = 28$) is smaller than that of the polycrystalline phase ($\varepsilon_r > 100$), [99] *a*-BST shows no appreciable dielectric tunability.

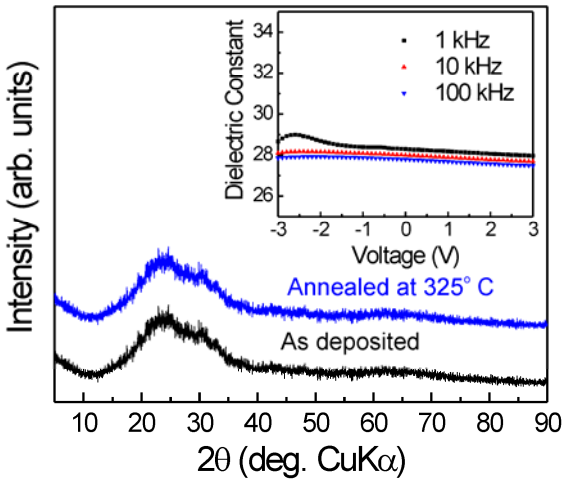

Figure 3.1: XRD patterns of amorphous BST film on glass substrate as deposited at room temperature and after annealed at 325 °C for 1 h. Inset: Dielectric constant measured on a Au/Ti/a-BST/ITO/Glass sample as a function of bias voltage and at 1, 10 and 100 kHz.

The inset of Figure 3.1 shows that the dielectric capacitance measured in Au(120nm)/Ti(5nm)/*a*-BST(170nm)/ITO/Glass samples using an Agilent 4284A LCR meter decreases only 3.0 % with frequencies ranging from 1 kHz to 100 kHz and bias voltages between -3 V and 3 V. This behavior is consistent with BST's amorphous nature and also is indicative of a low defect concentration [98, 99]. In these samples, the capacitance density is estimated to be 145 nF/cm^2 with breakdown field values of 1.4 MV/cm or higher. The leakage current densities were highly asymmetric due to the different electrodes (ITO bias electrode and Ti/Au ground electrode) with values of $< 10^{-7}$ A/cm^2 and 1×10^{-4} A/cm^2 at bias voltage of -3 V and +3 V, respectively. Therefore, *a*-BST combines a large voltage and frequency independent

dielectric constant which is desirable for the fabrication of *a*-IGZO-based TFTs with a large capacitance density.

3.1.3 Electrical characterization

Several *a*-BST/*a*-IGZO TFTs were fabricated using a channel width of W=1000 µm and channel lengths ranging from 100 to 5 µm. Figure 3.2 shows the measured transfer and output characteristics of the *a*-BST/*a*-IGZO TFT with a W/L=1000 µm/5 µm. All *a*-BST/*a*-IGZO TFTs exhibited *n*-channel transistor behavior with saturation mobility values of 10±1 cm^2/Vs, operating in the enhancement mode, with excellent sub-threshold slopes of 0.11±0.02 V/decade, low threshold voltages (0.5±0.1 V), and a high on-off current ratio up to 8×10^7 at 3 V (W/L=1000 µm/5 µm). The average values and standard deviations were calculated from measurements performed on 20 devices with four devices per given channel length.

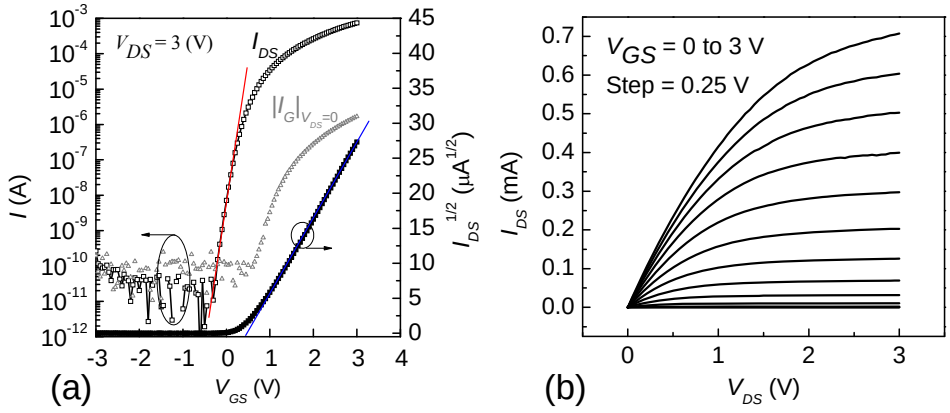

Figure 3.2: Operation characteristics of sputtered a-BST/a-IGZO TFT with L = 5 µm and W = 1000 µm. (a) Transfer characteristics (squares), V_{GS} was swept from –3 to +3 V at V_{DS} = 3 V, and leakage current (triangles) at V_{DS} = 0 V. (b) Output characteristics. V_{DS} was swept from 0 to +3 V at each V_{GS} varied from 0 to 3 V at 0.25 V steps.

The leakage current, $| I_G |$ as a function of V_G was also measured at $V_{DS} = 0$ V. As shown in Figure 6(a), even in these common gate devices, the leakage current in the off-region is around 10^{-10} A and in the on-region does not contribute in more than 0.1 % to the signal current. Further reduction of the leakage currents can be achieved when pattering the gate electrode.

3.1.4 Contact and channel resistances

Unlike organic or *a*-Si TFTs, very little experimental work has been reported on the source-drain contact resistance, R_c, effects on oxide TFTs. Figure 3.3(a) shows that g_m, calculated as its maximum value as a function of $V_{GS,}$ follows the expected L^{-1} dependence in TFTs down to 5 μm channel lengths. This behavior is only explained if μ remains constant as function of L, the standard deviation is around 10 % in both regions, since as shown in the inset of Figure 3.1, C_{gate} is voltage independent. The very small S values can then be explained by a large C_{gate} and by the fact that g_m does not seem to be limited by contact resistance effects.

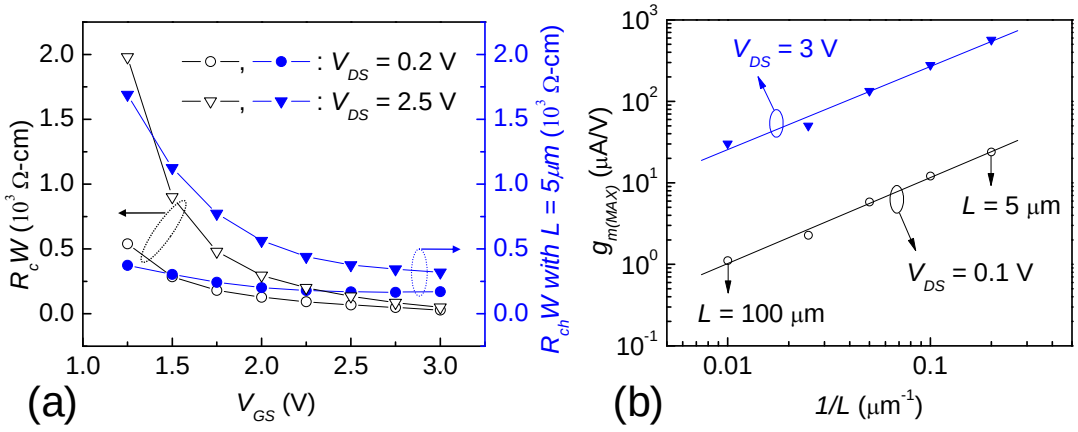

Figure 3.3: (a) Transconductance (g_m) versus inverse of channel length (*1/L*) in the linear (V_{DS} = 0.1 V) and saturation (V_{DS} = 3 V) regions for a-BST/a-IGZO TFTs. (b) Width-normalized contact resistance (R_cW) as function of channel length ranging from 5 μm to 100 μm and width-normalized channel resistance ($R_{ch}W$) at a channel length of 5 μm in the linear (V_{DS} = 0.2 V) and saturation (V_{DS} = 2.5 V) regions for amorphous IGZO TFTs.

The width-normalized contact resistance (R_cW) of *a*-BST/*a*-IGZO TFTs was extracted from devices with a channel width of 1000 μm and channel lengths ranging from 5 μm to 100 μm. In the linear (V_{DS} = 0.2V) and saturation (V_{DS} = 2.5V) regions, R_cW was compared with the width-normalized channel resistance ($R_{ch}W$) of a 5 μm channel length TFT at different gate voltages. Figure 3.3(b) shows that in the saturation region, R_c and R_{ch} are larger than in the linear region due to channel pinch-off at the drain contact, [85]. Furthermore, in both regions $R_{ch}W > R_cW$ above V_{GS} = 1.5 V, and at V_{GS} = 3V, R_cW < 50 Ω–cm represents < 20 % of $R_{ch}W$. Studies are underway to determine the origin of the very small contact resistance observed in our

devices. However, is expected that the major contribution to R_c comes from the bulk *a*-IGZO layer rather than from the a-IGZO/source(drain) interface [87, 88].

3.1.5 Summary

In summary, we have demonstrated high performance top contact bottom gate *n*-channel *a*-IGZO thin-film transistors that use a 170 nm-thick *a*-BST (ε_r = 28) as a gate dielectric material. Amorphous-BST films deposited at room temperature by rf-sputtering show negligible frequency and voltage dependence. With a high gate dielectric capacitance density of 145 nF/cm^2, *a*-BST/*a*-IGZO TFTs show high saturation mobility values of 10±1 cm^2/Vs, low threshold voltages of 0.5±0.1 V at 3 V and on-off current ratios up to 8x10^7. The very low source-drain contact resistance < 50 Ω–cm at 3 V obtained in these TFTs allows for very small sub-threshold slopes of 0.11±0.02 V/decade and a channel length independent mobility which does not limit the transconductance and potentially allows for TFTs capable of low power and high frequency operation.

3.2 InGaZnO TFTs with Al_2O_3 gate insulator grown by atomic layer deposition

In devices using high-mobility semiconductors, operating voltages can be reduced by developing gate dielectric materials capable of large capacitance densities with low-leakage currents that have good compatibility for the growth of the semiconductor channel, leading to low-trap densities at the semiconductor-gate dielectric interface. Using 170 nm-thick amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ (*a*-BST) (ε_r = 28) as the gate dielectric, we demonstrated low-voltage high-performance amorphous indium gallium zinc oxide (*a*-IGZO) TFTs with electron mobility

values of 10 cm^2/Vs, threshold voltages (V_T) of 0.5 V, and very small subthreshold slopes (S) of 0.11 V/decade [89] as described in pervious Section 3.1. However, the small bandgap (3.3 eV) and relatively large electron affinity (4 eV) of *a*-BST forces careful control over the TFTs geometry to reduce the leakage currents and limits its operational range. The use of larger bandgap dielectrics is then desirable to increase the energy band offsets with respect to *a*-IGZO. As an alternative approach to increase the capacitance density of the gate dielectric, we used a 100 nm-thick Al_2O_3 layer deposited by atomic layer deposition (ALD). With a high dielectric constant of 9 and a large bandgap of 8 eV, Al_2O_3 is a good candidate to produce gate dielectrics with low leakage and high capacitance density. Furthermore, ALD is a well-known deposition process that yields highly conformal, defect-free dielectric layers at relatively low temperatures [96, 100]. Dielectric films grown by ALD have a high resistivity and good barrier properties and have been used to produce high performance polycrystalline ZnO-TFTs [37, 101]. However, such TFTs usually have large V_T and S, forcing them to operate at relatively high voltages. Here we developed *n*-channel InGaZnO (IGZO) TFTs with Al_2O_3 gate insulator grown by ALD.

3.2.1 Experimental details

In this work, the TFTs were fabricated with a bottom gate and top-contact source and drain electrodes geometry. First, a tri-layer of Ti (6 nm)/Au (50 nm)/Ti (6 nm) was deposited using electron-beam (e-beam) at room temperature on a glass substrate (Corning 1737) and patterned by photolithography followed by a lift-off process. A 100 nm-thick Al_2O_3 gate dielectric layer was then deposited by ALD at 80 °C by using $Al(CH_3)_3$ and H_2O as the precursors. Contact holes were formed by a lift-off process to provide access to the gate

electrode. A 40 nm-thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) active layer was then deposited by rf sputtering at room temperature using a power of 125 W, a working pressure of 5 mTorr, and an O_2/Ar (1/10) atmosphere. After deposition of the *a*-IGZO layer, the device was annealed at 325 °C for 30 minutes in air. To define the channel, the *a*-IGZO layer was patterned by a wet-etching process using hydrochloric acid (HCl: H_2O = 1:100) diluted in DI water. Then, Ti (6 nm) and Au (120 nm) were sequentially deposited by e-beam and patterned by a lift-off process to form the source and drain electrodes, creating a total gate to source/drain electrode overlap area of 4×10^{-5} cm^2, assuming an overlap channel length of L_{ov} = 5 μm and a channel width of W = 400 μm. Several Al_2O_3/*a*-IGZO TFTs were fabricated using a channel width of W=400 μm and channel lengths (L) of 100, 20, 10 and 5 μm.

A Savannah100 ALD system from Cambridge Nanotech Inc. was used to deposit the Al_2O_3 dielectric films. The Al_2O_3 films were deposited at 80 °C using alternating exposures of tri-methyl-aluminum ($Al(CH_3)_3$) and H_2O vapor at a deposition rate of approximately 0.1 nm per cycle. Each deposition cycle (one monolayer) lasted 24 s, yielding a total deposition time of around 6 h for 1,000 cycles. Details about the Al_2O_3 films grown by ALD were described in Chapter 2.

3.2.2 Dielectric properties of Al_2O_3 grown by atomic layer deposition

The dielectric properties of Al_2O_3 films sandwiched between Ti (6 nm)/Au (120 nm) and Ti (6 nm)/Au (50 nm)/Ti (6 nm) on glass substrates were characterized using parallel plate capacitors of various areas ranging from 1.1×10^{-3} cm^2 to 4.2×10^{-3} cm^2.

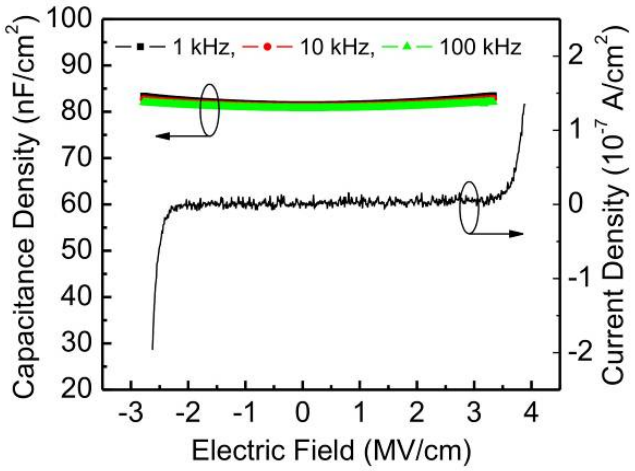

Figure 3.4: Capacitance density measured on a Au/Ti/Al_2O_3/Ti/Au/Ti/Glass sample as a function of electric field at 1, 10, and 100 kHz. Current density measured on the same sample.

Figure 3.4 shows a leakage current reaching a value of 10^{-7} A/cm^2 at 3.5 MV/cm and below the noise level for smaller electric fields. Similar values were also measured in capacitors with different thicknesses. Using an Agilent 4284A precision LCR meter, $C_i = 81 \pm 1$ nF/cm^2 was measured, yielding a dielectric constant of $\varepsilon_r = 9$. As shown in Fig. 5, variations smaller than 2 % were observed for frequencies ranging from 1 kHz to 100 kHz and bias voltages between -30 V and +35 V. Therefore, the Al_2O_3 layers deposited by ALD combine a small leakage current with a large dielectric constant that is independent of voltage and frequency, which is indicative of a low defect concentration [99].

3.2.3 Electrical characterization

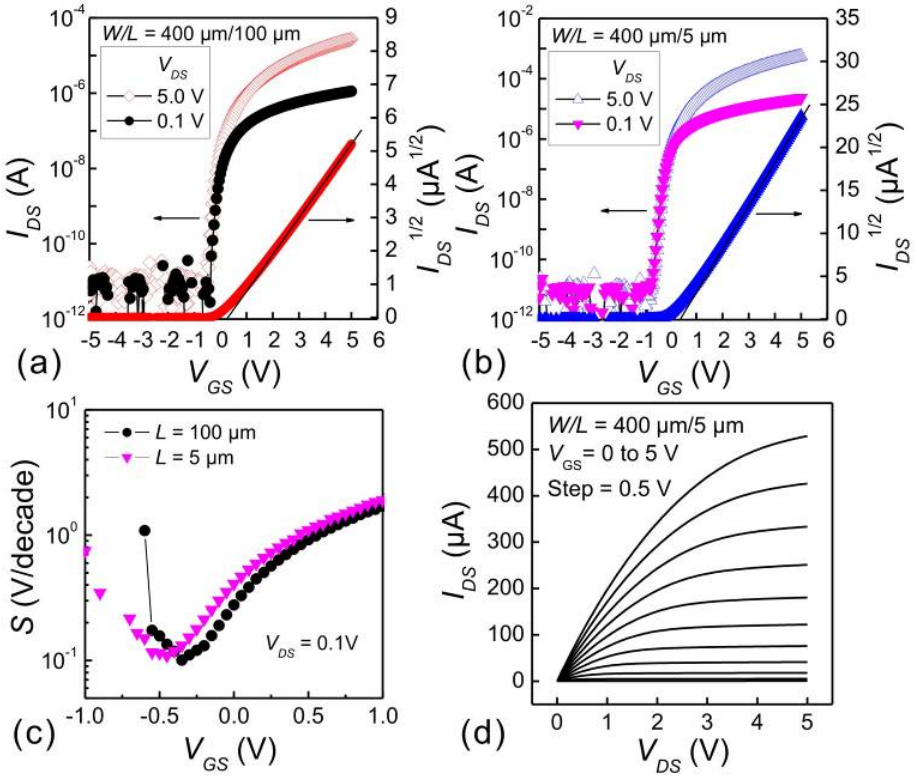

Figure 3.5: Hysteresis transfer characteristics of Al_2O_3(ALD)/*a*-IGZO TFTs with *L* = 100 μm and *W* = 400 μm (a) or *W* = 5 μm (b); (c) V_{GS} dependence of subthreshold slope in the linear region for TFTs with *L* = 5 μm and 100 μm, and *W* = 400 μm; (d) Output characteristics of a *W*/*L* = 400 μm/5 μm TFT.

Figure 3.5(a) shows the overlapping hysteresis transfer characteristics measured in the linear (V_{DS}=0.1 V) and saturation (V_{DS}=5 V) regions in a TFT with *W*/*L*=400 μm/100 μm. Figure 3.5(b) shows the same behavior in a TFT with *W*/*L*=400 μm/5 μm. Consistent with capacitor measurements, the leakage currents (not shown) at the operating voltages in all TFTs

remained below the noise level of 10 pA. All Al_2O_3(ALD)/*a*-IGZO TFTs exhibited n-channel transistor behavior operating in the enhancement mode with saturation mobility values of μ_{SAT} = 9 ± 1 cm^2/Vs, threshold voltages of V_T = 0.4 ± 0.1 V, and $I_{on\text{-}off}$ = 6 × 10^7 at 5 V (*W/L*=400 μm/5 μm). Figure 3.5(c), shows that *S* = 0.1 ± 0.01 V/decade in the linear region for the TFTs shown in Figures 3.5(a) and (b). The same *S* values were found in the saturation region. The average value and the standard deviation of *S*, and the other parameters presented, were calculated from measurements performed on 20 devices with four devices per given channel length. The subthreshold slope can be used to estimate upper limits to the bulk and semiconductor/gate dielectric interface density of states (DOS) by using the equation [82]. At 300 K, a maximum subgap DOS at the *a*-IGZO/Al_2O_3 interface is estimated to be 3.4 × 10^{-11} $cm^{-2}eV^{-1}$, corresponding to a maximum bulk DOS of 7 × 10^{-16} $cm^{-3}eV^{-1}$. Subthreshold slope values around 0.1 V/decade have also been reported in *a*-BST(C_{gate} = 145 nF/cm^2)/*a*-IGZO TFTs [89] and SiO_2(C_{gate} = 34 nF/cm^2)/*a*-IGZO TFTs [82] having gate dielectrics with significantly different capacitance densities and surface properties. These results complement recent observations [88] indicating that, in contrast to polycrystalline TFTs, the physics at the surface of the semiconductor/gate dielectric interface may not be playing a dominant role in determining the subthreshold properties of *a*-IGZO-based TFTs. While detailed studies are needed to confirm this hypothesis, the collective evidence seems to indicate that the key to achieve very small subthreshold slopes and enable low voltage operation lies in finding the processing conditions for *a*-IGZO that minimize the bulk subgap DOS. Figure 3.5(d) shows the output characteristics measured in TFTs with *L* = 5 μm, showing good linearity at low V_{DS} and small effects of channel length modulation approaching V_{DS} = 5 V.

3.2.4 Contact and channel resistances

The channel length-invariant properties observed in these TFTs suggest very small effects due to parasitic resistances. In the linear regime, these effects can be extracted from the electrical properties of devices with different channel lengths. As described in Ref. [89] using the transmission line method,[85, 91] the width-normalized contact resistance (R_cW) of Al_2O_3(ALD)/*a*-IGZO TFTs was extracted for W =400 µm and L ranging from 5 µm to 100 µm.

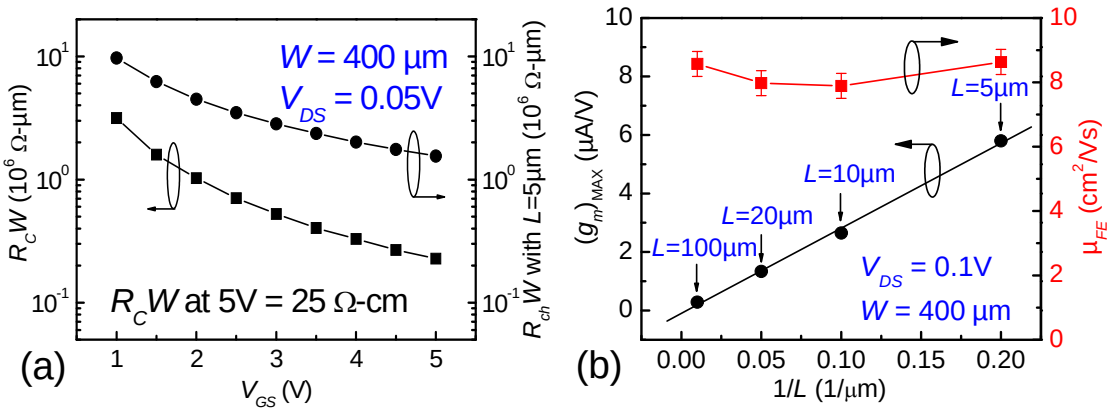

Figure 3.6: (a) Width-normalized contact resistance (R_cW) as function of channel length and width-normalized channel resistance ($R_{ch}W$) at a channel length of 5 µm in the linear (V_{DS} = 0.05 V) region for Al_2O_3(ALD)/a-IGZO TFTs. (b) Transconductance (g_m) and field effect mobility (μ_{FE}) versus inverse of channel length ($1/L$) in the linear (V_{DS} = 0.1 V) region for Al_2O_3(ALD)/*a*-IGZO TFTs.

Figure 3.6(a) shows that R_cW, at V_{DS} = 0.1 V, is less than 30 % of the width-normalized channel resistance ($R_{ch}W$) on a 5 µm channel length TFT for V_{GS} varying from 1.0 to 5.0 V. The very small values of R_cW, down to 25 Ω-cm at V_{GS} = 5 V, achieved in our devices are consistent

with prior experiments in patterned gate *a*-IGZO TFTs that indicate that the major contribution to the contact resistance comes from the bulk *a*-IGZO layer, namely the resistance to access the channel, rather than from the *a*-IGZO/source(drain) electrode interface [87, 88].

Another consequence of achieving very small values of R_cW is that the transconductance $g_m = Max\left(\partial I_{DS}/\partial V_{GS}\right)\big|_{V_{DS}}$ is maximized. As shown in Figure 3.6(b), this is confirmed by g_m being linearly dependent on L^{-1} and by a channel–length independent field-effect mobility $\mu_{FE} = L\, g_m/WC_iV_{DS} = 8.3\,\mathrm{cm^2/Vs}$. Therefore, we estimate that a TFT with L = 5 μm and an effective channel area of $A_{eff} = 6\times10^{-5}$ cm^2 could operate in the linear regime with a cutoff frequency of $f_T = g_m/(2\pi C_iA_{eff})$ = 0.2 MHz. In the saturation regime, we calculate a $g_m(V_{DS}$=V_{GS}=5V) of 240 μA/V that yields f_T = 7.8 MHz. Recently, Bayraktraroglu *et al*. [102] also demonstrated high current and power gain cut-off frequencies of 500 and 400 MHz from 2 μm channel length ZnO TFTs produced on GaAs substrates. Assuming the same electrical bias, we estimate that our value is comparable with f_T values measured in ZnO-based TFTs (C_i = 115 nF/cm^2, $A_{eff} = 1\times10^{-6}$ cm^2) that show similar electrical performance.

3.2.5 Summary

In summary, we have demonstrated high-performance top-contact bottom-gate n-channel *a*-IGZO thin-film transistors that use 100 nm-thick Al_2O_3 grown by ALD as the gate dielectric material. Al_2O_3 films deposited by ALD show very small leakage current below 10^{-7} A/cm^2 up to 3.5 MV/cm with a field and frequency independent C_i = 81 ± 1 nF/cm^2. Al_2O_3(ALD)/*a*-IGZO TFTs operate in enhancement mode with high μ_{FE} of 8 ± 1 cm^2/Vs, low V_T of 0.4 ± 0.1 V at 5

V, and $I_{on\text{-}off}$ of 6×10^7. The very small S of 0.1 ± 0.01 V/decade yield very small subgap DOS and allow very low operating voltages. Moreover, with R_cW = 25 Ω–cm at 5 V, much smaller than $R_{ch}W$, μ_{FE} is channel–length independent and does not limit the transconductance, potentially allowing TFTs capable of low power operation up to frequencies around 7.8 MHz.

3.3 Active matrix organic light-emitting diode backplane circuit

This study was conducted to develop active matrix organic light-emitting diode (AMOLED) backplane circuit based on *n*-channel *a*-IGZO TFTs. The potential for thin, light-weight, and low-power displays continues to drive the interest for the development of flexible AMOLED displays. Flexible thin-film transistors (TFTs) are of great interest because they are a key component for the development of such technologies. AMOLED displays have been demonstrated using both organic and amorphous silicon TFTs on flexible substrates [103-106]. However, their low mobility ~1 cm^2/Vs, which may not be sufficient to drive large area OLED displays, and/or their environmental stability and reliability continue to be areas of concern [107, 108]. Using *a*-IGZO with 200 nm thick SiO_2 as gate dielectric, a conventional two transistor and one capacitor (2Tr-1C) AMOLED display driver circuit has been demonstrated with a frame frequency of 240 Hz [109]. In this case, the "thick" gate dielectric requires high operating voltages (> 10 V). However, for circuit applications, such as AMOLED displays, inverters, and ring oscillators, low-voltage operation is desirable to reduce power consumption.

3.3.1 Experimental details

In this work, we demonstrated an AMOLED display driver circuit driven by a-IGZO channel TFTs. A 30 nm-thick layer of Al_2O_3 deposited by electron-beam (e-beam) as a gate dielectric was used for the TFTs. The detailed structure of the TFTs is shown in Figure 3.7(a) and the TFTs were fabricated with a bottom gate and with top-contact source and drain electrodes.

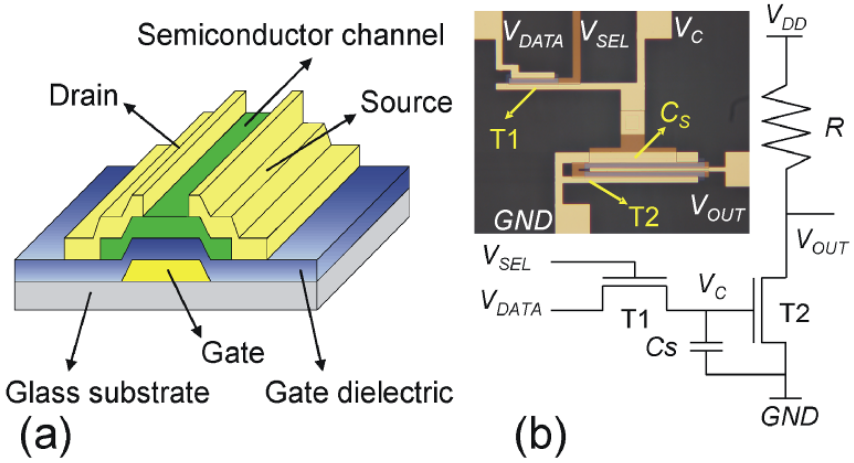

Figure 3.7: (a) Schematic cross section of the sputtered a-IGZO TFT on glass substrate with bottom gate and top contact. (b) Schematic and photograph of the simple 2Tr-1C pixel driver circuit for active-matrix OLED display. The switching TFT (T1), driving TFT (T2), and storage capacitor (*Cs*) are designed with *W/L* = 200 μm/20 μm, *W/L* = 1000 μm/20 μm, and a capacitance of 36 pF.

The AMOLED pixel driver circuit used two transistors and a capacitor (2Tr-1C) configuration, as shown in Figure 3.7(b). The circuit was fabricated using the following procedure: first a tri-layer Ti(6nm)/Au(50nm)/Ti(6nm) was deposited using electron-beam (e-beam) at room temperature on a glass substrate (Corning 1737) and patterned by

photolithography and lift-off processes; then, an Al_2O_3 layer (30 nm thick) was deposited by e-beam on the substrate to act as the gate dielectric, and contact holes were formed by a lift-off process; a 40 nm-thick active layer of a-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) was then deposited by RF sputtering, without intentional heating of the substrate, using a power of 125 W, a working pressure of 5 mTorr, and an O_2/Ar (1/10) atmosphere. After deposition of the a-IGZO layer, the device was annealed at 325 °C for 30 minutes in air and patterned by wet-etching process using hydrochloric acid (HCl) diluted in DI water (HCl:DI = 1:100). Another bilayer of Ti (6 nm)/Au (120 nm) was then deposited by e-beam and patterned by lift-off process to form the source and drain electrodes and the interlayer connections. This defined a $L_{overlap}$ (5 μm) × W overlap area between the source (drain) and the gate electrodes. The area and capacitance of the storage capacitor (Cs) were 400×50 μm^2 and 36 pF (180 nF/cm^2), respectively. A picture of the fabricated circuit is shown in the inset of Figure 8(b).

3.3.2 Electrical characterization

Figure 3.8 shows the measured transfer and output characteristics of the single TFTs with the same channel length (L= 20 μm) and different channel widths (W = 200 μm and 1000 μm). The TFTs exhibited n-channel transistor behavior with saturation mobilities of 4.5±0.5 cm^2/Vs, operating in the enhancement mode and showed excellent sub-threshold slopes of 0.09±0.01 V/decade at a voltage of 3.5 V. These small subthreshold slopes are consistent with those obtained in IGZO-TFTs that show a very small contact resistance [89, 92]. Small S value is desirable to achieve high-speed and low-voltage operation TFTs.

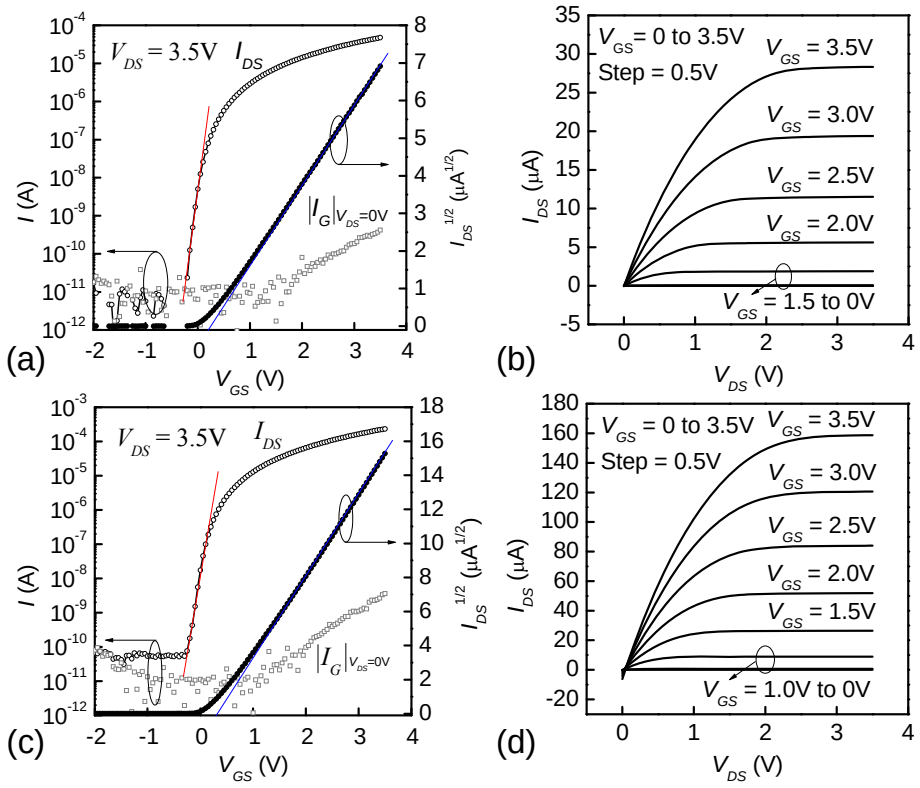

Figure 3.8: Transfer and output characteristics of a-IGZO TFTs with L = 20 μm, and W = 200 μm (a) and (b); and with L = 20 μm, and W = 1000 μm (c) and (d). The leakage current on both TFTs at V_{DS} = 0 is shown in (a) and (c).

A comparison of the both TFT electrical parameters is shown in Table 3.1. Despite the small thickness of the gate dielectric, as shown in Figure 3.8, small leakage currents below 3.7 $\times 10^{-8}$ A (<1.3 $\times 10^{-5}$ A/cm^2) were measured on both TFTs.

Table 3.1 Summary of the extracted parameters for n-channel a-IGZO thin film transistors based on 30nm thick Al_2O_3 gate dielectric material. W/L, channel width/channel length; μ_{SAT}, saturation mobility; V_T, threshold voltage; V_{ON}, turn-on voltage; S, sub-threshold slope; $I_{ON/OFF}$, on-off current ratio.

V_{DS} = 3.5 V, V_{GS} = -2 V to 3.5 V	μ_{SAT} (cm^2/Vs)	V_T (V)	V_{ON} (V)	S (V/decade)	$I_{ON/OFF}$
W/L =1000 μm /20 μm	4.5	0.3	-0.2	0.09	1.0×10^7
W/L =200 μm /20 μm	4.3	0.3	-0.2	0.09	2.0×10^6

The switching TFT (T1) and driving TFT (T2) designed to have W/L = 200 μm/20 μm and W/L = 1000 μm/20 μm, respectively, as components of the AMOLED pixel driver circuit are shown in Figure 3.7. The positive threshold voltages of TFTs (T1, T2) allow the TFTs to be operated in the enhancement mode using only positive voltage control signals. The pixel driver circuit works as follows: a signal voltage (V_{SEL}) is applied to T1 to control writing and holding of the data signal voltage (V_{DATA}) into C_S. Then, V_{DATA} is applied to T2 and stored in Cs. After switching off V_{SEL}, Cs maintains the gate voltage required for T2 to provide a constant current to drive the OLED to the desired brightness. An important property of the circuit is its ability to hold the programmed V_{DATA} through the frame time. To test the storage ability of the AMOLED driver circuit, we connected an external load resistor (R) in place of the OLED and measured the drain voltage of T2. A resistor of R = 100 kΩ at V_{DD} = 3.5 V, was selected to test the output characteristics of in-circuit T2. The value of V_{SEL} = 3.5 V, was selected to allow T1 to be operated either in the linear or saturation regions using the high value of the data signal input, V_{DATA} = 2.5 V (On state: $V_{SEL} - V_{DATA} = 1V > V_T$). With a V_{DD} (supply voltage of T2) of 3.5 V, pulse signals were applied to V_{DATA} (0 V – 2.5 V, 60 Hz, duty cycle of 50 %) and V_{SEL} (0 V –

3.5 V, 120 Hz, duty cycle of 12.5 %), yielding a modulation of 60 Hz at the resistor *R*, as shown in Figure 3.9.

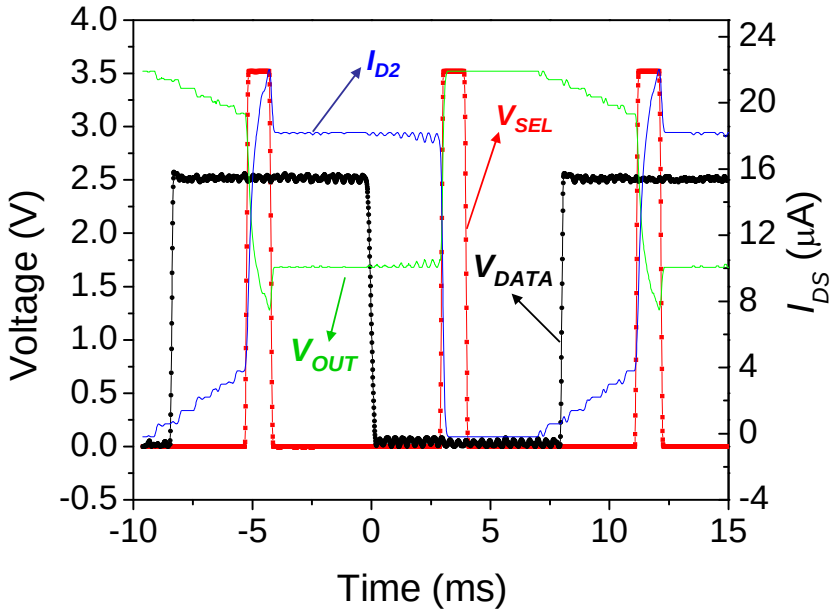

Figure 3.9: Driving control signals (V_{DATA}: 0 V to +2.5 V, duty 50%, 60 Hz, V_{SEL}: 0 V to 3.5 V, duty 12.5 %, 120 Hz) applied to the a-IGZO TFT driving circuit. Measured output voltage (V_{OUT}) and current (I_{D2}) from an external load resistor (R = 100 kΩ) connected to the drain of driving TFT (T2) and supply voltage (V_{DD}).

The C_S successfully holds the gate voltage to get a nearly constant output current around 18 μA. Only small variations (0.3 μA) of the output current at V_{DATA} = 2.5 V were observed meaning that the leakage currents through the dielectric layers connected to the gate electrode of T2 were negligible. The output current (~18 μA) of the in-circuit driving TFT with the load

resistor (R = 100 kΩ) was smaller than that (~80 μA) of the same size single TFT due to low V_{DS} (~1.7 V) and threshold voltage degradation during operation. For a top emissive AMOLED display, at least 1 μA is required to drive RGB pixel with an area of 370×123×3 μm^2 [110, 111]. Despite the large width of the TFTs in our driving circuit, even if W is reduced 10 times to fit realistic pixel area, such circuit could provide enough current (~1.8 μA) to drive an AMOLED display like the one described in Ref. [110, 111]. When V_{DATA} = 0 V, only the leakage through the gate-to-drain dielectric in T2, most likely due to the large gate-to-drain overlap area ($W \times L_{overlap}$ = 1000 μm × 5 μm) on T2, contributes to an increase of the gate voltage in T2 and consequently a decrease in V_{OUT}. However, this small variation should not significantly affect the brightness of an OLED connected to this circuit, because the time averaged changes in the output current are small and the high value of OLED resistance at low voltage may decrease the leakage currents. The use of atomic layer deposition to deposit the gate dielectric should lead to significant reduction of the leakage currents and its parasitic effects on the circuit performance [100].

3.3.3 Summary

In summary, we have demonstrated a low-voltage 2Tr-1C pixel driver circuit for AMOLED display driven by high performance enhancement mode a-IGZO channel thin film transistors. Low-voltage operation for the pixel driver circuit was achieved by using a 30 nm-thick electron-beam deposited Al_2O_3 as a gate dielectric material. With high gate dielectric capacitance density of 180 nF/cm^2, the TFTs showed large saturation mobility values of 4.5±0.5 cm^2/Vs, excellent sub-threshold slopes of 0.09±0.01 V/decade, low threshold voltages of

0.5±0.2 V, and high on-off current ratios of above 10^6 at a voltage of 3.5 V. While further optimization is possible, the data presented shows the potential of IGZO-based transistors to develop low voltage and high frequency driving circuits for AMOLED displays.

CHAPTER 4 ORGANIC-INORGANIC HYBRID COMPLEMENTARY CIRCUITS

In chapter 3, we reported on high performance *n*-channel a-IGZO TFTs with high-*k* and/or thin insulators as gate dielectric layers. Here, we reported on high performance organic-inorganic hybrid complementary inverters based on high mobility *n*-channel *a*-IGZO and *p*-channel pentacene TFTs on flexible substrates. All-organic or organic-inorganic hybrid TFTs have the potential to lead to a generation of low cost complementary circuits, processed at low-temperatures on flexible substrates. This work involves the integration of *n*-channel *a*-IGZO and *p*-channel pentacene TFTs into complementary inverters. Achieving balanced *on*-currents is particularly important for the realization of high performance complementary circuits. The differences in electron and hole mobilities, and threshold voltages, will be compensated by resizing the width (W) of the *n*- and *p*-channel layers, optimization of fabrication processes, and proper selection of gate dielectrics. Organic or oxide thin-film transistor (TFT)-based electronic components such as inverters and logic circuits are attractive because they can be processed at low-temperature, into large-area and flexible substrates. Generally, practical electronic devices are expected to use *p*- and *n*-channel TFTs-based complementary inverters to operate with low power consumption, high gain values, and high and balanced noise margins. To do this, the *p*- and *n*-channel TFTs should yield comparable output characteristics despite of differences in the materials used to achieve such performance. The static gain is commonly used to evaluate the performance of a complementary inverter. Although noise margins (noise margin low and noise margin high) are not commonly reported, the importance of achieving balanced noise margins

cannot be underscored. Logic circuits comprise chains of complementary inverters where high and balance noise margins are required because they limit the signal regeneration property of an inverter. In other words, they limit the range of input values that will produce an acceptable logic output for the next inverter in the chain. To achieve balanced and high noise margins, complementary inverters should operate at a supply voltage that yields a switching threshold voltage that is half of its value. The supply voltage that realizes such condition should be used to evaluate the performance of a complementary inverter.

4.1 Introduction

4.1.1 Operation and characterization of a static complementary MOS inverter

Complementary MOS inverter has two important advantages. The first and perhaps the most important advantage is that the steady-state power dissipation is virtually negligible, except for small power dissipation due to the leakage currents. The other advantages are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD}, and that the VTC transition is usually very sharp. To realize balanced complementary inverters, we need to understand some important performance parameters such as noise margin and inverter threshold voltage with the inverter operation [77, 78].

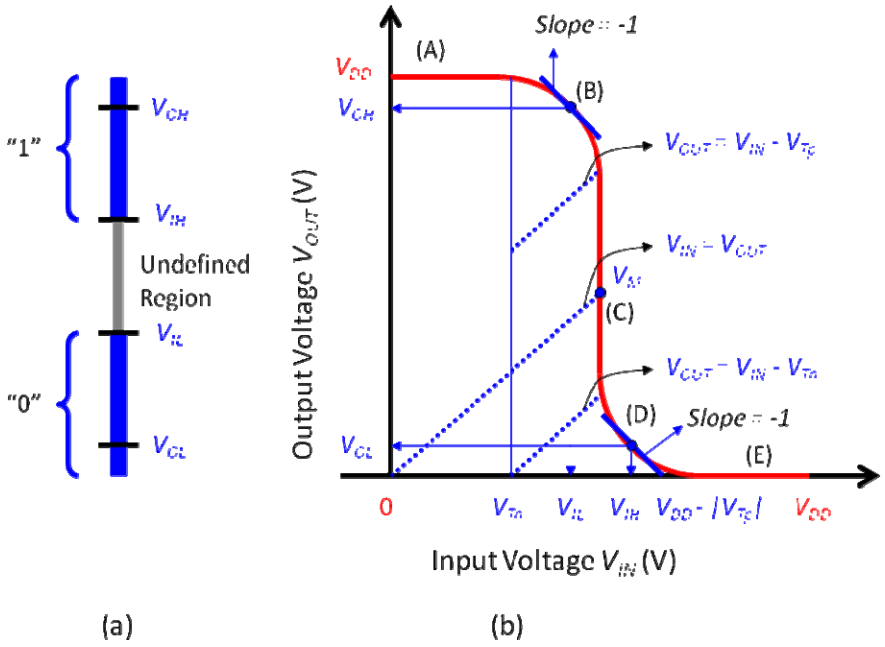

Figure 4.1: (a) Relationship between voltage and logic levels; (b) Voltage transfer characteristic of inverters.

Figure 4.1(a) illustrates how a logic level is represented in reality by a range of acceptable voltages, separated by a region of uncertainty, rather than by normal levels alone. The regions for acceptable high and low voltages are delimited by the V_{IH} and V_{IL} voltage levels, respectively. A typical voltage transfer characteristic (VTC) of CMOS inverters is shown in Figure 4.1(b). The V_{IH} and V_{IL} represent by definition the points where the slope (= dV_{OUT}/dV_{IN}) of the VTC equals -1 as shown in Figure 4.1(b). The region between V_{IH} and V_{IL} is called the undefined region. Steady-state signals should avoid this region if proper circuit operation is to be ensured. The VTC of a CMOS inverter plots the output voltage (V_{out}) as a function of the input voltage (V_{in}). Here, we identify five distinct regions, labeled (A) through (E), each

corresponding to a different set of operating conditions. Table 4.1 lists these regions and the corresponding critical input and output voltage levels.

Table 4.1: Operating regions of CMOS inverters.

Region	V_{IN}	V_{OUT}	nMOS	pMOS
(A)	$< V_{Tn}$	V_{OH}	Cut-off	Linear
(B)	V_{IL}	High $\approx V_{OH}$	Saturation	Linear
(C)	V_M	V_M	Saturation	Saturation
(D)	V_{IH}	Low $\approx V_{OL}$	Linear	Saturation
(E)	$> (V_{DD}+V_{Tp})$	V_{OL}	Linear	Cut-off

For a gate to be robust and insensitive to noise disturbances, it is essential that the "0" and "1" intervals be as large as possible. A measure of the sensitivity of a gate to noise is given by the noise margin NM_L (noise margin low) and NM_H (noise margin high), which are defined for low and high input levels using the following equations, respectively:

$$NM_L = V_{IL} - V_{OL} \qquad \text{Eq. (4.1)}$$

$$NM_H = V_{OH} - V_{IH} \qquad \text{Eq. (4.2)}$$

Noise margins represent the levels of noise that can be sustained when gates are cascaded as illustrated in Figure 4.2. It is obvious that the margins should be larger than 0 for a digital circuit to be functional and should be as large as possible.

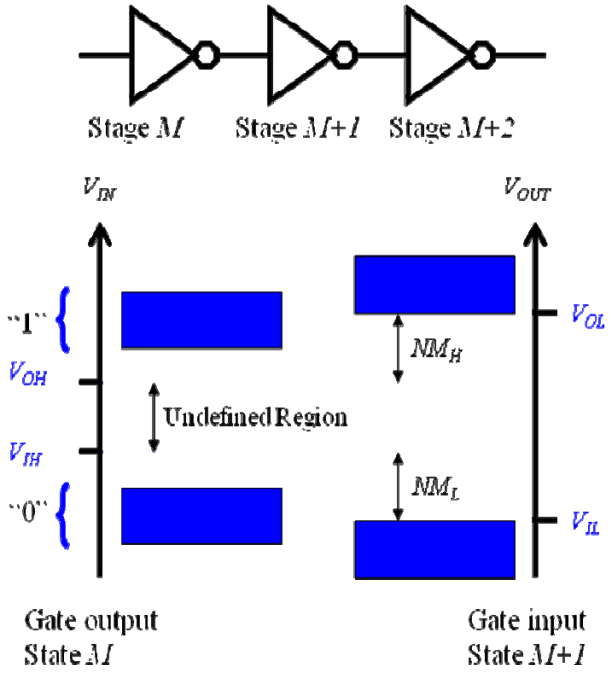

Figure 4.2: Cascaded inverter gates: definition of noise margins.

In a CMOS inverter operating in steady-state, the drain current of the NMOS transistor is always equal to the drain current of the PMOS transistor. The inverter threshold voltage, V_M, is defined as the point where $V_{IN} = V_{OUT}$. Since the CMOS inverter exhibits large noise margins and a very sharp VTC transition, the inverter threshold voltage emerges as an important parameter characterizing the static performance of the inverter. As shown in Figure 4.1(b), a

switching threshold voltage (V_M) can be obtained graphically from the intersection of VTC with the line given by $V_{IN} = V_{OUT}$. In this region, both PMOS and NMOS are saturated, and the expression of V_M is obtained by equating the currents through the transistors.

$$\frac{k_n}{2}(V_M - V_{Tn})^2 = \frac{k_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2 \qquad \text{Eq. (4.3)}$$

which yields

$$V_M = \frac{r(V_{DD} - |V_{Tp}| + V_{Tn})}{1+r} \quad with \quad r = \sqrt{\frac{k_p}{k_n}} \qquad \text{Eq. (4.4)}$$

$$k_n = \mu_n C_i \frac{W_n}{L_n} \qquad \text{Eq. (4.5)}$$

$$k_p = \mu_p C_i \frac{W_p}{L_p} \qquad \text{Eq. (4.6)}$$

where V_{Tn}, k_n ,μ_n ,W_n/L_n and V_{Tp}, k_p ,μ_p , W_n/L_p are the threshold voltage, current gain factor, the mobility, and the width-length ratio in the NMOS and PMOS transistors, respectively, and C_i is the capacitance density of the gate insulator.

This leads to the conclusion that V_M is situated in the middle of the available voltage swing (or $V_{DD}/2$) when $k_n = k_p$ (assuming that the threshold voltages of the PMOS and NMOS transistors are comparable). Note that if the threshold voltage values of *n*- and *p*-channel TFTs are different, it is necessary to adjust the k_p/k_n ratio to maximize the noise margins and obtain symmetrical VTC characteristics. The effect of changing the k_p/k_n ratio is to shift the transient region of the VTC. Increasing the width of the *p*-channel transistor or the *n*-channel transistor moves V_M towards V_{DD} or ground, respectively. The signal gain of the inverters equals the gain

at the switching threshold V_M. A high gain in the transition region is very desirable. The dc gain can be easily extracted from the VTC curve by calculating the derivative of V_{OUT} over V_{IN}. The gain mainly depends on transconductances of *n*- and *p*- channel TFTs at the midpoint voltage of the inverter. The static CMOS inverter can also be used as an analog amplifier, as it has a high gain in its transition region. This region should be very narrow. The highest dc gain corresponds to the switching threshold voltage.

4.2 Organic-inorganic hybrid complementary inverters

4.2.1 Introduction

Complementary inverters have been realized with organic TFTs on flexible substrates [42, 112]. Using *p*-channel pentacene and *n*-channel C_{60} TFTs, all-organic complementary inverters achieve high performance with a static gain of 180 V/V and balanced noise margins of 80 % of their theoretical maximum [112]. However, C_{60} is known to be sensitive to oxygen, moisture and requires the use of low work-function metals, which are reactive and oxidize instantly in air [4]. In contrast, *n*-channel oxide semiconductors, such as ZnO [9] and amorphous InGaZnO (*a*-IGZO) [25], do not require low work function metals, have better air stability and higher mobility values than their organic counterparts. Oxide semiconductors also can be processed at low temperatures and are compatible with flexible substrates. Therefore, they are an attractive alternative to electron transport organic semiconductors for the realization of hybrid circuits based on complementary metal-oxide semiconductor technology. To date, there are only few reports of hybrid complementary circuits [113-115]. On flexible substrates, Oh *et al* [113] recently demonstrated complementary inverters on polyethersulfone

(PES) substrates using ZnO and pentacene channels with the same aspect ratio. Following this hybrid approach, these inverters showed the highest reported static gain of 100 V/V at a switching threshold voltage of 5 V with a supply voltage of 7 V. Although not provided in the paper, unbalanced noise margins can be expected in such inverters. Furthermore, ZnO films are polycrystalline even when deposited at room temperature, leading to channels with grain boundaries that deteriorate the TFT stability, uniformity[116]. On the other hand, pentacene/*a*-IGZO complementary inverters only have been reported on rigid substrates [114] with gains of 56 V/V with supply voltage of 7 V but at a switching threshold voltage of 2.8 V. Unbalanced noise margins can also be expected in that case.

In this work, we report on hybrid pentacene/*a*-IGZO complementary inverters composed of TFTs with different channel aspect ratios fabricated on flexible PES substrates. We propose a method to find the switching threshold voltage based on the resistance of the *p*- and *n*-channel TFTs, discuss the conditions for an optimum supply voltage, and propose a method for its estimation.

4.2.2 Experimental details

Complementary organic-inorganic hybrid inverters were fabricated with a bottom gate and top-contact source and drain electrode geometry, as shown in Fig. 4.3(a). First, a tri-layer of Ti (7 nm)/Au (70 nm)/Ti (7 nm) was deposited using electron-beam (e-beam) at room temperature on flexible PES substrates (*i*-components) through a shadow mask. A 300 nm-thick Si_3N_4 gate dielectric layer was deposited by PECVD at 180 °C. A 30 nm-thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) active layer was then deposited by rf sputtering at a

temperature of 90 °C using a power of 125 W, a working pressure of 6 mTorr, and an O_2/Ar (1/20) atmosphere using a shadow mask. Then, a 50 nm-thick layer of pentacene was deposited using thermal evaporation with a substrate temperature of 25 °C and an initial pressure of 2 x 10^{-8} Torr. Prior to thermal evaporation, pentacene was purified using gradient zone sublimation. Finally, Au (25 nm)/Al (25 nm) source/drain electrodes were deposited through a shadow mask over the pentacene and *a*-IGZO channels.

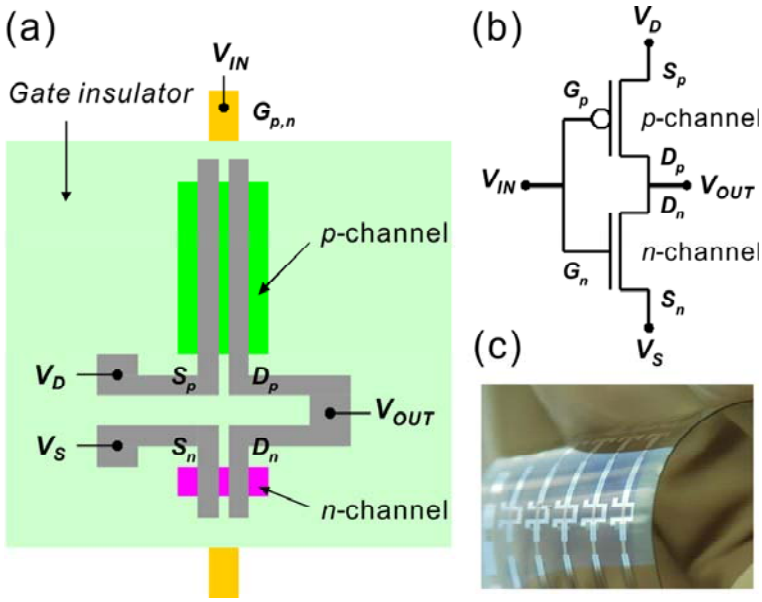

Figure 4.3: (a) Schematics of the hybrid complementary inverter fabricated on a PES substrate with pentacene and *a*-IGZO as active channel layers. (b) Complementary inverter circuit diagram. (c) Photograph of complementary inverters on PES.

Complementary inverter circuits, as shown in Fig. 4.3(b), were constructed using *p*-channel pentacene and *n*-channel *a*-IGZO TFTs with a channel length of L = 180 µm and

channel widths of W^p = 4000 μm and W^n = 400 μm, respectively. A picture of the flexible inverters is shown in Fig. 4.3(c). The use of Au source/drain electrodes is expected to yield balanced electron and hole injection since, in both cases, the energy barrier for charge injection is ~ 0.6 eV [117, 118]. The channel width ratio of W^n / W^p = 10, was selected to compensate for: 1) differences in electron and hole mobility; and 2) differences in the threshold voltage. The gate electrodes were patterned for both TFTs and served as the input voltage (V_{IN}) of the inverter circuit.

4.2.3 Electrical characterization

The current-voltage characteristics of independent *p*-channel and *n*-channel TFTs, fabricated on the same substrate with the same channel aspect ratio as those used in the complementary inverter, are shown in Figs 4.4(a)-(d). The transfer and output characteristics of all TFTs were measured using an Agilent E5272A medium-power source/monitor unit connected to a probe station. The transfer curves and leakage currents measured for both forward and reverse gate biases are shown in Fig. 4.4(a) (*p*-channel) and Fig. 4.4(b) (*n*-channel). A saturation mobility of 0.13 cm^2/Vs and a threshold voltage of -10.3 V were obtained for pentacene TFTs. These values are comparable with the ones found in pentacene/Si_3N_4 TFTs on rigid substrates [119]. The small hysteresis in these TFTs, also found on rigid substrates, is due to a shift in the threshold voltage which is attributed to trapping at the pentacene/Si_3N_4 interface. The use of passivation layers is expected to significantly improve the hysteresis characteristics of these pentacene TFTs [112] without significantly affecting the properties of the *a*-IGZO

channel. The *n*- channel *a*-IGZO TFT shows a saturation mobility of 3.8 cm^2/Vs and a threshold voltage of 13.6 V with negligible hysteresis.

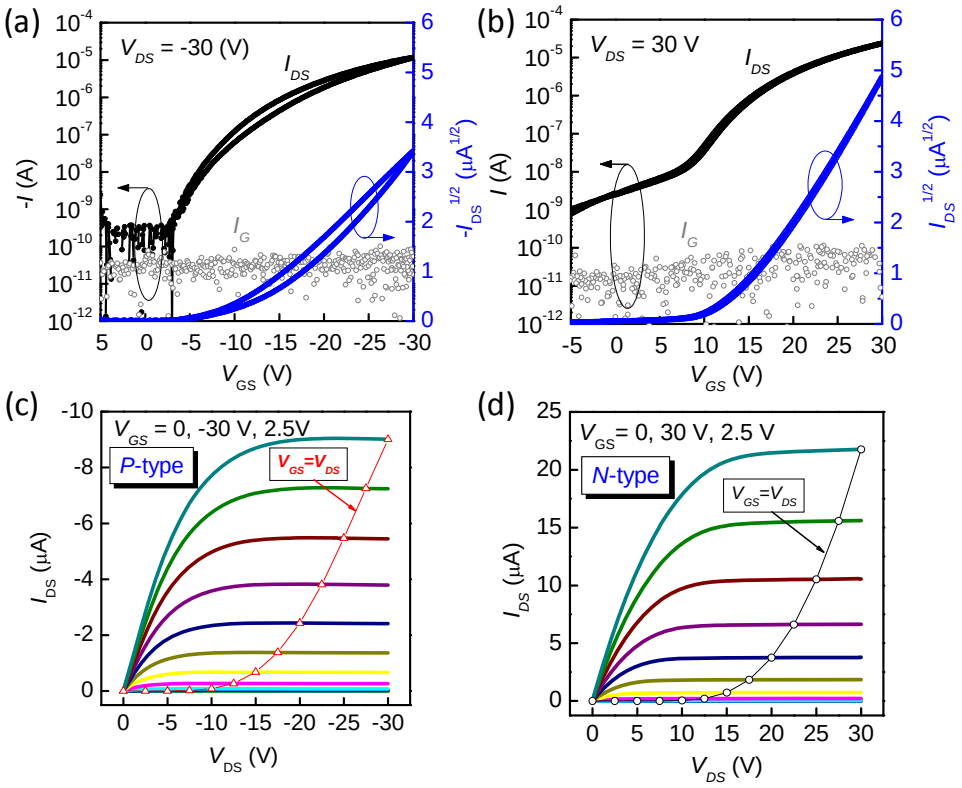

Figure 4.4: (a) Representative (a) hysteresis transfer and (c) output characteristics of pentacene TFTs with L = 180 µm and W^p = 4000 µm. Representative (b) hysteresis transfer and (d) output characteristics of *a*-IGZO TFTs with L = 180 µm and W^n = 400 µm.

On rigid substrates, higher mobility values have been obtained because differences in processing conditions are expected to yield *a*-IGZO films with a slightly different stoichiometry than previously obtained. Higher mobility values are expected upon further optimization of the

deposition process. The output curves shown in Fig. 4.4(c) (*p*-channel) and Fig. 4.4(d) (*n*-channel) exhibit good linearity at low drain-to-source voltage (V_{DS}) despite the relatively large energy barrier for charge injection. A comparison of the both TFT electrical parameters is shown in Table 4.2.

Table 4.2: Summary of the extracted parameters for *p*-channel pentacene and *n*-channel a-IGZO thin film transistors based on 300 nm thick SiN_x gate dielectric material. *W/L*, channel width/channel length; μ_{SAT}, saturation mobility; V_T, threshold voltage; $I_{on(MAX)}$, maximum drain-to-source current.

Semiconductors	V_{DS} (V)	V_{GS} (V)	*W/L* (μm/ μm)	μ_{SAT} (cm^2/Vs)	V_T (V)	$I_{on(MAX)}$ (A)
p-channel Pentacene	-30	0V to -30V	4000/180	0.15	-10.2	1.2×10^{-5}
n-channel InGaZnO	30	0V to 30V	400/180	3.8	13.6	2.4×10^{-5}

The static performance of an inverter is evaluated by its static gain and noise margin values. Achieving high and balanced noise margin values is necessary for reliable circuit operation in complex logic circuits such as ring oscillators. The noise margin, is limited by the steepness of the transition and by the position of the switching threshold voltage ($V_M = V_{IN} = V_{OUT}$). Highest values of noise margins are found when the ideal condition $V_M = 0.5V_D$ is met, hence when $V_M = V_{IN} = 0.5V_D = V_{OUT}$. However, the value of V_{IN} at which this transition occurs is generally not $0.5V_D$. The actual value of V_M depends on the range of V_D. A complementary inverter can be modeled by two series-connected voltage-dependent variable resistors. In general, for a given supply voltage, V_D, V_M corresponds to the input voltage that makes equal the resistance of the *n*-channel TFT ($R_{TN}=V_{DS}/I_{DS}$) and the *p*-channel TFT ($R_{TP}=-V_{DS}/-I_{DS}$). Note

that R_{TN} and R_{TP} can be extracted from independent TFTs either from the output characteristics through the condition $V_{GS} = V_{DS}$ (as shown in Figs. 4.4(c)-(d)), or by directly measuring I_{DS} in a TFT with shorted gate and drain electrodes ($V_{GS} = V_{DS}$).

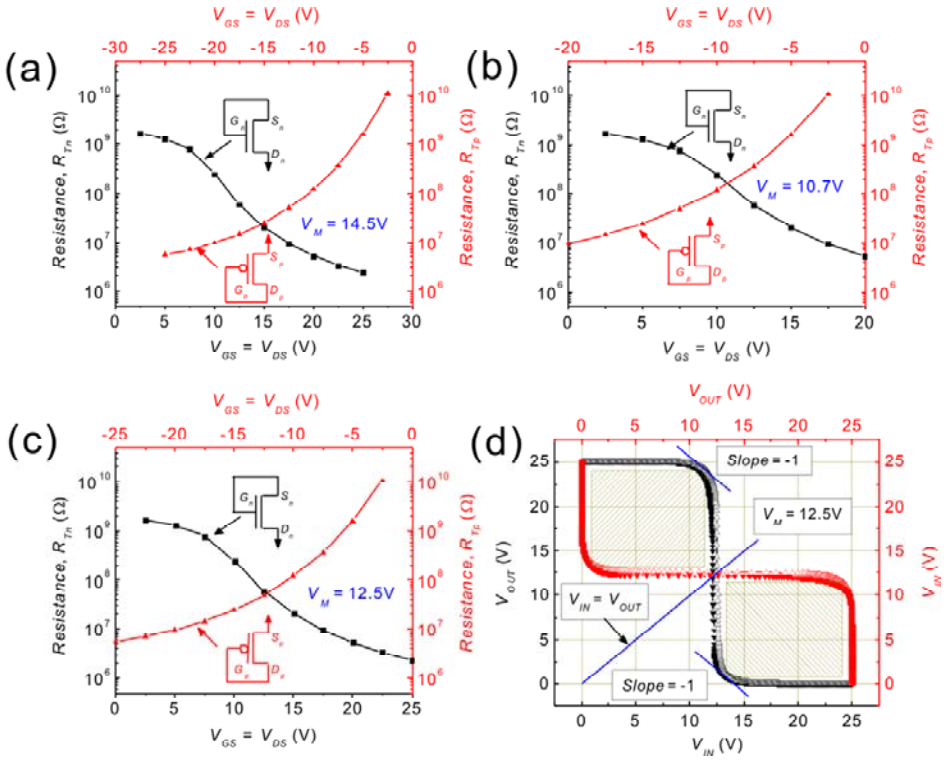

Figure 4.5: (a) Total resistance of pentacene *p*-channel and *a*-IGZO *n*-channel TFTs at $V_{GS} = V_{DS}$ by sweeping V_{GS} from (a) 0 V to ±30 V (positive for *n*-channel TFT, negative for *p*-channel TFT); (b) 0 V to ±20 V; and (c) 0 V to ±25 V (Insets show schematics of *n*- and *p*-channel TFT at $V_{GS} = V_{DS}$); (d) Bi-stable hysteresis voltage transfer characteristics at V_D = 25 V.

Figure 4.5 shows the values of R_{TN} and R_{TP}, extracted by following the first approach, for different values of $V_{GS} = V_{DS}$. Also note that the conventional analytical equation used to find V_M, derived from the MOSFET square law model, assumes that the mobility and threshold

voltage remain constant during operation [77, 84]. However, in organic or oxide TFTs, this analytical approach may not always hold true. An accurate calculation of V_M would require a fitting procedure to get the functional dependence of the mobility and threshold voltage as a function of V_{GS} and V_{DS}. In contrast, the proposed method does not require any fitting parameters, such as mobility or threshold voltage, and in principle requires just a pair of measurements of R_{TN} and R_{TP} as a function of $V_{GS} = V_{DS}$.

As mentioned earlier, to achieve balanced noise margins it is important to find the optimum value of V_D, such that $V_M = 0.5V_D$. To find the optimum range for V_D, a graphical solution is proposed as follows: 1) first, for a given range of $V_{DS} \in [0, \pm V_D]$ ($+V_D$ for the *n*-channel TFT and $-V_D$ for the *p*-channel TFT), the value of V_M is calculated as previously described; 2) if $V_M \neq 0.5V_D$ the range of V_{DS} needs to be adjusted. As shown in Fig. 4.5(a), if $V_M < 0.5V_D$, then V_D needs to be decreased and the procedure start over again until $V_M = 0.5V_D$ is found. Correspondingly, as shown in Fig. 4.5(b), if $V_M > 0.5V_D$, V_D needs to be increased and the procedure repeated until the condition $V_M = 0.5V_D$ is found. Figure 4.5(c) shows the values of R_{TN} and R_{TP} extracted following this procedure for $V_{DS} \in [0, \pm 25\text{V}]$, the range where $V_M = 0.5V_D = 12.5$ V. Figure 4.5(d) shows the measured bi-stable hysteresis voltage transfer characteristics at a supply voltage of $V_D = 25$ V. The cross-hatched rectangles, defined by the negative slope criteria [77, 84], are used to determine a graphical solution of the noise margins for a given inverter characteristic. At $V_D = 25$ V, the inverters show identical noise margin low (NM_L) and noise margin high (NM_H) of 10.5 V (84% of their theoretical maximum). These values are among the highest values obtained in organic, or hybrid inverters. Note that testing at different V_D values is not really necessary once the output characteristics are measured for a

large enough range of $V_{GS} = V_{DS}$. This is because the values of I_{DS} and consequently R_{TN} and R_{TP} can be interpolated from the output characteristics of the *n*-channel and *p*-channel TFTs. Therefore, the absolute value of the difference of R_{TN} and R_{TP}, $R_d = |R_{TN} - R_{TP}|$ can be estimated for arbitrary values of V_D. The value of V_M is given as the V_{GS}=V_{DS} value where R_d reaches a minimum value. If $V_M \neq 0.5V_D$, the range of the V_D can be adjusted numerically until the condition V_M=$0.5V_D$ is found as described before.

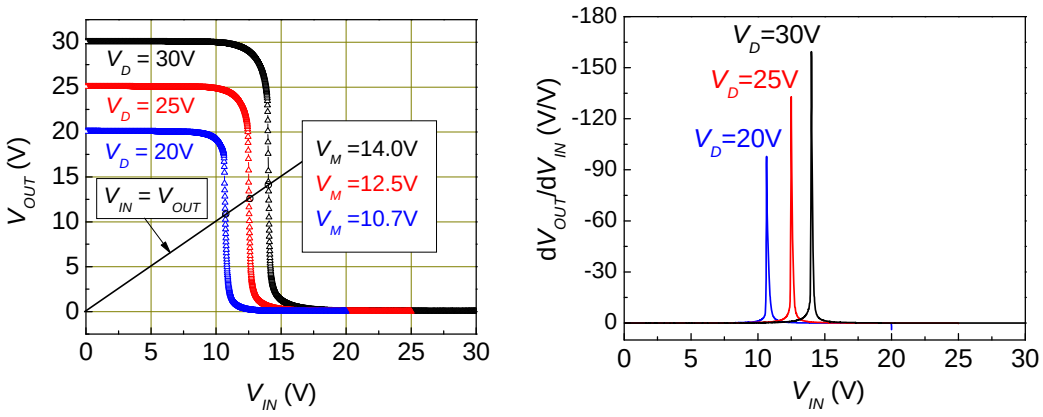

Figure 4.6 Voltage transfer characteristics and static gain of the hybrid complementary inverter.

Figure 4.6 shows the measured voltage transfer characteristics and static gain values of the inverter for V_D = 20, 25, and 30 V. The maximum static gain values for V_D = 20 and 30 V are -100 V/V at V_M =10.7 V and -165 V/V at V_M = 14.5 V, respectively. The corresponding values of NM_H and NM_L are 7.5 and 9.4 V for V_D = 20 V, and 13.9 and 11.4 V for V_D = 30 V. As expected from a shift of V_M from its optimum value, unbalanced noise margins are obtained

when $V_D \neq 25$ V. While higher gain values are obtained at larger V_D values, from a circuit operation perspective the best compromise is obtained when balanced noise margins are achieved. At the switching threshold voltage values, R_{TP}=R_{TN} are 164, 54.3, and 23.5 MΩ for V_D = 20, 25, and 30 V respectively. From these values we estimated a maximum dissipated power of 1.22, 5.76, and 19.1 μW for V_D = 20, 25 and 30 V, respectively.

4.2.4 Summary

In summary, we demonstrated organic-inorganic hybrid complementary inverters fabricated on flexible PES substrates that use *n*- and *p*-channel TFTs with channels having different aspect ratios to achieve high static gains and balanced high noise margins. With a Si_3N_4 gate dielectrics, *p*- and *n*- channel TFTs show saturation mobility values of 0.13 and 3.8 cm^2/Vs. We also proposed a new approach to find the switching threshold voltage and the optimum value of V_D to operate a complementary inverter. Using this method, we demonstrated hybrid inverters that achieve a very high gain of 130 V/V at V_D = 25 V with high and balanced noise margin values of 84% of their theoretical maximum. In contrast with previous analytical methods, the proposed method does not require fitting to any transistor model, can be implemented with a pair of measurements and should also be applicable to any complementary or complementary-like (one that uses ambipolar TFTs) inverter configuration.

CHAPTER 5 ORGANIC-INORGANIC AMBIPOLAR TFTS AND CIRCUITS

Here, we report on high performance ambipolar transistors and complementary circuits based on *n*-channel *a*-IGZO and *p*-channel pentacene hybrid geometry. The ambipolar TFTs (ATFTs) and inverters were fabricated using similar processes as described in Chapter 4, in a bottom-gate top-contact configuration. In this work, we propose a novel geometry to realize ambipolar TFTs that preserve the high electron and hole mobilities found in unipolar TFTs and, at the same time, produce balanced *p*- and *n*-channel operation. Therefore, we demonstrate that the proposed approach leads to hybrid ATFTs with high mobility and balanced *n*- and *p*- type operation and to high performance hybrid ambipolar inverter circuits on rigid or flexible substrates. On the other hand, six different regimes have been used to describe the operation of ATFTs by assuming a single threshold voltage for *n*- and *p*-type operation. These regimes are defined by the sign and relative magnitudes between the drain-source voltage and the difference between the gate-source voltage and the threshold voltage. However, assuming a single V_T is in general not a good approximation for two unipolar TFTs operating in parallel. In the most general case, the threshold voltage of the *n*-channel and *p*-channel can be expected to be different. We show that in this configuration, the number of regimes of operation of an ATFT are increasing from six [120] to eleven, and lead to ATFTs that achieve a high performance because the onset of operation for ambipolar behavior can be controlled. The implications of such change are better understood by reviewing the operation of an unipolar TFT under all bias

conditions. We define five different regimes different from conventional three regimes such as linear, saturation, and cut-off regimes for both *n*- and *p*-channel TFTs, respectively.

5.1 Introduction

5.1.1 Background

Ambipolar thin-film transistors (ATFTs) are attractive microelectronic devices because, unlike unipolar TFTs, they operate independently of the sign of the gate voltage [53, 54]. When used in complementary digital circuit configurations, this intrinsic characteristic of an ATFT can simplify circuit design by reducing the number of control lines and by enable circuits with multifunctional operation. For instance, a single digital circuit operating as a logic gate can adaptively operate like two logic gates (i.e. NOR and NAND) depending upon the polarity of the input voltages [52]. So far, ATFTs have been realized following different approaches, categorized into three major groups with respect to their geometry [55]: (i) a single layer of a neat semiconductor that can transport both holes and electrons; (ii) a blend of two semiconductors; or (iii) a bilayer of two vertically stacked semiconductors. The device architecture of these ATFTs is shown in Figure 5.1(a)-(c) for a top electrode geometry.

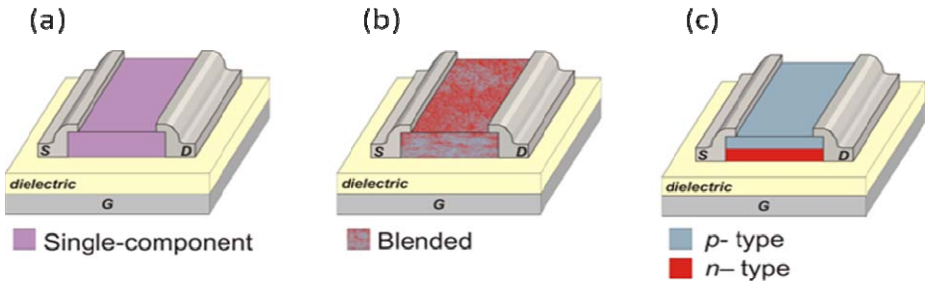

Figure 5.1: Conventional structures of ambipolar TFTs: (a), (b), and (c).

Each approach presents challenges and offers advantages that have previously been discussed [55]. However, compared with their unipolar counterparts, all of these geometries typically yield ATFTs with degraded electrical properties due to either unbalanced hole/electron charge injection [54, 55] or to the existence of a *pn*-heterojunction [53, 62]. Achieving balanced injection into single-component or blended semiconductors, and subsequently balanced transport characteristics, remains one of the biggest challenge to realize high performance ATFTs [55, 56]. On the other hand, material approaches having *pn*-heterojunctions with a large surface area could increase scattering processes that severely impair charge transport and ultimately lead to ATFTs with degraded performance [54, 62, 121]. For instance, transport in organic semiconductors is particularly susceptible to energetic and/or positional disorder in the bulk and at the critical interfaces of a ATFT [53, 56]. Hence, blended or bilayer all-organic ATFTs typically yield lower mobilities than those obtained in their unipolar counterparts and suffer from charge trapping and contact resistance effects [54, 69].

ATFTs that achieve a performance similar to that of unipolar TFTs will be necessary if ambipolar circuits are to be realized. Furthermore, from a digital circuit perspective, balanced electron and hole currents are desirable to enable useful complementary-like circuits. In previous ATFT geometries, with a shared channel aspect ratio, this requirement leads to the stringent condition of finding a material or material combination with matched electron and hole mobilities. This condition also constitutes a major barrier for the realization of high performance ATFTs and complementary-like circuits that use a hybrid inorganic/organic approach. Hybrid TFTs approaches, could lead to either complementary or complementary-like

circuits that have higher mobility and better air-stability than their all-organic counterparts. For instance, oxide semiconductors, such as ZnO and amorphous-IGZO (*a*-IGZO), are very attractive the realization of thin-film transistor technologies because they can be processed at low temperatures on flexible substrates and have better electron mobilities and ambient shelf stability than its organic counterparts [25, 122]. Amorphous-IGZO is particularly attractive as an alternative to *n*-type organic materials because despite being amorphous, the isotropic nature of the metal *s* orbitals constituting the bottom of its conduction band yield a high electron mobility (10 cm^2/Vs) [25, 33]. Because *p*-type oxide semiconductors that match the electrical performance and low processing temperatures of their *n*-type counterparts are proving difficult to realize [38], oxide semiconductor-based ATFTs and their complementary-like circuits so far rely on the use of hybrid structures with semiconductor channels vertically distributed (Fig. 5.1(c)). Pentacene has been commonly used as hole transporting material, because of its relatively large hole mobility, in the range of 0.1 to 1 cm^2/Vs when processed at low temperatures. Hybrid ATFTs that use pentacene and oxide semiconductors with vertically distributed channels have recently been demonstrated [68, 71]. However, they either show balanced mobilities during *n*-type and *p*-type operation, $\mu_{n\text{-}op}$, $\mu_{p\text{-}op}$ respectively, with low values in the range of 10^{-2} cm^2/Vs, [68, 71] or when higher values have been reported ($\mu_{n\text{-}op}$ = 13.6 cm^2/Vs and $\mu_{p\text{-}op}$ = 0.16 cm^2/Vs), the expected differences in material properties lead to unbalanced ATFT operation [70]. Therefore, hybrid ambipolar inverters have yielded low gain values at high operating voltages (gain of 12 V/V at 100 V) [68]. Even with an all-organic approach, ATFT-based complementary-like inverters so far yield gain values below 20 V/V at operating voltages typically above 60 V [40, 54, 64-66].

5.1.2 Operation modes of ambipolar transistors

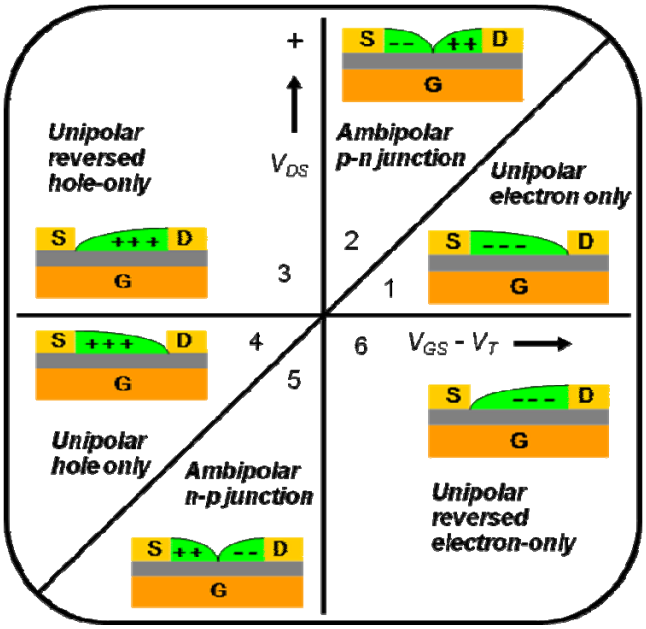

Figure 5.2: A sketch of all operating regimes for the conventional ambipolar TFTs as a function of drain and gate biasing in the channel.

In general, six different regimes have been used to describe the operation of an ATFTs by assuming a single threshold voltage for *n*- and *p*-type operation as shown in Figure 5.2 [60]. These regimes are defined by the sign and relative magnitudes between the drain-source voltage and the difference between the gate-source voltage and the threshold voltage. For $|V_{GS} - V_T| > |V_{DS}|$ with V_{DS} and V_{GS} having the same sign, unipolar transport occurs. For $V_{GS} - V_T > 0$, electron accumulation in the channel leads to current flowing in the *n*-type channel layer while, in principle, no current flows through the *p*-type layer. Correspondingly, for negative $V_{GS} - V_T$,

holes accumulated in the channel lead to a current flow in the p-type channel layer while the n-type layer remains off. When $|V_{DS}|=|V_{GS}-V_T|$, the effective gate potential at the drain is zero and the channel becomes pinched. If now $V_{DS} > V_{GS}-V_T > 0$ the effective gate potential becomes negative at the drain, increasing the pinch-off region in the *n*-type channel, hence making it operate in saturation, while forcing mobile holes to accumulate towards the drain electrode on the *p*-type layer, making it also operate in saturation. The opposite situation holds true when $V_{DS} < V_{GS}-V_T < 0$. Therefore, when $|V_{DS}|>|V_{GS}-V_T|$ a sign inversion in the effective gate potential yields ambipolar transport and both channels of the TFT operating in saturation. Note that if V_{DS} has opposite sign with respect to $V_{GS}-V_T$ the transistor operates as a unipolar TFT, with source and drain inverted. In both p- and n-type operations, high on-off current ratios at low V_{DS} are possible. At higher V_{DS} contribution of "opposite" sign carriers in the unipolar region in the off-region, where $V_{GS}-V_T$ and V_{DS} have opposite sign, significantly decrease the on-off current ratios. Their ability to operate at both positive and negative V_{GS}, makes possible to build complementary circuits that with the same number of TFTs, operate in one more quadrant than their unipolar counterparts.

5.1.3 Operation modes of ambipolar TFT-based inverters

In the inverter circuit, the gate is common for both ambipolar TFTs and serves as the input voltage (V_{IN}). Figure 5.4(a) shows the voltage transfer characteristics (VTCs) and DC gain of the inverter with a positive voltage of V_D and a ground of V_S, corresponding to the circuit schematic in Figure 5.3(a). Here, T_{AMB1} and T_{AMB2} show *p*- and *n*-channel operations, respectively. The switching voltage (V_M) was obtained graphically from the intersection of the

VTC with the line V_{IN}=V_{OUT} (V_{OUT} denotes output voltage). Due to a mismatch in threshold voltage and mobility during *p*- and *n*-channel operations V_M can be shifted from its theoretical value of 0.5V_D.

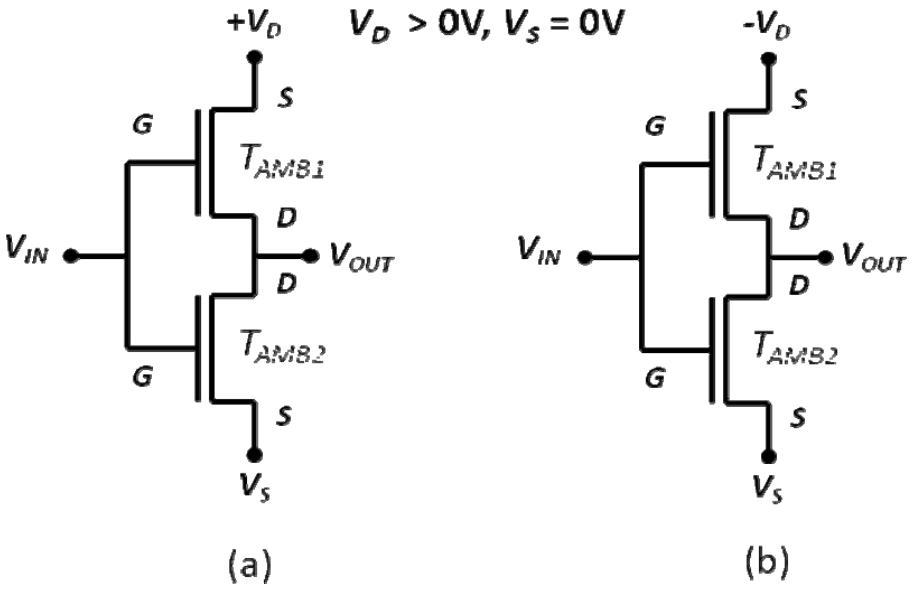

Figure 5.3: Circuit Schematics of inverters operating at 1st quadrant region with positive V_D and V_S = 0V (a) and 3rd quadrant region with negative V_D and V_S = 0V (b).

Figure 5.4(b) can be achieved in the same inverter under reversed voltage polarity with a negative voltage of V_D and a ground of V_S, corresponding to the circuit schematic in Figure 5.3(b). In this case, T_{AMB1} and T_{AMB2} now operate as *n*- and *p*-channel TFTs, respectively. Hence, unlike complementary inverters build with unipolar TFTs which are sensitive to the polarity of the input voltage, these ambipolar TFTs inverters can operate regardless of the polarity of V_{IN}. Although the performance of ambipolar TFTs inverters is slightly degraded because there is always a leakage current flowing through it, as neither transistor is ever fully switched off, the

ability of ambipolar TFT to be insensitive to the polarity of the input voltage provides the opportunity to simplify circuit design and lead to multifunctional circuits, as recently demonstrated in the context of logic gates [52].

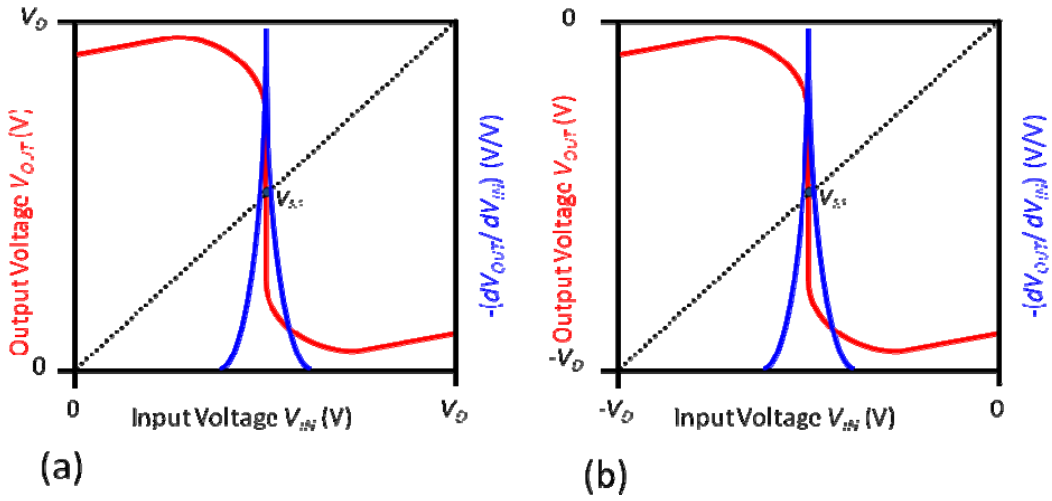

Figure 5.4: Voltage transfer characteristics and DC gains of inverters operating at 1st quadrant region (a) with positive V_{IN} and V_{OUT} (a) and 3rd quadrant region with negative V_{IN} and V_{OUT} (b).

5.2 Co-planar channel organic-inorganic hybrid ambipolar TFTs and inverters

5.2.1 Co-planar channel ambipolar TFT

Conventional structures of ambipolar TFTs have been realized the following three different approaches that can be categorized with respect to their semiconductor layers as single-component, blend or bilayer ambipolar transistors as shown in Figures 5.5(a) to (c) for a top contact geometry [56]. As previously discussed in the introduction of this chapter, each of these approaches presents particular challenges.

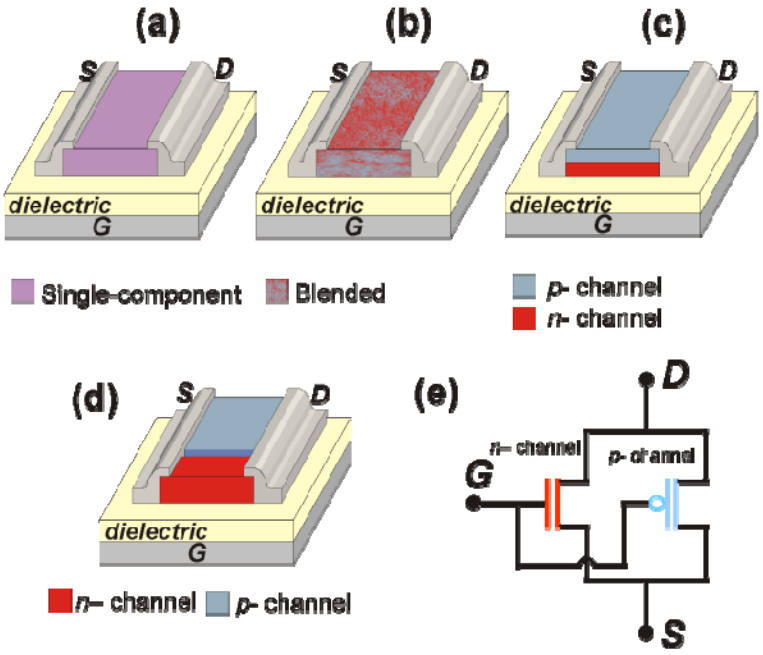

Figure 5.5: Ambipolar TFTs geometries: (a) single-component; (b) blended; (c) vertical bilayer; (d) co-planar. (e) Equivalent circuit of an ambipolar TFT with geometry (d) or in the limit of infinite recombination.

In this research, we introduce a co-planar channel geometry for the realization of ATFTs and complementary-like circuits. Figure 5.5(d) illustrates this geometry, wherein *n*- and *p*-channels, with different aspect ratio, are horizontally distributed without overlapping with each other. In the limit of an infinite recombination rate in the channel, ATFTs operate equivalently to an *n*- and a *p*-channel TFT connected in parallel [60]. Figure 5.5(e) shows the equivalent circuit in such limit. The proposed ATFTs physically realize this geometry. Differences in electron (μ_e) and hole (μ_h) mobilities, and threshold voltages, can then be compensated by resizing the width (W) of the *n*- and *p*-channel layers. The absence of a *pn*-heterojunction

removes potential problems associated with charge recombination, trapping, and control of the semiconductor morphology at this interface. Furthermore, the realization of such parallel-TFT configuration increases the regimes of operation of an ATFT, from six [60] to eleven, and leads to ATFTs and inverter circuits that can achieve high performance because the onset of operation for ambipolar behavior can be controlled. While a similar geometry has been reported in the past [123], a key difference of our approach is that channel resizing allows the implementation of ATFTs and their circuits with a variety of materials regardless of their relative mobility. This removes a key barrier for the realization of high performance ambipolar devices since the high mobilities and optimized performance of unipolar TFTs can be preserved. Therefore, we demonstrate that the proposed approach leads to hybrid organic-inorganic ATFTs with a performance similar to that of unipolar TFTs, preserving high charge mobility and threshold voltages, and to high performance hybrid ambipolar inverter circuits on rigid or flexible substrates. Compared to previous approaches, this horizontal geometry increases the complexity for the fabrication of a single ambipolar TFT. However, the number of steps required for the realization of unipolar TFT-based complementary circuits operating with the same dynamic range may in fact be reduced because less control lines are required for the operation of ambipolar TFT-based complementary circuits [52].

5.2.2 Experimental details

Thin-film transistors on heavily *n*-doped silicon substrates (*n*+-Si) were fabricated with a Ti/Au (20 nm/200 nm) layer deposited with a Kurt J. Lesker electron-beam (e-beam) deposition system on the backside of the *n*+-Si substrate to act as the gate electrode. A 200 nm-

thick Al_2O_3 (Al_2O_3, ε_r = 9) layer was grown by atomic layer deposition (ALD) as the gate dielectric. The capacitance density of Au/Al_2O_3/Si/Ti/Au metal-insulator-metal (MIM) structures using various areas ranging from 1 mm^2 to 5 mm^2 was estimated to be 40 nF/cm^2. A Savannah 100 ALD system from Cambridge Nanotech Inc. was used to deposit the Al_2O_3 dielectric films. The Al_2O_3 films were deposited at 120 °C using alternating exposures of tri-methyl-aluminum ($Al(CH_3)_3$) and H_2O vapor at a deposition rate of approximately 0.1 nm per cycle. Each deposition cycle (one monolayer) lasted 24 s, yielding a total deposition time of around 12 h for 2000 cycles [92, 100]. 30 nm-thick *n*-channel *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) active layer on a Al_2O_3/Si substrate was then deposited by rf-sputtering through a shadow mask at room temperature using a power of 125 W, a working pressure of 5 mTorr, and an O_2/Ar (1/10) atmosphere. After deposition of the *a*-IGZO layer, the device was annealed at 275 °C for 25 minutes in air. Then, 50 nm of pentacene as a *p*-channel active layer was deposited using thermal evaporation at a deposition rate of 0.3 Å/s. Depositions were done at 25 °C and an initial pressure of 2 x 10^{-8} Torr. Prior to thermal evaporation, pentacene was purified using gradient zone sublimation. Finally, a 50 nm-thick Au film was deposited through a metal shadow mask to serve as top source/drain electrodes.

Ambipolar inverters on polyethersulfone (PES, *i*-Components Co. Ltd.) substrates were fabricated with a tri-layer of Ti (7 nm)/Au (70 nm)/Ti (7 nm) deposited by e-beam through a shadow mask to act as the gate electrode. A 300 nm-thick Si_3N_4 gate dielectric layer was then deposited by PECVD at 180 °C. A 30 nm-thick *a*-IGZO (Ga_2O_3:In_2O_3:ZnO = 1:1:2 mol %) active layer was deposited through a shadow mask by rf-sputtering at a low temperature of 90 °C using a power of 125 W, a working pressure of 6 mTorr, and an O_2/Ar (1/20) atmosphere.

Then, a 50 nm-thick *p*-channel active layer of pentacene was deposited using thermal evaporation as previously described. Finally, Au (25 nm)/Al (25 nm) on both *p*-channel pentacene and *n*-channel *a*-IGZO were deposited to serve as top source/drain electrodes through a shadow mask.

Samples were transferred in a vacuum-tight vessel without being exposed to atmospheric conditions into a nitrogen glove box (O_2, H_2O < 0.1 ppm) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit. The output characteristics (drain current I_{DS} vs. drain-source voltage V_{DS} at multiple constant gate-source voltages V_{GS}) and transfer characteristics (I_{DS} vs. V_{GS} at fixed V_{DS}) of the TFTs were measured using an Agilent E5272A medium-power source/monitor unit connected to a probe station.

5.2.3 Operation of co-planar channel ambipolar transistors

The current flowing through an ATFT can be dominated by holes, electrons, or both, depending on the electrical bias across the channel. In the literature, six different regimes have been identified in the operation of an ATFTs by assuming a single threshold voltage for *n*- and *p*-type operation [60]. These regimes are defined by the sign and relative magnitudes between the drain-source voltage (V_{DS}) and the difference between the gate-source voltage (V_{GS}) and the threshold voltage (V_T). For instance, for *n*-channel operation three regimes are defined as follows: 1) if $0 < V_{DS} < V_{GS} - V_T$, as in unipolar TFTs, an electron current in the linear regime flows through the ATFT; 2) if $0 < V_{GS} - V_T < V_{DS}$, the electron current saturates like in an unipolar TFT, but a hole current also flows through the ATFT channel leading to ambipolar

transport; 3) if V_{GS} -V_T < 0 < V_{DS}, only holes flow through the ATFT channel [60]. Similarly, three regimes are also defined for *p*-channel operation. However, assuming a single V_T is in general not a good approximation for two unipolar TFTs operating in parallel.

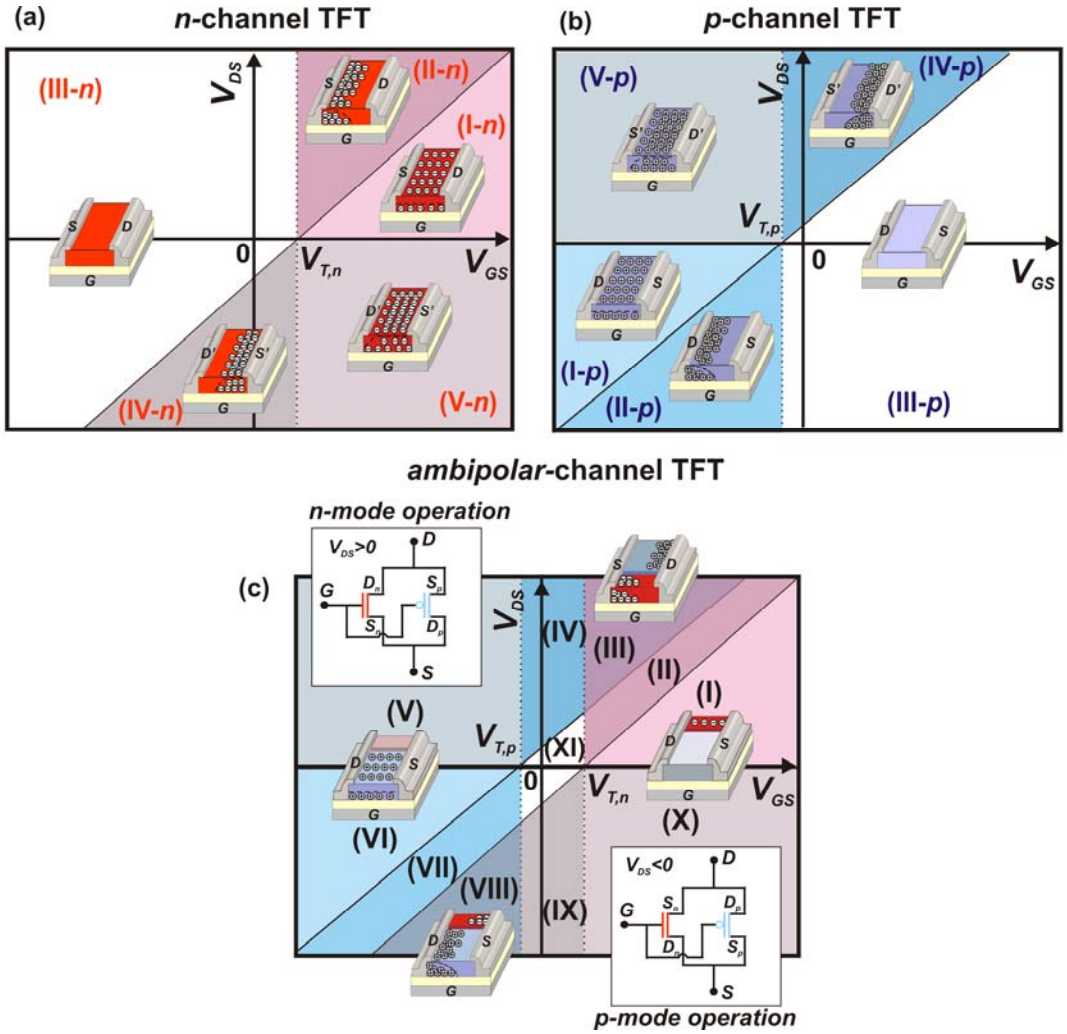

Figure 5.6: Charge distributions and energy diagrams under five different regimes found during *n*-channel (a) and *p*-channel (b) operation of TFTs, respectively. (c) Equivalent circuit, eleven different operation regimes, and charge distributions found during ambipolar TFT operations.

In the most general case, the threshold voltage of the *n*-channel ($V_{T,n}$) and *p*-channel ($V_{T,p}$) can be expected to be different. The implications of such a change are better understood

by reviewing the operation of an unipolar TFT under all bias conditions. Figure 5.6(a) shows the five regimes of operation of an unipolar *n*-channel TFT and the corresponding band diagram. These regimes are better understood by considering that a positive V_{DS} causes an increase of the work function of the drain electrode allowing electrons injected from the source to be collected. If $0 < V_{DS} < V_{GS} - V_{T,n}$ (regime I-*n*), the TFT operates in the linear regime. If $0 < V_{GS} - V_{T,n} < V_{DS}$ (regime II-*n*), the *n*-channel TFT operates in the saturation regime. Both regions are divided by the pinch-off condition defined by a diagonal defined by $V_{DS} = V_{GS} - V_T$. If $V_{GS} - V_T < 0$ (regime III-*n*), the TFTs is off because the barrier for electron injection from either electrode increases as $V_{GS} - V_T$ becomes increasingly negative. If now we apply a negative V_{DS}, the work function of the drain electrode decreases making the driving force for electron injection at the drain larger than at the source. Under this condition, an electron current would flow from the drain to the source. Since the terms drain and source are relative to the direction of current flow, the roles of source and drain are effectively reversed. Therefore, an *n*-channel TFT biased at $V_{DS} < 0$ is referred to as being operating in reverse mode. In reverse mode operation, *S* = *D*', and *D*= *S*', where the primes denote the effective role played by that electrode. Considering that the source electrode remains grounded, $V_S = 0$ V, the main consequence of this change is that a change in $V_{DS} = V_D - V_S = V_D = V_{S'}$ leads to a simultaneous change of $V_{GS'}$ and $V_{D'S'}$. This implies that for an *n*-channel TFTs that follows the square-law model, the current-voltage equations in reverse mode are given by:

$$I(V_{DS} < V_{GS} - V_{Tn} < 0) \propto -(V_{GS'} - V_{Tn})^2 = -(V_{GD} - V_{Tn})^2, \qquad \text{Eq. (5.1)}$$

$$I(V_{DS} < 0 < V_{GS} - V_{Tn}) \propto -(V_{GS'} - V_{Tn})V_{D'S'} + V_{D'S'}{}^2 = (V_{GD} - V_{Tn})V_{DS} + V_{DS}{}^2. \qquad \text{Eq. (5.2)}$$

Therefore, significant currents flow in reverse mode operation by changing either the drain or gate electrode potentials. Equations (1) and (2) describe the current-voltage characteristics of regimes IV-*n* and V-*n*, respectively. If V_{GS}-$V_{T,n}$ < V_{DS} < 0, the TFTs remains off (regime III-*n*) due to the large barrier for electron injection at the drain and source electrodes. Figure 5.6(b) shows the analogous five regimes of operation for a *p*-channel TFT.

In the most general case, the *I*-*V* characteristics of an ATFT arise from the linear superposition of the five operating regimes of its unipolar channels due to its parallel circuit configuration. Figure 5.6(c) shows the eleven operating regimes that exist in such a superposition. The key difference provided in this configuration with respect to the previous descriptions of ambipolar TFT behavior, is that two additional regimes exist, regime II (intersection of II-*n* and III-*p*) and VII (intersection of II-*p* and III-*n*), where unipolar currents can reach saturation in one channel without experiencing significant "leakage" currents from the other channel. Therefore, by displacing the regimes of ambipolar transport, regime III (intersection of II-*n* and IV-*p*) and VII (intersection of II-*p* and IV-*n*), a co-planar channel geometry leads to the possibility of controlling the "leakage" currents in ATFTs by tailoring the threshold voltages for the independent channels. Note that if $V_{T,n} = V_{T,p}$, the six regimes [60] for ATFT operation commonly described in the literature are recovered.

5.2.4 Electrical characterization: co-planar channel ATFTs

We fabricated ATFTs with a bottom gate top electrode geometry on an Al_2O_3(200 nm)/Si substrate to illustrate the properties of ATFTs with a co-planar geometry. Non-overlapping pentacene (hole transport) and amorphous-InGaZnO (*a*-IGZO) (electron transport)

channels horizontally distributed with different aspect ratios were fabricated as shown in the insets of Figure 5.7. Gold source and drain electrodes were used to provide a similar energy barrier of ~ 0.6 eV for the injection of holes into pentacene and electrons into *a*-IGZO [118, 124].

In ATFTs with a co-planar geometry, further optimization of the injection characteristics can easily be achieved by selecting suitable metals for the source and drain electrodes of each channel. Despite the relatively large energy barrier for charge injection, the performance of the ATFTs did not suffer from contact resistance effects due to the large channel dimensions used. The horizontal channels had a channel length of L = 180 μm and channel widths of W^p = 4000 μm and W^n = 400 μm for the *p*- and *n*-channel, respectively. Independent pentacene and *a*-IGZO TFTs with the same geometry were fabricated as reference. Devices with the channel width ratio of W^n / W^p = 10, was selected to compensate for: 1) differences in μ_e and μ_h; and 2) differences in the threshold voltage observed in unipolar devices.

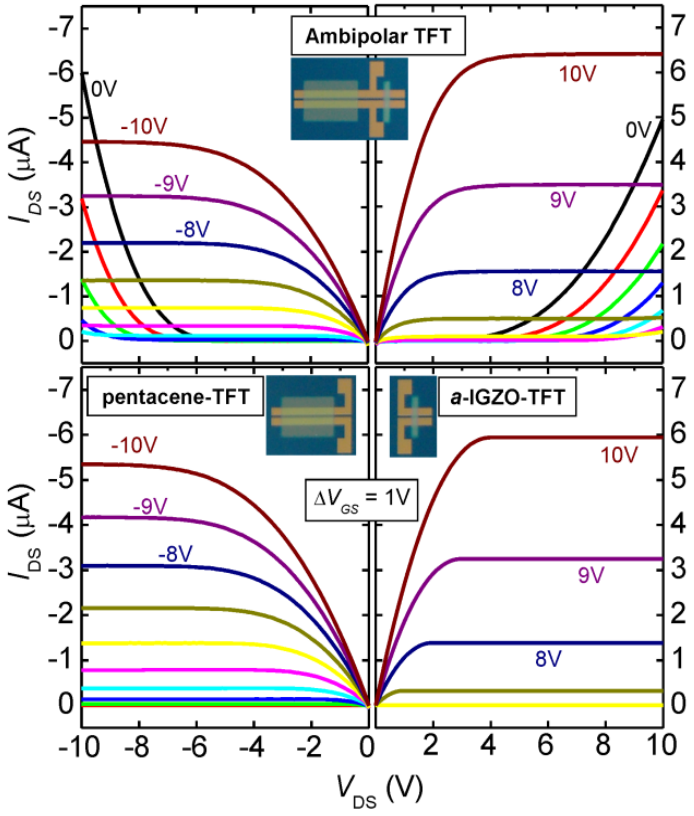

Figure 5.7: Comparison of output characteristics of ambipolar TFT during *p*-type and *n*-type operation with corresponding unipolar *p*-type (pentacene) TFT and *n*-type (*a*-IGZO) TFT output characteristics. Insets show pictures of the devices.

Figure 5.7 shows the output characteristics of hybrid ATFTs and of unipolar pentacene and *a*-IGZO TFTs. The relatively high gate dielectric capacitance density, 40 nF/cm^2, allows all TFTs to reach saturation at low V_{DS}. The drain-source currents (I_{DS}) measured in ATFTs yield similar values similar to those measured in unipolar TFTs. The linear dependence of I_{DS}, at low V_{DS}, provides evidence that the performance of these TFTs is not contact limited. In contrast with unipolar TFTs, for $V_{GS} < V_{T,n(p)}$ and at large V_{DS}, I_{DS} increases due to "opposite" carrier electron ($-3V < V_{GS} < 0$) and hole currents ($0 < V_{GS} < 5V$) that arise in reverse mode operation.

As previously mentioned, the appearance of these "leakage" currents is directly related with the values of $V_{T,n(p)}$. Unlike other configurations, in these ATFTs, the values of $V_{T,n(p)}$ can in principle be controlled independently to minimize such currents. As V_{GS} is increased above threshold, I_{DS} monotonically increases due to unipolar operation (regimes I and VI) until it reaches saturation (regimes II and VII) when $|V_{GS}-V_{T,n(p)}| < |V_{DS}|$. Figure 5.7 shows that due to channel resizing, the on-currents for the *p*- and *n*-type operation are well-balanced. Furthermore, since in the saturation regimes II and VII, only one channel remains active in the ATFT, the current-voltage characteristics are nearly identical to those of unipolar TFTs, with no "opposite" carrier contributions even at large $|V_{DS}|$ values.

Figure 5.8(a) shows the overlapping hysteresis transfer characteristics for ATFTs at different values of V_{DS} below saturation. At $|V_{DS}| = 0.5$ V, the transfer characteristics of ATFTs are due to single carrier charge transport in the operating regimes I and II for *n*-type operation, VI and VII for *p*-type operation and the regime XI where both channels remain off. This allows the on-off current ratio ($I_{on\text{-}off}$) to approach 10^5 at $|V_{DS}| = 0.5$V. In these regimes the field-effect mobility (μ_{FE}) can be determined through the transconductance, g_m, using the following equation:

$$g_m = \left(\partial I_{DS}/\partial V_{GS}\right)\Big|_{V_{DS}=small} = (\mu_{FE}\,\varepsilon_0\,\varepsilon_r\,WV_{DS})/(Ld), \qquad \text{Eq. (5.3)}$$

where W is the channel width, L is the channel length, ε_0 is the free-space permittivity, ε_r is the relative dielectric constant of the gate insulator and d is the thickness of the gate insulator.

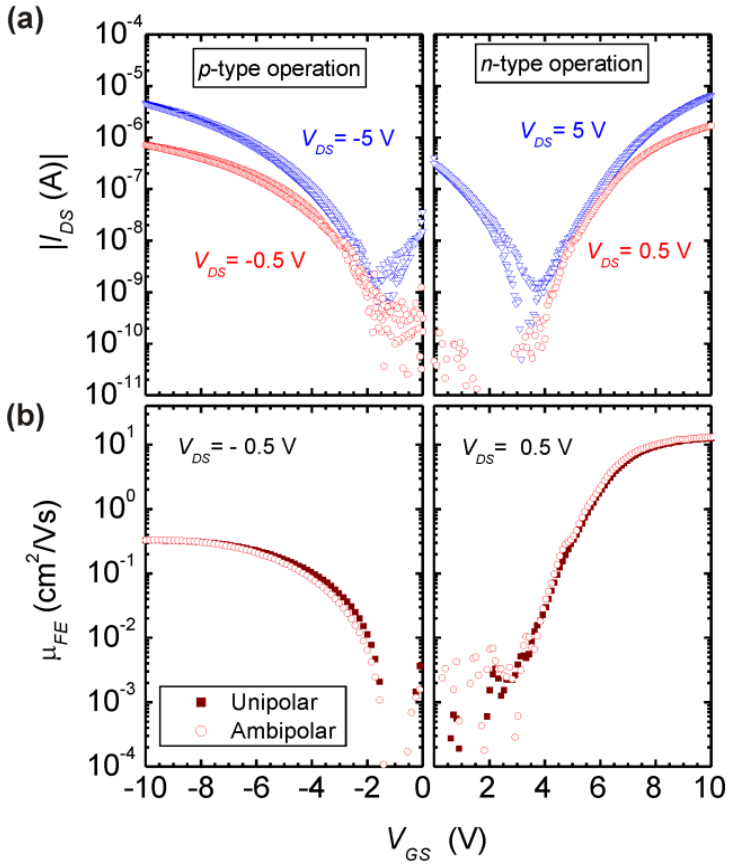

Figure 5.8: (a) Hysteresis transfer characteristics at low V_{DS} measured in ambipolar TFT during *p*-type and *n*-type operation. (b) Comparison of the field-effect mobility measured in an ambipolar TFT during *p*-type and *n*-type operation with that measured on *p*-type (pentacene) TFT and *n*-type (*a*-IGZO) TFT in the linear regime.

Figure 5.8(b) shows a direct comparison of the field-effect mobility values (μ_{FE}) in ATFTs and unipolar TFTs. Unlike previous approaches, the values of μ_{FE} found in ATFTs equal those in their unipolar counterparts with values approaching $\mu_{p\text{-}op} = \mu_h = 0.3$ cm^2/Vs and $\mu_{n\text{-}op} = \mu_e = 10.5$ cm^2/Vs. Within the resolution of our setup, all parameters between ATFTs and unipolar TFTs are identical in this regime. Close to saturation, at 5V, $I_{on\text{-}off}$ approaches 10^4 despite the reduction of the off-currents due to ambipolar operation in regimes III and VIII.

Figure 5.9 shows that at larger values of $|V_{DS}|$, the $I_{on\text{-}off}$ in ATFTs is further reduced due to "opposite carrier" contributions in the ambipolar regimes. This is a typical signature of ATFTs and is expected even if, as in this case, the individual channels of the ATFT show a performance similar to that of unipolar TFTs. However, Figure 5.9 also shows that for large enough value of V_{GS}, the values of I_{DS} in these ATFTs rapidly converge to the values found in unipolar TFTs.

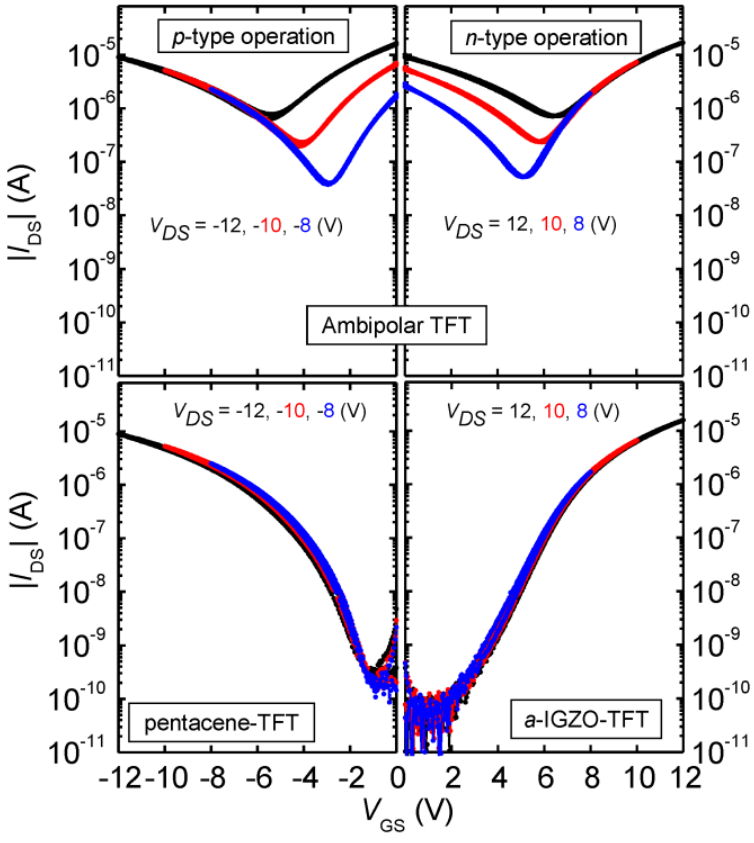

Figure 5.9: Hysteresis transfer characteristics in saturation measured in ambipolar TFT during *p*-type and *n*-type operation and the corresponding transfer characteristics measured on *p*-type (pentacene) TFT and *n*-type (*a*-IGZO) TFTs.

Since around pinch-off ($|V_{DS}| = |V_{GS} - V_{T,n(p)}|$) the ATFT is expected to operate like a unipolar TFT, the source-to-drain current for both unipolar and ambipolar TFTs can be approximated by:

$$I_{DS} = \frac{\mu \varepsilon_0 \varepsilon_r W}{2Ld}(V_{GS} - V_{T,n(p)})^2, \qquad \text{Eq. (5.4)}$$

where μ is the effective saturation mobility, $V_{T,n(p)}$ is the effective threshold voltage, W is the channel width, L is the channel length, ε_0 is the free-space permittivity, ε_r is the relative dielectric constant of the gate insulator, and d is the thickness of the gate insulator. A summary of the parameters extracted through a fitting procedure using Eq. (5.4) is found in Table 5.1.

Table 5.1: Summary of parameters extracted, using equation (5-4), on ambipolar TFTs and on *p*-type (pentacene) TFT and *n*-type (*a*-IGZO) TFTs.

	V_{DS} [V]	V_{GS} [V]	μ_{SAT} [cm^2/Vs]	V_T [V]	I_{Max} [A]
		Ambipolar TFTs			
p-type operation	-8	0 to -8	0.27	-3.4	-2.3×10^{-6}
	-10	0 to -10	0.32	-3.7	-5.1×10^{-6}
	-12	0 to -12	0.33	-3.7	-9.0×10^{-6}
n-type operation	8	0 to 8	8.09	5.6	1.9×10^{-6}
	10	0 to 10	11.10	6.0	7.3×10^{-6}
	12	0 to 12	13.00	6.3	1.7×10^{-6}
		Unipolar TFTs			
p-type (pentacene)	-8	0 to -8	0.29	-3.3	-2.5×10^{-6}
	-10	0 to -10	0.34	-3.7	-5.3×10^{-6}
	-12	0 to -12	0.35	-4.0	-8.9×10^{-6}
n-type (*a*-IGZO)	8	0 to 8	7.28	5.6	1.7×10^{-6}
	10	0 to 10	10.20	6.0	6.6×10^{-6}
	12	0 to 12	12.30	6.6	1.6×10^{-6}

Hence, in the linear regime the output and transfer characteristics of these ATFTs show nearly identical performance with respect to unipolar TFTs. In saturation, $I_{on\text{-}off}$ values are reduced due to ambipolar operation, but the effective mobilities, threshold voltages and values of I_{DS} current values are similar to the ones measured in unipolar TFTs.

5.2.5 Co-plannar channel ATFT-based inverters

Ambipolar TFTs offer the potential to yield multifunctional digital and analog circuits.[3] With their unipolar counterparts, complementary circuits that operate regardless of the sign of the input voltage would require an increased number of control lines. To investigate the performance of such circuits, complementary-like or ambipolar inverter circuits were constructed using two identical ATFTs with a co-planar channel geometry (ATFT-1 and ATFT-2), as shown in the inset of Fig. 5.10(a) and 5.10(b). Unlike unipolar inverters, ambipolar inverter circuits operate regardless of the sign of the input voltage (V_{IN}). Figure 5.10(a) shows the measured hysteresis voltage transfer characteristics and static gains of the ambipolar inverter fabricated on a rigid substrate at $V_D = \pm 10$ V ($V_S = 0$ V). When V_{IN} is swept from 0 V to positive V_D, a gain of 50 V/V at $V_D = +10$ V is achieved with high steepness and small hysteresis. From 0 V to negative V_D, the inverter shows similar performance, with a gain of 35 V/V at $V_D = -10$ V. These high gains can be attributed to the high on-off ratios achieved at $V_{DS} = \pm 5$ V by their component ATFTs (see Figure 5.8). The average switching voltages $V_M = 6.7$ V and -3.5 V obtained, are slightly shifted from their theoretical value of $0.5V_D$ mainly due to the threshold voltage mismatch ($V_{T,n} = 6.0$ V and $V_{T,p} = -3.7$ V), which reflects in different

channel resistances around $0.5V_D$. The noise margin low (NM_L) and noise margin high (NM_H), characterized using the negative slope criteria,[24] yield values of NM_L = 5.9 V and NM_H = 1.6 V at V_D = 10 V and NM_L = 5.6 V and NM_H = 2.2 V at V_D = -10 V. Compared with previous ambipolar inverters, these inverters show smaller degradation of V_{OUT} during pull down and pull up, an intrinsic characteristic of ambipolar inverters.[53, 54] Further improvements could be expected if the transistor channels have better matched threshold voltages. Therefore developing methods to tailor the threshold voltage of organic and semiconductor oxide transistors is expected to be critical to achieve further enhancements in circuit performance.

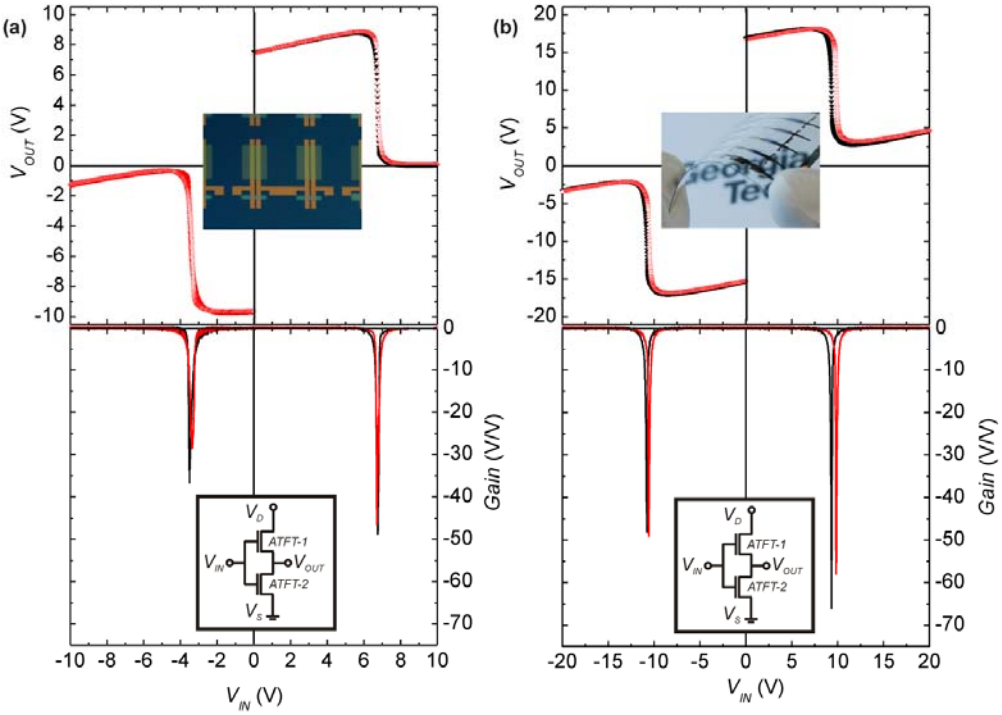

Figure 5.10: (a) Hysteresis transfer characteristics at low V_{DS} measured in ambipolar TFT during *p*-type and *n*-type operation; (b) Comparison of the field-effect mobility measured in an ambipolar TFT during *p*-type and *n*-type operation with that measured on *p*-type (pentacene) TFT and *n*-type (*a*-IGZO) TFT in the linear regime.

To further demonstrate the potential of this co-planar geometry we fabricated hybrid ATFTs on a flexible polyethersulfone (PES) substrate with the same hybrid material platform and channel geometry previously described. Figure 5.10(b) shows the voltage transfer characteristics of such ATFT-based inverters. Using a 300 nm-thick Si_3N_4 gate dielectric layer, these inverters show gains of 66 V/V and 50 V/V with a V_M = 9.7 V and -10.6 V at $V_D = \pm 20$ V, respectively. Compared to ambipolar inverters on Si substrates, these inverters achieve higher gains due to better matched threshold voltages ($V_{T,n}$ = 10.5 V and $V_{T,p}$= -10.2 V) and balanced *on*-currents during *p*- and *n*-type operation. Furthermore, better matched threshold voltages also lead to a sharp transition and to a well centered switching voltage that in turn yields excellent noise margins of NM_L = 5.4 V and NM_H = 7.2 V at V_D = 20 V and NM_L = 4.9 V and NM_H = 7.1 V at V_D = -20 V. Although a comparison with previous reports is difficult because the noise margins of ambipolar inverters are not commonly reported, the combined gains and noise margins of these flexible ambipolar inverters start approaching those of complementary inverters based on unipolar *n*- and *p*- type TFTs. Compared to ATFTs fabricated on rigid substrates, in these ATFTs, $\mu_{p\text{-}op}$ = 0.1 cm^2/Vs and $\mu_{n\text{-}op}$ = 2.8 cm^2/Vs. These values are not as high as the ones obtained on Si but they are comparable to unipolar TFTs fabricated on PES. While it is clear that complementary-like ambipolar inverters dissipate more power than complementary inverters, at this point it is unclear what will be the ultimate limit to the performance of such ambipolar circuits. However, the proposed geometry allows independent optimization of key parameters affecting their performance, such as mobilities, threshold

voltages and channel aspect ratio. An estimation of such limit based on this geometry is being pursued.

Table 5.2: Comparison of state-of-art ATFTs and ambipolar inverters.

Geometry	*Gate Dielectric /Substrate*	*N/P-type Semi-conductors*	*Operating range* (V)	$\mu_{n\text{-}op}$ (AMB) μ_e (UNI) (cm^2/Vs)	$\mu_{p\text{-}op}$ (AMB) μ_h (UNI) (cm^2/Vs)	V_D (V)	V_{IN} (V)	*Max. Gain* (V/V)	V_M *in 1st (3rd) quadrants* (V)	*Avg. NM* (%)	*Ref.*
Single layer	SiO_2 /Si	PCBM	-75 to +20	1×10^{-2} –	8×10^{-3} –	±60	0 to ±60	18	~ 24 (-28)	–	[54]
Single layer	SiO_2/Si	Nickel dithiolene	±30	8×10^{-4} –	2×10^{-3} –	±20	0 to ±20	6	~11 (~-9.5)	–	[66]
Single layer	Poly(vinylphenol)/polymer (flexible)	Nickel dithiolene	±30	~ 8×10^{-5} –	~ 2×10^{-4} –	–	–	–	–	–	[66]
Blended	SiO_2 /Si	C_{60} /CuPc	±80	2×10^{-2} 7×10^{-2}	5×10^{-5} 6×10^{-4}	±90	0 to ±90	18	~ 45 (-45)	28 ~ 42	[64]
Vertical bilayer	SiO_2 /Si	ZnO /Pentacene	±100	8×10^{-3} 0.29	6×10^{-3} 7×10^{-2}	–	–	–	–	–	[71]
Vertical bilayer	SiO_2 /Si	IZO /Pentacene	-100 to +40	13.8 16	0.16 0.14	–	–	–	–	–	[70]
Vertical bilayer	SiO_2 /Si	In_2O_3 /Pentacene	±100	0.07 –	0.02 –	±100	0 to ±100	12	~ 35 (-62)	–	[68]
Co-planar	Al_2O_3 /Si	*a*-IGZO /Pentacene	±10	11.1 10.2	0.32 0.34	±10	0 to ±10	50	6.7 (-3.5)	75	This work
Co-planar	SI_3N_4 /PES (flexible)	*a*-IGZO /Pentacene	±20	2.8 2.3	0.1 0.1	±20	0 to ±20	66	9.7 (-10.6)	63	This work

Table 5.2 shows a comparison of the properties of ATFTs and ambipolar inverters reported in this work with respect to those reported in the literature. Emphasis is placed on ATFTs that were used to demonstrate complementary inverters and, due to the similarity with respect to the material platform used in this work, on the existing reports on hybrid oxide

semiconductor/pentacene ATFTs. As clearly shown, without significant device optimization, the novel co-planar geometry yields ATFTs and inverters that define the state-of-the art.

5.2.6 Dynamic characteristics of ambipolar TFT-based inverters

Figure 5.11 shows the dynamic behavior of the ATFT inverter biased with square wave inputs $|V_{IN}|$ oscillating from 0 to 10 V at 5 Hz. The inverting operation is clearly shown for both polarities of V_{IN}. The large overlapping capacitance between source/drain and gate electrodes due to the common gate geometry limits the rising and falling time to ~10 ms. The switching speed can easily be improved by patterning the gate electrode and resizing the area of transistor. For optimized ATFT circuits, their switching speed is expected to be only limited by the mobility of the individual materials.

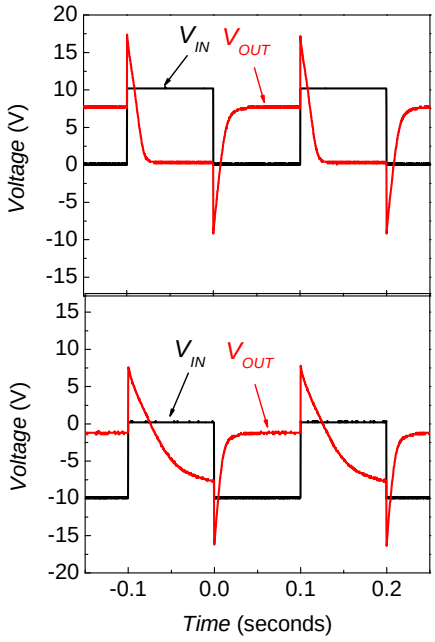

Figure 5.11: Dynamic characteristics of ATFT-based inverters, on rigid Al_2O_3 (200 nm)/Si substrates, at 5 Hz with V_D varied from 0 V to ± 10 V.

5.2.7 Summary

In summary, we proposed a co-planar channel geometry for the realization of high performance ambipolar TFTs. Using non-overlapping horizontal channels of pentacene and *a*-IGZO we demonstrated high performance ambipolar TFTs with channels that show electrical properties comparable to those found in unipolar TFTs with the same channel aspect ratios. By retaining key parameters of the electrical performance of unipolar TFTs, this geometry can easily be implemented with other material platforms because it allows for the same optimization approaches used for unipolar devices to be followed. While this new geometry may increase the complexity for the fabrication of a single ambipolar TFT, from an analog or digital circuit design perspective, the complexity in circuit fabrication may not be increased. With the new design flexibility we demonstrated hybrid ambipolar inverter circuits, in rigid and flexible substrates, that show a significant improvement over the performance found in previously reported complementary-like inverters. From a materials perspective, this work shows that future breakthroughs in performance of unipolar *n*-type and *p*-type semiconductors could be directly transposed into ambipolar transistors and circuits. Hence, we expect that this geometry will provide new strategies for the realization of high performance ambipolar TFTs and novel ambipolar microelectronic circuits.

CHAPTER 6 CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

In this dissertation, we demonstrated low voltage high performance oxide TFTs with high-k and/or thin dielectrics as gate insulators and *p*-channel pentacene and *n*-channel *a*-IGZO TFT based organic-inorganic hybrid complementary and complementary-like inverters with high gains and high and balanced noise margins. With different challenges in the development of oxide TFTs, unipolar TFT-based complementary and ambipolar TFT-based complementary inverters, the dissertation was categorized into three major parts: oxide TFTs and electronic circuits (Chapter 3), organic-inorganic hybrid complementary inverters (Chapter 4), and organic-inorganic hybrid ambipolar TFTs and ambipolar TFT-based complementary-like inverters (Chapter 5). The summary and conclusions are as follows.

In Chapter 3, the research focused on the development of low voltage high frequency oxide TFTs and electronic circuits using high-*k* and/or thin dielectrics as gate insulators. Section 3.1 focused on developing high performance top contact bottom gate *n*-channel *a*-IGZO TFTs that use a 170 nm-thick *a*-BST ($\varepsilon_r = 28$) as a gate dielectric material. Amorphous-BST films deposited at room temperature by rf-sputtering showed negligible frequency and voltage dependence. With a high gate dielectric capacitance density of 145 nF/cm^2, *a*-BST/*a*-IGZO TFTs showed high saturation mobility values of 10 ± 1 cm^2/Vs, low threshold voltages of 0.5 ± 0.1 V at 3 V and on-off current ratios up to 8 × 10^7. The very low source-drain contact resistance < 50 Ω.cm at 3 V obtained in these TFTs allowed for very small sub-threshold slopes of 0.11 ± 0.02 V/decade and a channel length independent mobility which does not limit the

transconductance (g_m) and potentially allows for TFTs capable of low power and high frequency operation. However, the small band gap (3.3 eV) and relatively large electron affinity (4 eV) of *a*-BST forces careful control of the TFTs to reduce the leakage currents and limits its operational range. The use of larger bandgap dielectrics is then desirable to increase the energy band offsets with respect to *a*-IGZO. In Section 3.2, we demonstrated low voltage high speed oxide TFTs with low leakage current. As an alternative approach to increase the capacitance density of the gate dielectric, we used a 100 nm-thick Al_2O_3 layer deposited by ALD. With a high dielectric constant of 9 and a large bandgap of 8 eV, Al_2O_3 was a good candidate to produce gate dielectrics with low leakage and high capacitance density. Furthermore, ALD is a well-known deposition process that yields highly conformal, defect-free dielectric layers at relatively low temperatures. Therefore, we developed high-performance top-contact bottom-gate n-channel *a*-IGZO thin-film transistors that use 100 nm-thick Al_2O_3 grown by ALD as the gate dielectric material. Al_2O_3 films deposited by ALD showed very small leakage current below 10^{-7} A/cm^2 up to 3.5 MV/cm with a field and frequency independent $C_i = 81 \pm 1$ nF/cm^2. Al_2O_3(ALD)/*a*-IGZO TFTs operated in enhancement mode with high μ_{FE} of 8 ± 1 cm^2/Vs, low V_T of 0.4 ± 0.1 V at 5 V, and $I_{on\text{-}off}$ of 6×10^7. The very small S of 0.1 ± 0.01 V/decade yielded very small subgap density of state (DOS) and allowed very low operating voltages. Moreover, with width normalized contact resistance (R_cW) = 25 Ω.cm at 5 V, much smaller than width normalized channel resistance ($R_{ch}W$), μ_{FE} is channel–length independent and does not limit the transconductance, potentially allowing TFTs capable of low power operation up to frequencies around 7.8 MHz. In Section 3.3, we have demonstrated a low-voltage two transistors and one capacitor (2T1C) pixel driver circuit for AMOLED display driven by high performance

enhancement mode *a*-IGZO channel thin film transistors. Low-voltage operation for the pixel driver circuit was achieved by using a 30 nm-thick electron-beam (e-beam) deposited Al_2O_3 as a gate dielectric material. With high gate dielectric capacitance density of 180 nF/cm^2, the TFTs showed large saturation mobility values of 4.5 ± 0.5 cm^2/Vs, excellent sub-threshold slopes of 0.09 ± 0.01 V/decade, low threshold voltages of 0.5 ± 0.2 V, and high on-off current ratios of above 10^6 at a voltage of 3.5 V. While further optimization is possible, the data presented shows the potential of IGZO-based transistors to develop low voltage and high frequency driving circuits for AMOLED displays.

In Chapter 4, the research focused on the development of high performance organic-inorganic hybrid complementary inverters based on high mobility *n*-channel *a*-IGZO and, a widely used, *p*-channel pentacene TFTs on flexible substrates. All-organic or organic-inorganic hybrid TFTs have the potential to lead to a generation of low cost complementary circuits, processed at low-temperatures on flexible substrates. This work involved the integration of *n*-channel *a*-IGZO and *p*-channel pentacene TFTs into complementary inverters. We demonstrated organic-inorganic hybrid complementary inverters fabricated on flexible PES substrates that use *n*- and *p*-channel TFTs with channels having different aspect ratios to achieve high static gains and balanced high noise margins. With a Si_3N_4 gate dielectrics, *p*- and *n*- channel TFTs showed saturation mobility values of 0.13 and 3.8 cm^2/Vs, respectively. We also proposed a new approach to find the switching threshold voltage and the optimum value of the supply voltage (V_D) to operate a complementary inverter. Using this method, we demonstrated hybrid inverters that achieved a very high gain of 130 V/V at V_D = 25 V with high and balanced noise margin values of 84% of their theoretical maximum. In contrast with

previous analytical methods, the proposed method does not require fitting to any transistor model, can be implemented with a pair of measurements and should also be applicable to any complementary or complementary-like (one that uses ambipolar TFTs) inverter configuration.

In Chapter 5, the research focused on ambipolar transistors and complementary-like inverters based on an *n*-channel *a*-IGZO and *p*-channel pentacene hybrid geometry. In this work, we proposed a new co-planar channel geometry for the realization of high performance ambipolar TFTs. Using non-overlapping horizontal channels of pentacene and *a*-IGZO we demonstrated high performance ambipolar TFTs with channels that showed electrical properties comparable to those found in unipolar TFTs with the same channel aspect ratios. By retaining key parameters of the electrical performance of unipolar TFTs, this geometry can easily be implemented with other material platforms because it allows for the same optimization approaches used for unipolar devices to be followed. With the new design flexibility we demonstrated hybrid ambipolar inverter circuits, in rigid and flexible substrates, that show a significant improvement over the performance found in previously reported complementary-like inverters. For instance, on flexible substrates, gains approach 70 V/V at 20V with average noise margins larger than 60 % of their theoretical value ($0.5\times V_D$). This represents improvements of at least 3.5× on the gain, a reduction of at least 3× in the operating voltages and a 2× increase in the noise margins, over the best ambipolar inverters (organic or hybrid) reported in the literature to date. This novel geometry, constitutes a new approach for the realization of ATFTs that can easily be adapted to existing organic, inorganic or hybrid TFTs material platforms, and is particularly suited for printable materials. This work defines the state-of-the-art and shows that high performance unipolar *n*- and *p*-channel TFTs can directly yield

high performance ATFTs without further material or device optimization. From a materials perspective, this work shows that future breakthroughs in performance of unipolar *n*-channel and *p*-channel semiconductors could be directly transposed into ambipolar transistors and circuits. Hence, we expect that this work will provide new strategies for the realization of high performance ambipolar TFTs and novel ambipolar microelectronic circuits.

6.2 Recommendations for future work

Based on the results in this dissertation and by others in the research community, this section provides recommendations for future work in organic–inorganic hybrid circuit integration.

6.2.1 Recommendations for research on oxide TFTs

Device stability of amorphous IGZO TFTs: In this dissertation, the research focused on the realization of high-performance amorphous IGZO TFTs with a high mobility, a low threshold voltage, a low subthreshold slope, and a high on/off current ratio operating at low voltage. Amorphous IGZO TFTs have shown excellent electrical properties, including a high mobility and an excellent on-off current ratio, which make these transistors a very promising alternative to amorphous silicon (*a*-Si) TFTs especially in a backplane application for AMOLED displays. However, for commercial circuit applications, the devices should maintain similar electrical performance parameters during long periods of operation with excellent reproducibility and good electrical stability under electrical stress. The electrical stability of the TFT is especially critical in the case of current driven OLED displays because it can lead to variations in the pixel

brightness. It is well known for *a*-Si:H [125], poly-Si [126], and several organic [127] TFTs that prolonged application of gate bias on the TFTs can result in the deterioration of the current-voltage characteristics. This bias effect can lead to changes in mobility, threshold voltage, and subthreshold slope. Though amorphous oxide TFTs have been extensively studied by various groups, very little work has been reported on the bias stress effect. Oxide TFTs showed degradation of the threshold voltage under electrical stress with small variations of the mobility during continuous dc bias stress. The threshold voltage instabilities of oxide TFTs under dc bias stress can be explained by charge trapping at or near the oxide channel layer and gate dielectric based on the amorphous Si framework [128-131]. The device instability of amorphous Si TFTs has been explained by charge trapping in the gate dielectric or the creation of metastable dangling bond states in amorphous Si [132-134]. In addition, oxygen and moisture in the ambient atmosphere might affect the transistor properties due to the adsorption/desorption dynamics of these molecules onto the exposed back-channel region of the oxide transistor [135-137]. Therefore, it is important to investigate the physical mechanisms that hinder device stability of amorphous oxide TFTs, especially the variation of threshold voltage, under electrical bias stress and exposure to ambient air.

6.2.2 Recommendations for research on hybrid circuit integration

1. Optimization of pentacene TFTs: In order to take full advantage of complementary technology, both *p*-channel and *n*-channel TFTs should have comparable performance parameters, such as mobility and threshold voltage. Although we achieved high gain and high and balanced noise margin values in organic-inorganic hybrid complementary and

complementary-like inverters by appropriately sizing the width of the *n*- and *p*-channel TFTs, the limitation of the operating frequency in these inverters comes from the material with the lower mobility. A strategy can be implemented to control the morphology of the pentacene film, especially the first monolayer close to the dielectric interface, by tuning the substrate temperature, deposition rate and film thickness during the pentacene deposition. In addition, the diffusion of the top source/drain electrode metals into the pentacene films could affect the morphology. Therefore, the thickness and deposition parameters of the source/drain metals could be controlled to optimize the morphology for high charge mobility.

2. Device stability of organic TFTs: For practical applications, the devices should be less sensitive to electrical changes during prolonged operation and environmental conditions. In addition to the hysteresis behaviors observed in some organic TFTs, organic TFTs show a degradation of their electrical performance parameters such as mobility and threshold voltage during electrical stress. Particularly, the degradation of the threshold voltage can be easily observed during electrical bias stress. Therefore, it is important to investigate the physical mechanisms that hinder device stability. On the other hand, environmental conditions also degrade the performance of organic TFTs. Generally organic TFT devices should be protected by encapsulation to provide longer operational lifetime due to the sensitivity of these electronics to moisture and oxygen in the environment [138-140]. Attaching a metal or glass lid to the substrate with a low-permeation adhesive is one encapsulation method used to protect organic materials (especially for organic light emitting diode displays). A desiccant is often incorporated to remove the byproduct from the adhesive drying process. However, this method is not compatible with flexible electronics due to the rigidity, weight, and cost of the lid. As an

alternative approach, a thin-film barrier coating on both the bottom and top side of the electronics can protect these devices while maintaining both a flexible form factor and a light weight. Inorganic films like oxides can protect the organic devices from oxygen and moisture. However, compared to glass, there are always imperfections and defects caused by surface topography and particles introduced during deposition. Polymer/inorganic multilayer structures offer a significant improvement in permeation-barrier performance [141]. For example, a highly conformal, defect free dielectric Al_2O_3 grown by ALD or Al_2O_3/polymer multi-layers processed at a low temperature could be one of the choices to protect organic devices.

3. Complementary circuit integration: Oxide based circuits such as IGZO-based ring oscillators have been reported, but they are implemented with only *n*-channel oxide TFTs. To achieve high gains and high and balanced noise margins as described in this dissertation, complementary circuits are preferable. Compared with unipolar TFT-based inverters, organic-inorganic hybrid complementary inverters can achieve higher gains and noise margins. Furthermore, complementary inverters can be used to implement more complex circuits including ring oscillators to achieve high performance. To do this, high mobility *p*-channel TFTs are still necessary.

4. Complementary-like circuit integration: Organic-inorganic hybrid ambipolar thin-film transistors (ATFTs) and ATFT-based complementary inverters demonstrated as described in Chapter 5 are attractive because, unlike unipolar TFTs, they operate independently of the sign of the gate voltage. When used in complementary digital circuit configurations, this intrinsic characteristic of an ATFT can simplify circuit design by reducing the number of control lines and by enabling circuits with multifunctional operation. However, there are only a few reports

for circuit applications up to now. For instance, a single digital circuit operating as a logic gate can adaptively operate like two logic gates (i.e. NOR and NAND) depending upon the polarity of the input voltages. We still need to investigate more possible applications such as analog circuits, including mirror circuits.

5. Vertical integration: Most of the conventional complementary circuits based on all organic or organic-inorganic hybrid TFTs have been demonstrated using horizontally distributed *p*- and *n*-channel semiconductors due to the limitations of the fabrication. Vertical integration of the complementary inverters may increase the complexity for the fabrication of the TFTs, however, with respect to circuit performance, the parasitic resistance can be reduced by reducing interconnect distance between TFTs. In addition, this approach can increase the density of circuits by stacking the TFTs vertically.

6.3 Selected publications

6.3.1 Selected articles published in peer-reviewed journals

1. **J. B. Kim**, C. Fuentes-Hernandez, S.–J. Kim, S. Choi, and B. Kippelen, "Flexible hybrid complementary inverters with high gain and balanced noise margins using pentacene and amorphous InGaZnO thin-film transistors", **11**, 1074 *Organic Electronics* (2010).

2. J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage Jr, X.-H. Zhang, and B. Kippelen, "Low-voltage InGaZnO thin-film transistors with Al_2O_3 gate insulator grown by atomic layer deposition", *Applied Physics Letters* **94**, 142107 (2009)

3. **J. B. Kim**, C. Fuentes-Hernandez, and B. Kippelen, "High-performance InGaZnO thin-film transistors with high-k amorphous $Ba_{0.5}Sr_{0.5}TiO_3$ gate insulator", *Applied Physics Letters* **93**, 242111 (2008)

4. Vaibhav Vaidya, **Jungbae Kim**, Joshua N. Haddock, Bernard Kippelen, and Denise Wilson, "SPICE optimization of organic FET models using charge transport elements", *IEEE Transactions on Electron Devices*, **56**, 38 (2009)

5. Andreas Haldi, **Jung B. Kim**, Benoit Domercq, Abhishek P. Kulkarni, Stephen Barlow, Angela P. Gifford, Samson A. Jenekhe, Seth R. Marder, and Bernard Kippelen, "Fabrication of a Blue M × N Pixel Organic Light-Emitting Diode Video Display Incorporating a Thermally Stable Emitter", *IEEE Journal of Display Technology*, **5**, 120 (2009)

6. V. Vaidya, S. Song, **J. B. Kim**, A. Haldi, J. Haddock, B. Kippelen, and D. M Wilson*, "Comparison of Pentacene and Amorphous Silicon AMOLED Display Driver Circuits", *IEEE Transactions on Circuits and Systems-I:Regular Papers* **55** , p.1177 (2008)

7. S. Yoo, W. J. Potscavage, B. Domercq, **J. Kim**, J. Holt, and B. Kippelen, Integrated organic photovoltaic modules with a scalable voltage output", *Applied Physics Letters* **89**, 233516 (2006)

6.3.2 Selected published proceedings and conferences

1. **J. B. Kim**, C. Fuentes-Hernandez, S.–J. Kim, S. Choi, and B. Kippelen, "High gain complementary inverter using pentacene and amorphous InGaZnO channel thin-film transistors on flexible polyethersulfone substrates", *MRS Fall Meeting*, Boston, November 30 – December 04 (2009).

2. **J. B. Kim**, C. Fuentes-Hernandez, S.–J. Kim, W. J. Potscavage Jr, S. Choi, and B. Kippelen, "High-performance ambipolar thin-film transistors and circuits", *MRS Fall Meeting*, Boston, 11/30-12/04 (2009).

3. Jungbae Kim, William J Potscavage, Xiaohong Zhang, Vaihav Vaidya, Denise Wilson, and Bernard Kippelen "Low Voltage High Performance Amorphous InGaZnO based Thin Film Transistors", *MRS Fall Meeting* Symposium B, B5.8, Boston, November 01-05 (2008)

4. William J. Potscavage, Seunghyup Yoo, Benoit Domercq, **Jungbae Kim**, Joe Holt, and Bernard Kippelen, "Integrated organic photovoltaic modules", *Proc. of SPIE* 6656, 66560R-1 (2007)

5. **J. B. Kim**, A. Haldia, S. Yoo, B. Domercq, S. Barlow, C. J. Tonzola, A. P. Kulkarnid, A. P. Gifford, W. Kaminsky, S. A. Jenekhe,, S. R. Marder and B. Kippelen, "An M × N Pixel Blue Organic Light-Emitting Diode Display", *Proc. of the 3rd Americas Display Engineering and Applications Conference*, Atlanta, GA, October 24-26 (2006)

6.3.3 Papers submitted

1. **J. B. Kim**, C. Fuentes-Hernandez, S.–J. Kim, W. J. Potscavage Jr, S. Choi, and B. Kippelen, "Ambipolar thin-film transistors with a co-planar channel geometry", submitted to *Organic Electronics* (2010).

6.3.4 Proceedings and conferences submitted

1. **J. B. Kim**, C. Fuentes-Hernandez, S.–J. Kim, S. Choi, W. J. Potscavage Jr, and B. Kippelen, "The operation and performance of organic/inorganic ambipolar and unipolar thin film

tranisistors and inverters", accepted to t*he 9th International Symposium on Functional π-Electron Systems (F-π-9)*, Atlanta, May 23 – 28 (2010).

2. **J. B. Kim**, C. Fuentes-Hernandez, S.–J. Kim, W. J. Potscavage Jr, S. Choi, and B. Kippelen, "High performance flexible complementary and complementary-like inverters using pentacene and amorphous InGaZnO thin-film transistors", accepted to *SPIE Photonic Devices and Applications*, San Diego, CA, August 1 - 5 (2010).

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