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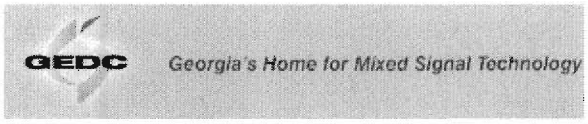

Document Nr.: XXXX
Rev.: 1.0
Security Classification: unclassified, confidential

Technical Progress Report

Linearization circuits for analog optical datalinks

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Executive Summary

This summarizes work performed for Infinera under a STTR project. Goal of this research was to develop linearizing circuits that could meet stringent military requirements. Based our initial designs we proposed advanced structures that could improve well beyond the required performance.

Implementation

To improve the SFDR even further we propose to supplement our transmitter side linearizer with a receiver side linearizer as shown in Figure 1. In Phase I we demonstrated the improvements in linearity of the receiver side linearizer. We will continue optimizing this linearizer and customize it for the improved EA modulator. We also will tape out, fabricate, and completely characterize this linearizer; both as a stand-alone IC as well as in conjunction with the improved EA modulator.

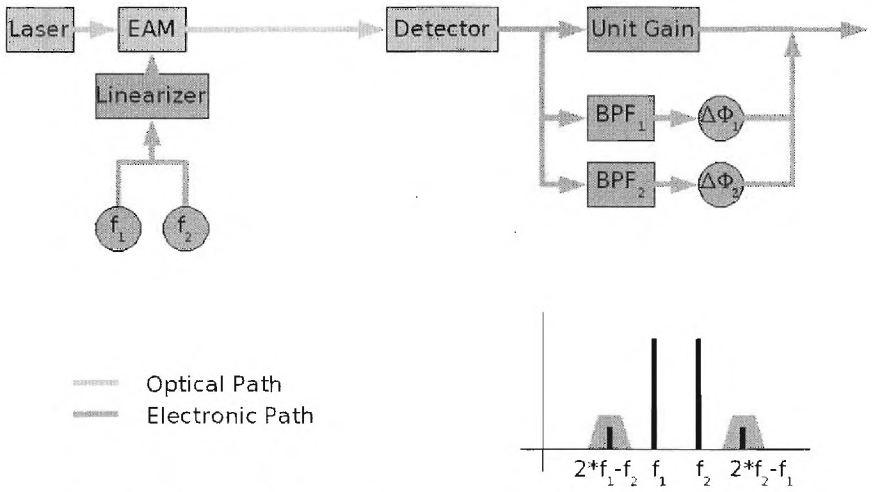

Figure 1: block diagram of a combined transmitter and receiver side linearizing circuit.

Based on our Phase I study, we now know that a transmitter linearizer will most likely not be sufficient to meet the original requirement of > 120dB $Hz^{2/3}$. For that reason we

propose to expand our current design to include a receiver side linearizer that can significantly improve IM3 as shown in Figure 1.

Rationale:

A multitude of linearization techniques have been proposed and demonstrated including feedforward linearizers, reflect forward adaptive linearizers and predistortion linearizers. True to the specific application (airborne deployment in a highly-integrated photonic package) we have chosen a highly effective predistortion linearizer architecture. This linearizer has the distinct advantage that it can be fabricated on a die size of approx. 1 x 1 mm^2 and does not require a second optical modulator. Feed forward linearizers or reflect forward adaptive linearizers typically require that the signal be detected in the optical domain and a correction signal be injected into the optical path. This approach has been proven to be effective, however, it results in rather bulk transmitters that are not necessarily compatible with the weight and space requirements of airborne applications. Our predistortion linearizer is designed true to the overarching idea of a highly integrated PIC. To further improve the IM3 performance we propose to implement a receiver side linearizer in combination with the transmitter side predistortion linearizer, resulting in superior end-to-end linearity and addingflexibility and adaptability to the overall system.

Description of the transmitter side linearizer

See previous report.

Description of receiver side linearizer

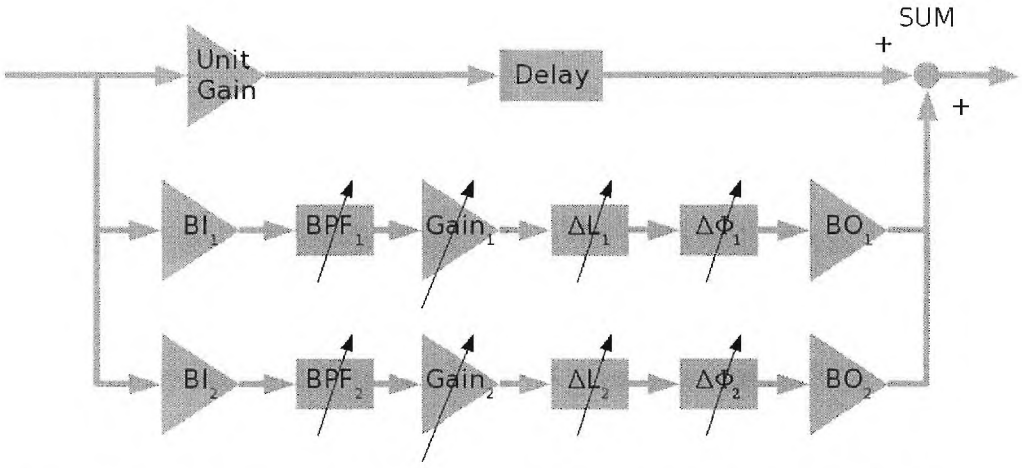

Figure 2: Block diagram of the receiver linearizer. BI/BO: buffered input/output, BPF: bandpass filter.

A detailed block diagram of the receiver side linearizer is shown in Figure 2. The receiver linearizer is implemented as an analog circuit using standard bi-CMOS technology at the 0.180 μm node to achieve sufficient bandwidth for 20 GHz signals. The input signal is tapped and split into two separate signal paths. Since the output of the photo receiver is terminated (are you sure you mean terminated, I don't think this sentence makes sense) into 50, Ω *input buffers* (BI_1 and BI_2) are necessary. These input buffers establish high input impedance and avoid loading the main signal path. The *bandpass filters* BPF_1 and BPF_2 filter out the IM3 inter-modulation product at $2f_1 - f_2$ and $2f_2 - f_1$. These filters will be implemented as tunable filters and depending on the exact NAVY requirements a switchable filter bank can be used to cover the full 20 GHz frequency band. The subsequent *variable gain amplifier* accomplishes two tasks: 1) provides appropriate signal amplitude $|2f_1 - f_2|$ or $|2f_2 - f_1|$ to exactly match the main signal path and 2) provides a 180° phase shift to enable interferometric cancellation with the signal path at the summation point. The *delay* ΔL provides fine tuning to compensate for process

variations and to match delay relative to the main signal path. In previous designs we have learned that it is opportune to add a separate *phase delay* $\Delta\Phi$ to fine tune the relative phase of the tapped signal relative to the main signal path. After this phase delay, the proposed circuit makes available two out of (two out of What?)phase IM3 signal that will be used to cancel the original IM3 signals. The *output buffer* BO_1 and BO_2 establishes high output impedance and avoids loading of the main signal path. In addition to the *unity gain* element in the main signal path, a *delay element* guarantees the constructive interference of the IM3 signals after the *summing node*.

The whole circuit including a switchable filter bank can be implemented in an integrated circuit of approx. 1 x 3 mm^2 and will be fully compatible with Infinera's PIC transmitter and receiver module.

Circuit Level implementation:

Key components of this IM3 canceller are the two variable gain amplifiers (VGAs) that also provide a 180° phase shift. Many approaches have been proposed to accomplish this goal. Our objective is to utilize on-chip integration using standard IC processes. We previously designed similar variable gain amplifiers using voltage controlled Gilbert cell based VGAs with 180° analog active phase rotators as shown in Figure 3. This circuit operates from a 1.8 V supply and is capable of accepting a few hundred mV of input swing. It is important to note that the design does not require any inductive elements.

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Figure 3: Layout of a Gilbert cell based variable gain amplifier and phase shifter.

Feasibility:

To demonstrate feasibility of this approach we simulated a transmission link that includes the predistortion circuit (developed in Phase I of this project), the EAM and ideal fiber span and optical receiver and our receiver linearizer. (is there a way to make this sentence two different sentences because it is a run-on) We believe these assumptions are justified since to the best of our knowledge this specific NAVY application will use relatively short fiber spans (as compared to link spans of communications links). The simulations were performed using ADS. If longer fiber spans are required we will be able to add equalizers to the electronic design. We are currently developing electro-optic capabilities using OptSim/ADS co-simulations to account for this possibility.

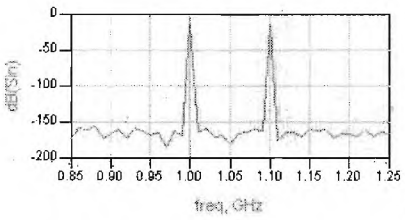
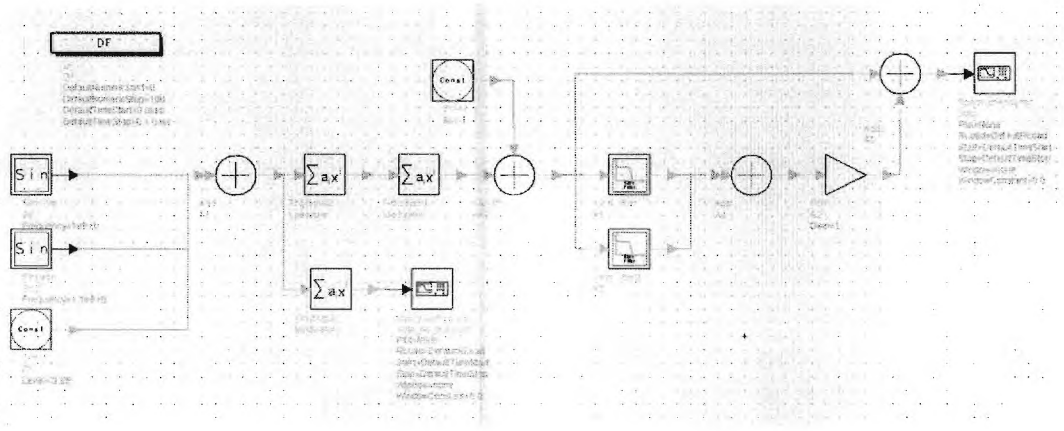


Figure 5: Input signal into transceiver equalizer

For this feasibility study we chose two tones around 1.0 GHz with spacing of 100 MHz and an input power of -30 dBm per channel as shown in Figure 5. After the predistorter developed in Phase I and using measured EAM transfer functions we inject the signal into the receiver linearizer shown in Figure 2. An idealized ADS implementation of this linearizer is shown in Figure 4. As shown in the figure above, the setup consists of two complimentary linearization techniques. The transmitter side linearization was demonstrated in Phase I and is incorporated in this simulation (but



not shown here for clarity). The receiver side linearization consists of ideal filters, variable gain blocks, and are followed by the summing block. The finallinearized output is monitored by the spectrum analyzer. Figure 6 shows a comparison between the effect of the transmitter linearizer as well as both the transmitter and receiver linearizer on IM3. The simulations assume a noise floor of -150 dBm. The improvement in SFDR is approx. 80 dB.

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Figure 6: Output spectrum of combined transmitter and receiver. Red: transmitter linearizer only; blue: transmitter and receiver linearizer.

Risk Assessment

Clearly a SFDR improvement of 80dB is not realistic. This large value is due to the strong simplifications that have been made for this study. We expect significant performance degradations for the physical circuit implementations. The most important degradation mechanisms are jitter and non-ideal performance of the band pass filters. The contribution of jitter is that at the summing node the out of phase signal will not completely cancel. The proposed architecture has a fine-tuning mechanism that allows for fine alignment. In this way, we are able to compensate for things such as process variations and drift. However, such fine-tuning is generally not capable to compensate for fast random fluctuations in timing. In addition the actual performance of the receiver linearizer will strongly depend on the quality of the bandpass filters. High Q filters are highly desirable for superior performance. Various techniques to implement high Q filters are well known, however the specific technique is strongly dependent on

the specific requirements. We will select the appropriate filter technology when we get a better understanding of the NAVY's specification.

With all these caveats, our experience with similar linearization techniques and based on measured data, our conservative guess is that a IM3 improvement of at least 20 dB is feasible with the receiver linearization described above. (previous sentence does not make sense) Using a similar approach as described above for a wireless system we were able to demonstrate improvements of between 15 dB and 30 dB over a wireless channel[1].

Conclusions

We have demonstrated that a transmitter linearizer is capable of improving SFDR of an EAM by 18dB. To further improve the SFDR we propose to implement a receiver linearizer. This receiver linearizer has potential to improve SFDR by an additional 20 dB. The overarching goal of our linearizer design is to be consistent with NAVY airborne requirements and will not require any modification of Infinera's optical photonic integrated circuit. Moreover, the proposed circuits will be fast tunable and fully capable to meet requirements of frequency hopping military wireless transmission systems.

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[1] A. Raghvan, Gebara, E., Tentzeris M., and Laskar J. "An Active Interference Canceller for Multistandard Collocated Radio", IEEE MTT-S Microwave Symposium Digest, 2005, pp. 723-726.