DEVELOPEMENT OF HIGH-EFFICIENCY SOLAR CELLS ON THIN SILICON THROUGH DESIGN OPTIMIZATION AND DEFECT PASSIVATION

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Manav Sheoran

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DEVELOPEMENT OF HIGH-EFFICIENCY SOLAR CELLS ON THIN SILICON THROUGH DESIGN OPTIMIZATION AND AND DEFECT PASSIVATION

Approved by:

Dr. Ajeet Rohatgi, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Phillip N. First
School of Physics
Georgia Institute of Technology

Dr. Walter A. de Heer
School of Physics
Georgia Institute of Technology

Dr. Mei-Yin Chou
School of Physics
Georgia Institute of Technology

Dr. Miroslav M. Begovic
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: February 09, 2009

This work is dedicated to

my mother, Mrs. Hemvati Sheoran

my father, Mr. Mahipal Singh Sheoran

my brother and mentor Mr. Pranav Sheoran

my sister in law Mrs. Ritvika Sheoran

my friends, for their support, love and patience.

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Without Sun, this world, solar PV, and this thesis would not have been possible. So I start by offering a prayer to the God of the Sun:

ॐ विश्वानि देव सवितर्दुरितानि परासुव। यद् भद्रं तन्न आसुव।

यजुर्वेदः, ३०: ३

(O God, the creator of the universe (sun) and the giver of all happiness. Keep us far from bad habits, bad deeds, and calamities. May we attain everything that is auspicious.) **Yajur Veda, 30: 3**

तमसो मा ज्योतिर्गमय

(From darkness to light)

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Many times, apparently complex problems have a simple diagnosis, provided you use the right approach. This thesis is no different.

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LIST OF SYMBOLS AND ABBREVIATIONS

τ	Recombination lifetime or lifetime
τ_b	Bulk lifetime
τ_{eff}	Effective lifetime
τ_{n0}	Characteristic electron lifetime
τ_{p0}	Characteristic hole lifetime
$\Delta n/\Delta p$	Injection level or excess carrier density for electrons/holes
a-Si	amorphous Si
c-Si	Crystalline Si
J_0	Reverse saturation current density
J_{01}	1st diode reverse saturation current density
J_{02}	2nd diode reverse saturation current density
J_{sc}	Short-circuit current density
mc-Si	multi-crystalline Si
n_2	2nd diode ideality factor
Q_{FB}	Flat band equivalent charge density
R_s	Series resistance
R_{sh}	Shunt resistance
S_{n0}	Characteristic electron surface recombination velocity
S_{p0}	Characteristic hole surface recombination velocity
SiN_x	Silicon nitride
V_{oc}	Open-circuit voltage

Al-BSF	Aluminum back-surface field
ARC	Antireflection coating
BSRV	Back surface recombination velocity
BSF	Back surface field
Cz	Czochralski
FF	Fill factor
FGA	Forming gas anneal
FSRV	Front surface recombination velocity
FZ	Float zone
HEM	Heat exchanger method
IQE	Internal quantum efficiency
I-V	Current-Voltage
LBIC	Light beam induced current
LBSF	local back surface field
LID	Light-induced degradation
NREL	National renewable energy laboratory
PECVD	Plasma-enhanced chemical vapor deposition
PV	Photovoltaics
RTP	Rapid thermal processing
SEM	Scanning electron microscope
SIMS	Secondary ion mass spectrometry
SRH	Shockley-Read-Hall
SRV	Surface recombination velocity

SUMMARY

Photovoltaics (PV) has the potential of solving world's energy and the environmental problems simultaneously by converting sunlight into electrical energy with zero emission and zero pollution. However, PV comprises of < 0.1% of the world's energy portfolio today. This is because the cost of PV generated electricity is a factor of two to four times more expensive than the conventional energy sources. Crystalline silicon (Si) based modules currently account for ~90% of the total PV modules produced and Si alone accounts for ~50% of the cost of a module. Therefore, use of a thinner, cheaper or lower quality Si material can have a significant impact on cost reduction provided no significant compromise in efficiency is made. Therefore the focus of this research is to investigate the potential of lower quality cast multicrystalline Si (mc-Si) as well as thin single and mc-Si cells.

The overall goal of this research is to improve fundamental understanding of the hydrogen passivation of defects in low-cost Si and the fabrication of high-efficiency solar cells on thin crystalline silicon through low-cost technology development. This is addressed by a combination of five research tasks. The key results of these tasks are summarized below.

The silicon nitride (SiN_x) coating on the front side of a solar cell not only acts as an anti-reflection coating but also passivates the defects in the bulk of the low-cost solar cell materials by releasing the hydrogen during the contact formation cycle. In order to achieve maximum benefit from this process, a better understanding of hydrogen (H) release and diffusion in Si is nessary. In *task 1*, a novel method was developed to determine the concentration and flux of H diffusing into the Si. This method involved the

deposition of deuterated silicon nitride (SiN_x:D) on the front and sputtered amorphous Si film on the rear side of float zone (FZ) wafers. The samples were annealed for different times and temperatures during which the deuterium released from the SiN_x film migrates through the FZ Si wafer and is captured in the sputtered amorphous Si layer on the rear. The concentration of this trapped deuterium (D) is then measured by secondary ion mass spectrometry (SIMS). This study led to several important findings. The minimum concentration of D injected into the Si was estimated to be 4.7 x 10^{15} cm^{-3} for a short anneal time of 1 s at 750 °C. The captured D content in the sputtered Si layer increases with the anneal time. However, the flux of D injected into the silicon from the SiN_x layer decreases as anneal time increases. The flux values for various anneal times were correlated with the lifetime enhancement of defective String ribbon Si wafers. It was found that a higher flux for shorter anneal times leads to an enhanced defect passivation in low-cost Si. It was concluded that the higher flux of H during the short rapid thermal processing (RTP) anneal is responsible for the observed enhanced hydrogenation of the defects in Si, even though the total amount of H injected into the Si is less. Higher flux leads to a greater net association with the defects in the c-Si bulk, prior to cooldown, because of the constant dehydrogenation from the defects at high temperatures. At an anneal temperature of 750 °C, D was found to penetrate through a 575 μm thick wafer in as little as 1 second peak anneal time in an RTP system. It was found that the presence of a capping layer of SiN_x:H on top of the SiN_x:D leads to more D injection inside the bulk Si, which would otherwise be lost to the ambient. Measurements of penetrated D concentrations at higher anneal temperatures of 800 and 850 °C showed a much higher amount of D diffusing through the c-Si compared to 750 °C anneals. For similar anneal

times, the D flux at 800 and 850 °C was found to be much higher compared to the flux at 750 °C. However, the lifetime enhancement in defective String Ribbon Si was higher at 750 °C anneal. This is attributed to the faster increase in the dehydrogenation rate at higher temperatures compared to the increase in flux. Study of D diffusion at lower temperatures showed that for the SiN_x films deposited at 400 °C, D starts to diffuse at temperatures as low as 525 °C for 600 s anneal. The amount of D diffusing through the c-Si increases sharply as the anneal temperature is increased above 525 °C.

The understanding of defect passivation acquired in task 1 was used to fabricate high-efficiency solar cells on cast mc-Si wafers in *task 2*. An optimized co-firing process was developed, which resulted in ~17% efficient 4 cm^2 screen-printed solar cells with single-layer AR coating, and no surface texturing or selective emitter. The HEM mc-Si wafer gave an average efficiency of 16.5%, with a maximum of 16.9%. The identical process applied to the un-textured Float zone (FZ) wafers gave an efficiency of 17.2%. These cells were fabricated using the same simple, manufacturable process involving $POCl_3$ diffusion for a 45 Ω/sq emitter, PECVD SiN_x:H deposition for single-layer antireflection coating and rapid co-firing of a Ag grid, an Al back contact, and Al-BSF formation in a belt furnace. These high efficiencies are attributed to the combination of effective gettering and hydrogenation, good ohmic contacts, and effective BSF achieved by this rapid process scheme. It is shown that if the lifetime during processing can be enhanced above a certain threshold (~100 μs for this cell design), the as-grown lifetime becomes relatively inconsequential. We were able to raise the bulk lifetime exceeding 100 μs in the finished cells to obtained a tight efficiency range of 16.6-16.8%, even though the starting lifetimes in the cast mc-Si wafers were in the range of 4 -70 μs. Using

a similar process sequence, a high-efficiency of 17.1% was achieved on high sheet-resistance HEM mc-Si with good quality contacts. In the second part of this task, the effects of changing several device parameters on the efficiency of the solar cells was modeled with PC1D and guidelines were established to improve the efficiency from ~17% to over 20% cells on low lifetime (100 μs), thin (140 μm) silicon wafers.

The understanding of enhanced defect hydrogenation and the optimized fabrication sequence in the previous two tasks was applied to fabricate high-efficiency solar cells on top, middle, and bottom regions of several mc-Si ingots in *task 3*. Screen-printed solar cells were fabricated on different regions of four boron doped ingots and one gallium doped ingot. High post-diffusion and post-hydrogenation lifetime values were obtained, which resulted in high-screen printed cell efficiencies of ≥ 15.9% for wafers from all the regions and ingots, except for the bottom region of the lower-resistivity boron-doped ingot and the gallium-doped ingot. Using a lower-resistivity boron-doped mc-Si ingot did not improve the efficiency. As expected, the concentration of oxygen in the three boron-doped ingots was found to increase from top to bottom. At a concentration of 14 ppm in a 2 Ω·cm resistivity wafer, about 2.5% (relative) light-induced degradation (LID) in efficiency was observed. A relatively tighter and superior distribution in efficiency was found for the boron-doped ingot compared to the gallium-doped ingot. However, the gallium-doped ingot was found to be very stable under illumination, irrespective of the location of the wafer in the ingot. Device modeling showed the merit of tailoring the thickness, based on the doping and the bulk lifetime, aimed at achieving a more uniform and optimized efficiency distribution over the entire ingot. Device modeling showed that thinner wafers with good back surface

recombination velocity (BSRV) can reduce the impact of resistivity and lifetime variations in the mc-Si ingot. Solar cells were fabricated on wafers from top, middle and bottom regions of cast multicrystalline silicon ingots with resistivities of 1.5 Ω·cm and 0.6 Ω·cm and thicknesses of 225 μm and 175 μm from the same supplier. The expected increase in the performance with increased doping was not realized, however, V_{oc} enhancement was observed for the lower resistivity cells despite significantly lower bulk lifetimes compared to higher resistivity cells. The low lifetime in the low resistivity ingot was attributed to the dopant-defect interaction, which lowered the lifetime in mc-Si. After gettering (during P diffusion) and hydrogenation (from SiN_x) steps used in cell fabrication, the bulk lifetime in 225 μm thick wafers from the middle of the ingot decreased from 253 μs to 135 μs when the resistivity was lowered from 1.5 Ω·cm to 0.6 Ω.cm. An increase in the average V_{oc} of up to 4 mV was observed upon decreasing the base resistivity, which was counterbalanced by the loss in lifetime and J_{sc}. Consistent with PC1D modeling, solar cells fabricated on 175 μm thick, 1.5 Ω·cm, wafers showed no appreciable loss in the cell performance compared to the 225 μm thick cells. Device modeling was performed to show that the dopant-defect interaction has the effect of increasing the optimum base resistivity to higher values. Solar cells fabricated on the first two ingots grown by a novel process, which produced single-crystal Si wafers by HEM casting method, achieved efficiencies of 16% and 17.2% on planar and textured surfaces, respectively. Lifetime in the middle region of both the ingots exceeded 100 μs after cell processing; however top and bottom regions had lower lifetimes due to the impurities that could not be gettered or passivated. Due to the single-crystal nature of the mono-cast ingots, the wafers were textured easily, which decreased the front surface reflectance

from 11.8 to 5.3% and resulted in an enhanced J_{sc} by ~ 3mA/cm^2. Large area (100 cm^2) solar cells fabricated from the middle regions of this novel mono-cast material achieved an efficiency of 16.5%. The mono-cast grown by the HEM process is still under optimization, however, these results show that the material has a great potential for achieving high-efficiencies at a lower cost.

Since the cost of Si material alone is ~50% in a PV module, therefore, in *task 4*, attempts were made to fabricate thin Si cells with full area Al-BSF and to identify the key factors responsible for efficiency loss in thin cells with conventional Al-BSF. The contact firing cycle for each thickness was adjusted so that all the wafers experience the same peak contact firing temperature. Planar solar cells were fabricated on HEM mc-Si wafers along with single crystal FZ silicon, grinded down to desired thickness. Selected cells were also fabricated with low and high sheet-resistance emitters to evaluate the influence of emitter design on thin cells. All cells were 4 cm^2 screen-printed with a single layer SiN_x antireflection (AR) coating and a full area aluminum back-surface field (Al-BSF). Screen-printed cell efficiencies of 17.8 and 18.5% were achieved on 125 μm and 300 μm thick textured FZ wafers, respectively, with high sheet-resistance emitters (80-100 Ω/sq). Screen-printed cell efficiencies of 16.4 and 16.8% were achieved on 115 and 150 μm thick planar HEM mc-Si cells with a high sheet-resistance emitter. The 0.5-1% difference in the efficiency of thick and thin cells was analyzed by detailed cell characterization and PC1D modeling. The processed bulk lifetime was found to be in excess of 200 μs for all the cells, which made the thin cells more sensitive to BSRV and less dependent on lifetime. It was found that the high BSRV (300-400 cm/s) and low back surface reflectance (BSR) (63-70%) associated with the full area Al-BSF were the major reasons

for the reduced performance of thin cells. Model calculations showed that a BSRV of ≤ 100 cm/s and BSR of ≥ 95% can virtually eliminate the efficiency gap between 300 μm and 115 μm thick cells for these ≥ 200 μs bulk lifetime wafers. Manufacturing cost modeling showed that reducing the mc-Si wafer thickness from 300 μm to 115-150 μm reduces the module manufacturing cost in spite of ~1% lower cell efficiency.

Full area Al-BSF cells in task 4 suffered efficiency loss upon thinning due to a relatively higher BSRV and poor BSR of Al-BSF. Therefore, in *task 5,* attempts were made to fabricate, characterize and model, a device structure with local back-surface field. In this task, thin solar cells, without any bowing, were fabricated using the dielectric passivated structure and screen-printed contacts. The process sequence involved the deposition of a spin-on dielectric layer on the rear (planar) side of a single-side textured FZ wafers. This was followed by the curing of the spin-on dielectric, formation of an n^+ emitter on the textured front side, and formation of an in-situ front oxide in a single furnace anneal step. After the deposition of SiN_x on both sides, Ag grid was screen-printed on the front and Al dots on the rear. Front and rear local contacts were formed by co-firing in a belt furnace followed by the deposition of Ag reflector on the rear. The spin-on dielectric layer capped with SiN_x was found to provide a very good and stable surface passivation, even after a firing step, with low SRV values of < 40 cm/s on ~2 Ω·cm FZ wafers. A high average implied V_{oc} of 677 mV was measured on the test structures after the co-firing cycle without the presence of metals. In addition, the charge density in the dielectric stack was found to be low ($2\text{-}3 \times 10^{11}$ cm^{-2}), which reduced the parasitic shunting of the rear contacts relative to the SiN_x layer alone. Scanning electron microscopy (SEM) micrographs of the rear local contacts showed a local BSF formation

underneath the contacts with an SRV value of ~1000 cm/s, calculated through effective lifetime measurements. A 29 mV loss in V_{oc} was observed after the application of the front and rear contacts, measured with suns V_{oc} measurements. High screen-printed solar cell efficiencies of 19.4, 19.2, and 19.2% were achieved on 300 μm thick full area Al-BSF, LBSF cell with evaporated Ag reflector, and LBSF cell with screen-printed Ag paste reflector, respectively. The corresponding efficiencies on 140 μm thick cells were 18.3, 18.7, and 18.4%. This process sequence is compatible with thin cell fabrication and resulted in bow-free devices. The V_{oc} and J_{sc} for the thin LBSF cells was higher than the full area Al-BSF cell, however, their performance was limited by low FF and high series resistance partly due to somewhat non-uniform punch through of local contacts and BSF. Hence, in its present form, this fabrication sequence is not yet capable of achieving efficiencies over 20% on thin substrates, but further improvements or modifications to the metallization sequence might be able to get there. Enhancement in V_{oc} and J_{sc} of these LBSF solar cells was clearly reflected in the long-wavelength LBIC and the IQE response. Device modeling in the PC1D revealed high BSR values in the range of 96-98% for the dielectric passivated cells compared to a low value of 65% for the full area Al-BSF cells. The rear dielectric stack was able to provide low BSRV values of 125 cm/s compared to a BSRV in the range of 300-500 cm/s for the full area Al-BSF. I-V parameters for the dielectric cells matched quiet well with the one dimensional PC1D modeling by the introduction of a rear surface charge and a rectifier shunt diode introduced between the inversion layer and the rear contact.

CHAPTER 1

INTRODUCTION AND RESEARCH OBJECTIVES

1.1. Photovoltaic market overview

World energy consumption and demand have been increasing at a steady pace. Traditionally, this demand for energy has been fulfilled by fossil fuels (Oil, coal, and natural gas), which are depleting rapidly. Use of fossil fuels also injects harmful greenhouse gases in the atmosphere, resulting in global climate changes. Other sources of energy production include nuclear and renewable energy. Nuclear energy, apart from being potentially dangerous to produce, still has problems of nuclear waste disposal. Renewable energy, which provides alternative to these problems, comprised of only ~18% of the world energy portfolio in 2006, however, its share has been increasing steadily in the past few years. Figure 1.1 shows the fuel shares of the world total primary energy supply in 2004 [1]. Even though energy from the sun is virtually unlimited, solar energy comprises of < 1% of the world energy portfolio. Solar photovoltaics (PV), which is the direct conversion of sunlight to electricity, comprises of only 0.04% of the global energy consumption. The main challenge in PV is the cost of energy production. Figure 1.2 shows that the current PV module price is 3-4 $/W, which is about two-four times more expensive than the conventional energy produced from fossil fuels. For PV to be competitive, the cost of PV modules needs to be ~1 $/W. In spite of its high cost, PV has been growing at a rate of ~40% since 1998. In the year 2007, world PV market grew by 62% and reached 2.8 gigawatts peak (GWp) with $17.2 billion in global revenues [2]. Fig.

1.3 shows that more than 90% of the installed PV is in Germany, Japan, and United States [3].

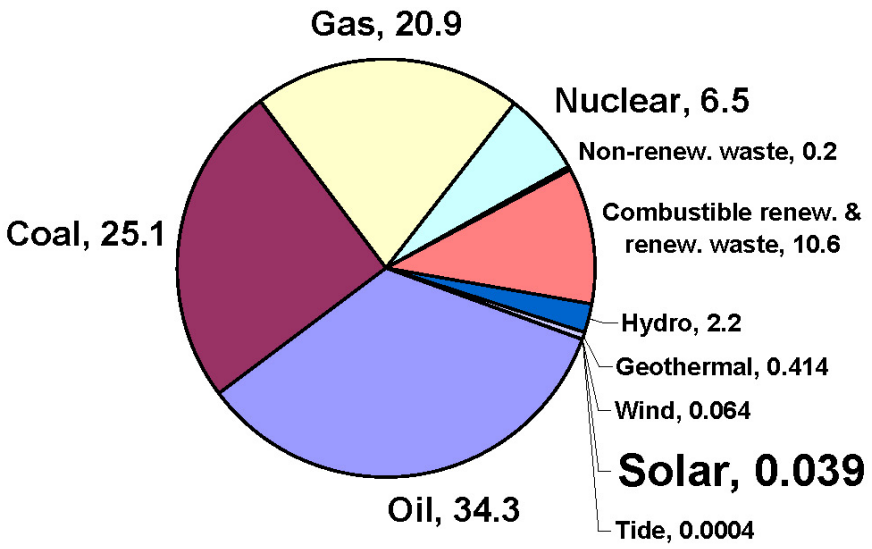


Figure 1.1 Fuel shares of the world total primary energy supply in 2004 [1].

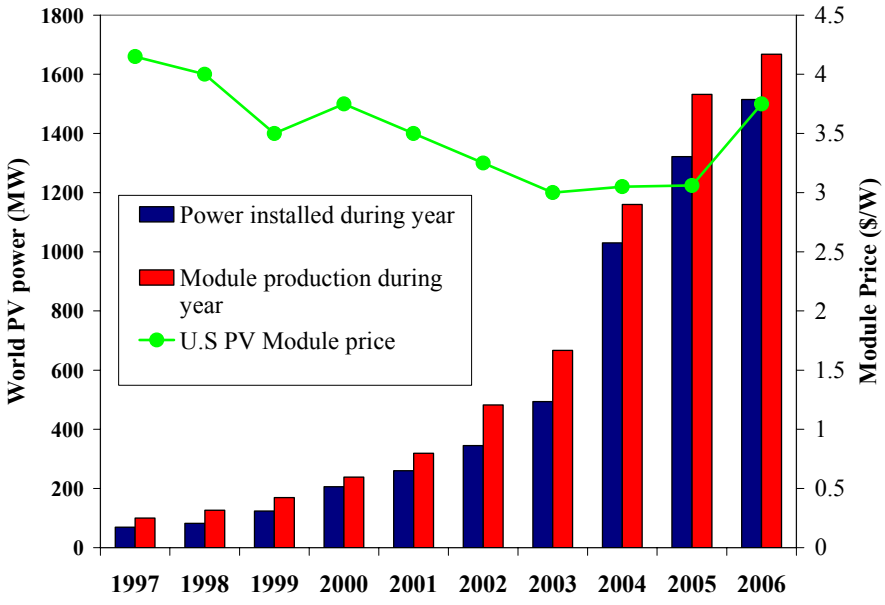


Figure 1.2 Global installed power and modules produced during the years 1997 to 2006. Figure also shows the U.S module price during this period [3].

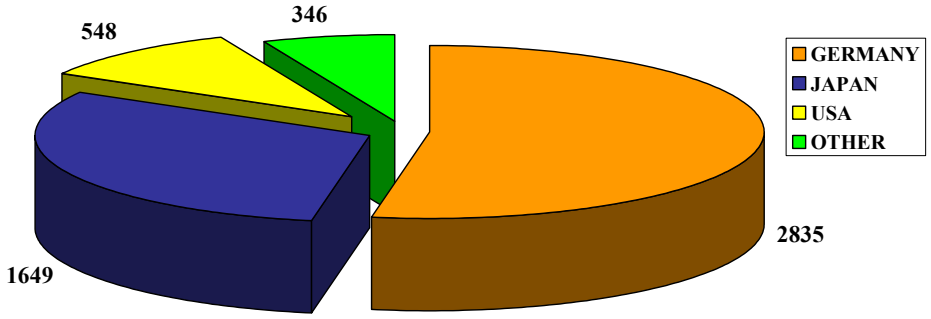


Figure 1.3 Total PV power installed in the period 1995-2006. Other denotes the rest of the countries reported by the EIA [3].

1.2. Motivation

Crystalline silicon (c-Si) currently accounts for ~70% of the total modules produced in the U.S and ~90% of the modules produced worldwide. To achieve grid parity, the point at which PV generated electricity is equal to or cheaper than the power from the grid, the target module cost is ~1 $/W. Since cost of Si wafer alone is currently ~50% in a module [4], the module cost can be significantly reduced by producing high-efficiency solar cells on a thinner and lower-cost Si. This provided the motivation for this research. Figure 1.4 shows the U.S PV cell and module shipments by material type for the years 2004 to 2006 [3]. Due to the recent shortage of Si, thin film solar cells have increased their share to ~10%. Within the c-Si modules, the cheaper cast and ribbon Si materials account for ~60%, and the remainder is accounted for by somewhat more expensive single-crystal Float Zone (FZ) and Czochralski (Cz) Si. The low-cost c-Si

substrates (cast and ribbon) contain appreciable amount of impurities and defects, which tend to lower the cell performance, compared to the single-crystal Si. Hence in addition to using a thinner substrate, material quality enhancement during the solar cell processing can play a very important role in achieving high-efficiency cells and lowering the module cost. Therefore the overall goal of the research is to fabricate high efficiency solar cells on lower-cost thin Si substrates through defect engineering and cell design.

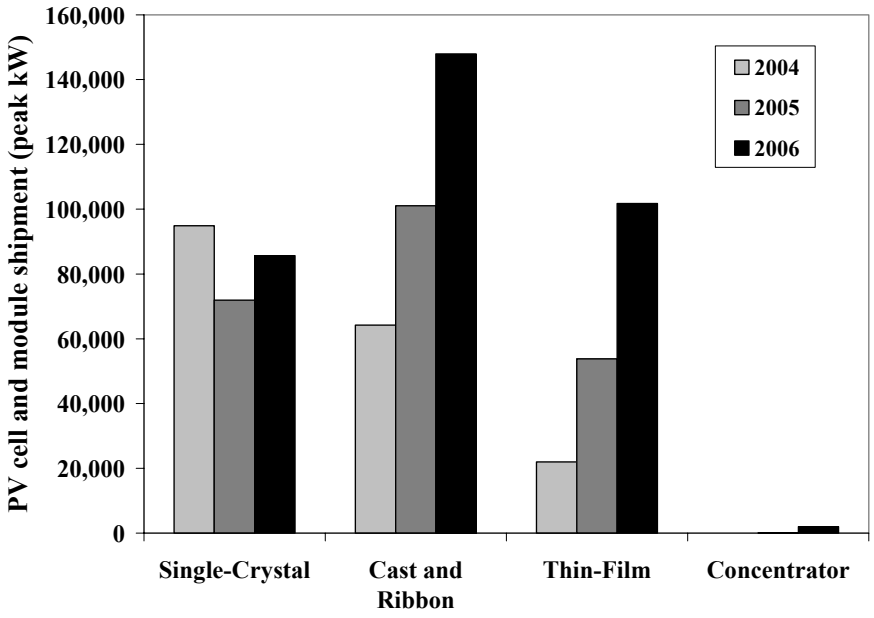


Figure 1.4 U.S PV cell and module shipment by type for the years 2004 to 2006 [3].

1.3 Specific Research objectives

The overall objective of the research is to develop high-efficiency solar cells on thin crystalline silicon through technology development and fundamental understanding of the hydrogen passivation of defects. Cost of Si alone is ~50% of the cost of a current Si solar cell module because of the high cost of feedstock Si. Both higher efficiency and the use of thinner Si can reduce the amount of Si in a PV module. In addition, use of

cheaper but slightly lower quality multicrystalline silicon (mc-Si) can lead to further cost reduction of Si PV if cells of comparable efficiencies can be achieved. This research attempts to accomplish this goal by a combination of fundamental understanding of the passivation of defects in mc-Si to improve the material quality during cell processing and the development of a low-cost screen printing technology to achieve high-efficiency solar cells on thin crystalline Si. This thesis is divided into 5 tasks. Task 1 deals with fundamental understanding of the hydrogen diffusion into Si from the SiN_x anti-reflection (AR) coating and passivation of defects in mc-Si in order to improve the quality of the mc-Si material during cell processing. The understanding of the enhanced hydrogenation of defects in task 1 is used to develop a process sequence and fabricate high-efficiency solar cell on mc-Si in task 2 along with the investigation of solar cells fabricated on mc-Si with low, medium, and high as-grown lifetime. In task 3, process-induced bulk lifetime enhancement is investigated in the top, middle, and bottom regions of HEM mc-Si ingots and co-related with the nature of impurities and defects in those regions. High-efficiency solar cells were fabricated on wafers from top, middle, and bottom regions of several HEM mc-Si ingots and two novel mono-cast HEM ingots. In task 4, solar cells are fabricated on thin silicon wafers with conventional full area aluminum back surface field (Al-BSF) and detailed analysis is preformed to identify key factors responsible for the efficiency loss in thin cells. Finally, in task 5, a low-cost process is developed with dielectric back and local BSF to achieve high-efficiency cells on thin crystalline silicon. This novel process involved the fired-through aluminum point contacts through the dielectric passivation on the rear surface of the solar cells. This resulted in high-efficiency solar cells on thin silicon, without any wafer bowing.

1.2.1 Task 1: Understanding of hydrogen diffusion in the underlying silicon from the PECVD silicon nitride film during the contact firing

mc-Si generally contains several defects including metals, metal precipitates, oxygen, oxygen donors, grain boundaries, and dislocation etc. These defects tend to lower the bulk lifetime and the conversion efficiency. Hydrogen (H), released from the PECVD SiN_x antireflection coatings during the contact firing is known to diffuse into the Si and passivate the defects. However, an improved understanding of the hydrogen diffusion kinetics (amount of H diffused, flux, and retention at the defects) can be highly instrumental in improving the lifetime of lower quality mc-Si. In this task, the amount of H introduced into the Si and the flux of hydrogen during the annealing of the SiN_x film for various annealing cycles is determined by a novel method which involves sputtering amorphous Si on the back side of single crystal wafers. Deuterium (D), the stable H isotope, is used to replace H in the SiN_x films to monitor and track the diffusion of H through the Si. Upon annealing, D released from the SiN_x films is injected into the underlying Si, diffuses through the Si, and is then captured by the sputtered Si films on the rear side. The trapped D in the sputtered film is analyzed by Secondary Ion Mass Spectrometry (SIMS). From the areal density of the trapped D in the sputtered Si films, the minimum amount of D injected into the Si during the annealing cycle is determined. The flux of D in the Si during the annealing is determined and co-related with the lifetime enhancement of the defective mc-Si. This understanding is used to tailor the contact firing cycle to achieve effective defect passivation in low cost mc-Si.

1.2.2 Task 2: Fabrication of high efficiency baseline mc-Si solar cells on low, medium, and high as-grown lifetime wafers.

This task involves the development of a cell process sequence to implement the understanding of effective hydrogenation of defects from task 1. More specifically, a contact firing cycle is designed to achieve maximum bulk lifetime and a superior contact formation, both at the same time, in the finished device. Complete solar cells were fabricated to achieve high-efficiency, un-textured, screen-printed heat exchanger method (HEM) mc-Si cells with a single layer of SiN_x antireflection coating and were analyzed in detail. High-efficiency solar cells were fabricated on mc-Si wafers with low, medium, and high as-grown lifetimes to demonstrate that an optimized process sequence with effective gettering and hydrogenation can shrink the efficiency gap of cast mc-Si ingot, in spite of appreciable difference in as-grown material quality. Finally, device modeling was performed in this task to establish the requirements for achieving high efficiency cells on low lifetime material. Effect of parameters such as bulk lifetime, resistivity, thickness, and surface recombination velocity was examined through device modeling, to provide guidelines to achieve 18-20% efficient cells on low lifetime, thin Si material.

1.2.3 Task 3: Investigation of solar cells fabricated from different regions of HEM mc-Si ingots

The optimized process sequence in task 2 was applied to fabricate high-efficiency solar cells on top, middle, and bottom regions of several mc-Si ingots. This task also deals with the understanding of the degree of process-induced lifetime enhancement in mc-Si wafers from top, middle, and bottom regions of mc-Si ingot. Attempt was made to explain the difference in the degree of bulk lifetime enhancement on the basis of defects and impurities contained in wafers from different regions of the ingot. Device modeling is used to provide guidelines to minimize the efficiency variation due to variation in lifetime in different regions of the ingots. Solar cells fabricated on the first two ingots

grown by a novel process, which produced single-crystal Si wafers by HEM casting method are also investigated in this task.

1.2.4 Task 4: Solar cells fabricated on thin silicon with full area aluminum back surface field

Si wafer alone accounts for about ~50% of the current module cost; therefore the cost of Si PV can be reduced significantly by using thinner silicon substrates. Other benefits of thinner Si wafers include lower loss in efficiency due to light-induced degradation, better utilization of lower quality material, and better performance for selected cell structures. This provided the motivation to investigate solar cells made on thin silicon wafers in this task. Since thinner wafers heat up and cool down faster, the contact firing cycle for each thickness was tailored to ensure that all the wafers experience the same peak contact firing temperature in the belt furnace. This is necessary for accurate evaluation of the impact of thickness reduction alone. The effect of lowering the resistivity and thickness of screen-printed mc-Si, with full areal Al-BSF, is investigated and the difference in the efficiency is analyzed by detailed cell characterization and device modeling. Guidelines are presented for enhanced performance of thin cells. Finally, cost modeling is performed to assess the combined impact of thickness reduction and efficiency loss on the module manufacturing cost.

1.2.5 Task 5: Design and fabrication of dielectric passivated local back-surface field solar cells on thin silicon

Solar cells fabricated on thin silicon with conventional full area Al-BSF suffer from bowing due to stress and a loss in efficiency due to higher back surface recombination velocity (BSRV) and lower back surface reflection (BSR). To address this issue, in this task, a new contact technology with local BSF is developed which involves

a spin-on oxide capped with a SiN_x layer for back surface passivation. Ohmic contacts are made by co-firing the screen-printed Ag grid on the front and Al point contacts through the dielectric stack on the rear. A low-temperature Ag paste is screen-printed on the rear to provide good BSR. Low value of BSRV provided by the oxide/SiN_x passivation and high value of BSR provided by Ag reflector on the rear produces high-efficiency cells on thin crystalline silicon, without any bowing.

CHAPTER 2

OPERATING PRINCIPLES AND DEVICE PHYSICS OF SOLAR CELLS

2.1 Introduction

This chapter discusses the operating principles and the device physics of a solar cell. Section 2.2 discusses the basic equations that describe the conversion efficiency of a solar cell along with the key cell parameters used throughout this thesis. Section 2.3 discusses the device physics of a Si p-n junction solar cell. The principles of carrier drift, diffusion, generation, and recombination are discussed resulting in the formulation of the transport equations and the derivation of the current-voltage (I-V) characteristics of a p-n junction solar cell under illumination.

2.2 Operating principles of solar cells

Using the photovoltaic effect, a solar cell converts sunlight directly into electricity. A solar cell has three essential features: a light absorbing material, the presence of a built-in electric field, and a conductive contact layer. When photons are absorbed in a material, electrons are excited to higher energy state in the material. These excited electrons are then pulled away by the electric field within the photovoltaic device, before they can relax back to their ground state. The separated electrons are then fed to an external circuit via conductive contacts to do electrical work as shown in Fig. 2.1. Section 2.2 describes the photovoltaic cell characteristics and the performance parameters.

2.2.1 Photocurrent and quantum efficiency

The short-circuit photocurrent density (J_{sc}) is related to the incident light spectrum by the cell's quantum efficiency (QE), which is the probability that an incident photon of energy E will deliver one electron to the external circuit. Hence J_{sc} is given by:

$$J_{sc} = q\int b_s(E)QE(E)dE\,, \tag{2.1}$$

where b_s is the incident spectral photon flux density and q is the elementary charge.

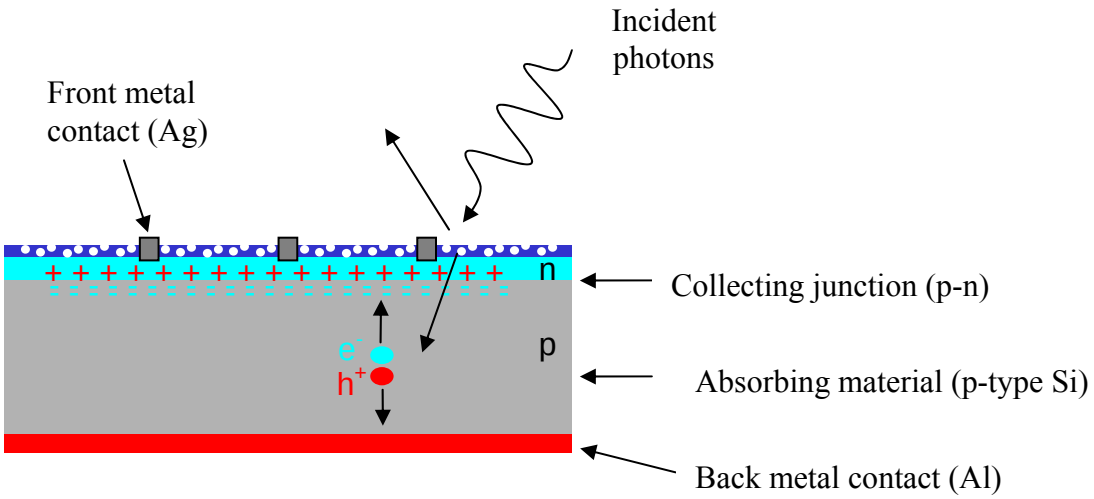


Figure 2.1 Typical silicon solar cell consisting of a p-type absorbing base, a p-n junction, and front and back metal contacts.

2.2.2 Dark current and open-circuit voltage

Dark current is the current due to forward bias induced by light generated charge carriers without any input electrical signal. This current acts in the opposite direction to the photocurrent and the net current is reduced from its short-circuit value. Most solar cells act like a diode and hence the dark current density $J_{dark}(V)$ varies as

$$J_{dark}(V) = J_0 \cdot \left[\exp\left(\frac{q \cdot V}{k_B T}\right) - 1\right], \tag{2.2}$$

where J_0 is a constant, k_B is Boltzmann's constant and T is the temperature.

From the superposition principle, current-voltage (I-V) characteristic can be approximated by the sum of J_{sc} and J_{dark} and can be written as

$$J(V) = J_{sc} - J_{dark}(V). \tag{2.3}$$

Hence for an ideal diode, using Eq. 2.2,

$$J = J_{sc} - J_0 \cdot \left[\exp\left(\frac{q \cdot V}{k_B T} \right) - 1 \right]. \tag{2.4}$$

In the open circuit condition, the short circuit current and the dark current cancel out, giving the maximum voltage, also called the open-circuit voltage (V_{oc}):

$$V_{oc} = \frac{k_B T}{q} \ln\left(\frac{J_{sc}}{J_o} + 1\right). \tag{2.5}$$

2.2.3 Efficiency

Figure 2.2 shows the I-V characteristics of a solar cell in dark and under illumination.

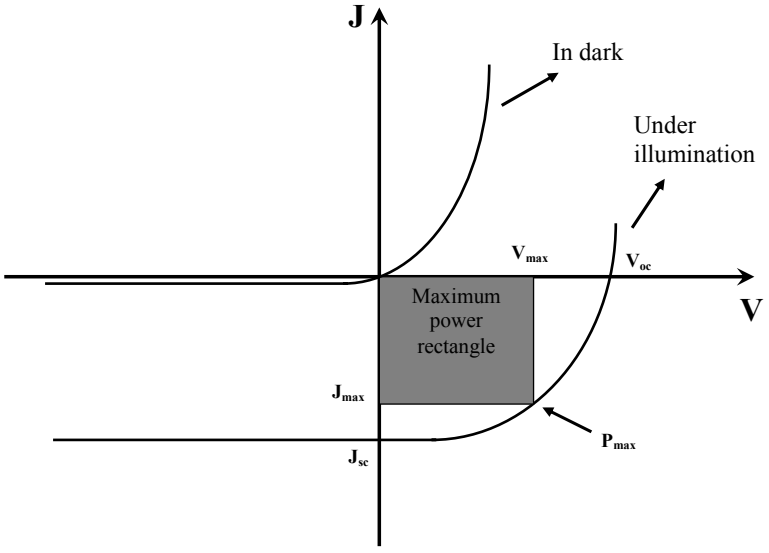


Figure 2.2 I-V curve of a solar cell in dark and under illumination.

The power density of the cell is given as

$$P = JV \,. \tag{2.6}$$

At maximum power point, with voltage V_{max} and a corresponding current density, J_{max}, power (P_{max}) density reaches its maximum. The fill factor (FF) of the cell is defined as

$$FF = \frac{J_{\max} V_{\max}}{J_{sc} V_{oc}}, \tag{2.7}$$

which denotes the squareness of the IV curve. The efficiency (η) of the solar cell is defined as

$$\eta = \frac{J_{\max} V_{\max}}{P_{in}}, \tag{2.8}$$

where P_{in} is the incident power density. Using Eq. 2.7, efficiency is defined as

$$\eta = \frac{J_{sc} V_{oc} FF}{P_{in}} \,. \tag{2.9}$$

η, J_{sc}, V_{oc} and FF are the main performance parameters of a solar cell and are reported under the standard testing condition of Air Mass 1.5 spectrum, incident power density of 1000 W m^{-2}, and at a temperature of 25 °C. Hence, the conversion efficiency of a solar cell is directly related to the J_{sc}, V_{oc}, and FF.

2.2.4 Parasitic resistances and junction recombination in a solar cell

In a real solar cell, the bulk resistance of the cell material, bulk resistance of the metallic contacts and the interconnections, and contact resistance between metallic contacts and the cell material give rise to series resistance (R_s). A shunt resistance (R_{sh}) arises in a solar cell due to the leakage across the collecting junction around the edges of

the device due to imperfections in the junction region and between contacts of different polarity. In a non-ideal diode, there could be recombination in the space-charge region due to the presence of defects or traps. This phenomenon is represented by a shunt diode in parallel with the solar cell and is characterized by a diode ideality factor n and junction leakage current J_{02}. Figure 2.3 draws the electrical equivalent of a real solar cell, due to the presence of these parasitic series and shunt resistances, and junction recombination.

To account for the parasitic series and shunt resistances and junction recombination, the ideal diode Eq. 2.4 is modified as Eq. 2.10 to obtain the I-V characteristics of a non-ideal solar cell:

$$I = I_{sc} - I_{01} \cdot \left[\exp\left(\frac{q \cdot (V + IR_s)}{k_B T} \right) - 1 \right] - I_{02} \cdot \left[\exp\left(\frac{q \cdot (V + IR_s)}{n_2 k_B T} \right) - 1 \right] - \left(\frac{V + IR_s}{R_{sh}} \right). \qquad (2.10)$$

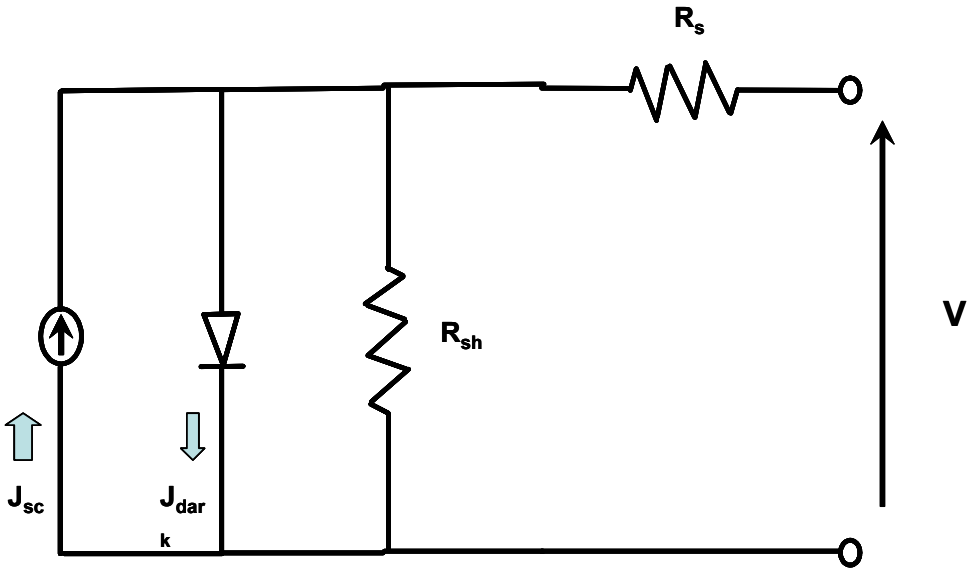


Figure 2.3 Electrical equivalent of a real solar cell with parasitic series and shunt resistances.

It is clear from Fig. 2.3 that the presence of shunt diode and shunt resistance (R_{sh}) reduces the terminal current, and the presence of series resistance (R_s) reduces the terminal voltage by IR_s, resulting in a decrease in power output or cell efficiency.

2.3 Device physics of p-n junction solar cells

A visible photon can provide enough energy to excite charge carriers from the conduction band to the valence band of a semiconductor. This makes semiconductor material suitable for photovoltaics. The p-n junction forms the basis of charge separation in a photovoltaic device. Section 2.3 will first review the various transport phenomenons in semiconductor devices which are applicable to solar cells and then review the I-V characteristics of a p-n homojunction.

2.3.1 Carrier drift and diffusion

For a semiconductor in equilibrium, the electron and hole densities follow the law of mass action of carriers [5]:

$$np = n_i^2 , \tag{2.11}$$

where n is the density of electrons per unit volume, p is the density of holes per unit volume and, n_i is the intrinsic carrier density.

No net current flows in a semiconductor in equilibrium, however for a semiconductor under bias (by exposure to light of energy greater than semiconductor band gap energy or by electrical injection of electron and holes through electric bias) the n and p are above their equilibrium value and, assuming that Boltzmann statistics applies, can be obtained from:

$$n = N_c e^{-(E_c - E_{F_n})/k_B T} , \text{ and} \tag{2.12}$$

$$p = N_v e^{-(E_{F_p} - E_v)/k_B T} , \tag{2.13}$$

where N_c is the effective conduction band density of states, N_v is the effective valence band density of states, E_c is the energy of the conduction band edge, E_v is the energy of

the valence band edge, and E_{fn} and E_{fp} are the electron and hole quasi-Fermi levels, respectively.

The electron and hole densities now follow:

$$np = n_i^2 e^{\Delta\mu / k_B T}, \tag{2.14}$$

where $\Delta\mu$ is the difference in the chemical potential originating as a result of carrier excitation and measures the difference in the quasi Fermi levels,

$$\Delta\mu = E_{F_n} - E_{F_p}. \tag{2.15}$$

The electron and hole current densities under the applied bias are given by the gradient in the quasi Fermi level, under the relaxation time approximation and can be written as

$$J_n(\bar{r}) = \mu_n n \nabla_{\bar{r}} E_{F_n}; \tag{2.16}$$

$$J_p(\bar{r}) = \mu_p p \nabla_{\bar{r}} E_{F_p}, \tag{2.17}$$

The net current density would be given by the sum of electron and hole current densities,

$$J(\bar{r}) = J_n(\bar{r}) + J_p(\bar{r}). \tag{2.18}$$

which, within the Boltzmann approximation ($(E_c-E_{fn}) >> k_BT$ and $(E_{fp}-E_v) >> k_BT$), can be written as

$$J_n(\bar{r}) = qD_n \nabla n + q\mu_n Fn; \tag{2.19}$$

$$J_p(\bar{r}) = -qD_p \nabla p + q\mu_p Fp, \tag{2.20}$$

where F is the applied field, D_n and D_p are the diffusion coefficient of electron and holes respectively and μ_n, μ_p are electron and hole mobility respectively which are related by the Einstein relations as follows

$$\mu_n = \frac{qD_n}{k_B T} \text{ and} \tag{2.21}$$

$$\mu_p = \frac{qD_p}{k_B T}. \tag{2.22}$$

Eq. 2.19 and 2.20 can be split into drift and diffusion currents. In the drift current, carriers are driven by the applied field and net drift current can be written as

$$J_{drift} = q(\mu_n n + \mu_p p)F = \sigma F, \tag{2.23}$$

where σ is the semiconductor conductivity.

In the diffusion current, carriers are driven by the difference in their concentration gradients to reduce their electrostatic potential energy and net diffusion current can be written as

$$J_{diffusion} = q(D_n \nabla n - D_p \nabla p). \tag{2.24}$$

As in the case of excitation by illumination, the electron and hole gradients may be similar, and the net diffusion current is zero. Diffusion currents would arise in the case of p-n junction device configurations; where, carrier concentration gradients would be different, and current would be dominated by the minority carrier diffusion.

Notice that the drift and the diffusion processes are related through the Einstein's relations (Eqs. 2.21 and 2.22)

2.3.2 Carrier generation and recombination

Effect of bulk and surface recombination on solar cell performance is studied in this thesis. Therefore, this section will briefly review the basics of bulk and surface recombination mechanisms in a semiconductor.

Electrons and holes can be recombined or be generated in a semiconductor thereby changing the local carrier concentrations. The entire semiconductor must however remain space-charge neutral. This requirement leads to the injection or

extraction of charge at the contacts. The input energy required for generation of carriers in a semiconductor can be thermal (phonons or the vibrational energy of the lattice), radiative (photons) or Auger (kinetic energy of another carrier). The energy released upon recombination is also taken by the same processes. The transitions can be from either the band-to-band states or from band-to-bound (trap) states.

For direct-gap semiconductors, such as GaAs, InP, ZnS, etc., the minima of the conduction band and the valence band maxima occur at the same point in k space (k being the crystalline momentum). A radiative transition in this case proceeds as first order and is described by the Fermi's golden rule, which is the quantum mechanical transition probability per unit time from an initial filled state $|s\rangle$ to the final state $|k\rangle$ and is given by

$$W = \frac{2\pi}{\hbar}\left|\langle k|V|S\rangle\right|^2 \delta(E_k - E_s)\,. \tag{2.25}$$

where $\hbar$ is the plank's constant, and V is the perturbing potential inducing the transition.

For indirect band gap semiconductors, such as Si, Ge, etc., conduction band minima and the valence band maxima occur at different points in k space. An indirect radiative transition in this case is forbidden to first order; but can occur to second order, mediated by a phonon, which provides the necessary momentum for the transition to take place. The second order transition probability is given by

$$W = \frac{2\pi}{\hbar}\left|\sum_m \frac{\langle k|V|m\rangle\langle m|V'|S\rangle}{(E_s - E_m)}\right|^2 \delta(E_k - E_s)\,. \tag{2.26}$$

This transition from the initial state $|s\rangle$ to the final state $|k\rangle$ occurs through an intermediate state $|m\rangle$, which is mediated by a phonon event.

Equations 2.25 and 2.26 would yield the rate of transition from the initial to the final state when multiplied by the probabilities of the initial state being occupied ($f(E_s(k_s))$ and the final state being available ($1- f(E_k(k_k))$, where f(E) is the electronic occupation function.

Photogeneration, which is the generation of mobile electrons and holes as a result of light absorption, is the most important generation mechanism for solar cells. Recombination, which is the reverse of generation, refers to the loss of mobile carriers. Generation and recombination in semiconductors is discussed below.

2.3.2.1 Generation

If α is the semiconductor's wavelength dependent absorption coefficient, then the attenuation of light intensity can be expressed as

$$I(x) = I(0)e^{-\int_0^x \alpha(E,x')dx'} . \quad (2.27)$$

for radiation of energy E and I(0) is the intensity just inside the front surface. Equation 2.27 reduces to the Beer-Lambert law for uniform α,

$$I(x) = I(0)e^{-\alpha x} . \quad (2.28)$$

The generation rate, per unit volume, at depth x below the surface, can be calculated from the incident flux $b_s(E)$, reflectivity of the front surface R(E), for light of energy E, incident normally and can be expressed as

$$g(E,x) = (1-R(E))\alpha(E)b_s(E)e^{-\int_0^x \alpha(E,x')dx'} , \quad (2.29)$$

which accounts for the front surface reflection and the attenuation given by Eq. 2.28.
The total generation rate, at distance x from the front surface and inside the bulk, is thus given by integrating Eq. 2.29 over energies where photon absorption results in free carrier generation and can be expressed as

$$G(x) = \int g(E,x)dE \,. \tag{2.30}$$

Direct band gap semiconductors are more efficient light absorbers and need only a few microns of material to absorb most of the light as compared to several microns for the indirect band gap semiconductors such as Si.

2.3.2.2 Bulk recombination

Recombination is the inverse process of generation, where the e-h pairs are lost. Recombination mechanisms can be classified as intrinsic and extrinsic mechanisms. *Intrinsic (band-to-band) recombination* is always present in the semiconductor, is unavoidable, and occurs via direct band-to-band transition of an electron. Depending on the way the e-h pairs combine, intrinsic mechanisms can be divided into two categories, radiative band-to-band recombination and Auger band-to-band recombination. *Extrinsic (band-to-bound, trap-assisted) recombination* occurs via a defect, which gives rise to traps or energy levels inside the band gap of a semiconductor. This recombination type is commonly known as the Shockley-Read-Hall (SRH) recombination. These three mechanisms are depicted in Fig. 2.4.

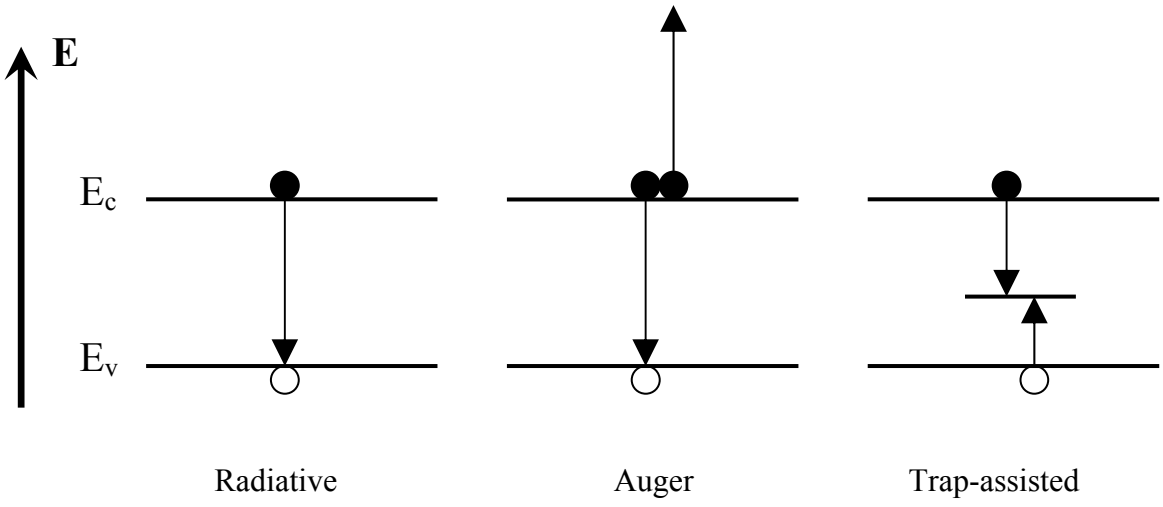


Figure 2.4 The three carrier recombination mechanisms in semiconductors.

Radiative recombination involves the recombination of an e-h pair, resulting in an emission of a photon with energy approximately equal to the band gap. The net radiative recombination rate is given by:

$$U_{rad} = B_{rad}(np - n_i^2)\,. \tag{2.31}$$

Here B_{rad} is the radiative recombination coefficient and is given as:

$$B_{rad} = \frac{1}{n_i^2}\frac{2\pi}{h^3c^2}\int_0^\infty n_s^2\alpha(E)e^{-E/k_BT}E^2dE\,, \tag{2.32}$$

where n_s is the refractive index of the semiconductor. B_{rad} represents the quantum-mechanical probability of a radiative transition and depends directly on α (E), as a result it is more dominating in direct band gap semiconductors than in indirect band gap semiconductors. If n_0 and p_0 the are equilibrium electron and hole densities, respectively, and Δn and Δp be the excess carrier densities for electron and holes. Then, for non-equilibrium concentrations of $n = n_0 + \Delta n$ and $p = p_0 + \Delta p$ and assuming charge neutrality ($\Delta p = \Delta n$), Eq. 2.31 can be written as:

$$U_{rad} = B_{rad}(n_0 + p_0) + B_{rad}\Delta n^2\,; \tag{2.33}$$

consequently, the radiative recombination lifetime (τ_{rad}) can be written as

$$\tau_{rad} = \frac{1}{B_{rad}(n_0 + p_0 + \Delta n)}\,. \tag{2.34}$$

Auger recombination is a three particle process in which the energy released by the recombination of an e-h pair is transferred to a third free carrier, which subsequently releases its excess energy as phonons. The third free carrier can be either a conduction band electron or a valence band hole, so the Auger recombination rate (U_{Aug}) would

either be proportional to n^2p (eeh-process) or to np^2 (ehh-process). Hence U_{Aug} would be given by:

$$U_{Aug} = C_n(n^2p - n_0^2p) + C_p(np^2 - n_0p_0^2), \tag{2.35}$$

where C_n and C_p are the Auger coefficients for the eeh and ehh processes. Similar to Eq. 2.34, Auger lifetime can be expressed under low level injection (LLI) and high level injection (HLI) conditions as:

LLI conditions:

$$\tau_{Aug,lli} = \frac{1}{C_n N_D^2} \quad \text{for n-type,} \quad \text{and} \quad \tau_{Aug,lli} = \frac{1}{C_p N_A^2} \text{ for p-type.} \tag{2.36}$$

For HLI conditions:

$$\tau_{Aug,hli} = \frac{1}{(C_n + C_p)\Delta n^2} \quad \text{for n-type and p-type.} \tag{2.37}$$

The most commonly quoted values for the Auger coefficients are those determined by Dziewior and Schmidt on n-type and p-type Si with a doping concentration greater than $5x10^{18}$ cm^{-3} (C_n=$2.8x10^{-31}$ cm^6s^{-1} and C_p=$0.99x10^{-31}$ cm^6s^{-1}) [6].

Trap-assisted or the Shockley-Read-Hall (SRH) recombination is the most important form of recombination in defective semiconductors. These defects could be due to the presence of impurities, crystallographic imperfections, etc. and would produce a defect level or trap level within the band gap. In 1952, Shockley and Read [7] and Hall [8] formulated the theory of recombination through defects from purely statistical considerations and determined the recombination rate from a single defect level as a function of defect, material and excitation parameters. The net recombination rate for SRH recombination (U_{SRH}) through defects can be written as:

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)}. \tag{2.38}$$

where τ_{n0} and τ_{p0} are the capture time constants of electrons and holes, which are related to the thermal velocity υ_{th}, the defect concentration, N_t, and the capture cross-sections of electron and hole σ_n and σ_p of the specific defect as

$$\tau_{p0} \equiv \frac{1}{\sigma_p \upsilon_{th} N_t} \text{ and } \qquad \tau_{n0} \equiv \frac{1}{\sigma_n \upsilon_{th} N_t}. \tag{2.39}$$

n_1 and p_1 are defined as:

$$n_1 \equiv N_C \exp\left(-\frac{E_C - E_t}{kT}\right) \qquad \text{and} \quad p_1 \equiv N_V \exp\left(-\frac{E_t - E_V}{kT}\right). \tag{2.40}$$

n_1 and p_1 are the equilibrium densities of electrons and holes when the Fermi level E_f coincides with the defect energy E_t and they also satisfy the law of mass action of carriers Eq. 2.11 ($np = n_i^2$).

Assuming negligible carrier trapping ($\Delta n = \Delta p$), SRH lifetime can now be written as:

$$\tau_{SRH} = \frac{\tau_{n0}(p_0 + p_1 + \Delta n) + \tau_{p0}(n_0 + n_1 + \Delta n)}{n_0 + p_0 + \Delta n}. \tag{2.41}$$

SRH recombination is the strongest when n and p are of similar magnitude. Equation 2.38 shows that for a midgap (deep) trap with equal capture times, U_{SRH} has a maximum when n and p are equal. Hence in undoped regions, where n and p may be similar, SRH recombination is more important than the radiative recombination, which depends on the np product (Eq. 2.31).

The assumption of the single defect level used in deriving these equations would be valid for point defects; however, it may be invalid for precipitates and surface defect

energies, which tend to be distributed continuously in certain regions of the band gap. The surfaces of silicon substrate represent an abrupt discontinuity in the crystal structure. The interfaces between different crystal regions in a multicrystalline material (grain boundaries) also have a similar nature of defects. These defect states at surfaces and interfaces include crystal defects due to partially broken bonds and extrinsic impurities. These trap states are concentrated in two dimensions; hence the recombination is expressed in terms of trap density per unit area rather than per unit volume.

2.3.2.3 Surface recombination

The *surface and grain boundaries recombination* is expressed with the extended SRH formalism and the overall surface recombination rate U_s is given as:

$$U_s = (n_s p_s - n_i^2) \int_{E_V}^{E_C} \frac{\nu_{th} D_{it}(E_t)}{\frac{n_s + n_1(E_t)}{\sigma_p(E_t)} + \frac{p_s + p_1(E_t)}{\sigma_n(E_t)}} dE_t , \tag{2.42}$$

where $D_{it}(E_t)$ is the interface trap density, and n_s and p_s are the electron and hole density at the surface. To measure directly the recombination activity of the surface, we define the surface recombination velocity (SRV) as:

$$S \equiv \frac{U_s}{\Delta n} , \tag{2.43}$$

which can be expressed in the special case of flat band as:

$$S = \int_{E_V}^{E_C} \frac{(n_0 + p_0 + \Delta n_s)\nu_{th} D_{it}}{\frac{(n_0 + n_1 + \Delta n_s)}{\sigma_p} + \frac{(p_0 + p_1 + \Delta n_s)}{\sigma_n}} dE , \tag{2.44}$$

where Δn_s is the excess carrier density at the surface. A review of grain boundary structure and electronic properties in semiconductors is given by Groveno [9].

The overall recombination rate is the sum of the three bulk recombination mechanisms and the surface recombination component, and we can define the effective lifetime (τ_{eff}) as:

$$\frac{1}{\tau_{eff}} = (\frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}}) + \frac{1}{\tau_{surface}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}}. \quad (2.45)$$

To maintain a high value of τ_{eff}, the bulk and surface recombinations should be minimized to achieve high-efficiency solar cells. The effect of τ_{eff} on the solar cell performance has been studied in detail in this thesis.

2.3.3 Transport equations

With the formulation described in the previous two sections for carrier drift, diffusion, generation, and recombination, the semiconductor transport equations can be setup for each charge carrier. There are two governing principles: 1) The number of carriers of each type must be conserved, and 2) the electrostatic potential due to the charge carriers obey Poisson's equation. Hence the transport equations can be written as:

$$\frac{dn}{dt} = \frac{1}{q}\nabla.\overline{J_n} + G_n - U_n, \quad (2.46)$$

for electrons and,

$$\frac{dp}{dt} = -\frac{1}{q}\nabla.\overline{J_p} + G_p - U_p, \quad (2.47)$$

for holes, where $G_{n(p)}$ and $U_{n(p)}$ are the volume rates of generation of electrons (holes). Poisson's equation can be written as:

$$\nabla^2\phi = \frac{q}{\varepsilon_s}(N_a - N_d + n - p), \quad (2.48)$$

where ϕ is the electrostatic potential, ε_s is the dielectric permittivity of the semiconductor, and N_a and N_d are the densities of ionized acceptors and donors.

Generation rate is given by Eqs. 2.29 and 2.30. Recombination rate is given by the sum of bulk recombination Eqs. 2.31, 2.35, 2.38 and Eq. 2.42 for the surface recombination. For crystalline material, $\overline{J_n}$ and $\overline{J_p}$ are given by Eqs. 2.16 and 2.17. n, p, and ϕ are solved from the set of three coupled differential Eqs. 2.46, 2.47, and 2.48 as a function of depth and time, with given boundary conditions. Solar cells operate in steady state; therefore transport equations are solved under the condition $\frac{dn}{dt} = \frac{dp}{dt} = 0$.

2.3.4 The p-n junction solar cell operation

The previous two sub-sections briefly discussed charge generation, recombination, and transport. To get the photovoltaic energy conversion, this charge has to be separated by means of a driving force. This driving force is provided by the p-n junction, as a result of which the electrons are collected at the n contact and the holes at the p contact. In this subsection the analytic solution for the J (V) characteristic is reviewed under different conditions. With the formation of a p-n junction, a space charge region is formed as a result of diffusion of majority carriers across the metallurgical junction. The width of the p-n junction is fixed when the diffusion of carriers is counter balanced by the drift of carriers in the opposite direction, in the space charge region with built in electric field. The space charge region, which is depleted of both electrons and holes, presents a barrier to the majority carriers and a low resistance path for the minority carriers. The photogenerated minority carriers in the n and p region of the solar cell reach the junction region via diffusion.

Figure 2.5 shows an n^+-p junction, the type of structure used throughout the thesis. Base material is doped p-type, and emitter is heavily doped n-type, forming an n^+-p homojunction.

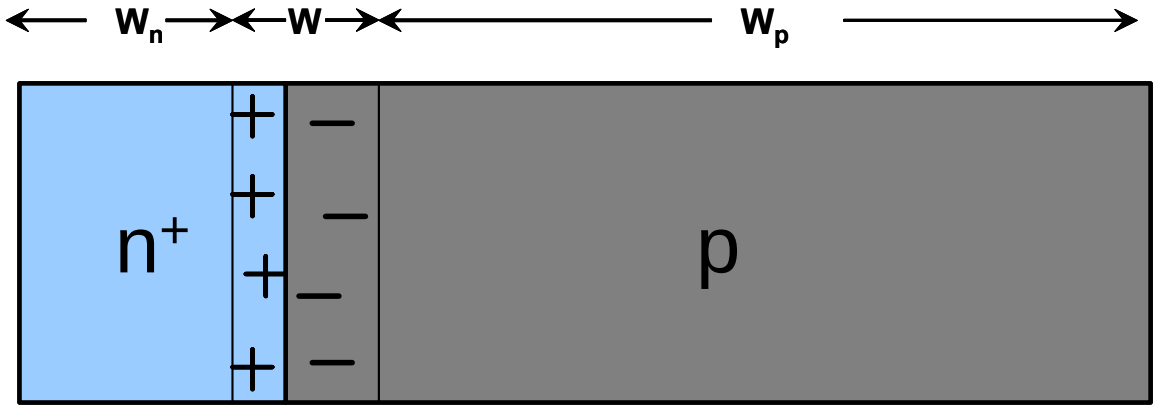


Figure 2.5 The n+-p homojunction.

Width of the base and emitter is W_p and W_n, respectively. W is the width of the depletion region. The structure can be divided into three parts: the neutral n- and p-type regions, (quasi-neutral regions or QNR), and the charged region (space charge region or SCR) around the junction with strong electric field. To understand the operation of a solar cell, we want to determine the current that passes through this device in steady state under illumination and for a given potential difference between the terminals. To get analytic solutions for the J (V) characteristics, two approximations are necessary:

- The depletion approximation: The charged region around the junction contains no free carriers, and outside this region the net charge density is zero. This is an idealization of the actual charge distribution in the depletion region so that the electric field is confined to the depletion region.
- The superposition approximation: Recombination rates in the QNR regions are linear in minority carrier density. This helps to decouple the effect of bias from

the effect of illumination, so that the solutions under bias and illumination can be added to give the solution under light and applied bias.

The difference in the work function of the n- and p-type materials in a p-n junction is taken up by a step in the conduction and valence band edges resulting in the built-in potential (V_{bi}), given by:

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right). \tag{2.49}$$

where N_a and N_d is the density of the acceptor and donor impurity atoms respectively. The width of the SCR is given as:

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)V_{bi}}. \tag{2.50}$$

The carrier and current densities in the QNR can be solved under the depletion approximation, as a result of which the Poisson's Eq. 2.48 becomes zero, and the drift terms in Eqs. 2.19 and 2.20 become zero, and thus there is only a diffusion component. In one dimension, Eq. 2.19 can be written as:

$$J_n = qD_n \frac{dn(x)}{dx}. \tag{2.51}$$

Under steady state ($\frac{dn}{dt} = 0$), the continuity equation for electrons becomes:

$$\frac{1}{q}\frac{\partial J_n}{\partial x} = (U - G). \tag{2.52}$$

From Eqs. 2.51 and 2.52, under steady state in QNR, in the depletion approximation, electrons follow the equation:

$$\frac{d^2 n(x)}{dx^2} = \frac{U(x) - G(x)}{D_n}. \tag{2.53}$$

Similarly, for holes we get:

$$J_p = -qD_p \frac{dp(x)}{dx}, \tag{2.54}$$

and

$$\frac{d^2 p(x)}{dx^2} = \frac{U(x) - G(x)}{D_p}. \tag{2.55}$$

Eqs. 2.53 and 2.55 are second order differential equations, which require expressions for U and G to determine the general solution, and the boundary conditions to find the particular solution.

It is useful to define the diffusion length, which is a measure of the average distance a minority carrier will diffuse before recombining. Diffusion length of electrons and holes can be defined as:

$$L_n = \sqrt{\tau_n D_n}, \tag{2.56}$$

for electrons and,

$$L_p = \sqrt{\tau_p D_p}, \tag{2.57}$$

for holes. The excess carrier density decays according to:

$$\Delta n(x) = \Delta n(0) e^{-x/L_n}, \tag{2.58}$$

for electrons and

$$\Delta p(x) = \Delta p(0) e^{-x/L_p}, \tag{2.59}$$

for holes, with $\Delta p(x) = p_n(x) - p_{no}$ and $\Delta n(x) = n_p(x) - n_{po}$,

where n_{p0} is the electron concentration in p-type material at equilibrium (minority concentration), p_{n0} is the hole concentration in n-type material (minority concentration) at

equilibrium, p_n is the total hole concentration in n-type material, and n_p is the total electron concentration in p-type material. A higher value of lifetime and hence the diffusion lengths are desired to obtain a higher conversion efficiency of the solar cells.

p-n junction in dark

In the case of no illumination and no applied bias, there will be no minority carrier diffusion currents in the QNR and no net recombination in the SCR; as a result the current density is zero. If however a bias is applied to the junction in dark, built in potential reduces (forward bias) and more majority carriers diffuse across the junction, resulting in a net electron current from n to p side and hole current from p to n side. The quasi Fermi levels are split in the SCR and there is a net recombination, which adds to the current. From Fig. 2.5, for the condition $W_p >> L_n$ and $W_n >> L_p$ and under forward bias (V), Eqs. 2.54 and 2.59 give the hole current at the edge of depletion region in the n-side as:

$$J_p = \frac{qD_p}{L_p}\Delta p_n(0) = \frac{qD_p}{L_p} p_{n0}(e^{qV/k_BT} - 1). \tag{2.60}$$

Similarly from Eqs. 2.51 and 2.58, the electron minority carrier current on the p-side can be written as:

$$J_n = \frac{qD_n}{L_n}\Delta n_p(0) = \frac{qD_n}{L_n} n_{p0}(e^{qV/k_BT} - 1). \tag{2.61}$$

Total diffusion current can be written by adding Eqs. 2.60 and 2.61:

$$J_{diff}(V) = q(\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0})(e^{qV/k_BT} - 1). \tag{2.62}$$

Recombination current from SCR, assuming SRH as the dominating recombination process can be written as [10]:

$$J_{scr}(V) = J_{scr,0}(e^{qV/2k_BT} - 1), \tag{2.63}$$

where

$$J_{scr,0} = \frac{qn_iW}{\sqrt{\tau_n\tau_p}}. \tag{2.64}$$

The radiative recombination current, which has the same bias dependence as the diffusion current (Eq. 2.31), would be given as [10]:

$$J_{rad}(V) = J_{rad,0}(e^{qV/k_BT} - 1). \tag{2.65}$$

and can be significant in direct band gap materials. Total dark current can be written from Eqs. 2.62, 2.63, and 2.65 as:

$$J_{dark}(V) = q(\frac{D_p}{L_p}p_{n0} + \frac{D_n}{L_n}n_{p0})(e^{qV/k_BT} - 1) + J_{scr,0}(e^{qV/2k_BT} - 1) + J_{rad,0}(e^{qV/k_BT} - 1). \tag{2.66}$$

For indirect band gap materials such as Si, J_{rad} would be small and the recombination in the depletion region is also very small because $W<<L_{n/p}$. Eq. 2.66 can then be approximated as:

$$J_{dark}(V) \approx q(\frac{D_p}{L_p}p_{n0} + \frac{D_n}{L_n}n_{p0})(e^{qV/k_BT} - 1). \tag{2.67}$$

Comparing with the Shockley or ideal diode equation, the reverse saturation current (J_0) can be written as:

$$J_0 = q(\frac{D_p}{L_p}p_{n0} + \frac{D_n}{L_n}n_{p0}). \tag{2.68}$$

When depletion region recombination is also dominant, non-ideal diode Eq. 2.10 would result. For direct band gap materials and in situations where depletion region

recombination is also dominant, dark current would take the more general form of Eq. 2.66.

Effect of surface recombination on the reverse saturation current

If the dimension of the solar cell and the effects of surfaces are taken into consideration, then continuity Eq. 2.55 for holes in the n region under steady state with no illumination, but with a forward bias V, can be written as:

$$\frac{d^2\Delta p}{dx^2} = \frac{U(x)}{D_p} = \frac{\Delta p}{D_p \tau_p} = \frac{\Delta p}{L_p^2}. \tag{2.69}$$

Solving Eqn. 2.69 with the surface boundary condition:

$$S_p \Delta p = D_p \frac{d\Delta p}{dx}. \tag{2.70}$$

and hole concentration at the depletion edge (law of junction),

$$p_n = p_{n0} e^{qV/k_B T}, \tag{2.71}$$

and then substituting in Eq 2.54, we can calculate the hole current in the n^+ region, at the edge of the depletion region as:

$$J_p = -\frac{qD_p}{L_p}\frac{n_i^2}{N_D}\left[\frac{\frac{S_p L_p}{D_p} + \tanh(\frac{W_n}{L_p})}{1 + \frac{S_p L_p}{D_p}\tanh(\frac{W_n}{L_p})}\right]\left(e^{qV/k_B T} - 1\right). \tag{2.72}$$

Similarly the electron current in p-region can be written as:

$$J_n = -\frac{qD_n}{L_n}\frac{n_i^2}{N_A}\left[\frac{\frac{S_n L_n}{D_n} + \tanh(\frac{W_p}{L_n})}{1 + \frac{S_n L_n}{D_n}\tanh(\frac{W_p}{L_n})}\right]\left(e^{qV/k_B T} - 1\right), \tag{2.73}$$

where S_p and S_n are the hole and electron surface recombination velocities. Total current can now be written as:

$$J_T = J_p + J_n = (J_{0n} + J_{0p})\left(e^{qV/k_BT} - 1 \right). \tag{2.74}$$

Hence J_0 can be expressed as a sum of the saturation current component from the base (J_{0b}) and from the emitter (J_{0e}):

$$J_0 = J_{0e} + J_{0b} = \frac{qD_p}{L_p}\frac{n_i^2}{N_D}F_N + \frac{qD_n}{L_n}\frac{n_i^2}{N_A}F_P, \tag{2.75}$$

where

$$F_N = \left[\frac{\frac{S_pL_p}{D_p} + \tanh(\frac{W_n}{L_p})}{1 + \frac{S_pL_p}{D_p}\tanh(\frac{W_n}{L_p})} \right] \quad \text{and} \quad F_P = \left[\frac{\frac{S_nL_n}{D_n} + \tanh(\frac{W_p}{L_n})}{1 + \frac{S_nL_n}{D_n}\tanh(\frac{W_p}{L_n})} \right]. \tag{2.76}$$

The saturation current density (J_0), or the values of the base (J_{ob}) and the emitter (J_{oe}) contributions to J_0, should be minimized to improve the performance (V_{oc}) of the solar cells as seen from Eq. 2.5 for V_{oc} of the solar cell.

<u>p-n junction under illumination</u>

To solve for the carrier concentration and current characteristic under illumination, we can write Eq. 2.55 for minority carrier holes in the n-side as:

$$\frac{d^2\Delta p}{dx^2} = \frac{\Delta p}{D_p\tau_p} - \frac{G}{D_p}. \tag{2.77}$$

with the assumption of a uniform generation rate G and linear recombination in the n layer. Solving for the carrier concentration with the boundary conditions:

$$\Delta p = G\tau_p, \tag{2.78}$$

i.e. finite minority carrier concentration, far from the junction and the junction law (Eq. 2.71), and substituting in Eq. 2.54, the hole current in the n^+ region, at the edge of the depletion region can be written as:

$$J_p(x) = \frac{qD_p p_{n0}}{L_p}\left(e^{qV/kT} - 1\right) - qGL_p \,. \tag{2.79}$$

Similarly, the current for minority carrier electrons in the p-side can be written as:

$$J_n(x) = \frac{qD_n n_{p0}}{L_n}\left(e^{qV/kT} - 1\right) - qGL_n \,. \tag{2.80}$$

Assuming uniform generation and no recombination in the depletion region, the light generated current in the depletion region can be written as:

$$J_{dep} = qGW \,. \tag{2.81}$$

Total current is the sum of the current from the three regions and can be written from Eqs. 2.79, 2.80, and 2.81 as:

$$J_{Total} = \left[\frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p}\right]\left(e^{qV/kT} - 1\right) - qG(L_n + L_n + W) = J_{dark} - J_{light} \,. \tag{2.82}$$

Here (L_n+L_p+W) represents the distance or volume over which the photo-generated carriers can be collected. Notice that Eq. 2.82 has been written as the *superposition* of the dark and the light generated currents, i.e., solutions for the bias and light induced currents are independent and is valid under the depletion approximation when minority carrier recombination is linear.

Eq. 2.82 can also be written as:

$$J = J_0\left(e^{qV/kT} - 1\right) - J_{sc} \,, \tag{2.83}$$

where J_0 is given by Eq. 2.68.

Hence the diode or dark characteristic is shifted down by J_{sc} into the quadrant where current is negative, voltage is positive, and power (I.V) is negative; hence, diode is generating power instead of absorbing. This is the basic principle of solar energy conversion.

2.4 Conclusions

For a given spectrum of incident light, the conversion efficiency of the solar cell is described in terms of three parameters: the short–circuit current density, open-circuit voltage, and the fill factor of the solar cells. All three parameters are directly related to the conversion efficiency and should be maximized to achieve higher efficiency. The parasitic resistances should be minimized to achieve higher efficiency. A higher effective lifetime (or the diffusion length) of the carriers and a lower value of the saturation current density maximizes these three parameters and would yield a higher efficiency. The semiconductor transport equations were used to formulate the I-V characteristics that describe the operation of p-n junction solar cells.

CHAPTER 3

CRYSTALLINE SILICON SOLAR CELL: MATERIALS, LIFETIME ENHANCEMENT, AND DESIGN

3.1 Introduction

Crystalline Si is the most commonly used substrate for solar cell fabrication, capturing 90% of the worldwide PV market. This chapter first discusses the various techniques used to grow single and multicrystalline Si (section 3.2). The low-cost Si materials used to fabricate c-Si solar cells come with many defects and impurities, which reduce the performance. Section 3.3 discusses the techniques of gettering and hydrogen passivation that can improve the bulk quality of low-cost substrates and also reviews the common surface passivation layers applied to Si surfaces in order to reduce surface recombination. Section 3.4 discusses the conventional n^+-p-p^+ solar cell and some advanced solar cell designs from literature.

3.2 Crystalline silicon growth techniques

Work performed in this research uses various crystalline silicon (c-Si) substrates for the base material. Within c-Si family for solar cells, the low-cost cast and ribbon mc-Si growth technologies accounted for approximately 44% of the cell and module shipments in 2006 and single crystal Si accounted for about 25% (Fig. 1.4). With the current Si feedstock shortage and high prices, market share of thinner and low-cost materials is expected to increase. The various promising technologies used to produce Si wafers for solar cells are shown in Fig. 3.1. This section first reviews the high-quality

single crystal growth techniques and then the low-cost multicrystalline Si (mc-Si) grown as ingots and sheets.

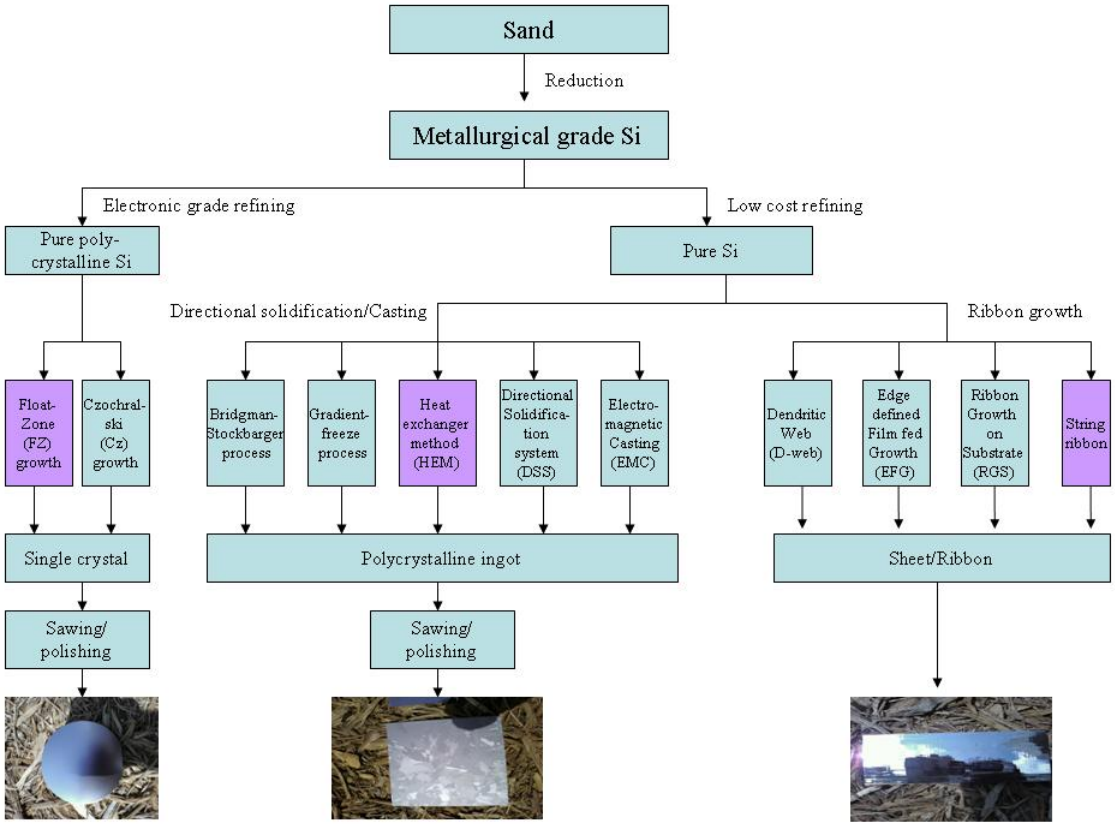


Figure 3.1 Flowchart depicting various common c-Si growth techniques.

3.2.1 Single crystal silicon

Single crystal Si (sc-Si) is grown mainly by the Float-zone (FZ) or the Czochralski (Cz) technique. The metallurgical grade Si obtained after carbothermic reduction of sand is refined further with the electronic grade process to yield high purity poly-crystalline rods. In the FZ technique, the crystal is heated locally by rf heater and floating molten zone traverses thought the hanging feed crystal and is also in contact with a seed crystal, resulting in the growth of single crystal. The molten silicon is not in contact with any crucible, resulting in high purity sc-Si. In Cz technique, crystals are

grown from melt in a crucible where a seed crystal is brought in contact with the melt and is pulled out slowly. Single crystal Cz grows at the seed. Si melt in Cz technique is in contact with the crucible, therefore, unlike FZ, there is unavoidable contamination in this material. Cz mainly suffers from high concentrations of oxygen, in the range of 10^{17} to 10^{18} cm^{-3}, which is detrimental to the performance of solar cells made on Cz wafers. It can also contain some carbon and very small amounts of metallic contaminants; therefore, bulk lifetime in Cz is often lower than FZ.

The single crystal rods thus obtained have to be sliced with diamond or wire saw to obtain single crystal wafers. The wafers are finally polished, mechanically and chemically, to remove surface damage from sawing. FZ Si with high bulk lifetime has been used extensively in this research as a reference/process control material.

3.2.2 Muti-crystalline silicon (Ingot)

Molten Si is solidified in the form of ingots by directional solidification. In the casting technique, Si melt is poured in a crucible for solidification. In other techniques, the melting and solidification are both done in the same crucible. In either case, the basic principle is directional solidification. The container materials are usually made of high-density graphite, SiO_2, Si_3N_4, SiC, etc., with the inside of the crucible coated with powdered Si, graphite, SiO_2, or Si_3N_4, to reduce adhesion to the crucible walls. The various solidification techniques differ in the manner in which heat is extracted from the melt. The five different ways of solidification are shown in Fig. 3.1 and are discussed below.

In *Bridgman-Stockbarger* process, the container carrying the melt is moved in a fixed temperature profile and the melt is solidified from bottom to top. Heat extraction

takes place through the crucible and crystallization occurs at the crucible walls first, preventing the melt from further contamination. This however results in a higher thermal stress in the bottom of the ingot, resulting in higher dislocation densities in those regions.

In *gradient-freeze* process, the container and the heating system are fixed and temperature profile is varied by reducing the heat in a controlled way. Heat is extracted from the top and bottom surfaces of the ingot resulting in a uniform temperature profile over the cross section of the ingot, thus resulting in lower internal stresses and higher material quality. This also results in larger grain sizes and a columnar grain structure through the entire ingot. The walls of the container are kept at higher temperature for longer periods; hence care has to be taken to suppress contamination from the crucible walls.

Heat exchanger method (HEM) [11] is a special case of gradient-freeze process and is used for the growth of large crystals. A schematic of a conventional HEM furnace is shown in Fig. 3.2 [12]. A heat exchanger is seated at the bottom of the crucible through which there is a localized heat extraction. A stream of helium gas is forced through the heat exchanger to prevent it from melting. The process thus results in a homogeneous distribution of large columnar grains. Figure 3.3 shows a picture of a HEM system.

Picture of a typical HEM ingot after solidification is shown in Fig. 3.4 [13]. HEM furnace initially was adapted to produce single-crystal silicon ingots [14] but was later used to produce larger multicrystalline ingots [15, 16]. The advantages of growing an ingot through HEM include the ability to control the heat input and extraction independently, in-situ annealing of the ingot after growth, higher growth rates, and the elimination of labor intensive seeding step in the fully automated HEM furnaces [16].

mc-Si wafers grown by HEM have been used extensively for characterization and solar cell fabrication in this research.

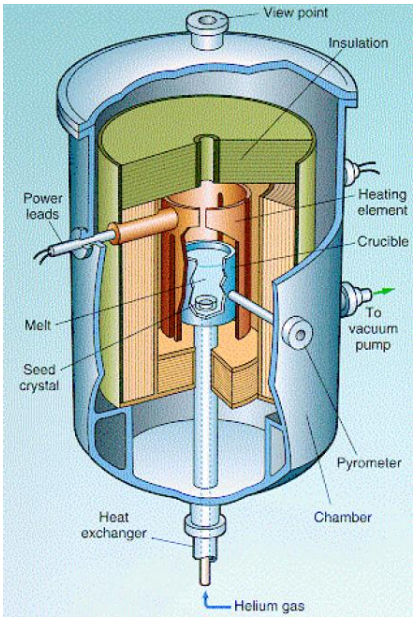


Figure 3.2 Schematic of a conventional HEM furnace with a seed crystal placed at the bottom of the crucible and on top of a heat exchanger [12].

Figure 3.3 Typical HEM system for growing mc-Si ingots.

Very recently there has been interest into casting the HEM wafers as sc-Si ingots, which can then be textured easily to improve the performance. *The first two single-crystal Si ingots grown by a novel HEM process have been characterized in this research to compare their performance with mc-Si HEM ingots.*

Figure 3.4 Typical HEM ingot after solidification [13].

In *directional solidification system (DSS)*, the crucible is kept stationary and the heat flow flux is controlled by the insulation movement. This technique results in shorter process times and a relatively planar solid-liquid interface. Bottom loading in a DSS furnace is much easier compared to the top loading in HEM furnace. Figure 3.5 shows a DSS system for growing mc-Si ingots. *The first experimental ingot grown by the DSS system has been analyzed in this research.*

Electromagnetic casting (EMC) [17] is based on induction-heated cold-crucible melt confinement and has no crucible bottom. The bottom platform is withdrawn downward, solidyfing the Si, while new Si feed material is introduced from the top [18].

The purity of EMC ingots is high and EMC also has the highest throughput of all the ingot technologies due to the ease of heat transfer to a cold environment. However, this results in a smaller grain size due to the rapid cooling.

Figure 3.5 DSS system for growing mc-Si ingots.

The main drawback of casting technology is that the wafers have to be sliced from the ingot with a wire saw. The sawing process results in a loss of ~40-50% of the original material, which is very undesirable. Certain growth techniques eliminate this step by solidifying Si in the form of sheets or ribbons. These technologies are briefly discussed in the next section.

3.2.3 Ribbon growth technologies

Ribbon Si materials, which are pulled directly from the melt to maximize Si usage, are also promising candidates for low-cost PV. However, due to the high thermal stress

during the growth, they suffer from many structural defects such as dislocations and twin boundaries. This results in reduced efficiency of solar cells compared to single-crystal Si and cast mc-Si. The most common ribbon growth technologies are: String Ribbon Si, edge-defined film fed growth (EFG), dendritic web growth (D-Web), and ribbon growth on substrate (RGS). In first three of these technologies solidification proceeds parallel to the sheet growth direction, whereas in RGS, solidification is perpendicular to the sheet growth direction. Some other ribbon growth technologies developed include silicon sheet from powder (SSP), supported web (S-Web), and ramp assisted foil transport (RAFT).

String Ribbon growth technique uses foreign filaments or strings to support the ribbon Si in between the strings. Figure 3.6 shows a schematic of the String Ribbon Si growth [19]. String Ribbon growth takes place directly from a pool of molten Si without a die. The position of the edges is maintained by two strings fed through the bottom of the crucible, which pass through the melt to support the meniscus and the ribbon. *String Ribbon silicon has been used in this research to study the lifetime enhancement via hydrogenation from PECVD* SiN_x *film.*

In *EFG growth* technique, liquid Si rises by capillarity up a narrow channel in the shaping die and spreads across the die's top surface, which defines the base of the meniscus from which the shaped crystal solidifies. *Dendritic web* Si is grown directly from molten Si in a crucible without any shaping devices. It typically has no grain boundaries except for some multiple twin boundaries running parallel to the external surfaces. In the *RGS growth* technique, the Si melt reservoir and die are placed in close proximity to the top surface of a substrate on which the ribbon is grown. Si wafers grown

by these techniques are not a part of this research; however the lifetime enhancement techniques studied in this thesis are applicable to these materials as well.

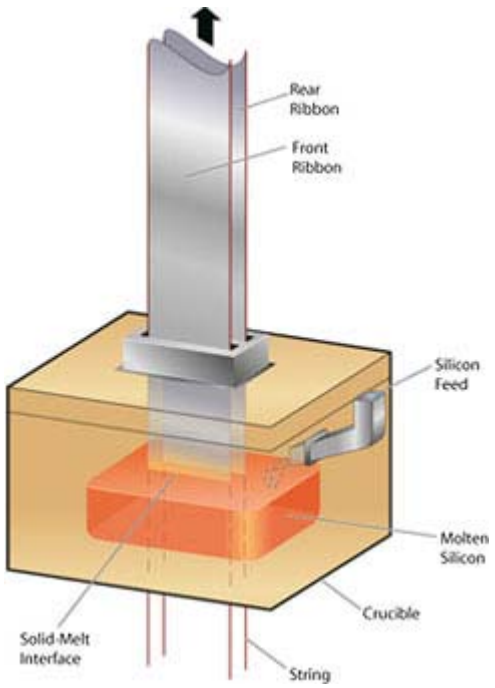


Figure 3.6 Schematic of a String Ribbon Si growth [19].

All the low-cost growth techniques suffer from low as-grown material lifetime. However, certain process steps can be applied to enhance the lifetime of these materials. These steps are discussed in the next section.

3.3 Lifetime enhancement of low-cost multicrystalline silicon

The performance of c-Si solar cells is a function of the quality of material used. Due to the low-cost and hence a poor quality of starting material used in PV, solar cell processing steps should be designed to improve the quality of the material in-situ. Due to the difference in the growth process of these low-cost materials, their impurity content and microstructure also varies, as a result, the response to various lifetime enhancing

steps is different for different materials. Several solar cell processing steps tend to either remove or passivate the harmful defects in the bulk of low-cost materials. *These techniques have been used and optimized in this research to achieve high-efficiency mc-Si cells.* This section first discusses these bulk-lifetime-enhancing steps of gettering and hydrogen passivation and then concludes by discussing the various surface passivation techniques employed.

3.3.1 Gettering

Gettering refers to the process in which the impurities are extracted from the active bulk region and are sent to accumulate in a region of a wafer, such as surfaces, where they are no longer active or harmful. These impurities then also can be removed by etching or by isolating from the active device regions such as the bulk for solar cell devices. The presence of these impurities can severely affect the cell performance [20]. To keep the processing cost down, it is desirable to incorporate the gettering treatments in conjunction with cell processing steps, such as emitter formation, rather than as a separate step. Gettering can be divided broadly into extrinsic and intrinsic gettering. *Extrinsic gettering* refers to techniques that use purposely applied regions, which can later be removed. *Intrinsic gettering* refers to the techniques that use the internal structures of a wafer such as oxygen precipitates, dislocations, or grain boundaries. As opposed to microelectronic devices, impurities need to be removed from the whole bulk of the device, which is the active region for solar cells. Also, gettering techniques can be divided into non equilibrium or relaxation gettering and equilibrium or segregation gettering. In relaxation gettering (eg., by silicon oxide precipitates) precipitate sites are intentionally formed in the regions away from the device surface and works on the

principle of impurity supersaturation. Segregation gettering is based on the gradient or discontinuity in the effective solubility of the impurity. Due to the difference in the electrochemical potential of the impurities, the regions of higher solubility act as sink for impurities in the lower solubility regions. This difference in solubility can result from the difference in phase (eg., between crystalline and liquid silicon during crystal growth), difference in material (eg., Al layers deposited on silicon surface), difference in doping levels in different areas of the wafers, or due to strain. An important feature of segregation gettering is that it requires no supersaturation as opposed to relaxation gettering, and hence even small impurity concentrations can be removed easily.

Gettering mechanism involves, in the same sequence, three basic processes: 1) Release of impurities; 2) Diffusion to gettering sites; and 3) Capture of impurities at gettering sites [21]. Any of these three steps can be a limiting mechanism for effective gettering. All steps exhibit strong temperature dependence, which should be considered when applying a gettering treatment, especially for mc-Si where material quality can severely degrade at high temperatures due to thermal degradation. Based on the capture part of the mechanism, Myers, et al., divided the gettering mechanisms into five groups: 1) Metal-silicide precipitation; 2) Segregation into second phases; 3) Atomic trapping at defects; 4) Interaction with electronic dopants; and 5) Phosphorous gettering [22]. Gettering by phosphorous is a special case of segregation into second phases, but is the most prevalent and easy to apply.

Gettering by phosphorous is a by-product of the n^+-p junction formation during solar cell processing, but this step should still be optimized to achieve most effective gettering, without sacrificing the junction quality [23]. Goetzberger and Shockley gave

the first evidence of gettering by phosphorous using P_2O_5 [24]. Phosphorous gettering combines the principles of both segregation and relaxation gettering together with enhanced diffusion of metals by injection of silicon self-interstitials and the kick-out mechanism [25, 26]. Different regions of cast mc-Si have different nature of impurities and defects, as a result wafers from these regions respond differently to gettering treatments [27]. Gettering efficiency can be reduced in the case of very bad regions, such as those with high dislocation density [28, 29] and for some highly stable compounds in mc-Si that cannot be removed by standard solar cell processing [30].

Gettering by aluminum (Al) is a by-product of the contact formation process in solar cells processing and also should be optimized to achieve most effective gettering without sacrificing the contact quality [23]. Al gettering and its beneficial effects have been studied extensively in the literature for both single-crystalline and mc-Si [31-34]. Impurities are segregated to the molten aluminum layer during contact formation due to the difference in the solubility of the impurity in the liquid Al-Si phase and in the solid Si [35].

Fast-diffusing impurities such as Fe, Cu. and Ni are gettered more easily compared to slow-diffusing impurities such as Ti and Mo [20]. P/Al co-gettering has been shown to be more effective than either treatment alone [36].

3.3.2 Hydrogen passivation

Hydrogen plays an important role in all silicon device processing techniques, since it can be incorporated at different stages in the device processing (intentionally or unintentionally) and can alter the electrical properties of the device. Hydrogen has both an acceptor and a donor state in the Si band gap. It exists as a positive charge state (H^+) in

p-type Si and as negative charge state in n-type material (H^-). H can passivate not only electrically active shallow acceptor and donor dopants, but also the deep level impurities in silicon. The hydrogen diffusion coefficient in Si was first determined at high temperatures by Van Wieringen and Warmoltz [37] and later confirmed by other researchers. This section reviews the configuration of H in Si, various methods used for incorporation of H in Si, passivation of deep and shallow levels by H, thermal stability of hydrogen passivation, and the diffusion of H in Si.

3.3.2.1 Configuration of H in Si

A comprehensive survey of the configuration of H in Si is provided in ref. [38]. According to the theoretical calculations, hydrogen is predominantly located at the bond-centered site in undoped Si and in p-type materials. In n-type material, H is located at the tetrahedral interstitial site. The possible charge states and configurations of hydrogen in p-type Si are: H^+, H^0, H_2, or Si-H. In n-type Si it exists as: H^-, H^0, H_2, and as H^0, H_2, or Si-H in undoped Si [38]. The trapping of hydrogen at the unsaturated Si bonds, such as point defects, grain boundaries, etc., forms the Si-H site, which has the lowest potential energy.

3.3.2.2 Incorporation of hydrogen in Si

Incorporation of hydrogen in semiconductors in a controlled way can be achieved in the following three ways: hydrogen plasma exposure, hydrogen implantation, and most recently, hydrogen introduced in Si via annealing of hydrogenated amorphous silicon nitride (SiN_x) films on top of Si. The first two techniques usually occur at low temperatures (typically 100-400 °C for the H plasma exposure and ~150 °C for H implantation) while the SiN_x hydrogenation, which is most common for solar cell

applications, typically proceeds at high temperature (≥ 700 °C). In the hydrogen plasma exposure, hydrogen is incorporated by exposure to low-power-density H_2 plasma. The penetration depth of hydrogen by this method can vary from a few tenths of a μm to ~ 100 μm. The second method of hydrogen implantation incorporates hydrogen in the semiconductor at low ion energy and high beam current. Ion sources, commonly called Kaufmann ion sources, however, have the disadvantage of causing surface damage due to ion bombardment. The penetration depth of hydrogen is typically ~ 1 μm in Si (hence useful for passivating a-Si solar cells). Due to the low diffusivity of H at low temperatures, the diffusion depth of H in Si is low for these methods and long processing times are required for passivation. To keep the processing time and cost down, it is preferable to include the passivation treatments in conjunction with cell processing steps, like hydrogenation from SiN_x during contact formation. Recently, it was confirmed that H is incorporated in Si via annealing of hydrogenated SiN_x films at high temperatures [39]. Due to high diffusivity of atomic hydrogen at high temperatures, this technique is useful for passivating defects deep inside the Si bulk; hence is most useful for solar cell applications, where low recombination is desired throughout the bulk.

3.3.2.3 Passivation of deep and shallow levels by hydrogen

Deep levels can be introduced by metallic impurities (Fe, Cu, Ni, Au, and other transition metals), oxygen and oxygen related thermal donors, process related defects, and crystalline defects in semiconductors. Deep level defects are most detrimental to the device performance but can be passivated by hydrogen. The mechanism of passivation of dangling bonds is clear; however passivation of metallic impurities is still debated. Hydrogen bonded to a dangling bond can form a bonding state that is pushed into the

valence band or an antibonding state that is pushed into the conduction band and thus becomes electrically inactive. The passivation of shallow level impurities in semiconductors has been very well established. For example in Si, the shallow acceptor levels originating due to boron [40], gallium, and aluminum are completely passivated by hydrogen. However, the donor levels such as those caused by phosphorous and arsenic can only be weekly passivated. The mechanism of passivation of negatively charged acceptor ions in p-type Si occurs by pairing due to coulomb attraction.

3.3.2.4 Thermal stability of hydrogen passivation

Defects passivated by hydrogen can be reactivated upon annealing. The reactivation of a passivated defect can be described by a simple model assuming first order kinetics and is given by [41]:

$$E_D = kT \ln\left[\frac{1}{t\upsilon}\left(\frac{N_0}{N}\right)\right], \qquad (3.1)$$

where:

E_D: Activation energy of dissociation; υ: Attempt (dissociation) frequency; N_0, N : Initial and final concentration, such that (N_0/N) represents the fraction of defect-hydrogen complexes remaining after annealing; and t: Annealing time at a temperature (T).

Most stable passivated defects generally are introduced by dislocations and grain boundaries. Deep level passivated defects are moderately stable followed by shallow level defects, which are the least stable to an annealing treatment. As an example, the recovery of hydrogen passivated shallow acceptors is shown in Fig. 3.7 [42]. Value of E_d for B, Ga, Al is 1.1, 1.6, and 1.9 eV, respectively, and varies between 2.2-2.5 eV for

common metals and is 2.5 eV for grain boundaries. Dislocations are most stable with dissociation energy of 3.1 eV [43].

3.3.2.5 Diffusion of hydrogen in Si

Diffusion coefficient (D) as a function of temperature is given by the Arrhenius law as:

$$D = D_0 \exp\left[-\frac{E_a}{kT}\right], \tag{3.2}$$

with E_a as the activation energy for hydrogen diffusion and D_0 as a prefactor.

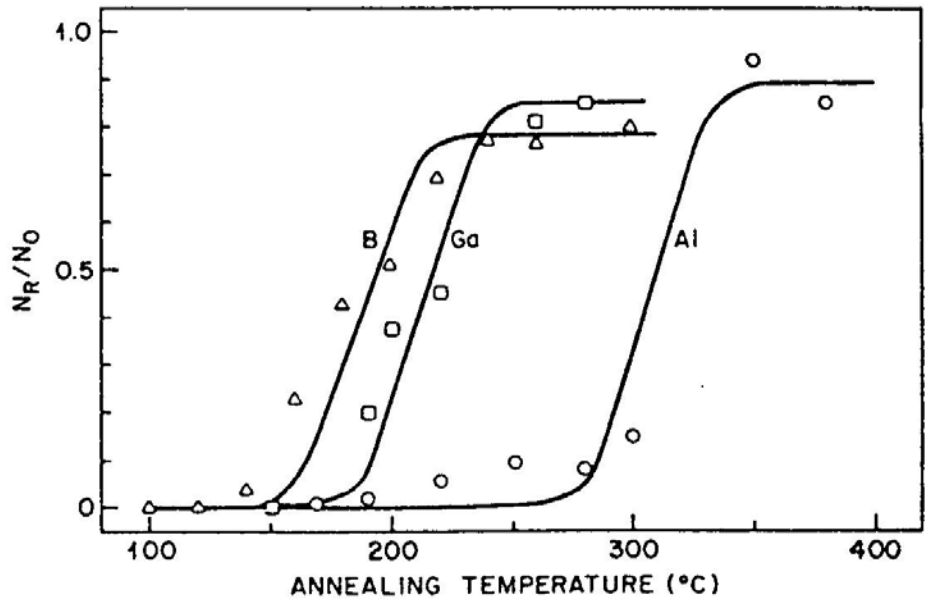


Figure 3.7 Recovery of electrical activity of passivated acceptors in Si.

Diffusion coefficient is an important characteristic to understand the diffusion mechanism of hydrogen in Si. First determination of the diffusion coefficient was performed by Van Wieringen and Warmoltz (VWW) [37], who determined the following relation for D (cm^2/s) to be valid in the high temperature (970 to 1200 °C) regime:

$$D = 9.4X10^{-3} \exp\left[-\frac{0.48}{kT}\right]. \tag{3.3}$$

For the low temperature regime (400 to 550 °C), Ichimiya and Furuichi [44] determined that the tritium diffusivity is given by:

$$D = 4.2X10^{-5} \exp\left[-\frac{0.56}{kT}\right]. \tag{3.4}$$

Presence of traps however impedes the diffusivity and results in an effective diffusion coefficient (D_{eff}) whose value could be several orders of magnitude lower than the trap free diffusivity at high temperatures. The extrapolation of VWW and Ichimiya and Furuichi diffusivity along with other experimentally determined diffusivities, as summarized in [38] for n- and p-type Si is shown in Fig. 3.8.

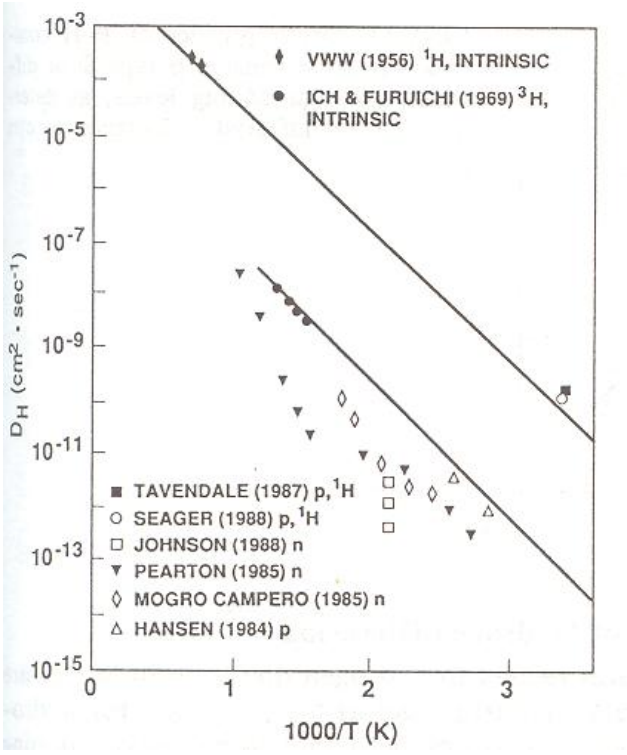


Figure 3.8 Extrapolation of VWW and Ichimiya and Furuichi diffusivities and other experimentally determined diffusivities.

From the diffusivity data, it can be concluded that, D_{eff} for low temperature range (25-350 °C) approachs the extrapolated VWW diffusivity for low hydrogen concentrations (Tavendale, et al., and Seager, et al.) and low impurity content [38]. For normal experimental conditions, D_{eff} is 2-3 order of magnitude lower than the VWW diffusivity, due to hydrogen bonding/trapping at the impurities in Si.

Passivation of defects in low cost mc-Si, deep inside the Si bulk, by high temperature annealing of SiN_x is due to the hydrogen released in the form of H^0 and is expected to follow the VWW diffusivity during the high temperature annealing process used to form the contacts to the solar cell. However this process has to be optimized to simultaneously yield an enhanced bulk and surface passivation and superior contacts. *This simultaneous optimization of hydrogen passivation and screen-printed contacts is studied and applied throughout this research.*

3.3.3 Surface passivation

Similar to the grain boundaries in the bulk of a mc-Si, surfaces introduce a continuous density of states in the Si band gap. These states can be passivated either by depositing various layers of dielectric (silicon oxide, silicon nitride, amorphous silicon, silicon carbide, and negatively charge dielectrics) or by adsorbed foreign atoms (HF or halogen: methanol solutions). Passivation of surface states by the dielectric layers is very important to attain high efficiency devices, especially on thinner substrates. This section reviews the common surface passivation techniques applied to solar cell surface passivation. Thermal stability of the passivation is very critical and should not degrade when the solar cell is annealed at high temperature (>700 °C) to form contacts. The stability of promising passivating layers is also discussed in this sub-section.

3.3.3.1 Silicon oxide (SiO_2)

Passivation of Si surface by silicon oxide (SiO_2) is widely used in semiconductor industry. Thermal oxidation takes place in oxygen ambient, typically at temperatures > 1000 °C. To improve the quality of oxide passivated interfaces, an additional low temperature (~400 °C) anneal in forming gas is applied. If this anneal is carried on with evaporated Al on top, then "alneal" process takes place, which improves the surface passivation further [45]. Record-high efficiency of solar cells fabricated have used the thermal oxide [46] and wet oxide [47] on single crystal and mc-Si substrates, respectively, to passivate the surfaces. The quality of SiO_2 layers degrades during the high temperature firing of screen-printed contacts in air ambient, however, the passivation can usually be recovered by a separate low temperature (~400 °C) FGA treatment or by alneal.

3.3.3.2 Hydrogenated PECVD amorphous silicon nitride (a-SiN_x:H)

Surface passivation by plasma-enhanced chemical vapor deposited (PECVD) silicon nitride (SiN_x:H) has been shown to provide excellent surface passivation [48]. SiN_x layers have been shown to provide low surface recombination velocities (SRV) of 4 cm/s on 1.5 Ω·cm p-type Si substrate [49]. Additional benefit of these layers is the low temperature (300-450 °C) deposition. However when applied directly to a p-type surface on the rear of a solar cell, SiN_x causes an inversion layer to build up, which causes parasitic shunting, leading to loss in J_{sc} of the solar cell [50]. Inversion layer is caused due to the high positive charge density of 1×10^{11}-5×10^{12} cm^{-2} in the SiN_x layer [51]. SiN_x layers have been shown to be very stable under high temperature annealing and represent an attractive option for low-cost cell processing.

3.3.3.3 Hydrogenated amorphous Si (a-Si:H)

Surfaces passivated by hydrogenated amorphous Si (a-Si:H) deposited at ~200 °C have been shown to provide excellent surface passivation [52]. High-efficiency solar cells have been produced by a-Si rear surface passivation [53]. However passivation provided by a-Si:H layer is unstable at high temperature, hence alternate low temperature device processing steps have been developed to preserve the superior surface passivation. This approach has recently resulted in >21% efficient HIT (Heterojunction with Intrinsic Thin-layer) solar cells [54] with surface recombination velocities of ≤ 10 cm/s.

3.3.3.4 Hydrogenated amorphous silicon carbide (SiC_x:H)

PECVD deposited hydrogenated amorphous silicon carbide (SiC_x:H) films have been shown to provide excellent surface passivation recently [55, 56]. High conversion efficiency (>20%) of solar cells utilizing SiC_x as back surface passivation have been reported [57]. SiC_x has also been shown to be stable under a high temperature annealing step and is a promising new material for surface passivation.

3.3.3.5 Negatively charge dielectrics

Negatively charge dielectrics (eg., Al_2O_3 [58] and $Al2O_3/TiO_2$ peudo-binary alloy [59]) have been shown recently to provide good passivation and high thermal stability (upto 1000 °C [59]). These also represent a new passivation mechanism which has potential for solar cell applications.

3.3.3.6 Iodine: methanol solution

Another common method for surface passivation that has been used throughout this research is the use of iodine:methanol solution. Halogen atoms adsorbed at the

surfaces provides very low surface recombination velocity of < 1 cm/s [60, 61] and provide a quick and easy way to determine the properties of bulk Si via lifetime measurements.

Certain passivating layers (eg., SiO_2) are not stable under the high temperature annealing step; however, a combination of these dielectric layers can achieve the desired passivation and thermal stability. For example, a silicon oxide and silicon nitride stack has been shown to be stable upon annealing [57] and provides low surface recombination velocity [62]. This stack can also avoid the parasitic shunting issues associated with passivation with SiN_x alone [57].

The next section describes the most common c-Si solar cell structures as well as advanced cell structures, which utilize superior pasivation provided by these dielectric layers.

3.4 Crystalline silicon solar cell: device design and optimization

CHAPTER 2 discussed the basic operation of an n^+-p junction solar cell. There are however several efficiency enhancing features in the final device. Many design features when applied to the front and back side of a device can yield greater generation, less recombination, and better collection of the carriers to produce high performance. Some of the features that can be controlled and optimized are the base doping density, doping profile of the diffused n^+ layer, passivation of the front and rear surfaces, reduced reflectivity of the front surface, and optimum design and formation of ohmic contacts. Several device structures have been developed, however the basic n^+-p-p^+ device is the most common in PV industry today. This basic structure has been optimized and utilized

throughout this research and also serves as a reference to compare the effects of efficiency enhancing design changes that are selectively introduced.

3.4.1 Conventional features of n^+-p-p^+ solar cell with full area aluminum back surface field

A cross section view of the standard n^+-p-p^+ device structure that has been fabricated throughout this research is shown in Fig. 3.9. It consists of a p-type Si with an n^+ layer diffused on top to form the n^+-p homojunction. On the front is an antireflection coating (ARC) (usually SiN_x) and a metal contact grid (usually Ag). Al typically forms the back contact. In a conventional low cost process sequence, screen-printed Ag on top of SiN_x, punches through the SiN_x layer to form the front contact upon annealing at high temperature (>700 °C). On the rear side, for annealing temperatures greater than the Al-Si eutectic (577 °C), an Al doped p^+ layer, also know as Al back surface field (Al-BSF), is formed. Al metal on top of Al-BSF forms the rear contact in the same step. The regions in Fig. 3.9 are not drawn to scale. Typical thicknesses of these regions are 700-1100 Å, 0.25-0.5 μm, 5-8 μm, and 10-30 μm for the ARC, n^+ emitter, Al-BSF, and Al contact, respectively. Base thickness typically varies from 100-300 μm.

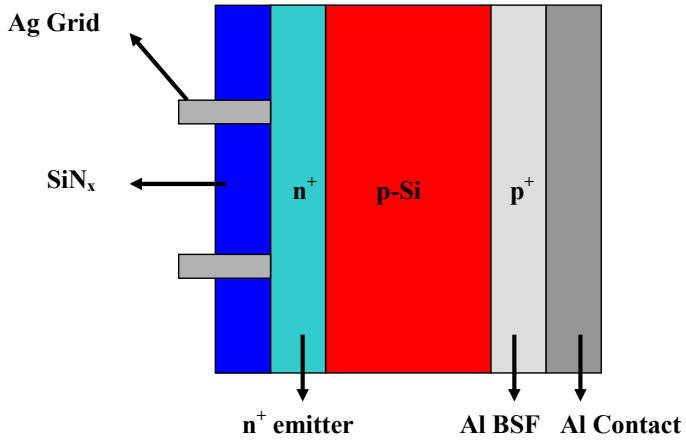


Figure 3.9 Cross-section of the n^+-p-p^+ solar cell (not drawn to scale).

3.4.2 Advanced cell design with local BSF

The BSRV provided by Al-BSF is in the range of 350-500 cm/s [63], which is not sufficient for very high efficiency cells. In addition, full Al-BSF formed by screen-printed Al warps thin wafers [64]. Dielectric passivation can solve both the problems. However, the rear metal contact for devices that use dielectric passivation has to be made by either opening the dielectric locally or by firing through the dielectric. Figure 3.10 illustrates such a structure, where local BSF is formed underneath the point contacts. As shown in the Fig. 3.10, minority carrier electrons would be repelled at the local BSF points, decreasing contact recombination, and the series resistance.

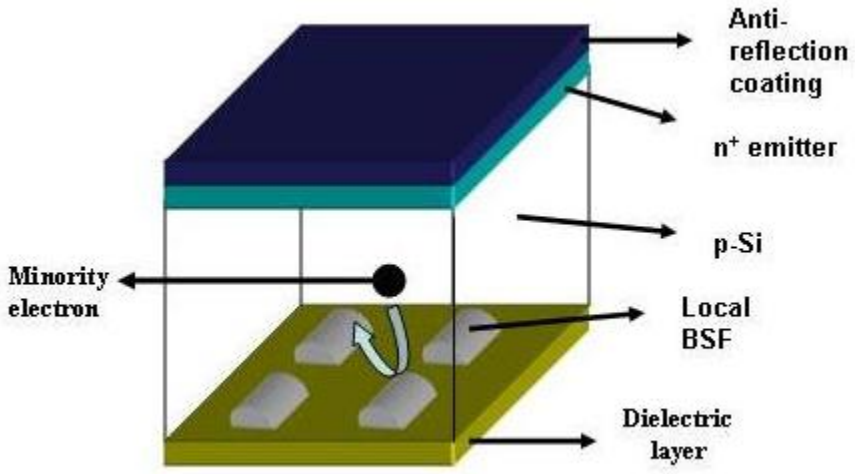


Figure 3.10 Dielectric-passivated, local BSF solar cell structure.

The challenge is to open vias through the dielectric by a low-cost technology. Photolithography and laser ablation type techniques have been used but these techniques add additional steps and increase the cost. Secondly, a good quality local BSF needs to be formed through this vias. Finally, the choice of dielectric is also important for such

structures. For example, if SiN_x is used to passivate the back, it can lead to parasitic shunting at the back contact, lowering the J_{sc} [50]. Similar care has to be taken to fabricate the devices that use n-type floating junction to passivate p-type Si [65]. These extra steps however increase the manufacturing cost.

In this thesis, attempt has been made to form cells on thin wafers with local Al-BSF using a novel dielectric and contact formation technique.

3.4.3 Review of high-efficiency solar cell structures

This section discusses some of the contemporary high-efficiency solar cell structures fabricated in the laboratory and on industrial scale.

3.4.3.1 PERL cell:

PERL cell (Fig. 3.11) utilizes most of current technological advancements in the solar cell design [66]. The structure has produced 24.7% efficiency, the highest efficiency for a c-Si device under 1 sun illumination. However it uses eight high-temperature, five masking, and five photolithography steps.

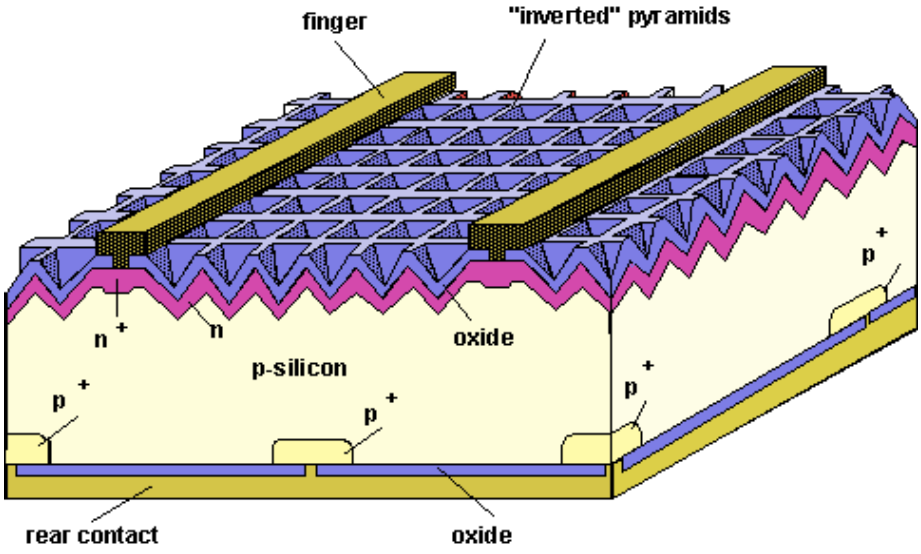


Figure 3.11 Structure of a passivated emitter, rear locally-diffused (PERL) cell [66].

Salient features of the PERL cell that minimize the reflective, resistive, and surface recombination losses include [66, 67]:

- High quality, thick base material.
- Front surface texturing by inverted pyramids.
- Excellent front and back surface passivation by thin silicon oxide (SiO_2).
- Selective emitter with heavy doping underneath the grid and light doping in between.
- Local boron diffused BSF.
- Rear reflector and light trapping with evaporated Al.
- Double layer ARC.
- Evaporated front contacts.

3.4.3.2 Fraunhofer ISE's high efficiency mc-Si cell:

In 2004 Fraunhofer ISE announced the highest efficiency to date of 20.3% on mc-Si with an area of 1 cm^2 [68]. The structure of the cell is shown in Fig. 3.12 [69]. This device structure utilized evaporated contacts, double layer ARC, thin SiO_2 for surface passivation, plasma-textured front surface, a thin base (99 μm), SiO_2 passivated rear surface, evaporated Al for back mirror, and high doping concentration under rear contacts. The key feature was the use of wet oxidation and laser-fired contacts (LFC), which locally anneals the rear point contacts and leaves the passivated oxide around the contact unaffected and well passivated [70].

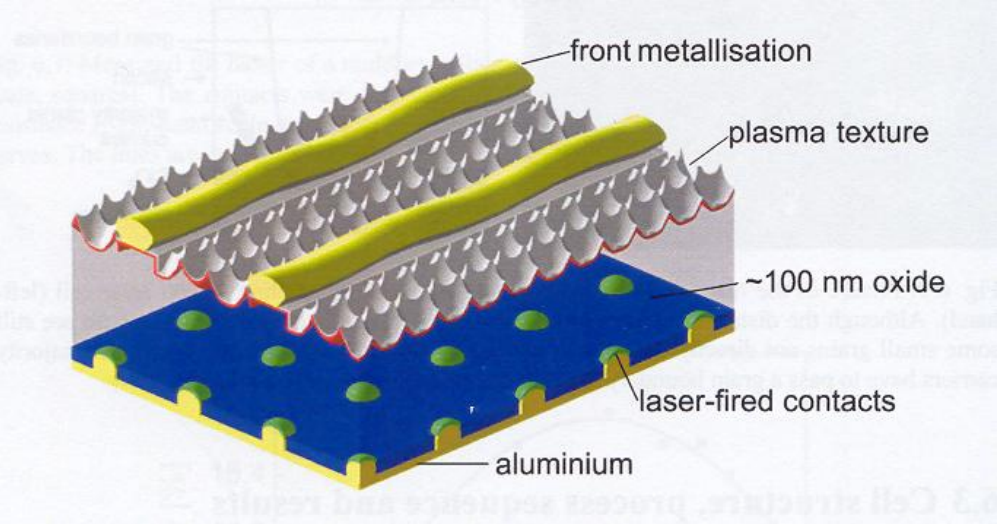


Fig 3.12 Device structure of 20.3% efficient mc-Si by Fraunhofer ISE.

All these high-efficiency device features discussed above require very clean fabrication processes, along with complex and multiple steps and are not practical for low-cost fabrication. However, high performance demonstration has provided knowledge and guidelines for processing these structures in a cost-effective manner.

3.4.3.3 SunPower back contact cell:

SunPower Corporation designs and manufactures the highest available commercial c-Si modules [71]. Basic structure of SunPower's back contact cell is shown in Fig. 3.13 [72].

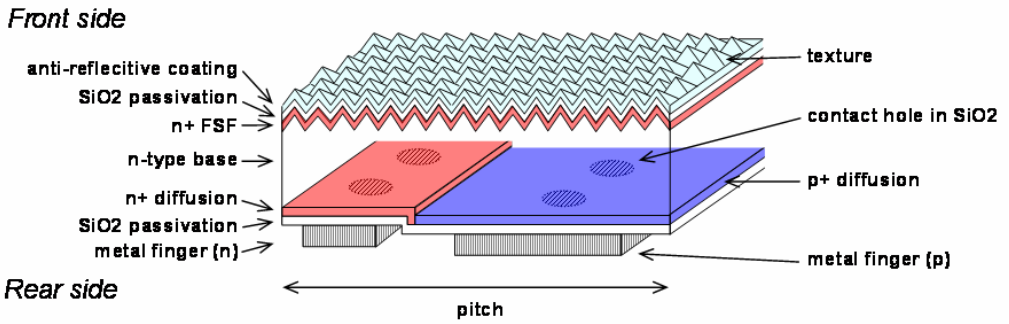


Figure 3.13 SunPower's back contact A-300 solar cell structure [72].

Key features of Sunpower's design include interdigitated n^+ and p^+ diffusions to reduce recombination loss at the contact. The contact grid lines are located entirely at the rear of the cell, which completely eliminates the shadow loss of the incident light [72].

SunPower's device requires multiple high temperature steps, however high conversion efficiency is achieved on large area devices (149 cm^2). SunPower began ramping up their Gen 2 solar cells in January 2008, with a cell efficiency of 22.4% and a high module efficiency of 20.1%. Recently they announced their Gen 3 device with a high efficiency of 23.4%. Improved efficiency from the previous designs was due to improved patterning techniques, lower carrier recombination, higher carrier collection, and lower series resistance.

3.4.3.4 Sanyo's Hetero-junction with Intrinsic Thin-layer (HIT) cell structure:

Sanyo Electric Co. announced large area (100.3 cm^2) solar cells using the HIT structure with a conversion efficiency of 21.5% [73]. HIT solar cell structure is shown in Fig. 3.14 [73].

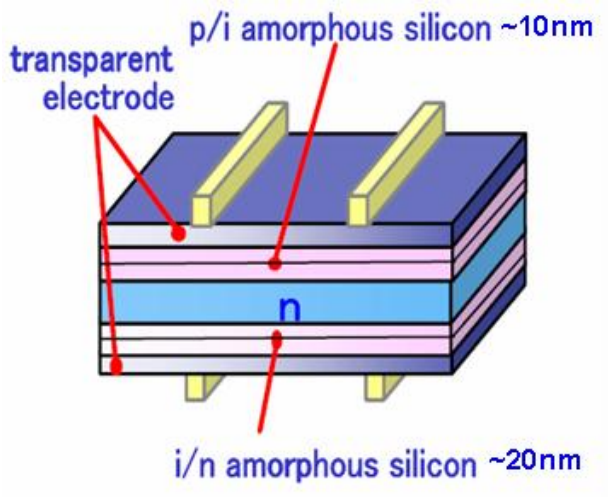


Figure 3.14 Device structure of HIT cell [73].

HIT structure consists of a n-type ~200 μm thick substrate, with a top a-Si:H p/i layer of thickness 10 nm and bottom a-Si:H i/n layer of thickness 20 nm, which passivate the surfaces. Cell processing is done at temperatures below 200 °C to preserve surface passivation by a-Si:H.

3.5 Conclusions

Crystalline Si can be grown in the form of single crystal or multicrystalline Si. Multicrystalline Si can be grown either as ingots or sheets. The bulk quality of the low cost mc-Si wafers can be improved by the techniques of gettering and hydrogen passivation, which should be incorporated in the cell processing steps to keep the processing cost down. Solar cell design criteria revolve around maximizing J_{sc} and V_{oc} and minimizing the power loss from parasitic mechanisms (series and shunt resistance). Several advance design features can be employed to improve the performance of the device; however they should be incorporated in a way that does not increase the cost.

CHAPTER 4

FABRICATION AND OPTIMIZATION OF BASELINE SILICON SOLAR CELLS

4.1 Introduction

This chapter focuses on the fabrication and optimization of baseline solar cells on p-type Si. Section 4.2 discusses the fabrication sequence employed. The diffusion profile optimization for different sheet resistance emitters is presented in section 4.3, followed by a discussion of the firing profile optimization to form high-quality contacts. Section 4.3 concludes with an investigation of the passivation provided by two different kinds of silicon nitride films (low- and high-frequency) suitable for solar cell manufacturing.

4.2 Fabrication of baseline silicon solar cells

Baseline Si solar cells refer to the conventional front junction n^+-p-p^+ solar cell structure, Fig. 3.9, currently most prevalent in the industry. Solar cells fabricated by an optimized baseline process on 300 μm thick Si have been used throughout this thesis as reference or control cells to study the effects of key material and device parameters, such as base (material, thickness, resistivity, and doping type) and emitter profile (sheet resistance of diffused emitter surface and junction depth).

To fabricate the baseline solar cells, p-type Si wafers first are chemically etched in acid to remove the saw damage followed by a standard RCA clean. Wafers are then diffused using liquid phosphorus oxychloride ($POCl_3$) as the dopant source to form the n^+ emitter. The glass formed on the wafer surface after the diffusion process is etched off in dilute HF and wafers are coated with a PECVD SiN_x film on top of the emitter to serve as

an ARC. Al paste is then screen-printed on the rear followed by screen-printing of Ag grid on the front using commercial pastes. Front and back contacts are co-fired at ~750 °C using an optimized process in a lamp-heated IR belt furnace, resulting in simultaneous formation of an Al-doped p^+ back surface field (BSF), back Al contact, and the front Ag grid metallization. Cells are then mechanically isolated with a dicing saw to define an active cell area of 4 cm^2. Finally, cells are annealed at 400 ^oC for 15 min in forming gas before testing and analysis. This fabrication sequence is summarized in Fig. 4.1.

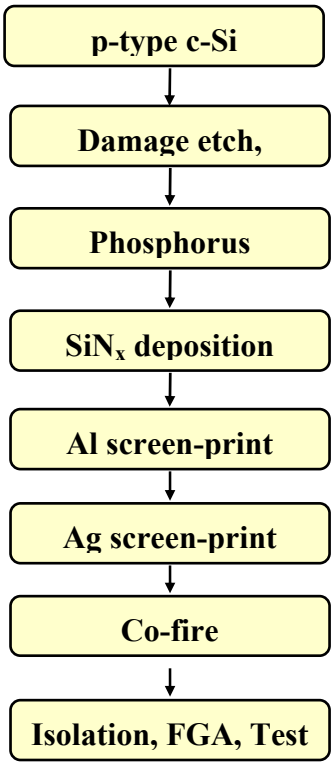


Figure 4.1 Fabrication sequence for baseline p-type c-Si solar cells.

4.3 Optimization of baseline silicon solar cells

Each step in the fabrication sequence shown in Fig. 4.1 has to be optimized to achieve high-efficiency solar cells. A study was conducted to optimize the emitter profile

for screen-printed contacts to achieve higher J_{sc} in conjunction with a lower loss from parasitic series and shunt resistances. SiN_x films, deposited in two different reactors (low- and high-frequency PECVD), were compared to determine their efficacy in passivating the emitter surface and the bulk defects in solar cells. This section discusses the results of optimization that led to high-efficiency baseline solar cells.

4.3.1 Emitter diffusion

Phosphorus diffusion profiles of different sheet resistance emitters fabricated and studied in this research are shown in Fig. 4.2. These emitters were formed on polished n-type Cz wafers in a tube furnace to determine the phosphorus concentration profile via spreading resistance measurements. Change in sheet resistivity and profile was achieved by changing the diffusion temperature, which ranged from 890 to 835 °C, resulting in sheet resistivity in the range of 40 to 120 Ω/sq. The emitter saturation current density (J_{0e}) is a function of the phosphorus surface concentration, profile, and the emitter penetration depth [74]. However for a given penetration depth, J_{0e} has an optimum (lowest) value, which is a function of surface concentration and surface recombination velocity.

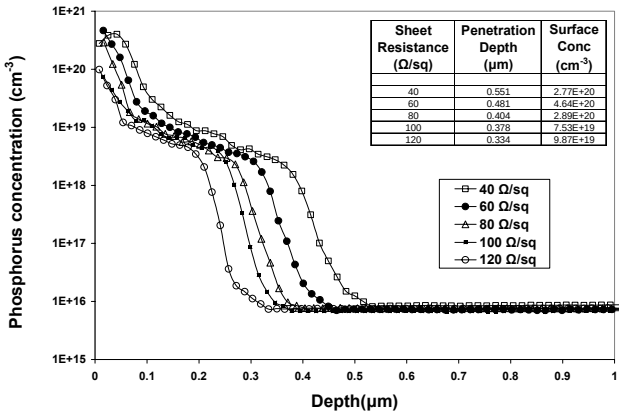


Figure 4.2 Spreading resistance measurements to determine the diffused phosphorus concentration for emitters with sheet resistivity varying from 40 Ω/sq to 120 Ω/sq.

Contact resistivity increases to >1 $m\Omega cm^2$ for surface concentration values $<5 \times 10^{19} cm^{-3}$ [75], however a high surface concentration, which is desirable for low contact resistivity, would lead to increased recombination in the emitter region thus reducing the J_{sc}. Furthermore, Ag crystallite growth, which establishes a current path for electron transport from emitter to metal grid, is also shown to be dependent on the phosphorous surface concentration [76]. Figure 4.2 shows that both penetration depth and surface concentration decrease as sheet resistivity increases. Hence there is a tradeoff between J_{sc} and series resistance as we go towards high sheet-resistance emitters. Optimized emitter profiles shown in Fig 4.2 were obtained by adjusting the diffusion time and temperature in the tube furnace to give a high enough ($> 5 \times 10^{19} cm^{-3}$) surface concentration (for reduced contact resistance) even for lower penetration depths (for increased J_{sc}). It should however be noted that the low sheet resistance emitters maintain a higher concentration of diffused phosphorous inside the Si and generally lead to a more tolerant contact firing process. Shallow emitters would be more prone to shunting if the front contact metal diffuses into the junction during contact firing.

4.3.2 Development of an optimized co-firing cycle in a belt furnace to form the front and back contacts

Commercially available Ag and Al pastes were used for screen-printing. Eight finger front grid pattern was used for low sheet-resistance emitters (~45 Ω/sq) and 10 finger pattern for high sheet-resistance emitters (>70 Ω/sq). The finger, bus bar width, and spacing was optimized to provide least shading, without increasing the power loss from parasitic resistances. Thickness of screen-printed Al was ~40 μm, which formed a uniform BSF at the peak annealing temperature.

Figure 4.2 shows three different firing profiles, with different peak temperatures, measured on the Si wafer traveling through the belt. Firing profiles were tailored by adjusting the belt-zone temperatures and the belt speed. Firing profiles were optimized for each Ag and Al paste combination used for different sheet-resistance emitters by varying the ramp-up and ramp-down rates, and the peak temperature, to yield solar cells with uniform BSF, low series resistance, and no shunting.

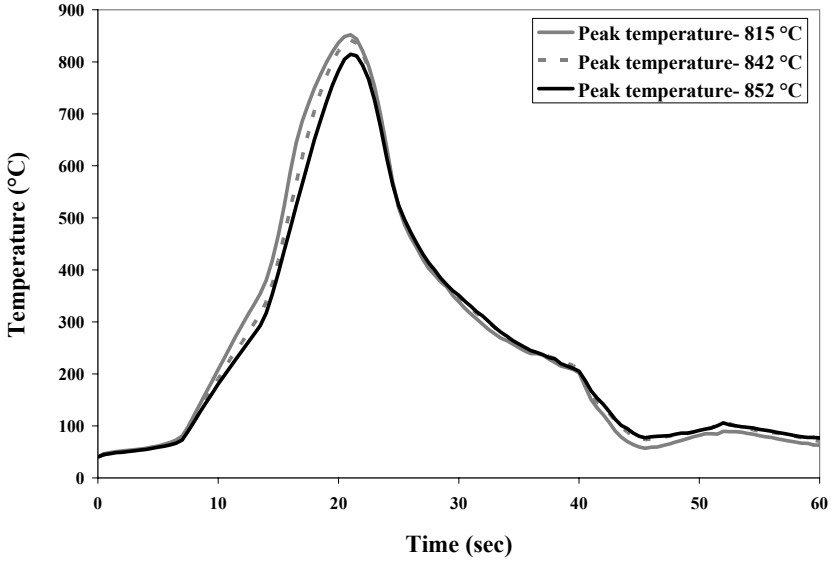


Figure 4.3 Temperature firing profiles in a belt furnace with high ramp-up and ramp-down.

4.3.3 Passivation provided by low- and high-frequency PECVD SiN_x films

Bulk lifetime enhancement and good surface passivation are important for high efficiency solar cells. It has been shown that Plasma-Enhanced Chemical Vapor Deposition (PECVD) of silicon nitride (SiN_x) can accomplish both [77-80], but the degree of enhancement is a function of SiN_x deposition and annealing conditions. In this study, two types of SiN_x films were evaluated for emitter surface and bulk defect passivation of the solar cells. The first film was grown at low-frequency (LF) at 425 ^{o}C in

a horizontal tube reactor, and the second film was deposited at high-frequency (HF) in a parallel plate reactor at 300 ^{o}C. The quality of emitter surface passivation was quantified by J_{0e} measurements and bulk passivation was quantified through lifetime measurements. In addition, solar cells were fabricated and analyzed by IV and IQE measurements to study the impact of surface and bulk defect passivation from LF and HF SiN_x films. The bulk lifetime in HEM mc-Si was also monitored in sister wafers to characterize the bulk lifetime enhancement due to hydrogenation from LF and HF SiN_x films during the contact anneal cycle. Thus this study includes the effect of three variables: frequency, temperature, and reactor.

4.3.3.1 Impact of LF and HF PECVD SiN_x films on emitter surface passivation

Various values of J_{0e} have been reported in the literature for different sheet resistivity emitters passivated with SiN_x films [79, 81-84]. Si rich SiN_x films (index >2.3, measured at 633 nm) are known to give a lower J_{0e} [81]. However, nearly stoichiometric SiN_x films (index ~2.0), which are more suitable for solar cells because of low absorption, were analyzed in this study.

For the J_{0e} measurements, symmetric n^+-n-n^+ structures were prepared on ~700 Ω·cm n-type FZ Si wafers. The wafers were etched chemically in acid before a standard RCA clean. Phosphorus diffusions were performed at various temperatures in the range of 835 ^{o}C to 915 ^{o}C with $POCl_3$. The sheet resistivity was measured on each wafer with a four point probe after removing the phosphorous glass layer in dilute HF. By varying the temperature from 915 ^{o}C to 835 ^{o}C, sheet resistivities in the range of 30 Ω/sq to 120 Ω/sq were obtained. Silicon nitride was deposited on both sides of each wafer using direct LF and HF PECVD reactors. The HF PECVD SiN_x film was deposited at a frequency of

13.56 MHz and at a temperature of 300 ^{o}C while the deposition of LF PECVD SiN_x was performed at a frequency of 50 kHz and a temperature of 425 ^{o}C. J_{0e} was measured on each wafer before and after a heat treatment in an IR-heated belt furnace using the same temperature profile that is used for contact firing during solar cell processing. J_{0e} was obtained by the transient photoconductance decay technique (tcpd) using the slope of inverse effective lifetime ($1/\tau_{eff}$) vs. excess carrier concentration (Δn) [85].

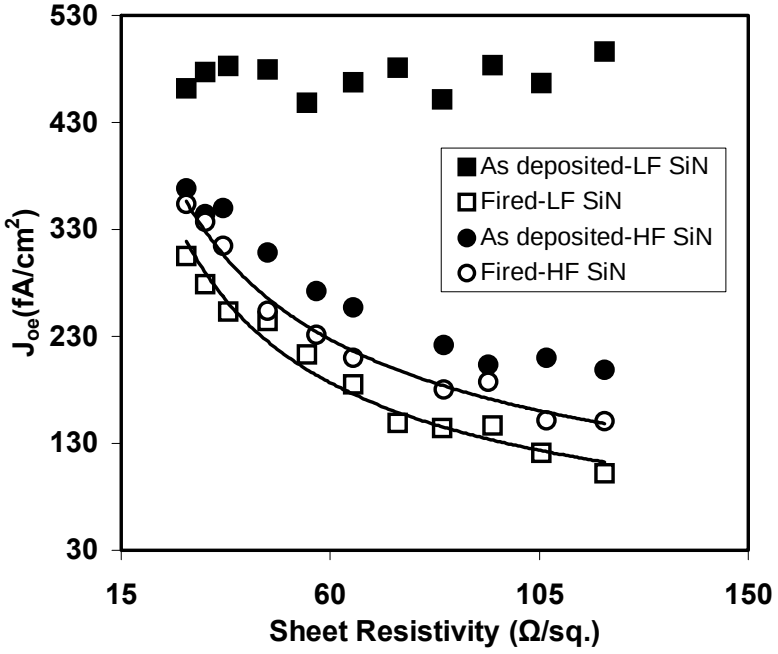


Figure 4.4 J_{0e} comparison for phosphorous diffused n^+ emitters with different sheet resistivities for LF and HF SiN_x. The trend line is a guide to the eye.

Fig. 4.4 shows that the J_{0e} values for as-deposited LF SiN_x were very high (~ 480 fA/cm^2) and relatively independent of the sheet resistivity. On the other hand, the as-deposited J_{0e} values for the HF SiN_x were much lower and decreased from 368 to 199 fA/cm^2 as the sheet resistance increased from 30 to 120 Ω/sq. However, after firing in the belt furnace, the J_{0e} values for LF SiN_x decreased substantially, and became lower than the HF SiN_x counterpart. For example, for the 45Ω/sq emitter passivated by LF SiN_x, the

J_{0e} dropped from 480 fA/cm^2 to 244 fA/cm^2 after firing while the J_{oe} for the HF SiN_x passivated emitter decreased from 308 fA/cm^2 to 254 fA/cm^2 after firing. This effect was even more pronounced for higher sheet resistance emitters. For a 95Ω/sq emitter the J_{0e} decreased from 484 fA/cm^2 to 147 fA/cm^2 after firing the LF SiN_x, while the J_{0e} dropped from 203 fA/cm^2 to only 187 fA/cm^2 in the case of HF SiN_x. Note that the J_{oe} decreases as the sheet resistivity increases, or surface concentration decreases [74]. The J_{0e} values reported here are not the lowest [86] because the SiN_x films in this research were optimized for best solar cell performance, rather than surface passivation.

The higher post-deposition J_{0e} for the LF films, compared to the HF films, can be explained by the greater degree of surface damage caused by the plasma ions in the low frequency reactor during the deposition. However, a more dramatic decrease in J_{0e} after the anneal of the LF films indicates that the hydrogen trapped at LF SiN_x-Si interface defects is released during annealing and is able to passivate the emitter surface more effectively compared to the HF SiN_x films [87].

4.3.3.2 Impact of LF and HF PECVD SiN_x films on FZ and mc-Si cell performance and bulk defect passivation

Solar cells were fabricated on ~1 Ω-cm p-type FZ Si and ~1.5 Ω-cm HEM cast mc-Si using the baseline process to determine the effect of depositing and annealing LF and HF SiN_x films on the emitter surface and bulk defect passivation. $POCl_3$ diffusion was used to form a ~45 Ω/sq emitter, followed by deposition of LF and HF SiN_x AR coating on the front. The bulk lifetime in HEM mc-Si was monitored in sister wafers to characterize the bulk lifetime enhancement due to hydrogenation from LF and HF SiN_x films during the contact anneal cycle. Lifetimes were measured before and after firing in the belt furnace. Bulk lifetimes were measured by the quasi steady state

photoconductance technique (QSSPC) [88] with surfaces passivated by an iodine-methanol solution [60]. Post cell processing lifetimes were measured by chemically etching off the metal contacts, SiN_x layer and the emitter and Al-BSF and then performing QSSPC lifetime measurements by passivating surfaces in iodine-methanol solution.

Table 4.1 I-V data for 4 cm^2 solar cells on FZ and mc-Si wafers for LF and HF coated SiN_x.

Wafer type/ System	Eff (%)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)
FZ LF	17.2	34.64	632	78.4
FZ HF	16.8	33.89	630	78.8
HEM LF	16.8	34.24	627	78.0
HEM HF	16.1	33.22	623	77.6

The solar cell data in table 4.1 shows that LF SiN_x gives higher J_{sc} and V_{oc} and solar cell performance. The difference in V_{oc} is 2 mV for FZ cells with HF and LF SiN_x, while in the case of the HEM mc-Si cells, this difference increases to 4 mV. Table 1 also shows that the difference in J_{sc} between FZ cells with LF and HF SiN_x is 0.75 mA/cm^2. IQE and diffuse reflectance measurements were performed on FZ and mc-Si cells with HF and LF SiN_x films to determine if the difference in J_{sc} and V_{oc} are due to surface reflectance, surface recombination, or bulk recombination. Fig. 4.5 shows that the reflectance of FZ solar cells with LF and HF SiN_x AR-coatings are very similar and cannot account for the difference in performance between the FZ cells. Fig. 4.5 shows that the short wavelength (350-650 nm) IQE of the FZ cell with LF SiN_x coating is superior to that of the FZ cell with the HF SiN_x coating, indicating a higher degree of front surface passivation provided by LF films. For example, there is a 6% enhancement

in the IQE response for the LF SiN_x at 450 nm, relative to the HF SiN_x at the same wavelength. Figure 4.5 also shows that the choice of the SiN_x film did not affect the long wavelength IQE response of FZ cells, indicating no appreciable change in Al BSF quality or lifetime.

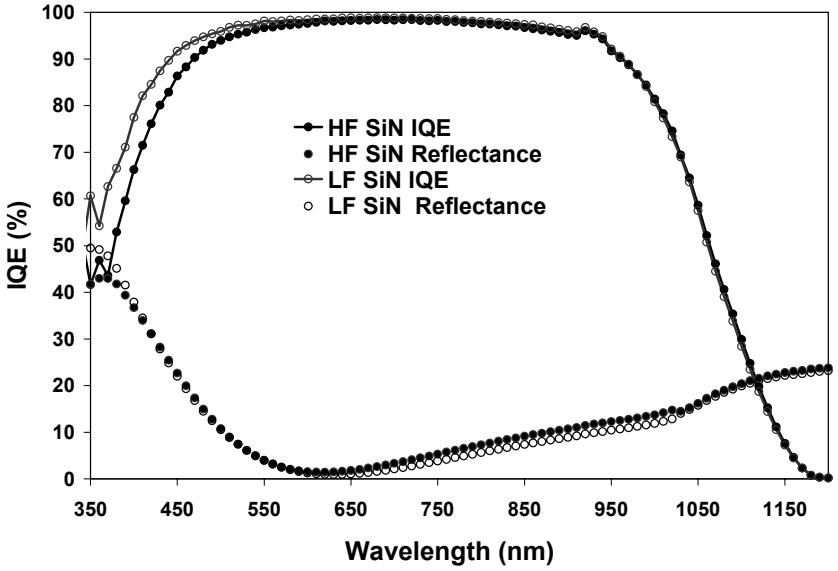


Figure 4.5 IQE response and reflectance for LF and HF SiN_x coated FZ wafers.

Figure 4.6 shows the IQE response of the two HEM mc-Si cells with HF and LF SiN_x. Similar to the FZ cells, the short wavelength response is greater for the LF SiN_x coating. In contrast to the FZ cells, the HEM mc-Si cell with the LF SiN_x coating show superior long wavelength response. This is indicative of more effective bulk defect passivation relative to high frequency SiN_x. This is further supported by Fig. 4.7, which shows the average as-grown lifetime, post-cell-processing lifetime, and corresponding solar cell efficiencies for a high and low as-grown lifetime HEM wafers.

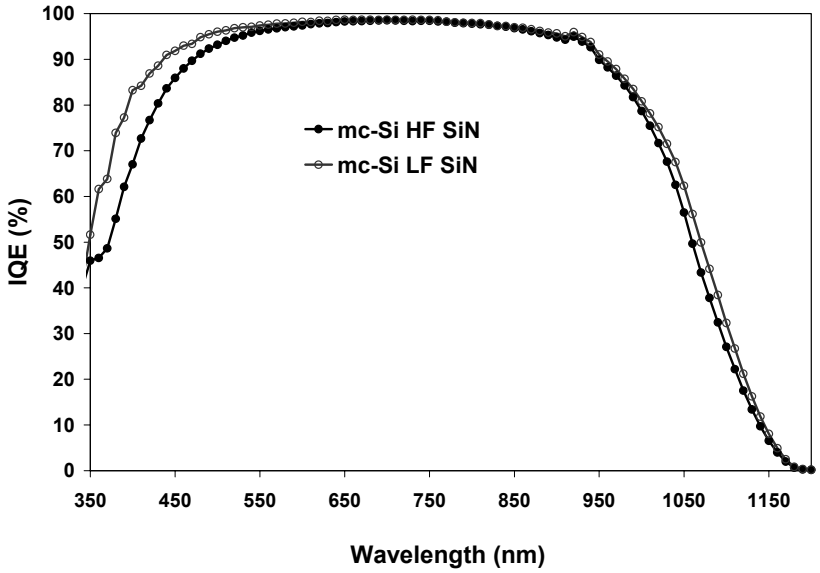


Figure 4.6 IQE response for LF and HF SiN_x coated HEM wafers.

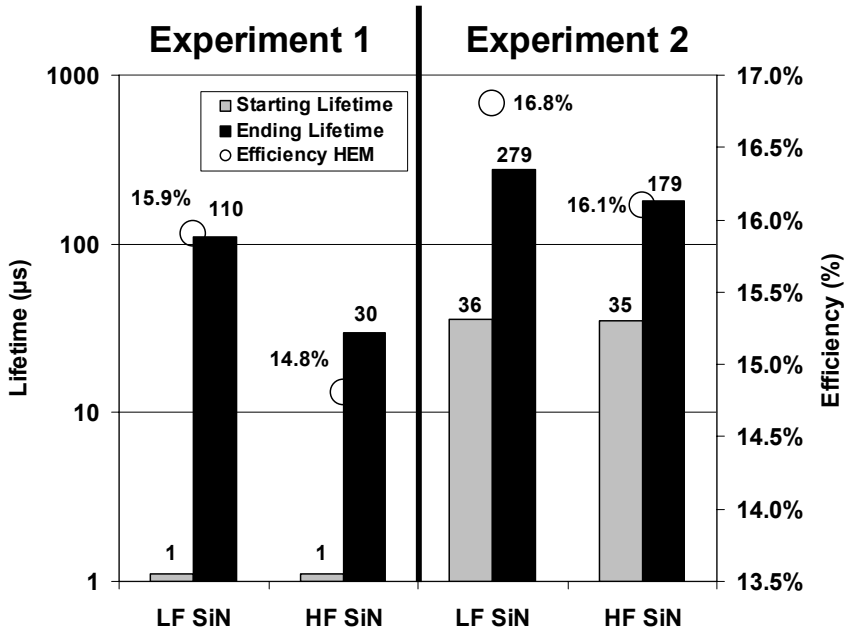


Figure 4.7 Average as-grown and post-processing lifetime in HEM mc-Si wafers with LF and HF SiN_x and the corresponding cell efficiencies.

The carrier lifetime for the HF SiN_x deposited at 300 ^oC improved from 1 µs to 30 µs for lower lifetime mc-Si wafer (experiment 1) and from 35 µs to 179 µs for the high lifetime mc-Si wafer (experiment 2), resulting in cell efficiencies of 14.8% and 16.1%,

respectively. The LF SiN_x deposited at 425 ^oC improved the bulk lifetime from 1 to 110 μs in low lifetime wafer (experiment 1) and from 36 μs to 279 μs in the high-lifetime wafer (experiment 2) with corresponding cell efficiencies of 15.9% and 16.8%, respectively. The data in Fig. 4.7 shows that the defect passivation from the LF SiN_x is more effective and also reduces the efficiency gap between the cells made on low and high lifetime HEM mc-Si wafers. Thus, the LF SiN_x film deposited at 425 ^oC results in higher efficiency FZ cell due to superior emitter surface passivation and higher efficiency mc-Si cells because of improved emitter surface passivation as well as bulk defect passivation.

It should however be pointed out that the density of the LF films deposited in this study was higher than the HF films due to a higher deposition temperature (425 °C for LF compared to 300 °C for HF). It has been shown in literature that higher density films provide better passivation [89]. *These optimized LF SiN_x films, deposited at 425 °C, are used throughout this thesis for solar cell fabrication.*

4.4 Conclusions

This chapter describes the process sequence of a baseline solar cell used in this research. Each process step in the fabrication sequence is optimized to achieve high efficiency. $POCl_3$ emitter diffusion profiles are optimized to achieve high phosphorus surface concentration (for reduced contact resistance) and lower penetration depths (for increased J_{sc}). Front Ag contact grid is optimized in conjunction with the emitter sheet resistance to provide low contact resistance and shading losses. Optimized firing profile is developed for co-firing of Ag and Al pastes, which also improves the material quality via hydrogenation of defects. Emitter surface and bulk defect passivation provided by the

LF SiN_x film deposited at 425 °C was found to be superior for LF SiN_x films deposited at 425 °C compared to a HF SiN_x film deposited at 300 ^oC. The contact firing cycle is found to induce a significant decrease in the J_{0e} of the LF SiN_x passivated phosphorus doped emitters. J_{0e} values for LF SiN_x reduced dramatically after contact firing to 100-200 fA/cm^2, well below the J_{0e} for fired HF SiN_x passivated emitters. This is attributed to annealing of the as-deposited damage at the emitter surface. During the post-deposition firing, hydrogen is released from the SiN_x film and improves the passivation of the emitter surface and defects in the bulk. Baseline solar cells fabricated on FZ and mc-Si with LF SiN_x gave efficiencies of 17.2% and 16.8%, respectively, while the corresponding efficiencies were 16.8% and 16.1% for the HF SiN_x ARC. The enhanced cell performance of LF SiN_x coated sample is corroborated by a higher short wavelength IQE due to better emitter surface passivation in both FZ and mc-Si cells and a higher long wavelength IQE in mc-Si due to better bulk defect passivation. The LF SiN_x film employed in this study gave significant improvement in bulk lifetime and J_{0e} and reduced the performance gap between cells made on low- and high- lifetime HEM mc-Si wafers.

CHAPTER 5

UNDERSTANDING OF HYDROGEN DIFFUSION IN SILICON FROM PECVD AMORPHOUS SILICON NITRIDE

5.1 Introduction

The SiN_x coating on the front side of a solar cell serves not only as an anti-reflection coating but also passivates the defects in the bulk of the low-cost solar cell materials by releasing the hydrogen during the contact formation cycle. Section 5.2 of this chapter first discusses the factors that influence the SiN_x induced defect passivation and the techniques that are used to study this phenomenon. A novel method to determine the concentration and flux of H diffusing into the Si is then introduced followed by the correlation of flux with the lifetime enhancement in defective String Ribbon Si. Section 5.3 discusses further applications of the novel methodology to account for H diffusing through c-Si. Finally, sections 5.4 and 5.5 discuss the high-temperature (800 and 850 °C) and low-temperature (≤ 650 °C) H diffusion from SiN_x.

5.2 Hydrogen diffusion in silicon from PECVD silicon nitride

Hydrogen (H) released during the annealing of hydrogenated amorphous silicon nitride (SiN_x:H) films diffuses through the crystalline silicon underneath and passivates the defects. This section discusses the factors that influence the SiN_x induced defect passivation in Si and the techniques that are used to study the effect. A novel method is introduced to determine the concentration and flux of H diffusing through the Si, which is then correlated with the measured lifetime in defective String Ribbon Si.

5.2.1 Factors that influence SiN_x induced defect passivation in silicon

As discussed in CHAPTER 3, H diffusion in the Si from an amorphous hydrogenated silicon nitride (SiN_x) antireflection coating is critical for the passivation of defects in the low-cost Si materials used in photovoltaics. Figure 5.1 shows the structure of a solar cell made on low-cost Si that has defects such as grain boundaries, dislocations, metals and dangling bonds. The cell structure has a PECVD SiN_x AR coating on front, which contains 10-20% atomic H. When this structure is annealed at high temperature (700-800 °C) to form screen-printed contacts, H is released from SiN_x and passivates the defects in bulk Si underneath. H released from the SiN_x film diffuses into the Si, where it interacts and attaches to the defects (hydrogenation). However, contact firing temperature is high enough that it also dissociates from the defects (dehydrogenation). Thus, defect passivation or H retention at defects is the result of competition between hydrogenation and dehydrogenation during the contact firing. The degree of defect passivation and H retention depends on the following factors:

- Release of H from SiN_x film,
- Diffusion of H in Si, and
- Dehydrogenation from defects.

The above factors can be influenced by the firing temperature, time, and the temperature ramp up and cooldown rates. Growth kinetics of SiN_x also can influence the content and release of H from the SiN_x film.

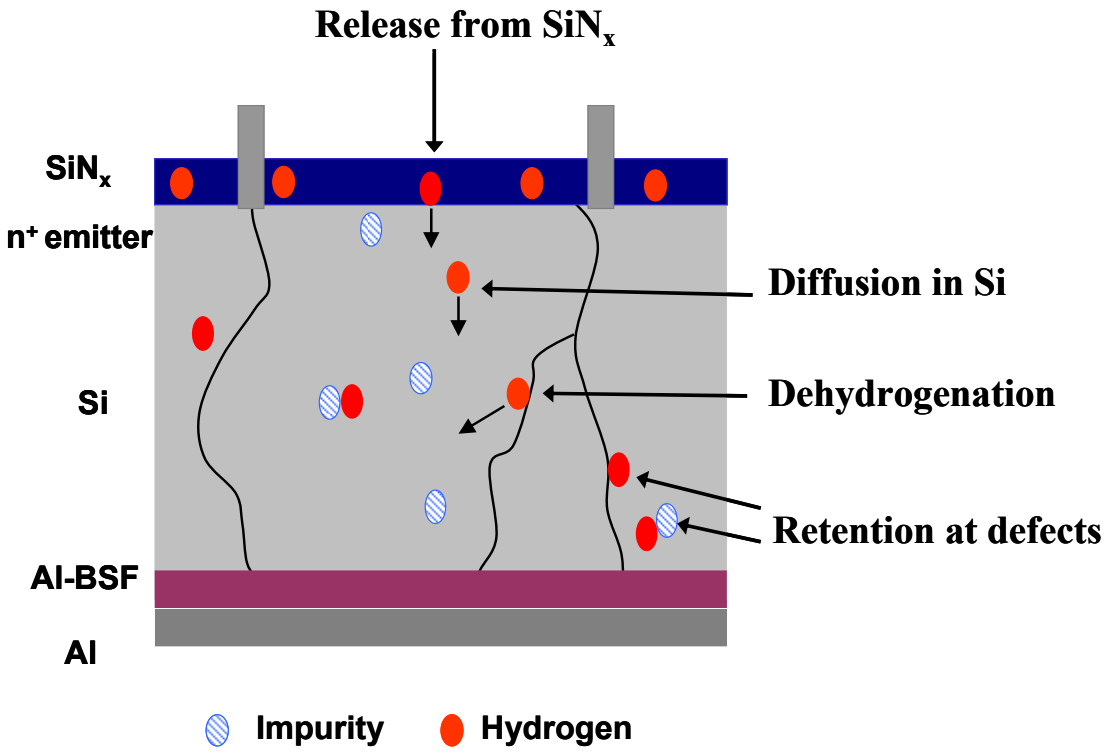


Figure 5.1 Picture of a solar cell made on low-cost, defective Si and the interaction of H released from SiN_x with defects.

5.2.2 Techniques used to study H diffusion and passivation

The H concentration in Si is generally very low and below the detection limit [39, 90, 91] of most tools; therefore, the positive effects of H released from hydrogenated SiN_x (SiN_x:H) film during high-temperature annealing (hydrogenation) have been observed and reported mostly via indirect measurements such as increase in minority carrier lifetime [92] and improved current-voltage and spectral response of solar cells [93, 94]. Several studies have been reported in the literature to optimize the properties of the SiN_x film, which give the best bulk passivation. Dekkers, et al., found an optimum mass density of 2.9 gm/cm^3 for the SiN_x film that provides best bulk defect passivation [89]. Romijn, et al., reported on optimum Si-N bond density, which is related to the mass density, that gives the best bulk and surface passivation [94].

High surface concentrations of deuterium (D) and H, trapped by defects generated on the Si surface during SiN_x deposition, have been reported in literature [95, 96]. However, this concentration falls rapidly below the detection limit of most measurements, as shown in Fig. 5.2 [95].

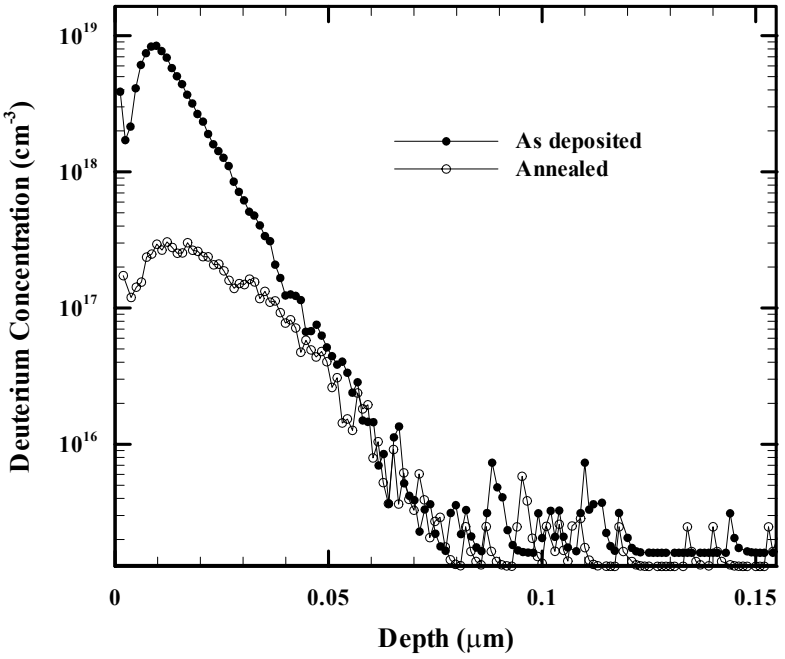


Figure 5.2 Concentration of D measured close to the surface by SIMS, taken from ref. [95].

There have been attempts to detect the presence of H in the bulk Si directly since not long ago it was conjectured that the H lost from the annealed SiN_x:H film was released into the atmosphere and not into the Si [97]. Infrared absorption measurements of Pt-H complexes in Si have recently demonstrated a large diffusion depth of H in Si and have placed a lower limit on the total amount of H diffusing into the crystalline Si samples [39]. FTIR data in Fig. 5.3, taken from ref. [39], shows unambiguously that H released from the SiN_x diffuses into the Si substrate and forms complexes with defects in

bulk Si. A minimum H concentration of ~10^{15} cm^{-3} was established inside the silicon for the best case [91]. However the annealing profile (ramp-up and -down rates), for short anneal times, for the thick (~1500 μm) samples used in their study to improve the measurement detection limit, may be different than the temperature profile used for the contacts in conventional belt furnaces [91]. Also, the presence of heavy Pt traps inside the bulk Si could alter the H diffusion kinetics. SIMS measurements were used by Hahn, et. al. to directly measure the deuterium (D) trapped by oxygen inside the bulk of mc-Si [90].

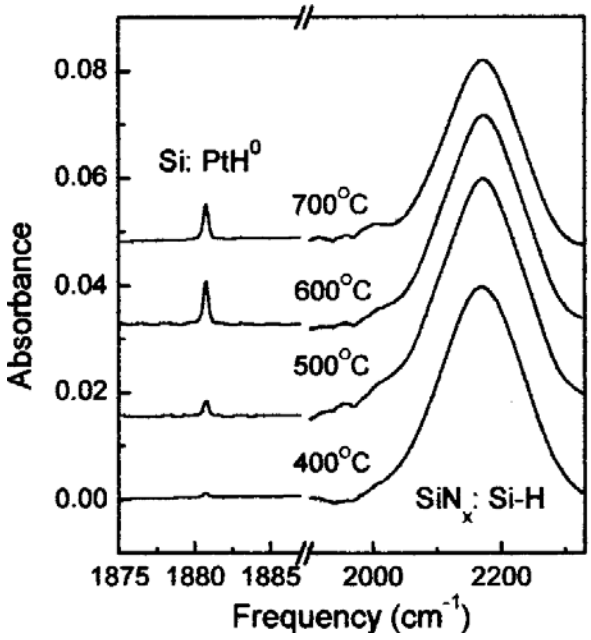


Figure 5.3 IR spectra of vibrational lines assigned to Si–H bonds in the SiN_x layer and to PtH complexes in the Si for an annealed Pt sample with a SiN_x layer deposited on its surface [39].

5.2.3 Development of a novel method to determine the concentration and flux of hydrogen injected in silicon from the PECVD SiN_x film

In this research, a novel structure and process sequence shown in Fig. 5.4 was developed to improve the understanding of the H diffusion kinetics and determine the amount of H that diffuses through the Si during the annealing of the SiN_x film. This experiment involved the deposition of SiN_x:D using deuterated silane (SiD_4) and

deuterated ammonia (ND_3) as precursors in a low-frequency plasma-enhanced chemical vapor deposition (PECVD) reactor at 400 °C. The substrates were 215 µm thick, 0.35 Ω•cm float zone (FZ) wafers. The thickness of the deposited SiN_x:D films was 80 nm, with a refractive index of 2.0 measured at 633 nm. D has a low natural abundance, which lowers the detection limit of H by SIMS measurements. SiN_x:D films are, structurally and physically, slightly different from SiN_x:H films for the same growth conditions [98]. However, these differences can be eliminated [99] by adjusting the process parameters. The passivation ability, mechanism, and kinetics for SiN_x:D films are expected to be similar to that of SiN_x:H films [100]. rf sputtering was then used to deposit 1.5-2.5 µm thick amorphous Si (a-Si) films on the rear side of the wafer in an argon ambient, at a substrate temperature of 200 °C. This sputtered layer was found to be highly defective, which is ideal for trapping high concentrations of deuterium. Samples coated with SiN_x:D on one side and a-Si on the other side were annealed in a Rapid Thermal Processing (RTP) system at 750 °C for 1, 5, 60, and 300 s, with fast ramp-up and ramp-down rates, similar to what is used for contact firing during solar cell fabrication. SIMS measurements of D profiles were performed within the sputtered a-Si films with a Cameca IMS5f using a cesium primary ion beam. Figure 5.4 illustrates the schematic of the structure and the process sequence used in this study.

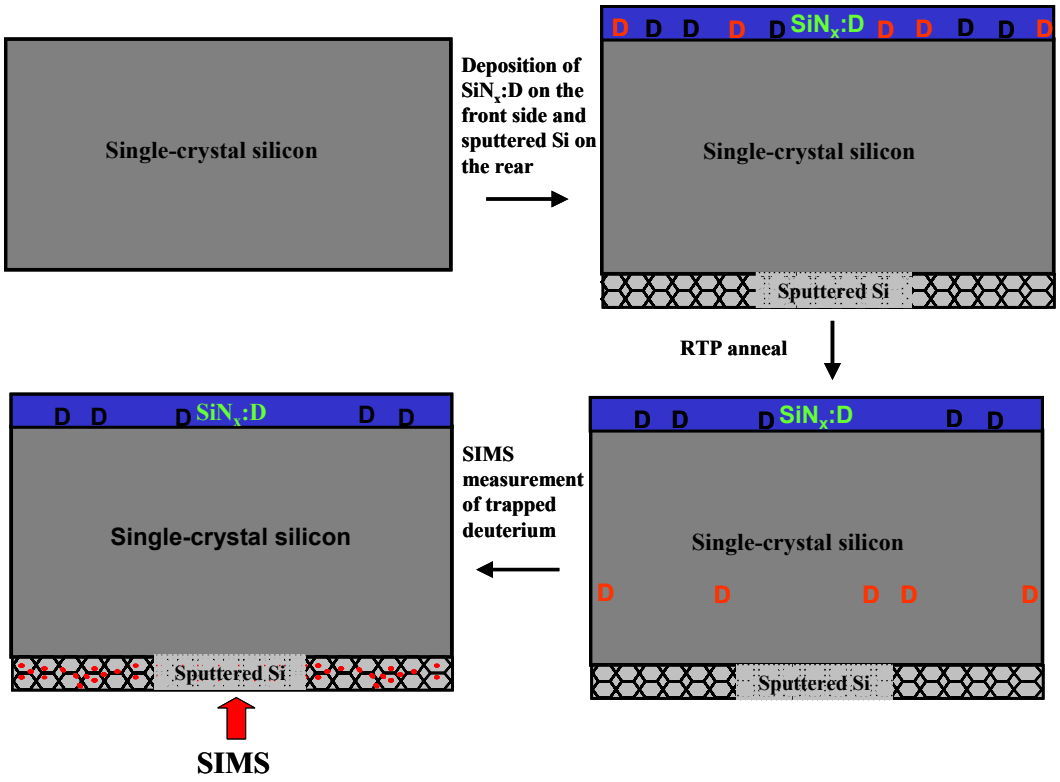


Figure 5.4 Illustration of the structure used to trap deuterium, which is released from the SiN_x:D film on top of Si and traverses through the single-crystal silicon.

5.2.4 Measurement of the concentration and flux of H released from SiN_x film into Si upon annealing

Figure 5.5 shows the measured D concentration profiles in the sputtered Si layer on the rear side of the FZ samples. The peak D concentration in the sputtered Si film for 1, 5, 60, and 300 s anneals was found to be 3.84 x 10^{18}, 4.43 x 10^{18}, 5.23 x 10^{18}, and 7.87 x 10^{18} cm^{-3}, respectively. Figure 5.5 also shows the D content in the sputtered Si layer for a sample that had no SiN_x on the front and was coannealed with the 300 s sample. No D was detected in this sample, which establishes that the source of D detected in sputtered Si is the SiN_x:D film on the front side and that D gets there via diffusion through the c-Si wafer. The concentration of the trapped D increases in the sputtered Si layer as the anneal time increases, but the increase is limited by the supply of D from the SiN_x:D film. The D

concentration inside the sputtered Si layer shows a typical diffusion profile with a tail away from the c-Si/ sputtered Si interface decreasing toward the free surface. This indicates the diffusion of D through the c-Si and into the sputtered Si, rather than diffusion from the ambient. One might suspect that id the D released into the atmosphere could wrap around and diffuse in the sputtered Si from the rear. As expected, in the absence of traps, the D concentration rapidly falls below the detection limit inside the FZ Si. Also, the peak concentration of 7.87 x 10^{18} cm^{-3} for the 300 s sample does not show any sign of saturation, which indicates that the defects in the sputtered Si layer can still hold more D. This implies that the sputtered Si film captures most of the D that passes through the c-Si and the measured D represents the "accumulated" D concentration that went through the c-Si. The D concentration in sputtered Si falls below the detection limit before reaching the free surface, which again indicates a complete capture of all the D traversing the c-Si.

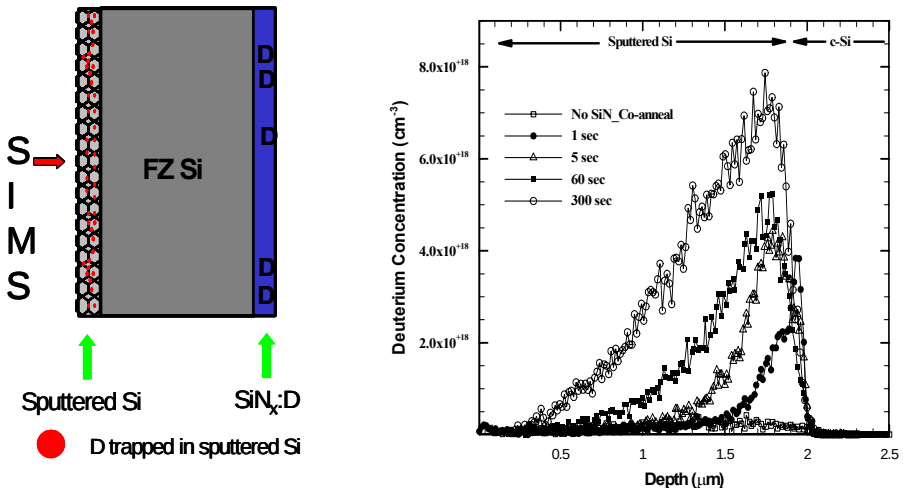


Figure 5.5 Penetrated deuterium concentration in the sputter Si layer on the back of the wafers, released from the front SiN_x:D film, for times of 1, 5, 60 and 300 s at 750 °C in RTP. Also shown is the deuterium concentration for a sample with no SiNx:D film, but co-annealed with the 300 sec sample.

Figure 5.6 shows the average "areal density" of D (integrated area under the concentration curves) in the sputtered Si layers. Notice that the areal density increases, but its slope decreases with the increase in anneal time. This suggests a rapid decrease in the rate of release of D from the SiN_x:D film. This is consistent with some observations in literature, where it has been suggested that the total H content and the Si-H and the N-H bond densities in the SiN_x:H film decrease initially at a higher rate and then slows down for longer anneal times [97, 101]. The fraction of H lost from the SiN_x:H that diffuses into the Si also depends on the density of the SiN_x:H film [101, 102]. Thus, the merit of measuring the penetrated or diffused H through the defect-free Si in this study is that it provides a measure of H that would be available for defect passivation if SiN_x:H film was deposited on top of a defective Si substrate. This is a much more useful quantity than measuring the loss of H from the SiN_x film, which would also involve H escaping from the front surface to the ambient. From the areal density of the trapped D, the average flux (areal density divided by anneal time, in $cm^{-2} \cdot s^{-1}$) of D diffusing through the Si has been estimated and plotted in Fig. 5.6. The average flux values for the shorter anneal times are substantially higher relative to the longer anneal times. It is important to recognize that a higher flux of H during a shorter anneal should enhance defect passivation in Si because if can compete more effectively with the dehydrogenation process. For longer anneal times the average flux of H decreases, which in turn would decrease the ratio of the hydrogenated to the dehydrogenated defects. Therefore, a smaller fraction of defects will be in the passivated state just before the start of the cooldown cycle, resulting in inferior defect passivation even though the total amount of H released from SiN_x:H increases. It is important to recognize that hydrogenation and

dehydrogenation take place at the same time and the dehydrogenation rate is fixed. Therefore, the net hydrogenation will be dictated by the average flux rather than the total amount of H passing through the Si. If dehydrogenation was absent, then defect passivation or lifetime enhancement for longer anneal times would be better. Studies in the literature have indeed shown that low temperature H passivation provided by MIRHP improves the solar cell performance (J_{sc} and LBIC response) as hydrogenation time is increased for temperatures ≤450 °C, since there is little or no dehydrogenation taking place at these lower temperatures. H starts to dissociate from defects or dangling bonds at temperature above 500 °C [103].

If the total amount of D captured in the sputtered Si was trapped uniformly inside the 215 μm thick Si used in this study, the concentration would be at least 4.7 x 10^{15} cm^{-3} for the 1 s anneal and 2.7 x 10^{16} cm^{-3} for the 300 s anneal, which also can be viewed as the defect passivating capacity for these anneal times. These concentration estimates set a lower limit of D diffusing into the Si from SiN_x, at 750 °C.

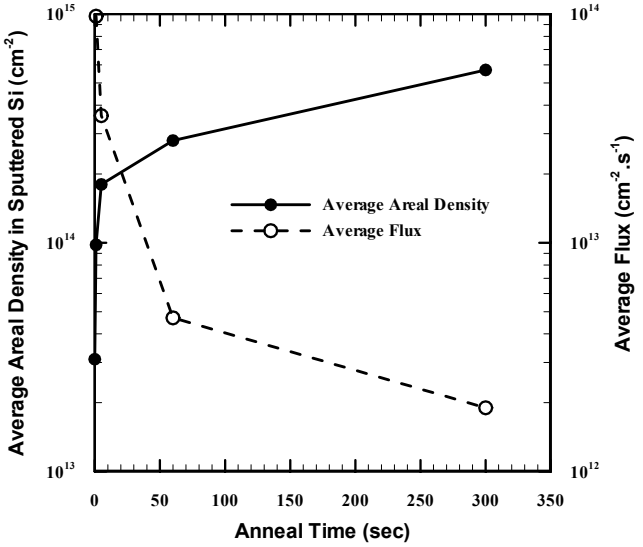


Figure 5.6 Average areal densities of D in the sputter Si film for different anneal times. Average flux of D injected in the Si is also shown.

5.2.5 SiN_x induced lifetime enhancement in String Ribbon silicon via rapid annealing and the correlation of H flux with the lifetime in String Ribbon Si

After establishing the incorporation of H into the Si bulk, the retention of H at the defects was studied, which is equally important for achieving higher lifetime and cell efficiency on defective, low-cost cast mc-Si wafers. Hence, we decided to conduct study on String Ribbon wafers, which are very sensitive to hydrogenation. Samples were first gettered with $POCl_3$ for a time and temperature typically used to form the n^+ emitter during the solar cell fabrication. After etching off the emitter, post gettering lifetime was measured and then an 80 nm thick low-frequency SiN_x:H film was deposited for hydrogenation study. After measuring the post gettering lifetime, samples were divided into two groups: greater and less than 15 μs lifetime. For every annealing condition, one sample from each group was chosen and annealed to see the effect of hydrogenation on the low and the high lifetime sample. Lifetime was measured at four different locations on a wafer; hence the reported lifetime is an average of eight measurements on two different wafers. A faster cooldown is expected to yield a higher lifetime due to trapping or quenching of H at the defects. To study the effect of only the anneal time, the cooldown rate was kept constant. Figure 5.7 shows the bulk lifetime after the gettering and hydrogenation steps. Notice that the highest lifetime is obtained for the shortest anneal time of 1 sec. Lifetime enhancement decreases as anneal time increases and then saturates after about 10 secs. Bulk lifetime was also measured after 1, 5, 60 and 300 secs anneals, with similar cooldown profiles. Figure 5.8 shows the correlation between the measured lifetime and the average D flux (Fig. 5.6) for different anneal times. 1 s firing produced maximum flux and highest lifetime. For longer anneal times, the flux of H

decreases; consequently, H passivation and bulk lifetime are reduced. Thus, higher H flux during shorter anneal enhances defect passivation in String Ribbon Si. Even though the total H passing through the Si is less for shorter annealing times, it is the higher flux that is more important for lifetime enhancement because of the defect dehydrogenation during the annealing cycle.

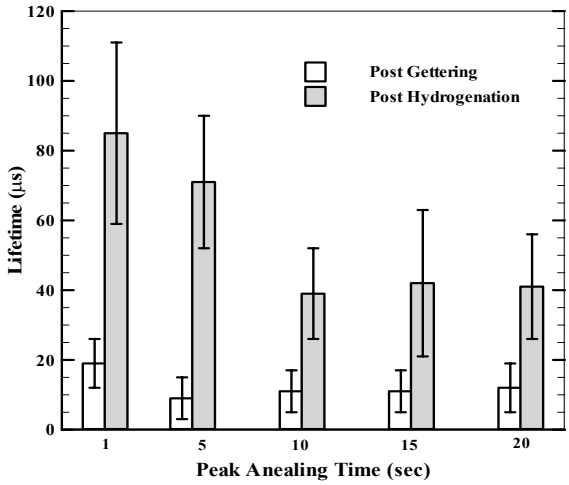


Figure 5.7 Average lifetimes of String ribbon wafers after gettering and hydrogenation for different peak anneal times. Error bars show the standard deviation.

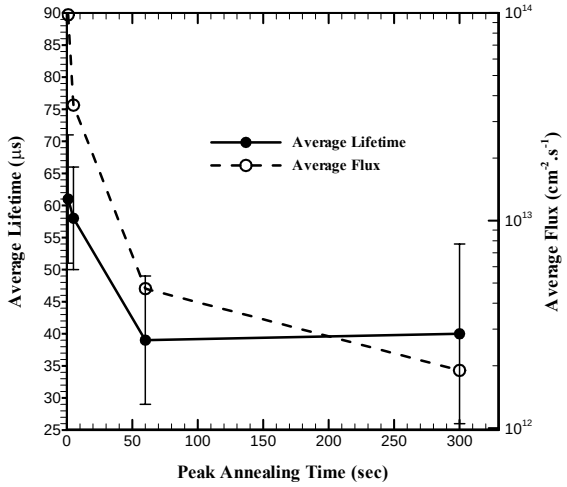


Figure 5.8 Average lifetime and average flux values for peak anneal times of 1, 5, 60 and 300 s. Cooling rates for lower anneal times were adjusted to the cooling rate of the 300 s sample.

5.3 Further applications of the methodology developed

With the methodology developed in the previous section, experiments were performed to see the effect of increasing the thickness of the Si substrate and the presence of a capping layer of SiN_x:H on top of SiN_x:D.

5.3.1 Effect of increasing the thickness of Si

The D concentrations in Fig. 5.5 are for a 215 μm thick defect-free FZ Si substrate. To study the effect of thickness and c-Si substrate, we also measured the penetrated D through a 575 μm thick Czochralski (Cz) Si wafer, which contains oxygen in the bulk and could trap some D [90]. Figure 5.9 shows the D concentration profiles in the sputtered Si layer on the rear side of the 575 μm thick n-type Cz Si wafer after 1 and 60 s anneals at 750 °C.

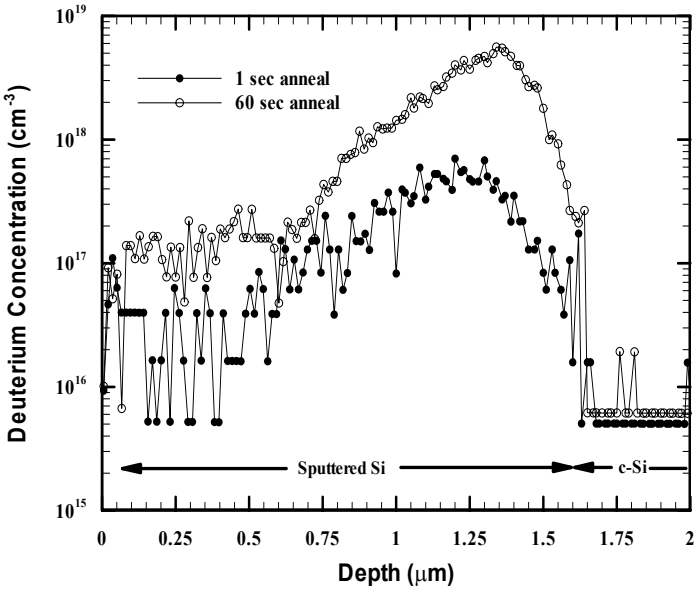


Figure 5.9 Penetrated D concentrations in the sputtered Si layers on the rear side of the wafers, for a 575 μm thick, n-type Cz wafer for anneal times of 1 and 60 s at 750 °C.

The peak D concentrations for 1 s and 60 s anneals were found to be 7 x 10^{17} and 5.6 x 10^{18} cm^{-3}, respectively. Figure 5.9 demonstrates that it only takes a 1 s (peak time anneal) at 750 °C for the D to penetrate through the entire 575 μm thick wafer. Thus, even in the presence of defects such as oxygen in Cz Si and a more than twofold increase in thickness, a considerable amount of D was detected on the rear side after the 1 s anneal. However, it should be noted that the peak anneal time of 1 s is equivalent to a 3.7 s peak time when the ramp-up and ramp-down rates are taken into account [104]. This is consistent with the high diffusivity of H measured by Van Wieringen and Warmolz (VWW) in single-crystal Si [37], emphasizing the fact that hydrogenation in c-Si at high temperatures is not diffusion limited [105].

5.3.2 Effect of a SiN_x:H capping layer on top of SiN_x:D film

Another study was conducted using this methodology to determine the effect of a SiN_x:H capping layer on top of the SiN_x:D layer. A 180 nm of SiN_x:H (deposition temperature 425 °C) was deposited on top of the 80 nm SiN_x:D film (deposition temperature 400 °C) and annealed at 750 °C for 60 sec. It should be recognized that the source of D is still the lower deuterated SiN_x layer. Figure 5.10 shows the deuterium concentration profiles measured in the sputtered a-Si. It is clear from Fig. 5.10 that the presence of the capping layer leads to higher injection of D into the Si, indicating that the cap prevents the escape of H into the ambient such that more D is injected into the Si. The difference between the two curves represents the amount of D that diffused out into the ambient when no cap is present. According to Fig. 5.10, this out-diffusion can be quiet significant.

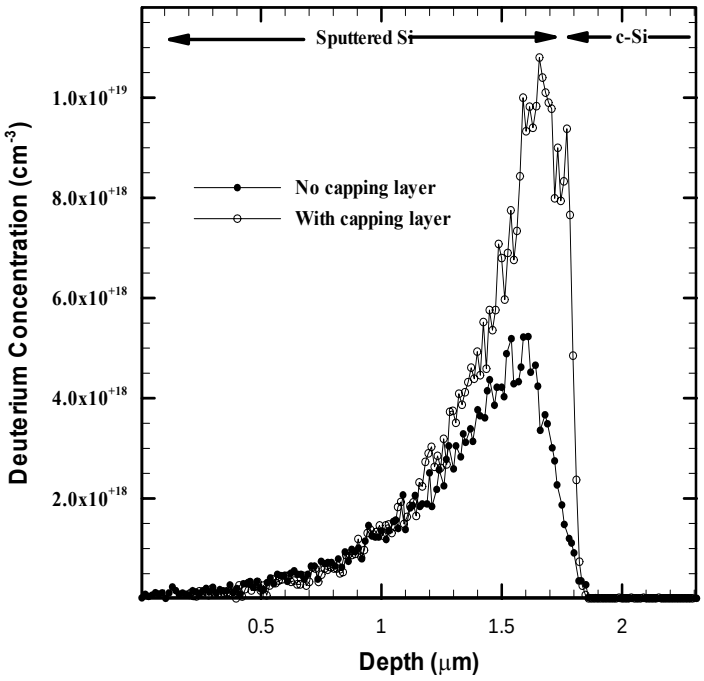


Figure 5.10 Penetrated D concentration in the sputtered Si layer for samples with and without a capping layer of 180 nm SiN_x:H on top of 80 nm SiN_x:D, for anneal at 750 °C for 60 s.

5.4 High temperature (800 and 850 °C) hydrogen diffusion in silicon from PECVD SiN_x film

In the previous sections, SiN_x anneal temperature was fixed at 750 °C. In order to see the impact of higher anneal temperatures, similar structures were prepared and annealed at temperatures of 800 and 850 °C for 1, 5, 60, and 300 s. Similar to the 750 °C anneal experiment, the tapped D concentration in the sputtered Si layer was determined and the instantaneous flux values were obtained from the slope of the areal density versus annealing time curves.

5.4.1 Trapped D concentration profiles for anneal temperature of 800 °C

Figure 5.11 shows the D concentration in the sputtered layers for 800 °C for anneal times of 1, 5, 60, 300, and 600 s. As opposed to the 300 s anneal at 750 °C (Fig. 5.5), D starts to escape from the rear surface for anneal times of 300 s and higher. As

expected, a much higher concentration of D is measured at 800 °C compared to 750 °C. It is interesting to note that the peak concentration for the sample fired for 600 sec decreases. This could be due to the limitation of the front SiN_x to constantly supply D after a long anneal time at high temperature such that the D supplied into the sputtered Si from c-Si is less than the concentration of trapped D diffusing out to the free surface from the sputtered layer. Hence, after long firing time of 600 s at 800 °C, the SiN_x layer is not able to increase or maintain the peak concentration of trapped D in the sputtered layer.

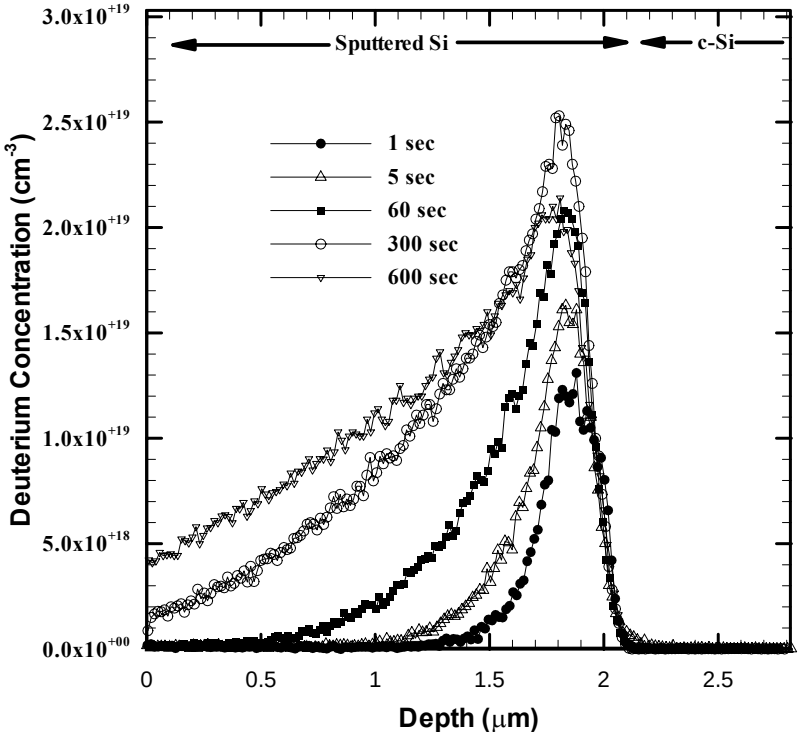


Figure 5.11 Penetrated deuterium concentration in the sputter Si layer on the back of the wafers, released from the front SiN_x:D film, for times of 1, 5, 60, 300, and 600 s at 800 °C in RTP.

5.4.2 Trapped D concentration profiles for anneal temperature of 850 °C

Figure 5.12 shows the D concentration in the sputtered layers for anneal temperature of 850 °C for anneal times of 1, 5, 60, and 300 s.

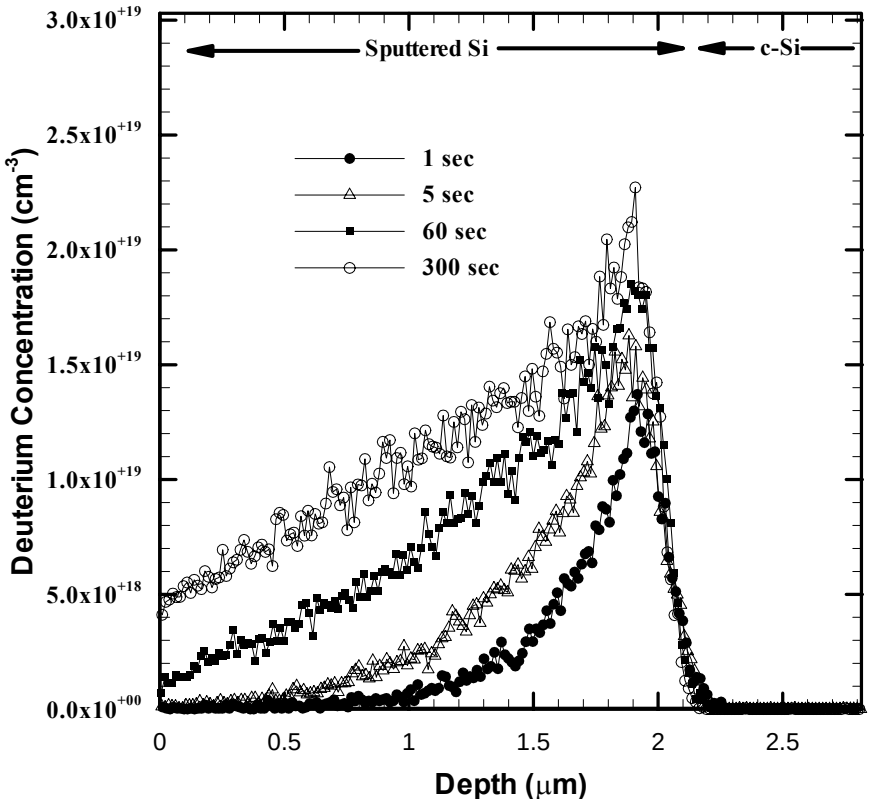


Figure 5.12 Penetrated deuterium concentration in the sputter Si layer on the back of the wafers, released from the front SiN_x:D film, for times of 1, 5, 60, 300 s at 850 °C in RTP.

At 850 °C, D starts to escape from the 2 μm thick sputtered Si layer for anneal times exceeding 60 sec. As expected, a substantially higher amount of D is trapped for anneals at 850 °C. For 1 and 5 s anneal times, the peak concentration values at 850 °C are higher than their counterparts at 800 °C. However, the trend is opposite for anneal times of greater than 60 s. This could be due to the increased diffusivity of D in the sputtered Si layer, consequently, the D concentration profiles spread out and at the same time, the front SiN_x is not able to supply D at the same rate as for the shorter anneal times. This drop in peak concentration for longer anneal times at 850 °C indicates towards a much quicker drop in the rate of supply of D from SiN_x at 850 °C, compared to the 800 °C anneals. This would manifest itself in similar values of flux for 800 and 850 °C for anneal

times of 60 s and higher, which is calculated in the next section. It should however be noted that the total amount of D trapped for 850 °C would still be higher than 800 °C for all anneal times.

5.4.3 Calculation of areal density of D in the sputtered a-Si layer and the corresponding flux of H in Si

To calculate the areal density of D in the sputtered Si for the profiles in which D escapes from the sputtered layers, Gaussian profiles were fitted and extrapolated up to the detection limit of SIMS for D (1e16 cm^{-3}). Figure 5.13 shows, as an example, the extrapolated data fitted and added to the measured data for the 300 s anneal at 800 °C shown in Fig. 5.11. However, it should be noted that the areal density of D calculated from the extrapolated data and the original data are not very different since the extrapolation is in the low D concentration range. Nevertheless, it was performed to get more accurate estimates. Areal density was then calculated by integrating the area under the concentration curves.

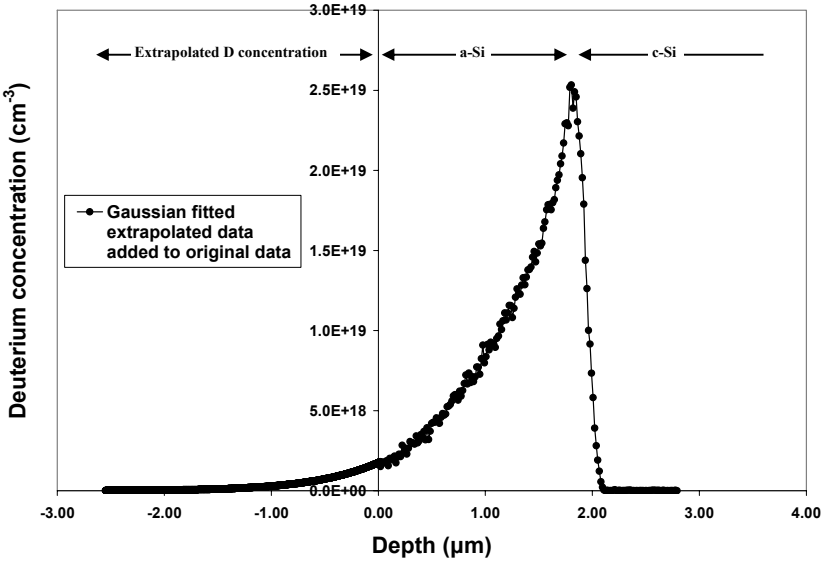


Figure 5.13 Example of the measured D concentration profile fitted with a gaussian function and extrapolated for samples in which D starts to escape from the rear sputtered Si layer.

Areal density of D in the sputtered layer for anneal temperatures of 750, 800, and 850 °C and for times of 1, 5, 60, and 300 s are shown in Fig. 5.14. Trend for higher anneal temperatures is similar to that of 750 °C, with the areal density saturating at higher anneal times. For the same anneal time, areal density increases significantly when temperature is increased from 750 to 800 °C; however, when the temperature is increased from 800 to 850 °C, the relative increase in areal density is less. Depending on the bonding state of the bonded H in the SiN_x, the activation energy for dissociation would be different. As a result, probably on increasing the temperature from 750 °C to 800 °C, more bonded H is made available from the new bonds that are broken. On further increasing the temperature to 850 °C, not as many new bonds are broken.

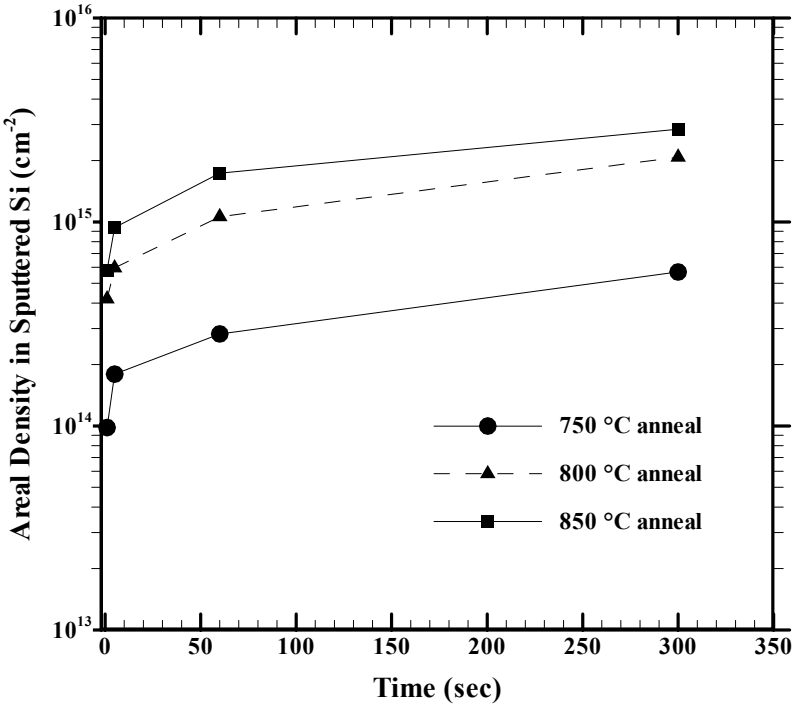


Figure 5.14 Areal density of D in the sputtered Si layer for anneal temperatures of 750, 800, and 850 °C and anneal times of 1, 5, 60, and 300 s.

The calculated flux values in Fig. 5.6 for the 750 °C anneals represent the average flux values obtained by simply dividing the areal densities by the anneal times. To get a better estimate of the change in flux as a function of anneal time, instantaneous flux values were calculated by fitting the areal density values of Fig 5.14 by Weibull function: $y = a - b\exp(-cx^d)$. Appropriate values of coefficients a, b, c, and d were determined from the fit for each curve in Figure 5.14. Figure 5.15 shows, as an example, the curve fitting of the Weibull function to areal density data for the 850 °C anneal in Fig. 5.14.

Instantaneous value of the flux ($\frac{d(areal\_density)}{d(time)}$) at any time was calculated by taking the slope of the Weibull function at that anneal time. Figure 5.16 plots the areal density from Fig. 5.14 along with the flux calculated at anneal times of 1, 5, 60, and 300 s for the anneal temperatures of 750, 800 and 850 °C.

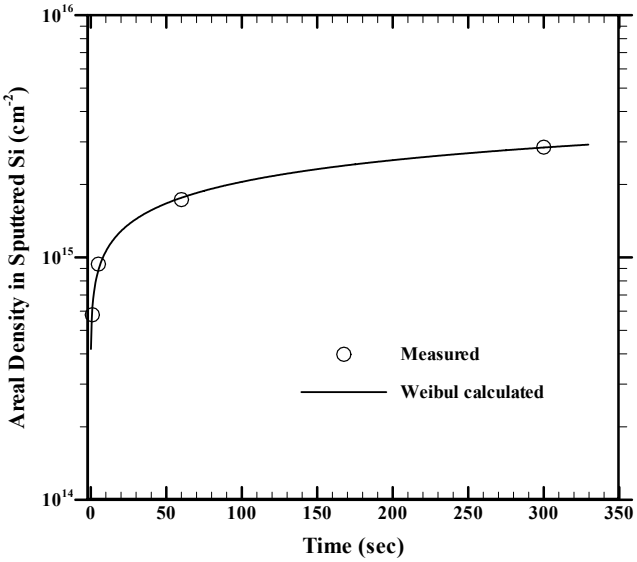


Figure 5.15 Curve fitting of the areal density of D in the sputtered layer for 850 °C anneal by Weibull function.

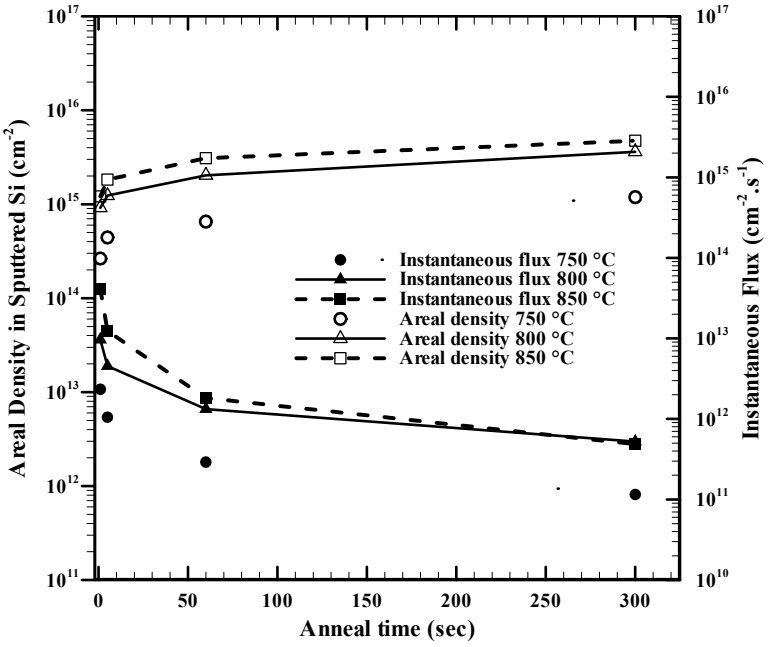


Figure 5.16 Areal density of D in the sputtered Si and the instantaneous flux values as calculated from the slope of Weibull function for temperatures of 750, 800, and 850 °C.

Note that the instantaneous flux values for 750 °C are significantly lower than the corresponding average flux values at 750 °C calculated in Fig. 5.6. This is because average flux values contain contribution from higher flux at previous times. The first noteworthy point from Fig. 5.16 is that the flux values are higher for higher temperature anneal, which should lead to a higher bulk defect passivation. However, due to a higher dehydrogenation rate at higher temperatures, it is the lower temperature that provides a better defect passivation, probably because dehydrogenation rate increases faster than the flux. This will be shown through lifetime measurements on String Ribbon samples in the next subsection. The second noteworthy point from Fig. 5.16 is that for temperatures of 800 and 850 °C and for anneal times greater than 60 s, the flux values are similar, which indicates a much quicker drop in the supply rate of D from SiN_x at 850 °C, as mentioned in section 5.4.2.

5.4.4 Lifetime measurements in String Ribbon to support the competition between the hydrogenation flux and dehydrogenation rate

Figure 5.17 shows the lifetime enhancement from hydrogenation of gettered String Ribbon samples for anneal time of 1 s and for temperatures of 725, 750, 800, and 850 °C. Similar to the lifetime measurements in section 5.2.5, gettered String Ribbon samples were divided into two sets. One set of samples had post gettering lifetime greater than 15 μs, and the other set had lifetime less than 15 μs. Lifetime measurements were performed at four different locations on a wafer.

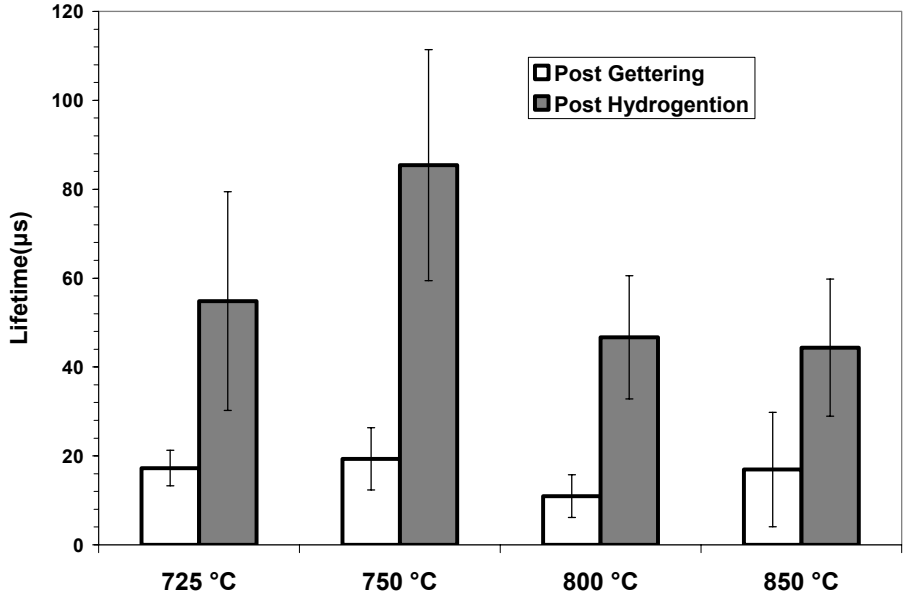


Figure 5.17 Lifetime enhancement in gettered String Ribbon samples annealed in RTP for 1 s at temperatures of 725, 750, 800, and 850 °C.

Although the flux values at higher temperatures increase as shown in Fig. 5.16, however the lifetime enhancement in defective String Ribbon Si is higher for 750 °C. This enhancement is attributed to the faster increase in the dehydrogenation rate at temperatures greater than 750 °C, which dominates the lifetime enhancement of defective Si rather than the increased flux. For a lower temperature of 725 °C, the dehydrogenation

rate is lower, but lifetime enhancement is also lower due to a faster decrease in flux relative to the dehydrogenation rate below 750 °C. Hence Fig. 5.17 shows that there is a competition between the dehydrogenation rate and the flux of H in Si, which dictates the lifetime enhancement. Temperatures in the vicinity of 750 °C seem to provide the best defect passivation for String Ribbon. The optimum temperature may be different for different materials depending on the nature of defects in the material. It should also be noted that for any given temperature, the shortest anneal time, which leads to the highest flux, should yield the best passivation or highest lifetime, since the dehydrogenation rate is fixed for a given temperature.

5.5 Low temperature (≤ 650 °C) hydrogen diffusion in silicon from PECVD SiN_x

The deposition temperature of the SiN_x:D films in this experiment was 400 °C. Hence, for anneal temperatures above 400 °C, H is expected to be released from the SiN_x. To ascertain the lowest temperature at which D starts to diffuse *through* the Si, the structure in Fig. 5.4 was subjected to low temperature anneals for 600 sec. Figure 5.18 shows the D concentration in sputtered layer for temperatures of 500, 525, 550, 600, and 650 °C for anneal time of 600 s. Fig. 5.18 clearly shows that for temperature as low as 525 °C, D diffuses through the 215 μm thick FZ Si. The amount of D diffusing through increases sharply as the temperature is increased above 525 °C. This is because more bonded D is released from the SiN_x at higher temperatures.

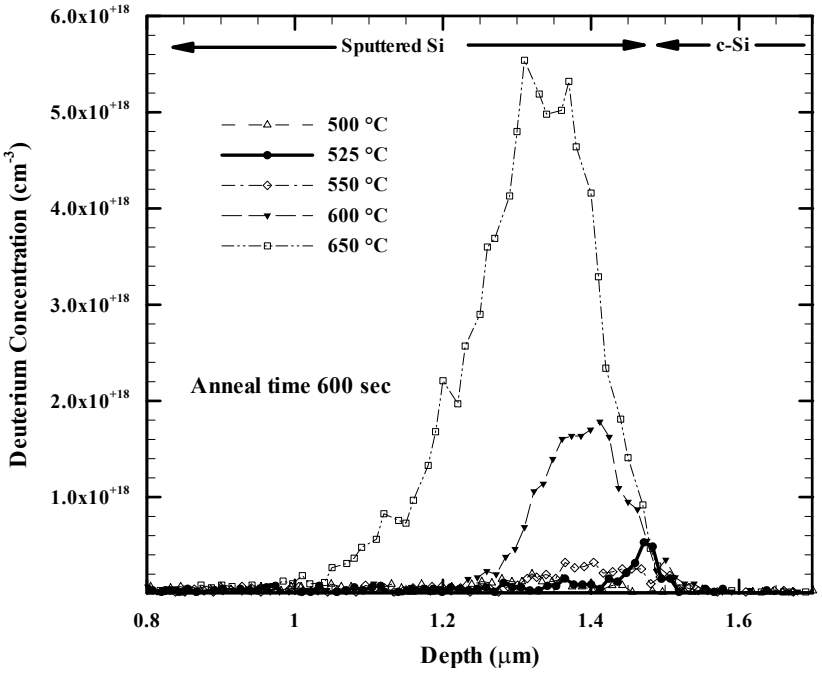


Figure 5.18 Penetrated deuterium concentrations in the sputtered Si layer on the back of the FZ wafers for samples fired at lower temperatures for 600 s.

5.6 Conclusions

This study shows that the stable H isotope deuterium (D), which is released during the annealing of deuterated amorphous silicon nitride (SiN_x:D) films, diffuses through the crystalline silicon and is subsequently captured by a thin, highly defective amorphous layer of silicon (a-Si) sputtered on the rear surface. The single-crystal Si wafers are highly transparent to D diffusion. Therefore, a significant amount of the released D is captured by the sputtered Si layer on the rear side of the sample. This chapter reports on the measurement of the concentration of "penetrated" deuterium (hydrogen), by secondary ion mass spectrometry (SIMS) to monitor the flux of D diffusing through a defect-free single-crystalline silicon wafer. The minimum concentration of D injected into the Si has been estimated to be 4.7×10^{15} cm^{-3} for a short anneal time of 1 s at 750 °C. The penetrated D content in the trapping layer increases

with the anneal time. However, the flux of D injected into the silicon from the SiN_x layer decreases as anneal time increases. The flux values for various anneal times were correlated with the lifetime enhancement of defective String ribbon Si wafers. It was found that a higher flux for shorter anneal times leads to an enhanced defect passivation in low-cost Si. It is the higher flux of H during the short RTP anneal that is crucial for enhanced hydrogenation of the defects in Si, which leads to a greater net association with the defects in the c-Si bulk, prior to cooldown, because of the constant dehydrogenation taking place from the defects at high temperatures.

At an anneal temperature of 750 °C, D was found to penetrate through a 575 μm thick wafer in as little as 1 second peak anneal time in a rapid thermal processing (RTP) system. The presence of a capping layer of SiN_x:H on top of the SiN_x:D was found to inject more D inside the Si, which would otherwise be lost to the ambient.

Measurements of penetrated D concentrations at higher anneal temperatures of 800 and 850 °C showed a much higher amount of D diffusing through the c-Si compared to 750 °C anneals. For similar anneal times, the increase in areal density is much lower as anneal temperature is increased from 800 to 850 °C, which indicates the rapid decrease in D content of the films when fired at high temperature. For similar anneal times, the flux of D for temperatures of 800 and 850 °C is much higher compared to the flux values at 750 °C, however the lifetime enhancement in defective String Ribbon Si is higher for 750 °C. This is attributed to the increase in the dehydrogenation rate at higher temperatures, which dominated the lifetime of defective Si rather than the increased flux.

Study of D diffusion at low temperatures showed that for the SiN_x films deposited at 400 °C, D starts to diffuse through the 215 μm thick FZ Si at temperatures as low as

525 °C, when annealed for 600 s. The amount of D diffusing through the c-Si increases sharply as temperature is increased further from 525 °C.

Hence, this study helps to quantify the amount of D that is injected into the Si from the SiN_x:D film during the firing of screen-printed contacts for solar cells. The concentration and flux of H diffusing through thick c-Si samples was determined which was correlated with the lifetime enhancement of defective String Ribbon Si samples.

CHAPTER 6

FABRICATION OF HIGH-EFFICIENCY SOLAR CELLS ON CAST MULTICRYSTALLINE SILICON AND DEVICE MODELING TO ESTABLSH GUIDELINES FOR ACHIEVING HIGH-EFFICIENCY SOLAR CELLS

6.1 Introduction

This chapter focuses on the fabrication and characterization of high-efficiency, planar solar cells on HEM mc-Si wafers. Section 6.2 reviews laboratory and industrial solar cell efficiencies on mc-Si wafers reported in the literature. Section 6.3 first discusses the fabrication and characterization of high-efficiency cells on HEM mc-Si wafers, followed by the fabrication and analysis of solar cells on HEM mc-Si with low- medium- and high- as-grown lifetime. Section 6.3 also presents the development of high-efficiency solar cells with high-sheet-resistance emitters. PC1D device modeling is used in section 6.4 to establish guidelines for achieving high-efficiency (>20%) solar cells on low-lifetime (100 μs) thin (140 μm) Si material.

6.2 Review of solar cell efficiencies on cast multicrystalline Si

Due to the high cost of Si material (~60%) in a PV module, the use of lower cost cast mc-Si and ribbon Si materials has increased steadily. These materials have defects which tend to lower the performance compared to the single crystal FZ and Cz Si. In spite of the challenges associated with texturing, inhomogenity, low as-grown lifetime, and thermal degradation effects [106], mc-Si solar cell efficiencies and fabrication technologies have advanced over the years, both on laboratory and industrial scale. This

section reviews the efficiency progress of the laboratory and industrial scale mc-Si solar cells.

6.2.1 Progress of laboratory scale mc-Si solar cells

Laboratory scale (1-4 cm^2 area) mc-Si cell efficiencies have benefited from the understanding and research on single-crystal Si solar cells as well as the development of novel processes suitable for mc-Si wafers.

Since the first patent on casting of mc-Si by Wacker [107] and the demonstration of *14%* (AM 1, 4 cm^2 area) efficiency about *three decades ago* [108], there has been significant progress in efficiency of mc-Si solar cells. Even though laboratory scale solar cells typically involve expensive process steps, they are highly instrumental in establishing the potential of low-cost materials and technology.

17.3% efficient (corrected from original 17.8%), 4 cm^2, passivated emitter solar cell (PESC) on cast polycrystalline Si was announced by UNSW *in 1990* [109]. This included a phosphorous pretreatment and rear aluminum treatment into the PESC fabrication sequence.

18.2 and 18.6% efficient 1 cm^2 planar 0.65 Ω·cm, cast mc-Si solar cells were reported by Georgia Tech *in 1996* using a relatively simple process, without the use of surface texturing, point contacts or selective emitters [110, 111]. This involved a 900 °C phosphorous diffusion for 30 minutes, followed by a second high temperature step to passivate the front surface by oxide. Al-BSF was formed and defect hydrogenation was achieved by FGA anneal. Front contacts were formed by photolithography, followed by the deposition of a double layer AR coating.

19.8% efficient 1 cm^2 mc-Si solar cells were reported by the UNSW *in 1998* [112]. This was achieved by using the PERL process sequence [67] on 260 μm thick 1.5 Ω·cm mc-Si wafer. Honeycomb surface texturing was performed using photolithography.

18.2% efficient solar cells on 0.5 Ω·cm Eurosil mc-Si substrates were reported by the Australian National University (ANU) *in 1997* [113]. The contact area of the rear Al metal underneath and oxide layer was varied to obtain a high V_{oc} of 654 mV with a DLAR coating on the front. *In 2000* ANU also reported *16.1% efficiency* on mc-Si substrate using the simplified PERC structure with both surfaces passivated by SiN_x [114]. Again, a high V_{oc} of 655 mV was reported on 0.2 Ω·cm, 200 μm thick mc-Si substrates. Small area (4 cm^2) solar cells with front and rear surface passivation by SiN_x were also reported by ISFH in Germany, with an efficiency of *18.1%*, using photolithography-free process sequence *in 2002* [115]. The front and rear contacts were evaporated using a shadow mask and LBSF was formed on the rear. A 300 μm thick, 1.0 Ω·cm BAYSIX mc-Si was used as substrate.

20.3% efficient 1 cm^2, 99 μm thick, 0.6 Ω·cm cast mc-Si solar cells were reported by Fraunhofer ISE *in 2004*. These represent the highest efficiency mc-Si cells to date [68]. Surface passivation was achieved at low temperature by wet oxidation. Process details and structure of this cell have been discussed in CHAPTER 3. Table 6.1 summarizes the efficiency progress of the high-efficiency laboratory-scale mc-Si solar cells discussed above.

Table 6.1 Progress of laboratory-scale mc-Si solar cells.

Year	Efficiency (%)	Reported by	Comments	Reference
1977	14	Fischer	AM 1 measurement	[108]
1990	17.3	UNSW	PESC	[109]
1996	18.6	Georgia Tech.	Al-BSF, FGA, Front contact by photolithography, DLAR	[111]
1997	18.2	ANU	Low Al metal contact underneath rear oxide	[113]
1998	19.8	UNSW	PERL cell, honeycomb texturing	[112]
2000	16.1	ANU	PERC, both surface passivated by SiN_x	[114]
2002	18.1	ISFH	Contacts evaporated with shadow mask, Local BSF	[115]
2004	20.3	Fraunhofer ISE	Wet oxidation for surface passivation, LFC	[68]

Several costly steps were incorporated to fabricate most of the above laboratory scale devices, which renders them cost-ineffective. However, they provide guidelines to fabricate large area, cost-effective, and manufacturable solar cells. Next sub-section discusses the progress in large area (>100 cm^2) industrial type solar cells.

6.2.2 Progress of industrial mc-Si solar cells

Apart from being larger in size (>100 cm^2), industrial solar cells should be cost-effective, scalable, reproducible, and less sensitive to variations in process parameters. These restrictions tend to lower the efficiency of these cells compared to the laboratory scale solar cells. Industrial mc-Si cell efficiencies have also shown steady progress starting from the *10.0% (AM 1, 121 cm^2) in 1977* [108].

15.1% efficient 225 cm^2 bifacial mc-Si solar cells were fabricated at Kyocera Corporation *in 1990* [116]. The cast mc-Si substrate was 300 μm thick with a resistivity 1.5 Ω·cm. The efficiency of the same structure was improved to *16.4% in 1993* by making further improvements to the front surface structure of the solar cell [117].

16.3% efficient 42 cm^2, 1.4 Ω·cm, 300 μm thick HEM mc-Si solar cells were fabricated at Sandia National Laboratories *in 1994*, which resulted in the world's first 15% efficient mc-Si modules [118]. Apart from surface texturing and Al-BSF, the front contacts were defined using photolithography and front surface had a double layer AR coating.

17.1% efficient 270 μm thick cast mc-Si cells were fabricated by Kyocera Corp. *in 1997* [119]. Reactive ion etching (RIE) was used to texture these mc-Si solar cells in order to reduce the surface reflectance. The area of these cells was 225 cm^2. Screen-printed Al formed the rear contact and Al-BSF. Front contacts were defined by photolithography, followed by Cu plating.

16.8% efficient cast mc-Si solar cells were fabricated by Mitsubishi Electric Corporation *in 2000* [120]. Texturing was applied using Na_2CO_3. Screen-printed metal contacts were fired through SiN_x AR coating in a belt furnace. 16% efficiency was achieved for 225 cm^2 cells. In the same year, Noel, et al., demonstrated *16.7% efficient* cells on polix mc-Si using lithography defined evaporated contacts [121].

16.7% efficient thin (200 μm) cast mc-Si solar cells (100 cm^2) were fabricated at IMEC *in 2004* [64]. Each process step was optimized for thin cells. Double layer (SiN_x/MgF_2) AR coating were applied and the contacts were screen-printed.

17.7% efficient solar cells were fabricated in 2004 by Kyocera corp. on 225 cm^2 cast mc-Si wafers *in 2004* [122]. The wafers were 280 μm thick with a resistivity of 1.5 Ω·cm. Front surface was reactive ion etching (RIE) textured with an emitter sheet resistivity of 90 Ω/sq with screen-printed contacts fired in belt furnace.

17% efficient cast mc-Si solar cells were reported by ECN *in 2005* [123]. An in-line fabrication sequence was used on 156 cm^2 wafers with a resistivity of 1.5 Ω·cm. Earlier *in 2004, 16.5% efficient* cells were achieved by the ECN inline process on a 156 cm^2 cast mc-Si wafers [124].

18.1% efficient buried contact cells were fabricated by University of Konstanz (UKN) *in 2006* [125]. Wafers were 138 cm^2 cast mc-Si. Mechanical V-texturing and electroless plating of Ni and Cu was used. Earlier *in 2003, 17.6%* 156 cm^2 cast mc-Si cells with buried front contacts were reported by UKN [126].

18.5% efficient cells on 233 cm^2 cast mc-Si were announced by Kyocera Corp. *in 2006* [127]. These cells were RIE textured with a shallow emitter and were an improvement over their previous cell efficiencies of *14.5% in 1989, 17.1% in 1996, and 17.7% in 2004* as discussed above.

18% efficient mc-Si cell was announced by Mitsubishi Electric Corp. *in 2007* [128]. These cells were made on 233 cm^2 cast mc-Si wafers which were RIE textured with new metal electrode material and reduced shading loss from front metal. Table 6.2 summarizes the efficiency progress of the high-efficiency industry-scale mc-Si solar cells discussed above.

Thus, the 20.3% efficient mc-Si cells by Fraunhofer ISE represent the highest reported efficiency on mc-Si [68]. The 18.5% efficiency by Kyocera Corp. [127] and 18% efficiency by Mitsubishi Electric Corp. [128] represent the two most significant developements on large area mc-Si.

The results of the cells summarized above are the best efficiencies on mc-Si wafers from different source, vendors, feedstock, and the casting method. The quality of

mc-Si wafers varies significantly depending on several factors such as the cleanliness of the casting crucible, feedstock, and location of the wafer in the ingot. The next sections discuss the solar cells fabricated in this study, on HEM mc-Si with varying as-grown quality, along with the fabrication of high-efficiency planar mc-Si solar cells with single layer AR coating and screen-printed contacts.

Table 6.2 Progress of industry-scale mc-Si solar cells.

Year	Efficiency	Reported by	Area (cm^2)	Comments	Reference
1977	10	Fischer	121	AM 1 measurement	[108]
1990	15.1	Kyocera	225	300 μm thick, 1.5 Ω•cm	[116]
1993	16.4	Kyocera	225	Improved front surface structure	[117]
1994	16.3	Sandia National Lab.	42	First 15% efficient module	[118]
1997	17.1	Kyocera	225	RIE texturing, Photolithography front contacts with Cu plating	[119]
2000	16.8	Mitsubishi	225	Na_2CO_3, SP contacts fired through SiN_x AR coating in a belt furnace	[120]
2004	16.7	IMEC	100	200 μm thickness, DLAR, SP contacts	[64]
2004	17.7	Kyocera	225	RIE texturing, 90 Ω/sq emitter, SP contacts	[122]
2005	17	ECN	156	Inline process	[123]
2006	18.1	Univ. of Konstanz	138	Buried contact, mechanical V-texturing, Electroless plating of Ni and Cu	[125]
2006	18.5	Kyocera	233	RIE textured, shallow emitter	[127]
2007	18	Mitsubishi	233	RIE textured, new metal electrode material	[128]

6.3 Fabrication of high-efficiency screen-printed solar cells on HEM cast mc-Si

The mc-Si and ribbon Si currently account for roughly ~60% of the PV market. These growth technologies provide silicon substrate at a lower cost. However, these materials suffer from a high density of defects, dislocations, grain boundaries, metallic impurities, and other macro defects compared to their single-crystal counterparts, like Czochralski (Cz) or Float Zone (FZ) silicon. This is mainly due to the higher impurity content of the silicon feedstock and a high growth/solidification rate, which furthermore prevents the segregation of impurities in the melt. As a result, the minority carrier lifetime in a cast mc-Si ingot is found to be as low as 3-4 μs from certain regions to as high as 60-70 μs. To obtain the high efficiency solar cells with high yield from wafers with such a wide variation in lifetime, it is important to develop a process sequence that can raise the bulk lifetime to a level where it has little effect on cell efficiency.

The progress in mc-Si solar cell efficiency has been was discussed in section 6.2. Efficiencies as high as 16.6% have been reported on 156 cm^2 cast mc-Si material using a screen-printed, single-layer SiN_x AR coating, isotropic texturing and a selective emitter [129]. This section reports on 4 cm^2, 16.9% efficient HEM mc-Si solar cells. The contacts were screen-printed, belt co-fired with a single-layer SiN_x AR coating. These results were confirmed by National Renewable Energy Laboratory (NREL). These cells do not have any texturing or selective emitter and represent the highest reported screen-printed cell efficiency for this cell design. The 1-2 Ω·cm, ~300 μm thick HEM wafers used in this study were provided by GT Solar.

The results of this section show that for a simple n^+-p-p^+ cell design, the screen-printed efficiency of the cast mc-Si cell became comparable to the untextured FZ-Si cells, because of a significant enhancement in bulk lifetime during processing. Equally

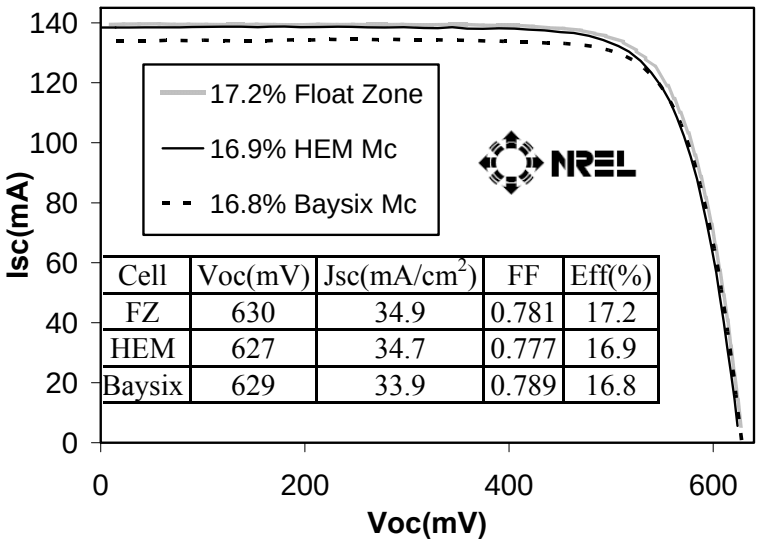
significant is the finding that the cell efficiency is relatively insensitive to the as-grown lifetime due to effective defect gettering and passivation. This is because once the lifetime exceeds 100 μs for this cell design then the efficiency no longer shows a strong dependence on the bulk lifetime. Performance becomes limited by the cell design, such as emitter and BSF profiles. A combination of gettering and hydrogenation steps used in this study was able to push even the low lifetime wafers above the threshold lifetime, resulting in comparable cell performance. Model calculations were performed using PC1D [130] to establish the threshold lifetime for this cell design, followed by the development of a process to achieve the lifetime in finished cells with efficiencies approaching 17%.

6.3.1 Fabrication and characterization of high-efficiency solar cells on HEM mc-Si

The average as-grown bulk lifetimes for the HEM mc-Si, Baysix mc-Si and FZ-Si wafers used in this study were ~23 μs, ~42 μs, and >200 μs, respectively. Bulk resistivity of all the wafers was in the range of 1-2 Ω·cm. For the mc-Si cells, V_{oc} values as high as 629 mV were achieved in conjunction with J_{sc} of ~34 mA/cm^2 and a fill factor in the range of 0.78-0.79. FZ Si cells gave a V_{oc} of ~630 mV and J_{sc} of ~35 mA/cm^2. In addition low series resistance (0.6-0.7 Ω·cm^2) and high shunt resistance values were achieved. Figure 6.1 shows the IV curves and the cell parameters for the best cells made on these three materials.

Nine 2 cm × 2 cm cells fabricated on 10 cm × 10 cm mc-Si wafers gave fairly uniform results across the wafer. Figure 6.2 shows one of the best efficiency distributions for the nine cells on a Baysix mc-Si wafer with an average efficiency of 16.7% and standard deviation of 0.1%. The average fill factor was 0.789 for these nine cells. This is

attributed to uniform printing and firing of the contacts. The average efficiency for the nine cells on a HEM wafer was 16.5%, with the best cell efficiency of 16.9%. It should be noted that 4 cm^2 mc-Si cells generally include several grains and thus the high efficiencies attained are partly attributed to effective defect passivation.



Cell	Voc(mV)	Jsc(mA/cm^2)	FF	Eff(%)
FZ	630	34.9	0.781	17.2
HEM	627	34.7	0.777	16.9
Baysix	629	33.9	0.789	16.8

Figure 6.1 Lighted IV curves and other IV parameters for the mono-Si FZ, HEM, and Baysix mc-Si solar cells, confirmed by NREL.

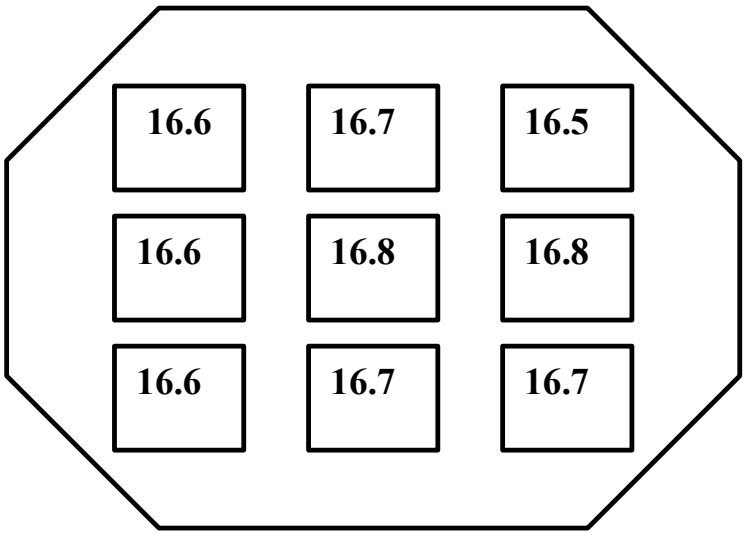


Figure 6.2 Distribution of the nine 4 cm^2 cells on a 10 cm x 10 cm Baysix mc-Si wafer.

In addition, similar results were obtained on these materials in many different runs. Figure 6.3 summarizes the efficiency distribution of 134 mc-Si cells fabricated in multiple runs.

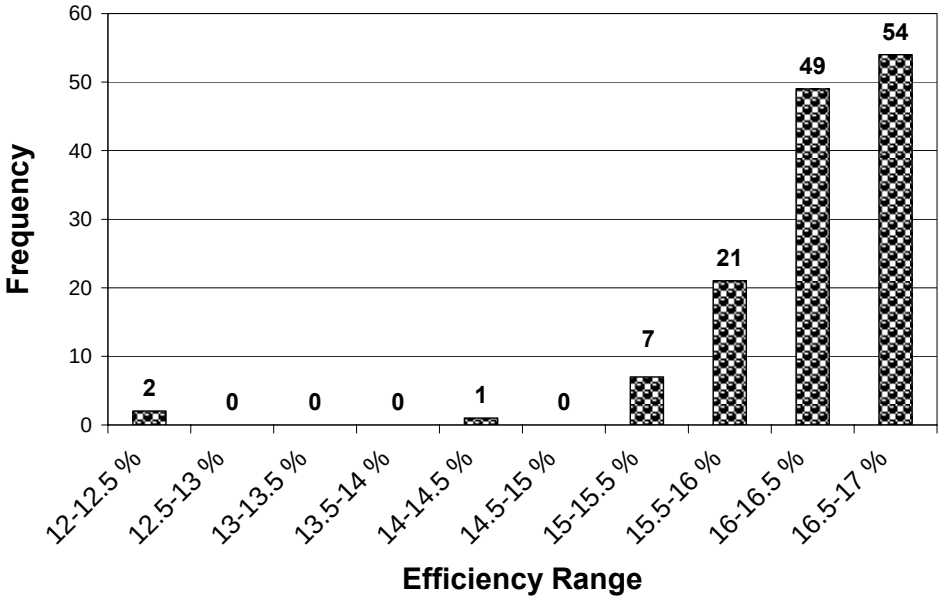


Figure 6.3 Efficiency distribution of 134 cells on mc-Si in multiple runs.

Spectral response and reflectance measurements were performed on these cells to determine the Internal Quantum Efficiency (IQE). The beam diameter for the spectral response measurement was only a few millimeters. Therefore, the spectral response was measured at four different spots on each 4 cm^2 solar cell. Figure 6.4 shows the best IQE response achieved on the highest efficiency FZ, HEM, and Baysix cells. The average weighted reflectance was found to be 11.21 %, 12.11%, and 11.43% for the FZ, HEM and Baysix cells, respectively. Figure 6.4 reveals that the HEM cell has an IQE response comparable to the FZ cell in the short wavelength range, whereas in the long wavelength, FZ shows a slightly superior performance. This is attributed to better or uniform BSF quality on single-crystal cells. This was further supported by the effective Back Surface

Recombination Velocity (BSRV) values of 350 cm/s for the FZ and 600, 800 cm/s for the HEM and Baysix mc-Si cells. These values were extracted by matching the long wavelength IQE response of the cells in PC1D using the average measured lifetime and the best IQE.

Light Beam Induced Current (LBIC) maps for the FZ and HEM cells are shown in Fig. 6.5 (a) and (b). Both wafers showed a fairly uniform distribution of high diffusion length regions over most of the cell area. The average LBIC response (amps/watt) for the FZ wafer was 0.546 amps/watt, compared to a 0.542 amps/watt for the HEM cell, supporting the comparable overall cell performance achieved for the HEM and un-textured FZ Si cells.

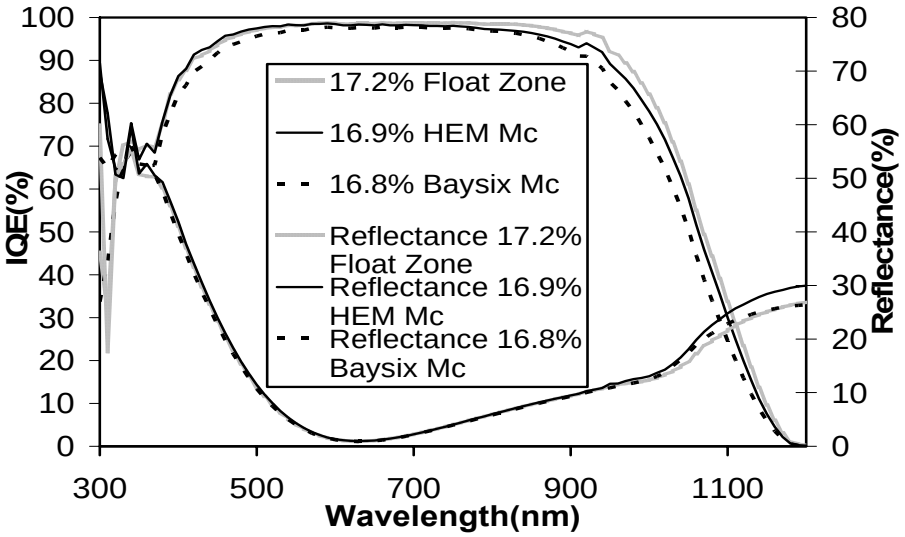


Figure 6.4 Internal Quantum Efficiency (IQE) and their reflectance curves for the FZ, HEM, and Baysix Si solar cells as a function of wavelength.

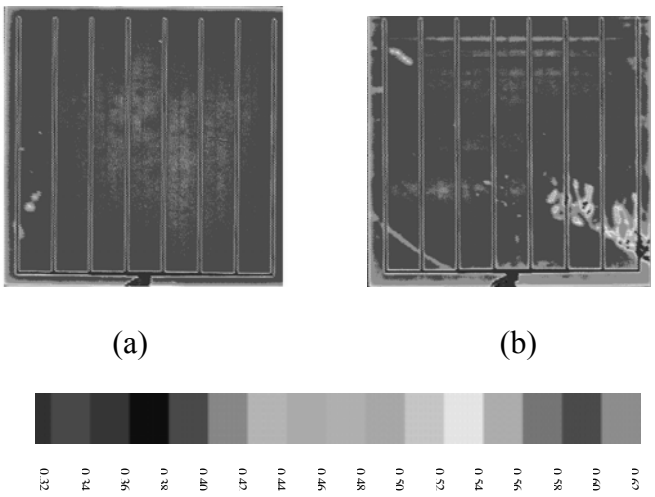


Figure 6.5 Light Beam Induced Current (LBIC) maps for (a) 17.2% FZ (average response: 0.546 A/W) and (b) 16.9% HEM (average response: 0.542 A/W).

6.3.2 High-efficiency screen-printed solar cells fabricated on cast mc-Si with low, medium and high as-grown lifetime

The high performance of FZ, HEM, and Baysix Si cells indicate that high-quality BSF, good ohmic contacts, effective $POCl_3$ gettering, and defect passivation via SiN_x-induced hydrogenation were achieved in mc-Si during the belt co-firing of the samples. Since the starting lifetime in all the three cells discussed above was ≥ 23 μs, we also investigated mc-Si wafers with an as-grown lifetime in the range of 4-70 μs, using the same optimized fabrication sequence. The relative position of these wafers in the ingot was not known. Solar cells were fabricated on three sets of low (~4 μs), medium (~40 μs), and high (~70 μs) lifetime wafers. Figure 6.6 shows the average starting wafer lifetime, average lifetime in the finished cells, and the *average* cell efficiencies obtained from the nine 4 cm^2 cells on each 10 cm × 10 cm wafer (one such set). It is noteworthy that a very small difference in the cell performance (16.6% to 16.8%) was observed in spite of a wide variation in the as-grown lifetime (4 to 68 μs). It has been shown that the low

lifetime could be the result of impurities or impurity decorated dislocation. However, if the dislocation density is below a certain level (10^4 cm^{-2}) then the impurities can be gettered and defects can be passivated [28]. If the low lifetime is due to high dislocation density > 10^6 cm^{-2}, which can be the case in the wafers from the bottom or the top region of mc-Si ingots because of rapid cooling, then the gettering and passivation of the defects in those regions is not as effective [27].

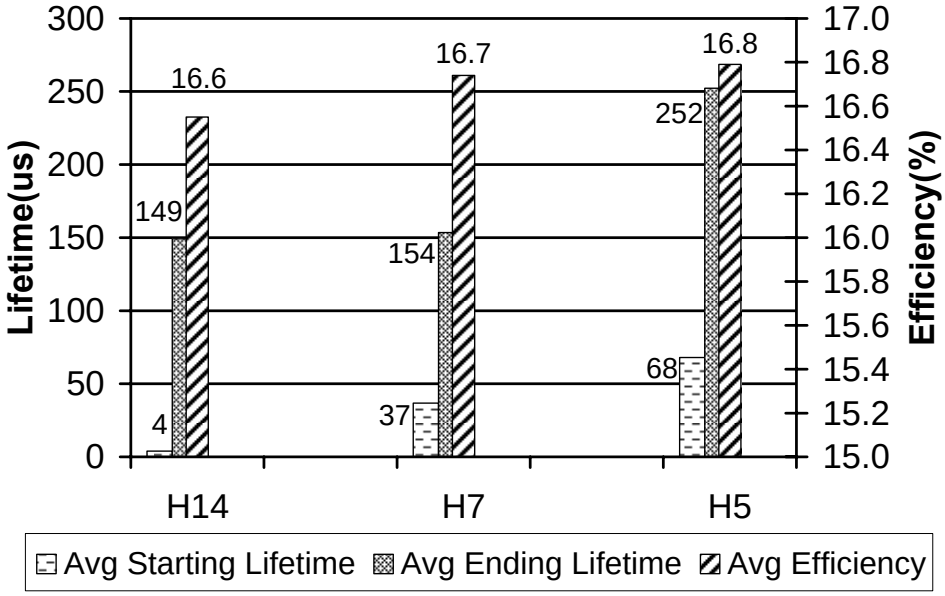


Figure 6.6 Average as-grown lifetime, average ending (after cell processing) lifetime, and average efficiency for the nine cells for three HEM mc wafers.

The IQE curves for the three mc-Si cells in Fig. 6.6 are shown in Fig. 6.7. The long wavelength response of all the three cells is quite comparable. The extracted BSRVs (using PC1D and measured lifetime) for these cells were found to be ~800, ~650, and ~600 cm/s, respectively, for the cells made on the low, medium, and high as-grown lifetime wafers. This is probably because low lifetime wafers also have more defects at

the surface, which may interfere with the formation of good and uniform BSF and result in a lower effective BSRV.

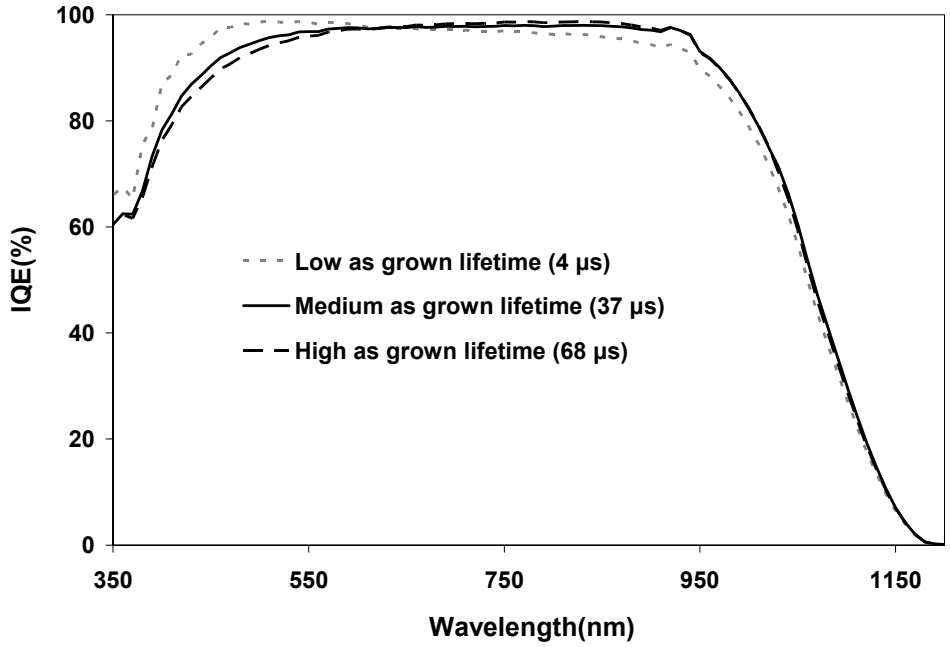
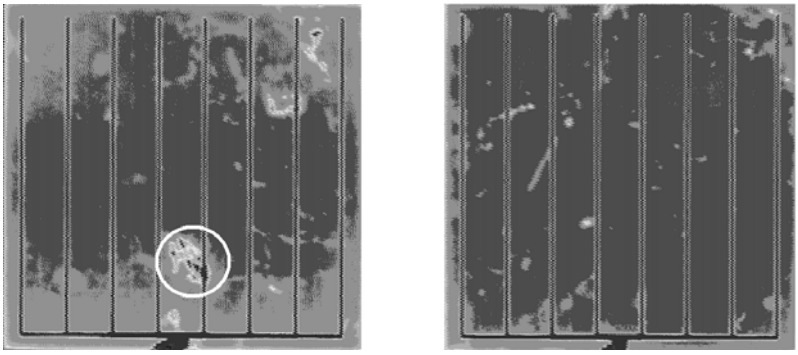


Figure 6.7 IQE response for HEM mc wafers with different starting (as-grown) lifetimes.

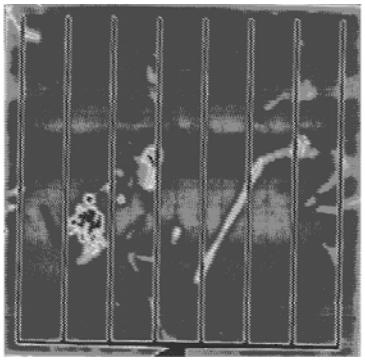
The LBIC response for the three cells from Fig. 6.6 is shown in Fig. 6.8. The average response (amps/watt) for these cells was consistent with the processed lifetimes. The LBIC map showed some low lifetime regions on the cells. One such spot was chosen on the wafer labeled H4-1 (circled in Fig. 6.8 (a)), and the IQE response was measured. Figure 6.9 shows that this region had very low long wavelength response compared to a high LBIC response region, which is indicative of low lifetime and/or low BSRV. There are probably un-passivated defects near the p-p+ interface that could increase the effective back surface recombination velocity.

The three HEM mc-Si cells (Fig. 6.6) with varying initial lifetimes were etched down to bare silicon to assess the processed lifetime. Processed lifetimes were found to

be 149 μs, 154 μs, and 252 μs for the low, medium, and high starting lifetime wafers, with standard deviations of 28 μs, 51 μs, and 74 μs. The processed lifetime distribution over the entire wafer is shown in Fig. 6.10 for the high as-grown lifetime wafer. These lifetimes were measured by a QSSPC setup at different locations on the wafer. The QSSPC setup measures lifetimes over a circle that is a few centimeters in diameter, giving an area-averaged number. The significant increase in the processed lifetime is the result of combined effect of $POCl_3$ gettering the SiN_x induced hydrogenation, since de-hydrogenation was minimized because of the *rapid* co-fire.



(a) H4-1 (4 μs) (b) H3-1 (37 μs)



(c) H2-1 (68 μs)

Figure 6.8 Light Beam Induced Current (LBIC) maps for solar cells with different as-grown lifetimes (a) 4 μs, (b) 37 μs, and (c) 68 μs on HEM mc-Si.

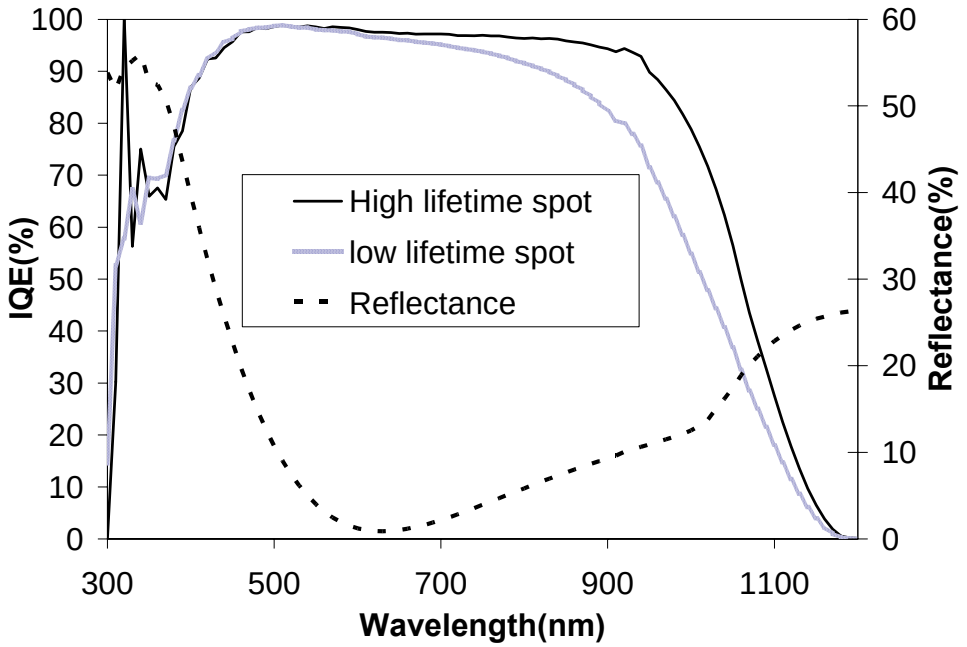


Figure 6.9 IQE responses and the reflectance for a low and high lifetime region of the same cell.

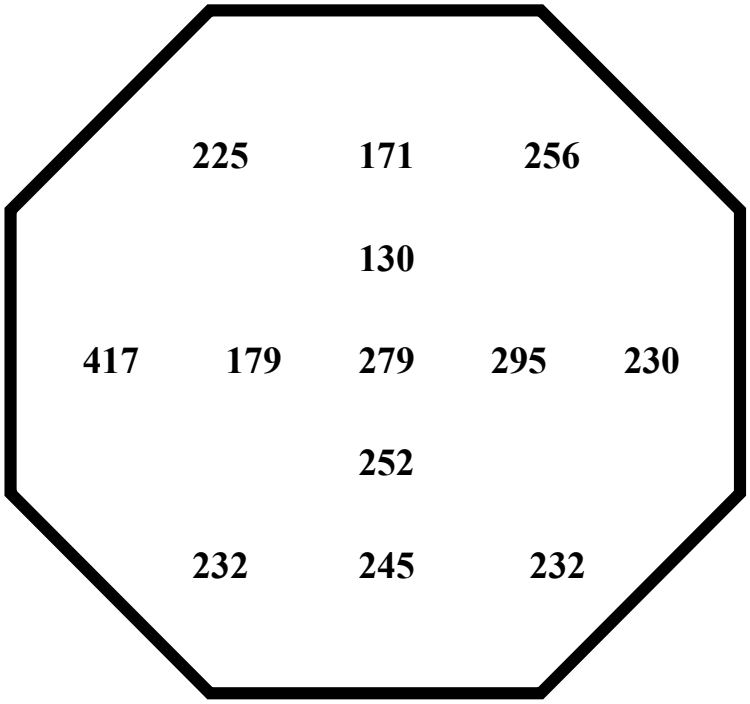


Figure 6.10 Lifetime distribution after cell processing for a high starting lifetime (68 μs) wafer.

6.3.3 Device modeling to see the effect of lifetime on solar cell efficiency

All the wafers, irrespective of their as-grown lifetime, benefited from gettering and hydrogenation. The measured cell parameters such as thickness, emitter profile, reflectance, R_{sh}, R_s, J_{02}, etc., were used to perform PC1D calculations. Figure 6.11 shows the dependence of efficiency on bulk lifetime for this cell design. Figure 6.11 also shows that for this cell design, efficiency does not change much for lifetimes values above 100 µs. This explains why there was not a significant efficiency gap between the mc-Si cells with a processed lifetime in the range of 149~252 µs (Fig. 6.6) as well as FZ wafers, with a processed lifetime of > 600 µs. Thus the performance of these cells is primarily limited by the cell design and technology and not the material quality.

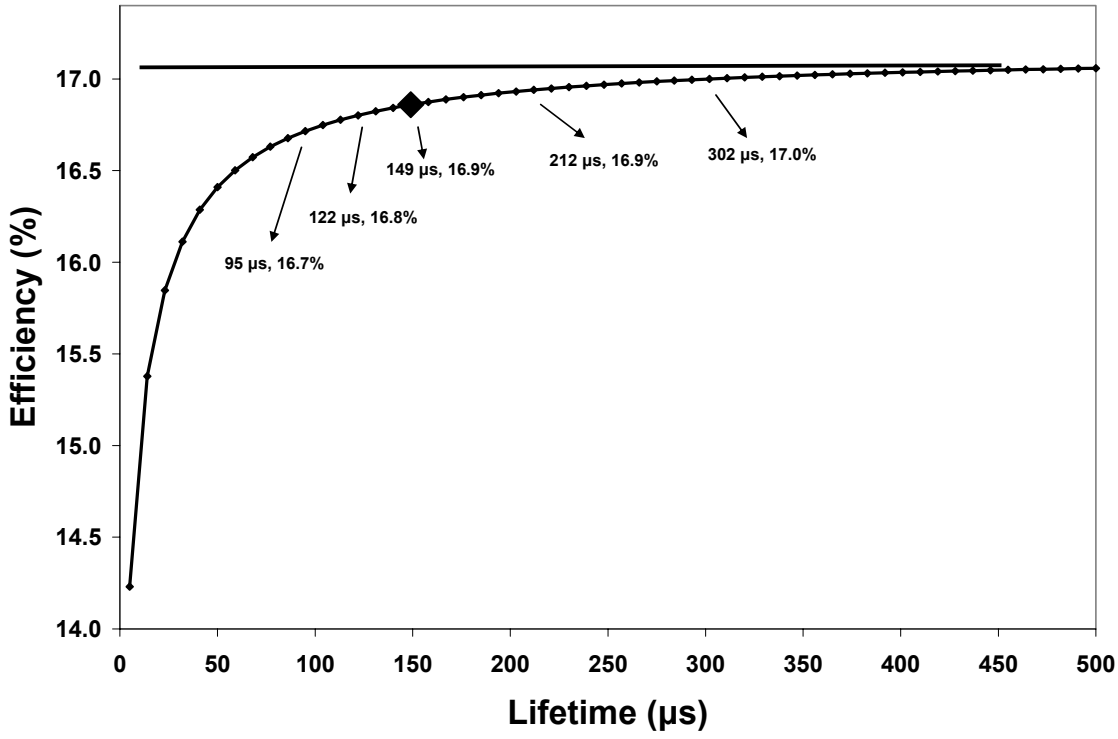


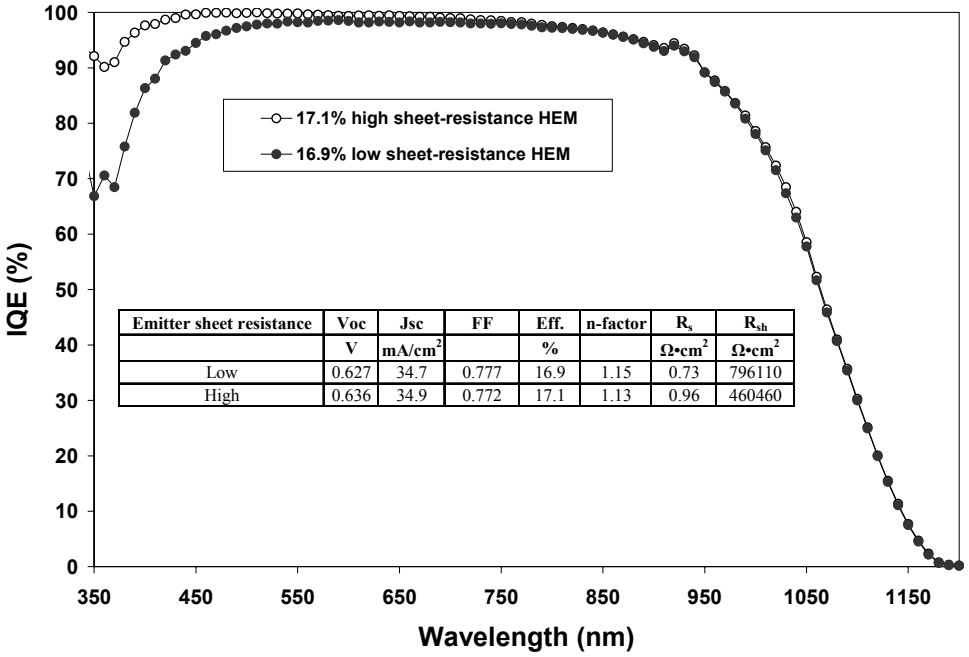
Figure 6.11 Calculations in PC1D showing the dependence of efficiency on bulk lifetime.

6.3.4 Fabrication and analysis of high-efficiency baseline mc-Si solar cells on high sheet-resistance emitters

The benefits of going to a high-sheet resistance emitter have been discussed in CHAPTER 4. Although the solar cells fabricated on high-sheet resistance emitters yield a higher J_{sc}, due of the reduced recombination in the emitter region compared to the low-sheet resistance emitters, but the formation of a good quality front contact is challenging. Due to the reduced surface concentration of the high-sheet resistance emitters, it is difficult to form contacts with low series resistance. The shallower emitter also makes them prone to shunting due to penetration of metal into the junction region.

Five different commercially available Ag pastes to form the front contact were studied by fabricating solar cells. The belt co-firing conditions were optimized carefully due to the reduced junction depth for the high-sheet resistance emitters. Over firing of the cells could lead to shunting and a higher n-factor. On the other hand, under fired cells would yield a higher series resistance. Of all the pastes analyzed, the front Ag paste by Ferro Corp. (CN 33-455) was found to yield the lowest series resistance, while retaining the benefits of the high-sheet resistance emitter. This resulted in the fabrication of 17.1% HEM mc-Si solar cell with a 100 Ω/sq emitter, independently confirmed by NREL. Process sequence was similar to the low-sheet resistance 16.9% cell discussed in section 6.3.1, except for the use of a different front Ag paste and a firing profile optimized for high-sheet resistance emitters. The 17.1% efficient solar cell had a single layer SiN_x AR coating on planar wafer and a full area Al-BSF. This represents the highest efficiency on planar, screen printed HEM mc-Si wafers with full area Al-BSF and a high sheet resistance emitter.

Figure 6.12 shows the IQE response and the I-V parameters of the 16.9% low sheet resistance (section 6.3.1) and the 17.1% high sheet resistance HEM mc-Si solar cell.



Emitter sheet resistance	Voc	Jsc	FF	Eff.	n-factor	R_s	R_{sh}
	V	mA/cm^2		%		Ω•cm^2	Ω•cm^2
Low	0.627	34.7	0.777	16.9	1.15	0.73	796110
High	0.636	34.9	0.772	17.1	1.13	0.96	460460

Figure 6.12 IQE response of the 16.9% low- and 17.1% high-sheet resistance HEM mc-solar cells.

There is a clear enhancement in the short wavelength IQE response for the high sheet resistance emitter, which shows up in the improved J_{sc} (0.2 mA/cm^2) of the solar cell. As expected, the long wavelength response is similar for the two cells.

The baseline process discussed in CHAPTER 4 has been further optimized for both low- and high-sheet resistance emitters to yield high-efficiency solar cells on HEM mc-Si wafers. This optimized process sequence is applied in the later chapters to study the effects of changing the base material and thickness of the solar cells.

6.4 Device modeling to establish guidelines for achieving high-efficiency (>20%) solar cells on relatively low-lifetime (~100 µs) and thin (~140 µm) Si wafers

After establishing the fabrication process sequence for high-eficiency low- and high-sheet resistance emitters, device modeling was performed with PC1D to establish the requirements for achieving high-efficiency (>20%) solar cell on relatively low lifetime (~100 μs) wafers. Device modeling was first performed to see the effects of various improvements that can be performed to the current high-efficiency baseline devices to improve the efficiency to over 20% on thin (~140 μm) silicon, which can make Si PV cost-effective.

Input parameters used for the 16.9% baseline solar cells are summarized in Table 6.3.

Table 6.3 Input parameters used in PC1D to model the high-efficiency 16.9% baseline solar cell.

PC1D input parameters-16.9% baseline		**Value**
Reflectance	Front external (inner layer thickness in nm/index	800/2.0
	Rear external (Fixed) (%)	70
	Internal reflectance (%)	80
Broadband reflectance (%)		5
Base contact (Ω·cm^2)		0.6
Thickness (μm)		280
Base resistivity (Ω·cm)		1.32
Emitter Sheet Resistance (Ω/sq)		45
Bulk lifetime (μs)		150
Front surface recombination velocity (cm/s)		30000
Back surface recombination velocity (cm/s)		450

Starting with the input parameters of Table 6.3, the change in efficiency was monitored when the following seven improvements were made to the device:

1) Change emitter sheet resistivity to 100 Ω/sq.
2) Change bulk resistivity to 0.5 Ω·cm.
3) Texture the front surface.

4) Change BSRV to 125 cm/s.

5) Change BSR to 97%.

6) Reduce contact resistance to 0.38 $\Omega \cdot cm^2$.

7) Change thickness to 140 μm.

Figure 6.13 shows the PC1D efficiency as a function of bulk lifetime for the baseline cell structure and the improvement in efficiency when these seven parameters were changed.

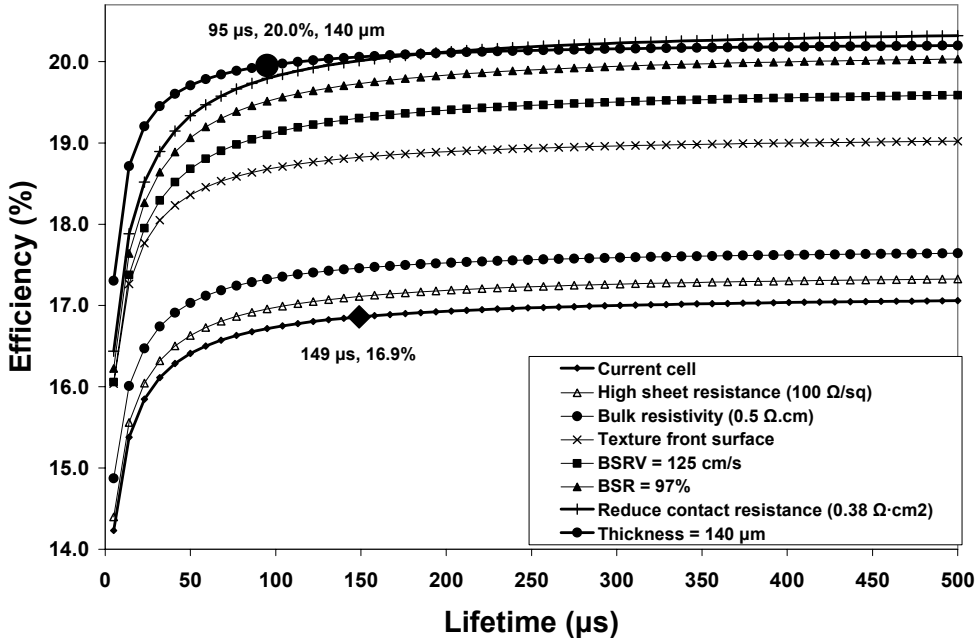


Figure 6.13 PC1D modeled efficiency as a function of bulk lifetime to see the effects of various improvements that can be applied to the current high-efficiency baseline solar cell.

By increasing the sheet-resistance of the emitter, lowering the bulk resistivity, and texturing the front surface, the efficiency of the baseline cell went up from 16.9% to 17.1, 17.5, and 18.8%, respectively. These three changes to the baseline device structure can be applied with the full area Al-BSF on the rear. However, to improve the efficiency further at this stage, the BSRV has to be lowered. Low BSRV values can be achieved by applying dielectric passivation to the rear surface. Several promising dielectric layers and

their passivation properties have already been discussed in CHAPTER 3. The application of these dielectric layers also would circumvent the bowing problems typical for the full area Al on thin Si wafers. An improvement in efficiency to 19.3% can be achieved if BSRV is lowered to a value 125 cm/s, and would further improve to 19.7% with a BSR of 97%. On further improving the contact quality by lowering the series resistance to at least 0.38 $\Omega \cdot cm^2$, efficiency can be pushed beyond 20%. After incorporating all these changes, if the thickness of device is reduced to 140 μm, no loss in performance is observed; and 20% efficient cells can be achieved.

Figure 6.13 shows that a crossover point occurs in lifetime range of 150 to 250 μs, where lower quality (lifetime), thin material would yield higher efficiency and a loss in efficiency would be observed for high-lifetime wafers. This crossover point would shift to the right, if BSRV value is increased; however, if the thickness is reduced below 140 μm, it would move to the left, hence favoring the lower lifetime materials. The threshold of 100 μs lifetime, after which the solar cell efficiency is not much dependent on the lifetime (section 6.3), also decreases once the advanced device features are applied to thin cells.

The results of Fig. 6.13 have been summarized in Fig. 6.14 in the form of a roadmap to achieve over 20% cells for a fixed bulk lifetime of 100 μs, on a 140 μm thick wafer. This 100 μs lifetime can be achieved even on low as-grown lifetime HEM mc-Si wafers by effective gettering and H passivation, as discussed section 6.3.2. It was also shown in CHAPTER 5 that ~100 μs lifetime can be achieved even in low quality String Ribbon substrates by effective H passivation of defects.

The first bar in Fig. 6.14 depicts the current industry standard of 14-16% cells. Next two bars represent the current high-efficiency baseline cells fabricated and characterized in the previous section, with a bulk lifetime of 150 µs. All the subsequent improvements are shown by assuming a bulk lifetime of 100 µs.

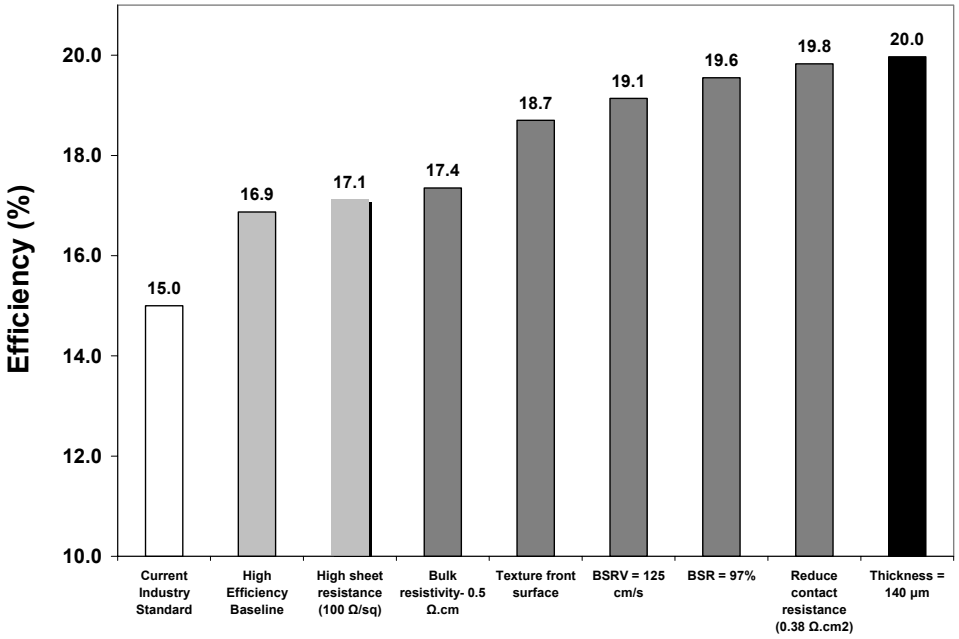


Figure 6.14 PC1D efficiency roadmap for achieving greater than 20% solar cells on 100 µs lifetime, 140 µm thick silicon wafers.

The two most significant improvements to push the efficiency to over 20% are the reduction of BSRV to at least 125 cm/s and increasing BSR to over 97%. These changes should ideally be incorporated in a low-cost manner to keep the module cost ($/W) down. Attempt has been made to accomplish this in CHAPTER 9 of the thesis to fabricate high-efficiency thin solar cells without any bowing.

6.5 Conclusion

An optimized co-firing process was developed to achieve high-efficiency cast mc-Si solar cells. This resulted in ~17% efficient 4 cm^2 screen-printed solar cells with single-

layer AR coating and no surface texturing or selective emitter. Nine 4 cm^2 cells on a 100 cm^2 Baysix mc-Si wafer showed an average efficiency of 16.7% and maximum efficiency of 16.8%. The HEM mc-Si wafer gave an average efficiency of 16.5%, with a maximum of 16.9%. The identical process applied to the un-textured Float zone (FZ) wafers gave an efficiency of 17.2%. These cells were fabricated using a simple, manufacturable process involving $POCl_3$ diffusion for a 45 Ω/sq emitter, PECVD SiN_x:H deposition for a single-layer antireflection coating and rapid co-firing of an Ag grid, an Al back contact, and Al-BSF formation in a belt furnace. These high efficiencies are attributed to the combination of effective gettering and hydrogenation, good ohmic contacts, and effective BSF achieved by this rapid process scheme. It is shown that if the lifetime during processing can be enhanced above a certain threshold (~100 μs for this cell design), the as-grown lifetime becomes relatively inconsequential. The bulk lifetime in the finished cells exceeded 100 μs and thus a tight efficiency range of 16.6-16.8% was obtained, even though the starting lifetimes in the cast mc-Si wafers used in this study were in the range of 4 -70 μs. Using a similar process sequence, a high-efficiency of 17.1% was achieved on high-sheet-resistance HEM mc-Si with good quality contacts. Finally, the effects of changing several device parameters on the efficiency of the solar cells was modeled with PC1D and guidelines were established to fabricate over 20% cells on low lifetime (100 μs), thin (140 μm) silicon wafers.

CHAPTER 7

INVESTIGATION OF SOLAR CELLS FABRICATED FROM TOP, MIDDLE, AND BOTTOM REGIONS OF HEM MULTICRYSTALLINE SILICON INGOTS

7.1 Introduction

High-efficiency boron- and gallium-doped multicrystalline silicon (mc-Si) cells were fabricated and compared in section 7.2 of this chapter. The quality of three different boron-doped mc-Si ingots and one gallium-doped mc-Si ingot was investigated and compared by means of lifetime measurements and solar cell efficiencies. Device characterization and modeling were performed to show that the combined effect of large variation in resistivity and lifetime along the gallium-doped mc-Si ingots results in variation in the cell efficiency from different regions of the gallium-doped ingots. Section 7.3 discusses the solar cell efficiency and lifetime enhancement during various solar cell processing steps for ingots from the same supplier with thicknesses of 225 and 175 μm and resistivities of 0.5 and 1.5 Ω·cm. Finally, section 7.4 presents the lifetime and solar cell efficiency results on the first two ingots grown by a novel process, which produces mono-crystalline ingots grown by the HEM casting process.

7.2 Bulk lifetime and efficiency enhancement due to gettering and hydrogenation of defects during cast multicrystalline silicon solar cell fabrication in top, middle, and bottom regions of a cast multicrystalline ingots from different suppliers

Despite the challenge of reaching efficiencies as high as its single-crystal counterpart, the market share of mc-Si remains above 50%. Current challenges in mc-Si include 1) variability in the quality of material associated with the position of the wafer in

the ingot, 2) non-uniformity within the wafer, 3) grain boundaries, twins, and dislocations acting as recombination sites, 4) difficulty in effective texturing due to random grain orientation, and 5) potential variability in light-induced degradation (LID) along the ingot length. The genesis of some of these problems is the use of a somewhat inferior quality of silicon (Si) feedstock, aimed at lowering the cost, diffusion of impurities from crucible walls, and segregation of impurities during the solidification from bottom to top. In general, mc-Si wafers from the sides, top, and bottom regions of a HEM mc-Si ingot are of inferior quality compared to those from the center region. The bottom part frequently suffers from lower bulk minority carrier lifetime (herein referred to as lifetime) because of oxygen and oxygen-induced thermal donors [131, 132] as well as high density of dislocations [133]. The low lifetime in the top region is attributed to metallic impurities that segregate in the melt and get incorporated in the top region. These impurities can also diffuse back in the top section of the ingot [133, 134]. The low lifetime in the top region of the ingot has also been attributed to thermal stress-induced defects and dislocations, which could be formed in the top region because of rapid cooling of the ingot at the end of the solidification process [27]. Several studies have been performed to observe the response of gettering, annealing, and hydrogenation on wafers from different regions of the mc-Si ingot [27, 132-137]. These studies have attempted to correlate the measured material and cell parameters (lifetime, J_{sc}, efficiency, etc.) with concentration and distribution of impurities. This section presents a systematic study of the variation in resistivity, oxygen, carbon, and bulk lifetime in silicon wafers sourced from different regions of cast mc-Si ingots and their response to different key process steps used during solar cell fabrication. Attempts are made to identify the steps to be incorporated or

modified to achieve a higher efficiency from low lifetime top and bottom regions of the ingot. In addition, the merit of growing gallium-doped mc-Si ingots is explored in an effort to achieve higher efficiency and eliminate the occasional LID observed in mc-Si solar cells.

7.2.1 Experimental

Sister wafers with identical electrical properties from the top, middle, and bottom regions of commercially grown mc-Si ingots were used in this study. Generally, the top 1-cm and bottom 2-cm regions of the cast mc-Si ingots are discarded because of unacceptably low lifetime. Wafers designated as top and bottom wafers in this section come from regions next to the discarded (1-2 cm) portions of the cast ingot. Solar cells were fabricated by the simple and manufacturable baseline process sequence (CHAPTER 4) shown in Fig. 7.1(a).

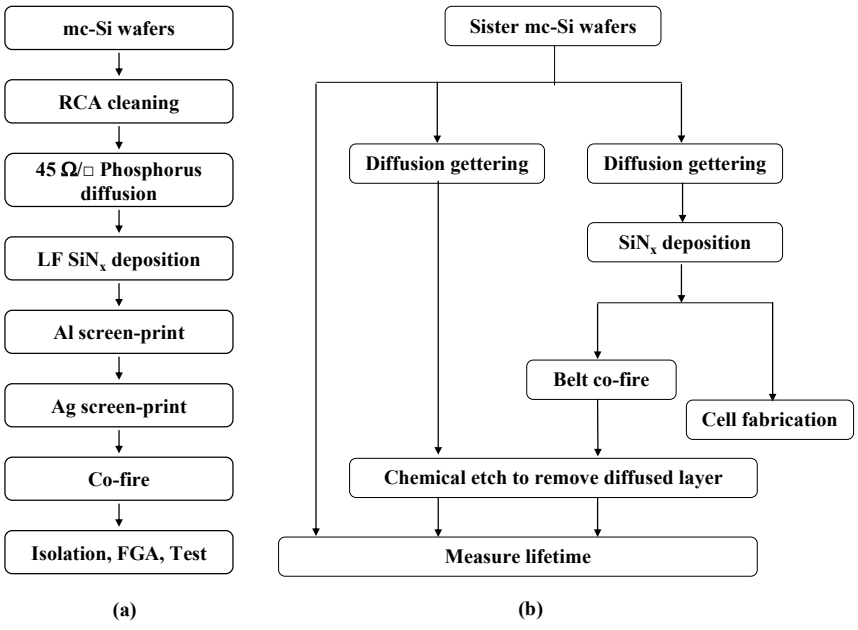


Figure 7.1 (a) Process sequence used for the fabrication of solar cells; (b) Schematic of the experimental plan followed.

The wafers used in this study first were etched chemically in acid to remove the saw damage folllowed RCA cleaning. Wafers were then diffused using liquid $POCl_3$ as the dopant source to form the n^+ emitter on both sides of the wafers. The $POCl_3$ diffusion or the impurity gettering step lasted for ~20 min at ~875 °C, resulting in a sheet resistivity of ~45 Ω/sq. The wafers were then coated with plasma-enhanced chemical vapor deposition (PECVD) SiN_x film deposited on one side of the wafer in a direct low-frequency reactor. Nine 4-cm^2 solar cells were fabricated on each 10 cm × 10 cm wafer by screen printing aluminum (Al) on the back and silver (Ag) grid on the front. The Al paste FX 53-038 from Ferro Corporation was used on the back side, and a commercial Ag paste from Dupont (4948) was used on the front. These cells were then co-fired using an optimized process in a lamp-heated IR belt furnace, resulting in the simultaneous formation of an Al back surface field (Al-BSF) and the Ag grid contact on the front. The nine cells were then isolated with a dicing saw. Finally, cells were annealed at 400 °C for 15 min in forming gas (FGA) before testing and analysis.

One set of companion wafers from different regions (top, middle, and bottom) was cleaned and diffused to form the $POCl_3$ emitter on both sides. In order to assess the impact of $POCl_3$ gettering, post-diffusion lifetimes were measured on these wafers after chemically etching the emitter and then passivating the surfaces with an iodine– methanol solution [61]. Another set of companion wafers was cleaned, diffused, and deposited with SiN_x on one side. This set was then fired in the belt furnace without any metallization followed by lifetime measurements in order to evaluate the impact of SiN_x-induced hydrogenation on bulk lifetime during the firing cycle. Post-hydrogenation lifetimes were measured after removing the SiN_x coating, chemically etching the emitter, and then

passivating the surfaces using an iodine–methanol solution. The experimental plan is shown in Fig. 7.1(b). Bulk lifetime measurements were performed using the quasi-steady-state photo conductance (QSSPC) technique [88], with both surfaces passivated using an iodine–methanol solution [61]. All reported lifetimes were measured at an injection level of 1×10^{15} cm^{-3}, averaged over ten different locations on a wafer.

7.2.2 Lifetime progress and corresponding solar cell performance

Four different ingots (1, 2, 3, and 4) from three different suppliers (A, B, and C) were investigated in this chapter. Ingots labeled ingot 1A and 2A were boron (B) doped from supplier A but had different base resistivities (1.3–1.5 Ω·cm and 0.5–0.7 Ω·cm, respectively). Ingot 3B was boron doped from supplier B with a base resistivity of 1.8–2.0 Ω·cm. Ingot 4C was gallium (Ga) doped from supplier C with a base resistivity ranging from 1.4 to 8.1 Ω·cm. Figures 7.2–7.4 show the lifetime enhancement in the three boron-doped ingots as a function of wafer position, $POCl_3$ gettering, and defect hydrogenation from the SiN_x film during the contact co-firing cycle. The best cell efficiency attained from the top, middle, and bottom regions of the three different boron-doped ingots is also shown in Figs. 7.2–7.4.

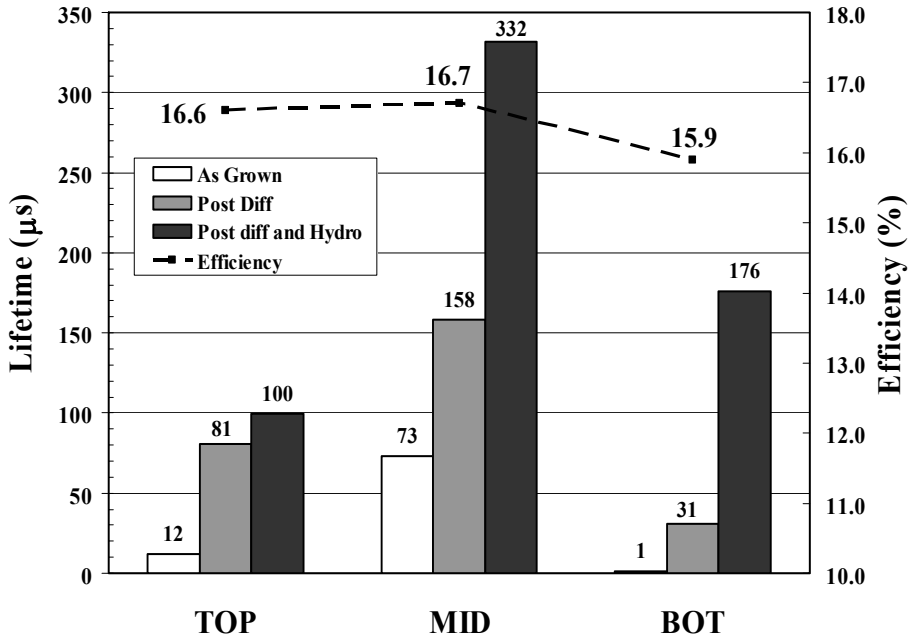


Figure 7.2 Lifetime progress and best solar cell efficiency for ingot 1A (supplier A, boron, resistivity ~1.5 Ω·cm).

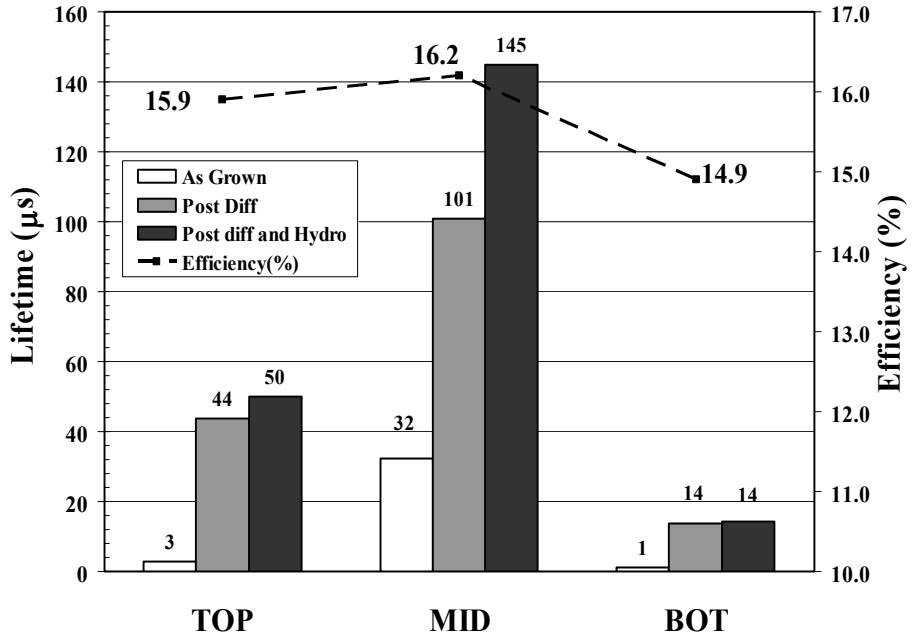


Figure 7.3 Lifetime progress and best solar cell efficiency for ingot 2A (supplier A, boron, resistivity ~0.5 Ω·cm).

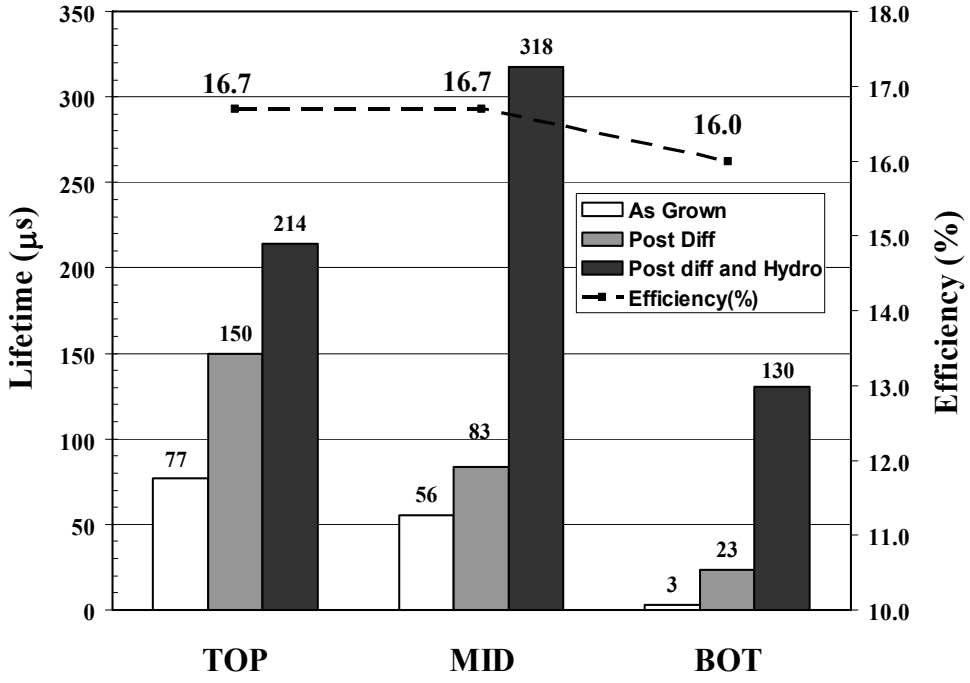


Figure 7.4 Lifetime progress and best solar cell efficiency for ingot 3B (supplier B, boron, resistivity ~2.0 Ω·cm).

7.2.2.1 Lifetime enhancement in the wafers from the top, middle, and bottom regions of the mc-Si ingots

The $POCl_3$ diffusion step to form the n^+ junction also acts as a gettering step, which extracts the metallic impurities from the active region of the cell, resulting in lifetime enhancement. The hydrogen released from the SiN_x coating passivates the defects, further enhancing the lifetime. Figure 7.5 summarizes the observed increase in lifetime due to these two key processing steps.

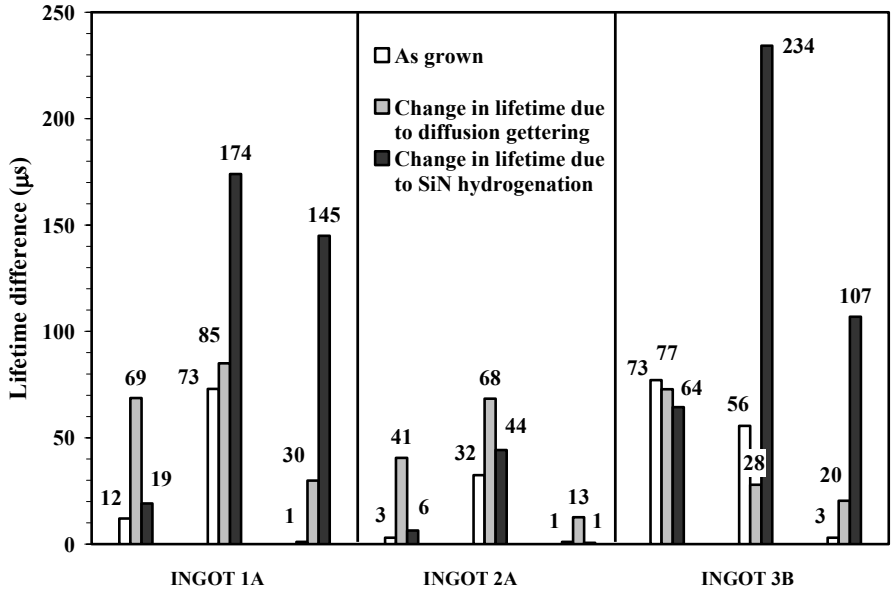


Figure 7.5 Change in lifetime in different regions (top-middle-bottom, in the same sequence) of the three ingots due to the solar cell processing steps of diffusion-gettering and SiN_x-induced hydrogenation.

It is evident from Fig. 7.5 that the top region of all the three ingots benefited most from the $POCl_3$ diffusion gettering step because the metal impurities tend to accumulate in the top region and diffuse back in the ingot after the solidification process. In addition, the back diffusion length of these impurities would be governed by their diffusivities and the ingot cooling time, which in turn would be a function of the ingot size. Fortunately the fast interstitially-diffusing impurities can be gettered out easily during the short diffusion-gettering step (~ 30 min). The slow substitutionally diffusing impurities, which are difficult to getter out in the short gettering step, dictate the post-gettering lifetime in conjunction with the impurities present in the form of precipitates, oxides, and silicides which are very difficult to getter. Figure 7.5 shows that the as-grown lifetime of 12 μs in the top region of the ingot 1A increased to 81 μs (lifetime change = 69 μs) after the diffusion gettering alone. However, hydrogenation from the SiN_x film did not improve

the lifetime as dramatically as the diffusion gettering. In Fig. 7.5, SiN_x-induced hydrogenation improved the bulk lifetime of the top region of ingot 1 A from 81 to 100 μs (lifetime change = 19 μs). In contrast to the top region, bottom region benefited more from the hydrogenation step. For example, diffusion gettering raised the bulk lifetime of the bottom region of ingot 1A from 1 to 31 μs, but hydrogenation took it to 176 μs. Hence for ingot 1A, hydrogenation was very effective in passivating the lifetime limiting defects in the bottom region. As discussed earlier, bottom region generally has more oxygen, oxygen and metal precipitates, crystal defects, and fast diffusing metallic impurities that diffuse in the ingot from the crucible wall through solid-state diffusion during the ingot cooling. Bottom of the ingot also has more grain boundaries (smaller grain size) and a higher density of dislocations because of the higher temperature gradient in the bottom during the start of the crystallization process. Higher oxygen content in the bottom region also can induce dislocations. Fast interstitially-diffusing impurities are gettered by the short diffusion giving rise to modest lifetime enhancement. However, impurities and precipitates decorating the dislocations and grain boundaries are hard to getter but easier to passivate. That is why we observe much greater lifetime enhancement in the bottom wafers by the SiN_x-induced hydrogenation. The lifetime in the middle part of the ingots improved significantly from both gettering and hydrogenation. For example, in Fig. 7.5, gettering raised the bulk lifetime of the middle region of ingot 1A from 73 to 158 μs and hydrogenation increased it to 332 μs. The poor response of the wafers from the bottom region of ingot 2A in Fig. 7.5 indicates that there are some lifetime-dominating defects that could neither be gettered nor hydrogenated. There could be a higher degree of dopant defect interaction in this low resistivity ingot, which can also

lower the lifetime [138-140]. Figure 7.5 shows that for these three ingots, the increase in lifetime due to diffusion-gettering is more effective in the top regions, and SiN_x-induced hydrogenation is more effective in the bottom regions (except for the bottom region of ingot 2A). The hydrogenation trend observed in this study is consistent with the results of Geerligs [137], who showed that the degree of hydrogenation (or J_{sc}) increases as we move from middle to bottom regions of the ingot.

7.2.2.2 Effect of lowering the resistivity on mc-Si solar cell performance

It is apparent from Fig. 7.2 that high post-hydrogenation lifetimes (≥100 μs) were attained from all three regions (top, middle, and bottom) of ingot 1A. For the lower-resistivity ingot 2A (Fig. 7.3), lifetime revived only in the middle region of the ingot. The top region of the ingot showed good response to the gettering and reached a reasonably good lifetime value of 50 μs. However, the bottom showed very little improvement, with lifetime remaining below 20 μs. The best cell efficiencies from the top, middle, and bottom wafers of ingot 1A were 16.6%, 16.7%, and 15.9%, respectively, and the corresponding efficiencies for lower-resistivity ingot 2A were 15.9%, 16.2%, and 14.9%, respectively. Thus, lowering the resistivity below 1 Ω·cm seems to retard the process induced lifetime enhancement and lowers cell performance. This could be due to a higher dopant–impurity interaction in lower-resistivity ingot 2A, which makes it difficult to getter and passivate. Hence, the expected benefits of going to a lower base resistivity [138] are not realized in mc-Si cells because the increase in the open circuit voltage (V_{oc}) resulting from lowering the resistivity is not able to compensate for the decrease in the lifetime and the short-circuit current (J_{sc}). Dopant-defect interaction and its effect on cell performance and optimum resistivity is discussed and modeled in section 7.3.

7.2.2.3 Effect of higher bulk lifetime on cast mc-Si solar cell performance

The effect of higher bulk lifetime on solar cell performance was evaluated by comparing cast mc-Si ingots 3B and 1A from different vendors as well as the top and middle regions within these ingots. Figure 7.4 shows that there is a significant enhancement in lifetime in wafers from the top, middle, and bottom regions of ingot 3B, with the average bulk lifetime reaching 214, 318, and 130 μs, respectively, after complete cell processing. The screen printed cell efficiencies were 16.7%, 16.7%, and 16.0% from the top, middle, and bottom regions of ingot 3B, respectively. It is interesting to note that ingot 3B had a significantly higher lifetime compared to ingot 1A in the top region. In addition, lifetime was higher in the middle region than the top region in both ingots 1A and 3B; however, cell efficiencies were very similar in the top and middle regions of both ingots. Device simulations were performed using PC1D [130] to understand this behavior, with the input parameters listed in Table 7.1.

Table 7.1 Input parameters for PC1D used in the simulations

Parameter name	PC1D input
Reflectance front external	Coated: 80 nm (index 2.0); Broadband reflectance 6%
Reflectance rear external	70% (Fixed)
Reflectance internal	Front Surface: 92% (First and subsequent bounce); specular Rear Surface: 80% (First and subsequent bounce); diffuse
Base contact	0.6 Ω
Internal Conductor	2e-3 S
Internal Diode	1e-8 A
Material file	si.mat
Front Diffusion	45 Ω/sq. sheet resistance; erfc profile
Front surface recombination velocity	45000 cm/s
Illumination intensity	0.1 W cm^{-2}
Illumination spectrum	File: am15g.spc

A back surface recombination velocity (BSRV) of 450 cm/s, typical for solar cells with an Al-BSF, and a resistivity of 1.3 Ω·cm were used in the modeling. Model calculations in Fig. 7.6 show that for the screen printed cells designed and fabricated in this study, once bulk lifetime exceeds 100 μs, lifetime has little impact on cell efficiency, as also pointed out in CHAPTER 6.

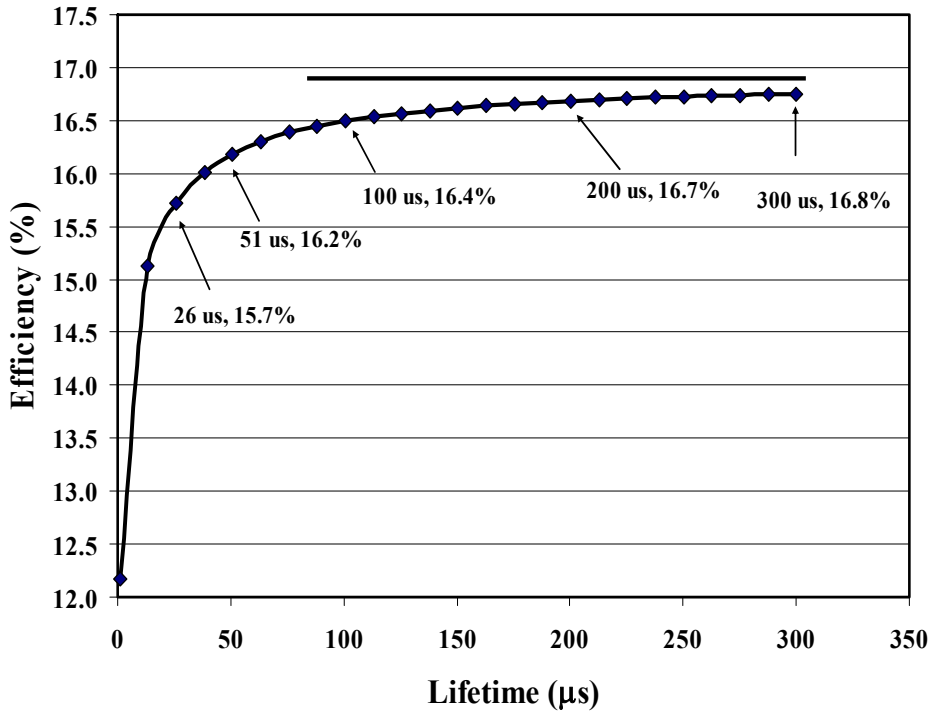


Figure 7.6 PC1D-modeled efficiency dependence on lifetime. After a lifetime of ~100 μs, efficiency is not a strong function of lifetime.

This explains why cell performances from ingots 3B and 1A were virtually identical in spite of the difference in lifetime. Figure 7.6 also reveals that if the bulk lifetime in the finished device does not reach 100 μs, it will degrade the cell efficiency. It should be noted that the measured efficiencies of the cells from the top and middle regions of the ingot agree well with this simulation, but the efficiencies of cells from the bottom region of ingots 1A and 3B were lower than expected from the simulation. This

could be due to oxygen precipitate-induced local non-uniformities, which are not accounted for in the PC1D model calculations. The average lifetime values obtained in this paper agree well with those of Henze, et al. [141], who reported a lifetime of 340 μs after gettering and hydrogenation on comparable resistivity (1.3 Ω·cm) B-doped wafers. Cell data in Figs. 7.2–7.4 reveal that our process sequence produced 4-cm^2 screen printed cell efficiencies of ≥ 14.9% for all the ingots regardless of the wafer location. Cell efficiencies of ≥ 15.9% were achieved from the top and middle regions of all three ingots. Only the wafers from the bottom region of ingot 2A showed a low as-grown lifetime (1 μs), which remained low (14 μs) even after gettering and passivation, resulting in a cell efficiency of 14.9%. Figures 7.2–7.4 show the best cells obtained from the three ingots. Table 7.2 shows the average values of the solar cell parameters.

Table 7.2 Average values of solar cell parameters for the 4 cm^2 cells fabricated from different regions of the three ingots

Ingot #	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff (%)	# of cells	Region
Ingot 1A	620	33.2	78.20	16.1	13	TOP
	621	34.6	77.43	16.2	15	MID
	620	32.9	76.53	15.6	13	BOT
Ingot 2A	621	32.3	77.62	15.6	10	TOP
	625	32.8	77.30	15.9	12	MID
	604	30.5	76.58	14.1	14	BOT
Ingot 3B	618	34.1	77.32	16.3	9	TOP
	617	34.0	77.61	16.3	17	MID
	615	32.9	77.29	15.7	9	BOT

It should be noted that the cells in Table 7.2 were fabricated in two experiments. Some wafers were broken during processing, and cells with unusually high series resistance or low shunt resistance were omitted from the average values in Table 7.2. Average efficiencies in the range of 15.6%–16.3% were achieved from all regions of the three ingots, except for the bottom region of ingot 2A, which had a lower resistivity. High average V_{oc} values (~620 mV) were also obtained for most of the cells, which is also consistent with the high lifetimes achieved in Figs. 7.2–7.4. The standard deviations of the solar cell parameters listed in Table 7.2 are in the range of 3–5 mV, 0.2–0.5 mA/cm^2, 0.72%–1.54%, and 0.2%–0.4% for V_{oc}, J_{sc}, FF, and efficiency, respectively, for all the cells from different regions.

Close examination of the cell data revealed that the fill factors (FF) of the cells from the bottom region of the ingots were consistently lower relative to the FF of the cells from the other regions. This suggests that the impurities or defects in the bottom region, that could not be effectively gettered or passivated by the process sequence, also introduce excess recombination in the junction region. This was further supported by the suns V_{oc} measurements that showed higher J_{02} values for the bottom region as compared to the middle and the top region. For example for ingot 2A, J_{02} values were 42, 37, and 56 nA/cm^2 for the top, middle, and bottom regions, respectively.

To understand the impact of process-induced lifetime on cell performance, Internal Quantum Efficiency (IQE) measurements were performed on cells fabricated on wafers from top, middle, and bottom regions of all the three ingots. The IQE response of cells from top, middle, and bottom regions of ingot 1A is shown in Fig. 7.7.

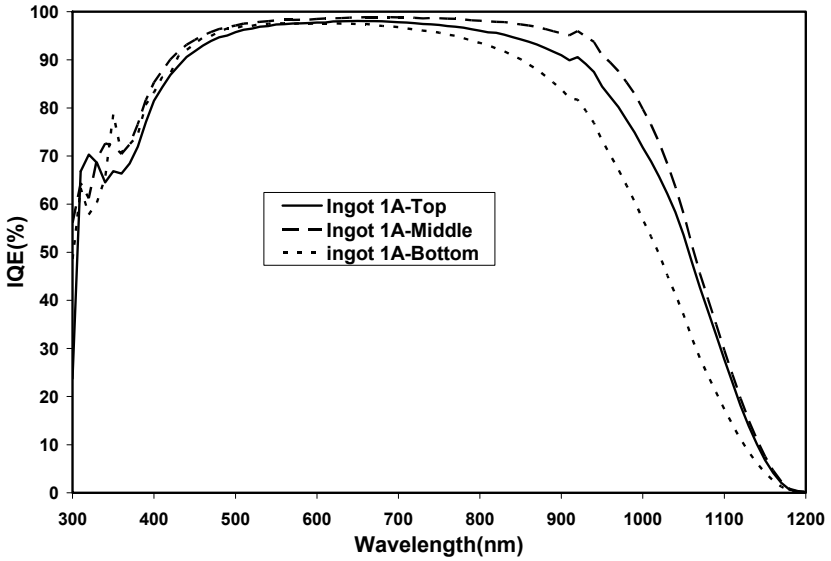


Figure 7.7 Internal Quantum Efficiency (IQE) response for wafers from top middle, and bottom regions of ingot 1A (see Figure 7.2).

Qualitatively similar behavior was observed for all other ingots. It is important to note that IQE may have some spatial variation over the cell area. Hence the IQE response was evaluated at various regions in the cell and only the best response is reported. All the wafers from the middle showed a superior IQE response relative to the wafers from the top or bottom. This is consistent with the lifetime-efficiency data for these ingots. For ingot 3B, cells from the top region showed a comparable performance to the middle region, which is not surprising because the bulk lifetime in both regions was found to be greater than 100 μs threshold, above which cell efficiency is not very sensitive to bulk lifetime.

7.2.3 Light-induced degradation in boron doped cast multicrystalline silicon solar cells

The oxygen and carbon content of the wafers was measured using fourier transform infrared spectroscopy (FTIR). Figure 7.8 shows the interstitial oxygen content

in different regions of the three ingots (ingots 1A, 2A, and 3B). Figure 7.9 shows the substitutional carbon content in the same three ingots.

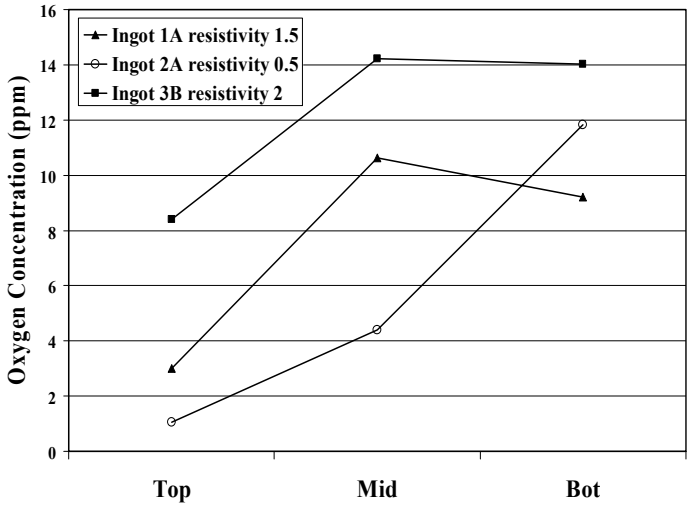


Figure 7.8 Interstitial oxygen concentration in parts per million for ingots 1A, 2A, and 3B with resistivities of 1.5, 0.5, and 2 Ω · cm, measured using FTIR.

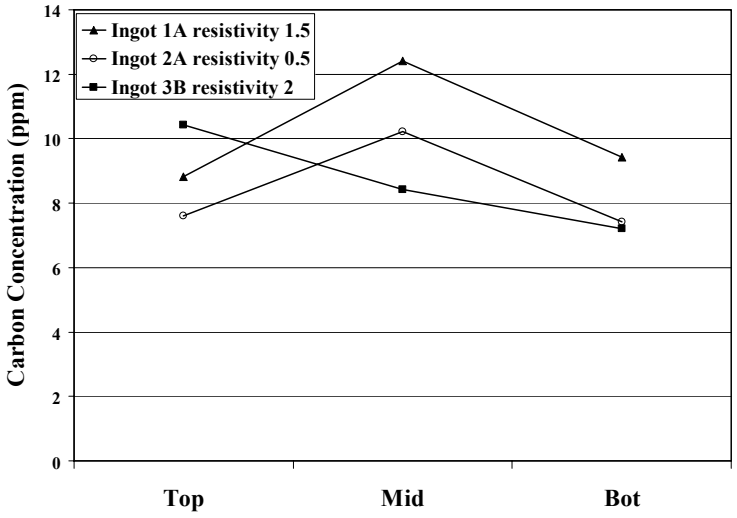


Figure 7.9 Substitutional carbon concentration in ppm for ingots 1A, 2A, and 3B with resistivities of 1.5, 0.5, and 2 Ω · cm, measured using FTIR.

Interstitial oxygen concentration increases from top to bottom of the ingot in most cases. This oxygen is incorporated mainly close to the surface and the bottom regions of

the ingots following the reaction of the molten silicon with the quartz crucible [142]. This increases the likelihood of oxygen precipitation in the bottom region of the ingot during cooling. This could partly explain the low as-grown lifetime in the bottom region. Oxygen precipitates can getter metal impurities and, in combination with dislocations or grain boundaries, can enhance metal precipitation at these sites. These metals could be subsequently released in the bulk during high-temperature solar cell processing steps and may give rise to electrically active local regions. This may slow down the gettering process if the dissolution rate of precipitated impurities is slow and rate limiting [143]. This may explain the limited recovery of lifetime in the bottom wafers of some of the ingots. Defects resulting from carbon in mc-Si are less electrically active, but they can enhance the formation of as-grown oxygen precipitates in the crystal growth process [144]. Also, these defects can trap recombining impurities, specifically oxygen [145]. A relatively high oxygen concentration in the bottom and middle wafers of ingot 3B and ingot 2A prompted us to look for the LID in these wafers.

LID in Czochralski (Cz) silicon has been studied and explained on the basis of the B_sO_{2i} complex, which acts as a lifetime-reducing recombination center [146-150]. LID in mc-Si was first reported by Nagel, et al. [151], and since then, it has been observed and reported by other researchers as well [152]. However, it is a more serious problem in single-crystal Cz-Si, where a ~1% reduction in absolute efficiency has been reported for 1 Ω·cm cells with ~ 10^{18} cm^{-3} (~20 ppm) oxygen. However, in mc-Si, because of the relatively low oxygen concentration, LID is not viewed as a serious problem. In regions with a high oxygen concentration in mc-Si, a reduction of 2%–4% (relative) in efficiency has been reported [153]. To study the LID phenomenon in these mc-Si cells, two cells

from each region of the three B-doped ingots were soaked in light for about 25 h at ~1 sun. The cells were annealed in dark at 200 °C for 25 min to remove the LID, if any, prior to subjecting them to a light soak for 25 h. The most degradation resulting from illumination is observed in the first few hours after which the lifetime stabilizes [154]. The temperature of the wafers during the light soaking process in our setup reached ≥ 80 °C. Light I–V and internal quantum efficiency (IQE) measurements were performed before and after the light soaking.

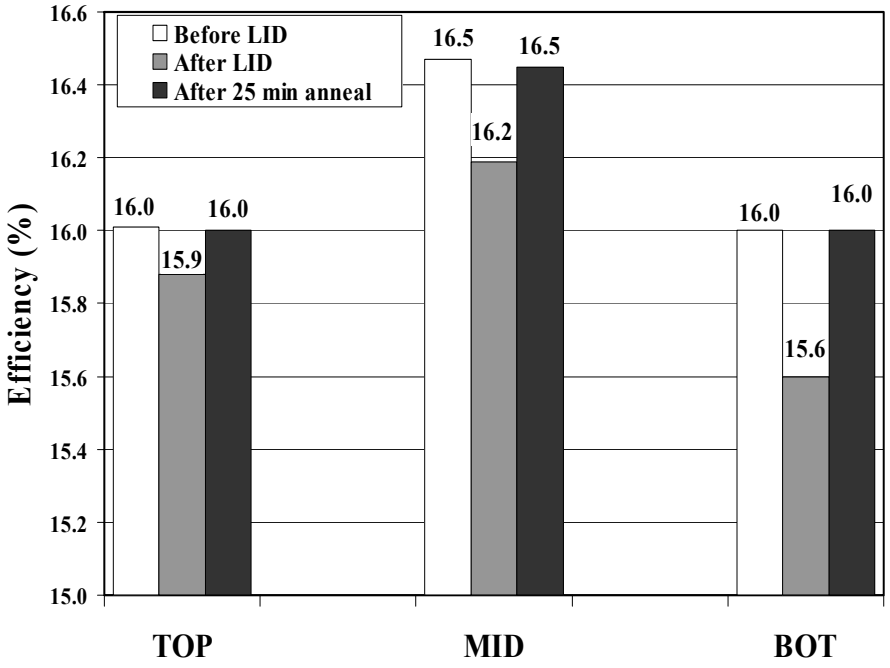


Figure 7.10 Observed LID in efficiencies for ingot 3B (resistivity 2 Ω·cm).

Fig. 7.10 shows that the middle and bottom regions of ingot 3B showed LID, but only about 2% relative degradation in efficiency was observed in the middle region cells with ~14 ppm oxygen, and 2.5% relative degradation was observed in the bottom region cells with ~14 ppm oxygen. The top of ingot 3B, with only ~8 ppm oxygen, did not show any appreciable LID. It should be noted that this ingot had intermediate doping (2.0

Ω·cm). Contrary to the expectation, ingot 2A, which showed reasonably high oxygen concentration in the bottom region along with high doping (0.5 Ω·cm), did not undergo any appreciable LID in efficiency. This is attributed to the fact that the lifetime in the bottom of ingot 2A is quite low (14 μs) to begin with, compared to ingot 3B, so a degradation in bulk lifetime resulting from LID would not have much impact on the final lifetime and cell efficiency. The middle region of ingot 2A, with a higher lifetime (~150 μs), also showed no LID because of the very low oxygen concentration (~4 ppm). Figure 7.10 shows that all the wafers recovered after an anneal in the dark at 200 °C for 25 min, supporting the presence of the metastable defect associated with boron–oxygen pairing [154]. These wafers were then again subjected to light soking for three days, and the same efficiency degradation was observed. LID was also confirmed by the decrease in long wavelength IQE response. The IQE response, before and after LID, for solar cells from the bottom region of ingot 3B is shown in Fig. 7.11.

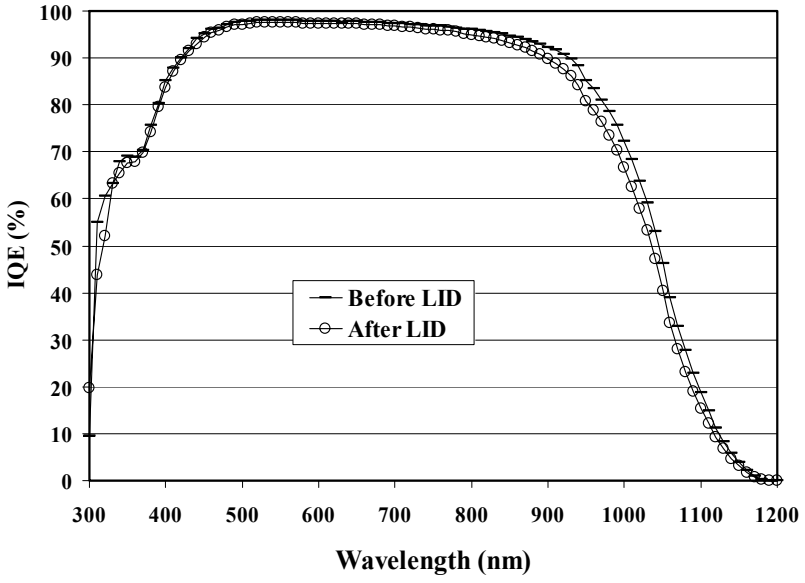


Figure 7.11 IQE response for solar cells from the bottom region of ingot 3B (see Figs. 7.4 and 7.10) before and after LID.

7.2.4 Effect of gallium doping on efficiency and light-induced degradation in cast multicrystalline solar cells

The LID observed in some mc-Si cells led to the investigation of alternatives to boron doping. Gallium doping has been suggested as an alternative to boron for higher efficiency cells with no LID, and some positive results have been reported [152]. This section presents a systematic study of the process-induced lifetime enhancement and a comparison of the Ga- and B-doped mc-Si cells.

Figure 7.12 shows the as-grown lifetime, processed lifetime, average cell efficiency (20–25 cells), best cell efficiency, and resistivity of wafers from the top, middle, and bottom regions of the Ga doped ingot 4C.

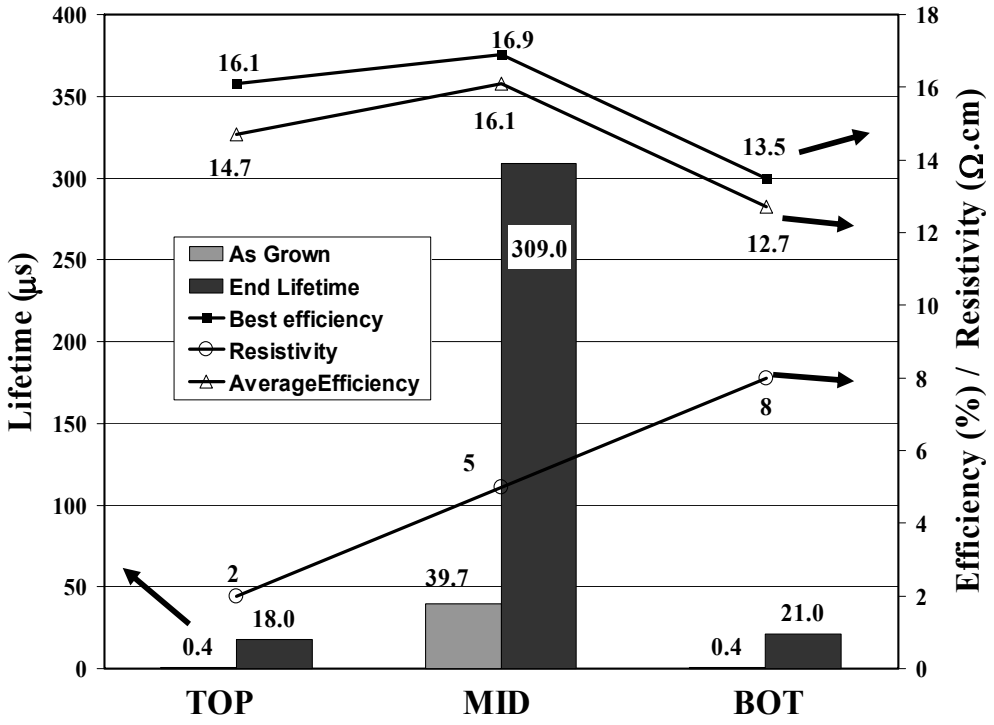


Figure 7.12 Lifetime progress and best solar cell efficiency for ingot 4C (supplier C, gallium, resistivity 2–8 Ω · cm).

As seen from Fig. 7.12, the middle region of the Ga-doped ingot showed a very favourable response to the solar cell processing steps, with processed lifetime exceeding 300 μs. However, wafers from the top and bottom of the ingot did not show much improvement. This could be due to a high concentration of impurities in these regions incorporated during the growth by supplier C. Therefore, another boron-doped ingot (ingot 5C) was obtained from the same supplier for proper comparison. The resistivity of ingot 5C was in the range of 1.0–1.2 Ω·cm. Figures 7.13 and 7.14 show the efficiency distribution of about 20 cells from each region of ingots 4C and 5C.

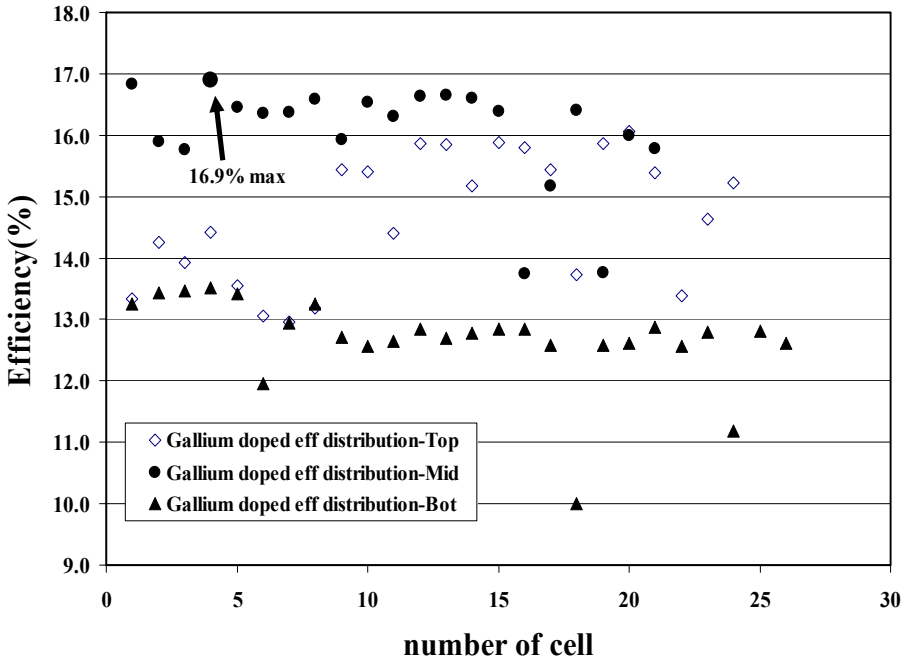


Figure 7.13 Efficiency distribution of solar cells processed from top, middle, and bottom regions of the Ga-doped ingot (ingot 4C) from supplier C.

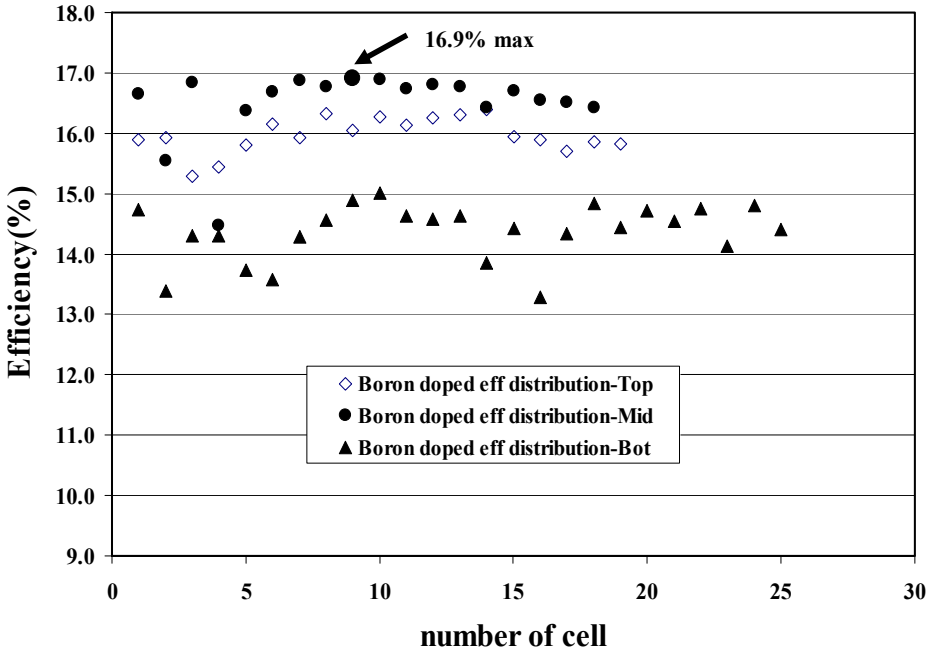


Figure 7.14 Efficiency distribution of solar cells processed from top, middle, and bottom regions of B doped ingot (ingot 5C) from supplier C.

A maximum efficiency of 16.9% was attained from the middle portion of both the Ga- and B-doped ingots. However, the top and bottom regions of the B-doped ingot yielded higher efficiencies. The spread of efficiencies is also tighter (lesser standard deviation) for the B-doped ingot. It should be noted that this finding is based on only one Ga-doped ingot used in this study and should not be generalized. Some researchers have reported a more uniform distribution of efficiencies from the different regions of a Ga doped ingot [152], where a special 70-kg ingot was grown and studied. High J_{sc} values were obtained from the 5 Ω·cm resistivity middle region of the Ga-doped ingot (best: 36 mA/cm^2, average: 35 mA/cm^2) along with high V_{oc} (best: 625 mV, average: 620 mV). The fill factors were lower in the Ga-doped ingots. However, the top and bottom regions of the Ga-doped ingot yielded very low V_{oc} (606 and 555 mV, respectively) and J_{sc} (32.4

and 31.1 mA/cm^2, respectively), indicating a much lower lifetime dominated by impurities. This was also supported by the IQE response (Fig. 7.15) of the cells from the three regions.

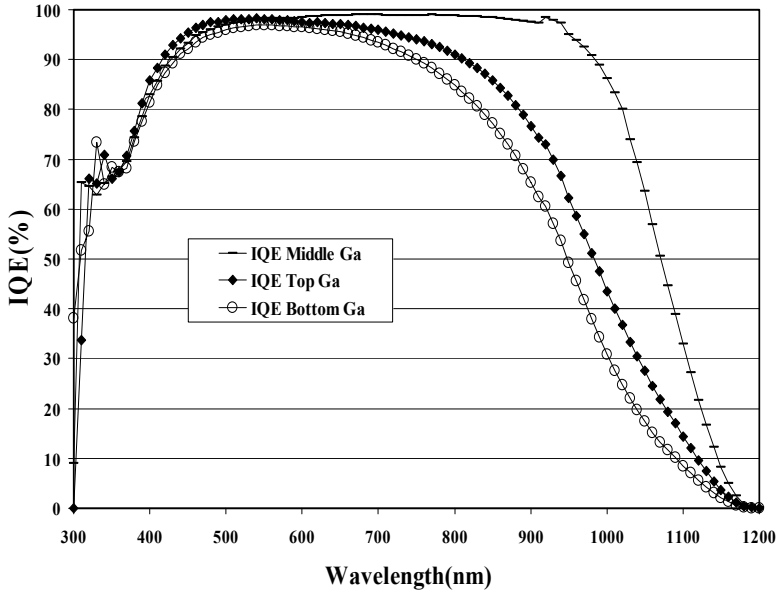


Figure 7.15 IQE response for solar cells from top, middle, and bottom regions of the Ga-doped ingot (ingot 5C).

No LID was observed in any region of the Ga-doped ingot. This supports the expected finding that replacing B with Ga dopant should eliminate LID completely and affirms that LID in B-doped mc-Si cells is much less than reported for B-doped Cz cells. The solar cell efficiencies obtained from the B-doped ingots were comparable to the efficiencies from the impurity-free middle region of the Ga-doped ingot. Hence, Ga doping in mc-Si did not produce an appreciable advantage over B doping [141].

7.2.5 Device design and modeling to reduce the effect of resistivity variation on gallium-doped cell efficiencies

Gallium has a lower segregation coefficient than boron, resulting in a wide variation in resistivity of the wafers from the top to bottom regions. This can lead to an

appreciable variation in the efficiencies of cells from different regions if the device design and parameters are not optimized. Device modeling was performed using PC1D device simulation program [130] to devise some design rules for optimizing performance and reducing spread in efficiency when there is a large resistivity and bulk lifetime variance. Device modeling was performed using an n^+-p-p^+ device structure. The common parameters used in all the PC1D simulations are listed in Table 7.1.

7.2.5.1 Understanding the Optimum L/W Ratio

Figure 7.16 shows the efficiency versus thickness curves for resistivities varying from 2 to 5 Ω·cm. These curves are for bulk lifetimes varying from 20 to 200 μs with a fixed BSRV of 200 cm/s.

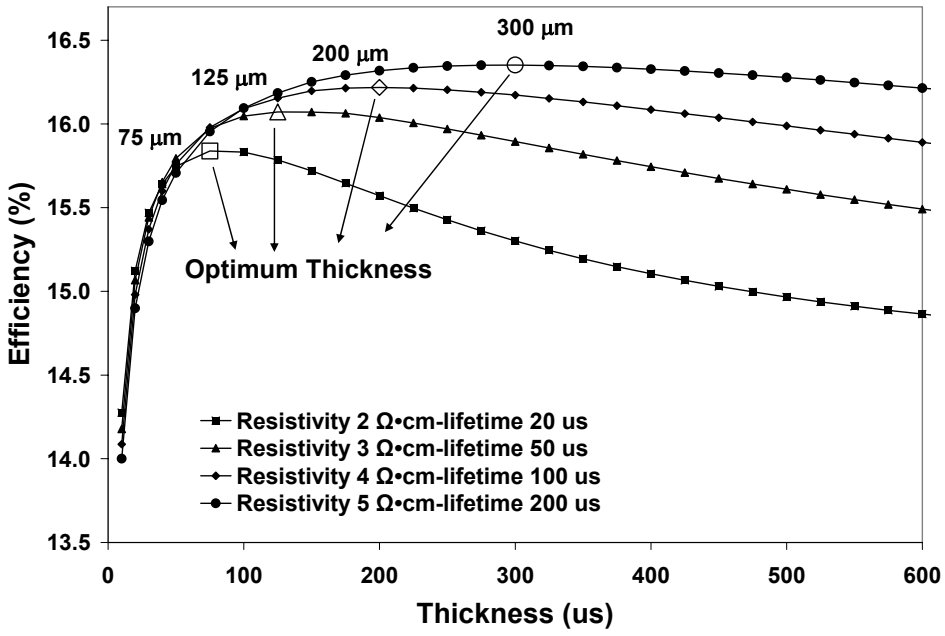


Figure 7.16 Efficiency versus thickness curves for different resistivities and lifetimes, showing a peak in the efficiency at a given thickness. These curves are for a BSRV of 200 cm/s.

Figure 7.16 shows that for a fixed diffusion length (L), base doping, and BSRV, cell efficiency peaks at a particular thickness (W), yielding an optimum L/W ratio for that diffusion length, doping, and BSRV combination.

7.2.5.2 Effect of Lifetime and Doping on Optimum L/W Ratio

Simulations were performed to determine the optimum L/W ratio ($(L/W)_{OPT}$) for solar cells with bulk lifetimes varying from 25 to 1000 μs and base resistivities in the range of 0.2–20 Ω·cm. Most PV materials fall into this lifetime and resistivity range. Figure 7.17 shows the results of these model calculations.

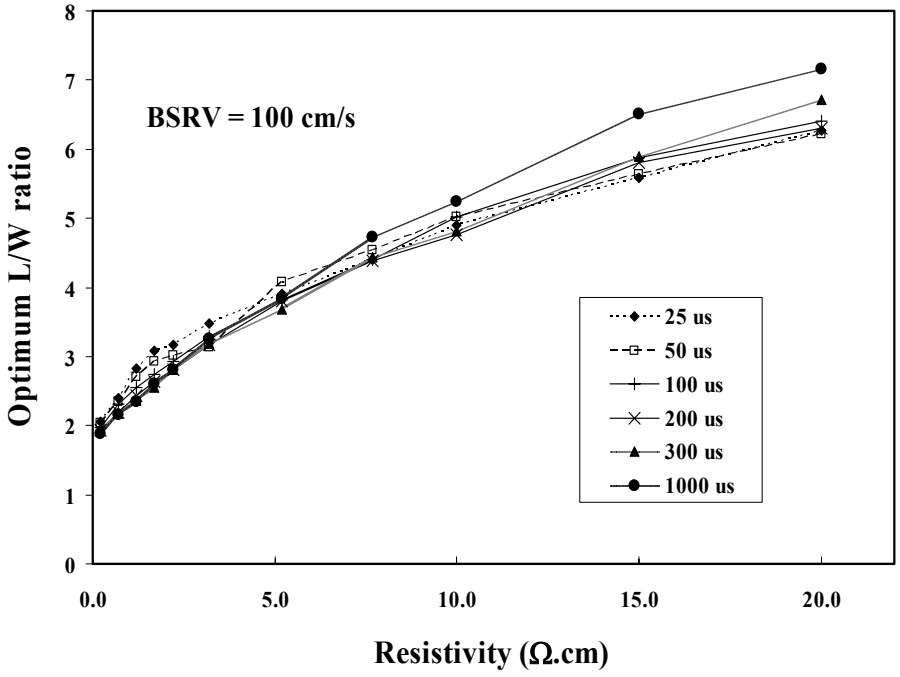


Figure 7.17 Optimum L/W ratios as a function of base doping for different lifetimes. These curves are for a BSRV of 100 cm/s.

Figure 7.17 shows that for a low BSRV of 100 cm/s, $(L/W)_{OPT}$ varies from 2 to 7 as resistivity changes from 0.2 to 20 Ω·cm. It should also be noted that the $(L/W)_{OPT}$ ratio is not as strong a function of bulk lifetime. Further model calculations showed that the

optimum L/W ratio becomes more sensitive to bulk lifetime as BSRV is increased. Thus, the optimum thickness (W_{OPT}) will vary depending on the location of the wafer in a gallium-doped ingot, which typically has a large resistivity gradient, with higher resistivity favoring thinner wafers.

Table 7.3 Determination of optimum thickness from the optimum L/W ratio for resistivities of 1.2 and 5.2 Ω·cm, lifetimes of 50 and 200 μs, and BSRV of 100 cm/s.

Resistivity (Ω.cm)	Lifetime (μs)	$(L/W)_{opt}$ ratio	W_{opt} (μm)
1.2	200	2.5	309
1.2	50	2.7	140
5.2	200	3.8	199
5.2	50	4.1	92

Table 7.3 shows that, for a BSRV of 100 cm/s, if the resistivity of an ingot changes from 1.2 to 5.2 Ω·cm, with the bulk lifetime fixed at 200 μs, $(L/W)_{OPT}$ increases from 2.5 to 3.8, reducing the optimum thickness from 309 to 199 μm. However, if the resistivity is fixed at 5.2 Ω·cm and the bulk lifetime changed from 200 to 50 μs, the optimum L/W ratio increases from 3.8 to 4.1, resulting in a decrease in the optimum thickness to 92 μm.

7.2.5.3 Reduction in Efficiency Spread for HEM mc-Si Through L/W Ratio Modeling

Figure 7.18 shows the modeling for a Ga-doped ingot, wherein resistivity varies from 2 to 8 Ω·cm as we move from top to bottom, with a bulk lifetime of 20 μs in the top and bottom regions, and a lifetime of 200 μs in the middle region.

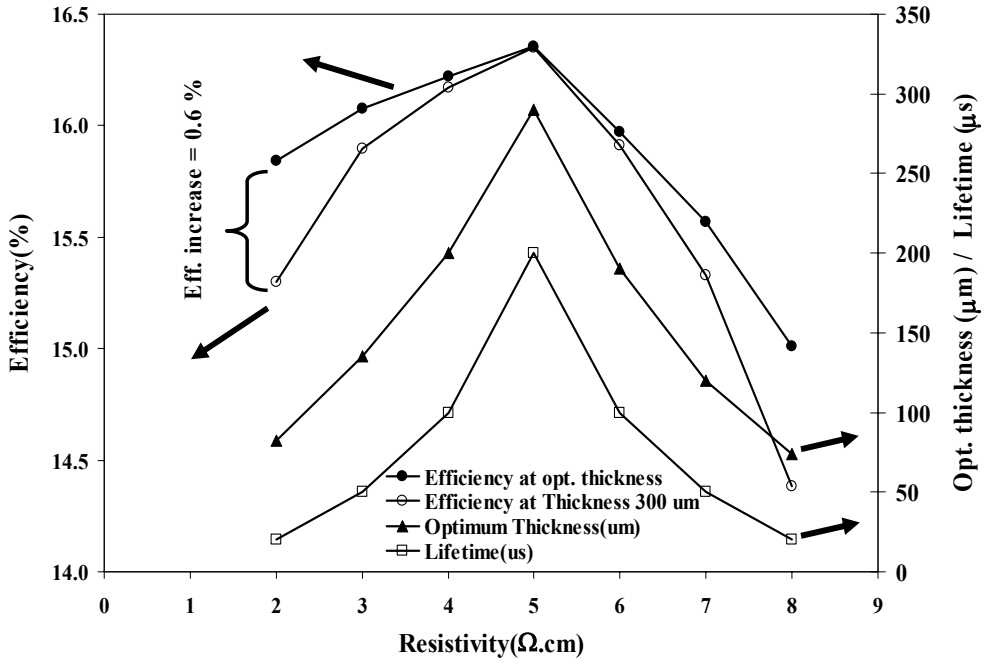


Figure 7.18 PC1D simulated curves for efficiencies at 300 µm and at optimum thicknesses. Also shown is the value of optimum thickness and the corresponding lifetime value for each resistivity used in the modeling. These curves are for a BSRV of 200 cm/s.

Figure 7.18 also shows the calculated W_{OPT} from $(L/W)_{OPT}$ ratio and the cell efficiencies for a constant thickness of 300 µm as well as for optimum thickness W_{OPT}. These curves were generated for a BSRV of 200 cm/s. These data clearly show that reducing the cell thickness from 300 µm to W_{OPT} in the top and bottom regions reduces the efficiency spread. Hence, for a BSRV of 200 cm/s, the efficiency spread is reduced from 2% (16.4%–14.4%) to 1.4% (16.4%–15%). This optimization will have a more positive impact for a lower BSRV. For higher BSRV, the effect of this optimization on efficiency spread will be less pronounced, but it will produce the best attainable efficiencies with less silicon, resulting in a better utilization of the whole ingot.

The design rules established above give an overview of the merit of optimizing thickness based on bulk lifetime and resistivity. It would be impractical, however, to cut

wafers of different thicknesses along the ingot length. A more practical approach based on the above design optimization would be to cut the entire ingot with wafer thickness equal to minimum W_{OPT}, which would correspond to the optimum thickness for wafers from the top and bottom low lifetime regions. Another rule of thumb could be to cut the wafers as thin as possible (~100 μm) if the BSRV is on the order of 100–200 cm/s. Simulations performed for a constant thickness of 150 μm along the entire ingot length showed no appreciable compromise in the cell efficiencies relative to the W_{OPT} case. These guidelines can also be used for boron-doped ingots as well, where resistivity is nearly constant, but the lifetime in the top and bottom regions is low.

The four ingots B-doped and one Ga-doped ingot analyzed in this study were from three different vendors because of which there could be variability in the impurity content and type, depending on the quality of the Si feedstock used, the cleanliness of the crucible and the thermal profile during solidification employed by the vendor. To minimize the effects of such variations, solar cells were also fabricated on four different B-dope ingots from the same supplier. The results are presented in the next section.

7.3 Investigation of the effects of resistivity and thickness on the performance of HEM mc-Si solar cells from top, middle, and bottom regions of four different ingots from the same supplier

The mc-Si wafers investigated in this section were obtained from the same supplier and are expected to have a similar impurities and defects. The impact of reducing the resistivity and thickness of the solar cells on wafers from the top, middle, and bottom regions of these mc-Si ingots was investigated.

A low resistivity of 0.2-0.3 Ω·cm has been shown to be optimum for high quality single-crystal silicon for solar cells. However, for lower quality cast mc-Si, this optimum

resistivity increases due to dopant-defect interaction, which reduces the bulk lifetime at lower resistivities. An enhancement in efficiency can be realized by reducing the base resistivity for high quality FZ, single crystal, Si solar cells, which show an optimum at 0.2-0.3 Ω·cm [138]. This increase in performance is due to the increase in the open circuit voltage (V_{oc}) of the solar cell, without significant loss in the short circuit current (J_{sc}). However, the benefits of going to lower resistivity are not realized in Cz Si due to dopant-induced light induced degradation [150] and in mc-Si solar cells due to dopant-defect interaction. Hence, this section analyzes the impact of increasing the base doping through lifetime monitoring and mc-Si cell fabrication and analysis.

Currently, silicon constitutes about 50% of the total module cost and, therefore, a significant cost reduction could be realized if the wafer thickness is reduced without compromising yield and cell performance. Reduction in thickness often results in a decrease in performance of cells with conventional design with an aluminum back surface field (Al-BSF). However, somewhat lower cell efficiency on thinner wafer can be more cost effective compared to a higher cell on thick wafer [155]. In this study, the effect of reducing the wafer thickness on cell performance and cost is investigated by comparing 225 μm and 175 μm thick wafers.

7.3.1 Experimental

Solar cells were fabricated using the standard, manufacturable baseline process with 45 Ω/sq emitter and SP contacts on wafers from the top, middle, and bottom regions of four different boron doped p-type ingots from the same supplier, as shown in Table 7.4. To minimize the bowing, a special low bow Al paste was used on the rear side. Lifetime in the finished cell was measured after etching off the emitter and the Al-BSF.

Table 7.4 Thickness and resistivity of ingots used in this study.

Ingot #	Thickness (μm)	Resistivity (Ω·cm)	Region*
1	225	0.6	T,M,B
2	225	1.5	T,M,B
3	175	0.6	T,M,B
4	175	1.5	M
* T = Top; M = Middle; B = Bottom			

7.3.2 Lifetime and performance of thick and thin mc-Si solar cells

The I-V results of solar cells with SP contacts on 225 μm and 175 μm thick wafers in Table 7.5 show that wafers from the middle of each ingot yielded the best cells with peak efficiencies in the range of 16.4 to 16.7%.

Table 7.5 Best I-V parameters of solar cells fabricated on various thicknesses and resistivities and from different regions of ingots 1-4, using screen-printed contacts.

V_{oc} (V)	J_{sc} (mA/cm^2)	FF	Eff (%)	Region
Ingot-1 Thickness: 225 μm. Resistivity : 0.6 Ω·cm				
0.623	32.7	0.7908	16.1	TOP
0.624	33.3	0.7868	16.4	MID
0.620	32.5	0.7867	15.9	BOT
Ingot-2 Thickness: 225 μm. Resistivity : 1.5 Ω·cm				
0.615	32.7	0.7813	15.7	TOP
0.624	34.1	0.7847	16.7	MID
0.615	33.9	0.7817	16.3	BOT
Ingot-3 Thickness: 175 μm. Resistivity : 0.6 Ω·cm				
0.617	31.2	0.7810	15.0	TOP
0.627	33.0	0.7922	16.4	MID
0.623	32.8	0.7812	16.0	BOT
Ingot-4 Thickness: 175 μm. Resistivity : 1.5 Ω·cm				
0.623	33.9	0.7840	16.5	MID

No dependence on wafer resistivity or thickness was observed for the cells from the middle of each ingot. Cells made on wafers from the top of each ingot showed lower J_{sc} and V_{oc} values, suggesting that the bulk lifetime in these wafers was lower than those

from the middle of the ingots. Figure 7.19 summarizes the as-grown, post diffused, and post-fired lifetimes in wafers from ingots 1-4.

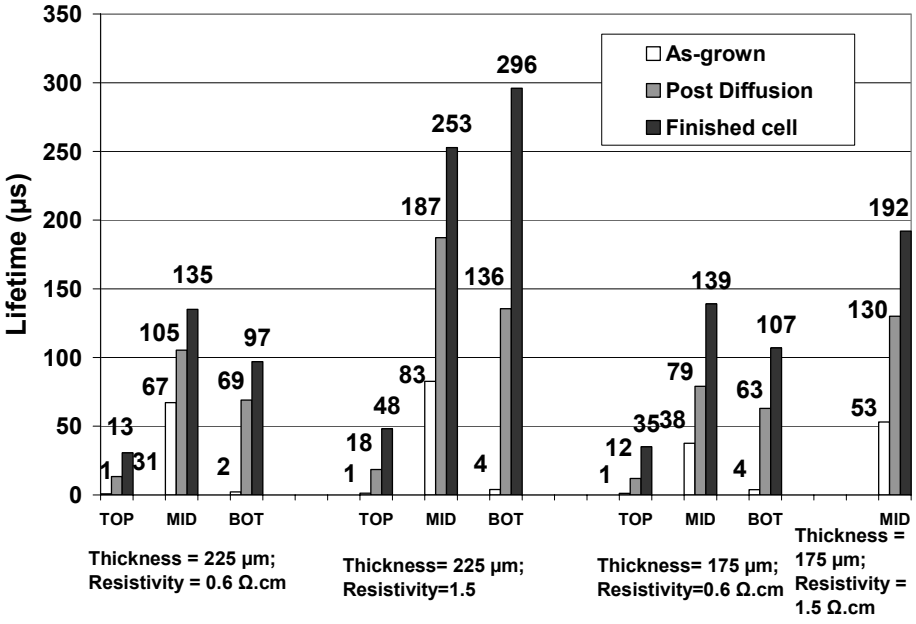


Figure 7.19 As-grown, post diffusion and finished cell lifetime of solar cells fabricated in this study.

The results in Fig. 7.19 again show that wafers from the middle of the ingots have high bulk lifetimes after growth (38-83 µs), while wafers from the top and bottom of the ingots have much lower lifetimes (1-4 µs). Gettering during $POCl_3$ diffusion improved the lifetime in all regions of the four ingots, but was particularly more effective in wafers from the bottom of the ingots where the lifetime increased to 63-136 µs. The middle region also benefited significantly from the gettering process. Lifetime was further enhanced during the co-firing cycle due to SiN_x-induced hydrogenation of defects in both middle and bottom regions. Figure 7.19 shows that the gettering and passivation treatments in this study were more effective in the middle and bottom regions of the ingots. After both P-gettering and hydrogenation steps, the lifetime in middle and bottom regions of most of the ingots was close to or in excess of 100 µs, while the lifetime in the

top regions was below 50 μs. This is contrary to the expectation that P gettering should be more effective in the top regions of the ingot (Section 7.2.2.1). This could however be due to high density of dislocations (>10^6 cm^{-2}), typical to wafers from the top of the ingots, if it cools down faster at the end of the solidification process. These dislocations, or impurity decorated dislocations, then would dominate the lifetime, even after interstitial and substitutional impurities have been gettered or passivated [27]. Thus, lifetime recovery in the top or bottom or both regions could be dependent on the nature of impurities and crystallographic defects, which in turn could be different for different suppliers. For the ingots investigated in this section, the lifetime enhancement profile is different compared to the ingots in section 7.2.2.1, which possibly is due to the difference in feedstock quality, crucible, and the thermal profile used by this supplier during ingot growth.

Figure 7.19 also shows that the bulk lifetime in wafers from the middle of ingots 1 and 2 decreased from 253 μs to 135 μs when the resistivity was lowered from 1.5 Ω·cm to 0.6 Ω·cm. This decrease in lifetime is again attributed to a dopant-defect interaction and is analyzed in the following sub-sections.

7.3.2.1 Effect of lifetime and base resistivity on the performance of mc-Si solar cells

The results in Table 7.5 and Fig. 7.19 show that there was no significant difference in the best cell efficiency of the solar cells made on different resistivity substrates, despite a significantly lower finished cell lifetime in low resistivity wafers. This can be partly explained by the dependence of efficiency on bulk lifetime. As shown earlier, once the bulk lifetime exceeds 100 μs for this cell design, efficiency is no longer a strong function of lifetime. In this study the lifetime in the wafers from the middle of

ingots 1 (0.6 Ω·cm) and 2 (1.5 Ω·cm), exceeded 100 μs after processing leading to >16% efficient 4 cm^2 cells. Even with a lower final lifetime, no change in V_{oc} was observed for the lower resistivity wafers. For example, an increase in *average* V_{oc} of 2 mV was found in the bottom region wafers of 0.6 Ω·cm (ingot 1) wafers, compared to the 1.5 Ω·cm (ingot 2) wafers, even though lifetime was ~200 μs lower in the lower resistivity case.

7.3.2.2 Effect of reducing the wafer thickness on the performance of mc-Si solar cells

The performance of mc-Si solar cells could increase or decrease when the wafer thickness is reduced depending on the device parameters such as bulk lifetime and back surface recombination velocity (S_r) [156, 157]. An improvement in V_{oc}, on decreasing the thickness, can be observed if S_r on the back of the p-type wafer is kept below a critical value given by $S_{r,cr} = D/L$ (D: Diffusion constant for minority carriers, L = diffusion length of minority carriers in the base region) as is evident from Eq. 7.1, where J_{0b} (dark saturation current of base) increases for values greater than $S_{r,cr}$. On the other hand for S_r values less than $S_{r,cr}$, an enhancement in V_{oc} would be observed due to a decrease in J_{0b}.

$$J_{0b} = \frac{qDn_i^2}{LN_A}F, \tag{7.1}$$

with

$$F = \frac{\frac{S_r L}{D} + \tanh(\frac{W}{L})}{1 + \frac{S_r L}{D}\tanh(\frac{W}{L})}, \tag{7.2}$$

where,

S_r : Rear surface recombination velocity,

W: Device thickness, and

N_A: Doping concentration.

Hence, V_{oc} is a key parameter to assess whether reducing the thickness is beneficial or not. For low lifetime top region wafers (eg., ingot 1- lifetime: 31 μs; resistivity: 0.6 Ω·cm), $S_{r,cr}$ is ~800 cm/s. Whereas, for higher lifetime middle region (ingot 1- lifetime: 135 μs; resistivity: 0.6 Ω·cm), $S_{r,cr}$ is ~ 400 cm/s. For the screen-printed solar cells fabricated in this study, the Al-BSF gives an S_r values > 700 cm/s for the 0.6 Ω·cm wafer. This was estimated from the calculated Al-BSF profile and an SRV model. Hence, a slight improvement in V_{oc} is expected by reducing the thickness of the low lifetime top region wafer where $S_{r,cr}$ is ~800 cm/s. However, an appreciable reduction in V_{oc} is expected for high lifetime middle region where $S_{r,cr}$ is ~400 cm/s. This was indeed found to be the case, where the *average* V_{oc} practically remained unchanged for the top region, whereas it showed a 6 mV decrease for the middle region. This was further supported by V_{oc} data of high lifetime cells from middle and bottom regions of other ingots, where 4-6 mV decrease in the V_{oc} was observed on reducing the thickness. For example, the average V_{oc} reduced from 615 mV for 225 μm-thick wafers in the middle of Ingot 2 to 610 mV for 175 μm-thick wafers in the middle of Ingot 4, a decrease of 5 mV. The values of J_{sc} did not decrease much with the reduction in thickness from 225 μm to 175 μm. Hence it can be concluded that for the set of wafers studied here, thickness variation in the range of 225 to 175 μm does not degrade the cell efficiency, it only reduces the cost.

7.3.3 Device modeling to see the impact of base doping and thickness on solar cell performance

Device modeling was performed using PC1D [130] to study the effects of changing the base doping and thickness on the device performance. A front surface

recombination velocity of 45000 cm/s and S_r (BSRV) of 600 cm/s were assumed. It should be noted that the S_r values are expected to be slightly higher for lower resistivity wafers, but in these simulations, the same value of S_r is assumed for all resistivities and the effect of doping on bulk lifetime is described by a model for dopant defect interaction given by equation 7.3 [158].

$$\tau_{n0} = \tau_{p0} = \frac{\tau_{0\infty}}{1 + N_A / N_{ref}} \quad . \tag{7.3}$$

Where N_{ref} is the measure of dopant-defect interaction. $\tau_{0\infty}$ is the lifetime when there is no dopant-defect interaction. A higher value of N_{ref} implies lower dopant-defect interaction. N_{ref} value of infinity would imply no dopant-defect interaction. Figures 7.20 and 7.21 show the efficiency dependence on resistivity and thickness for lifetimes ($\tau_{0\infty}$) of 25 μs and 250 μs, representing the two extremes in lifetimes observed in cast mc-Si cells. In these calculations an N_{ref} value of 2×10^{16} cm^{-3} was assumed. The data in Fig. 7.19 shows that the lifetime of the low resistivity 0.6 Ω·cm wafers is approximately half the lifetime for 1.5 Ω·cm wafers. Hence an approximate value of N_{ref}, comparable to the base doping is used, which reduces the bulk lifetime by a factor of two. Figure 7.20 shows that for lower lifetime materials (25 μs), cell efficiency improves for lower values of thickness (< 100 μm) and base resistivity (~ 0.5 Ω·cm). On the contrary, for higher lifetime case of 250 μs, the maximum efficiency is shifted to higher values of base thickness (> 300 μm) and there is a broad maxima for doping and thickness (Fig. 7.21). The calculated optimum resistivity for the high lifetime case still remains at ~0.5 Ω·cm. Furthermore from the data in Fig. 7.20, for the thickness and doping ranges studied here,

efficiency lies in the narrow range of 15.5% to 15.7%. For the high lifetime case in Fig. 7.21, when the resistivity swings from 1.5 to 0.6 Ω·cm and thickness swings from 225 to 175 µs, the calculated efficiency swings in the range of 16.5% to 16.8%. This is consistent with the cells fabricated here, supporting that no significant change in efficiency is observed for these wafers when thickness is reduced from 225 µm to 175 µm and doping changed from 1.5 Ω·cm to 0.6 Ω·cm for N_{ref} value of 2×10^{16} cm^{-3}. Results may change for different N_{ref} values.

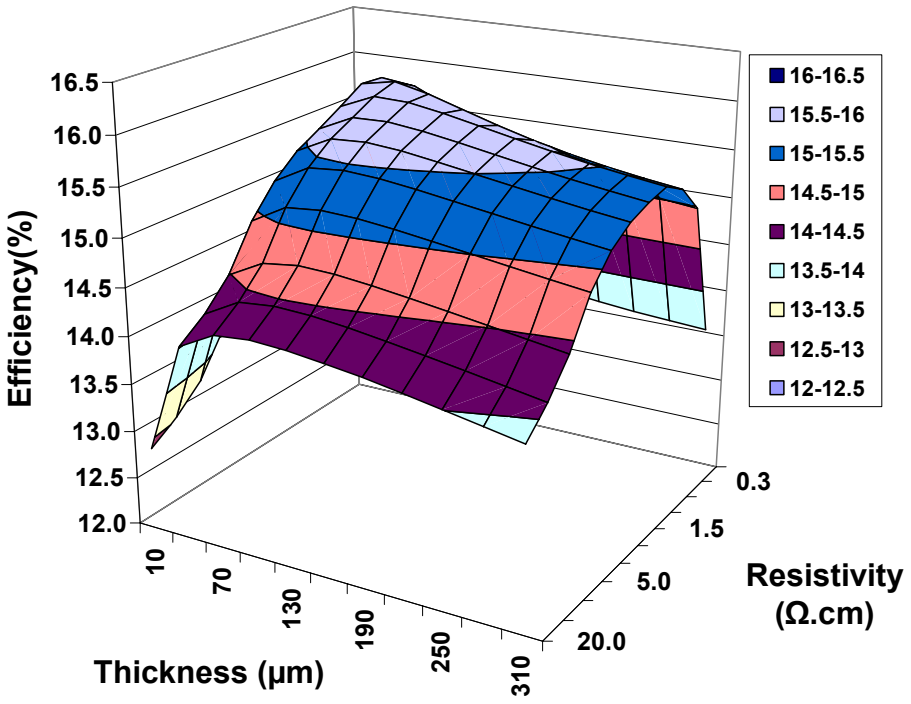


Figure 7.20 Efficiency dependence on resistivity and thickness for bulk lifetime of 25 µs, S_r of 600 cm/s and N_{ref} of 2×10^{16} cm^{-3}.

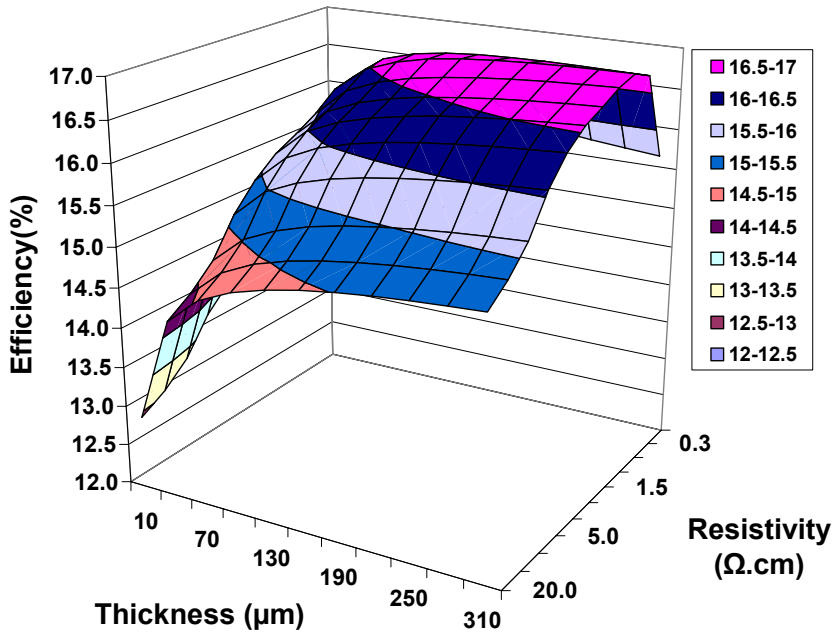


Figure 7.21 Efficiency dependence on resistivity and thickness for bulk lifetime of 250 μs, S_r of 600 cm/s and N_{ref} of 2×10^{16} cm^{-3}.

Further device modeling was performed using an N_{ref} value of infinity (no dopant-defect interaction). The same conclusion was reached regarding thickness but the optimum resistivity decreased to a lower value (~0.3 Ω·cm). Hence dopant-defect interaction has the effect of increasing the optimum base resistivity. An optimum resistivity of 0.5 Ω·cm was found to be true for the set of wafers from this study. This optimum resistivity would however increase or decrease based on the value of N_{ref}.

7.4 Investigation of solar cells fabricated on top, middle, and bottom regions of a novel "mono-cast" HEM Si ingot

A novel method of ingot growth developed at GT Solar [159] is capable of producing single-crystal ingot and wafers using the modified HEM casting technique. Due to the single-crystal nature of these wafers, several of the inherent disadvantages of mc-Si wafers can be avoided. First of all, the mono-cast wafers can be textured with ease,

they are more uniform or homogeneous, and the recombination due to grain boundaries and dislocations is reduced. While still in the optimization stage, *the first two mono-cast p-type, boron doped, ingots* grown by GT Solar have been characterized in this section through lifetime measurements and complete solar cell fabrication.

7.4.1 Characterization of mono-cast HEM ingot 1

The mono-cast HEM ingot wafers from the first ingot were 5 cm × 5 cm, with crystal orientation of <111>. Wafers were sourced from different locations in the ingot and characterized via resistivity and lifetime measurements at different stages of cell processing. Four 4 cm^2 planar solar cells were fabricated on each 5 cm × 5 cm wafer by the baseline process.

Figure 7.22 shows the variation in resistivity of wafers from different locations in the ingot measured by four-point probe. Resistivity varied in the range of 1.81 to 1.07 Ω·cm from the bottom to top of the ingot.

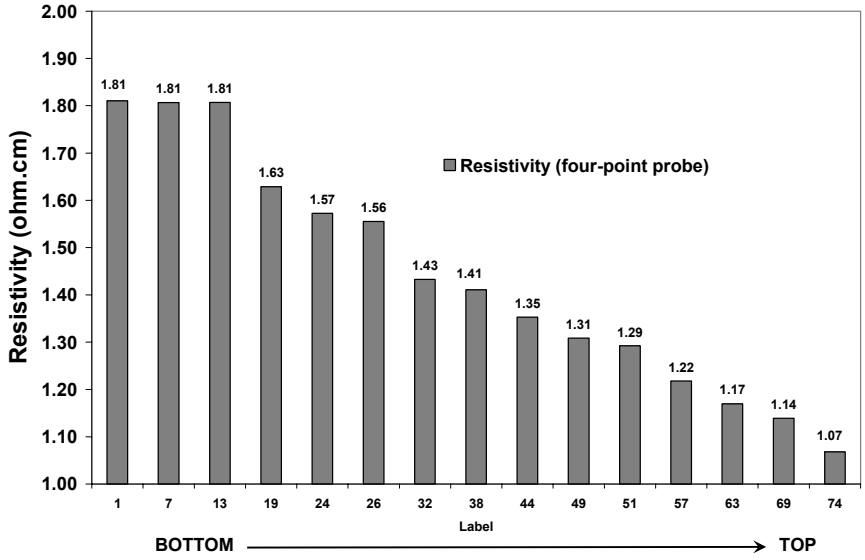


Figure 7.22 Resistivity variation along the length of the ingot for mono-cast ingot 1.

The as-grown, post-diffused and post-fired lifetime was measured to evaluate the quality enhancement. Planar solar cells with a 45 Ω/sq emitter and single layer SiN_x AR coating were fabricated by the baseline fabrication sequence on wafers from different locations along with control FZ samples with resistivities of 1.3 and 2.3 Ω·cm to cover the resistivity variation from the bottom to top region of the mono-cast ingot 1. Table 7.6 shows the I-V results of the planar, screen-printed solar cells fabricated on FZ and mono-cast ingot 1 wafers.

Table 7.6 I-V parameters for planar mono-cast ingot 1 and reference FZ wafers.

Cell ID	Voc	J_{sc}	Eff.	FF	n-factor	R_s	R_{sh}	# cells
	V	mA/cm^2	%			Ω·cm^2	Ω·cm^2	
FZ_1.3 ohm.cm	**0.635**	**33.9**	**16.9**	**78.33**	**1.14**	**0.6**	**150900**	
Average	0.633	33.7	16.7	78.20	1.15	0.6	24765	18
19 (bottom-most)	**0.564**	**28.5**	**12.2**	**75.72**	**1.23**	**0.7**	**19280**	
Average	0.563	28.5	11.7	72.83	1.23	1.4	11168	4
24	**0.566**	**28.1**	**12.1**	**75.85**	**1.21**	**0.7**	**14760**	
Average	0.567	28.0	12.0	75.57	1.29	0.7	12173	4
26	**0.581**	**28.9**	**12.8**	**76.11**	**1.34**	**0.5**	**13640**	
Average	0.577	28.8	12.6	76.09	1.29	0.6	39865	4
32	**0.599**	**30.5**	**13.9**	**75.81**	**1.27**	**0.8**	**23070**	
Average	0.597	30.3	13.7	75.94	1.27	0.7	26855	4
44	**0.619**	**32.7**	**15.2**	**74.92**	**1.29**	**1.0**	**1632**	
Average	0.619	32.7	15.1	74.64	1.22	1.2	10964	3
49	**0.625**	**32.7**	**16.0**	**78.41**	**1.18**	**0.6**	**50110**	
Average	0.623	33.0	15.9	77.23	1.18	0.7	20476	3
57	**0.624**	**33.2**	**15.9**	**76.53**	**1.16**	**0.9**	**5344**	
Average	0.621	33.1	15.6	75.81	1.16	1.0	4653	3
63	**0.623**	**32.2**	**15.5**	**77.29**	**1.22**	**0.7**	**13740**	
Average	0.619	32.3	15.3	76.37	1.22	0.9	8098	3
69 (top-most)	**0.602**	**30.9**	**14.1**	**75.85**	**1.22**	**0.9**	**13410**	
Average	0.594	29.6	13.4	76.03	1.22	0.8	16344	4
FZ_2.3 ohm.cm	**0.634**	**34.4**	**17.0**	**78.01**	**1.16**	**0.7**	**161500**	
Average	0.632	34.1	16.7	77.68	1.18	0.7	90247	18

V_{oc}, J_{sc}, and the efficiency values in the bottom region of the ingot 1 were very low, owing to the impurities incorporated from the crucible during the crystal growth.

Cell efficiencies remained low to ~12% in the bottom section. Efficiency started to increase towards the middle of the ingot reaching ~16%. Efficiency starts to decrease from middle to top. Best efficiency of 14.1% was achieved for solar cells made from the top-most region. Efficiency of the reference FZ wafer solar cell was 16.9% and 17% for the 1.3 and 2.3 Ω·cm resistivity, respectively.

Lifetime was monitored at different stages during the fabrication and is shown in Fig. 7.23, along with the cell efficiencies for wafers sourced across the ingot.

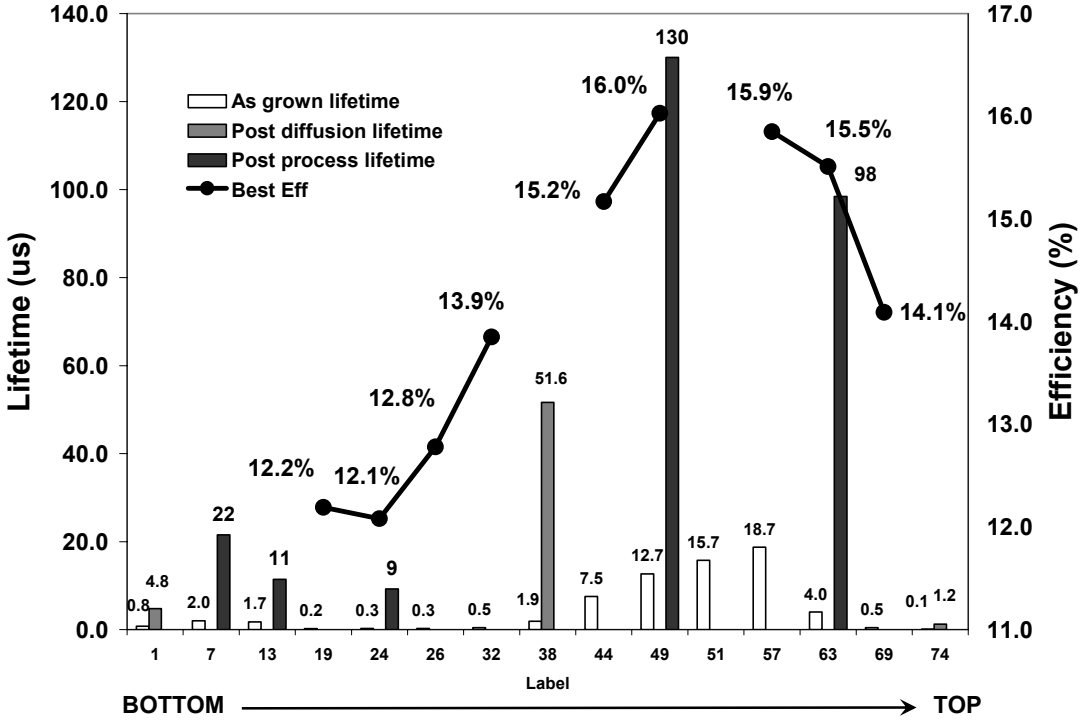
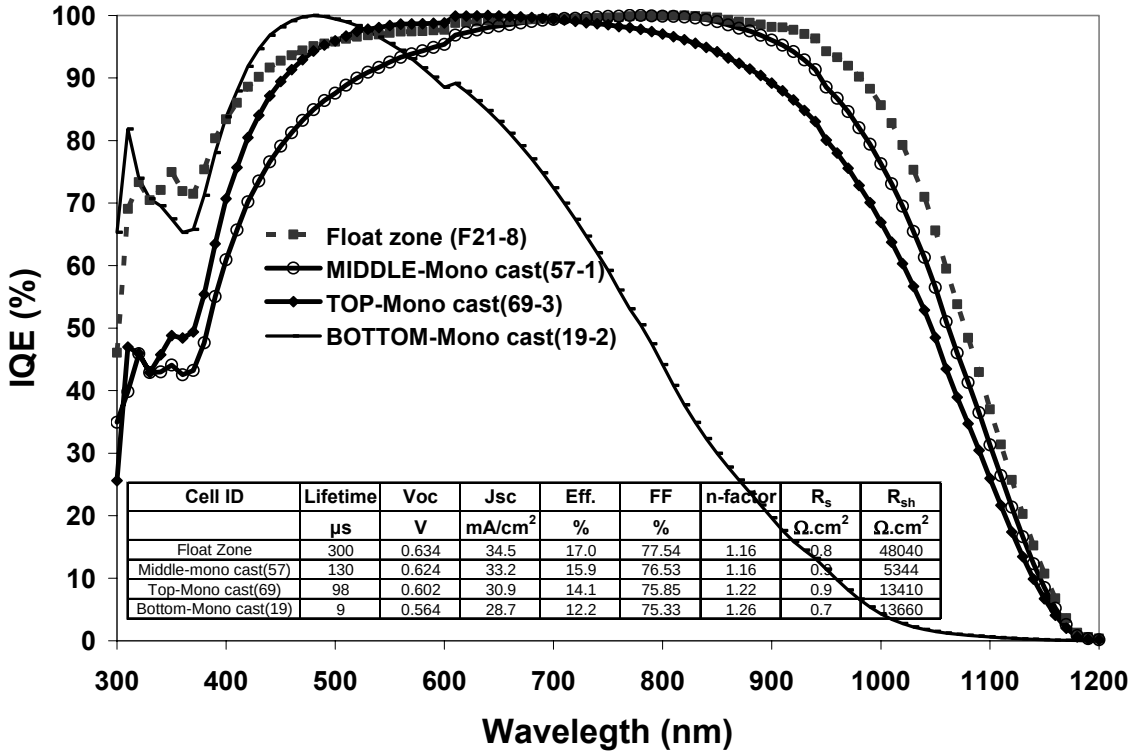


Figure 7.23 Lifetime progress as a function of solar cell processing steps for the mono-cast ingot 1. Also shown is the efficiency of the solar cells fabricated.

For most portion of the ingot, the as-grown lifetime had a low value of <1 μs, except for a small region in the middle and towards the top, where the as-grown lifetime value peaked at 19 μs. Post-diffusion lifetime increased to 4.8, 52, and 1 μs for the bottom, middle and the top region of the ingot, respectively. Post-process lifetime was

measured after stripping of the metal and etching the emitter and the BSF. Lifetime in the bottom region of the ingots remained low in the range of 9 to 22 μs. The middle region of the ingot reached a lifetime value of 130 μs, whereas lifetime in the top region increased to 98 μs. The efficiencies of the solar cells closely followed the post-process lifetime values. It should be noted that the size of the first mono-cast ingot was much smaller than the conventional HEM ingots, as a result contamination from the crucible walls had much greater impact on lowering the lifetime and ingot quality.

Figure 7.24 shows the measured IQE response, along with the I-V parameters and the post-process lifetime for these wafers.



Cell ID	Lifetime	Voc	Jsc	Eff.	FF	n-factor	R_s	R_{sh}
	μs	V	mA/cm^2	%	%		Ω.cm^2	Ω.cm^2
Float Zone	300	0.634	34.5	17.0	77.54	1.16	0.8	48040
Middle-mono cast(57)	130	0.624	33.2	15.9	76.53	1.16	0.9	5344
Top-Mono cast(69)	98	0.602	30.9	14.1	75.85	1.22	0.9	13410
Bottom-Mono cast(19)	9	0.564	28.7	12.2	75.33	1.26	0.7	13660

Figure 7.24 IQE response for the solar cells from top, middle, and bottom regions of the mono-cast ingot and for the 2.3 Ω·cm FZ wafer. Also shown are the I-V parameters and the post-process lifetimes.

The IQE response of the solar cells is consistent with the cell efficiencies and the lifetime values. The cell from the bottom-most region had very low lifetime and low V_{oc} of 564 mV, resulting in a very poor IQE response. High-lifetime FZ wafer had the best efficiency and IQE, as expected.

7.4.2 Characterization of mono-cast HEM ingot 2

Mono-cast ingot 2 was grown somewhat larger in size with a crystal orientation of <100>. Ingot size was 19 cm × 19 cm × 8.4 cm from which 10 cm × 10 cm wafers were cut at different locations for characterization and solar cell processing. Due to the <100> crystal orientation, the wafers could be easily textured to reduce reflectance and increase light trapping. Nine 4 cm^2 solar cells were fabricated on each 10 cm × 10 cm wafer from different locations in the ingot. Large area (100 cm^2) solar cells were also fabricated from wafers in the middle region.

7.4.2.1 Small area (4 cm^2) solar cell fabrication and characterization

Figure 7.25 shows the resistivity variation for wafers along the ingot length.

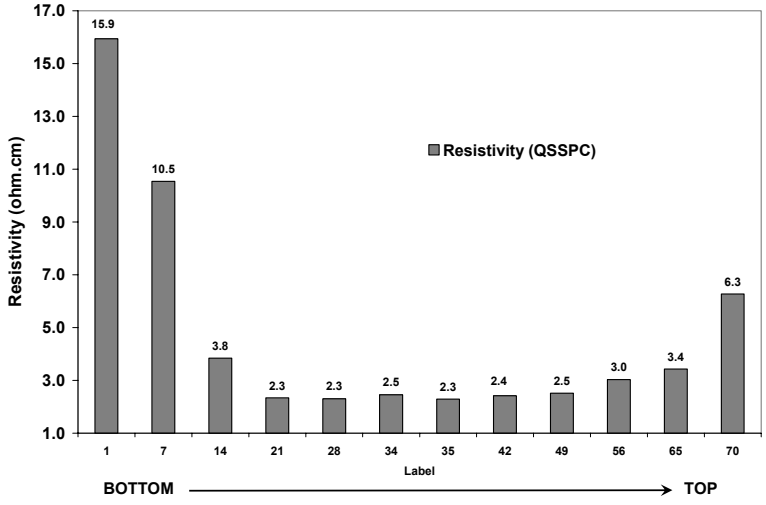


Figure 7.25 Resistivity variation along the length of the ingot for mono-cast ingot 2.

The resistivity varied in the range of 2.3 to 3.0 Ω·cm for most part of the ingot, except for the some regions in the bottom and top, where it increased to unusual values.

As-grown, post diffused and post-fired lifetimes were measured. All wafers were textured by the standard KOH/isopropyl texturing process used for the single-crystal Si. Textured solar cells were fabricated with ~45 Ω/sq emitter and single layer SiN_x AR coating from different locations along with the control FZ control FZ with a resistivity of 1.3 Ω·cm. Table 7.7 shows the I-V results of the solar cells fabricated on textured FZ and mono-cast ingot 2 wafers.

Table 7.7 I-V parameters for solar cells on textured mono-cast ingot 2 and textured reference FZ wafer.

Cell ID	Voc	J_{sc}	Eff.	FF	n-factor	R_s	R_{sh}	# cells
	V	mA/cm^2	%			Ω·cm^2	Ω·cm^2	
FZ_1.3 Ω·cm	**0.633**	**37.4**	**18.2**	**76.82**	**1.22**	**0.7**	**32720**	
Average	0.633	37.3	17.9	75.90	1.24	0.8	681974	18
7 (bottom_most)	**0.551**	**33.5**	**14.0**	**75.65**	**1.18**	**0.7**	**165200**	
Average	0.554	32.7	13.2	73.03	1.34	0.9	71433	4
21	**0.618**	**35.3**	**15.9**	**72.76**	**1.51**	**1.0**	**98350**	
Average	0.606	34.5	15.2	72.94	1.42	1.1	53751	7
28	**0.622**	**36.1**	**17.2**	**76.55**	**1.21**	**0.7**	**49150**	
Average	0.622	35.9	17.0	76.04	1.22	0.8	125260	6
31	**0.624**	**35.9**	**17.1**	**76.45**	**1.36**	**0.5**	**115200**	
Average	0.622	35.8	16.8	75.47	1.42	0.6	39115	9
32	**0.625**	**36.2**	**17.1**	**75.47**	**1.40**	**0.6**	**14170**	
Average	0.623	35.9	16.8	75.03	1.41	0.7	64745	7
34	**0.624**	**35.8**	**17.1**	**76.55**	**1.25**	**0.7**	**27690**	
Average	0.623	35.8	17.0	76.05	1.28	0.7	37765	6
49	**0.623**	**35.7**	**17.0**	**76.27**	**1.38**	**0.6**	**161500**	
Average	0.616	35.3	16.3	75.06	1.40	0.7	64916	5
56	**0.624**	**36.0**	**16.6**	**74.11**	**1.41**	**0.9**	**17050**	
Average	0.617	35.2	15.2	70.17	1.43	1.6	605037	6
65 (top-most)	**0.582**	**32.9**	**14.7**	**76.67**	**1.23**	**0.6**	**19790**	
Average	0.577	32.7	14.3	75.75	1.21	0.8	23743	7

Bottom region of the ingot suffered from impurities and low lifetime, resulting in low efficiency of 14% and a V_{oc} of 551 mV. The middle of the ingot gave an efficiency

peak at 17.2%. The cell efficiency decreased to 14.7% near the top. Efficiency was in a tight range of 17.0-17.2% for a broad range near the middle of the ingot. Best efficiency for the 1.3 Ω·cm textured FZ was 18.2%.

Figure 7.26 shows that the maximum as-grown lifetime value was 2.8 μs.

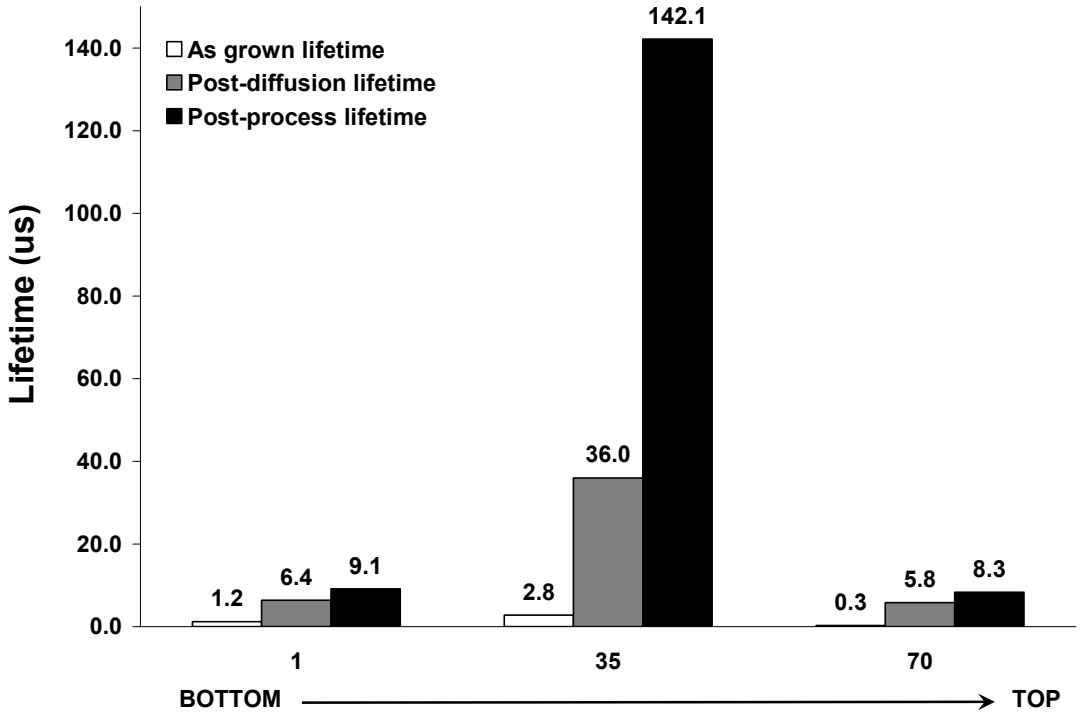
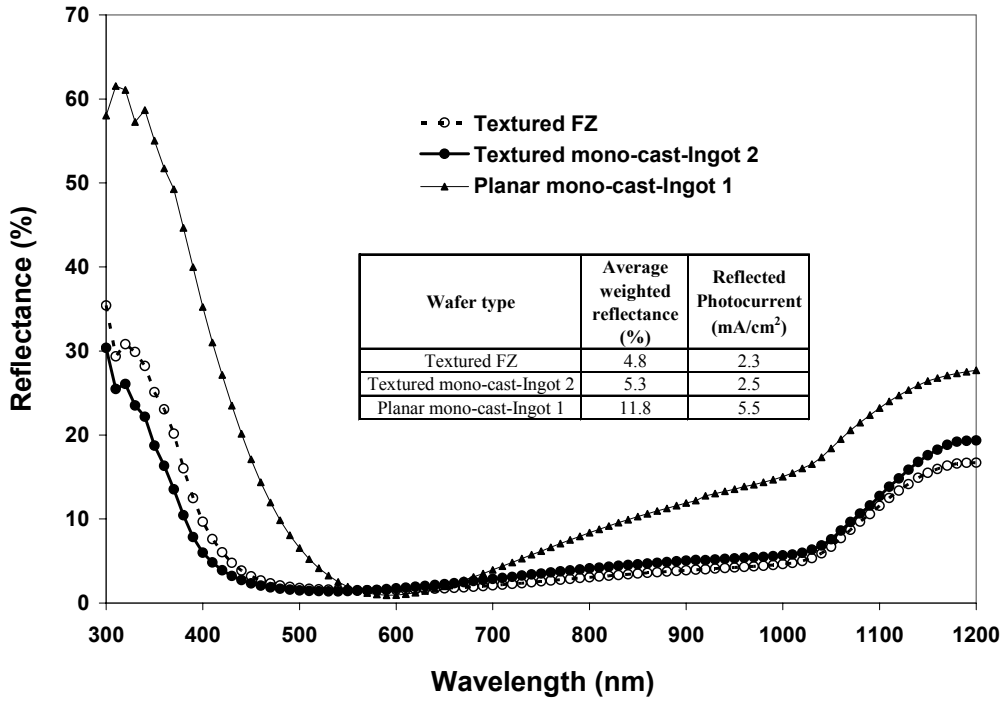


Figure 7.26 Lifetime progress as a function of solar cell processing steps for the mono-cast ingot 2.

After diffusion, lifetime increased to > 5 μs for the top and bottom regions while the middle section went up to 36 μs. Post-processing lifetimes were measured on cells ID: 7 (bottom-most), 32 (middle), and 65 (top-most) from Table 7.7, to get a range for the lifetime potential for this material. The lifetimes in the top- and bottom-most regions remained below 10 μs even after firing or hydrogenation, consistent with the low V_{oc} and J_{sc} of those cells (Table 7.7). The middle region, however, recovered from the low as-

grown lifetime value of 3 μs to 142 μs, after SiN_x-induced hydrogenation, consistent with >17% efficiency.

Although the mono-cast growth process is still in the optimization phase, a high efficiency of 17.2% shows the potential of this novel material. The J_{sc} for the textured cells of ingot 2 was 3.4 mA/cm^2 higher than the planar cells of ingot 1, resulting in 1.2% absolute increase in the efficiency. This highlights the importance of effective texturing of mono-cast to achieve high efficiency solar cells. Figure 7.27 shows the reflectance of the SiN_x coated textured FZ, planar mono-cast, and textured mono-cast wafers. The average weighted reflectance for the textured mono-cast cell is 5.3% compared to 11.8% for the planar wafers, which accounts for the increase of ~ 3 mA/cm^2 in the J_{sc} of the textured mono-cast cells.



Wafer type	Average weighted reflectance (%)	Reflected Photocurrent (mA/cm^2)
Textured FZ	4.8	2.3
Textured mono-cast-Ingot 2	5.3	2.5
Planar mono-cast-Ingot 1	11.8	5.5

Figure 7.27 Reflectance comparison of the textured wafers from ingot 2 and the planar wafer from ingot 1.

7.4.2.2 Large area (100 cm^2) solar cell fabrication and characterization

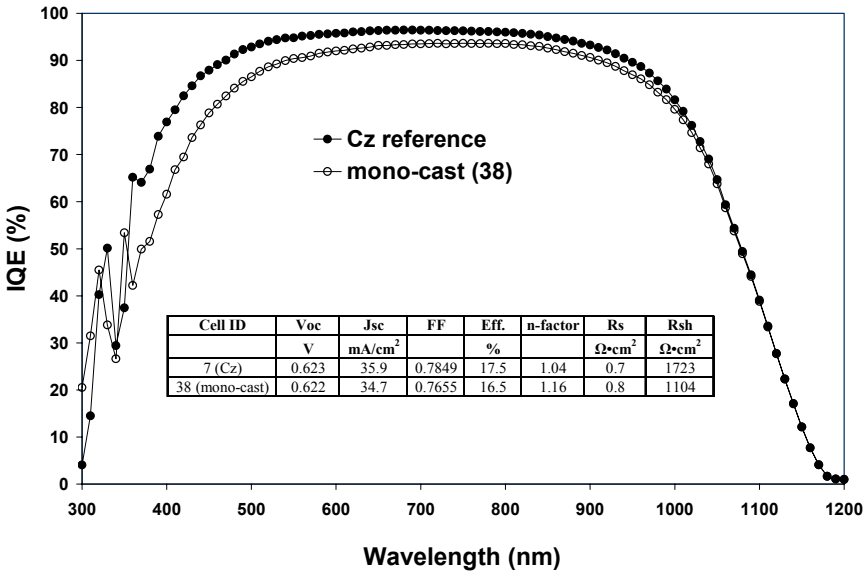
Due to the inherent inhomogenity in the HEM mc-Si wafers, fabrication of the large area solar cells leads to some loss in performance. This loss is expected to be smaller in the mono-cast wafers. Large area solar cells were fabricated on the 10 cm × 10 cm textured mono-cast wafers. Table 7.8 summarizes the I-V results for the textured mono-cast wafers from the middle region of the ingot, along with reference Cz solar cells.

Table 7.8 Large area, 100 cm^2, solar cell I-V parameters for solar cells on textured mono-cast ingot 2 and textured reference Cz wafers.

Cell ID	Resistivity	Voc	Jsc	FF	Eff.	n-factor	R_s	R_{sh}
	Ω·cm	V	mA/cm^2		%		$Ω·cm^2$	$Ω·cm^2$
GiTCz-1	1.80	0.623	36.1	0.773	17.4	1.10	0.8	2482
GiTCz-5	1.71	0.623	35.7	0.773	17.2	1.12	0.7	2107
GiTCz-7	**1.71**	**0.623**	**35.9**	**0.785**	**17.5**	**1.04**	**0.7**	**1723**
GiTCz-9	1.83	0.622	35.4	0.779	17.2	1.08	0.7	2001
GiTCz-10	1.34	0.626	35.3	0.780	17.2	1.08	0.7	1698
Mono-cast-29	2.25	0.621	34.9	0.754	16.3	1.32	0.8	608
Mono-cast-38	**2.26**	**0.622**	**34.7**	**0.766**	**16.5**	**1.16**	**0.8**	**1104**
Mono-cast-41	2.18	0.624	34.3	0.766	16.4	1.15	0.9	1115

An efficiency of 16.5% was achieved on the mono-cast wafer, compared to 17.5% for the reference Cz wafer. Most of the difference in efficiency came from the loss in J_{sc} of ~1.2 mA/cm^2 for the mono-cast cells. To explain the observed loss in J_{sc}, IQE measurements were performed. Figure 7.28 shows the IQE comparison of the Cz and mono-cast cells.

Long wavelength IQE is similar for the two cells, indicating a similar Al-BSF quality. There is a considerable difference in the short wavelength IQE which accounts for most of the loss in J_{sc}. Further optimization of the emitter and the front surface passivation should result in the reduction of this gap between the Cz and mono-cast cells.



Cell ID	Voc	Jsc	FF	Eff.	n-factor	Rs	Rsh
	V	mA/cm^2		%		Ω•cm^2	Ω•cm^2
7 (Cz)	0.623	35.9	0.7849	17.5	1.04	0.7	1723
38 (mono-cast)	0.622	34.7	0.7655	16.5	1.16	0.8	1104

Figure 7.28 IQE comparisons for the 100 cm^2, textured reference Cz wafer and the mono-cast wafer.

7.5 Conclusion

Screen-printed solar cells were fabricated on different regions of four ingots from different suppliers. High post-diffusion and post-hydrogenation lifetime values were obtained for most of the wafers. This study shows that the top region of the ingot generally benefits most from the gettering during the phosphorous diffusion used to form the n^+ emitter and the bottom region benefits most from the hydrogenation from the SiN_x film during the contact firing cycle. The middle region benefits from both. Lifetime values as high as 0.3 ms were achieved for the middle region of two boron-doped ingots and the gallium-doped ingot used in this study. These high lifetime values translated into high screen printed cell efficiencies of ≥ 15.9% for wafers from all the regions and ingots, except for the bottom region of the lower-resistivity boron-doped ingot and the gallium-doped ingot. Using a lower-resistivity boron-doped mc-Si ingot did not seem to improve the efficiency. As expected, the concentration of oxygen in the three boron-doped ingots

was found to increase from top to bottom and at a concentration of 14 ppm in a 2 Ω·cm resistivity wafer, LID of about 2.5% (relative) in efficiency was observed. A relatively tighter and superior distribution in efficiency was found for the boron-doped ingot compared to the gallium-doped ingot. However, the gallium-doped ingot was found to be very stable under illumination, irrespective of the location of the wafer in the ingot. Device modeling showed the merits of tailoring the thickness, based on the doping and the bulk lifetime in the solar cell, aimed at achieving a more uniform and optimized efficiency distribution for the entire ingot. In general, thinner wafers with good BSRV can reduce the impact of resistivity and lifetime variations in the mc-Si ingot.

Solar cells were fabricated on wafers from top, middle, and bottom regions of cast multicrystalline silicon ingots with resistivities of 1.5 Ω·cm and 0.6 Ω·cm and thicknesses of 225 μm and 175 μm from the same supplier. A standard manufacturable industrial cell fabrication process was used involving screen-printing of front and back contacts. The expected increase in the performance with increased doping was not realized, however, V_{oc} enhancement was observed for the lower resistivity cells despite significantly lower bulk lifetimes compared to higher resistivity cells. The low lifetime in the low resistivity ingot was attributed to the dopant-defect interaction, which lowered the lifetime in mc-Si. After gettering (during P diffusion) and hydrogenation (from SiN_x) steps used in cell fabrication, the bulk lifetime in 225 μm thick wafers from the middle of the ingot decreased from 253 μs to 135 μs when the resistivity was lowered from 1.5 Ω·cm to 0.6 Ω.cm. An increase in the average V_{oc} of up to 4 mV was observed on decreasing the base resistivity, which was counterbalanced by the loss in lifetime and J_{sc}. This study shows that solar cells fabricated on 175 μm thick, 1.5 Ω·cm, wafers showed no appreciable loss

in the cell performance when compared to the 225 μm thick cells, consistent with PC1D modeling. Device modeling revealed that an optimum thickness occurs at lower thickness and lower resistivity for low bulk lifetime wafers. For higher bulk lifetime wafers, an optimum still occurs at lower resistivities, but is shifted to higher thickness. Device modeling also showed that the dopant-defect interaction has the effect of increasing the optimum base resistivity to higher values.

Solar cells fabricated on the first two ingots grown by a novel process, which produced single-crystal Si wafers by HEM casting method, achieved efficiencies of 16% and 17.2% on planar and textured surfaces. Lifetime in the middle region of both the ingots exceeded 100 μs after cell processing; however top and bottom regions had lower lifetimes due to the impurities that could not be gettered or passivated. Due to the single-crystal nature of the mono-cast ingots, the wafers were textured easily, which decreased the front surface reflectance from 11.8 to 5.3% and resulted in an enhanced J_{sc} by ~3 mA/cm^2. Large area (100 cm^2) solar cells fabricated from the middle regions of this novel mono-cast material achieved an efficiency of 16.5%. The mono-cast grown by the HEM process is still under optimization, however, these results show that this growth technique has a great potential for achieving high-efficiencies at a lower cost and bridging the efficiency gap between cast and Cz methods.

CHAPTER 8

THIN CRYSTALLINE SILICON SOLAR CELLS WITH FULL AREA ALUMINUM-BACK SURFACE FIELD

8.1 Introduction

The influence of reducing the thickness of multi- and mono-crystalline silicon wafers on the performance and cost of screen-printed solar cells with full area aluminum-back surface field (Al-BSF) has been investigated. First, in section 8.2, a literature review of the solar cell efficiencies on thin Si is presented along with the benefits of using thinner Si. Device modeling is performed in section 8.3 to assess the impact of reducing wafer thickness for low- and high- lifetime c-Si solar cells. Section 8.4 lists the five sets of wafers analyzed to study the impact of thickness reduction. This section also discusses the importance of adjusting the belt co-firing profiles to assess accurately the impact of thickness reduction on cell performance. I-V and IQE results for the five sets of wafers, along with the lifetime measurements and PC1D modeling of the cell data is presented in section 8.5. Section 8.6 identifies the critical parameters that can improve the performance of thin cells. Finally, cost modeling is performed in section 8.7 to calculate the impact of reducing the wafer thickness on the total module manufacturing cost.

8.2 Review of solar cell efficiencies on thin crystalline Si and the benefits of using thin Si

Silicon (Si) accounts for about 50% of the cost of current Si solar cell modules, therefore, the cost of Si PV can be reduced significantly by using thinner silicon substrates. Current silicon feedstock shortage and high cost has expedited the need for thinner substrates. Current industry standard is 200-250 μm thick substrates as compared

to 275-300 μm thick substrates couple of years ago. Cost calculations by Münzer, et al., showed that 50 μm reduction in wafer thickness can result in ~5% cost reduction ($/W), which can be reduced further by improving the yield [160]. Silicon is a poor light-absorber, therefore, thinner cells generally produce lower efficiencies due to the reduced short-circuit current density (J_{sc}). This loss can be mitigated by a more effective light trapping, back-surface passivation, and back surface reflectance (BSR) compared to the conventional full Al-BSF cells. Zhao, et al., demonstrated that excellent optical and electrical confinement in a ~50 μm thin Si can produce 21.5% PERL cells. Kray, et al., reported 20.1% RP-PERC cells on 37 μm thick Si substrate with a BSRV of 120 cm/s and BSR of ~98% [161]. Ristow, et al., showed that screen-printed silver paste on thin silicon nitride dielectric layers can produce BSR values in excess of 98% [162]. Certain cell structures like the EWT cells are well suited for thin, lower lifetime Si wafers, because EWT structure enables carrier collection from both surfaces. Glunz, et al., showed a high J_{sc} value of 40.6 mA/cm^2 in 235 μm thick EWT cells with diffusion length of only 187 μm [163]. For an efficient carrier collection with certain other cell structures such as the rear contact cells [164], either the diffusion length should be large or the cells should be very thin if the material quality is low. Glunz, et al., showed strong degradation of 28.8% relative for rear contact cells as compared to a degradation of only 1.8% for the EWT cells [163]. Thinner cells can also reduce LID in Si cells [160, 165, 166]. Kray, et al., showed a significant reduction in diffusion length from 778 μm to 187 um due to LID in a 132 μm thick 0.8 Ω.cm Cz cell, but the efficiency loss was only 0.2%, compared to 1.6% loss in efficiency for 250 μm thick wafer [167]. They observed no degradation due to LID in 36 μm, 0.8 Ω.cm boron-doped Cz wafers [161]. Steckemetz, et al., also

reported smaller loss in efficiency as thickness is reduced [168]. This is because for low diffusion length wafers, minority carrier electrons generated at the rear of the cell have a higher probability of collection in thinner cells. Thus, there are several direct and indirect benefits of using thin wafers. Direct benefits include a) reduced material/module-manufacturing cost ($/wafer), b) increased manufacturing output (grams of Si/wafer), and c) enhanced performance from certain cell structures with good light trapping and BSRV. The indirect benefits include a) reduced light-induced degradation, b) better utilization of lower quality material, and c) easier adoption of some advanced cell structures like back contact and emitter wrap through (EWT) solar cells. There are, however, several challenges in using thin wafers, such as a) reduced yield, b) wafer bowing or warping due to contact firing of full area Al-BSF, and c) reduced mechanical stability due to surface texturing. Bowing not only reduces the mechanical yield during cell production but also during module manufacturing. Some of these challenges can be overcome by appropriate cell designs and processing so that the advantages of reduced thickness can be harnessed. Yield enhancement can be achieved by going down the learning curve over time [169] and by the development of suitable equipment. In the current study the yield issue has been neglected since that requires statistical analysis on the production line. Emphasis is placed on the change in cell performance when thickness is reduced. Bowing can be partly mitigated by using the special low bow aluminum paste; however, it often degrades the quality of Al-BSF and cell performance. Therefore adjustments to the conventional cell processing are necessary as the thickness is reduced below 200 μm [140, 157, 160, 170-173]. Table 8.1 lists, in chronological order, the efficiencies achieved on various thicknesses of c-Si solar cells in recent years.

Table 8.1 Solar cell efficiencies on c-Si of reduced thickness from recent years.

Authors	Year	Efficiency (%)	Thickness (μm)	Area (cm^2)	Material	Structure	Comments
Münzer, et al., [160]	1999	17.2	150	100	Cz	Boron BSF; Dry oxide 20-40 nm	
Finckenstein, et al., [174]	2000	15.2	180	100	mc-Si	Full area Al-BSF	14.1% for back contact, fired through SiN_x
Warta, et al., [166]	2000	20.2	165	4	Cz	RP-PERC	Acid texture
		20	115				
Bruton, et al., [169]	2000	14.6-17	160-313	-	Cz	LGBC	Poor Al-BSF
		16.9	140	100			Improved BSF
Kray, et al., [167]	2001	18.4	132	-	Cz	RP-PERC	
		20.5	109		FZ		
		20.5	72		FZ		
Steckemetz, et al., [168]	2001	15.2	300	4	Cz	Textured; Rear contact fired through SiN	Screen-printed contacts; co-firing
		15.1	200				
		15	100				
		16.8	300		FZ		
		16.6	200				
		15.6	100				
Mittelstädt, et al., [157]	2002	15.1	300	4	mc-Si	Full area Al-BSF	Rear contact through SiN_x opened with mechanical abrasion and evaporated Al
		14.9	200				
		13.9	100				
		15.5	300			SiN_x rear	
		15.7	200				
		14.9	100				
Schneider, et al., [175]	2002	15.1	200	156	mc-Si	Full area Al-BSF	
Tool, et al., [171]	2002	12.4-13.5	150-325	100			
Duerinckx, et al., [172]	2004	16.7	200	100			Textured DLAR
Glunz, et al., [176]	2004	20.2	37	-	-	LFC	Resistivity of 0.25 Ω·cm
Kray, et al., [161]	2004	19	36	-	Cz	LFC	Resistivity of 0.8 Ω·cm
		20.4	65		FZ		Resistivity of 0.1 Ω·cm
		20.1	37		FZ		Resistivity of 0.25 Ω·cm
		19.6	34		FZ		Resistivity of 0.5 Ω·cm
Le Quang, et al., [177]	2004	15.3	150	156	mc-Si	Al back connected by grid pattern	36 cell module efficiency
Schneiderlöchner, et al., [178]	2004	17.7	170	100	FZ	LFC	
		16.4	170	100	FZ	Full area Al-BSF	
		17.7	170	147	FZ	LFC	
Schultz, et al., [179]	2004	20.3	99	1	mc-Si	LFC	Textured; DLAR; wet oxide
Tool, et al., [180]	2004	14.2	175	100	mc-Si	Full area Al-BSF	Acid texture

Agostinelli, et al., [181]	2005	16	180	100	mc-Si	i-PERC	
		17.2	180	100	Cz		
		16.5	160	156	Cz		
Bähr, et al., [182]	2005	14.4	200	243	mc-Si	Full area Al-BSF	
		13.9	100				
Janβen, et al., [183]	2005	14.4	180	-	mc-Si	Full area Al-BSF	
		14.7				Al grid fired through SiN on back	Grid pattern on back
Kränzl, et al., [184]	2005	15.6	200	100	mc-Si	Boron BSF	BBr3 open tube diffusion
Sánchez-Friera, et al., [185]	2005	13.3	200	-	mc-Si	BBr3 + Phosphorous BSF	n-type
Schindler, et al., [173]	2005	14.2	200	450	mc-Si	Al grid fired through SiN on back	Very large area
Agostinelli, et al., [186]	2006	16.6	180	Full area Al-BSF	mc-Si	i-PERC	
		15.6				Full area Al-BSF	
		16.1	150			i-PERC	
		15.1				Full area Al-BSF	
		17.6	130		Cz	i-PERC	
		16.2				Full area Al-BSF	
		17.3	105			i-PERC	
		15.1				Full area Al-BSF	
Janβen, et al., [187]	2006	15	180	-	mc-Si	Al grid fired through SiN_x on back	
		14.4				Full area Al-BSF	
Mason, et al., [188]	2006	20.1	140	149	FZ	LGBC/LFC	

This chapter focuses on the loss in performance incurred when the cell thickness is reduced for the conventional cell structure with full area Al-BSF and screen-printed contacts. In addition to quantifying the loss in performance, guidelines are presented to enhance the performance of thin cells. Finally, cost analysis is performed to see the tradeoff between thickness and performance reduction using traditional cell processing.

8.3 Device modeling to assess the impact of thickness reduction on cell performance as a function of bulk lifetime

Impact of thickness is a strong function of material quality, technology and cell design. In this study, device modeling is performed using the PC1D program [130] to assess the effect of thickness reduction on the performance of a simple screen-printed n^+-p-p^+ solar cell with full area Al-BSF.

Figures 8.1 (a) and (b) show the PC1D modeled effect of reducing the wafer thickness on V_{oc} of planar solar cells for a low and a high quality substrate, respectively. These calculations were performed as a function of BSRV. Figure 8.1 (a) shows that for a low quality Si with bulk lifetime of 25 μs, thickness reduction below 300 μm results in higher V_{oc}, for BSRV values up to 1000 cm/s. Improvement in V_{oc} due to thickness reduction decreases as BSRV increases. For high-lifetime wafers (τ = 200 μs, Fig. 8.1(b)), reducing the cell thickness leads to V_{oc} enhancement only if the BSRV is below 300 cm/s. These trends can be explained on the basis of relative magnitudes of diffusion velocity of the material ((D/L where D is the diffusion constant for minority carriers and L is the diffusion length of base) and the BSRV.

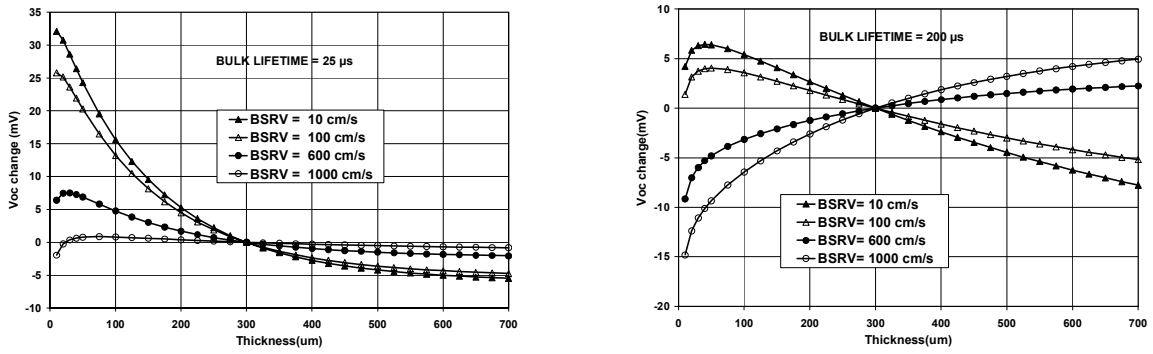


Figure 8.1 Change in V_{oc} as a function of cell thickness for different BSRVs with lifetime of (a) 25 μs and (b) 200 μs.

When BSRV > D/L, V_{oc} decreases with thickness reduction and vice versa. Figure 8.2 shows a plot of critical BSRV (= D/L) as a function of material quality (L) and resistivity (which also alters the D value). If the cell technology cannot produce the critical BSRV for a given τ and resistivity of the material, then thickness reduction will hurt the performance. For example, for a Si substrate with bulk lifetime of 100 μs and resistivity of 1.5 Ω.cm, cell technology should provide a BSRV of 536 cm/s or lower to achieve V_{oc} enhancement from thickness reduction.

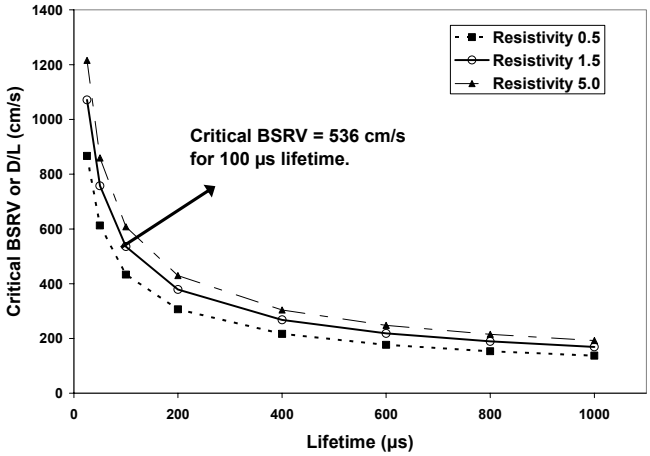


Figure 8.2: The critical value of BSRV = D/L below which an increase in V_{oc} can be observed on reducing the thickness. Resistivity values of 0.5, 1.5 and 5.0 Ω.cm are shown.

Silicon has a low absorption coefficient, which results in low light absorption, especially in the long wavelength, resulting in a lower J_{sc} and hence the need for thicker wafers. Additional device modeling reveals a drop in J_{sc} with thickness reduction, for high lifetime (>150 μs) wafers, irrespective of the BSRV value for both planar and textured front surfaces. For low lifetime (<25 μs) cells, a loss in J_{sc} is observed for BSRV values >400 cm/s (eg., for Al-BSF), but an increase in J_{sc} is observed for lower values of BSRV. Change in J_{sc} with thickness reduction dominates the increase or decrease in the efficiency of the solar cells. Thus, even for very low BSRV values, a loss in efficiency

could occur in high lifetime thin wafers due to the loss in J_{sc}, unless effective light-trapping schemes are utilized.

8.4 Experimental

8.4.1. Material selection and cell fabrication to understand and quantify the impact of thickness reduction

The wafers used were p-type boron doped, mono- and mc-Si. All HEM mc-Si wafers used in this work had a reasonably good as-grown lifetime (30-83 μs), measured by Quasi-Steady-State Photo-conductance (QSSPC) technique [88], with the surface passivated in iodine-methanol solution [189]. Lifetimes were measured at an injection level of 1 x 10^{15} cm^{-3} at various locations in the case of mc-Si, wafers and an average lifetime value is reported. The following five sets of wafers were analyzed:

- Set 1 had HEM wafers with an average as-grown lifetime of 41 μs and were from the same ingot region. These wafers were ground down from one side to obtain wafer thicknesses of 115, 150, 175, 225, and 280 μm. The resistivity for this set of wafers was ~1.3 Ω·cm, and the sheet resistance of the diffused emitter layer was ~45 Ω/sq.
- Set 2 had 1.3 Ω·cm FZ silicon wafers which were ground down to thicknesses of 115, 150, 175, 225, and 280 μm prior to cell fabrication. FZ wafers were used as a reference to observe the effect of thickness reduction on high lifetime material with no lifetime inhomogenity. The emitter sheet resistance was ~45 Ω/sq for these cells.
- Set 3 wafers were fabricated to evaluate the benefit of texturing on thickness reduction. Cells were fabricated on 1.3 Ω·cm textured FZ material for three

different thicknesses of 125, 210, and 300 μm, with emitter sheet resistance of ~45 Ω/sq.

- Set 4 wafers were used to assess the impact of thickness reduction on the cells with high emitter sheet-resistance. Cells were fabricated on 1.3 Ω·cm textured FZ material for three different thicknesses of 125, 210, and 300 μm with emitter sheet resistance of ~80 Ω/sq.
- Finally, in set 5, cells were fabricated on 115 and 150 μm thick HEM mc-Si wafers with emitter sheet resistance of ~85 Ω/sq. These wafers were from different ingots than the wafers in set 1 and were sawn directly to their respective thicknesses from the ingots.

Planar wafers used in this study first were etched chemically in acid to remove surface damage followed by RCA cleaning. Wafers were then diffused using liquid $POCl_3$ as the dopant source to form the n^+-p junction. As discussed in CHAPTER 7, this also serves as a gettering step, which often enhances lifetime in mc-Si wafers. After the $POCl_3$ diffusion, wafers were coated with SiN_x film deposited in a direct low frequency PECVD reactor. Nine 4 cm^2 solar cells were fabricated on each wafer by screen printing aluminum on the back and silver grid on the front. Screen-printing was performed in a semi-automatic screen printer, which adjusted the print parameters depending on the wafer thickness. This minimized the variation in the print quality. The cells were then co-fired using an optimized process in a lamp-heated IR belt furnace, resulting in the simultaneous formation of an Al-BSF [190] on the rear and the Ag grid contact on the front. Finally, cells were isolated with a dicing saw and annealed at 400 °C for 15 min in forming gas before testing and analysis. The post-diffusion lifetimes were measured after

etching off the emitter and the post-processing cell lifetimes were measured after chemically stripping off the metal and then etching the emitter on front and the BSF layer on the back.

8.4.2 Belt firing adjustment to maintain the same temperature profile for each thickness

By virtue of lower mass, thinner wafers heat up and cool down faster. In addition, textured wafers reach a higher peak temperature compared to planar wafers for the same firing condition in belt. Finckenstein, et al., suggested that thinner wafers must be fired at higher belt speeds [174]. However, the precise variation in firing conditions on different cell thickness and on textured surfaces was not taken into account. This is true for most of the work in literature. In this study we used the datapaq to precisely monitor the peak temperature as seen by the wafer surface during the firing cycle. Figure 8.3 shows the firing profiles for wafers with varying thickness and for a high belt speed furnace setting. Figure 8.4 shows the effect of thickness on the peak firing temperature for fixed belt zones settings. It is interesting to note that a 115 μm thick wafer sees ~70 °C higher temperature than the 280 μm thick wafer for the same setting of the belt furnace. Figure 8.5 shows the effect of varying the belt speed on the peak firing temperature. As expected, higher belt speed leads to a larger difference in the peak temperatures of the thin (115 μm) and the thick (280 μm) wafers. It should also be pointed out that a high belt speed is desirable to form good quality BSF and for more effective hydrogenation of bulk.

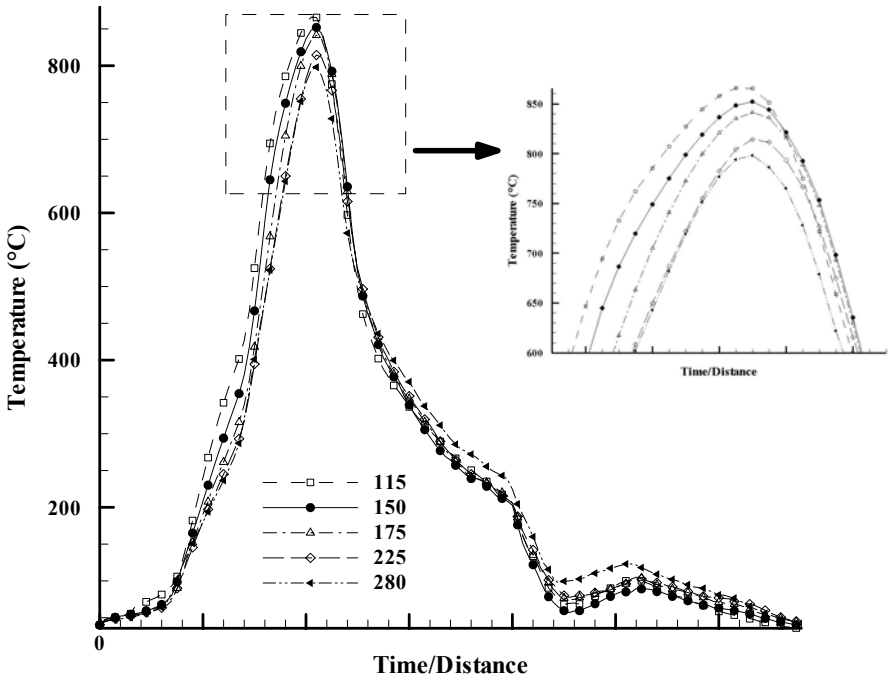


Figure 8.3 Belt firing profiles for different thicknesses show that for the same temperature setting in the furnace, thinner wafers heat and cool down faster than the thick wafers.

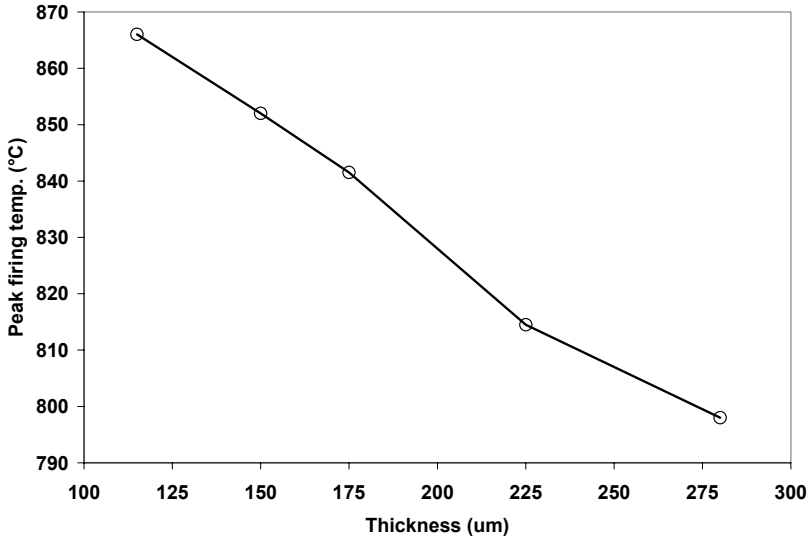


Figure 8.4 Peak firing temperature as "seen" by wafers of different thicknesses for high belt speed. For the same temperature settings, a 115 µm thick wafer sees ~70 °C higher temperature than a 280 µm thick wafer.

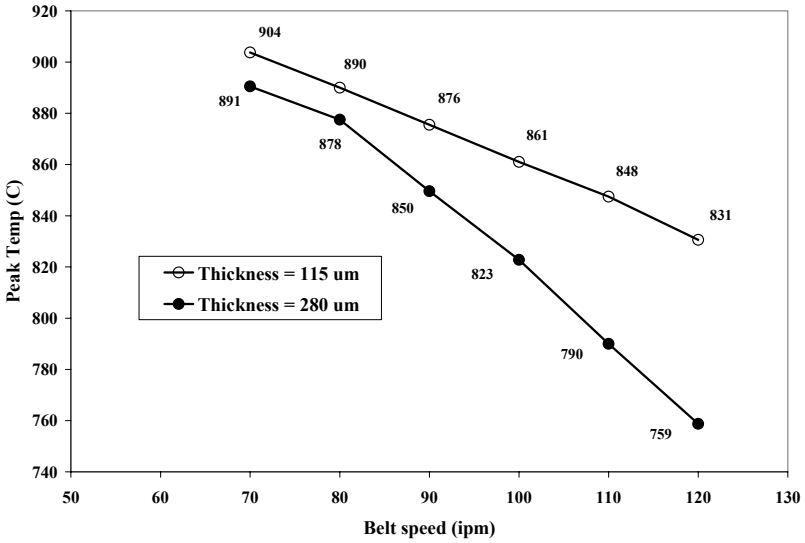


Figure 8.5 Effect of belt speed on peak firing temperature for wafers 115 and 280 μm thick. The higher the belt speed, the more the difference between the peak temperatures of the two thicknesses.

A similar effect was observed for textured wafers, which absorb more heat for a given belt setting as compared to planar wafers. For example, a textured 300 μm thick wafer experiences ~30 °C higher temperature than the counterpart 300 μm thick planar wafer for the same temperature settings in a belt furnace and a high belt speed of 120 ipm. Thus a 115 μm thick textured wafer could have ~100 °C higher temperature compared to the 300 μm thick planar wafer. This effect alone could lead to significant difference in the contact firing cycle and cell performance and could lead to a wrong assessment of the thickness reduction effect. This is why the belt settings were tailored to achieve similar firing profile for each thickness. For example, experimental data in Fig. 8.6 shows the impact of deviating from the optimum peak firing temperature on the cell efficiency for a 300 μm, textured FZ cells. The efficiency decreases by ~0.5% absolute when the peak firing temperature is lowered by 18 °C or increased by 28 °C relative to the optimum firing temperature. However, it should be pointed out that the behavior in Fig. 8.6 is specific to the Ag and Al pastes used in this study.

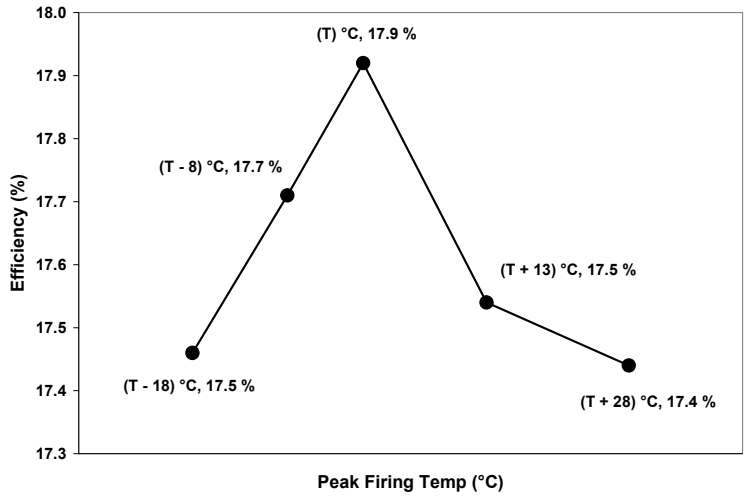


Figure 8.6 Textured cell efficiency as a function of peak firing temperature. T °C represents the optimum peak firing temperature.

In the past some studies on thin wafers did not account for these effects [171, 174]. Therefore, the next step was to adjust the belt zones temperatures and the belt speed to achieve the same contact firing profile for each thickness. This is necessary for the accurate assessment of the impact wafer thickness. The firing profiles for textured wafers were also adjusted for each thickness to maintain the same temperature profile seen by each wafer.

8.5 Performance of characterization of thin solar cells

8.5.1 Effect of wafer thickness on the performance of screen-printed, un-textured mc-Si cell (set 1)

HEM wafers were sourced from the same region of the brick and were carefully ground from one side to reach the desired thicknesses of 225, 175, 150, and 115 μm. Solar cells were fabricated on these wafers along with the standard wafer thickness of 280 μm. A high as-grown average lifetime of 41 μs was measured in these wafers.

8.5.1.1 Lighted I-V results on thin HEM mc-Si wafers

Lighted I-V results from the ground HEM wafers are shown in Table 8.2.

Table 8.2 I-V results measured (best and average) and PC1D simulated I-V for the best cells for HEM wafers from the same ingot, grinded to the desired thickness.

Thickness	Data	V_{oc}	J_{sc}	Eff.	FF	# of cells
µm		V	mA/cm^2	%	%	
280	Best	0.628	34.2	16.8	78.39	
	PC1D	0.626	34.0	16.8	78.85	
	Average	0.623	33.9	16.5	78.37	18
225	Best	0.628	33.4	16.4	78.39	
	PC1D	0.629	33.4	16.4	78.08	
	Average	0.628	33.4	16.2	77.26	15
175	Best	0.628	33.5	16.5	78.29	
	PC1D	0.626	33.5	16.5	78.57	
	Average	0.625	33.5	16.1	76.77	15
150	Best*	0.628	33.1	16.3	78.05	
	PC1D	0.625	33.1	16.2	78.55	
	Average	0.620	33.0	15.7	76.67	13
115	Best	0.618	33.0	15.7	77.23	
	PC1D	0.623	33.0	15.9	77.44	
	Average	0.615	33.0	15.5	76.35	20

*** Independently confirmed by National Renewable Energy Laboratory (NREL)**

For the basic n^+-p-p^+ cell design, cell efficiency decreased systematically from 16.8% to 15.7% when the cell thickness was reduced from 280 to 115 µm. V_{oc} of the best cell for each thickness was maintained at 628 mV, until the cell thickness decreased to 115 µm. At 115 µm, the average V_{oc} decreased to 615 mV, and J_{sc} decreased from 34.2 (280 µm) to 33.0 mA/cm^2. This is attributed to the lack of light trapping, which is discussed in the later sections. It is interesting to note that the performance of these planar HEM cells decreased from 16.8% to only 16.3%, when wafer thickness was decreased by almost a factor of two, from 280 µm to 150 µm.

Table 8.2 shows that reducing the thickness of mc-Si wafers from 225 µm to 175 µm does not cause much change in the cell performance. Münzer, et al., reported

efficiencies over 17%, relatively independent of the cell thickness [160]. Warta, et al., showed comparable performance for thick and thin cells, due to efficient light trapping, with a BSR of 97% and BSRV <200 cm/s [166]. Bruton, et al., fabricated 140 μm cells with efficiencies equal to that of 300 μm standard production cells [169]. Tool, et al., also reported efficiencies independent of wafer thickness [171]. Bähr, et al., showed that electrical performance is maintained down to 150 μm thickness [182]. Agostinelli, et al., also reported no loss in V_{oc} upon thinning the wafers down from 300 μm to 140 μm [181]. The conditions under which this happens will be discussed later.

8.5.1.2 Lifetime and Internal Quantum Efficiency (IQE) response of planar HEM mc-Si cells of different thicknesses

Figure 8.7 shows the average lifetime in the as-grown, diffused, and fully processed wafers.

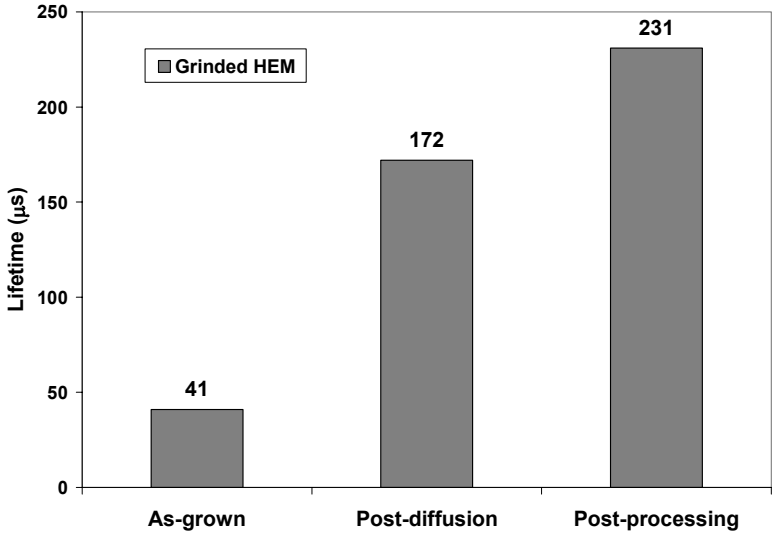
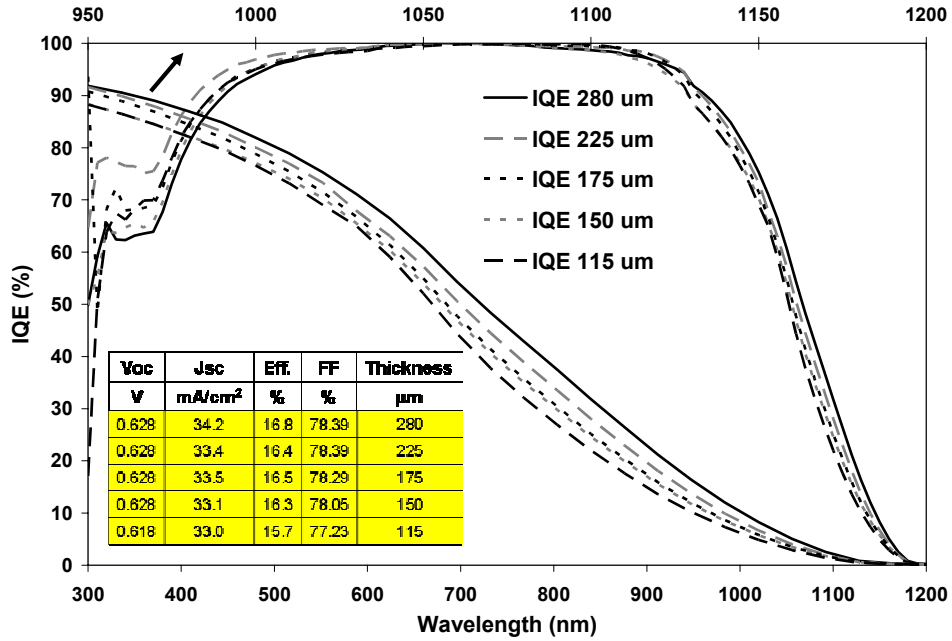


Figure 8.7 As-grown, post gettering and post-processing lifetime for HEM wafers which were ground to desired thickness, with I-V results shown in Table 8.2.

As-grown, post-diffusion, and post-processing lifetimes in these HEM wafers were 41, 172, and 231 μs, respectively. The average post-process lifetime, which includes

the effects of P and Al gettering and hydrogenation from the SiN_x film, was very high (231 μs), corresponding to a diffusion length of 813 μm, indicating that BSRV should play a dominating role in dictating the long wavelength IQE response and the performance of these cells.

Figure 8.8 shows the Internal Quantum Efficiency (IQE) response for the best cells listed in Table 8.2, for each thickness. Since the primary difference is expected to be in the long wavelength range, this response is shown more clearly on the secondary X-axis in the wavelength range 950-1200 nm. The IQE was measured at three different spots on each mc-Si cell and the best IQE is reported in Fig. 8.8.



Voc	Jsc	Eff.	FF	Thickness
V	mA/cm²	%	%	μm
0.628	34.2	16.8	78.39	280
0.628	33.4	16.4	78.39	225
0.628	33.5	16.5	78.29	175
0.628	33.1	16.3	78.05	150
0.618	33.0	15.7	77.23	115

Figure 8.8 IQE responses for the best cells shown in Table 8.2, for HEM wafers from the same ingot grinded to desired thickness. Response for the long wavelength is shown on secondary X-axis.

It is clear that as the wafer thickness decreases, the long wavelength IQE response also decreases. This is because the back surface becomes more influential with the thickness reduction.

8.5.1.3 PC1D modeling of HEM mc-Si cell data

Device modeling was performed using PC1D [6] to match the cell data and extract the relevant device parameters for these mc-Si cells. IQE and I-V parameters were matched simultaneously to ensure the accuracy of this analysis. Experimentally determined values of front surface reflectance, series and shunt resistances, base and emitter sheet resistivity, bulk lifetime, and grid shading were used in the modeling. Figure 8.9 shows an example of the match between the experimental and PC1D simulated I-V and IQE data for the best 115 μm thick HEM mc-Si cell in Table 8.2. Table 8.3 lists the parameters extracted from IQE fitting for these cells. Rear surface reflectance values were in the range of 63 to 67% for all the thicknesses, confirming the poor reflection properties of the Al-BSF surface. BSRV value was found to be ~400 cm/s for all the cells. For these devices, the critical BSRV (section 8.3) is 360 cm/s (Resistivity: 1.7 Ω·cm; L : 812.8 μm), which is comparable to the extracted BSRV of 400 cm/s, hence V_{oc} (best cell) loss was not observed on reducing the thickness (Table 8.2). FSRV values for thickness of 175, 150, and 115 μm were similar and between 120,000 and 140,000 cm/s. For 225 μm it was 75,000 cm/s, and for 280 μm it was 250,000 cm/s.

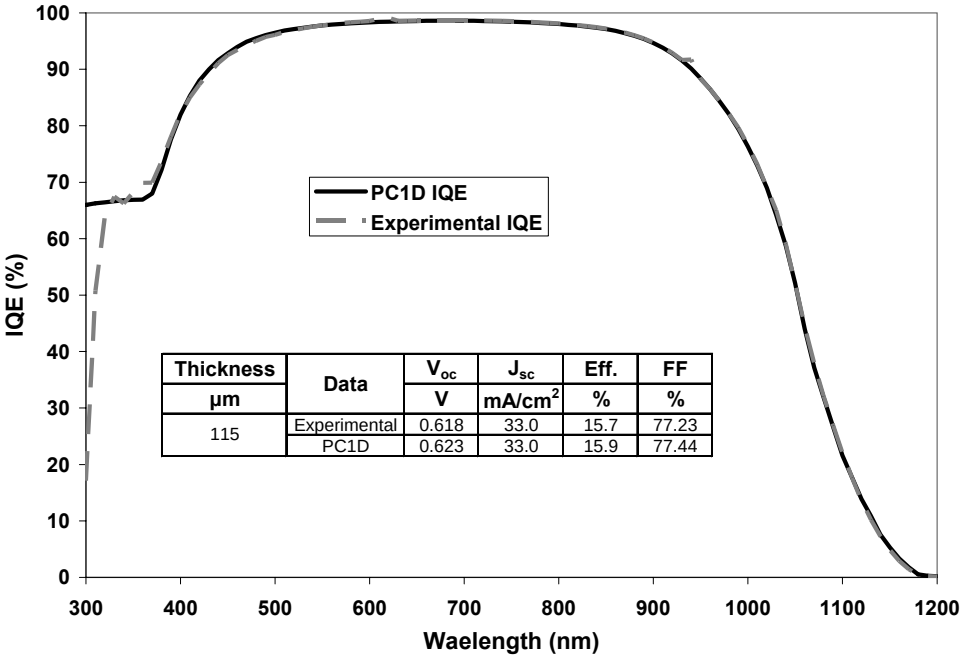


Figure 8.9 PC1D generated and experimental IQE for 115 µm HEM cell from Table 8.2.

Table 8.3 Parameters extracted from PC1D simulation for the best cells in Table 8.2.

Device Thickness (µm)	Bulk Lifetime (µs)	Internal Reflectance-Rear Surface (%)	BSRV (cm/s)	FSRV (cm/s)	L/W ratio
280	231	65	400	250000	2.9
225	231	63	400	75000	3.6
175	231	63	400	120000	4.6
150	231	63	400	140000	5.3
115	231	67	400	120000	7.0

8.5.2 Analysis of thick and thin FZ Si cells (set 2)

HEM mc-Si wafers in set 1 had lateral inhomogeniety, which could distort the study of the impact of thickness reduction. Therefore, in this section, solar cells were fabricated and analyzed on homogeneous, high lifetime FZ wafers of different thicknesses.

8.5.2.1 Lighted I-V results on thin FZ wafers

Table 8.4 shows the I-V parameters of the FZ cells with thickness range of 280-115 µm.

Table 8.4 I-V results measured (best and average) and PC1D simulated I-V for the best cells, for planar FZ wafers, ground to the desired thickness.

Thickness	Data	V_{oc}	J_{sc}	Eff.	FF	# of cells
µm		V	mA/cm^2	%	%	
280	Best*	0.637	34.7	17.4	78.74	
	PC1D	0.635	34.5	17.3	78.79	
	Average	0.635	34.4	17.1	78.33	17
225	Best	0.636	33.8	16.9	78.37	
	PC1D	0.635	33.9	16.9	78.56	
	Average	0.633	33.8	16.6	77.44	18
175	Best	0.634	33.6	16.7	78.25	
	PC1D	0.634	33.5	16.7	78.49	
	Average	0.631	33.6	16.2	76.39	27
150	Best	0.633	33.2	16.5	78.36	
	PC1D	0.634	33.3	16.5	77.94	
	Average	0.631	33.2	16.1	77.09	26
115	Best*	0.634	33.1	16.5	78.64	
	PC1D	0.634	33.1	16.5	78.70	
	Average	0.628	33.1	16.0	77.01	12

*** Independently confirmed by National Renewable Energy Laboratory (NREL)**

In the case of FZ cells with varying thickness, a systematic decrease in V_{oc} and J_{sc} was observed with the reduction in cell thickness. The un-textured, screen-printed FZ cell efficiency was 17.4% for 280 µm thick substrate, while the 115 µm thin FZ substrate had an efficiency of 16.5%. Like the HEM mc-Si cells, FZ cells also showed a decrease of ~1% in efficiency when the thickness was reduced from 280 µm to 115 µm.

8.5.2.2 IQE response of FZ cells with varying thickness

IQE response of FZ Si solar cells with different thicknesses is shown in Fig. 8.10. As expected, there is no variation in the short wavelength response. Again the long wavelength response shows a systematic decrease with the decrease in cell thickness.

Long wavelength IQE response is shown more clearly on the secondary X-axis, in the wavelength range 950-1200 nm.

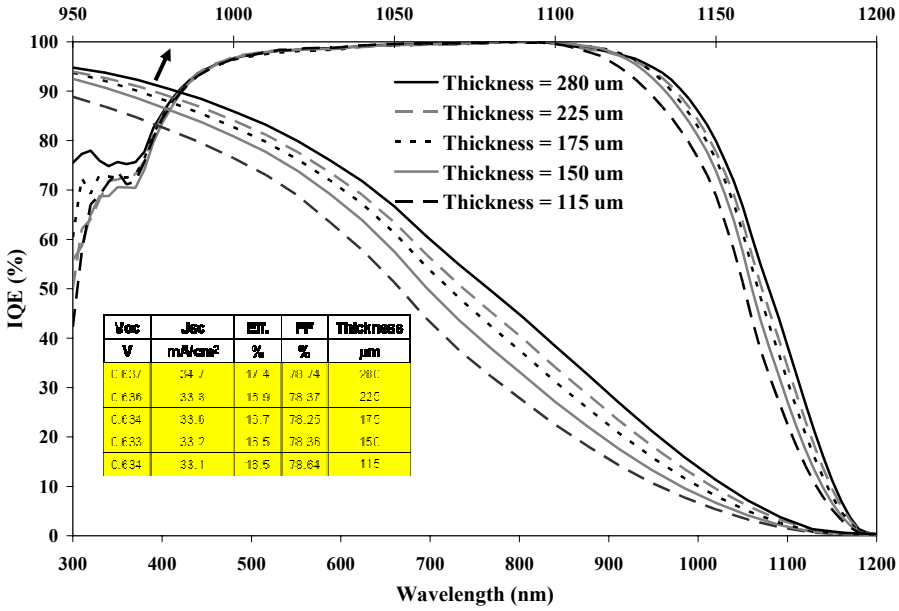


Figure 8.10 IQE response for best cells made on FZ silicon, of different thicknesses as listed in Table 8.4. Response for the long wavelength is shown on secondary X-axis.

8.5.2.3 PC1D modeling of FZ cell data

Similar to the HEM mc-Si cells, PC1D modeling was performed to match the I-V parameters and the IQE response simultaneously, using the measured cell parameters. Table 8.4 shows the match between the measured and simulated I-V parameters of the FZ cells with varying thicknesses. Cell parameters extracted from modeling are listed in Table 8.5. BSR values were in the range of 65-69%, BSRV was 300 cm/s, and FSRV values were in the range of 60,000 to 70,000 cm/s.

Table 8.5 Parameters extracted from PC1D fitting for the best planar FZ cells from Table 8.4.

Device Thickness (µm)	Bulk Lifetime (µs)	Internal Reflectance-Rear Surface (%)	BSRV (cm/s)	FSRV (cm/s)	L/W ratio
280	304	69	300	70000	3.3
225	304	69	300	65000	4.1
175	304	69	300	60000	5.2
150	304	67	300	70000	6.1
115	304	65	300	70000	8.0

Figure 8.11 shows the experimentally measured reflectance of the FZ cells. There is not much difference in the escape reflectance when thickness is lowered. This difference is due to the low, diffused BSR values (65-69%) of the Al-BSF cells. PC1D modeling showed that for a higher BSR and a specular reflectance (eg., Ag BSR), escape reflectance should be more for thinner wafers and might start to affect the J_{sc}.

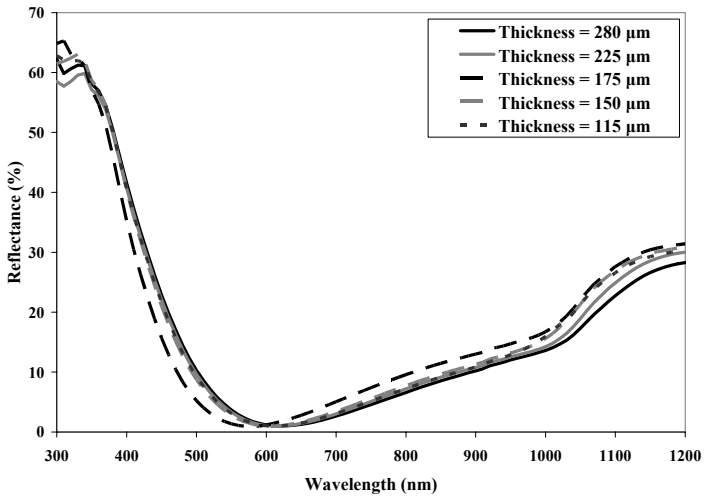


Figure 8.11 Experimental front surface reflectance for FZ cells of different thicknesses. Escape reflectance does not change much with thickness due to the low BSR values.

8.5.3 Modeling and analysis of thick and thin textured FZ Si cells (set 3)

In the previous sections only planar cells were investigated. To see the effect of light trapping by surface texturing, 1.3 Ω.cm FZ wafers in set 2 were thinned down in

KOH and textured to provide three different thicknesses of 300, 210, and 125 µm. Sheet resistivity of the emitter diffused layer was kept the same for a fair comparison with the planar FZ cells in set 2.

8.5.3.1 Lighted I-V results on textured FZ wafers

Table 8.6 shows the I-V parameters of the (300, 210, and 125 µm thick) textured FZ cells.

Table 8.6 I-V results measured (best and average) and PC1D simulated I-V for the best cells, for textured FZ wafers, etched in KoH and textured to achieve the desired thickness.

Thickness	Data	V_{oc}	J_{sc}	Eff.	FF	# of cells
µm		V	mA/cm^2	%	%	
300	Best*	0.632	37.5	18.1	76.38	
	PC1D	0.632	37.2	18.0	76.52	
	Average	0.630	36.9	17.7	76.02	27
210	Best	0.633	36.7	17.7	76.31	
	PC1D	0.633	36.7	17.7	76.23	
	Average	0.632	36.5	17.3	75.21	17
125	Best*	0.631	35.9	17.3	76.16	
	PC1D	0.631	36.0	17.3	75.99	
	Average	0.629	35.9	16.7	74.15	17

*** Independently confirmed by National Renewable Energy Laboratory (NREL)**

The cell data shows that the V_{oc} does not change appreciably when thickness is reduced; however J_{sc} still reduces with thickness. There is about 1% (0.8% for the best cell) absolute efficiency loss due to thickness reduction from 300 to 125 µm for these textured screen-printed cells. This is similar to what was observed for planar cells, and is in agreement with the study conducted by Tool, et al., [180]. In this study, a high efficiency of 18.1% and 17.3% were achieved on 300 µm and 125 µm thick FZ wafers, respectively, and on 45 Ω/sq emitter.

8.5.3.2 Analysis of IQE response of textured FZ cells with varying thickness

Figure 8.12 shows the IQE response of the best textured cell for each thickness in Table 8.6. IQE as a function of cell thickness showed the same trend as in the case of planar FZ cells. Long wavelength response decreased appreciably with thickness reduction but short wavelength response remained unchanged.

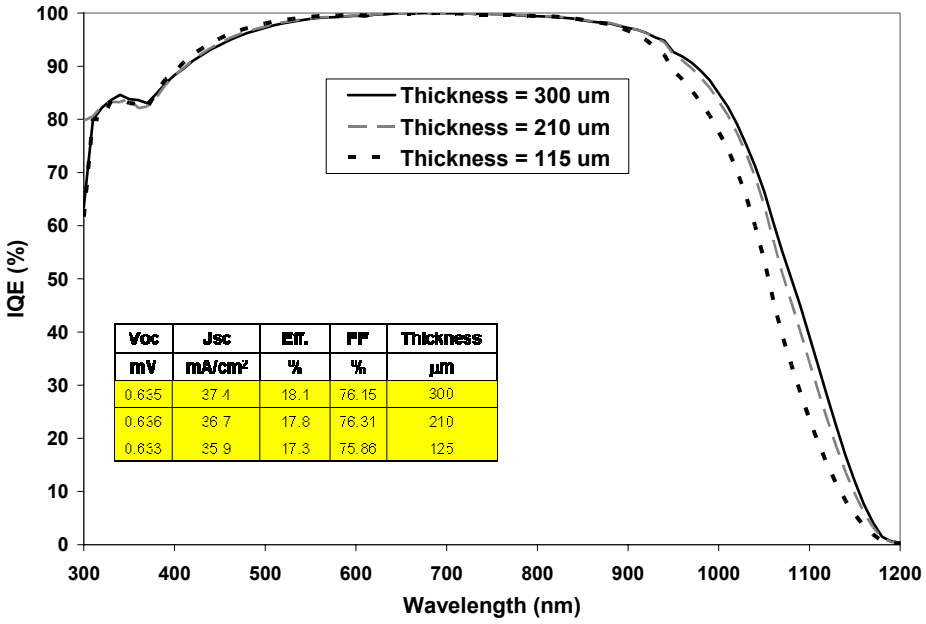
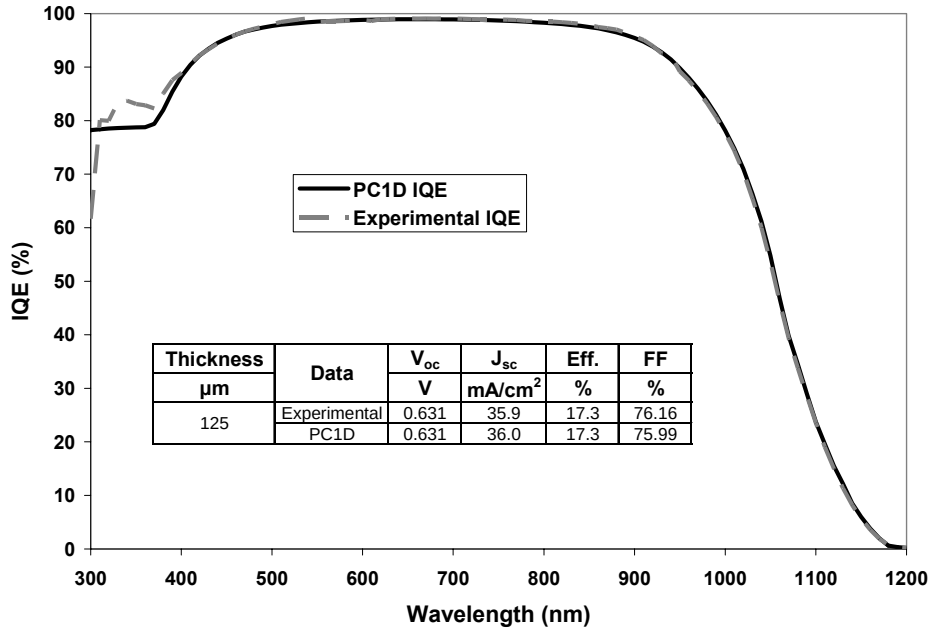


Figure 8.12 IQE response for best cells made on textured FZ silicon, of different thicknesses as listed in Table 8.6.

8.5.3.3 PC1D modeling of the textured cell data

PC1D modeling was performed for the best textured FZ cell for each thickness to match the I-V parameters (Table 8.6) and the IQE simultaneously. Figure 8.13 shows the experimental and modeled IQE and I-V data for the 115 µm thick, 17.3% textured FZ cell.



Thickness	Data	V_{oc}	J_{sc}	Eff.	FF
µm		V	mA/cm^2	%	%
125	Experimental	0.631	35.9	17.3	76.16
	PC1D	0.631	36.0	17.3	75.99

Figure 8.13 PC1D generated and experimental IQE for 125 µm textured FZ cell from Table 8.6.

Table 8.7 shows relevant cell parameters extracted by matching the I-V and IQE response, for the textured FZ cells.

Table 8.7 Parameters extracted from PC1D fitting of the best textured FZ cells from Table 8.6.

Device Thickness (µm)	Bulk Lifetime (µs)	Internal Reflectance-Rear Surface (%)	BSRV (cm/s)	FSRV (cm/s)	L/W ratio
300	304	70	350	70000	3.1
210	304	70	350	70000	4.4
125	304	67	350	50000	7.3

Modeling and analysis revealed that the internal rear surface reflection was 70% for 200 and 210 µm cells and 67% for the 125 µm cell. As expected, slightly higher BSRV of 350 cm/s was obtained for textured cells, compared to 300 cm/s for the planar cells. FSRV was in the range of 50,000 to 70,000 cm/s for these textured ~45 Ω/sq emitter cells. Such high FSRV can increase J_{oe} and lower the V_{oc} and cell performance. High J_{0e} can also mask the effect of change in J_{0b} due to thickness reduction. Therefore,

in the next section, cells were fabricated with higher emitter sheet resistance that should increase the sensitivity to change in J_{0b} due to thickness reduction.

8.5.4 Fabrication and analysis of thick and thin textured FZ Si cells with high sheet-resistance emitter (set 4)

In order to reduce the influence of emitter or J_0 (J_{0e}+J_{0b}) on V_{oc} or to enhance the impact of thickness reduction on J_0, FZ cells were fabricated with high sheet resistance emitter (80 instead of 45 Ω/sq) FZ wafers were thinned down in KOH and textured to achieve three different thicknesses of 300, 210, and 125 μm prior to cell fabrication.

8.5.4.1 Lighted I-V results on textured FZ wafers with high sheet-resistance emitter

Table 8.8 shows the lighted I-V data for the textured 300, 210, and 125 μm thick FZ cells with high sheet-resistance emitter.

Table 8.8 I-V results measured (best and average) and PC1D simulated I-V for the best cells on textured FZ wafers with high sheet-resistance emitters.

Thickness	Data	V_{oc}	J_{sc}	Eff.	FF	# of cells
μm		V	mA/cm^2	%	%	
300	Best*	0.639	37.4	18.5	77.29	
	PC1D	0.639	37.5	18.5	77.17	
	Average	0.635	37.1	18.0	76.14	44
210	Best	0.637	37.1	17.9	75.61	
	PC1D	0.638	37.2	18.0	75.60	
	Average	0.633	37.0	17.5	74.83	33
125	Best*	0.639	36.7	17.8	76.01	
	PC1D	0.638	36.7	17.8	76.10	
	Average	0.636	36.4	17.4	74.90	32

*** Independently confirmed by National Renewable Energy Laboratory (NREL)**

Note that the cell V_{oc} again does not change appreciably with thickness, however the J_{sc} decreases with thickness. This trend is similar to the low emitter sheet resistance cells in the previous sections. There is still ~0.6% average efficiency difference between the 300 and 125 μm cells. This suggests that for these thin cells, the rear surface

dominates the performance, therefore improving the front surface response did not shrink the efficiency gap between thick and thin cells, regardless of emitter sheet resistance. This was confirmed by PC1D modeling, which revealed that for the cell structure fabricated in this study, there was no appreciable change in efficiency difference between thick and thin cells due to the use of a high sheet-resistance emitter. However, absolute efficiency increased by ~0.5% absolute for high-sheet resistance emitter. Tables 8.8 and 8.6 reveal that the high sheet-resistance emitter gives a higher J_{sc} and V_{oc}. A screen-printed cell efficiency of 17.8% was achieved on 125 μm thick textured FZ wafer.

8.5.4.2 Analysis of the IQE response of textured FZ cells with varying thickness and high sheet-resistance emitter

IQE response of the best textured cell for each thickness in Table 8.8 is shown in Fig. 8.14. Again the IQE response in the long wavelength decreased with the thickness reduction, but the short wavelength response remained unaffected. A comparison of the IQE response of the 125 μm thick textured FZ cell with low sheet resistance (~45 Ω/sq) emitter in Fig. 8.14 reveals an enhancement in the short wavelength regime which accounts for the performance enhancement due to high sheet resistance emitter. (See Table 8.6 and 8.8.)

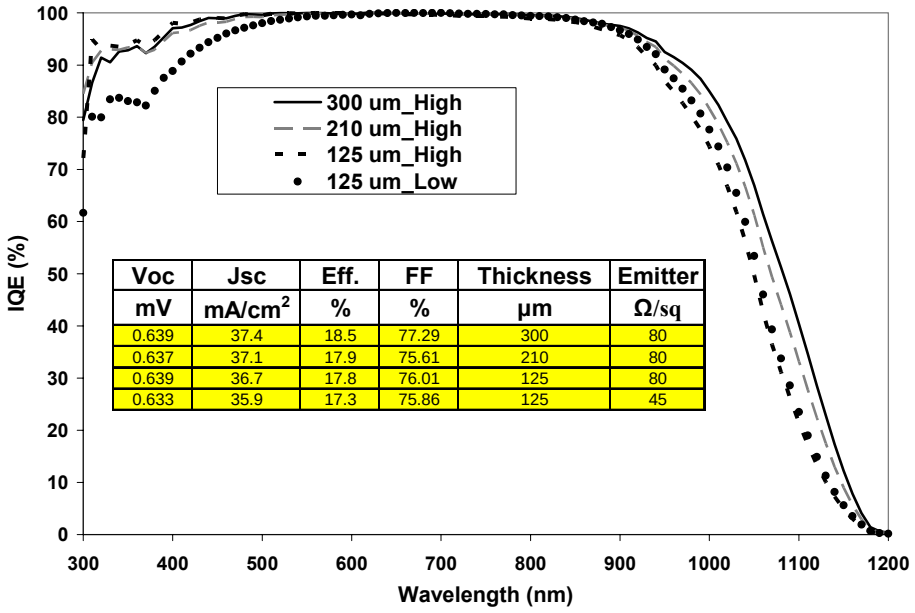


Figure 8.14 IQE response for best cells made on textured FZ Si with thickness of 300, 210, and 125 µm and a high sheet-resistance emitter as listed in Table 8.8.

8.5.4.3 PC1D modeling of the cell data with high emitter sheet resistance

PC1D modeling was also performed for the best textured FZ cells in Table 8.8 for each thickness to match the I-V parameters and the IQE simultaneously. Table 8.8 shows the comparison of the measured and simulated I-V data. Table 8.9 shows the extracted cell parameters from this analysis.

Table 8.9 Parameters extracted from PC1D fitting of the best textured FZ cells from Table 8.8.

Device Thickness (µm)	Bulk Lifetime (µs)	Internal Reflectance-Rear Surface (%)	BSRV (cm/s)	FSRV (cm/s)	L/W ratio
300	304	70	400	11000	3.1
210	304	70	400	14000	4.4
125	304	63	400	10000	7.3

In the case of high emitter sheet resistance cells, internal rear surface reflection was found to be 70% for 300 and 210 µm cells and 63% for the 125 µm thick cell. BSRV

was 400 cm/s but the FSRV values were much lower, in the range of 10,000-14,000 cm/s, as opposed to 50,000-70,000 cm/s for low sheet resistance emitter (Table 8.7). This is the result of reduced recombination in the lightly doped emitter and better surface passivation due to lower surface concentration.

8.5.5 Analysis of HEM mc-Si with high sheet-resistance emitter (set 5)

Finally, to see the effect high sheet-resistance emitters on HEM mc-Si, planar solar cells were fabricated on 150 and 115 μm thick HEM mc-Si wafers with emitter sheet resistivity of 85 Ω/sq.

8.5.5.1 Lighted I-V results on thin HEM mc-Si wafers with high sheet-resistance emitter

Table 8.10 shows the I-V data for the HEM cells fabricated on the 85 Ω/sq emitter.

Table 8.10 I-V results measured (best and average) and PC1D simulated I-V for the best cells, for high sheet resistance emitter HEM wafers.

Thickness	Data	V_{oc}	J_{sc}	Eff.	FF	# of cells
μm		V	mA/cm^2	%	%	
150	Best*	0.634	34.4	16.8	77.13	
	PC1D	0.635	34.5	16.8	76.71	
	Average	0.630	34.4	16.2	74.96	34
115	Best*	0.633	33.7	16.4	76.81	
	PC1D	0.633	33.7	16.4	76.65	
	Average	0.627	33.4	15.8	75.51	20

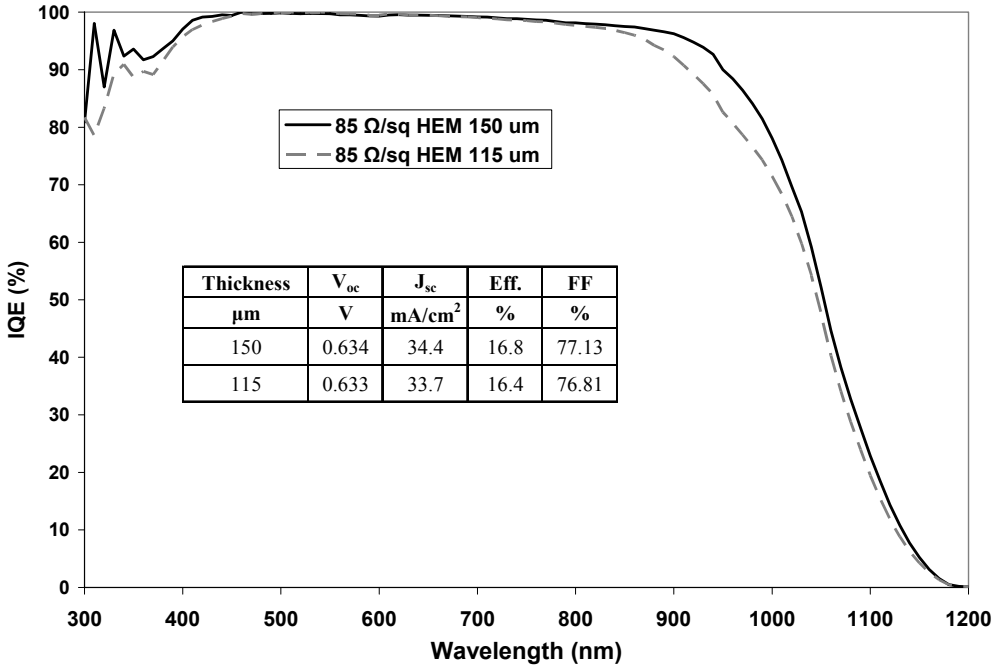
*** Independently confirmed by National Renewable Energy Laboratory (NREL)**

The front Ag paste, the grid pattern, and contact firing were optimized for high sheet resistance emitter and to ensure that both 150 and 115 μm wafers experience the same peak temperature. A much higher V_{oc} of 634 mV (average of 630 mV) was achieved on the 150 μm cells along with higher J_{sc} of 34.4 mA/cm^2. This resulted in impressive efficiency of 16.8% on 150 μm thick mc-Si. The 115 μm thick cell also showed superior performance, yielding a V_{oc} of 633 mV and J_{sc} of 33.7 mA/cm^2, and cell

efficiency of 16.4%. High sheet resistance gave 0.5% and 0.7% higher absolute efficiency relative to the counterpart 45 Ω/sq emitter cells. These efficiencies represent the highest reported efficiencies for such thin screen-printed mc-Si cells, with a full area Al-BSF, and a single layer AR coating with no surface texturing. It should be noted that there was appreciable bowing in the 115 μm thick cell.

8.5.5.2 IQE response of the high sheet-resistance HEM mc-Si cells with varying thickness

The IQE response for the 150 and 115 μm cells is shown in Fig. 8.15.



Thickness	V_{oc}	J_{sc}	Eff.	FF
μm	V	mA/cm^2	%	%
150	0.634	34.4	16.8	77.13
115	0.633	33.7	16.4	76.81

Figure 8.15 IQE responses for best HEM mc-Si cells fabricated on high sheet resistance emitter as shown in Table 8.10.

As expected, the 115 μm cell has a lower long wavelength response than the 150 μm cell, which leads to loss in the J_{sc} and efficiency, but the V_{oc} is comparable.

8.5.5.3 PC1D modeling of cell data of high sheet resistance HEM mc-Si cells

I-V parameters in Table 8.10 and IQE response in Figure 8.15 were matched simultaneously using PC1D. Table 8.10 also shows the PC1D modeled I-V parameters, while Table 8.11 shows the extracted parameters (BSR, BSRV, and FSRV) along with post-process lifetimes.

Table 8.11 Parameters extracted from PC1D fitting of the best high sheet resistance HEM cells from Table 8.10.

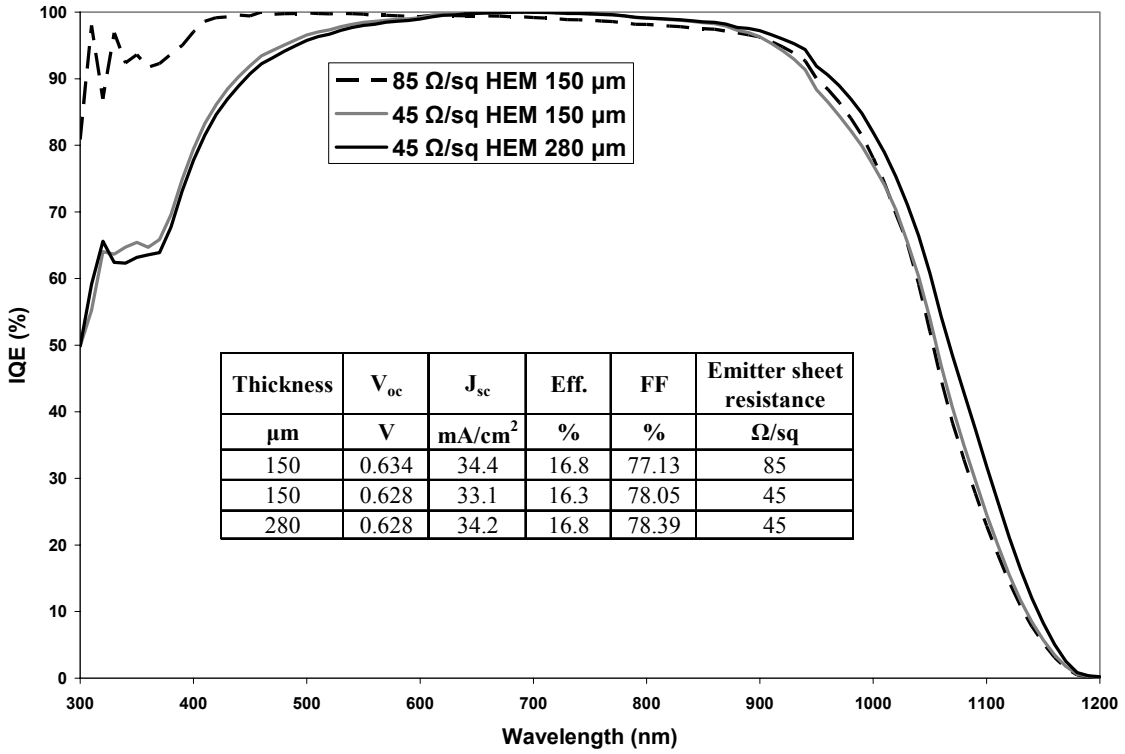
Device Thickness (μm)	Post-process lifetime (μs)	Internal Reflectance-Rear Surface (%)	BSRV (cm/s)	FSRV (cm/s)	L/W ratio
150	186	61	400	12000	4.8
115	171	61	400	25000	6.0

BSRV value was similar (400 cm/s) to the counterpart low sheet resistance cells. However, FSRV value of 12000 cm/s for the 150 μm cell and 25,000 cm/s for the 115 μm were far superior to the FSRV of low sheet resistance devices (Table 8.3).

8.5.5.4 A comparison of thick and thin 85 Ω/sq and 45 Ω/sq emitter mc-Si cells

Figure 8.16 shows a comparison of IQE and I-V data of the low and high sheet-resistance 150 μm thick mc-Si cells. For comparison, the IQE and I-V of the 45 Ω/sq, 280 μm thick mc-Si cell is also shown. Figure 8.16 clearly shows that thickness reduction from 280 μm to 150 μm for the 45 Ω/sq cells lowers the J_{sc} by ~1 mA/cm^2, resulting in ~0.5% loss in efficiency. The loss in J_{sc} is reflected in the loss in long wavelength IQE response. Increasing the sheet resistance from 45 to 85 Ω/sq increased the V_{oc} by 8 mV, J_{sc} by 1.7 mA/cm^2, and efficiency by 0.6%. Increase in J_{sc} is reflected in the higher short wavelength response for these cells. Notice that the efficiency gain could have been even

higher if the FF did not decrease from 0.78 to 0.76, due to higher contact and series resistance.



Thickness	V_{oc}	J_{sc}	Eff.	FF	Emitter sheet resistance
µm	V	mA/cm^2	%	%	Ω/sq
150	0.634	34.4	16.8	77.13	85
150	0.628	33.1	16.3	78.05	45
280	0.628	34.2	16.8	78.39	45

Figure 8.16 IQE comparisons for 150 µm, 45 and 85 Ω/sq emitter, and 280 µm thick, 45 Ω/sq HEM cells.

8.6 Guidelines for preventing the efficiency loss due to reduced cell thickness

After fabricating and analyzing the thick and thin cells, with and without texturing, and with low and high sheet resistance, further device modeling was performed to identify the factors that can help to boost the cell performance when thickness is reduced.

8.6.1 The impact of L/W ratio on thick and thin cells

The importance of L/W ratio in understanding and characterizing the cell performance has been reported [140, 191] and discussed in CHAPTER 7. L/W increases as the material quality or the diffusion length L improves or when the cell thickness W is

reduced. An understanding of this ratio is very important, especially for the mc-Si cells, in which the lifetime of the wafers changes with the ingot (vendors) as well as the position of the wafer within the ingot. Tables 8.3, 8.5, 8.7, 8.9, and 8.11 show the measured L/W ratios for the cells fabricated in this study. Device modeling was performed using PC1D to see if this L/W ratio was optimum for the cell performance. The curves in Fig. 8.17 show the calculated cell efficiency as a function of the L/W ratio. For each curve, cell thickness was kept constant, and L was increased to change the L/W ratio. This was done for five different thicknesses: 280, 220, 160, 100, and 70 μm. A fixed BSRV value of 400 cm/s was used, which was extracted from the analysis of untextured HEM wafers in this study. Two points are highlighted on each curve. Highlighted point on the right side of each curve is the lowest L/W value after which efficiency does not change. Highlighted point on the left side of each curve is the L/W ratio and the corresponding efficiency for a modest 1% relative decrease in the maximum efficiency. For each point, lifetime value is calculated and shown for each L/W ratio and thickness to get a quantitative lifetime-value-change estimate. As seen in Fig. 8.17, a significantly lower L/W ratio (or lifetime) would suffice to get reasonable efficiencies for each thickness. For example, for the 100 μm thickness curve, an L/W ratio of 5.6 (lifetime = 111 μs) would yield an efficiency of 16.6%; however with a significantly lower L/W ratio of 3.6 (lifetime = 47 μs), a comparable efficiency of 16.4% can would achieved.

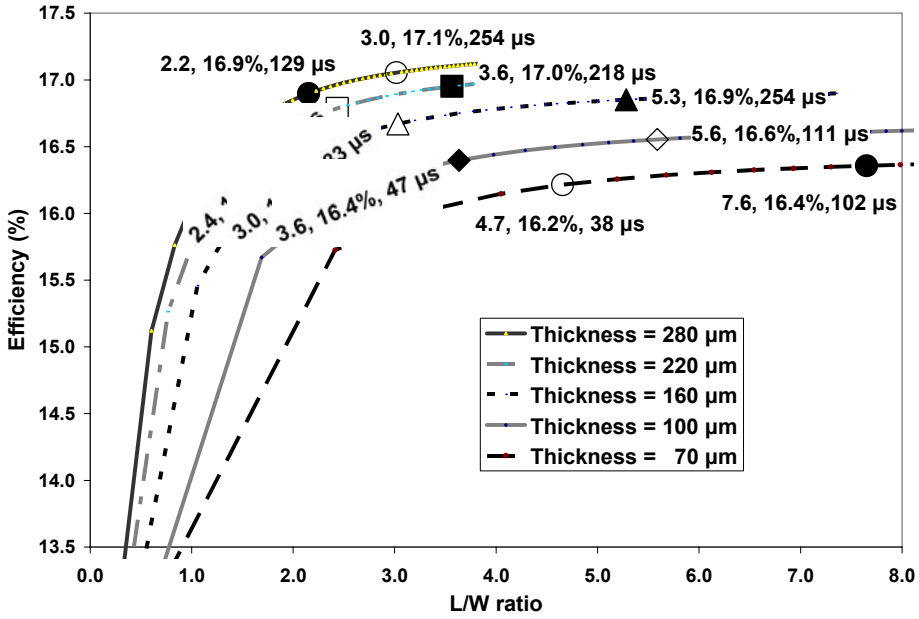


Figure 8.17 Efficiency dependence on L/W ratio. Highlighted point on the right side of each curve is the lowest L/W value after which efficiency does not change. Highlighted point on the left side of each curve is the L/W ratio and the corresponding efficiency for a 1% relative decrease in the maximum efficiency.

The L/W ratios in Tables 8.3, 8.5, 8.7, 8.9, and 8.11, on comparison with Fig. 8.17, reveal that the L/W ratios for the cells fabricated in this study are quiet high. A significantly lower L/W ratio, and hence a lower material quality wafer, could still have yielded comparable efficiencies. The curves of Fig. 8.17 are for a BSRV of 400 cm/s and a BSR value of 70%. These values would however be significantly different for lower BSRVs and higher BSRs.

8.6.2 Modeling to identify the parameters critical for a better cell performance on thinner substrates

In this sub-section, the critical parameters for improving the performance of thin wafers are identified. In particular, effects of texturing, BSRV, and BSR are analyzed. Figure 8.18 shows the efficiency dependence on thickness for a lifetime of 300 µs. The lowest curve (curve 1) simulates the change in efficiency when going towards thinner

wafers, with the current status of full area Al-BSF cells analyzed in this study. An experimental reflectance file for a planar wafer (grid shading 4% and average weighted reflectance of 12% (extrapolated in the long wavelength regime)) was used for generating this curve. Curve 2 shows the effect of texturing. An external reflectance file for a textured wafer (grid shading of 4% and average weighted reflectance of 4.5% (extrapolated in the long wavelength regime)) was used to generate this curve; however for simplicity, the increased BSRV for textured surface was not taken into account. For both curves 1 and 2, there is a reduction of ~0.5% in efficiency when going from 300 µm to 100 µm thickness. This difference of ~0.5% is maintained, even when BSRV is reduced from 400 cm/s to a low value of 100 cm/s, as seen in curve 3. A comparable efficiency for 300 µm and 100 µm wafer is obtained only when light trapping is introduced via enhanced BSR of 98%, which is evident from curve 4. This improvement retains the J_{sc} value for thinner cells and yields comparable efficiencies.

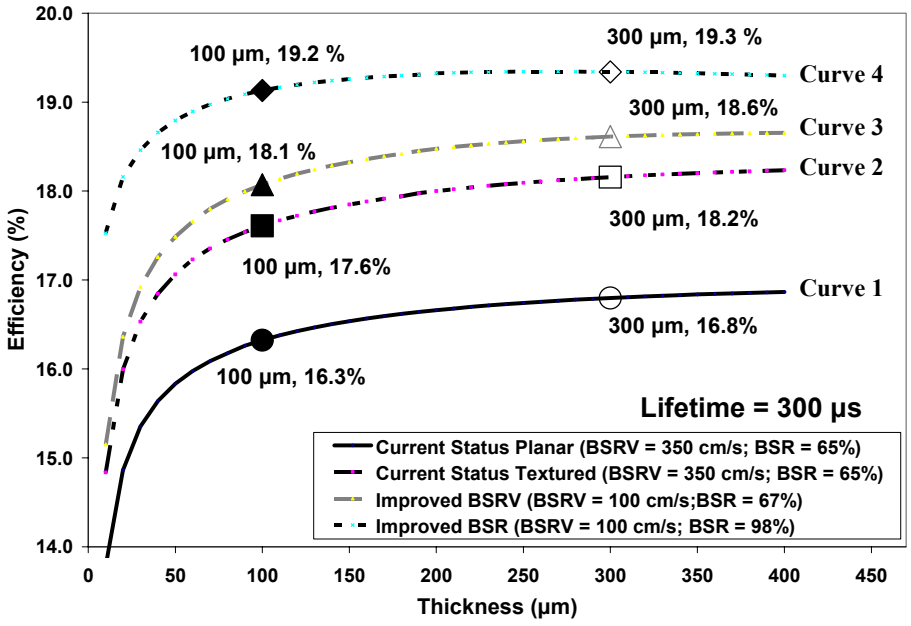


Figure 8.18 Cell efficiency as a function of thickness. The effects of texturing, improved BSRV and BSR are simulated for a lifetime of 300 µs.

Figure 8.19 shows the same set of curves as in Fig. 8.18, but for a lower lifetime of 30 μs (L: 290 μm, comparable to the thickest cell). The lowest curve (curve 1) simulates the change in efficiency when using untextured thin wafers with the current technology of full area screen-printed Al-BSF. The curve above that (curve 2) shows that texturing alone can produce ~1.2% enhancement in the efficiency of thin cells. Curve 3 shows that the implementation of a better BSRV (100 cm/s in place of 400 cm/s) gives ~0.3% enhancement in efficiency. Finally a 98% BSR, as opposed to 65%, gives another 1% increase in the efficiency for the 100 μm thin cells (curve 4). Figure 8.19 also shows that for a relatively low lifetime material (30 μs), thinning the wafer in conjunction with advanced design features (BSRV ~100 cm/s and BSR ~98%) can actually raise the efficiency from 17.8% to 18.5%. A difference in efficiency of 0.3% in 300 μm and 100 μm cells is observed, which is lower than the 0.5% difference for a high lifetime, 300 μs cell (curves 1 of Figs. 8.18 and 8.19). The 0.3% difference is maintained even after texturing and an improved BSRV of 100 cm/s (curves 2 and 3). Improving BSR to 98% in this case leads to an improved performance for the 100 μm cell, compared to the 300 μm cell, as seen in curve 4. Figure 8.19 also shows that reducing the thickness is more favorable for a lower lifetime wafer than a high lifetime wafer, if proper light trapping schemes can be implemented or even otherwise. Kray, et al., showed that the thin wafers indeed outperform their thicker counterparts for comparatively low bulk lifetimes. Thin cells on lower quality material exhibit higher V_{oc} and J_{sc} and an increased L/W ratio [161]. Steckemetz, et al., showed that the effect of huge difference in bulk lifetimes for Cz and FZ cells becomes negligible for 100 μm cells whereas the benefits of good surface passivation increases with decreasing wafer thickness as seen in Fig. 8.19 [168].

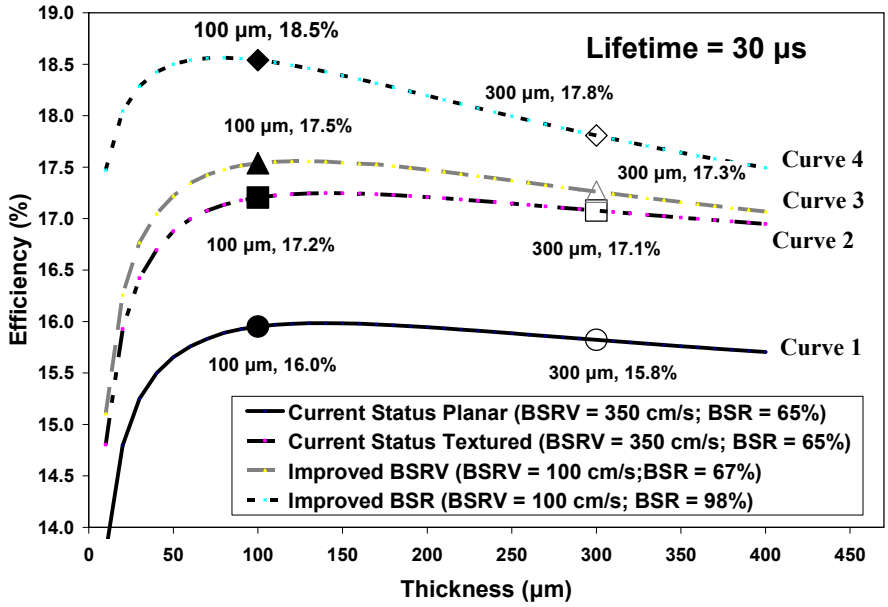


Figure 8.19 Cell efficiency as a function of thickness. The effects of texturing, improved BSRV and BSR are simulated for a lifetime of 30 µs.

8.7 Cost modeling

8.7.1 Manufacturing cost model

Several studies have been performed in literature, to analyze the cost of module production, which often differ in the assumptions for the input parameters. Cost analysis is performed in this study by using a simple and approximate model to assess the impact of wafer thickness and efficiency on the direct module manufacturing cost. This model was developed for screen-printed, cast mc-Si wafers and cells. Several factors such as kerf loss, yield, operating costs, and equipment costs were taken into account for calculating the direct module manufacturing cost. The key parameters and their input values, based on the current status of module manufacturing, are listed in Table 8.12.

Table 8.12 Some of the parameters and their input value, used in the cost analysis model.

Parameter	Input Value
Cell Area	225 cm^2
Kerf thickness	210 μm
Silicon cost	$100/kg
Wafer yield	92%
Cell yield	95%
Module yield	98%
Interest rate for capital	8%
Depreciation	7 years
Operator cost	$11/hr
Maintenance cost	$22/hr
Engineer cost	$30/hr
Overhead rate (as % of labor)	100%

Figure 8.20 shows the iso-efficiency curves on a plot for the total module cost in $/W vs. the thickness of the solar cell.

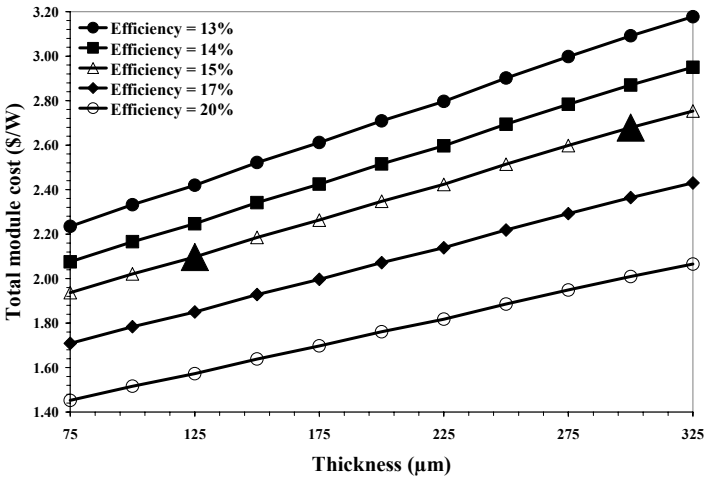


Figure 8.20 Total module cost vs. the thickness of the cell for efficiencies ranging from 13-20%.

Figure 8.20 assumes a constant yield when thickness is reduced. As seen from Fig. 8.20, the manufacturing cost can be reduced appreciably when the cell thickness is reduced because cost of Si is ~50% of the module manufacturing cost. For example, highlighted points in Fig. 8.20 show that the manufacturing cost of a module made from 15% efficient cells can be reduced by $0.58/W if 125 μm wafers are used instead of 300

μm wafers. However, this assumes that 15% efficient cells can be achieved on both thicknesses, which may not be the case. Figure 8.20 also shows that even if the efficiency of 125 μm cell drops to 14%, manufacturing cost would be lower than the 15% efficient cell on 300 μm thick wafer.

8.7.2 Cost implications of the thickness and efficiency tradeoff of the cells fabricated in current study

Figure 8.21 shows the experimental efficiency of the HEM mc-Si cells as a function of wafer thickness, as listed in Table 8.2. For each cell thickness and the corresponding efficiency, the module manufacturing cost was calculated using the model. Note that it is the relative cost saving that is more important in this study rather than the absolute manufacturing cost, which depends on inputs and assumptions. Assuming constant yield for thick and thin cells, the cost calculations indicate that even though the mc-Si efficiency in this study dropped from 16.8% to 15.7%, when the cell thickness was reduced from 280 to 115 μm, the direct manufacturing cost decreased by 36¢/W, which is very significant. This highlights the merit of thickness reduction for $100/kg feedstock Si, even with the current screen-printing technology with full area Al-BSF, which reduces the efficiency upon thickness reduction. If advanced design features are implemented, like dielectric back passivation and more efficient light trapping, the impact on cost would be even greater.

The direct manufacturing cost of the module made from 16.8% high-sheet-resistance emitter cells on 150 μm thick mc-Si cell in section 8.5.5 is calculated to be $1.95/W. This is higher than the manufacturing cost of $1.89/W for the 16.4%, 115 μm thick mc-Si cell, assuming the same yield. The module cost for each cell thickness and efficiency combination attained in this study is calculated and depicted in Fig. 8.21.

Reduced cell thickness results in reduced manufacturing cost even though cell efficiency decreases from 16.8% to 15.7%.

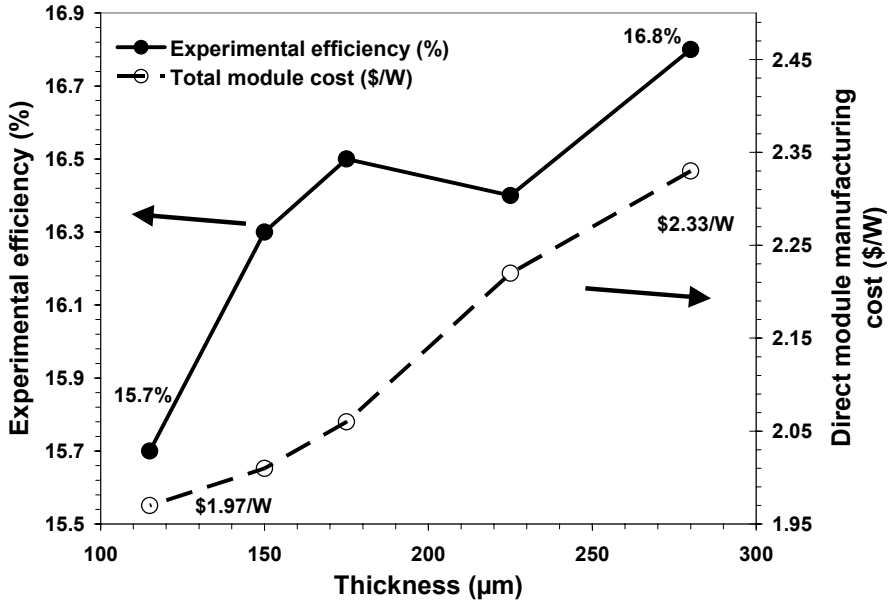


Figure 8.21 Experimental efficiency from Table 8.2 and the corresponding cost for the five different thicknesses of mc-Si cells fabricated in this study.

Since the cost calculations in Fig. 8.21 assumed same yield, additional calculations were performed in Fig. 8.22 to quantify the impact of the wafer, cell, and the module yield on the manufacturing cost of 115 μm thick, 16.4% efficient screen-printed mc-Si cell fabricated in this study. As expected, the cost increases as the yield decreases. The increase in cost is greater for the same loss of yield as you go from wafer to module.

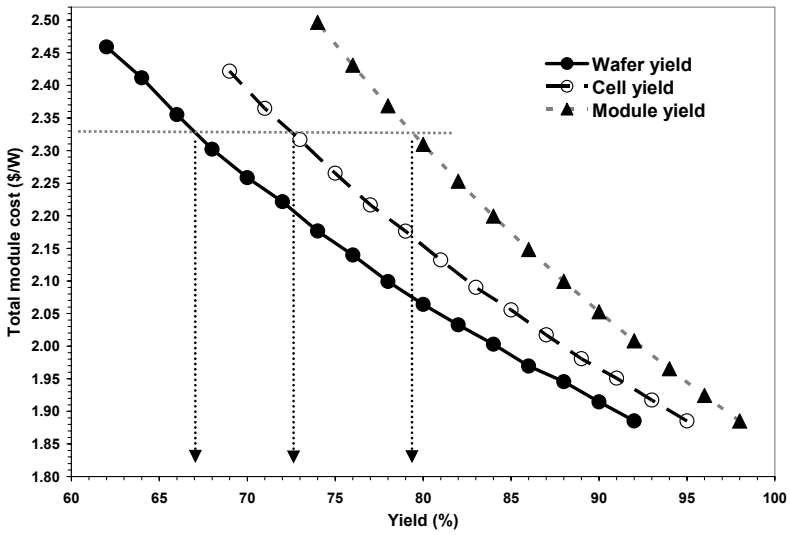


Figure 8.22 Total module cost as a function of yield at various stages in the cell fabrication. Baseline yields were 92, 95, and 98% for wafer, cell, and module. Only one yield was varied at a time to generate the three curves, while other two were fixed.

The dotted horizontal line in Fig. 8.22 is indicative of the module manufacturing cost of $2.33/W for the 280 μm thick mc-Si cell fabricated in this study. As shown by the three vertical lines in Fig. 8.22, same cost can be achieved with 16.4%, 115 μm thick cells if the wafer yield drops to 67%, or the cell yield decreases to 72%, or module yield reduces to 79%. This shows that there is a substantial leverage in the yield as you thin the device down.

8.8 Conclusion

In this chapter, solar cells were fabricated on thin c-Si wafers with full areal Al-BSF. The contact firing cycle for each thickness was adjusted so that all the wafers experience the same peak contact firing temperature. Planar solar cells were fabricated on HEM mc-Si wafers along with single crystal FZ silicon and ground down to desired thickness. Selected cells were also fabricated with low and high sheet-resistance emitters to evaluate the influence of emitter design on thin cells. All cells were 4 cm^2 screen-

printed with a single layer SiN_x antireflection (AR) coating and a full area aluminum back surface field (Al-BSF). Screen-printed cell efficiencies of 17.8 and 18.5% were achieved on 125 μm and 300 μm thick textured FZ wafers, respectively, with high sheet-resistance emitters (80-100 Ω/sq). Screen-printed cell efficiencies of 16.4 and 16.8% were obtained on 115 and 150 μm thick planar HEM mc-Si cells with a high sheet-resistance emitter. The 0.5-1% difference in the efficiency of thick and thin cells was analyzed by detailed cell characterization and PC1D modeling. The processed bulk lifetime was in excess of 200 μs for all the cells, which made the thin cells more sensitive to BSRV and less dependent on lifetime. It was found that the high BSRV (300-400 cm/s) and low Back Surface Reflectance (BSR) (63-70%) associated with the full area Al-BSF were the major reasons for the reduced performance of thin cells. Model calculations showed that a BSRV of ≤100 cm/s and BSR of ≥ 95% can virtually eliminate the efficiency gap between 300 μm and 115 μm thick cells for these ≥ 200 μs bulk lifetime wafers. Manufacturing cost modeling showed that reducing the mc-Si wafer thickness from 300 μm to 115-150 μm reduces the module manufacturing cost in spite of ~1% lower cell efficiency.

CHAPTER 9

FABRICATION, CHARACTERIZATION, AND MODELING OF LOW-COST, DIELECTRIC-FIRED-THROUGH BACK-SURFACE PASSIVATED SOLAR CELLS WITH LOCAL BACK-SURFACE FIELD ON THIN SILICON

9.1 Introduction

This chapter describes the fabrication, characterization, and modeling of a device structure with rear local Al contacts and BSF formed simultaneously by firing through a passivating dielectric layer. This process sequence is explored to determine its compatibility with the fabrication of high-efficiency solar cells on thin c-Si substrates. Section 9.2 first provides background and motivation behind using a dielectric to passivate the rear surface. Section 9.3 describes a novel process sequence used in this study for fabrication of the dielectric passivated local back-surface field (LBSF) cells, along with the formation of the dielectric layer and a metallization sequence. Results of the fabrication and a comprehensive characterization of thick and thin dielectric cells are presented in section 9.4. Finally, PC1D modeling is performed in section 9.5 to extract the relevant device parameters and model the solar cells fabricated in section 9.4.

9.2 Background and motivation for the use of dielectric to passivate the rear surface

Several cell structures have been reported in the literature to enhance performance of thin cells relative to the full area Al-BSF cells. Some of them are: laser-fired contacts (LFC) [70], *industrial* Passivated Emitter and Rear Cells (*i*-PERC) [181], Emitter Wrap-Through (EWT) [192], and Interdigitated Back Contact (IBC) [193]. Most of these

structures implement a suitable passivating layer and contact of the back to provide enhanced surface passivation, which is critical for thinner wafers. Three different back surface passivation schemes are usually applied, namely aluminum back-surface field (Al-BSF), boron back-surface field (B-BSF) and dielectric passivation. Solar cells with full area Al-BSF suffer from bowing and loss in efficiency on thinning the cells. B-BSF needs a second diffusion step at much higher temperature, because of lower diffusion coefficient of boron and often results in lifetime degradation. Therefore the use of a dielectric layer to passivate the rear is being pursued very aggressively and is the subject of this chapter.

Two of the recent studies, which use screen-printing for the front contacts, involve laser fired Al local BSF and contacts (LFC) on the rear. Schultz, et al., used screen-printing of hot-melt Ag paste for the front contacts, followed by the light-induced plating (LIP) [194], to achieve 19.3% LFC cells on 4 cm^2 FZ cells. Hörteis, et al., defined the front contacts by first printing a seed layer using an aerosol jet printer and Ag ink, followed by LIP to achieve line widths below 45 μm, resulting in a FF of 80.1% on a 110 Ω/sq emitter, and an efficiency of 20.3% LFC cells [195]. Both these structures involved Al evaporation and laser-firing to form the rear contacts. Despite the superior efficiencies and potential, LFC cells are not yet in production probably because of the challenges arising from the cost and ease of manufacturability.

Formation of a good-quality rear contact with dielectric passivation in conjunction with low-cost screen-printing technology is very challenging. Attempts have been made to form rear contact of the solar cell after the application of the dielectric layer by techniques such as LFC [70], mechanical abrasion [196], plasma etching and laser

ablation/patterning [197, 198], dielectric-fired-through [199], and etching pastes [198]; however the ensuing cost, throughput, and manufacturability remains the challenge. Therefore in this chapter we have made an attempt to develop a process sequence that uses the low-cost screen-printing technology to form local BSF and contacts without the need to locally open the vias through the dielectric layer. In addition, front and back screen-printed contacts are formed simultaneously, and this process sequence is capable of producing thin cells without any bowing.

9.3 Development and characterization of screen-printed solar cells with dielectric-fired-through local back-surface field and contacts

A cost-effective solar cell fabrication sequence was developed that involves a dielectric passivated rear surface, screen-printed front and rear contacts, and a screen-printed back surface reflector. Figure 9.1 shows the process sequence.

The following challenges were addressed to make the process sequence work, while keeping the fabrication cost low:

- Application of a suitable low-cost dielectric layer with low positive charge density to provide a good and stable surface passivation after contact firing.
- Simultaneous formation of screen-printed front and rear contacts that can fire through the AR coating on the front and passivating dielectric layer on the rear.
- Formation of an LBSF through the vias in the rear dielectric.
- Formation of an efficient back surface reflector composed of rear dielectric capped with screen-printed metal.

The next sub-sections discuss the process steps and the challenges in more detail.

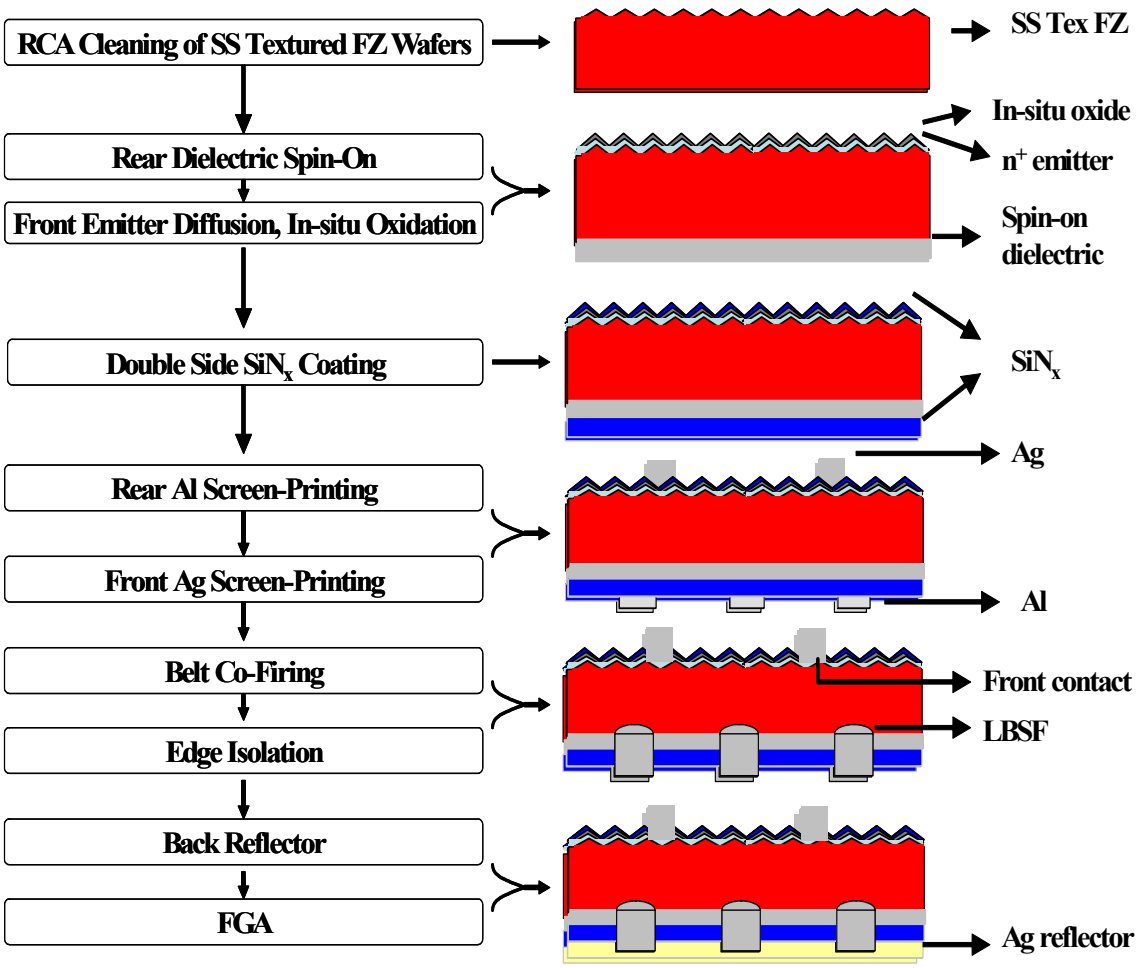


Figure 9.1 Fabrication sequence for the novel LBSF solar cells.

9.3.1 n^+ emitter formation on the front side

To reduce the number of processing steps, spin-on phosphorous coated Si wafers were used for limited solid source diffusion [200]. Solid source wafers were prepared in-house using a spin-on process and phosphoric acid. These wafers were stacked alternately with target wafers for making cells, as shown in Fig. 9.2. Limited source enables the formation of in-situ front and rear oxide due to negligible glass formation. This is accomplished by turning the oxygen gas on after the diffusion process.

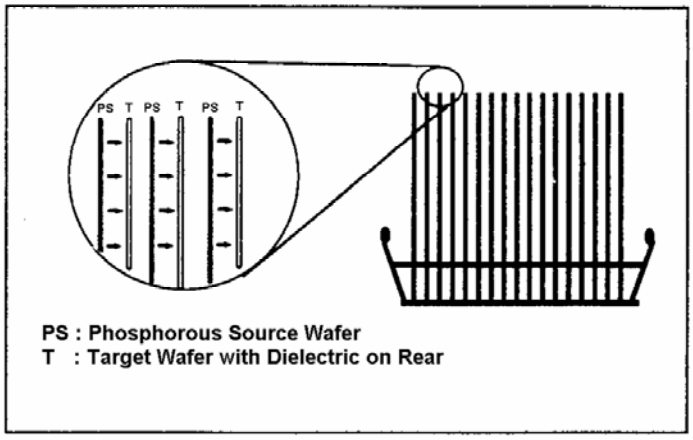


Figure 9.2 Stacking diagram showing the load positions of source and target wafers.

Prior to loading the target wafers, a spin-on dielectric was applied on the rear side of the wafers, which also acts as a mask to limit the cross-doping, ensuring that the n^+ emitter is formed only on the front side. Thus in a single high-temperature step, the following steps are achieved:

- n^+ emitter formation on the front side only.
- Curing of the spin-on dielectric layer on the rear.
- High-quality front and back in-situ oxide for superior surface passivation.

9.3.2 Desirable properties of the dielectric layer for the rear surface passivation

The dielectric layer at the rear surface should have the following properties:

- Low SRV to reduce the recombination of minority carriers at the rear surface.
- Good passivation even after the high temperature contact firing step in the belt furnace.
- Low charge density to limit the formation of an inversion layer on the rear side that could cause parasitic shunting due to the leakage of the minority carrier electrons from the rear contacts.

- Compatibility with the fire-through process sequence allowing the formation of uniform LBSF through the vias.
- Low absorption and formation of effective back surface reflector in conjuction with the metal cap.
- Low-cost growth or deposition.

In this study, a stack dielectric layer comprising of a spin-on dielectric and SiN_x was investigated to see its suitability for the rear surface passivation.

SiN_x deposition provides very good and stable surface passivation [49]. However, in the presence of contacts, SiN_x layer alone can lead to parasitic shunting [50] due to its high positive charge density of $\sim 2\times10^{12}$ cm^{-2} [201]. Oxide layer by itself provides great passivation due to high quality Si/SiO_2 interface, but the passivation degrades dramatically after firing of the screen-printed contacts in a belt furnace in air ambient. This led to the investigation of a stack dielectric layer comprising of a spin-on SiO_2 based dielectric layer, capped with a SiN_x layer. The properties of this stack layer were examined by means of effective lifetime and charge density measurements to ascertain its suitability to passivate the rear surface.

9.3.2.1 Surface passivation quality of the stack dielectric by effective lifetime measurements

Surface passivation quality of the stack dielectric layer was measured after different processing steps of the cell fabrication sequence (Fig. 9.1), using symmetric test structures prepared on ~2 Ω·cm planar FZ wafers. After the RCA cleaning, the spin-on dielectric was deposited on both surfaces and annealed in the tube furnace with the same recipe used to form the emitter and the in-situ oxide, but without the source wafers. SiN_x

was then deposited on top of the spin-on dielectric on both sides of the wafers. The wafers were then co-fired followed by an FGA anneal. Effective lifetime measurements were performed after each process step and are shown in Fig. 9.3. The effective surface recombination velocities were extracted from the effective lifetimes and are also plotted in Fig. 9.3.

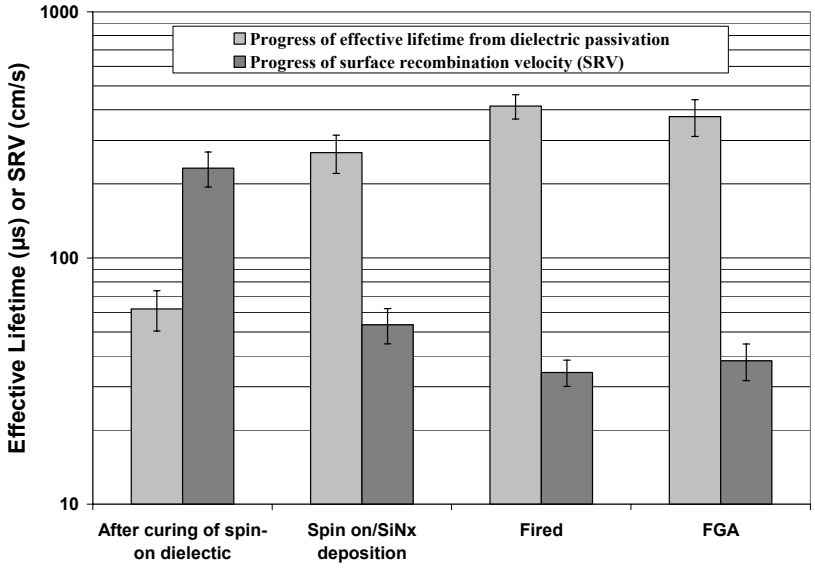


Figure 9.3 Effective lifetime progress as a function of different processing steps for the stack dielectric layer.

Figure 9.3 shows that the spin-on dielectric layer alone does not provide a very good surface passivation, with effective lifetime of ~60 µs. After the deposition of the SiN_x layer, effective lifetime improved to ~250 µs, which could be due to the hydrogenation of interface defect states during the SiN_x deposition. Effective lifetime improved further to > 400 µs after the contact firing cycle, due to the surface passivation provided by the hydrogen released from SiN_x during the firing. The effective lifetime remained at ~400 µs after the final FGA treatment. This shows that unlike thermal oxide, this dielectric stack passivation is not dependent on additional hydrogenation treatment to

passivate the surfaces after the firing cycle. This demonstrates a *good and stable* surface passivation provided by this low-cost stack dielectric. The SRV progress for different stages in Fig. 9.3 shows that the stack dielectric provides low SRV values of < 40 cm/s after contact firing. It was found that without the presence of the SiN_x cap layer on top of the spin-on dielectric, the passivation quality degrades significantly to < 5 μs after the firing step and an additional hydrogenation step such as the FGA is required to recover the passivation. This behavior is similar to the thermal oxide passivation and also shows that the spin-on dielectric alone cannot be used for rear surface passivation.

Implied V_{oc} measurements were performed to study the combined effect of the passivation quality of the rear dielectric layer and the emitter surface passivation provided by the in-situ oxide capped with SiN_x AR coating on the front side. Implied V_{oc} measurements were performed on ~2 Ω·cm FZ wafers with an emitter sheet resistivity of ~85 Ω/sq. Figure 9.4 shows the change in implied V_{oc} at various stages of the fabrication sequence.

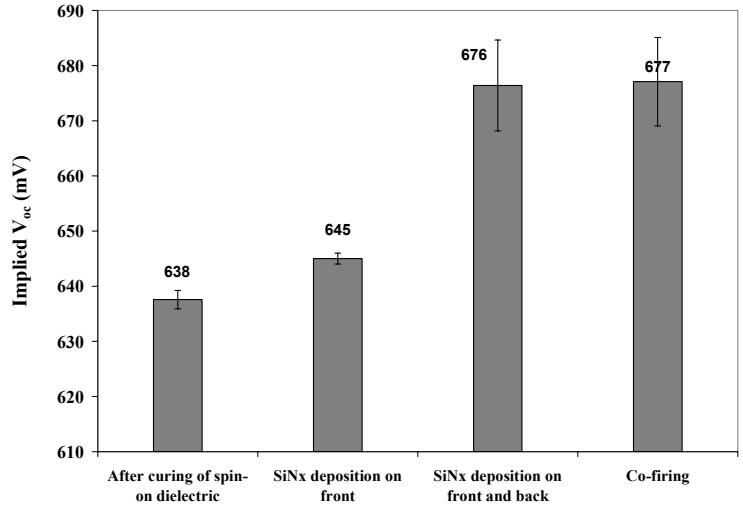


Figure 9.4 Implied V_{oc} progress on ~2 Ω·cm FZ wafers with ~85 Ω/sq emitter on one side, and surfaces passivated by stack dielectric on the rear and in-situ oxide capped with SiN_x on the front.

Average implied V_{oc} after curing the rear dielectric combined with in-situ oxide formation on ~85 Ω/sq emitter was only 638 mV. This improves slightly to 645 mV after the SiN_x deposition on the front surface. However, after the SiN_x deposition on the rear, implied V_{oc} improved significantly to 676 mV and stayed at 677 mV even after the contact co-firing cycle. This again supports the high-quality and stable surface passivation provided by the stack dielectric.

9.3.2.2 Determination of charge density in the stack dielectric layer

A low charge density is important for the dielectric layer that passivates the rear. The dielectric charge density and polarity were measured using a SemiTest SCA-2500 surface charge analyzer tool that allows a measurement of a flat-band equivalent charge density, Q_{FB} (total charge density at the flat-band condition) in the dielectric. Fig. 9.5 shows the charge density in the dielectric layers, measured on the test structures, fabricated on planar ~2 Ω·cm FZ wafers, at different stages of cell processing.

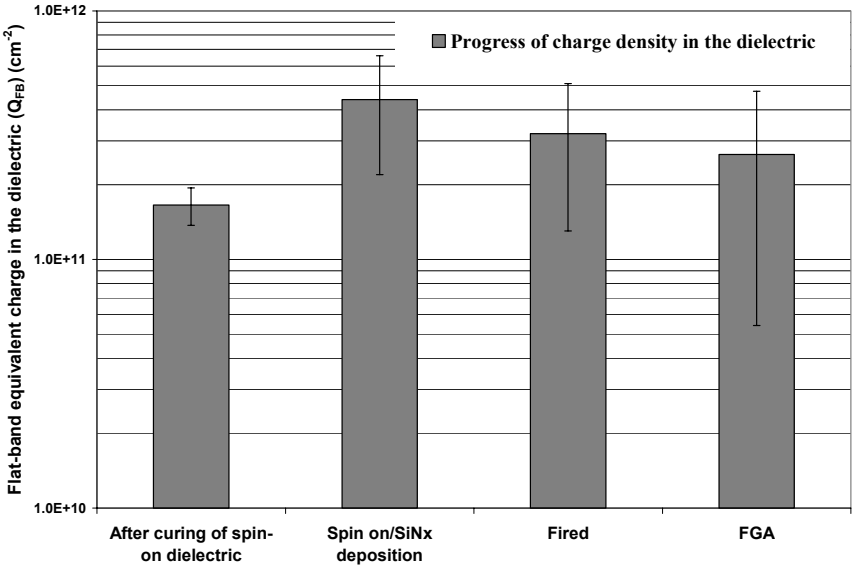


Figure 9.5 Progress in charge density of the stack dielectric layer as a function of the different processing steps.

Charge density in the dielectric layer was reasonably low (~1.7 $\times 10^{11}$ cm^{-2}) after it was cured at high-temperature in the tube furnace. After the SiN_x deposition, charge density increased to ~4 $\times 10^{11}$ cm^{-2} and then decreased to 2-3 $\times 10^{11}$ cm^{-2} after firing and the FGA treatment. Compared to the charge density of ~2 $\times 10^{12}$ cm^{-2} in the SiN_x layer [201], the charge density in the stack dielectric layer used in this study was much lower and, therefore, could minimize the inversion layer induced parasitic shunting, which leads to a loss in J_{sc}.

9.3.3 Development of a low-cost metallization process to form local BSF and rear screen-printed contacts fired-through the dielectric layer

Section 9.3.2 showed that the novel stack dielectric layer is able to provide very good surface passivation and has a low charge density. However, these properties have to be combined with a suitable low-cost metallization technique. To keep the cost down, a fired through metallization sequence, without opening the dielectric locally, was developed. Screen-printed Al dots were fired through the dielectric stack. Although the rear contact metal coverage was only ~5%, it is still highly desirable to form a local BSF underneath the contacts to keep the contact recombination low and to avoid the parasitic shunting. The quality of the contacts was assessed through scanning electron microscopy (SEM) images, effective lifetime measurements, and suns V_{oc} measurements.

9.3.3.1 Study of the contact quality by SEM imaging

Test structures were developed by printing Al dots on top of the rear dielectric stack and by firing in a belt furnace using the co-fire recipe. The openings in the screen were 100 μm × 100 μm with 800 μm spacing. This gave round screen-printed Al dots

ranging from 120-170 μm in diameter. The uniformity in the thickness and the height of the dots across the wafer depends on the print setting such as the squeegee pressure and its uniformity and the snap-off distance. Care was taken to print the dots with uniform thickness to avoid variations due to print quality. Fired samples were cleaved through the Al dots and SEM images were taken to determine the depth of the BSF. Reference FZ wafers that were processed simultaneously, but with full area Al-BSF on rear were also imaged to compare with the thickness of the local BSF formed by the point contacts. Figure 9.6 shows the cross sectional SEM micrograph of the reference full area Al-BSF wafer.

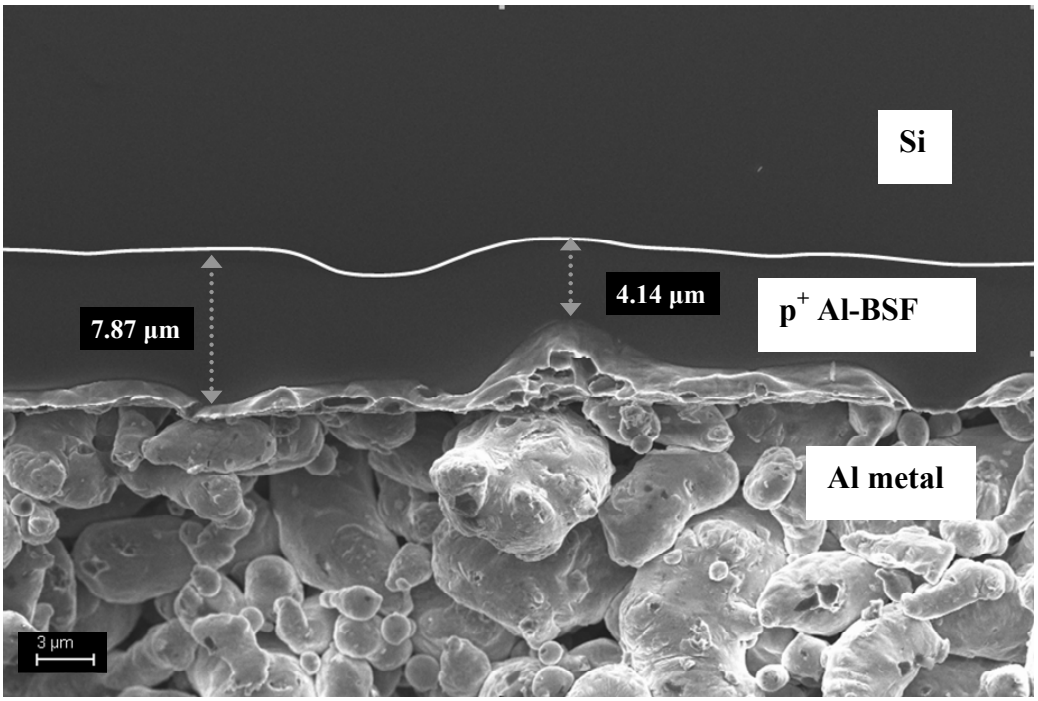


Figure 9.6 Cross-sectional SEM micrographs of the full area Al-BSF region showing the BSF thickness variation from ~4 μm to ~8 μm. White line is a guide to the eye.

The full area Al-BSF region, underneath the metal contact, was found to be ~4 μm to ~8 μm deep.

Cross-sectional SEM micrographs were also taken for the LBSF region. Figure 9.7 (a) and (b) show the cross-sectional SEM images of two consecutive Al dots that were fired-through the stack dielectric to form the local BSF.

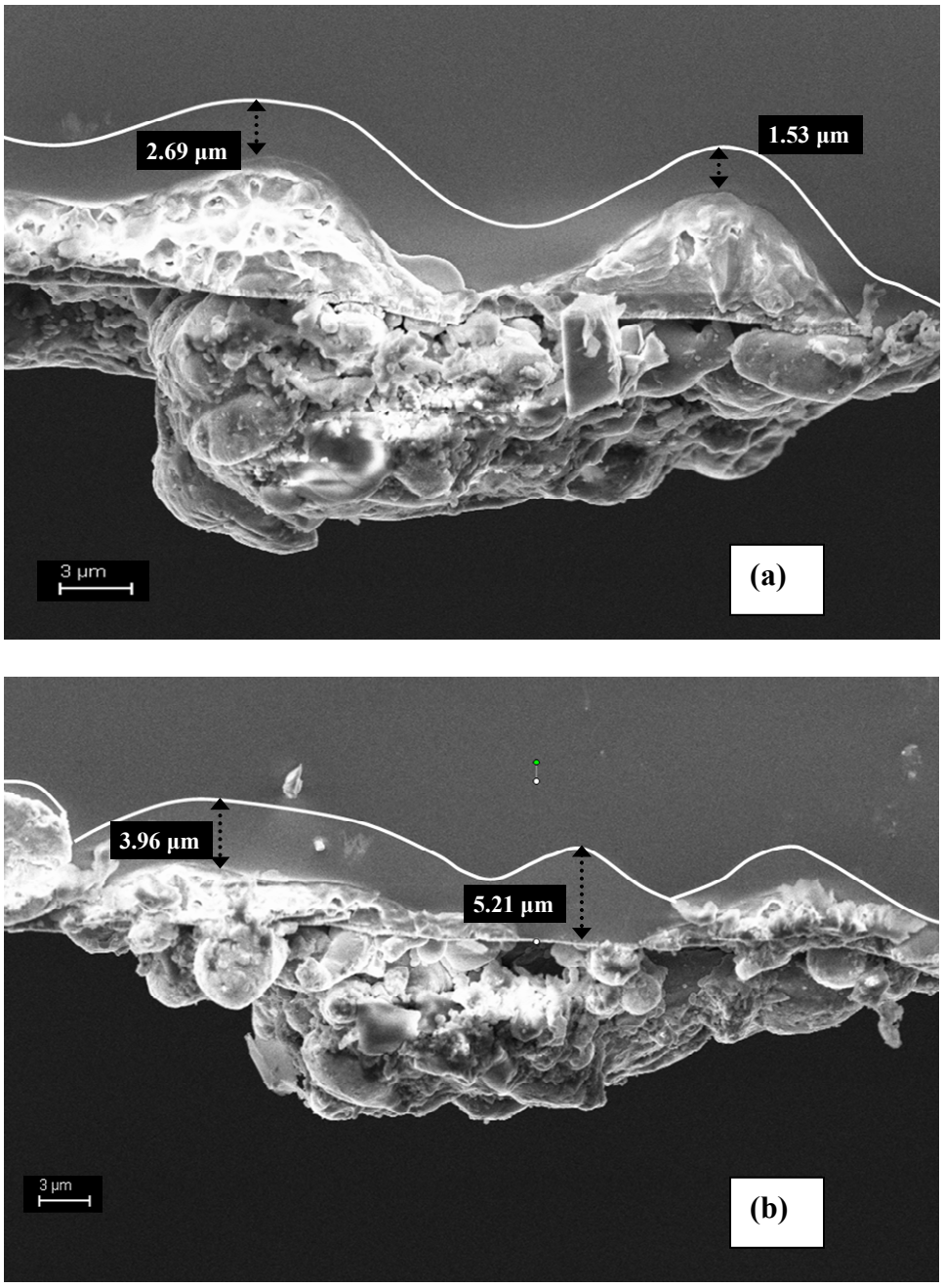


Figure 9.7 Cross-sectional SEM micrographs of the LBSF region underneath two consecutive Al dots that fired-through the stack dielectric. White lines are a guide to the eye.

Figure 9.7 (a) shows that the thickness of the LBSF region directly underneath the dot was between 1.5 and 2.7 μm. The LBSF becomes shallower on moving away from the center of the dot to the periphery. The LBSF region underneath the adjacent Al dot (Fig. 9.7 (b)) varied between 4 μm to 5.2 μm but at some places near the periphery of the dots, the LBSF became < 1 μm deep resulting in some disconnections. It should be noted that the thickness and uniformity of the BSF region depends on the peak alloying temperature, the ramp-up and ramp-down rates of the firing profile, and the thickness of the screen-printed Al layer [63, 202]. The co-firing profile used in this study was optimized to simultaneously yield a good quality front and back contacts. The height of the screen-printed Al dots also varied from the center of the dot to its periphery. This combined with somewhat non-uniform punching resulted in some non-uniformity in the LBSF thickness. Nevertheless, Fig. 9.7 shows that the Al dots were able to fire-through the stack dielectric in most regions to form contact and LBSF underneath the dielectric, although non-uniformly. It is important to realize that the formation of the LBSF region is important not only to reduce the recombination at the local contact regions but also to reduce the parasitic shunting of the electrons leaking to the back contact in the absence of LBSF.

9.3.3.2 Effective lifetime measurements to determine the impact of LBSF on rear surface passivation

Effective lifetime measurements were performed on a symmetric test structure. The dielectric stack layer was deposited on both sides of a planar ~2 Ω·cm FZ wafer. On one half of the wafer, aluminum dots were screen-printed on both sides and fired. The other half was fired without printing any metal. Effective lifetime measurements were performed directly on the half that had no metal. Al dots were chemically etched before

performing the effective lifetime measurements on the other half. Figure 9.8 shows the effective lifetimes and the corresponding SRVs on the two structures.

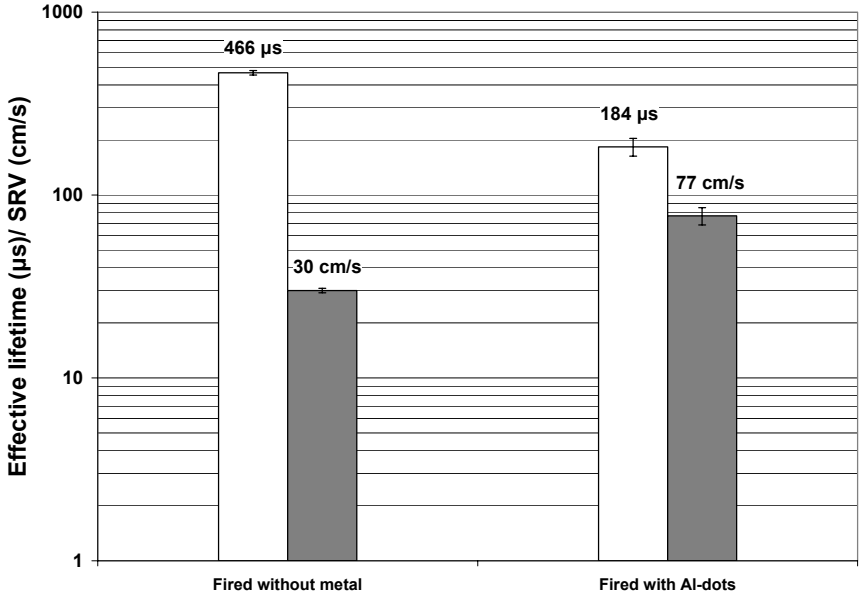


Figure 9.8 Effective lifetime measurements on stack passivated FZ wafers, fired with and without the Al dots. Corresponding SRVs are also shown.

Figure 9.8 shows that with the LBSF, the effective lifetime was 184 µs, as opposed to 466 µs in the absence of LBSF. Although the effective lifetime dropped significantly after firing with the Al dots, an average value of 184 µs represents a satisfactory quality of LBSF with ~5% coverage on the rear.

Due to the high-quality FZ material used in this study, the diffusion length (L_n) of the minority carriers is comparable to the spacing of 800 µm between the rear Al dots. Hence, the recombination of the minority carriers is controlled by an area-averaged recombination velocity given by [203]:

$$S_{eff} = rS_{metal} + (1-r)S_{dielectric}, \tag{9.1}$$

where S_{eff} is the effective SRV, r is the metallization area ratio, S_{metal} is the SRV at the metal contact, and $S_{dielectric}$ is the SRV at the dielectric/Si interface. Putting the values of

S_{eff} and $S_{dielectric}$ from Fig. 9.8 and assuming a 5% metal coverage, Eq. 9.1 gives the value of S_{metal} to be 969 cm/s. S_{metal} value of <1000 cm/s also supports the existence of local BSF underneath the contacts since the SRV at the metal-Si interface in the absence of a BSF is ~10^5-10^6 cm/s.

9.3.3.3 Suns V_{oc} measurements to study the contact quality

To further study the quality of the fired-through rear contact, suns V_{oc} measurements were performed on test structures by printing the front Ag grid, rear Al points and then co-firing the ~2 Ω·cm FZ wafers with emitter sheet resistivity of ~85 Ω/sq. Middle bar of Fig. 9.9 shows the suns V_{oc} after the co-firing cycle and before the deposition of the rear Ag reflector. For reference, the *implied* V_{oc} of the samples after co-firing, without any metal (taken from Fig. 9.4), is also shown along with the suns V_{oc} for the full area Al-BSF structure.

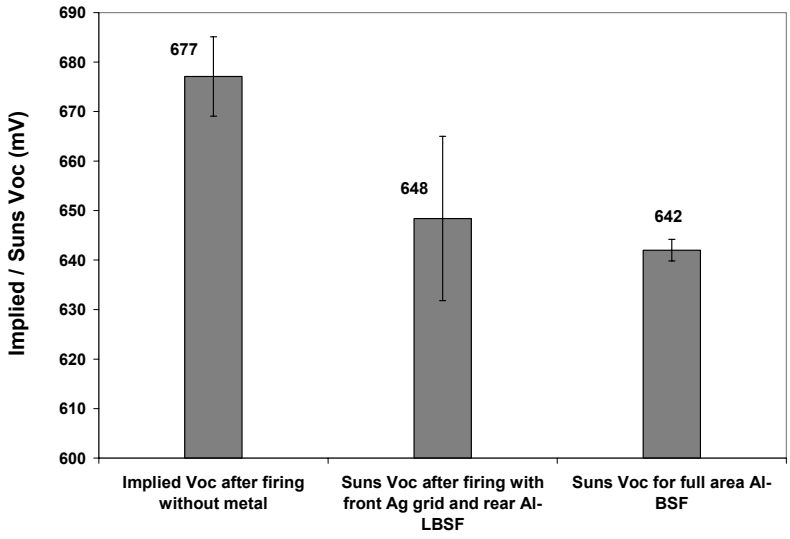


Figure 9.9 Suns V_{oc} of test structures after co-firing with metal contacts. The implied V_{oc} is also shown as reference for sample fired without any metallization, taken from Fig. 9.4.

An average implied V_{oc} of 677 mV, after firing without any metal contacts, dropped to suns V_{oc} of 648 mV when metal contacts were applied. Thus an average loss of 29 mV is incurred due to the added recombination occurring at the metal contacts. The suns V_{oc} for the full area Al-BSF sample was only 642 mV, which is 6 mV lower than the LBSF sample. Suns V_{oc} as high as 667 mV was measured for the ~2 Ω·cm LBSF sample which indicates towards a good quality of the local BSF, at least in some regions, and also a good surface passivation provided by rear dielectric.

9.4 Fabrication and characterization of low-cost, high-efficiency, screen-printed, dielectric-fired-through, thick and thin solar cells with local back-surface field

After the development of a suitable dielectric layer for back surface passivation and a metallization sequence to form the rear contact with LBSF, complete solar cells were fabricated by the process sequence shown in Fig. 9.1. This section presents the I-V results along with the detailed characterization of the fabricated cells.

9.4.1 Experimental

All solar cells were fabricated on boron doped p-type 1.7-2.3 Ω·cm FZ Si wafers with textured front surface and a planar rear surface. Emitter on the front side for all the wafers was formed using the process sequence described in section 9.3.1 with an emitter sheet resistivity in the range of 65-95 Ω/sq. The front structure of all the cells was kept the same, while three different rear structures were analyzed: 1) Full area Al-BSF 2) Dielectric fired through LBSF with evaporated Ag reflector, and 3) Dielectric fired through LBSF with screen-printed Ag paste reflector. Two different cell thicknesses (300 and 140 μm) were analyzed. Table 9.1 summarizes the devices fabricated and characterized.

Table 9.1 Thickness and rear surface characteristics of the devices fabricated in this study.

Thickness (μm)	Rear BSF	Rear Reflector
300	Full area	Screen-printed Al paste
	Local	Evaporated Ag metal
	Local	Screen-printed Ag paste
140	Full area	Screen-printed Al paste
	Local	Evaporated Ag metal
	Local	Screen-printed Ag paste

To obtain wafers with only the front side textured, SiN_x was first deposited on the rear side followed by alkaline texturing of the front side. After removing the SiN_x in dilute HF acid, wafers were RCA cleaned followed by the deposition of spin-on oxide on the rear. After the formation of the front emitter, curing of the spin-on dielectric, and the in-situ oxide formation in a single furnace anneal step, the wafers were coated with SiN_x on both sides. For the wafers with full area Al-BSF, SiN_x was deposited only on the front side and the rear spin-on dielectric was chemically etched. This ensured that all the solar cells have a similar front surface emitter and passivation and the differences in the cell performances can be attributed to the variations in the rear structure only. Nine 2 cm × 2 cm solar cells were fabricated on each 4 inch round FZ wafer by screen printing Ag paste on the front side. Al paste was screen-printed on the entire backside for the full area Al-BSF cells. For the LBSF cells, Al dots were screen-printed using a screen with 100 μm × 100 μm square openings and 800 μm spacing. Metallization area of the rear Al dots was ~5%. All wafers were co-fired in a belt furnace using optimized firing conditions to simultaneously form the front and the rear contacts. To reduce the recombination at the periphery of these 4 cm^2 devices, mesa etching was performed after protecting the surfaces with a photoresist and defining an active device area of 2 cm × 2 cm by a dicing saw. After removing the photoresist, Ag metal was evaporated on the rear of the LBSF

cells to form the back reflector. On other cells, Ag paste was screen-printed, dried at 200 °C and cured at 500 °C in a belt furnace to form the rear reflector. All wafers were annealed in FGA for 20 min to improve the front contact quality. For the thin cells, KOH was first used to thin the wafers, followed by the texturing of the front surface, such that the final thickness was ~140 µm. Thin solar cells were fabricated by the same process sequence described above except for a modification in the co-firing recipe such that the thin cells also experience the same thermal profile as the thick cells, as discussed in CHAPTER 8.

9.4.2 Lighted I-V measurement

I-V parameters of the solar cells structures listed in Table 9.1 are shown in Table 9.2.

Table 9.2 I-V parameters of solar cells fabricated on 300 and 140 µm thick FZ wafers with full area and LBSF.

Thic-kness	Rear Structure	V_{oc}	J_{sc}	Eff.	FF	n-	R_s	R_{sh}	# of cells
µm		mV	mA/cm^2	%		factor	Ω.cm^2	Ω.cm^2	
300 µm	Full area Al-BSF	645	37.9	19.4	79.56	1.11	0.5	18210	Best*
		642	37.2	19.0	79.32	1.13	0.5	16000	27
	Local BSF/ Evaporated Ag metal	648	38.2	19.2	77.41	1.22	0.7	45300	Best*
		645	37.9	18.3	74.95	1.27	1.2	83984	50
	Local BSF/ Screen-printed Ag paste	645	39.1	19.2	76.13	1.32	1.0	15540	Best*
		644	38.7	18.8	75.60	1.26	1.1	13407	22
140 µm	Full area Al-BSF	636	36.6	18.3	78.81	1.17	0.5	98270	Best*
		635	36.1	18.2	79.11	1.16	0.5	84876	18
	Local BSF/ Evaporated Ag metal	658	38.7	18.7	73.38	1.46	1.3	10290	Best*
		648	38.5	18.2	72.84	1.47	1.3	11893	18
	Local BSF/ Screen-printed Ag paste	649	38.3	18.4	74.02	1.31	1.3	6156	Best*
		647	38.1	18.1	73.20	1.46	1.2	43206	8

*** Independently confirmed by National Renewable Energy Laboratory (NREL)**

High screen-printed solar cell efficiencies of >19% were achieved on 300 μm thick wafers and >18% on 140 μm thick wafers. For the 300 μm thick cells, an efficiency of 19.4% was achieved with full area Al-BSF. This efficiency is 0.9 % higher than the best double-sided textured FZ wafers on high-sheet resistance emitter discussed in Table 8.8 of CHAPTER 8. The 0.9% difference in efficiency is due to the improved FF (lower n-factor) attributed to the mesa edge isolation. Corresponding efficiencies on LBSF cells with both evaporated and screen-printed Ag reflector were 19.2%. The LBSF cells have a higher V_{oc} and J_{sc} than the full area cells; however the efficiencies are limited by the low fill factor in spite of the mesa edge isolation. The average J_{sc} improved by 0.7 mA/cm^2 (evaporated Ag reflector) and 1.5 mA/cm^2 (screen-printed Ag reflector) compared to the cells with full area Al-BSF rear. This supports a lower BSRV and a higher back surface reflectance for the LBSF cells.

The 140 μm thick cells are able to fully utilize the benefit of the superior dielectric rear passivation. That is why the 140 μm thick full area Al-BSF cell had an efficiency of 18.3%, while the LBSF cells had an efficiency of 18.7% for the evaporated Ag reflector and 18.4% for the screen-printed Ag reflector. Average J_{sc} improved by 2.4 mA/cm^2 (evaporated Ag) and 2 mA/cm^2 (screen-printed Ag) compared to the full area Al-BSF wafers. A 22 mV enhancement in V_{oc} was observed for the evaporated Ag back compared to the full area, while the average V_{oc} improved by ~12 mV for the LBSF cells. However, the efficiency of thin LBSF cells was still limited by the low FF and high series resistance. Hence, in its present form, this fabrication sequence is not yet able to achieve efficiencies over 20% on thin substrates, and further improvements or modifications to the metallization sequence might be needed. It should also be mentioned that the 140 μm

cells with full area BSF suffered from severe bowing, which makes them impractical, however, the thin LBSF cells were not only bow-free, but also gave higher efficiencies. The best cell efficiencies in Table 9.2 were independently confirmed by NREL and are among the highest reported efficiencies on such thin devices with dielectric passivated rear and screen-printed contacts with local BSF. I-V data for the best 300 µm and 140 µm thick cells are summarized in Figs. 9.10 and 9.11, respectively, and reveal a clear enhancement in the I_{sc} and V_{oc} for the LBSF cells.

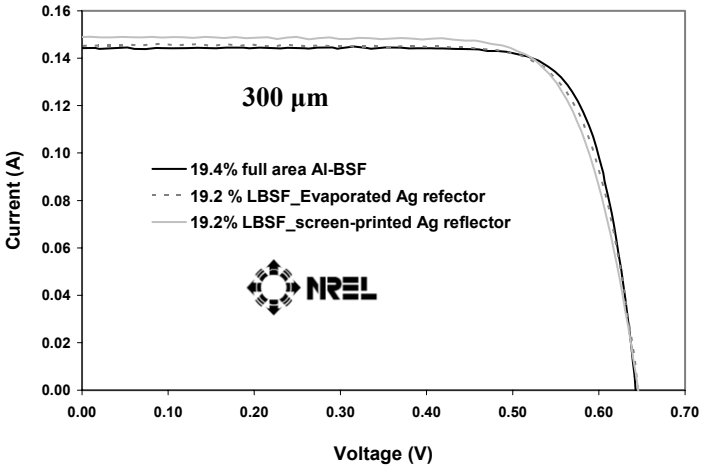


Figure 9.10 I-V curves for the best 300 µm thick solar cells from Table 9.2.

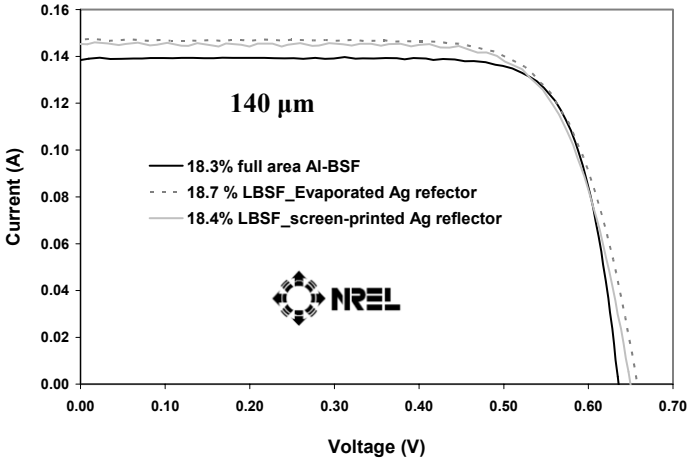


Figure 9.11 I-V curves for the best 140 µm thick solar cells from Table 9.2.

9.4.3 Long-wavelength light beam induced current (LBIC) response

Since front side of all the cells in Table 9.2 was similar for the three different rear structures, long-wavelength LBIC mappings were performed on the best cells from Table 9.2 to assess the degree of back passivation. Figures 9.12 and 9.13 show the LBIC responses with a 980 nm laser, for the 300 µm and 140 µm cells respectively.

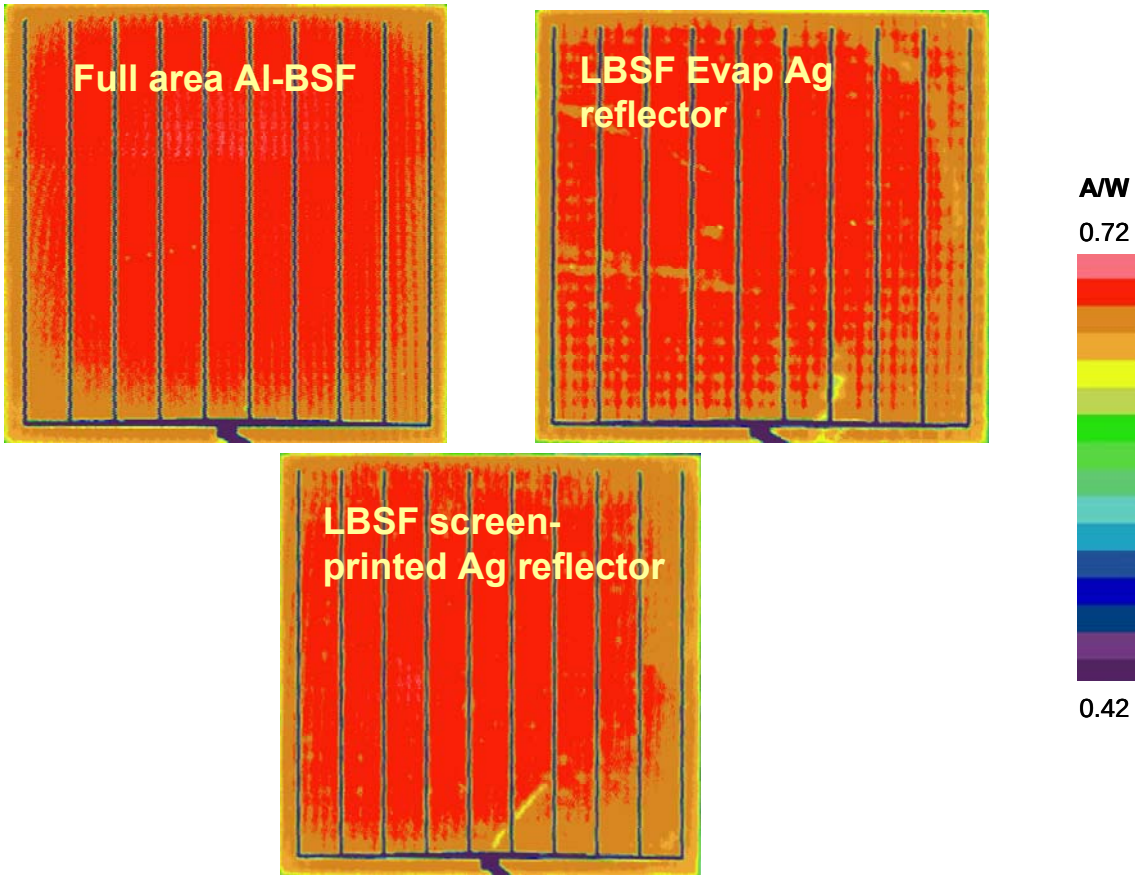


Figure 9.12 LBIC responses for the best 300 µm thick cells from Table 9.2.

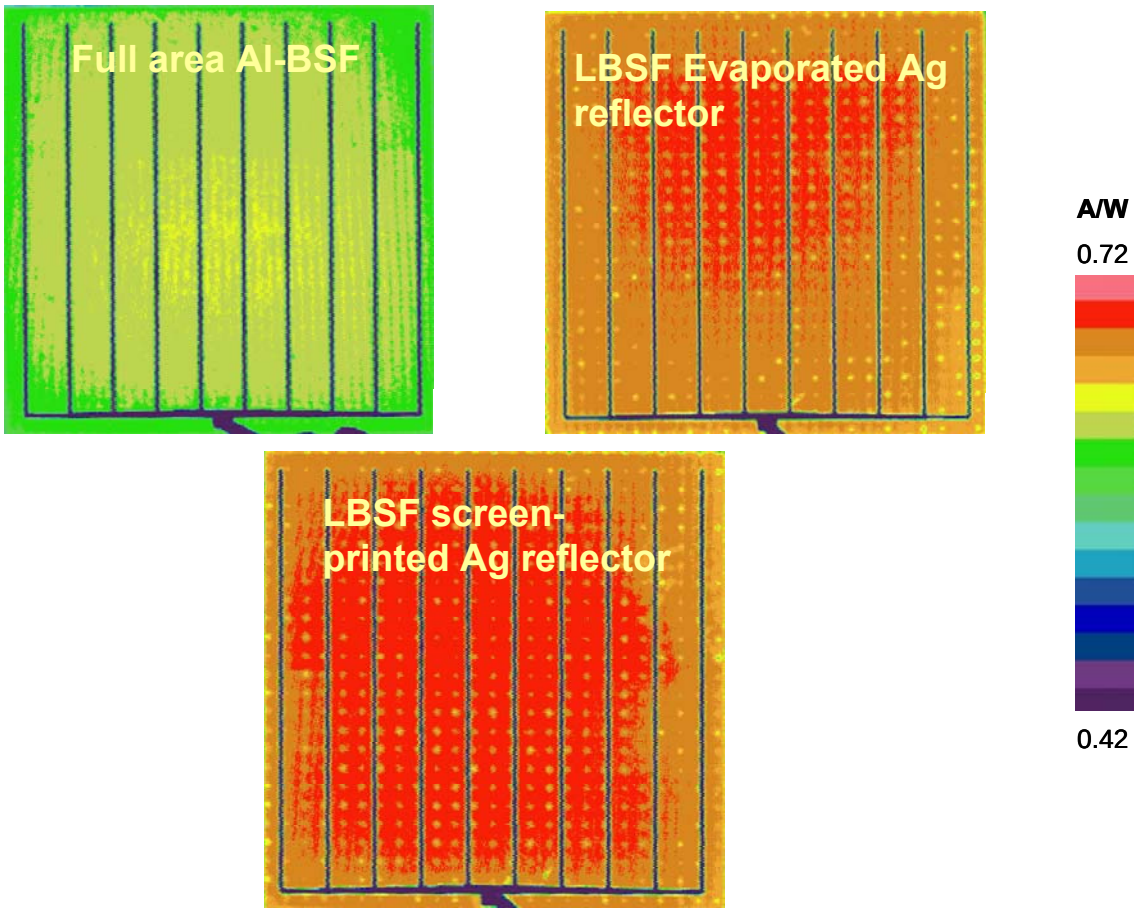


Figure 9.13 LBIC responses for the best 140 µm thick cells from Table 9.2.

The 300 µm cells showed fairly uniform and high LBIC response in the long-wavelength, however, the difference becomes apparent in the LBIC responses of the 140 µm cells. Due to the reduced thickness, the rear surface becomes more transparent to the 980 nm laser and the differences in the passivation quality of the rear surfaces become more evident. LBIC response for all the 140 µm cells was quiet uniform; however, the dielectric passivated cells have a superior response, supporting a much better rear surface passivation. This is also supported by the higher V_{oc} and J_{sc} for the LBSF cells. Notice that the rear LBSF areas show up in the LBIC map, indicating a higher recombination underneath the contact relative to the surrounding dielectric.

9.4.4 Reflectance and IQE measurements

Total reflectance was measured in the wavelength range of 300-1200 nm for the best 300 and 140 µm cells in Table 9.2. Figure 9.14 shows a comparison of reflectance as a function of wavelength for the three rear structures.

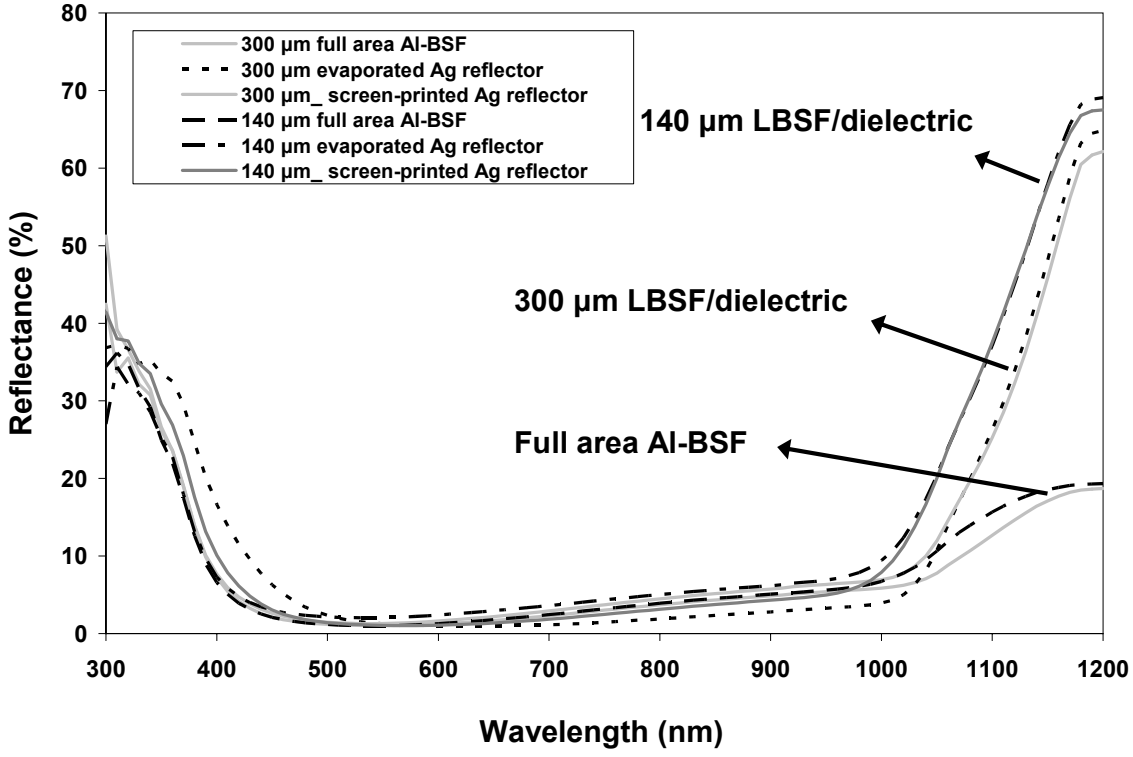


Figure 9.14 Total reflectances for the best 300 and 140 µm thick cells from Table 9.2.

Reflectance response for wavelengths <1000 nm was quiet similar. However the reflectance for wavelengths >1000 nm, which represents the escape reflectance, is much higher for the LBSF cells compared to the full area Al-BSF cells. This is indicative of a higher rear internal reflectance for the LBSF cells, which is desirable for coupling more light into the cell. As expected, the onset of the escape reflectance starts earlier for the thin wafers.

Spectral response measurements were performed on the best cells in Table 9.2 and IQE response was calculated from the spectral response and the total internal reflectance (Fig. 9.14). Spectral response measurements were performed with and without a constant 1 sun light-bias. IQE responses for the three 300 μm cells are shown in Fig. 9.15 along with the responses of the full area and the dielectric cell (screen-printed reflector) without a light-bias.

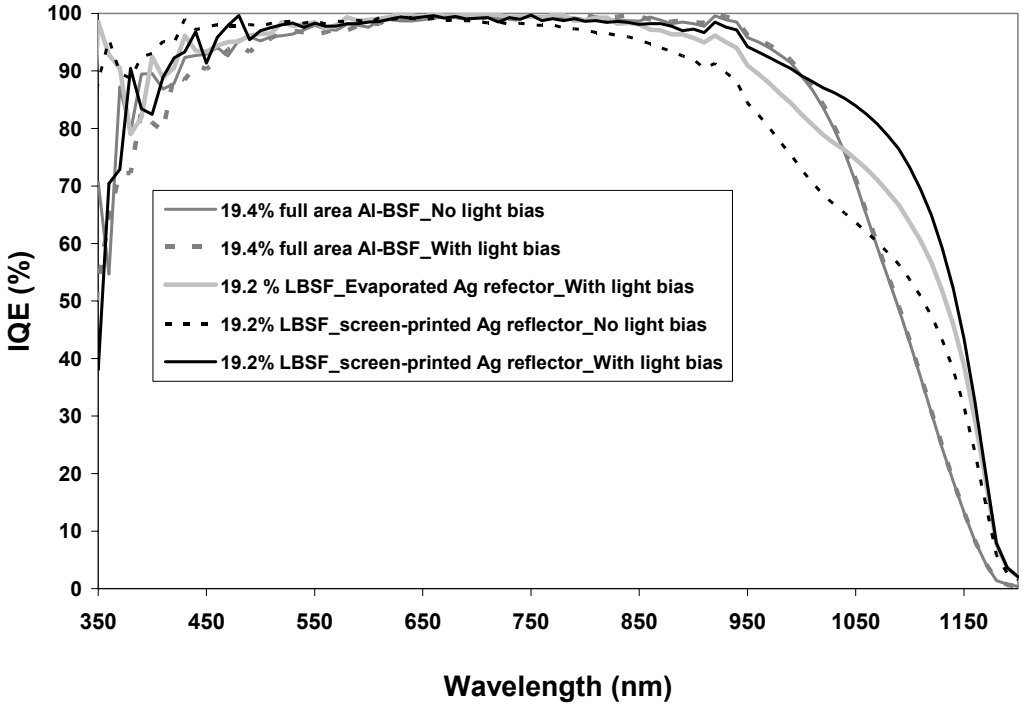


Figure 9.15 IQE comparisons for the best 300 μm thick cells from Table 9.2 with an applied light-bias. IQE response of the full area and the dielectric-passivated back (screen-printed reflector) cell without a light-bias is also shown.

There is no difference in the IQE of the 19.4% full area Al-BSF cell with and without light-bias; however IQE response of the dielectric passivated cell is very low in the long wavelength, in the absence of light-bias. However, when the light-bias is applied, which represents the operating condition of the solar cell, the IQE response for the dielectric back is significantly improved relative to the full area Al-BSF cell. This

behavior of IQE is due to the injection level dependence of the rear surface passivation provided by the dielectric and will be discussed later. The higher IQE for the dielectric cells is consistent with the high J_{sc} and V_{oc} (Table 9.2), and high long-wavelength LBIC response of the LBSF cells (Fig. 9.12).

Fig. 9.16 shows the IQE response of the 140 μm cells with light-bias.

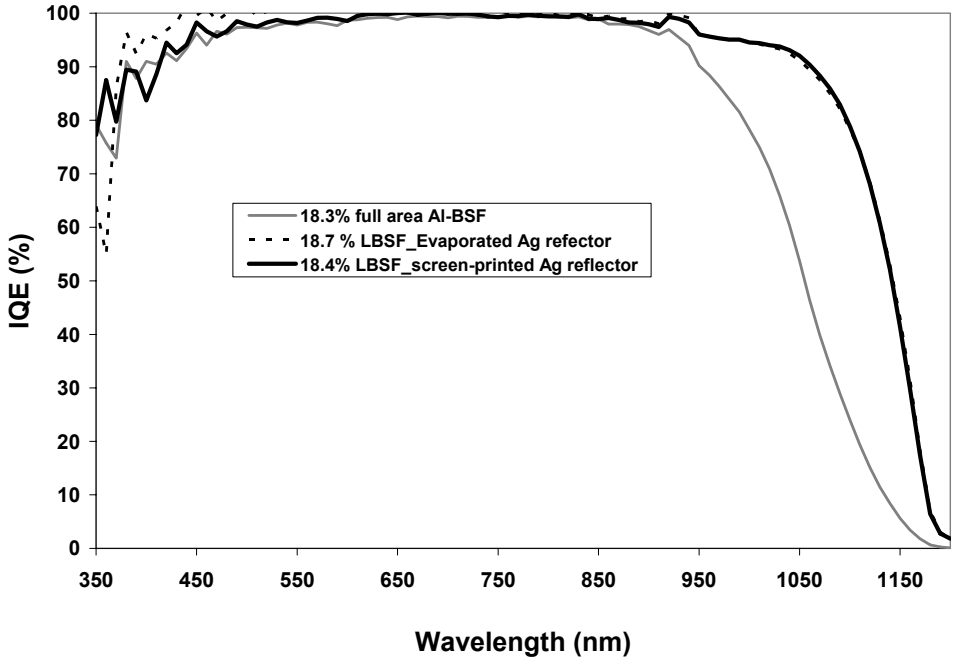


Figure 9.16 IQE responses for the best 140 μm cells from Table 9.2 with light-bias.

IQE response of the thin cells with light-bias also showed a significant improvement in the long wavelength IQE, which is consistent with the high J_{sc} and V_{oc} for the thin LBSF cells (Table 9.2). Figure 9.17 shows a comparison of the 300 μm and 140 μm cells with full area Al-BSF and LBSF cells with screen-printed reflector.

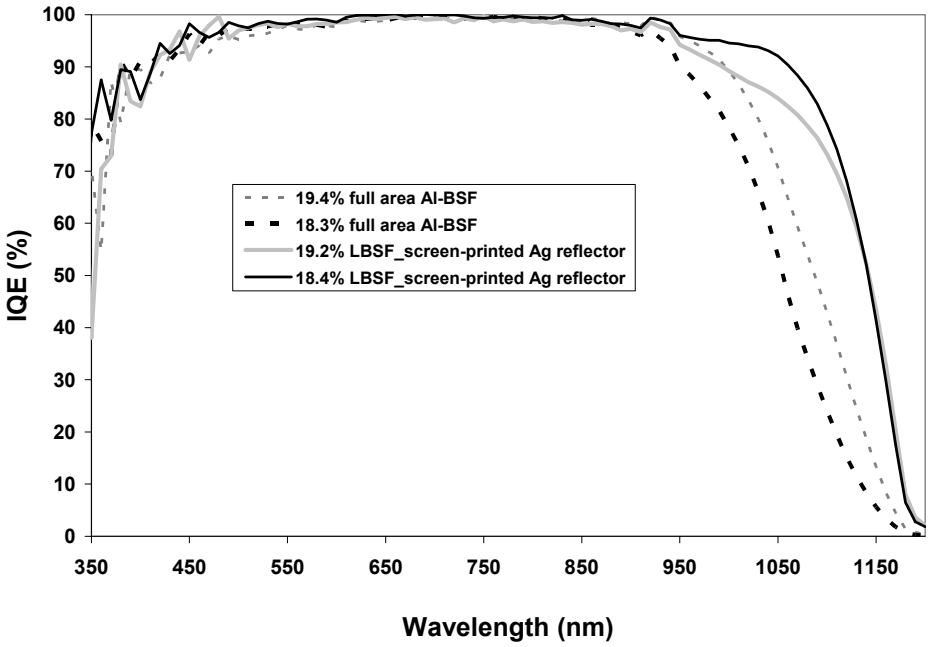


Figure 9.17 IQE comparison of the 300 and 140 µm thick solar cells with full area Al-BSF and dielectric back with the screen-printed Ag reflector.

It is interesting to note from Fig. 9.17 that thinning the device with the full area Al-BSF leads to a significantly lower IQE in the long wavelength, consistent with the lower J_{sc} for thin cells, due to a high BSRV and a low BSR, as also discussed in detail in CHAPTER 8. However, the IQE responses of the thick and thin dielectric cells are very similar, which is also consistent with the similar J_{sc} values for these cells (Table 9.2). This shows that the application of the superior dielectric passivation along with an effective BSR in this study maintains the higher J_{sc}, while using less than half the amount of Si compared to the thick cells. As mentioned previously, the reason for lower efficiency in the thin cells is poor FF partly due to a non-uniform fired through BSF and contacts. One way of achieving a better FF is by opening a vias prior to firing [204].

9.4.5 Dark I-V analysis

Dark I-V measurements were performed for the 300 and 140 μm thick cells with full area Al-BSF and dielectric cells with screen-printed Ag reflector. Figure 9.18 shows as an example, the dark I-V curves for the 19.4%, 300 μm thick full area Al-BSF cell and the 18.4%, 140 μm thick dielectric cell with LBSF.

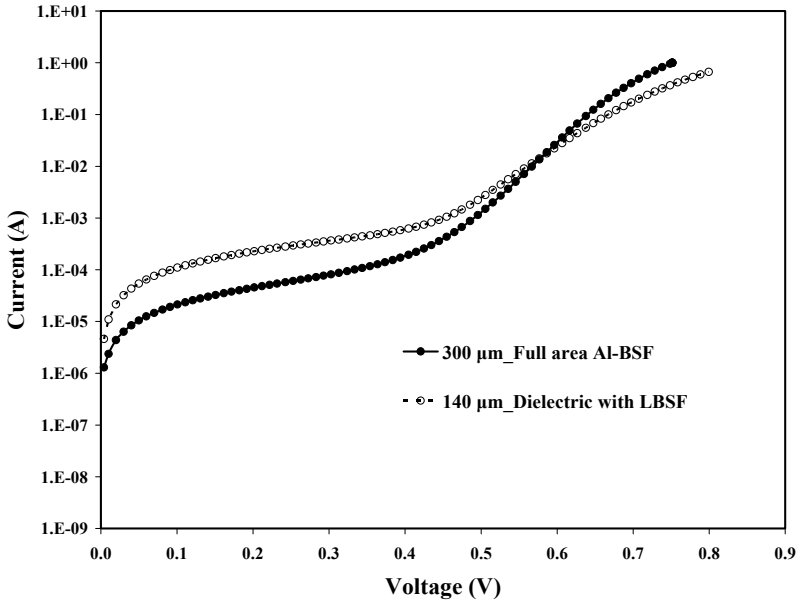


Figure 9.18 Dark I-V characteristics of the 300 μm cell with full area Al-BSF and the 140 μm thick cell with dielectric passivation and LBSF.

Measured dark I-V characteristics were fitted with the two-diode model of Eq. 2.10 to determine the J_{01}, J_{02}, and n_2. Table 9.3 summarizes the parameters extracted with the fitting.

Table 9.3 Extracted parameters from the dark I-V analysis.

J_{01}	J_{02}	n_2	Rear Structure	Thickness
pA/cm^2	nA/cm^2			
0.56	26.27	2.30	Full area Al-BSF	300 μm
0.61	335.23	2.93	LBSF_SP Ag	
0.58	24.24	2.27	Full area Al-BSF	140 μm
0.17	2.32	1.60	LBSF_SP Ag	

9.4.6 Bulk lifetime measurement

Bulk lifetime measurements were performed on 300 and 140 μm cells by etching the Al in hydrochloric acid solution and Ag metal in a mixture of nitric acid and hydrofluoric acid. After etching off the n^+ emitter and the BSF, lifetime measurements were performed by transient photo-decay technique with surfaces passivated by iodine-methanol. An average bulk lifetime of 550 μs was measured on the 300 μm thick wafers, while 140 μm thick wafers had a lifetime of 350 μs. The difference of 200 μs in lifetime for the 300 and 140 μm thick cells is not expected to cause much difference in the cell performances since the resulting diffusion lengths of 1280 μm (for 500 μs) and 1022 μm (for 350 μs) are much greater than their respective cell thicknesses.

The detailed characterization of the cells was used in conjunction with PC1D to model the cells and to extract other relevant device parameters. The results from the PC1D modeling are presented in the next sub-section.

9.5 Device modeling of the full area Al-BSF and LBSF solar cells

Device modeling was performed with one dimensional device simulation program, PC1D, to extract the relevant solar cells parameters for the full area Al-BSF cells and the LBSF cells with evaporated and screen-printed Ag reflectors. It should however be mentioned that the LBSF cells are best modeled by a two dimensional simulation, as is evident from the LBIC mappings for the 140 μm thick cells in Fig. 9.13, because SRV is different under the local contacts and the dielectric. However, for simplicity, one dimensional simulation was performed by incorporating additional elements in the basic device structure, to best replicate the dielectric passivated cells.

9.5.1 Extraction of back surface reflectance (BSR)

Back surface reflectance was extracted by matching the measured reflectance curves from Fig. 9.14 with the PC1D generated curves in the long wavelength range of 900-1200 nm, which is most sensitive to back-surface reflectance. Front surface reflectance was extrapolated for wavelengths greater than 900 nm to use as the front reflectance input for PC1D. Front surface texturing was activated in PC1D by assuming a texture angle of 54.34° and texture depth of 3.535 μm. This ensures that the enhanced front surface recombination and changes in the optical generation due to the textured front surface are also taken into account. Figure 9.19 shows as an example of the fit, the measured and PC1D calculated reflectance curves for the 300 μm thick full area Al-BSF and the LBSF cells with screen-printed Ag paste reflector. Figure 9.19 also shows the extrapolated front surface reflectance for the dielectric cell used as front surface reflectance input for PC1D. Table 9.4 summarizes the back surface reflectance parameters for the 300 and 140 μm thick cells with full area Al, evaporated Ag and screen-printed Ag on the back side.

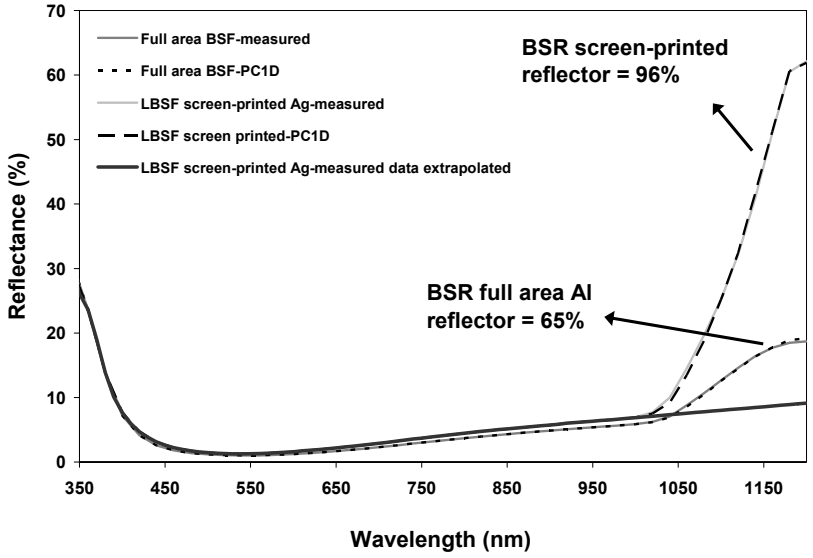


Figure 9.19 Comparison of the measured and PC1D fitted reflectance curves for the 300 μm thick full-area Al-BSF back and the dielectric passivated back with screen-printed Ag reflector.

Table 9.4 PC1D parameter for the best fit of the measured reflectance in the wavelength range 900-1200 nm.

Parameter name		Full area Al-BSF	Dielectric / Evap. Ag reflector	Dielectric/ screen-printed Ag reflector	Full area Al-BSF	Dielectric / Evap. Ag reflector	Dielectric/ screen-printed Ag reflector
Thickness (μm)		**300**			**140**		
Front internal reflection (Specular) %	First bounce	92	75	84	92	75	79
	Subsequent bounce	92	91	91	92	94	91
Back internal reflection (diffused) %	First bounce	**65**	**96**	**96**	**65**	**98**	**96**
	Subsequent bounce	65	95	95	65	97	96

Clearly, high BSR values of 96-98% were obtained with the evaporated and screen-printed Ag reflectors compared to only 65% for the full area Al-BSF. Additionally, the front internal reflection is more for the screen-printed Ag compared to the evaporated Ag for both the thicknesses. This shows that the screen-printed Ag reflectance from the rear surface is more "diffused" in nature than the evaporated Ag, which is more "specular". This diffused nature of the screen-printed reflectors is highly desirable to couple more light into the cell.

9.5.2 Extraction of FSRV and BSRV

Effective FSRV and BSRV values of the cells were calculated by fitting the measured short and long wavelength IQEs, respectively, (Figs. 9.15 and 9.16) with the PC1D generated IQEs. Measured value of the bulk lifetime, front surface reflectance (extrapolated in the long-wavelength), and resistivity were used as inputs to the PC1D model for the 300 and 140 μm thick cells. In addition, extracted internal reflectance

parameters from Table 9.4 were used for each cell structure. In the case of dielectric passivated cells, both the IQEs, with and without light-bias, were matched. Figure 9.20 shows the measured and PC1D simulated IQE response of the 19.4%, 300 µm thick cell with full area Al-BSF and the 18.4%, 140 µm dielectric passivated cell with screen-printed Ag reflector, (with and without light-bias). Table 9.5 shows the FSRV and BSRV values extracted form the PC1D fitting for the 300 and 140 µm cells.

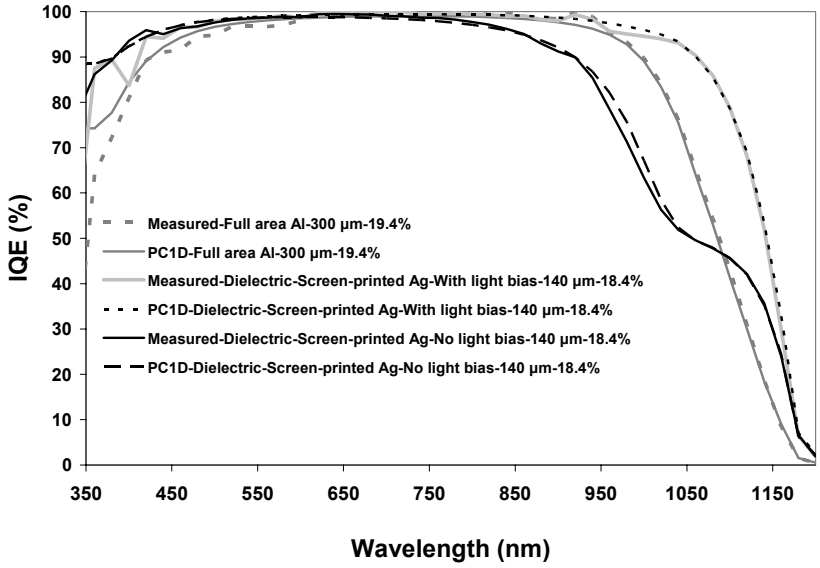


Figure 9.20 Measured and PC1D simulated IQEs of the 19.4%, 300 µm thick cell with full area Al-BSF and the 18.4%, 140 µm dielectric passivated cell with screen-printed reflector. The measured and PC1D fitted IQEs for the dielectric cell without the light-bias are also shown.

Table 9.5 FSRV and BSRV values extracted from PC1D fitting, for 300 µm cell with full area Al-BSF and the 140 µm cell with dielectric passivated rear and screen-printed Ag reflector, with and without light-bias.

Parameter name	Full area Al-BSF	Dielectric/screen-printed Ag reflector	
		No light-bias	Light-bias
Thickness (µm)	**300**	**140**	
FSRV (cm/s)	35000	18000	18000
BSRV (cm/s)	**300**	25000	**125**

Table 9.5 shows that the BSRV values for the 300 μm cell with full area Al-BSF was 300 cm/s. BSRV value for the 140 μm thick dielectric cell, without light-bias, was 25000 cm/s. This value is is high due to the injection level dependence of the stack dielectric passivation, which is discussed in the next sub-section. On the contrary, the BSRV in the presence of light-bias has a low value of 125 cm/s for the dielectric cell. Hence, under the operating conditions of the solar cell, dielectric passivation is able to provide a low BSRV value of 125 cm/s. By using the BSRV and FSRV values extracted in this section and the BSR values from section 9.5.1, these cells were modeled in PC1D to match the I-V parameters, which is discussed in the next sub-section.

9.5.3 PC1D matching of I-V parameters

PC1D was further used to match the I-V parameters of the full area Al-BSF and the LBSF solar cells, by using the extracted J_{02}, n_2 (Table 9.3), BSR (Table 9.4), and FSRV, BSRV (Table 9.5) values. The full area Al-BSF cells and the dielectric cells with screen-printed Ag reflector were simulated as representatives for both 300 and 140 μm thicknesses.

The full area Al-BSF cells were simulated using a similar basic PC1D device schematic discussed in CHAPTER 8. For the dielectric passivated cells, some additional features were added to the basic design. A positive surface charge density was applied on to the rear surface to emulate the charge density in the dielectric. In addition, a rectifier shunt diode was introduced between the inversion layer on the rear and the rear back contact to emulate the shunt path between the inversion layer and the back contact.

Figure 9.21 shows the two structures. In addition, Fig. 9.21 (b) shows the zoom-in of the rectifier shunt diode attached to the rear.

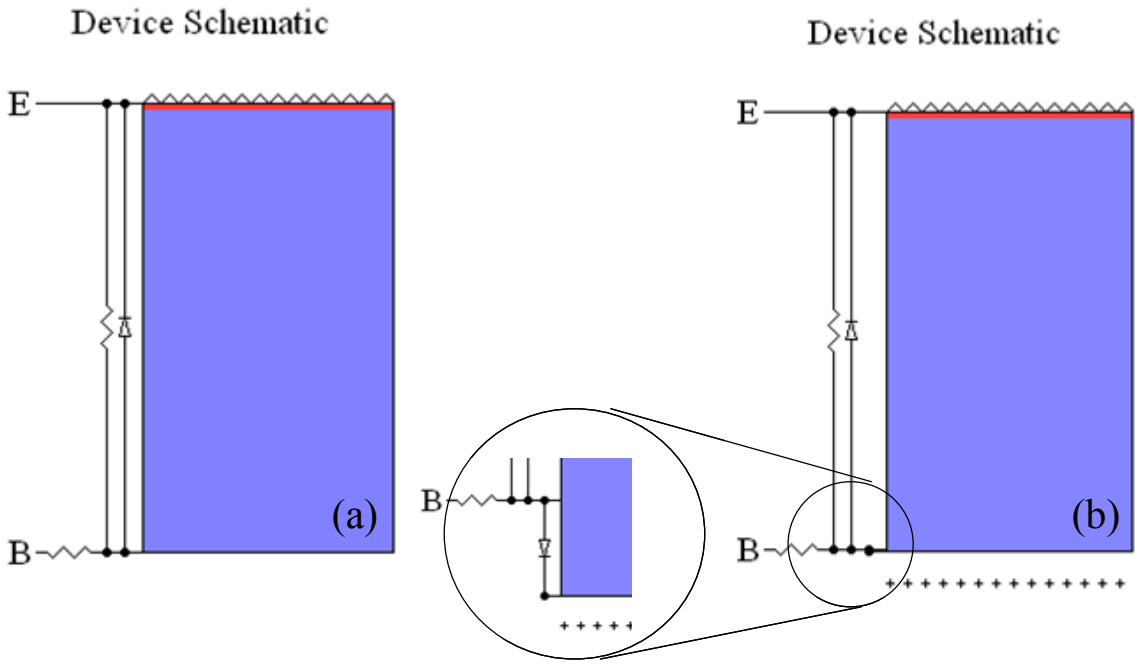


Figure 9.21 PC1D device schematic used to simulate (a) full area Al-BSF cells and (b) dielectric passivated cells. A zoom-in of the rectifier shunt diode attached on the rear is also shown.

The injection level dependence of the rear stack dielectric passivation, as discussed earlier, arises from the combination of 1) positive charge density in the dielectric 2) asymmetry of the electron and hole capture cross sections, that results in asymmetric rear surface recombination velocities for the electrons (S_{n0}) and holes (S_{p0}), and 3) parasitic shunting of the inversion layer. The S_{n0} and S_{p0} values were fixed at 1000 and 15 cm/s respectively, which represent the recombination activity of Si/SiO_2 interfaces [205]. The shunt diode on the rear was represented by a J_0 value and a diode ideality factor, which was fixed at 3.0 for simplicity. A higher J_0 value of the shunt diode would represent a more "leaky" diode and would create a low resistance shunt path between the inversion layer and the rear contact, resulting in J_{sc} loss. A lower J_0 value on the other

hand, would represent lesser parasitic shunting. The charge density in the dielectric layer was fixed at 2.5×10^{11} cm^{-2}. This value was calculated by applying a resistive shunt between the inversion layer and the rear contact with a low resistance value of 100 Ω. The charge density in the dielectric layer was then varied and J_{sc} was monitored. A high loss in J_{sc} was observed for a charge density of 1.93×10^{11} cm^{-2}, which represents the onset of shunting for a 1.7 Ω·cm material. The resistivity of the FZ wafers used in this study varied from 1.7 to 2.3 Ω·cm. Hence, the positive charge density was fixed at 2.5×10^{11} cm^{-2} for all simulations. This value is also in the range of the measured charge density shown in Fig. 9.5 for the stack dielectric. To simulate the dielectric cells, the value of J_0 for the rectifier shunt diode was varied to match the measured J_{sc}. Table 9.6 summarizes the measured and PC1D simulated I-V parameters for the 300 µm thick full area Al-BSF and the LBSF cells with screen-printed Ag reflector. Table 9.7 summarizes the measured and PC1D simulated results for the corresponding 140 µm thick cells.

Table 9.6 Measured and PC1D simulated I-V parameters for the 300 µm thick cells with full area Al-BSF and dielectric passivated cells with screen-printed Ag reflector.

Parameter name	Full area Al-BSF		Dielectric/screen-printed Ag reflector	
	Measured	Simulated	Measured	Simulated
Thickness (µm)	**300**			
V_{oc} (mV)	645	635	645	647
J_{sc} (mA/cm^2)	37.9	37.7	39.1	38.8
Efficiency (%)	19.4	19.1	19.2	19.3
FF (%)	79.56	79.8	76.13	76.85
J_0 of rectifier shunt diode (nA)	N/A		66	

Table 9.7 Measured and PC1D simulated I-V parameters for the 140 µm thick cells with full area Al-BSF and dielectric passivated cells with screen-printed Ag reflector.

Parameter name	Full area Al-BSF		Dielectric/screen-printed Ag reflector	
	Measured	Simulated	Measured	Simulated
Thickness (µm)	**140**			
V_{oc} (mV)	636	631	649	645
J_{sc} (mA/cm^2)	36.6	36.3	38.3	38.3
Efficiency (%)	18.3	18.3	18.4	18.2
FF (%)	78.81	79.92	74.02	73.67
J_0 of rectifier shunt diode (nA)	N/A		280	

Tables 9.6 and 9.7 show that the one dimensional PC1D simulation was able to match the measured I-V parameters quiet well, in spite of the two dimensional characteristics of the LBSF cells.

9.6 Conclusion

In this chapter, a dielectric stack layer and a metallization sequence was used for the fabrication of high-efficiency solar cells. The process sequence involved the deposition of a spin-on dielectric layer on the rear (planar) side of single-side textured FZ wafers. This was followed by the curing of the spin-on dielectric, formation of an n^+ emitter on the textured front side, and formation of an in-situ front oxide all in a single furnace anneal step. After the deposition of SiN_x on both sides, Ag grid was screen-printed on the front and Al dots on the rear. Front and rear local contacts were formed by co-firing in a belt furnace followed by the deposition of Ag reflector on the rear.

The dielectric layer developed was found to provide a very good surface passivation, which is stable even after a belt firing step and resulted in low SRV values of < 40 cm/s on ~2 Ω·cm FZ wafers. A high average implied V_{oc} of 677 mV was measured

on test structures after the co-firing cycle. In addition the charge density in the stack dielectric layer was found to be low (2-3 $\times$ 10^{11} cm^{-2}), which reduces the parasitic shunting of the rear contacts relative to the SiN_x layer alone. SEM micrographs of the rear local contacts showed a BSF formation underneath the contacts with an SRV value of ~1000 cm/s calculated through effective lifetime measurements. A 29 mV average loss in V_{oc} was observed after the application of the front and rear contacts, measured through suns V_{oc}. Suns V_{oc} as high as 677 mV was measured for a deielctric passivated LBSF cell after the contact firing.

High screen-printed solar cell efficiencies of 19.4, 19.2, and 19.2% were achieved on 300 μm thick full area Al-BSF, LBSF with evaporated Ag reflector, and LBSF cell with screen-printed Ag paste reflector, respectively. The corresponding efficiencies on 140 μm thick cells were 18.3, 18.7, and 18.4%. This process sequence is compatible with thin cell fabrication and resulted in bow-free devices, compared to the thin full area Al-BSF cells. The V_{oc} and J_{sc} for the dielectric cells was higher than the full area Al-BSF cells, however the efficiency of the LBSF cells was limited by the low FF and high series resistance partly due to somewhat non-uniform punch through of local contacts and BSF. Hence, in its present form, this fabrication sequence is not yet capable of achieving efficiencies over 20% on thin substrates and further improvements or modifications to the metallization sequence might be needed. Enhancement in V_{oc} and J_{sc} of these solar cells was clearly reflected in the long-wavelength LBIC and IQE responses. Device modeling in the PC1D revealed high BSR values in the range of 96-98% for the dielectric passivated cells compared to a low value of 65% for the full area Al-BSF cells. The rear dielectric stack was able to provide low BSRV values of 125 cm/s compared to a BSRV

in the range of 300-500 cm/s for the full area Al-BSF cells. I-V parameters for the dielectric cells matched quiet well with the one dimensional PC1D modeling by the introduction of a rear surface charge and a rectifier shunt diode between the inversion layer and the rear contact.

CHAPTER 10

GUIDELINES FOR FUTURE WORK

10.1 Introduction

In this chapter, guidelines are provided for work that can be performed to further improve the understanding the hydrogen diffusion mechanism in Si and to achieve high-efficiency thin solar cells using the dielectric fired-through LBSF solar cell structure. Section 10.2 provides guidelines for future work by using the novel methodology developed in this thesis to trap deuterium diffusing through the Si. Future work for the development of high-efficiency and low-cost cells with the novel solar cell structure developed in this thesis is presented in section 10.3.

10.2 Hydrogen diffusion in Si from PECVD SiN_x film

Further studies can be performed using the structure developed in CHAPTER 5 with SiN_x:D to study the effect of emitter on hydrogen diffusion in Si. Depending on the charge state of H, the presence of a junction may alter the hydrogen diffusion mechanism. By using the structure developed, the amount of hydrogen diffusing through the c-Si, with and without an emitter can be measured. Further experiments can be performed by changing the doping type of Si (n or p) to gain useful insights about the hydrogen diffusion mechanism.

The substrates used in CHAPTER 5 to trap deuterium were defect-free FZ wafers. However the diffusivity of H would be much lower in the presence of defects and traps in the bulk, especially at lower temperatures. Due to the limited release of hydrogen from SiN_x at low temperatures (< 500 °C), microwave induced remote deuterium plasma

(MIRDP) technique can be used as a source of deuterium to study deuterium diffusion at low-temperatures. Figure 10.1 shows the proposed structure.

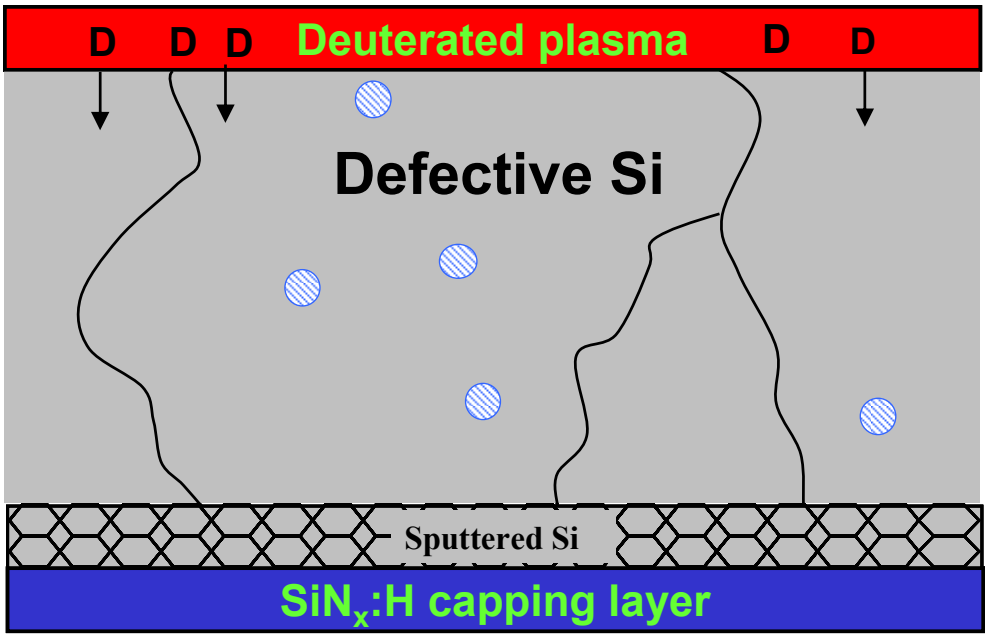


Figure 10.1 Proposed structure to study the diffusion and trapping of hydrogen at low temperatures.

MIRDP technique is able to maintain a constant and high concentration of D on the surface and can be applied at low temperatures. A SiN_x:H capping layer is required on top of the sputtered layer to block the deuterium diffusion from the rear side, to ensure that all the deuterium trapped inside the sputtered layer is diffusing through the c-Si. By varying time and temperature of the MIRDP treatment, and also the nature of defective Si, the changes in the amount of deuterium trapped in the sputtered layer can be measured. This can provide very useful information about hydrogen diffusion and trapping mechanism in Si, especially at low temperatures.

Future experiments can be performed by changing the properties of the SiN_x film (Density, thickness, index etc.) to clearly identify the critical and optimum parameters related to the release of hydrogen from the SiN_x film.

10.3 Fabrication of dielectric passivated LBSF cells

High-efficiencies of 19.2% on 300 μm thickness and 18.7 and 18.4% on 140 μm thicknesses were achieved using the dielectric passivated LBSF structure developed in CHAPTER 9; however the efficiencies were severely limited by the low FF, high series resistance and a high n-factor. In addition, all solar cells were fabricated on 4 cm^2 area, high-lifetime FZ wafers. This section proposes some of the steps that can be applied to improve the performance and to reduce the cost of the dielectric cells.

10.3.1 Improved series resistance

Further optimization of the rear SiN_x is required for a more uniform punch-through of the rear Al dots to improve the contact quality and the uniformity and depth of the LBSF on the rear. This can also be achieved through the development of the Al paste that is able to fire through the SiN_x more uniformly.

The pitch of the rear Al dots in this study was 800 μm and the resistivity of the FZ was ~2 Ω·cm. Reducing the pitch of the rear Al dots (increasing the density of dots) would lead to lower V_{oc} and J_{sc} due to increase in the contact area of higher recombination, however this would improve the FF. Additional theoretical modeling and experiments are needed to find an optimum pitch for a given resistivity that would improve the series resistance without compromising much on the V_{oc} and J_{sc}.

10.3.2 Application on low-cost and large area substrate

High-quality FZ material was used to fabricate the LBSF cells in this thesis. These materials, however, are not cost-effective. To reduce the cost, further experiments could be performed on low-quality substrates such as HEM mc-Si. Several changes in the process sequence would be required to achieve this. The curing temperature of the spin-

on oxide would have to be lowered to avoid any thermal degradation of the low-cost material. Also, the pitch of the rear Al dots will have to be optimized since the series resistance in the bulk of mc-Si materials is more due to the presence of grain boundaries and dislocations in mc-Si, which restrict the mobility of the carriers. Hence, a higher density of Al dots would be needed on the rear to achieve high FFs on mc-Si.

The typical industry standard size of solar cell is 149 cm^2 or larger as opposed to the 4 cm^2 solar cells fabricated in this thesis. Further work is needed to transform these small area cells into more cost-effective large area solar cells. To achieve this, the uniformity of the solar cells fabricated in this study needs to be improved and some changes in the processing parameters might be needed. Due to the non-uniformities in the mc-Si, it becomes more challenging to restrict the efficiency loss when the area of the solar cell is increased. The mono-cast HEM wafers discussed in CHAPTER 7 are very promising candidates for such large area cell development. This can also be achieved on single-crystal, solar-grade Cz materials. Preliminary results of the LBSF solar cells fabricated by this method were able to achieve a high and promising V_{oc} of 650 mV on 2-3 Ω·cm, 149 cm^2 Cz substrates. However, the efficiency was limited by low J_{sc} and FF.

The LBSF structure allows the use of thinner substrates. Hence, the thickness of the solar cells can be further reduced from 140 μm used in this thesis to ~100 μm. This would be even more beneficial for low-quality substrates or for substrates prone to LID.

10.3.3 Use of Al as back surface reflector

A screen-printed Ag reflector was used to fabricate the dielectric LBSF cells in this thesis. However, cheaper alternatives to the Ag paste, such as the development of an Al paste as the reflector can further reduce the cost.

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VITA

Manav Sheoran was born on September 30, 1979 in Jind, Haryana, India. He earned his Bachelor of Science in Physics from the Indian Institute of Technology, Kharagpur, India in 2001. He obtained his Master of Science degree in Physics from Georgia Institute of Technology in 2002. He is currently pursuing the Doctorate of Philosophy from the Georgia Institute of Technology in the School of Physics, under the supervision of Dr. Ajeet Rohatgi at the University Center of Excellence for Photovoltaic Research and Education. His graduate research has focused on the development of high-efficiency solar cells on thin crystalline silicon substrates by fundamental understanding of defect passivation in low-cost material and by optimizing the device design. This work resulted in over 15 publications in professional journals, international refereed conference proceedings, and workshop conference proceedings.