Early development of graphene electronics

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Abstract

Graphene has recently emerged as a material likely to complement or eventually succeed silicon in electronics. From 2001 to 2004, groundbreaking research was pursued behind the scenes at Georgia Tech; various directions were explored, including exfoliation techniques and CVD growth, but epitaxial graphene on silicon carbide emerged as the most viable route. This document provides archival information that may otherwise be difficult to obtain, including two proposals on file with the NSF, submitted in 2001 and 2003, and the first graphene patent, filed in 2003. The 2001 document proposes much of the graphene research carried out during this decade, and the 2003 proposal includes the data that was eventually published in J. Phys. Chem. B in Dec. 2004.

Note: Some personal information has been removed; original documents are available upon request.

As was typical in the early days of graphene research, the terms *graphite* or *monolayer graphite* are used in some cases where the context clearly indicates that the material in question is graphene.

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NSF 2001 (NSF proposal number 0210634)

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COVER SHEET FOR PROPOSAL TO THE NATIONAL SCIENCE FOUNDATION

3.1 Interdisciplinary Research Team

COVER SHEET FOR PROPOSAL TO THE NATIONAL SCIENCE FOUNDATION

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Project Summary: Patterned Graphite Nanoelectronics

The properties of nanoscopic graphitic ribbons are predicted to have much in common with carbon nanotubes. By tailoring their shapes (widths, passivating edge groups, edge roughness, crystallographic orientation) ribbon conductivity can be adjusted from semiconducting to metallic, just like nanotubes. Other properties that graphite ribbons share with nanotubes are *(i)* size-tunable electronic bandgaps, *(ii)* chemical robustness, *(iii)* immunity to electromigration (a major problem in nanoelectronics), *(iv)* high current capability, and *(v)* electrically tunable conductivity using the field effect via a proximal gate electrode ("gate-doping"). Just as for carbon nanotubes, carefully-prepared graphite ribbons are also predicted to be quasi-one-dimensional conductors, and possibly room temperature ballistic conductors, properties that would open new possibilities for nanoscale devices. However, in contrast to nanotubes, ribbons of different widths can be seamlessly joined, so that devices consisting of metallic and semiconducting sections can be patterned from a single graphite thin film, without foreign-metal contacts or junctions. This important property provides an easy path to large-scale integration, a goal that nanotube-based devices may never achieve. *Our vision is nothing less than a new form of large-scale integrated electronics based on ultrathin films of lithographically-patterned graphite*.

The first critical steps towards realizing this vision are embodied in a primary goal of this proposal: the development of an all-graphite field-effect transistor (grFET), which in its operation is closely related to the nanotube transistor. The grFET will not only show that robust nanoscale electronics can be realized, but will also blaze a clear path towards large-scale integration of these devices in contrast to nanotube devices.

This important goal will be achieved concurrently and interactively with investigations of fundamental properties of nanoscopic graphite objects. These investigations over a wide range of sizes include electronic and transport properties at ultra-low temperatures ($0.007\text{ K} < T < 300\text{K}$) and at high magnetic fields ($H \leq 14$ T), where quantum properties (i.e. quantum dot properties, coherent transport, quantum Hall effect) are most effectively probed.

These investigations will bear out whether room-temperature quantum confinement and ballistic transport can be achieved. This will result in a new class of ballistic transistors and devices based on the discrete electronic states in 2D graphitic quantum dots.

In order to achieve these goals the following research thrusts will be pursued:

1. Production of ultrathin epitaxial graphite films.
2. Production of graphitic nanostructures and devices.
3. Investigations of electronic properties of graphitic nanostructures and devices.
4. Investigations of transport properties of graphitic nanostructures and devices.

The team of Principle Investigators has been chosen carefully to provide complementary expertise and facilities for the project. Preliminary results of the team are encouraging.

Because it can be easily extended to large-scale integration (in contrast to nanotube electronics), the graphite field-effect transistor will rank among the most important achievements in nanoelectronics, possibly outweighing other alternatives such as molecular and nanotube electronics.

2 Introduction

The imminent end of miniaturization of silicon-based electronics due to fundamental properties of the materials involved has led to searches for alternatives. Recently many molecular-based nanoelectronics schemes have been proposed and are being actively pursued. Two of several directions that are seriously pursued are molecular electronics, where the devices are assemblies of molecules, and carbon nanotube electronics.[42–47] Both these directions derive their properties from conjugated carbon structures.

Key problems facing nanoelectronics with conventional electronic materials are:

1. *Doping*. Statistical fluctuations in the number of dopant atoms become important when the device volume is small.
2. *Electromigration*. Electrical contacts fail due to the unavoidable high current densities.
3. *Lithography*. Materials need to be manipulated and interconnected at the nanometer scale.

In principle, nanotubes provide solutions to the first two problems:

- Nanotubes are metals or semiconductors depending only on their geometry and need not be doped.[48,49]
- Nanotubes can sustain extremely high current densities without degradation.[44]

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- Nanotubes are one dimensional ballistic conductors, even at room temperature.[44,50]

The latter property demonstrates that quantum effects are important and introduces new possibilities for nanoelectronics.

On the other hand, there are serious problems with nanotubes as electronic elements:

- Basic nanotube properties (metal versus semiconductor) depend sensitively on their geometry which current production methods cannot control.[51,52]
- Nanotubes require nanoscopic metallic contacts which suffer from electromigration and large contact resistances.[53,54]
- It is entirely unclear how large-scale integration of nanotube devices is to be achieved.

Nanographite structures should retain the advantageous properties of nanotubes as an electronic material and at the same time provide attractive solutions to the problems mentioned above. Moreover, nanopatterned graphite opens the door to a host of novel electronic phenomena.

In particular, nanographite ribbons and devices are predicted to have the following properties:

- electronic structure (semiconductor or conductor) defined by geometry;[55,56]
- tunable band gaps;[55,56]
- large current capacity (as for graphite and nanotubes);
- amenable to wafer-scale lithography;
- no metal interconnects required at the device level;
- can be gated via gate structures which may themselves be graphitic;
- should be ballistic conductors[55–57] (as their nanotube counterparts[44]), which introduces a wealth of device possibilities for both high speed and low power electronics.

Besides ribbons, the properties of graphitic islands[58–63] add a new dimension to the possibilities. Graphitic islands will have quantum dot properties[61] which manifest quantum mechanical effects even at room temperature.[61]

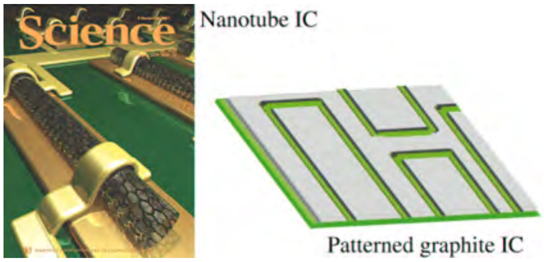


FIG 1: Left: A recent scheme for creating nanotube integrated circuits.[45] Right: Patterned graphite maintains a planar geometry, with no device-level contacts. The size scale of the patterned features would be $\sim$ 10 *nm for room temperature operation.*

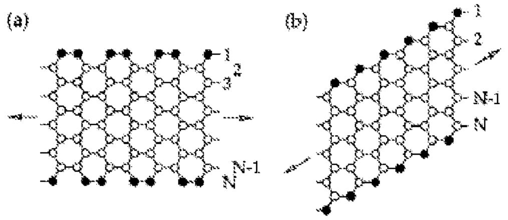


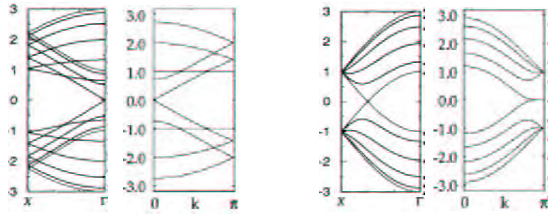
FIG 2: (a) Armchair graphite ribbon (ACGR). (b) Zigzag graphite ribbon (ZZGR). The ZZGR is predicted to be metallic, the ACGR semiconducting or metallic depending on its width (from Ref. 55).

It is telling that there are currently relatively few experimental investigations into the properties of nanostructured graphite[59,61,64–71] in comparison to the the multitudes of investigations on more complex curved nanographitic objects (nanotubes etc.). Hence, experimentally little is known about graphitic nanostructures other than the nanotubes. This is in a large part because graphene ribbons are not as easily produced as nanotubes, but also because of the extraordinary attention that nanotubes have received. It cannot be over-emphasized that there is no fundamental reason to put nanotubes on this pedestal to the exclusion of other graphitic systems, which share many of the properties of nanotubes.

2.1 Electronic properties of graphitic nanostructures

2.1.1 Graphite ribbons

A graphene ribbon[55,56,72–79] is a ribbon formed of a single layer of hexagonal graphite, while a graphite ribbon (GR) consists of several layers. Figure 2 shows the network and edge structure for GRs extending in the two most



(a) (b)

FIG 3: Calculated bandstructures for carbon nanotubes and graphite ribbons. Vertical scales are in eV and horizontal wavevector ranges span the Brillouin zone in each case. (a) Metallic armchair ribbon shown to the right,[55] nearly analogous metallic nanotube to the left.[80] Note that the 2 states at $E_F, k = 0$ are present for special ribbon widths, others have a band gap. (b) Metallic zigzag ribbon to the right[55] and nearly analogous metallic nanotube to the left.[80]

important crystallographic directions. If the edges of the ribbon have a zigzag structure, it is known as a zigzag ribbon (ZZGR). If the edges have an armchair structure it is known as an armchair ribbon (ACGR; note that the terminology refers to the long edges of the ribbons, whereas similar nomenclature for nanotubes refers to the bond geometry around the circumference of the tube).

Similarities to nanotubes. As originally pointed out by Dresselhaus[55] nanotubes (NTs) and graphene ribbons have much in common. This is clear from the comparison shown in Fig. 3. Both manifest electronic properties due to the confinement of the π electrons by the boundaries imposed by the system. In both cases, the confinement opens a gap at the Fermi level, which closes inversely proportional to the width.[49] For a nanotube the gap varies approximately as $E_{tube} = 1.2/D$ [eV] where D is the diameter in nm, while for a ribbon $E_{rib} = 1.0/W$ [eV] where W is the width in nm. The electronic properties near the Fermi level of all graphitic systems, and even conjugated molecules, are very well described in a tight-binding approximation which considers only the π orbitals.[47,56,76–78] This is primarily due to the fact that these orbitals hardly mix with the σ bonds, which in turn are far stronger than the π bonds.[81] Hence even relatively low-level theory reproduces the density of states (DOS) and wave function character for states near E_F, as compared with high-level calculations. For example, a small desktop computer can easily reproduce the published band structures of graphene bands with up to 1000 atoms per unit cell.[82] Hence, in contrast to most other electronic materials, very large graphitic systems (millions of atoms) can be reliably modeled with state of the art computers.

A very important property of both NTs and GRs is that for certain widths, two 1D subbands span the energy gap giving the structures metallic properties.[55,56] For nanotubes this occurs when the helicity index (n, m) is such that $n - m$ is a multiple of three.[49] For ACGRs this occurs when the number of hexagons (aromatic rings) across the width is a multiple of three.[55] Zigzag ribbons always have two conducting 1D subbands, which asymptotically approach the Fermi level. These bands are associated with the edge states of the ribbon.[56,60,76,78,83] For ACGRs the two 1D subbands are dispersionless, as they are for metallic NTs. On the other hand, an analysis of the wave functions of the two conducting subbands in the ZZGRs shows that they are localized at the edge atoms only at the 1D Brillouin zone boundary (i.e. for k_z=1 in normalized units). They decay exponentially from the edge towards the center of the ribbon with increasing decay length as k_z decreases to 2/3. For $k_z < 2/3$ the wave function is approximately sinusoidal (1/2-wave with nodes at the edges).[55]

The properties of multiwalled carbon nanotubes closely resemble those of single-walled nanotubes due to the weak interlayer couplings. Similar effects are expected for multilayered graphite ribbons.

Ribbon edges An important difference between NTs and GRs is that GRs have edges. Typically the edges are chemically passivated (by hydrogen for example).[58,60,69,78,83] Calculations indicate that chemical properties of the passivating groups do not distract from the general electronic structure above (as is found by introducing appropriate on-site potentials at the edges).[55,78] Passivating atoms or groups may localize carriers or introduce impurity bands, however gap size will generally not be affected. The precise effect is not known a priori however the various possible cases are interesting and can be utilized in nanoelectronic devices. While it is not expected that the passivating groups will significantly change the size of the gap, it may be, that the density of states at E_F, will be affected.

A *rough edge* (a non-ideal edge that can be characterized by additional or fewer hexagons at the edge compared with the ideal AC or ZZ edge) reduces the intensity of the peak in the DOS at the Fermi level, but does not generally open a gap at the Fermi level. Hence even rough edged ZZGRs are conducting. In contrast, theoretically, rough edged ACGRs are generally found to be semiconductors.[55,82]

Hence, in summary, as for carbon nanotubes, the electronic properties of graphite ribbons are determined by their structure. Band gaps can be tuned from about 1 eV to 0 eV by changing the width. The conducting and semiconducting properties can be tailored as well. These are highly desirable properties for nanoelectronics.

2.1.2 Graphite quantum dots

The π electrons will determine the electronic structure of very small single layer and multilayered graphite islands.[59,61,62,84] The confinement will lead to discrete quantum dot energy states. which can be probed even at room temperature due to the very low density of states at the Fermi level for nanosized objects. These graphitic quantum dots (GQDs) are expected to show interesting properties at low temperatures and high magnetic fields.[61,62,84] Investigations of the electronic properties of GQDs are invaluable to understand further the properties of ribbons, in particular those with rough edges or those consisting of domains, which may be seen as strings of GQDs.

The properties of GQDs with back gates or side gates will address questions regarding screening effects that are important for graphite nanoelectronics.

2.1.3 Transport properties

Graphene ribbons are expected to show several novel properties like itinerant ferromagnetism,[85] anomalous temperature dependent magnetic behavior[86] and zero-conductance resonances.[86] Like their nanotube counterparts, graphene junctions have been predicted to have device properties,[56] which is immediately clear from the fact that the electronic properties (semiconducting or metallic) depend on the width.[55] Hence, appropriately changing the width of the ribbon at the junction forms a semiconducting to metallic junction,[56] as shown in Fig. 4.

Multiwalled and single-walled carbon nanotubes have been found to be ballistic conductors.[44,50] Coherent ballistic transport has been demonstrated over many microns in SWNTs[50,57] and *dissipationless ballistic transport at room temperature* has been demonstrated for MWNTs[44,57] and nanotube junctions have device properties,[77] These effects will manifest in graphitic ribbons as well so that complex systems (for example islands and rings contacted with graphitic leads) can be constructed. The coherence will then manifest in mesoscopic transport phenomena[87] (universal quantum fluctuations, Aharonov-Bohm effect, quantum Hall effect), possibly at high temperatures. The experimental observation of any of these effects will be a spectacular advance for nanoscience.

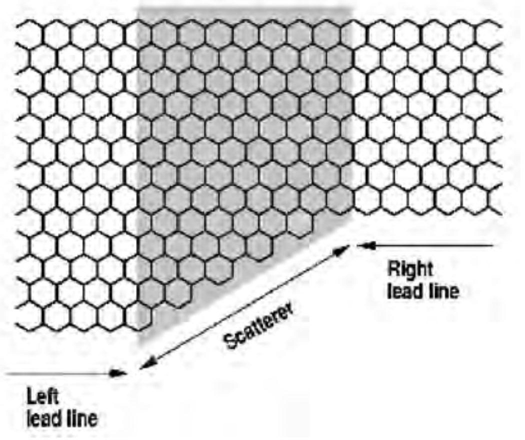


FIG 4: Example of a simple ribbon junction (from Ref. 56). The shaded central region scatters electrons coming into the junction from either of the two graphitic leads.

2.2 Patterned graphite devices

2.2.1 Contacts to graphitic nanostructures

One major consideration and potential advantage of patterned nanographite over carbon nanotubes is related to contacts. It is very difficult to make reliable, low resistance and durable metal contacts to nanotubes.[53,54] Patterned graphite will not require metal contacts since the contacts themselves are also graphitic.[56] For example a GR of 10 nm width will (generally) have semiconducting properties, while a GR of 100 nm width will be semimetallic at room temperature. These two structures can be connected seamlessly, so that there is no interface between different materials. This not only makes integration of structures far simpler, it also insures the long-term integrity of the structures. In contrast, the best metal leads to nanotubes are known to fail after relatively short times.[53]

On the other hand, the metal-graphite interface itself represents an interesting electronic system[54] due to the large disparity in the characteristics of the electrons (Fermi wavelength and Fermi energy) and dimensionality (2D or 1D versus 3D). The properties of these contacts are essentially unexplored; some inroads into this field have been made recently by two of the PIs (*de Heer, First* unpublished data).

2.2.2 The back-gated graphite transistor.

Nanotube transistors have been fabricated with both single-walled and multiwalled semiconducting carbon nanotubes.[42,43,45,88,89] The nanotubes were contacted on

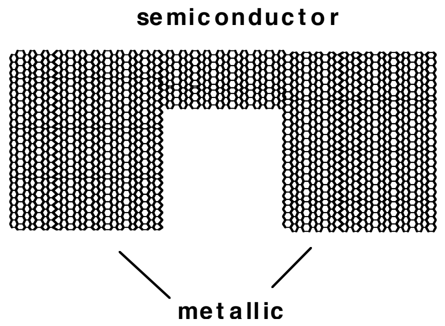


FIG 5: Graphite field-effect transistor (grFET) consisting of a semiconducting graphite ribbon (the channel) connected to metallic graphite leads (source and drain). The structure can have a buried gate or a side gate (a side gate can be patterned directly in the graphite layer).

both sides using lithographically patterned metal contacts. The nanotubes lay over a submerged gate patterned on an oxide-coated silicon wafer. A voltage applied to the gate causes the Fermi level of the tube to shift up or down towards the conduction or valence band (gate doping) which causes the nanotube to conduct, as in a field effect transistor.[42,43] This achievement was considered to be a breakthrough in nanoelectronics (NY Times, 27 Aug 2001, *IBM Creates a Tiny Circuit Out of Carbon*).

The above analysis indicates that conducting and semiconducting ribbons can be made by appropriately patterning a graphene sheet and hence graphite ribbon transistors analogous to NT transistors can be produced. However instead of metal contacts, graphite contacts can be made. For example the structure in Fig. 5 represents two conducting graphite leads connected by a semiconducting strip. If this structure is patterned on top of a submerged gate on a SiO_2 substrate (see Fig. 6) then the semiconducting strip will be made conducting by applying a voltage to the gate identical to the gating action accomplished with the nanotube transistor.[42,43,45,46,52,88–91] Note that the transistor does not require that the edges are perfect (see the previous discussion).

The transistor described above consists of a single layer of graphite. It is likely that multiple layers should function similarly, in analogy to the MWNT transistor.[89] The criterion is essentially that the fields produced by the back gate can effectively penetrate through the layers. The screening length is not known but it is large since the conductivity perpendicular to the layers is small. This will be investigated empirically. The multilayered transistor has clear advantages since it will have better defect tolerance.

When this transistor is realized it will have enormous advantages over its NT counterpart, since the entire structure is patterned graphite:

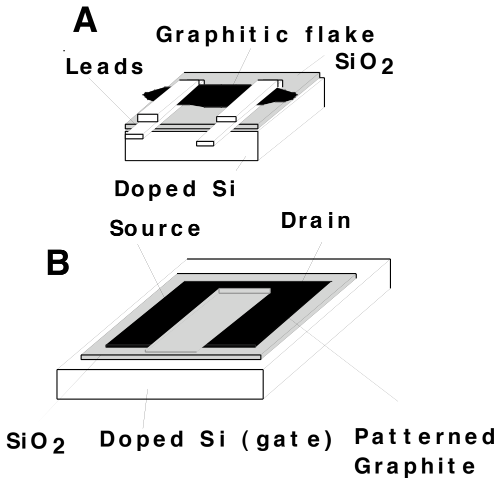


FIG 6: An example of a graphite FET composed of a graphitic flake that is laid down on two prepatterned metallic leads on a SiO2 substrate over a doped Si back gate. More metal is deposited over the prepatterned ones for better contact. B. FET composed of a patterned ultrathin graphite layer deposited on an SiO2 layer over a doped Si back gate.

- The structure does not require metal leads;
- The band gap is determined by the ribbon width;
- Perfect lithography is not required since some edge roughness will not interfere with the operation.
- When optimized lithographic methods are developed to pattern the graphite, then extended structures can be produced.
- The durability of graphite compared with the inevitable fragileness of the molecules and contacts with metals will make this technology more important than molecular electronics.

2.2.3 Ballistic devices

The grFET described above closely resemble its silicon microelectronic counterpart, where the source to drain current is modulated by adjusting the Fermi level of the channel. More ambitious devices rely on ballistic transport, which occurs when the electronic mean free path is long compared to the device size. For the very small devices considered here, it is probable that this condition is met even at room temperature, especially considering that ballistic transport on much larger scales are observed in single wall and multiwall carbon nanotubes. If the system is also quantum ballistic (i.e. the electronic coherence

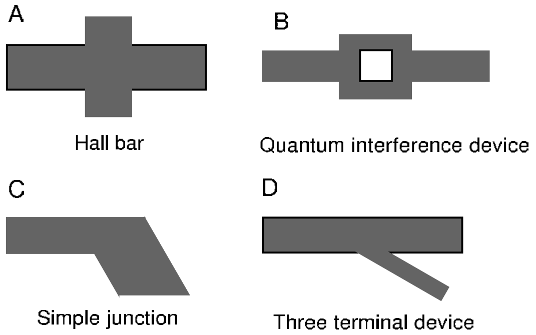


FIG 7: Generic patterned graphite structures. The device structures may be ballistic or diffusive depending on the mean free paths relative to the device size. Ballistic devices rely on phase coherent electron transmission and reflection. A. Hall bar structure (ballistic or diffusive): current flows from left to right and the potential is measured on the top and bottom leads, with a magnetic field applied perpendicular to the structure. B. Quantum interference device. (Ballistic) The current flow through the depends on the magnetic flux through the hole. This device serves as a magnetic field sensor (closely related to the SQUID). C. Simple junction, see also Ref. 56 Transmission through the junction is determined by the geometry of the junction. D. Generic three terminal device .The junction region is patterned so that it is semiconducting, while the leads are ballistic conductors. Applying a potential to the bottom lead affects the Shottky barrier at the junction and hence acts upon the electronic transmission through the device (see also Refs. 56 and 77).

length is longer than the device size), then quantum interference effects will be important for the transmission,[50,87] which opens up an entirely new paradigm for nanoelectronics. Examples of ballistic devices are the quantum interference device (QID),which is closely related to the SQUID. In this device (see Fig. 7), the electrons can take two paths from the left terminal to the right terminal, i.e. either over the hole or under the hole. These two paths will interfere with each other depending on the relative phases of the wavefunctions of the two paths. This in turn depends on the magnetic flux through the hole. Hence this device functions as a sensitive magnetic field sensor. Three terminal ballistic transistor devices (see Fig. 7D) rely on the effect that the back scattering of electrons that pass through the structure depends on the potential profile in the junction. There are several possible schemes to influence this potential. One is to construct a control lead that is coupled to the junction via a Schottky barrier, (by appropriately patterning the junction, see Ref. 56). A voltage applied to the control lead will enhance or reduce the transmission through the device, which hence functions as a ballistic transistor.

3 Projects

The patterned graphite nanoelectronics program breaks down into distinct projects. Aspects of each can be conducted in parallel. The four areas are:

1. Production of ultra-thin graphite films.
2. Production of graphitic nanostructures and devices.
3. Investigations of the electronic properties of graphitic nanostructures and devices.
4. Investigations of the transport properties of graphitic nanostructures and devices.

3.1 Production of ultra-thin graphite films
(Erbil, First, Wang)

The key to the development of large-scale integrated graphite nanoelectronics is the ready availability of single-crystal graphite films having thicknesses in the range of 1–30 graphene layers. Currently, it is impossible to grow large bulk crystals of graphite. Some preliminary experiments have demonstrated the feasibility of growing ultra-thin graphite layers on transition metals and carbides by the chemical vapor deposition (CVD) technique.[92–94] However, the growth of ultra-thin single-crystal graphite layers on *insulating* substrates is essential for the development of graphite nanoelectronics.

The goal of this part of the proposed program is to grow epitaxial graphite layers on commonly available insulating substrates or buffer layers by using the CVD technique. The growth process should produce films for initial scientific investigations as well as for large-scale device production in the future. In the CVD technique, a carbon-bearing compound is transported to the reaction zone and the formation of graphite occurs via the pyrolysis of the precursor on a surface. This process can take place catalytically in the temperature range of 700-1000 C. If the lattice match and the surface energies are compatible, the film will grow epitaxially on the substrate. During the life of the program, a close coupling will be maintained between film growth and materials characterization efforts.

We will particularly investigate three different approaches for the development of epitaxial graphite layers on insulating surfaces:

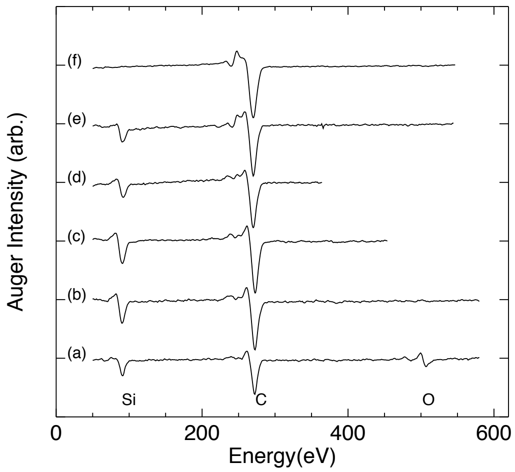


FIG 8: Auger spectra for successively higher flash-anneal temperatures of SiC(0001). (a) 950°*C, (b)* 1250°*C, (c)* 1350°*C, (d)* 1450°*C (e)* 1500°*C (f)* > 1500°*C. The data show that oxygen can be controllably removed (as SiO), followed by Si. Note the evolution of fine structure in the carbon peak as the Si/C ratio decreases (c–f). Data acquired recently by Erbil and First.*

3.1.1 Outdiffusion and CVD growth on SiC

Direct deposition of a single-crystal graphite film on the carbon surface of 6H-SiC(0001) by CVD. SiC is a wide bandgap (3 eV) semiconductor and has a good lattice match with a high order coincidence lattice.[95] SiC layer also can be grown as a buffer layer on a Si(111) wafer followed by the deposition of graphite film.

3.1.2 CVD growth on h-BN

Deposition of a single crystal graphite film on h-BN buffer layers grown on 6H-SiC surface. h-BN has a hexagonal layered structure with a band gap of 6 eV and a lattice mismatch less than 2%.

3.1.3 CVD growth on Ni/Si(111)

Deposition of graphite layer on nickel-coated silicon substrate. A thin oxide layer on the silicon wafer will be provided to slow the diffusion of nickel into the substrate[96] during the growth of the graphite layer. After the growth of the layer, a high temperature anneal will be performed to diffuse nickel into the silicon substrate. In this approach, we expect to produce films having crystallites with c-planes parallel to the substrate surface but there may not be in-plane order between the grains.

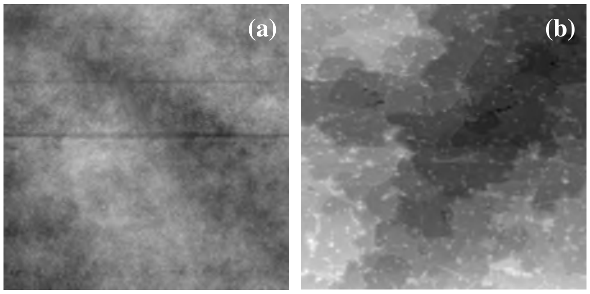


FIG 9: First attempt at graphitizing SiC (with imperfect temperature control). (a) 200x200 nm STM image of SiC after removing oxygen (see Fig. 8b). (b) 200x200 nm STM image of graphitized SiC (see Fig. 8f). Flat regions in (b) show graphite atomic structure in high-resolution images. Gray scales span 8 nm in each image. Data acquired recently by First.

The graphite films grown will be provided to the other members of the team for further physical property evaluation and device fabrication.

3.2 Production of graphitic nanostructures

Graphitic nanostructures can be formed in a variety of ways. The preferable method is lithographic patterning of deposited thin layers of graphite or graphene (see 3.1). The second method more closely resembles current nanotube technology, and relies on manipulation of self-assembled graphitic nanostructures. The graphitic nanostructures described below will be produced in the laboratories of ZL Wang, W de Heer, P. First and A Marchenkov

3.2.1 Lithographic patterning of graphitic nanostructures *(Berger, de Heer, Marchenkov, First, Wang)*

SPM lithography. This method will be used in order to demonstrate a working transistor prototype. Thin graphite platelets (micron sized) are formed by etching graphite as has been demonstrated by Ruoff[97] using the reactive ion etching process on graphite (Fig. 10). In addition, production of carbon ribbons by evaporation from a silicon carbide (SiC) electrode was demonstrated[98] (Fig. 14). These ribbons might provide an attractive alternative to platelets. The graphite platelets/ribbons are transferred to a suitable substrate (for example oxidized doped device grade silicon). The silicon wafer serves as the gate electrode. Nanoscopic patterns will be cut on these platelets using electrochemical SPM lithography. This method has been successfully applied to HOPG at our facilities by *Berger* following the procedure developed by McCarly et

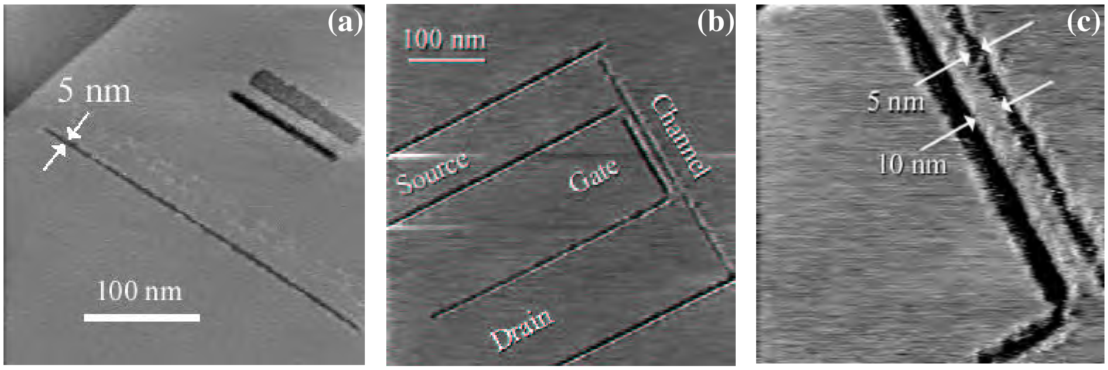


FIG 11: Examples of STM lithography on graphite. The techniques were developed very recently in our lab, following Refs. 100 and 99. (a) The three lines shown here show excellent control on width and line uniformity. (b) A patterned structure on HOPG which closely resembles ultimate side- and back-gated grFET structures. (c) Closeup of lower right-hand corner of the gate structure in (b)

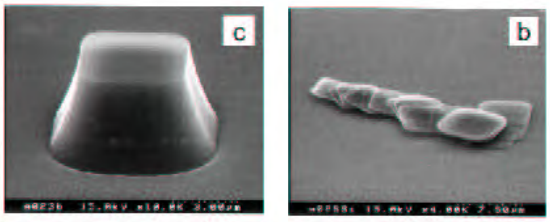


FIG 10: Left: SEM images of graphite tower created by oxygen plasma etching on an HOPG substrate. Right: SEM images of graphite platelets from tower deposited on a Si(001) substrate.[97]

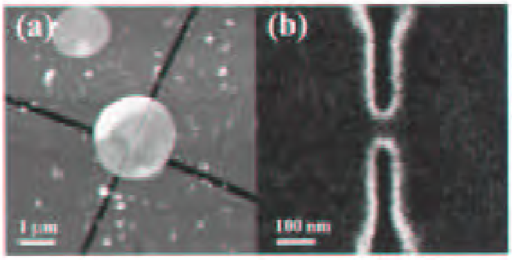


FIG 12: (a) AFM image of a 50 nm wide constriction cut into a 2.0 mm graphitic disk connected by four flat gold electrodes, which are separated by 150 nm wide grooves. (b) Detailed FIB image of a 40 × 70 *nm constriction cut into a graphitic disk. (from Ref. 64).*

al.[99] and Penner et al.[100] to produce truly impressive nanometer-sized patterns on HOPG. Feature sizes on the order of 10 nm with lines up to 300 nm long are reliably produced (Fig. 11). The Park Autoprobe SPM apparatus (see Facilities) is designed for SPM lithography. The source and drain electrodes can be produced by two methods:

1. An individual appropriate graphite platelet[97] will be located on the wafer and etched to the desired shape. Subsequently, leads will be added by evaporation methods to make contact to the graphite islands, which make the source and the drain similar to the methods to produce nanotube transistors[88] (Fig. 6).
2. Alternatively, an array of source and drain electrodes can be initially patterned on top of the SiO_2 insulating layer with the separation slightly smaller than the typical platelet size (Fig. 6a). A platelet can then be caught electrostatically to span the gap between the electrodes in a fashion similar to trapping metallic clusters and organic molecules. Subsequently, an additional layer of metal will be deposited on top of the existing electrode pattern to insure a reliable contact between graphite and electrodes. This method has the advantage of producing multiple samples on a single wafer in well-defined positions. The platelet shape can be modified subsequent to the electrode production.

Focused ion beam lithography. Focused ion beam (FIB) lithography has been successfully applied to thin graphitic structures. With this method lines have been cut in thin graphite islands with a precision of several nanometers.[64] Structures of virtually any shape can be cut this way. Furthermore, the method allows gold electrodes to be patterned by decomposing organometallics with the FIB. This method has successfully applied by Ebbesen who produced a 50 nm wide 50 nm wide graphite ribbon which connects two larger graphite islands[64] (see Figs. 12 and 13). *Marchenkov* will perform the FIB lithography at the NSF-sponsored National Nanofabrica-

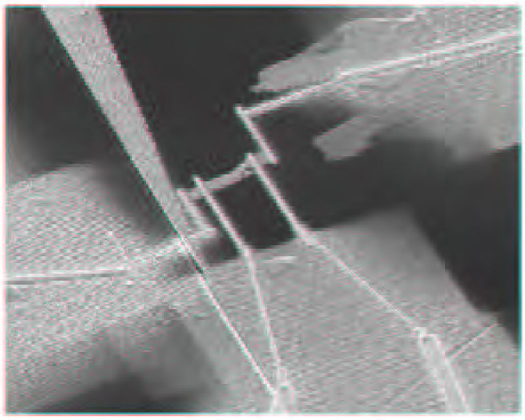


FIG 13: AFM image of a 4 electrodes system on a small graphene tape of around 2 sheets thickness and 100 nm width (F. Armand, M. Normand, V. Huc T. Ebbesen, H. Lezec[101]).

tion Network facilities. Note that the Georgia Tech Center for Nanoscience and Nanotechnology (under the direction of *Wang*) is in the process of acquiring a FIB lithographer.

Electron beam lithography. E-beam lithography methods will be used in order to produce and pattern a desirable electrode pattern on silicon and silicon carbide wafers, using standard methods.

In addition, conventional e-beam lithography methods will be attempted at the later stages of the project to fabricate integrated circuits (IC) out of thin graphite films deposited on top of appropriate insulating substrates. Two approaches can be envisaged here, depending on the quality and subsequent treatment of the carbon film produced by the deposition on a wafer of Si or SiC:[95]

1. The desired IC pattern can be obtained on a layer of photoresist deposited on top of a thin uniform graphite layer. The IC is then obtained by a combination of standard developing and dry-etching steps.
2. The desired IC pattern will be formed in a layer of photoresist on top of the substrate appropriate for the subsequent graphite deposition. After graphitization, the photoresist and graphite deposited on top of it can be removed by standard techniques.

The School of Physics is in the process of setting up an e-beam lithography facility that will be on-line in January 2002 under the supervision of *Marchenkov*.

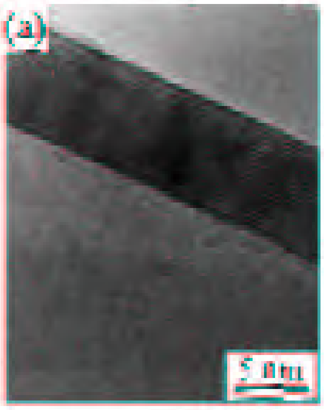


FIG 14: Graphite ribbon produced by a carbon arc in a hydrogen atmosphere.

Dip pen lithography. Dip pen lithography has recently been developed by Mirken and co-workers.[102] This experimental method uses an ambient scanning force microscope (for example the Park Instruments CP unit). The tip is used as a dip pen where the pen is first coated with a layer of water-soluble molecules which are transferred to the substrate when the tip writes over the substrate. In this way lines as narrow as 15 nm have been written both on metal as well as on semiconducting substrates. For these purposes molecules will be transferred to metal and semiconducting substrates. These molecules can be polymerized by chemical treatment or graphitized (for example by heating or e-beam illumination). Alternatively organometallic molecules deposited on the nonconducting substrate can be patterned with dip pen lithography to produce metallic lines. Two AFMs (one in WdH's lab and another in ZL Wang's lab) are suitable for this project.

3.2.2 Self assembly methods *(de Heer, Wang, Erbil)*

Arc produced graphite ribbons. Graphite ribbons have been produced in carbon arcs very similar to those used to produce nanotubes as shown in Ref. 98. The arc is struck in a hydrogen atmosphere and the electrodes are impregnated with SiC (Fig. 14). This process produces well formed graphite ribbons that can be harvested and manipulated similar to the methods developed for nanotubes. This process will be invaluable to demonstrate the properties of graphite ribbons and to produce prototype devices (closely paralleling the nanotube transistor development).[42]

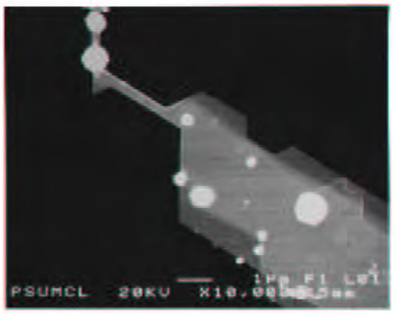


FIG 15: Secondary electron image of a graphite ribbon and diamond crystals nucleated on it. (from Ref. 103).

Microwave-plasma chemical vapor deposition. Nickel-assisted microwave CVD in a hydrogen plasma has been applied to produce impressive freestanding crystalline GRs (several 10s of nm wide and thick) by R. Roy et al.[103] (Fig. 15). These can be harvested and deposited on suitable substrates after which contacts can be applied using standard e-beam lithography methods (as is currently done with NTs.[42] Initial studies will involve obtaining material from Roy et al.[103] If this direction proves to be promising then it will be aggressively pursued and the Georgia Tech Nanotechnology Center (ZL Wang) will purchase the necessary equipment.

Etchpits in HOPG. Etch pits form in HOPG when it is heated in air.[69,104,105] The depth and diameter of the pits can be controlled to a reasonable degree by adjusting the temperature.[104] These holes occur at defects in the HOPG. When two etchpits nearly meet a narrow strip remains. This method is not appropriate to produce predetermined graphite patterns however it is a simple and well established way to produce a variety of well graphitized samples for investigations of the properties of low dimensional graphitic objects like islands and strips.

This technique has been successfully applied in *de Heer's* lab and imaged by *First* (Fig. 16).

Arc produced nanoparticles Small faceted graphitic particles ($\approx$5-50 nm) are abundantly produced in carbon arcs.[106] The particles are suspended in ethanol (using ultrasonic dispersion method) and dried on a substrate. WdH has extensive experience in the production of these nanoparticles.

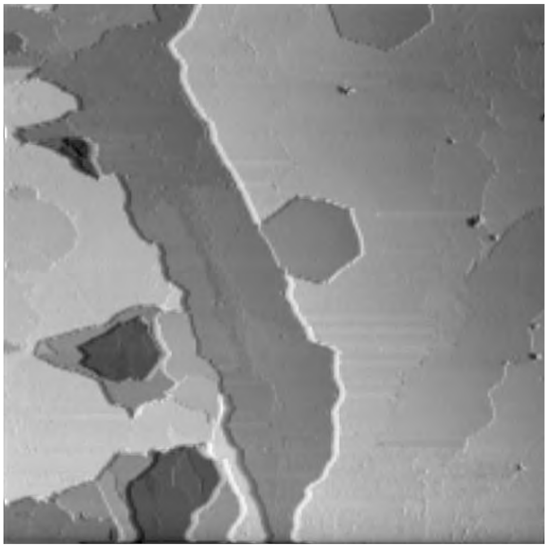


FIG 16: STM image of etch pits formed in HOPG by heating in atmosphere to 650° C. Image size 2 μm x 2 μm.

3.2.3 Structural characterization *(Wang, First, de Heer)*

The patterned graphitic structures will be characterized at the Georgia Tech electron microscopy facility. The Georgia Tech electron microscopy center has the instruments and the expertise for detailed chemical and structural characterization of the nanostructures that are produced by the methods described above. Further characterization will be performed with SPM (in air by WdH, in UHV by PF, in HV by ZLW).

3.3 Electronic properties of graphitic nanostructures & devices *(First, de Heer)*

In this project, the properties of graphene and graphite islands and ribbons will be investigated using scanning tunneling microscopy (STM) and spectroscopy (STS) in ultrahigh vacuum from 4K to 300 K and in magnetic fields up to 8 T (see Facilities). These experiments will probe the density of states (DOS) of the graphitic structures on the atomic scale. The DOS near the Fermi level will reveal directly the metallic or semiconducting nature of graphite ribbons and islands.

Investigations will begin with STS measurements of graphite steps, ribbons, and islands that occur naturally on HOPG surfaces (or ultrathin graphite films) fired in oxygen or similar atmospheres (see Sec. 3.2.2). Other self-assembled or lithographically-defined nanostructures will be studied as they become available. Due to the poor transport between graphite layers, we expect that armchair ribbons should show a distinct gap around E_F, even on the extended graphite substrate. Zigzag ribbons are expected to have a unique topological edge state at E_F (evidence already exists[67,69]) that could give rise to ballistic conduction. Maps of the spatial distribution of this state across the ribbon will be compared with calculations. For both ribbon types, we will determine experimentally the change of electronic structure with ribbon width, the effects of edge roughness and the sensitivity of the electronic structure to passivating edge groups. The effect of high magnetic fields on the ribbons (which may undergo an electronic phase transition in high fields) also will be probed.

Graphitic islands will be studied by STS concurrently with the graphite ribbons. In this case we expect that quantum dot properties will be observable at cryogenic temperatures, and perhaps higher. Energy-resolved DOS maps will be acquired in order to compare the wavefunction distribution with calculations (see also Sec. 5.3).

Patterned graphite devices can also be investigated via STM and STS. The low-temperature STM described under Facilities has connections for up to 4 contacts to the sample, sufficient for biasing many basic devices. Additionally, the sample can be positioned anywhere within a 5mm diameter circle with a $\sim$ 10 nm minimum step. This will allow nanoscale devices to be located, provided directional and identification marks are included in the lithography (the scanning range is 1.2 μm at 4 K).

In order to study the effects of gate-doping and electrostatic screening, potentials will be applied to electronic gates beneath or to the side of ribbons/islands. Such experiments (and even those mentioned previously) must properly account for the influence of the electrostatic field of the STM tip, somewhat analogous to the tip-induced band-bending on semiconductor samples.[107] The tip-field itself could be used to gate an operating grFET at selected positions along the channel. The effect on the source-drain current would provide more information on the local electronic structure along the channel (see also Sec. 3.4).

The properties of metal contacts (contact resistances and non-linear transport) and the electronic structure near metal islands on HOPG will be measured. Preliminary experiments (*First, de Heer*) have demonstrated important effects (high contact resistances, dramatically nonlinear dependence on contact area, and non-ohmic transport at high bias voltages).

3.4 Transport properties of graphitic nanostructures & devices *(Marchenkov, de Heer, Berger, First)*

A broad range of remarkable physical phenomena have been revealed through transport studies of electrons constrained to quasi two-dimensional sheets at low temperatures. For example, in the presence of intense magnetic fields, these 2D electron gases exhibit quantization of the Hall voltage to levels determined only by fundamental physical constants. Under these conditions, electrons do not exist in simple plane-wave states, but are arranged in Landau levels. The Quantum Hall Effect (QHE) is the direct consequence of the nature of these states in two dimensions. At even higher magnetic fields, the electrons further condense into unique many-body correlated states which occur at rational fractional filling $\nu = p/q$ of Landau levels (Fractional Quantum Hall Effect).

A variety of different topological 2D electron structures with nearly atomic resolution can be manufactured from graphite ribbons, sheets or films using either lithographic, or STM-based techniques. Examples include (Fig. 7) a Hall bar (QHE regime), a mesoscopic interferometer, a ribbon knee junction[56] (see also Fig. 4), and an asymmetric Y-junction, analogous to the nanotube case.[77]

Due to the presence of the morphological edges, graphitic ribbons add a remarkable twist to the multitude of electron transport phenomena studied in carbon nanotubes as well as other low-dimensional electron gases. Theoretical analysis[56] has shown that the conductance of graphite nanoribbons as well as that of the ribbon junctions crucially depends on their morphology as well as edge shapes. *Marchenkov's* group has capabilities to study electron transport phenomena on patterned structures at temperatures from 0.007 K to 300 K in the fields up to 9 Tesla (14 T with flux concentrator), which will provide detailed information on the nature of the carriers and other mesoscopic transport properties. Initially, various samples will be tested to determine the relation between the conductivity the morphology of the ribbon (width, aspect ratio, edge shape and roughness). Ribbon morphology will be determined using optical, electron, and scanned-probe microscopy methods as described above. Many of the graphite films produced at Georgia Tech will be sent to *Berger* at CNRS, who has facilities and expertise in materials characterization via transport measurements and electron spectroscopies.

Based on the energy scaling described in Sec. 2, graphite ribbons several nanometers in width are expected to show ballistic and quantum effects at room temperature. However, it is important to realize that low-temperature transport measurements will be essential for at least three reasons: 1) Characterization of material quality, 2) Fundamental measurements of electronic structure and electron-correlation effects, and 3) Low temperatures extend the size range at which ballistic and quantum effects can be observed. For the graphite structures of interest, it should be possible to observe the basic properties and device operation for ribbons tens of microns wide at the lowest temperatures. This reduces the patterning constraints to the level of optical lithography. Furthermore, high quality single-crystals of graphite are available in mm sizes (Kish graphite). Consequently low-temperature device measurements could begin immediately, independent of progress in the other project areas.

Low temperature measurements (4K) on these structures using STM methods will be carried out by *First* as previously described. Measurements of this kind have been particularly useful to characterize transport in contacted nanotubes and will do so for nanoribbons as well. It also may be possible to use the STM to do local null-current potentiometry (in the manner of a Kelvin probe) in order to map the distribution of QHE edge states.[108]

4 Education

Scientists educated through undergraduate, graduate, and post-graduate research constitute the most important means of technology transfer from universities to industry. Six Ph.D. students, 5 undergraduates, and 2 postdocs will be supported directly through this grant or associated cost-sharing. Their training is clearly the most direct benefit of this funding. However, all levels of education will benefit from the requested funds. In particular, we have noted a significant weakness in many graduate programs: stagnant Masters degree curricula. With partial support from this new funding and industrial sponsors, we hope to address this issue.

K-12 Education: Through the requested funding, the PIs will support K-12 education in several ways: 1) Through participation in the Georgia Industrial Fellowships for Teachers (GIFT) program (www.ceismc.gatech.edu/ceismc/programs/gift/homepg.htm) GIFT arranges summer fellowships for K-12 math and science teachers at several leading businesses and public science organizations (including Georgia Tech). The program is administered by the Georgia Tech College of Sciences' Center for Education Integrating Science, Mathematics and Computing (CEISMC). Last year, 80 teachers were granted fellowships throughout the state. 2) Through participation in the educational programs of the Georgia Tech Center for Nanoscience and Nanotechnology that has been established recently (*Z.-L. Wang,* Director). The new Center will establish a "Research Experiences for Teachers" program similar to GIFT, in addition to outreach programs. 3) Through less formal but more direct contact with K-12 students. Examples from the PIs experience in recent years include participation in "Science and Technology" nights at local schools, hosting lab visits for K-12 classes, loaning equipment or materials to the local science museum, etc.

Undergraduate Education: Funds to support 5 undergraduates per year have been requested specifically for the purpose of enhancing research opportunities for undergraduates. Students will work in conjunction with graduate students and postdocs on the projects described previously. Our goal is to have a student participate for at least 1 year in the research program. This is enough time for a good student to make a real contribution, and it is a sufficient basis for an advisor to write a meaningful letter of reference for graduate schools. The PIs will also continue to participate in the NSF-sponsored Research Experience for Undergraduates (REU) program administered through the School of Physics (J. L. Gole, PI). In this program, undergraduate students from around the country participate in full-time research for one summer.

Graduate Education: In the past 20 years or so, the rate at which fundamental discoveries appear in technological innovations seems to have increased. One oft-cited example is the phenomenon of "giant magnetoresistance," which went from discovery to computer hard-drives in about 7 years. This is not much more than one generation of Ph.D. students. There is a need for technology transfer and training on a time scale shorter than can be accommodated through Ph.D. research, yet with more depth than is possible at the undergraduate level. Vibrant Masters degree programs could help substantially.

We propose to develop a new Masters degree specialization: "Science at the Nanometer Scale," to be offered through the Schools of Physics, Chemistry, and Materials Sciences and Engineering. Furthermore, we hope to secure industrial sponsorship of graduate fellowships specifically for Masters study in this field. The degree program would consist of at least two special interdisciplinary courses (also open to Ph.D. students) and 1 year of focussed thesis research, in addition to selected graduate courses in the student's home department. The specialty courses will cover 1) the basic physics and chemistry of nanometer-scale structures, 2) the synthesis and characterization of such structures, and 3) present and future applications of nanoscale materials and devices. These courses will draw heavily from examples in the current literature. They will be integrated with the graduate curricula currently under development in the Georgia Tech Center for Nanoscience and Nanotechnology.

5 Organization and management

5.1 Interdisciplinary research team

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109–112

5.2 Team coordination

Area leaders are designated above. Interactions will be largely informal, since the collaborators are presently all within walking distance of one another. This will change when *Berger* returns to CNRS (Grenoble, France) at the end of 2002. Overseas contact will be mostly through email for information exchange, and express mail for sample exchange, with telephone (or netphone) calls when necessary. Additional funds will be sought to expand this partnership (see Sec. 5.3).

Monthly meetings of all Georgia Tech team members will be held to promote interactions and to give students an opportunity to present new research results. Such presentations are an important part of graduate (and undergraduate) education, yet often the number of opportunities is limited. We anticipate that each meeting would have one 30 minute talk by one of the students, with brief summaries of progress in each area from the others, and a discussion of proposed work for the next month. *Berger* will provide input before the meeting to other team members, and will be given a meeting summary afterwards. We will also attempt to use internet video collaboration methods (e.g. CUseeMe) to include *Berger* in the discussions more directly.

The five PIs will meet each semester (including summer) to discuss student support and large expenditures. Funds distribution will be approximately as indicated in the Budget Justification, but large purchases will be subject to approval of the Project Director (*de Heer*). In order to maintain some flexibility in the budget, yet avoid micromanagement, each PI will be allowed full control over a percentage (perhaps 70%; to be determined on a yearly basis by the Project Director and co-PIs) of their allocation shown in the Budget. Allocations in excess of this amount would require approval of the Project Director, with input from the co-PIs.

5.3 Additional collaborations

The present work forms the scientific basis for numerous potential applications and further fundamental studies. It is the start of an entirely new field. In order to facilitate expansion of this field and ultimately to create economic benefit, several additional collaborations will be forthcoming, as described below. The present partnership with CNRS will be continued and expanded, hopefully through supplemental funds from NSF that target international opportunities (as described in the program solicitation).

We anticipate expansion of the program in two directions: 1) towards fundamental properties of the 2D electron gas in graphitic nanostructures, and 2) towards large-scale integrated circuits composed of patterned graphite devices. Georgia Tech has local expertise in both directions, and joint projects will be sought after the initial results from the work proposed here. Please see letters in the Supporting Documents section of this proposal.

5.3.1 Fundamental properties

Prof. *Uzi Landman* has taken an active interest in the projects proposed here. He and his Center for Computational Materials Science are uniquely qualified to model many the properties that are the subject of investigation here. His broad experience in modeling transport in low dimensional systems (metal and semiconductor nanowires; semiconductor to metal junctions[128]) as well as correlation effects in low electronic density quantum dots,[129] will guarantee first-class theoretical support in the various scientific directions proposed here. It is particularly noteworthy that Landman's Center for Computational Materials Science is renowned for providing properties predictions of realistic systems.

5.3.2 Large-scale integration

The full economic value of this research will only be realized when these graphite structures are formed into practical integrated electronic devices. To accomplish this, the structures must be *a)* accurately modelled and optimized, *b)* integrated on the giga- to tera-scale, and *c)* usefully packaged.

Prof. *T. K. Gaylord* (ECE) has developed modelling and optimization techniques for 2D ballistic devices.[130–133] His expertise will be invaluable for implementing practical devices, especially multi-terminal diffractive devices. Prof. *James Meindl* (ECE, Director of Microelectronics Research Center) is known as a world-leader in microelectronics, with particular interests and expertise in giga-scale integration.[134–137] The resources of the NSF-sponsored *Packaging Research Center* at Georgia Tech will also be available for the last crucial step in creating a marketable integrated circuit.

5.4 Schedule

The schedule of the project is outlined below, subject to modification depending on the actual progress and findings.

Year1

- STM based nanolithography on HOPG, arc production of graphite ribbons; (WDH)

- UHV STM of graphitic nanostructures (steps and islands on HOPG, etch-pits, graphitic particles, arc produced graphite ribbons); graphite layers on SiC (PF)
- E-beam lithography of graphitic nanosystems; defined leads on arc produced graphite ribbons (AM)
- Epitaxial graphite films on metals; epitaxial graphite films on SiC (AE);
- TEM, SEM characterization of graphitic nanostructures produced by AE, WDH, PF; (ZLW)

Year 2

- STM based nanolithography on HOPG (continued), on epitaxial films on metals; and on epitaxial films on SiC ; arc production of graphite ribbons (continued); (WDH);
- UHV STM of lithographically patterned graphitic nanostructures; graphite layers on SiC (PF)
- Ultra low temperature transport on contacted graphite ribbons; patterned doping of SiC and other semiconductors to produce back gate structures; (AM)
- Epitaxial graphite films on semiconductors (AE); Metal assisted microwave CVD methods for film growth.
- TEM, SEM characterization of graphitic nanostructures produced by AE, WDH, PF; (ZLW)

Year 3

- STM lithography on back gate patterned graphite films; development of side-gate transistor (WDH);
- UHV STM,STS of lithographically patterned graphitic nanostructures; Effects of shape on DOS; effect of passivating atoms/molecules on DOS; (PF)
- Ultra low temperature transport on contacted back-gated and side-gated structures (AM)
- Epitaxial graphite films on semiconductors with patterned back gate doping (AE);
- TEM, SEM characterization of graphitic nanostructures produced by AE, WDH, PF; (ZLW)

Year 4

- Production of integrated nanographite device (at least two active elements, back-gated or side gated), using previously developed STM patterning methods (WDH)
- UHV STM, STS of prototype devices; High field effects; Quantum dot effects; Low temperature effects (PF)
- Ultra low temperature transport of patterned devices (AM)
- Improvement of epitaxial film quality and developments for mass production (AE);
- TEM, SEM characterization of graphitic nanostructures; (ZLW)

6 Conclusion

In conclusion, the projects outlined here will make important inroads into the area of nanographite science and engineering. The proposal is broad-scoped and involves overlapping areas of fundamental properties and device design.

The fundamental properties of nanoscopic graphite are investigated as a function of size, shape, temperature and fields. Nanotubes have demonstrated that quantum effects in nanographite systems are important, due to confinement and the low density of states at the Fermi energy. Electronic confinement in low dimensional systems (an important current field of research) gives rise the quantum Hall effect, ballistic transport, and correlated electronic effects (Luttinger liquids in ribbons, super-atoms in quantum dots). Electronic quantum properties are reflected in nanographite ribbons when kT is smaller than the bandgap (*cf.* nanotubes) which will manifest themselves, even for relatively wide ribbons (up to 50 nm) at room temperature. Initial nanographite electronic device structures are closely modeled after their nanotube counterparts to produce back- and side-gated grFETs where the bandgap is tailored with the width: $E_{gap} \sim 1/W$ [eV], W the ribbon width or nanotube diameter in nm. A major and crucial departure from nanotube electronics is that in the grFET semiconducting regions (i.e. narrow ribbons) are seamlessly joined to conducting regions (i.e. wide ribbons) by lithography methods. Hence, in contrast to nanotube and molecular electronics, non-graphitic metallic interconnects are not required. This clearly represents an overwhelmingly important advance over other proposed nanoelectronic architectures. In advanced devices the room temperature ballistic properties of nanographite ribbons will be exploited. Initial investigations will exploit a variety of methods to produce nanoscale graphite objects. Initial prototype devices will be constructed by STM lithography patterning of small graphite samples as demonstrated in this proposal. A critically important engineering challenge is to produce extended epitaxial graphite films on appropriate substrates. Important progress already made in this area (using single crystal SiC wafers) and indicates the path towards large-scale integration of patterned nanographite electronics.

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TITLE OF PROPOSED PROJECT **NIRT: Electronic devices from nano-patterned epitaxial graphite**

REQUESTED AMOUNT	PROPOSED DURATION (1-60 MONTHS)	REQUESTED STARTING DATE	SHOW RELATED PRELIMINARY PROPOSAL NO. IF APPLICABLE
$ **1,xxxxxx**	**48** months	**06/01/04**	

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Project Summary

Intellectual Merit. We propose to establish the potential of nano-patterned ultrathin epitaxial graphite (a.k.a. nano-patterned multilayered graphene, NG) on single crystal silicon carbide for nanometer scale electronic devices. The research is inspired by the demonstrated exceptional electronic properties of carbon nanotubes and the realization that the essential properties are shared by all nanographitic structures. Rationally patterned planar structures have obvious advantages over nanotubes. The research team has recently developed methods to produce nanopatterned ultrathin epitaxial graphite structures. The material can be gated. Patterned structures exhibit extraordinary two-dimensional electron-gas properties, previously seen only in semiconductor inversion layers, demonstrating its fundamental science potential. The interdisciplinary research team consists of seasoned experts in nanoscopic physics, surface physics and chemistry, transport, low temperature physics, and device engineering. The proposed research will create the foundation for graphene science and technology. It will 1) Produce extended defect free multilayered graphene, 0.3–3 nm thick, 2) Develop patterning methods, 3) Establish electronic and transport properties of extended films and defined structures, 4) Develop chemical modification (doping) methods, 5) Demonstrate simple devices, 6) Establish methods to integrate with Si based electronics. Intel Research has recognized the nanoelectronics potential and has provided significant seed funding.

Broader Impacts. The overall program ties research to education at all levels (K-12, undergraduate, graduate, continuing-ed), partly via participation in programs designed by education professionals. Through the Georgia Industrial Fellowships for Teachers (GIFT) program and similar programs under development, we will host high school teachers in a research laboratory so that they may rekindle their excitement for science and pass it to their students. Undergraduate students from Georgia Institute of Technology and the State University of West Georgia will participate directly in the research for periods of typically 1 yr/student (undergrads from anywhere in the U.S. can also participate through two REU summer programs). A planned course in "The Physics of Nanostructures" (part of a Nanoscience and Technology certificate program begun last year) will emphasize the latest breakthroughs in this field. Finally, a substantial focus on recruitment of underrepresented groups into nanoscience and engineering has been proposed, leveraging existing and pending Department of Education GAANN funds.

Research and education themes. The research proposed here falls most clearly under two of the main NSE research themes: *1) Nanoscale Structures, Novel Phenomena, and Quantum Control*, and *2) Nanoscale Devices and System Architecture*.

2 Introduction & background

Intellectual Merit. We propose to establish the potential of nano-patterned ultrathin epitaxial graphite (a.k.a. nano-patterned multilayered graphene, NG) on single crystal silicon carbide for nanometer scale electronic devices. The research is inspired by the demonstrated exceptional electronic properties of carbon nanotubes and the realization that the essential properties are shared by all nanographitic structures. Rationally patterned planar structures have obvious advantages over nanotubes. The research team has recently developed methods to produce nanopatterned ultrathin epitaxial graphite structures. The material can be gated. Patterned structures exhibit extraordinary two-dimensional electron-gas properties, previously seen only in semiconductor inversion layers, demonstrating its fundamental science potential. The interdisciplinary research team consists of seasoned experts in nanoscopic physics, surface physics and chemistry, transport, low temperature physics, and device engineering. The proposed research will create the foundation for graphene science and technology. It will 1) Produce extended defect free multilayered graphene, 0.3–3 nm thick, 2) Develop patterning methods, 3) Establish electronic and transport properties of extended films and defined structures, 4) Develop chemical modification (doping) methods, 5) Demonstrate simple devices, 6) Establish methods to integrate with Si based electronics. Intel Research has recognized the nanoelectronics potential and has provided significant seed funding.

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Simple nanographitic systems have attracted worldwide attention during the past decade.[29] Many consider nanotubes as the prototypical nanostructure because of their exceptional properties. Indeed some even prophesized that nanotubes alone will fundamentally impact technologies as diverse as electronics, materials, and energy storage. While these predictions are far from met,[30] the thesis that graphitic structures at any length scale are fundamentally important both for basic science as well as for industry needs no further amplification. The electronic properties of nanotubes in particular have been the focus of many investigators, in particular considering that the anticipated need for an alternative to the silicon MOSFET technology in a decade or so. In this proposal we suggest that patterned ultrathin graphite grown on silicon carbide may be a candidate. The research proposed here is actually only a small step in this direction. The work will be considered to be successful if we succeed in demonstrating the fundamental properties of the material as well as a simple prototype device structures. As we show, the patterned graphite structures that we already have built demonstrate remarkable (and possibly size dependent) two dimensional electron gas properties. We also show that the material can be gated.

It is well known that the basic electronic properties of the nanographites (i.e. nanoscopic single layered graphitic systems for which every atom is three-fold coordinated) can be understood in terms of the graphitic π bonds. In fact early calculations of C60,[31] nanotubes[32] and nanoribbons[33,34] were rather simple tight-binding calculations using bulk graphite tight-binding parameters. They nevertheless correctly predicted the properties of these systems near the Fermi level. Several features are common to all nanographitic systems (i.e. two dimensional graphitic systems for which every atom is three-fold coordinated). (1) They all exhibit low or vanishing densities of states at the Fermi-level, so that they are either metal-like or intrinsic semi-conductors. (2) The band-gap (or pseudo-bandgap) varies approximately as the inverse of the size L (i.e. nanotube diameter,[35] fullerene radius or ribbon width[36]). This gap is in the range of 1–5 eV/L, where L is in nm. This important feature of nanographites allows the electronic properties to be designed into the structures. For example, calculations show that a simple junction consisting of a narrow graphene (i.e a single graphite layer) ribbon connected to a wider ribbon, is electronically active.[37]

To optimally exploit this property requires that the nanographite structures are rationally designed and interconnected. Indeed there are numerous efforts along these lines, in particular to place and interconnect carbon nanotubes in order to produce functional electronic devices. These efforts have already produce remarkable results: several groups have successfully produced individual transistors[38,39] and even several interconnected carbon nanotube structures.[40,41] At the same time, it is clear that these efforts are still far from competing with current silicon nanoelectronics (the current standard feature size is 80 nm), where tens of millions of interconnected transistors are reliably patterned.

We argue that the nanotube approach to nanoelectronics is actually severely restricted. Not only because it is still impossible to chemically synthesize and to reliably position carbon nanotubes, but more because of their cumbersome geometry. Their cylindrical shape makes it impossible to seamlessly interconnect them, which in turn dictates that they must be interconnected using lithographically patterned metal wires.[42,43] These metal to nanotube contacts pose impedance problems due to their nanoscopic size, which for quantum mechanical reasons causes each connection to represent a contact resistance of at least 6.5 kΩ.[44–47] Some of these problems may be resolved in the future, however we believe that this proposal represents a rational alternative approach, with a clearly defined roadmap towards nanographitic electronics.

Our approach is strategically more conventional. We recognize the potential of nanographitic objects for nanoelectronics but we also assume that a traditional top-down approach to nanoelectronics may be more feasible. The approach is closely related to current silicon based nanoelectronics so that the roadmap towards large-scale integration is essentially built-in. The focus of this proposal is not so much in down-scaling as it is in demonstrating the potential of nanographites. The reciprocal relation between the band-gap and feature size for nanographites in general[35,36] indicates that larger objects at low temperature will function like smaller ones at higher temperatures.

The guiding principle is that nanotubes are by no means exceptional but merely examples of nanographite. Theory predicts that planar nanographitic ribbons (nanoribbons[33,34,37,48–53]) have properties that are similar to those of nanotubes. For example, like nanotubes, ribbons can be metallic or semiconductors.[33] Metallic ribbons transport trough two conducting subbands that intercept the Fermi level. Both have size dependent band gaps of similar magnitude, the properties of both depend on the geometry. Due to these similarities, we suspect that the patterned nanographites also will have nanotube-like transport properties, which include coherent transport,[54] ballistic transport[7,45] and high current capabilities.[4,7] However, in essential contrast to nanotubes, we can form and interconnect the structures at will. The interconnections involve junctions which have been shown to be electronically active. Furthermore, like nanotubes, patterned nanographite can be doped and gated. The preliminary results obtained by our research team amply demonstrate that we are on the right track.

As is shown in more detail below, our team that worked enthusiastically (without funding) for the past two years has succeeded in

- producing extremely thin epitaxially grown crystalline graphite layers, with excellent control of the crystal orientation on silicon carbide crystals.
- We have demonstrated that epitaxial graphite can be rationally patterned using standard nanolithography methods.
- Preliminary results suggest that the structures can be gated.
- We have demonstrated that at low temperatures the ultrathin graphite layers exhibit a variety of two dimensional electron gas (2DEG) properties.

It is rapidly becoming clear to us that the work outlined in this proposal will profoundly impact our understanding of nanographites in general, as well as provide critical insight in how to proceed to optimally exploit the electronic properties of nanographites. We presented earlier preliminary results to Intel Research, who were impressed enough to provide substantial seed funding for this project, which incidentally further attests to its technological significance. To the best of our knowledge our group is the only one currently pursuing this research.

2.1 Methods and preliminary results

The approach to nanographitic electronics proposed here is based on methods (developed by the GT research team) to pattern ultrathin graphite layers that are grown epitaxially on single crystal SiC. As demonstrated theoretically, these planar interconnected nanographitic structures have electronic properties that are closely related to those of nanotubes. However in contrast to nanotubes, patterned nanographitic structures can be

- constructed using lithographic methods.
- interconnected with graphite rather than with metals, thereby eliminating problematic metal to nanotube contacts.

Consequently, this proposal resolves the most serious problems of nanotube-based electronics. Patterned nanographite electronics

- utilizes the advantageous properties of nanographites;
- uses established Si patterning methods;
- creates a platform for ballistic and phase-coherent electronics.

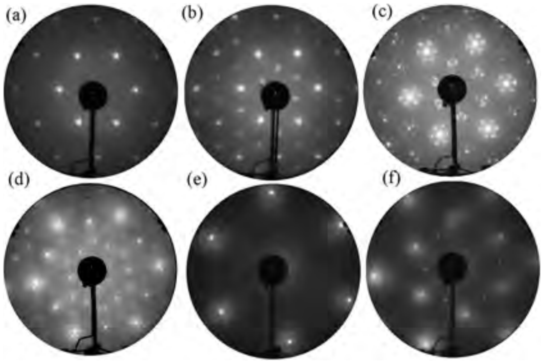

FIG 1: Evolution of LEED patterns on UHV-heated SiC(0001). (a) SiC 1×1, E=177eV. (b) SiC $\sqrt{3}\times\sqrt{3}R30°$, E=172eV. (c) Graphene on SiC (0001), $6\sqrt{3}\times6\sqrt{3}R30°$, E =109eV. (d) Graphene on SiC (0001), $6\sqrt{3}\times6\sqrt{3}R30°$, E=289eV. (e) Multilayer graphene on SiC(0001), only graphite spots with their satellites are observable, E=78eV. (f) Multilayer graphene on SiC(0001), the SiC spots are still visible at this incident electron energy, E=180eV.

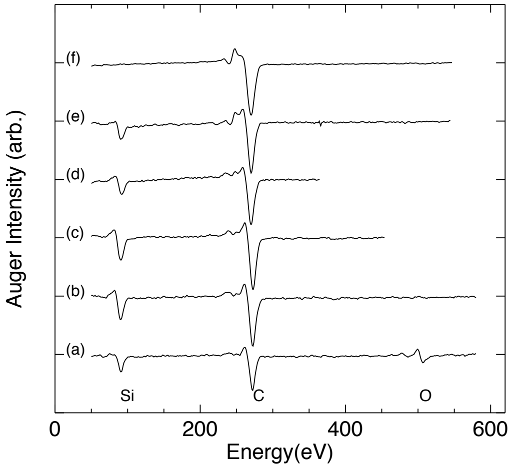

FIG 2: Auger spectra for successively higher flash-anneal temperatures of SiC(0001). (a) 950°C, (b) 1250°C, (c) 1350°C, (d) 1450°C (e) 1500°C (f) > 1500°C. The data show that oxygen can be controllably removed, followed by Si. Note the evolution of fine structure in the carbon peak as the Si/C ratio decreases (c–f).

2.1.1 Ultra-thin epitaxial graphite formation

At high temperatures, graphite grows on the (0001) face of synthetic 6H SiC crystals.[55–57] Essentially atomically flat SiC crystals are heated to very high temperatures (1400C) in ultra-high vacuum ($<10^{-10}$ Torr). In this process, silicon evaporates from the crystal and an epitaxial graphite layer is formed.[55–57] This process is well known and amply documented. The graphite grown by this method is known to be of exceptional quality, which surpasses that of natural or synthetic graphite.[58] An essential feature of these epitaxial layers is that they only weakly interact with the SiC substrate.[55,56]

In our efforts to reliably produce graphite layers, we have experimentally investigated graphite growth processes in some detail in order to optimize the growth conditions. After the UHV heat treatment the samples are probed by low energy electron diffraction (LEED) and Auger electron spectroscopy (AES). The former gives accurate information on the crystal structure of the graphite in various stages of the growth. As shown in Fig. 1, with increasing heat treatment time, the graphite diffraction spots become more intense while the SiC diffraction spots diminish. Note also the weaker diffraction spots due to the $6\sqrt{3}\times6\sqrt{3}$ reconstruction of graphite on SiC. The Moiré pattern between the graphite and SiC lattices gives a quasi-6×6 pattern that is observed in both LEED and STM experiments[59] (see also Figs. 1 and 5). These subside as the graphite layer becomes thicker. The AES results verify the formation of graphite on the SiC as evidenced by the decrease of the silicon intensity in the spectra shown in Fig. 2. We are currently calibrating these probes to provide accurate information on the thickness of the graphite layer. At present, graphite films with less than 5 graphene layers can be grown. Further study is required to fine-tune the procedures.

2.1.2 Patterning

The key to the success of this project is that the graphite layer is rationally patterned. The approach that we developed (patent pending) is to first pattern the silicon carbide crystal which is subsequently etched. The etched pattern is then graphitized.

The steps follow standard nanolithography procedure:[60] (1) A SiC wafer is diced to 5x6 mm blanks. (2) PMMA is spun onto the blank. (3) The blank is patterned at the GaTech / School of Physics e-beam facility, (4) developed, and (5) coated with a thin film of aluminum, (6) followed by chemical lift-off. (7) The exposed SiC is then plasma etched to a depth of about100 nm. (8) The aluminum is then removed. The final result is that the pattern is etched onto the SiC: the pattern appears as a raised mesa structure 100 nm above the etched base. Examples are shown in Fig. 3.

The graphitization step proceeds as described above (Sec. 2.1.1). An essential feature is that the walls of the mesas are not (or at best poorly) graphitized in the heat treatment, as evidenced by the high measured resistance between the mesas and the base. A lower temperature oxygen etch to remove poorly graphitized areas and to better define the graphene edges is anticipated. Similar procedures are also used to purify and open carbon nanotubes.[61] A low background of hydrogen insures that the graphene edges are hydrogen passivated. Other passivat-

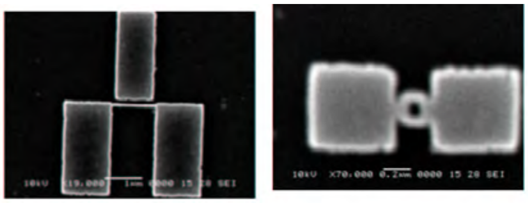

FIG 3: Recent examples of e-beam lithography of SiC. The height of the structures is ~ 100 nm above the etched base plane. Scale bars are 1 μm (left) and 0.2 μm (right).

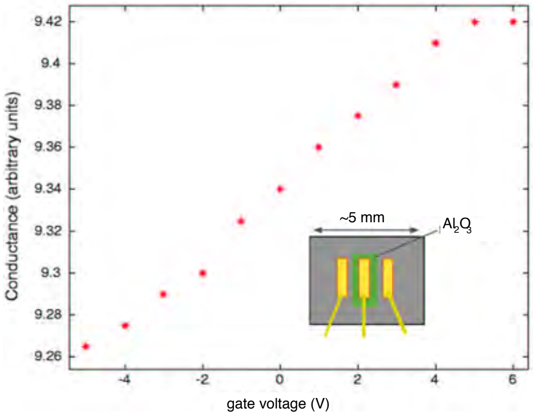

FIG 4: Field-effect gating of current flow. The change in resistance is 2%, even though the imperfect geometry drastically short-circuits the gate region. Required gate voltages are large because the gate insulator was very thick (100 nm).

ing species are anticipated in order to dope the graphene, as described in 3.2.4.

Oxide gate structures have been patterned on the samples using conventional methods: an oxide is e-beam evaporated on the graphite layer and a metal electrode is applied on top of that. Preliminary results indicate that the ultrathin graphite layers can be gated (in contrast to bulk graphite[62]), as shown in Fig. 4.

Currently, wiring is applied to the graphitized patterns using gold wires and silver paint in the usual way. A preliminary study indicates that palladium can be evaporated on the graphite to provide good contacts (see e.g. Ref. 43). This will further allow metallic interconnects and contacts to be patterned on the nanographitic structures.

2.1.3 Characterization

Besides LEED and AES, the patterns are currently characterized using ambient AFM, UHV STM and STS (scanning tunneling spectroscopy), and SEM (scanning electron microscopy). Examples of the various microscopies and spectroscopies are shown in Fig. 5. The STM clearly shows the $6\sqrt{3} \times 6\sqrt{3}$ reconstruction of the graphite layer.[56] Also interesting is the STS of the epitaxial graphite layer which appears to be continuous over an atomic step on the SiC surface. This indicates that the graphite drapes over such defects.

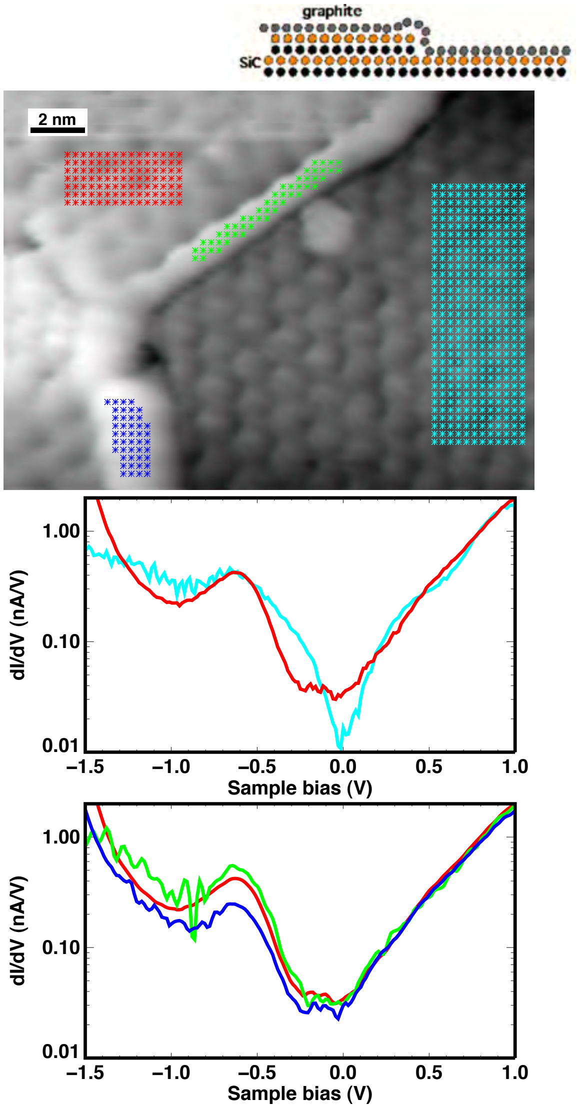

FIG 5: Top view STM image and spectra of features on graphitized-SiC. Step in the graphite layer is due to a step in the SiC, as shown in the cartoon cross-section (top). Periodic surface corrugation is due to "beating" between the graphite and SiC lattice periodicities (6x6 Moiré pattern). STS spectra show density-of-states within the SiC bandgap, consistent with graphite. STS on the step (green and blue) is very similar to the red region, implying that there is no break in the graphite film (see cartoon). Differences between cyan and red regions suggest differences in SiC/graphite alignment, or the effect of electron confinement.

Currently, electronic characterization is performed using standard low-temperature measurement methods. We have measured the properties of the structures from $T = 60$ K to 4 K, in magnetic fields up to $B = 8$ T at the CNRS-

Grenoble facility. These limits will soon be extended using a dilution refrigerator to achieve temperatures in the mK range. Higher fields measurements (up to 18 T) will be made at the NIST facility in Boulder.

2.1.4 Preliminary transport measurements on a nanopatterned graphite sample: evidence for 2D quantum properties

The fascinating transport properties of patterned epitaxial graphite layers are beautifully demonstrated in the preliminary magnetoresistance measurements made on sample #29, which consists of two patterned pads ($\sim 3 \times 1$ mm), that are connected by a 3×8 μm strip (see inset, Fig. 6a). Four contacts were applied to each pad and one to the ground plane. Four point magnetotransport measurements were made of the two pads and the strip.

Figure 6a shows the resistance as a function of temperature ($B = 0$ and 4 K<T<60 K), which increases with decreasing temperature for both pads and the strip. The resistance ratios $R(4\text{K})/R(60\text{K})$ are 3.2 for Pad 1, 4.8 for Pad 2 and 16.4 for the 3 μm strip. Resistance increases of about a factor of 2 are found for multiwalled carbon nanotubes.[46] Much smaller increases ($\sim 20\%$ in this temperature range) are observed in exfoliated graphite samples,[63] intercalated graphite[64,65] and other partially graphitic carbons[66,67] and are related to the quasi-2D nature of these systems which have an increased interlayer spacing compared with crystalline graphite (for 3D crystalline graphite the in-plane resistance decreases with decreasing temperature).

The resistance increase in quasi 2D graphitic systems and nanotubes[68] has been attributed to weak localization (for reviews, see[69–73]), which may be concluded from the observed $\log T$ dependence of the conductance: $G(T) = G_1 + G_2 \log(1 + T/T_c)$,[68] although other explanations have also been given.[46] A $\log T$ dependence may also be deduced for our samples (Fig. 6b). On the other hand, the large resistance increase suggests strong localization, which should follow Mott's law:[74] $R \sim \exp(T_0/T)^{1/3}$ for non-interacting 2DEGs as expected for an Anderson insulator; this law is approximately followed (Fig. 6c).

Magnetoconductance measurements (Fig. 7) show several striking features. The 2D nature of the sample is unambiguously demonstrated in the huge magnetoconductance anisotropy. For magnetic fields parallel to the graphite plane, the conductance ratio $G(B_{\|} = 8T)/G(B = 0) < 0.01$ for all three configurations. For magnetic fields perpendicular to the graphite plane, the conductance ratio $G(B_{\perp} = 8T)/G(B = 0)$ at $T = 5$ K is 2.4 for Pad 1, 6.3 for Pad 2 and 27 for the 3 μm strip. A positive magnetoconductance is often taken as evidence for weak localization in exfoliated graphite samples,[63] intercalated graphite[64,65] pre-graphitic carbons[66,67] and carbon nanotubes.[68] It is not observed in 3D crystalline graphite. However the unusually large values found here are exceptional. Furthermore, the relative insensitivity to temperature is also not

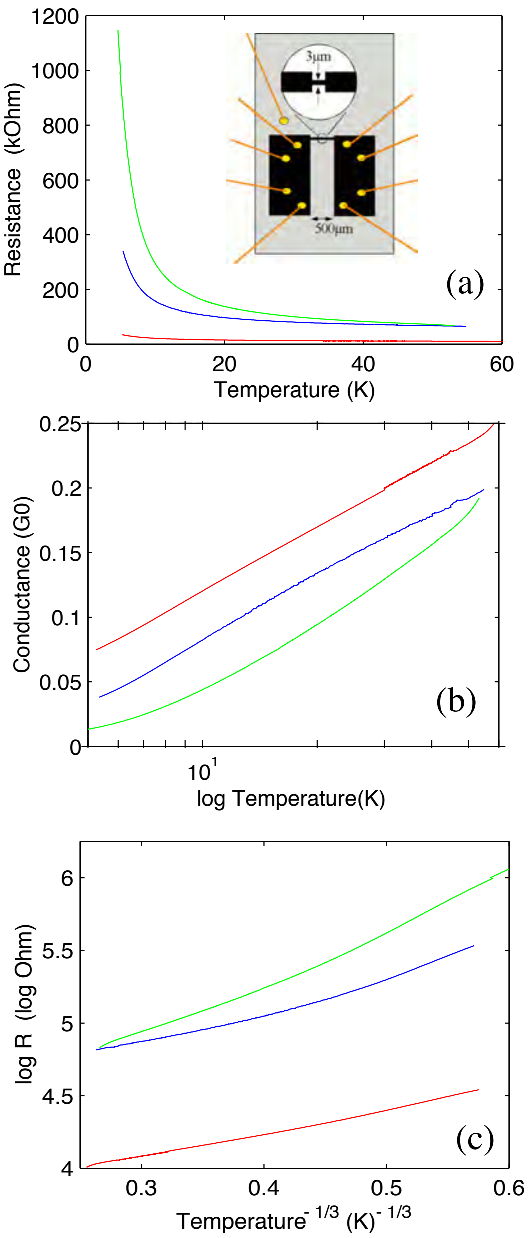

FIG 6: Temperature dependence of the resistance for the sample #29. a) four point resistances of Pad 1(red), Pad 2 (blue), and the 3 μm strip (green) (inset) schematic of the sample, showing the connections to Pad 1 (left four contacts) and Pad 2 (right four contacts).(b) Conductance versus log T should be a straight line for 2D weak localization. (c) Log R versus $T^{-1/3}$ should yield a straight line for a 2D Mott insulator.

expected for weak localization (see e.g. Refs. 46 and 68).*

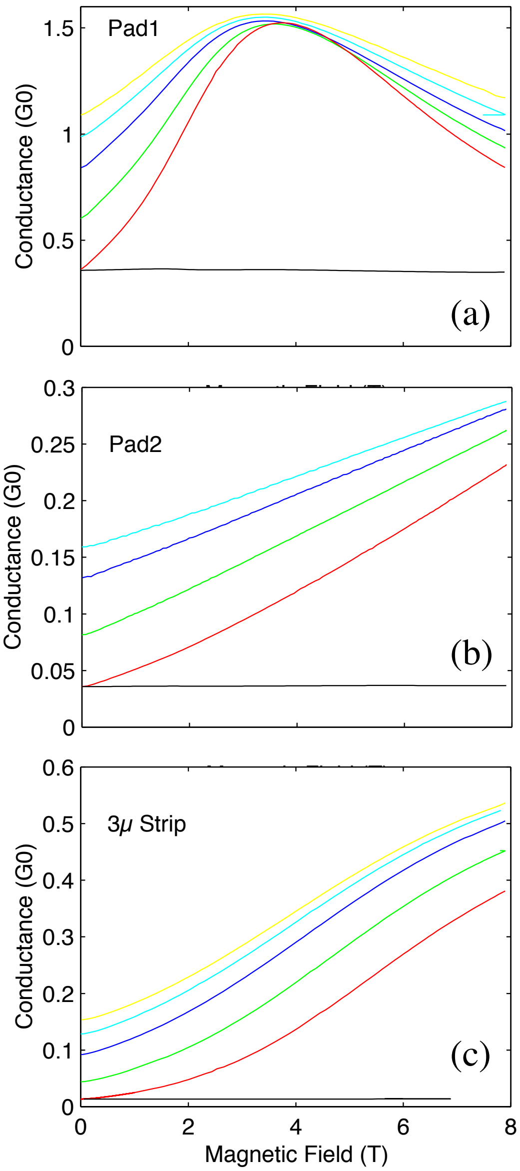

FIG 7: Four point magnetoconductance measurements of sample #29 in a perpendicular magnetic field from 0–8 T at temperatures T=40 K (yellow), 30 K (magenta) 20 K (blue) and 10 K (green) and 5 K (red), and in parallel magnetic field at 5 K (black). In all cases the perpendicular magnetoconductance is large and the parallel magnetoconductance is very small (ratio < 1%), indicative of a 2D system where the magnetotransport is caused by orbital (not spin) effects (a) The conductance of Pad 1 shows a striking field dependence which increases at low fields and decreases at high field, attaining a maximum at B=3.8 T which is practically temperature independent and within one percent of $3e^2/h(= 1.5G_0)$. (b) The magnetoconductance of Pad 2 can be scaled to overlap with that of Pad 1. (c) The magnetoconductance ratio is largest for the strip and it appears to approach saturation, reminiscent of Pad 1.

The magnetoconductance properties of Pad 1 are intriguing. The conductance first increases with increasing field and saturates at $G = 1.5G_0$ for $B \sim 3.5$ T after which it decreases again ($G_0^{-1} = h/2e^2 = 12.9k\Omega$). It appears that the saturation conductance and field are independent of temperature (from 4 K to 40 K).

The observed properties of Pad 1 are reminiscent of a magnetic-field-induced delocalization in strongly localized 2DEGs,[75,76] when the sample size is greater than the localization length. Jiang et al[77] have observed an insulator-to-metal transition in a modulation doped GaAs/AlGaAs heterostructures. At $T = 0.5$ K for this 2DEG, $R = 50$ kΩ at $B = 0$. R reduces to 10 kΩ at $B = 3.4$ T after which it increases to 500 kΩ at $B = 5.5$ T. The dip is more pronounced at lower temperatures. However at $B = 2.8$ T, the resistance $R \sim 40$ kΩ is independent of the temperature (80 mK<T< 550 mK). This unusual behavior is attributed to a field induced transition from an Anderson insulator to a quantum Hall conductor : away from the $\nu = 2$ Landau level filling at $B = 3.4$ T, the system is insulating. Physically the extended states, which exist at the center of each Landau level in high magnetic fields float up in energy as B goes to 0. This causes their energy to diverge and the system becomes insulating in low fields. This picture has been experimentally verified by Glozman et al.[78] We have not yet made Hall measurements on our samples: a quantum Hall plateau at the critical field will verify the nature of the insulator to metal transition in our samples.[77]

The properties of Pad 1, Pad 2 and the 3 μm strip are clearly related. The fact that they are not identical needs to be examined further. This may well be related to the fact that this system is close to a metal-insulator transition,[71] which probably makes it quite sensitive to small variations. In particular it may be that the mechanical stress caused by the contacts or perhaps inadvertent doping caused a change in the carrier density, which may well account for the differences.[71]

The very large magnetoresistance ratio observed for the strip may be a size effect. Since the graphite of this sample has about 5 layers (as concluded from the AES and the LEED pattern) it may be similar to graphene. A graphene strip of 3 μm width is expected to have either a band-gap (or pseudo-gap) of about 2 meV (i.e. 20 K) (see i.e. Ref. 36), (in contrast to the much larger pads for which the gap due to confinement is negligible). In

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[*] The 6H-SiC crystals used in our studies are n-doped, and hence they conduct at room temperature. However below $T = 90$ K the carriers are frozen out and the material becomes an insulator, as we have determined experimentally for the graphitized material. We were concerned that perhaps the graphitization caused an inversion layer at the interface, however the magnetoconductance measurements below clearly demonstrate that the properties are closely related to graphite and not to doped SiC. The very large magnetoresistive anisotropy also indicates that the effect is purely orbital, in contrast to the much smaller anisotropy observed in semiconductor 2DEGs.[71]

either case at low temperatures the resistance increase of the strip should be greater than for the pads due to this difference in the electronic structure. In other words, the difference may in fact reflect a quantum confinement effect. In order for the transport to be sensitive to the boundary implies that the phase coherence length is at least of the order of the ribbon width (i.e. 3 μm).

Whatever the ultimate explanation may be, it is already clear that these patterned ultrathin epitaxial graphite structures provide a wealth of new physics. They may well provide a new platform for 2DEGs.

3 Proposed research

Our preliminary results have established important facts about the NG system, and they have raised many fascinating scientific questions. The research plan proposed here aims to attain definitive answers to these questions through the development of high-quality materials and careful experiments, even down to millikelvin temperatures. This is entirely compatible with the further goals of developing functional room-temperature electronic devices from NG, and a detailed examination of their potential for large-scale integration. We will consider this project a success if we can accomplish the following goals:

1. Produce and characterize nanopatterned epitaxial graphite films on single-crystal SiC substrates.
2. Elucidate the quantum electronic properties of epitaxial graphite films and nanopatterned epitaxial graphite structures in different temperature regimes from 10mK–300K.
3. Demonstrate nanopatterned epitaxial graphite devices and interconnected NG devices.

These basic steps will be essential for determining the potential of this materials system for nanoscale electronics. In parallel, utilizing input from these results, we will:

- Initiate research to bridge the gap between Si and NG. This involves the development of low-temperature methods for graphite and SiC growth and incorporation on Si substrates.
- Research potential architectures for device integration and investigate intrinsic limits to integration density and power consumption.

3.1 Interdisciplinary Research Team

To achieve the stated goals we have assembled an interdisciplinary research team with a broad range of expertise.

Principal Investigators

Walt de Heer, GT Physics. Project Director. Nanolithography, transport, and magnetotransport measurements, metal/graphite and graphite/graphite contact studies.

Phillip First, GT Physics. Thin-film growth, characterization of graphene ribbons and ribbon edges, metal/graphite and graphite/graphite contact studies. Electronic structure of graphite/SiC interface.

James Meindl, GT Electrical and Computer Engineering and Microelectronics Research Center (Director). Nanolithography, device development, comparison with existing technologies, architecture development for graphene ballistic/coherent devices, fundamental limits to integration density.

Thomas Orlando, GT Chemistry. Characterization and control of ribbon edges, low-temperature CVD growth techniques for graphene and SiC, SiC growth on silicon.

Senior Participants

Mike Abrecht, NIST-Boulder. Metal/graphite contact resistances and magnetotransport measurements (postdoc with *Ekin*).

Claire Berger, CNRS, Grenoble, France (presently visiting scientist at GT). Nanolithography, transport, magnetotransport. CNRS has state-of-the-art equipment for all such measurements (see Facilities). Several of the results shown in Sec. 2.1 were obtained at CNRS Grenoble, France.

Mei-Yin Chou, GT Physics. First-principles calculations of graphite ribbon/edge electronic structure, including the effect of edge-bonded molecules.

Edward Conrad, GT Physics. X-ray and high-resolution electron diffraction studies to determine film thickness, defect structure, and stacking sequences.

Jack Ekin, NIST-Boulder. Metal/graphite contact resistances and magnetotransport measurements. Magnetoresistance and Hall effect measurements will be done from 1.5K–300K in fields up to 16 T.

Txxxxxxxxxxxxx Two-dimensional electron-wave device modeling applied to graphene devices. Electronic structure of graphene/SiC interfaces via ballistic electron emission spectroscopy (BEES).

Uxxxxxxxxxxxxxxxxxxxxxxxxxxxx Calculations of transport and coherence properties based on first-principles theory.

Axxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx. Characterization of graphite films and graphene edge chemistry via XPS, STM, TPD and other surface chemistry techniques.

Axxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx Millikelvin temperature measurements of transport and magnetotransport.

Pxxxxxxxxxxxxxxxxxxxxxxxxx. Production of atomically-flat SiC substrates.

3.2 Research thrusts

3.2.1 Graphene preparation and characterization

(*Berger, Conrad, de Heer, First, Gaylord, Leavitt, Neudeck, Orlando*)

Since the true scientific and technological potential of this system may not be known until very high quality material can be created, a great deal of effort will be devoted to this goal. Three primary tasks will be faced in this research thrust: Growth of high-quality SiC substrates, graphitization down to single graphene sheets, and electronic/chemical characterization of defects and graphene step-edges.

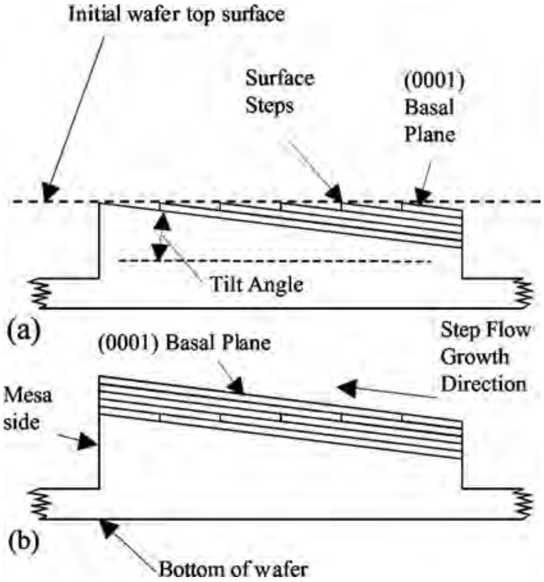

FIG 8: Diagram illustrating the growth of step-free mesas.[79] (a) Before growth, initial mesa surface parallel to bottom of wafer surface contains steps due to tilt of basal plane with respect to polished wafer surface. (b) After growth, steps have been grown out of existence, leaving a step-free mesa surface parallel to the basal plane i.e., tilted with respect to the initial surface.

SiC substrates. Preparation of highly-perfect graphene layers will depend on the quality of the SiC substrate. Until recently, this has been problematic due to the high density of defects (screw dislocations and micropipes) that result from the bulk growth process. With high temperature treatments and overgrowth, these defects can nucleate microfacets that grow to fill even more of the surface. *Neudeck* and collaborators at NASA Glenn[79–81] have recently developed a CVD technique to grow atomically-flat SiC mesas up to 400 μm x 400 μm. As shown schematically in Fig. 8, the SiC substrate is optically-patterned into raised mesas, followed by high-temperature (1600–1700 C) CVD growth using silane and propane precursors. The defect density on the surface is low enough that more than 50% of mesas contain no extended defects. Under CVD step-flow growth, all of the steps flow off the edge of the mesa, leaving an atomically flat surface.

We expect that the mesa CVD substrates ultimately will be the path to large-scale patterns and high-mobility material (the very highest quality graphene ribbons would likely utilize a thin CVD overgrowth *after* lithographic patterning). Still, much of our initial work will involve conventional samples in order to perfect techniques. *First* is presently making small modifications to the room-temperature UHV STM to enable precise location of mesas down to 50 μm x 50 μm for studies of graphene growth via UHV heat treatment (smaller mesas have lower probability of a single defect). The STM and LEED results presented in Sec. 2.1 were obtained on a NASA sample. However, in this initial work, it was necessary to grow a thick oxide to rid the surface of excess carbon that resulted from the use of a graphite susceptor in the CVD reactor. The oxidation step appears to have created many steps on the surface. Consequently, we don't yet know the effect of UHV heat treatment on the step structure of atomically-flat mesas.

Conrad has begun high-resolution LEED characterization (see Facilities) of the NASA samples. Fig. 9 shows an optical micrograph of one of the samples, with an arrow marking a microfacet which nucleated during CVD growth. The specular LEED profile in the inset was acquired from mesa "A," located by operating in a "scanning LEED microscope" mode recently implemented. This sample was prepared with a thinner oxide, and the diffraction line width of 0.004 Å^{-1} is instrument limited, showing the extremely high crystalline quality.

For conventional SiC substrates, high temperature H_2, H_2+HCl, or H_2+C_3H_8 etches[57,82,83] have been shown to produce atomically-flat terraces separated by unit-cell or half-unit-cell steps. *De Heer* and *Berger* are designing a

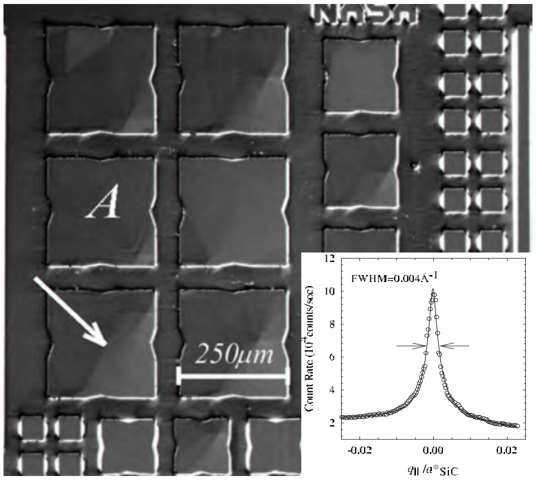

FIG 9: Optical image of a 1 mm x 1 mm 6H-SiC(0001) mesa sample. Mesa sizes range from 50μm to 250μm. **Arrow:** a facet nucleated during CVD growth. **Insert:** HRLEED specular diffraction profile from mesa “A.” Solid line is a Lorentzian fit plus background. The FWHM of the peak is instrument limited.

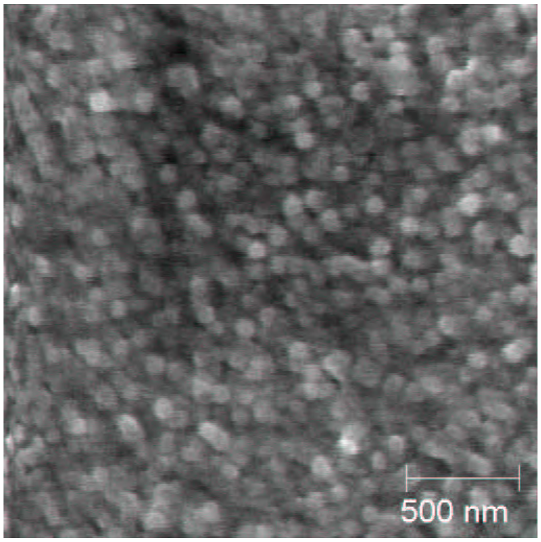

FIG 10: SEM image of a SiC nanocrystalline film grown using 5–11 eV electron-beam irradiation and acetylene dosing at 10^{-5} Torr for 30 min (base pressure < 10^{-10} Torr). Substrate temperature was 650 C. Crystallites with < 50 nm diameter can be seen. These images clearly demonstrate our ability to fabricate SiC films and nanocrystallites via the EB-CVD method.

high-temperature, high-vacuum, induction furnace to allow various processes (planarizing, oxidation, graphitization and passivation) to be performed, by careful control of temperature and introduction of reagent gasses in the furnace. The Microelectronics Research Center at Georgia Tech has also committed $50k toward a commercial rapid thermal processing unit that would allow these procedures to be done for whole SiC wafers.

With an eye on future integration with Si technology, alternative low temperature production methods of SiC on Si will be developed. *Orlando* has been investigating electron beam-stimulated CVD (EB-CVD) growth of SiC on Si. These experiments are at an early stage. Figure 10 shows a film of silicon carbide nanocrystallites grown recently on *n*-Si(111) with an acetylene background pressure of 10^{-5} Torr for 30 minutes under UHV. During growth, 5–11eV electrons irradiated the substrate stimulating film growth via low energy electron scattering processes such as dissociative electron attachments and the negative ion resonances of acetylene and silicon carbide. The substrate temperature of 650 C was much lower than typically reported for good film growth.[84] By using diffraction electron stimulated desorption (DESD),[85,86] we ultimately intend to impose a nanoscale pattern of SiC growth on the surface. In this method a surface electron standing wave is created by the incident and diffracted electron waves. Electron stimulated growth occurs preferentially at the antinodes of the standing-wave pattern. We aim to create short defect-free pillars of SiC on the Si surface which could serve as a strain-accommodating layer between Si and a CVD-grown SiC film. *Neudeck* and collaborators have achieved substantial overgrowth beyond the sides of mesas.[81] With properly chosen pillar spacing (adjustable via e-beam energy & angle) a similar technique (done as incoherent EB-CVD to keep the temperature below the melting point of Si) could result in a strain-free single-crystal SiC film on top of the pillars.

Graphene growth/characterization. Graphene surfaces prepared *in situ* in UHV will be examined via numerous surface science techniques found in the labs of the participants (see Facilities). Additional information about the subsurface structure and graphene multilayer thickness will be obtained at the Surface X-ray Scattering Facility of the Advanced Photon Source (*Conrad*).

First will continue studies of graphene formation using Auger spectroscopy, LEED, STM, and STS. Better control of growth conditions is required and detailed correlation with *post facto* Auger and LEED measurements. Studies will be carried out predominantly at room temperature. A Si deposition source will be installed to better control the initial surface reconstruction.[87,88] Film thicknesses and underlying morphology will be probed using the technique of “quantum-size microscopy” with the STM.[89,90] Complementary information on the graphene/SiC interface electronic structure will be obtained by *Gaylord* and *First* via ballistic electron emission microscopy/spectroscopy (BEEM/BEES)[17,18,91,92] down to 4 K[16,93] (see also Sec. 3.2.4).

A principle issue in any future studies of the electrical properties of 2D graphite sheets is a precise measurement of the film thickness. We would ideally like to have atomic layer-by-layer control on the graphite growth. Growth rates as a function of sample temperature are not known well. Previous ellipsometric measurements[94] have shown that heating SiC at 1300 C for 1 hour produces a 100 Å film on the Si-terminated (0001) face versus a 1000 Å layer on the C-terminated ($000\bar{1}$) face. Further heating does not increase the thickness much on the (0001) face, which suggests that Si diffusion through the graphite is the rate-limiting step. Thickness measurements using Auger electron spectroscoy (AES) have been attempted by measuring the relative strength of the Si and C Auger peaks.[95] Especially for small number of layers, interpretation of the Si/C ratio is complicated by the large carbon signal from the substrate.

STM is useful in looking at the top layer of graphite, but subsurface structure will always be subject to interpretation of electronic spectroscopies, such as those mentioned above. Surface X-ray diffraction (*Conrad*) is a direct structural probe capable of determining order in deeper layers. Furthermore, the measurements can be done *during* the growth process, since, in contrast to electron diffraction, X-rays are unaffected by sources of thermionic emission such as e-beam heaters. We will correlate the X-ray-determined film thickness and growth conditions with secondary probes of thickness and order: the Si/C Auger intensity ratio and graphite/SiC LEED intensities and reconstructions. This will make the growth methods transferrable to other participants. Detailed studies of the graphite/SiC reconstructions[59,96] will also be done using surface X-ray scattering, in order to answer some outstanding questions concerning the role of multiple scattering in the LEED patterns.[97]

Graphene edges. An important difference between nanotubes and graphene ribbons is that graphene ribbons have edges. Typically the edges are chemically passivated (by hydrogen for example). Calculations indicate that chemical properties of the passivating groups do not distract from the general electronic structure discussed previously.[33,98] Passivating atoms or groups may localize carriers or otherwise affect the density-of-states, however bandgap size will generally not be changed. Thus, while the chemistry of ribbon edges must be understood in detail to refine the proposed devices, we don't expect that the operation of devices based on semiconducting ribbons would be changed fundamentally by imperfect edges. Our recent magnetoresistance measurements (Sec. 2.1) strongly support this conclusion. Furthermore, appropriate *control* of the chemistry at ribbon edges could allow tuning of the electronic properties of the ribbon.

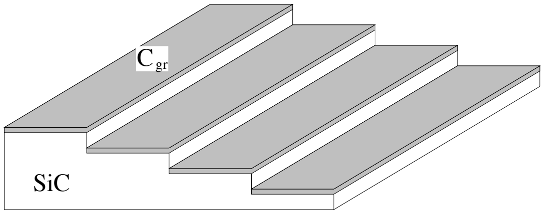

FIG 11: Schematic of vicinal SiC with graphene layers. These form 1) an array of well-oriented steps for surface chemistry studies of edge passivation and modification, and 2) ideal graphene ribbons. This geometry (occurring naturally on a vicinal-cut surface) will be used to obtain the best possible ribbons for electronic structure studies before lithographic techniques are fully refined. Note that ribbon edges might be "trimmed" by heating in oxygen.

In order to effectively study oriented graphene edges, vicinal SiC surfaces will be used (as also in studies of the electronic structure of "perfect" graphene ribbons; see Secs. 3.2.3 and 3.2.4). These are available from Cree Research with standard miscut angles of 3.5° and 8°, corresponding to linear step densities of 0.04 and 0.09 steps/nm (assuming full unit-cell step-heights), but other step densities could be achieved via appropriate polishing. Standard surface chemistry techniques will be applied to this uniform step array. *Orlando* has facilities for gas dosing, FTIR, temperature programmed desorption (TPD), AES, and laser spectroscopies. *Leavitt* adds the capabilities of X-ray photoemission spectroscopy (XPS) and *in situ* UHV STM. Using a "vacuum suitcase" and compatible sample holders, samples can also be exchanged with *First* for STM analysis. *Orlando* and *First* have already implemented this capability for a different project.

Electron stimulated desorption (ESD) is one of the few surface analytical techniques sensitive to hydrogen, the most common edge passivating species. *Orlando* and collaborators have recently developed a new technique for detecting and mapping surface adsorbates: Diffraction in electron stimulated desorption (DESD).[85,86,99] In these experiments, a low-energy electron beam (5–100 eV) is directed onto the surface which is mounted on a rotatable stage. Since the low-energy electron-beam can rotate nearly 160° relative to the plane of the surface, rotation of both the sample mount and e-gun allows one to map out desorption yields over the full hemisphere. During this measurement, the incident (reference beam) will interfere with the backscattered wave giving rise to changes in the desorption probability. Thus, we can create a hologram by detecting the diffraction signal which is embodied in the cation yields.[85] We will then be able to determine the location of adsorbates on the surface using a broad-beam sampling mode with chemical specificity and lattice-vector spatial resolution. We propose to further develop the DESD approach to include angle-resolved time-of-flight mass spectrometric techniques.

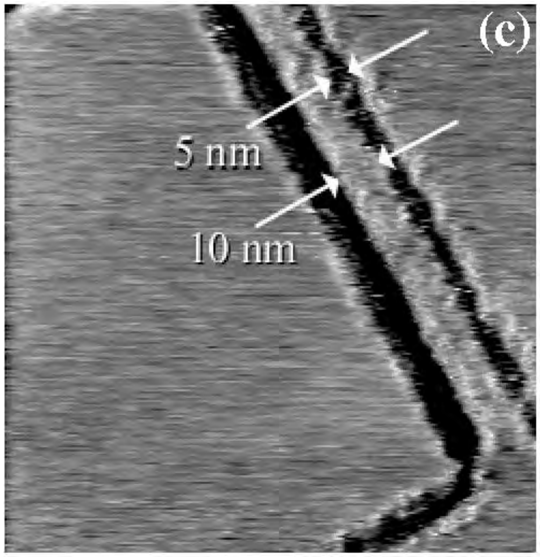

FIG 12: STM-based lithography performed on HOPG at Georgia Tech, demonstrating that feature sizes as small as 5 nm can be patterned on graphitic samples. This technique will be used to modify NG patterns produced by e-beam lithography, providing control at the 5 nm size scale. This capability is very useful for prototype development.

3.2.2 Lithography and patterning

(Berger, de Heer, Marchenkov, Meindl, Orlando)

E-beam lithography, performed at the School of Physics E-beam facility will be the primary lithography method for the first two year of this project (*Berger, de Heer*). This will be augmented by a new GT e-beam nanolithography facility, to be available within the next two years. The tool will have 10-nm resolution and greater flexibility for wafer-scale patterning (*Meindl;* see Facilities). Later phases will include shadow-masking for the application of patterned metals and oxide structures on the graphene (*Berger, de Heer, Meindl*). A crucial property of the epitaxial graphene films is that they are precisely oriented with respect to the SiC lattice. This control will be important for the finest features, in particular when the edge states dominate the transport.[33]

STM and AFM based graphite lithography will be used to locally modify patterned graphene structures (*Berger, de Heer*), allowing the change in transport properties to be correlated with sample modifications. This form of lithography has been developed by Quate[100] and others and has been successfully been applied by Berger and de Heer to produce patterns with 5 nm feature sizes, as shown in Fig. 12. This technique will significantly reduce the minimum feature sizes compared with what is possible with e-beam lithography.

Laser induced chemical modification methods for graphite formation as recently reported in Ref. 101,102. *Orlando* will investigate the feasibility of these techniques for NG, as well as exploring the potential of patterned *growth* of SiC on Si by DESD (see 3.2.1). *Marchenkov* will provide expertise in various nanolithographic methods including patterned thin oxide film technology and other tricks of the trade.

3.2.3 Electrical and thermal transport

(Abrecht, Berger, Chou, de Heer, Ekin, First, Landman, Marchenkov, Pustilnik and post-doc to be appointed)

The electronic transport processes in the graphene films and in the nanopatterned structures will be measured using standard transport measurement techniques. Four point magnetotransport measurements at temperatures from 1.2–300 K in magnetic fields from 0–18 T will be performed, initially at the CNRS facility in Grenoble (Berger, de Heer), and later at NIST (Abrecht, Berger, de Heer, Ekin, post-doc to be appointed). The measurements on films will provide information on the various elastic and inelastic scattering processes with their associated length scales. The low temperature measurements will determine the 2DEG properties, including quantum Hall properties and related effects. Electron mobilities will be determined. The properties will be correlated to the film preparation method and film properties determined from characterization (i.e. defect densities, dopant densities, film thickness etc).

Transport properties of confined structures will be determined as described in Sec. 2.1. These will provide information on electronic confinement effects. In particular, it will be possible to compare the transport properties of an extended film and a confined structure (i.e. a ribbon) on the same sample, which will provide important information on length-scales relevant to transport in the crossover from 1D to 2D and its field and temperature dependence (as already done for sample #29). Particularly interesting will be measurements of the coherence lengths and evidence for high temperature ballistic conduction. Attention will be given to novel 2DEG effects in these various confinement geometries (Berger, de Heer, First, Pustilnik, Landman).

Transport properties of confined gated structures will be relevant for FET-like devices. Device structures are discussed below.

3.2.4 Electronic structure and modification

(Chou, First, Gaylord, Landman, Leavitt, Orlando)

The local electronic structure of graphene layers and "perfect" ribbons (see Fig. 11) will be studied using STM/STS methods from 4K–300K, and in magnetic fields up to 8 T (*First, Gaylord, Leavitt;* see Facilities).[16] *Leavitt* will apply XPS and *Orlando* low-energy laser-induced photoemission. First-principles calculations of the electronic structure of graphene/SiC nanostructures will be undertaken by Chou and Landman for comparison with experimental results. These properties determine the transport parameters and consequently device operation.

Low-temperature STM/STS experiments probe the density of states (DOS) of the graphene structures on the atomic scale. The DOS near the Fermi level will reveal the metallic or semiconducting nature of graphene ribbons of different widths and orientations for comparison with predictions. We will map the local density of states across the graphene ribbon to investigate the topological state that is thought to give rise to ballistic conduction.[33] Observations of both localized and drift states in a magnetic field should help to clarify the role of disorder in the magnetotransport.[103] Such experiments must properly characterize the influence of the electrostatic field from the STM tip. Other combined STM/transport experiments would use the tip field to gate a graphite ballistic transistor at selected positions along the channel. The effect on the source-drain current would provide more information about the local electronic structure along the channel.

The low-temperature STM (LTSTM) described under Facilities has the capability to position the scanned region anywhere within a 5mm diameter circle with < 10 nm resolution. This will allow lithographically-patterned structures to be located, provided directional and identification marks are included in the lithography. The scanning range is 1.2 μm x 1.2 μm at 4 K. We are presently working on large-scale low-resolution imaging in a field-emission mode (tip 20–200 μm from the surface) so that very large device-locating scans can be taken using the large inertial steps of the Beetle-style LTSTM. Additionally, the LTSTM has connections for up to 4 contacts to the sample, sufficient for biasing many basic devices and imaging them under operation.

The electronic structure of the graphene/SiC interface will be studied via XPS (*Leavitt*), quantum-size microscopy,[89,90] and BEEM/BEES *(First, Gaylord)*. BEEM and BEES are 3-terminal techniques that measure the electron current transmitted *through* the graphene/SiC interface (see e.g. Refs. 20). Basic questions, such as the height and uniformity of the Schottky barrier, can be answered using BEEM/BEES. As a quantum mechanical transmission problem, this is a very interesting system due to the expected large wavevector mismatch at the interface.

Space prevents much detail, but another important aspect for ballistic transport and coherence effects is the electronic structure (and conductance properties) of metal/graphene contacts. This will be investigated using STM methods. Our initial measurements of conductance through nanometer-scale metal/graphite contacts with several different metals have shown remarkably low, and nearly universal, contact conductances of $\sim 10^{-5} G_0$.[104] The problem is similar to that of Schottky barrier formation. We expect to seek a collaborator in synchrotron-based photoemission for this work.

The possibility of controlling the carrier density by introducing different chemical "dopants" bound to the graphene edges cannot be ignored. Doping of extended graphene layers is usually done by intercalation, e.g. of potassium or other strong electron donors. The resulting interactions are highly ionic, i.e. electron transfer to the graphene extended orbitals is regarded as complete. For nanographene, these strong interactions may not be desirable. However, it should be possible to terminate the edge bonds with groups that are only slightly "electron withdrawing" or "electron-donating." Nitro groups for instance ($-NO_2$) might be used to deplete electrons in the ribbon. A combination of the electronic structure, surface, and transport techniques described above should enable us to study and control zero-bias carrier densities in the graphene ribbons.

3.2.5 Devices, Architectures, Integration

(de Heer, Gaylord, Meindl)

The novel properties of this material indicate that new device structures and architectures may be required. In anticipation of this eventuality, an interdisciplinary team will propose novel electronics device concepts, structures and architectures for this material.

We anticipate that long coherence lengths and ballistic transport on size scales comparable to those found for carbon nanotubes may exist in this material. A gated ballistic device is sketched in Fig. 13, where an electrostatic gate potential causes reflections of the incoming electrons and thereby gates the device. Device structures that rely on coherent transport may be relevant. An electrostatic quantum interference device, as sketched in Fig. 13. This Fabry-Perot like device relies on the two possible electronic paths. A side gate will modify the electronic wavelength and thereby alter the phase relation of the two electronic paths. Consequently, the transmission through the device will modulated by the gate potential. Other ballistic devices rely on the well known non-linear properties of asymmetric contacts to ballistic conductors.[44] Such asymmetric structures function analogously to directional couplers for microwave structures.

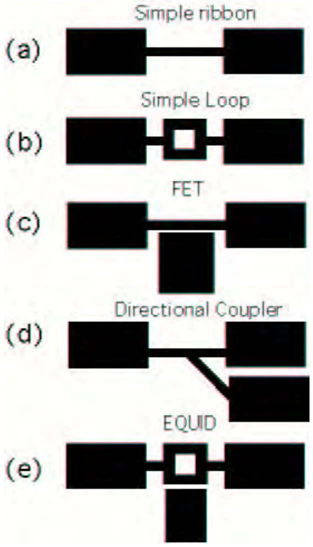

FIG 13: Examples of prototype device structures. a) Simple ribbon: 1D confinement effects. (b) Simple loop: Aharonov Bohm effect, coherent transport lengths. (c) Side gated field effect transistor. (d) Ballistic directional coupler (e) Electrostatic quantum interference device; relies on phase difference between the two paths induced by the electrostatic field (analogous to b for magnetic fields).

Clearly device engineering for this new materials concept will depend upon the material parameters determined in the other thrust areas. These can then serve as in input to rational design methodologies. Similar 2D electron-wave devices have been analyzed and designed previously by *Gaylord*.[91,105–107] For this work, rigorous analogies to electromagnetic wave optics were developed and used to create a design methodology for 2D diffractive and refractive electron-wave devices. The basic principle of steering ballistic electron current instead of storing charge may form the underpinnings of new integrated device architectures.

In previous work, *Meindl* and co-workers have shown that intrinsic fluctuations in dopant density are the critical intrinsic limitation to silicon MOS technology. It remains to determine what the intrinsic limitations will be for the NG materials system. Given material parameters and information about the sensitivity to fluctuations in ribbon-width (see previous Sections), research exploring the *fundamental* limits of integration density and power consumption for this materials system will be carried out. Techniques will be similar to similar to previous research[108–111] (see also 1).

With over 40 years experience in all facets of the semiconductor industry, *Meindl* also is intimately familiar with device and manufacturability issues of importance to industry. This knowledge will be invaluable for exploring potential new device technologies.

4 Integration of Research and Education

Scientists educated through undergraduate, post-graduate, and particularly graduate research constitute the most important means of technology transfer from universities to industry. Eight Ph.D. students and 8 undergraduates will be supported directly through this grant. Their advanced training in fields that impact future technologies is clearly the most direct educational benefit of this funding. However, all levels of education will benefit from the requested funds:

K-12 Education: Clearly the PIs are not experts in education at this level. Therefore our most effective contributions will be in conveying the excitement of science to teachers and students through participation in programs organized and run by professionals in the field. Aided by the requested funding, the PIs will support K-12 education in several ways:

1. Through participation in the Georgia Industrial Fellowships for Teachers (GIFT) program (`www.ceismc.gatech.edu`). GIFT arranges summer fellowships for K-12 math and science teachers at several leading businesses and public science organizations (including Georgia Tech). The program is administered by the Georgia Tech College of Sciences' Center for Education Integrating Science, Mathematics and Computing (CEISMC). Each year, approximately 85 teachers are granted fellowships throughout the state. Typically, a K-12 teacher participates in research during a summer term, interacting closely with senior researchers and graduate students to gain an appreciation of science/engineering principles and practice.

2. Through participation in a proposed Math/Science partnership among Georgia Tech, Fulton County Schools, and Emory University (proposal to be submitted to NSF Dec. 2003, Gary May, PI). This program will focus on 1) Narrowing the achievement gap between White/Asian and Black/Hispanic students by increasing minority academic achievement, and 2) Improving STEM (Science, Technology, Engineering and Math) articulation between high school and college. Georgia Tech and Emory would offer intensive content + simple research courses, short courses in advanced science topics, and a program similar to GIFT.

3. Through less formal but more direct contact with K-12 students. Examples from the PIs experience in recent years include participation in "Science and Technology" nights at local schools, hosting lab visits for K-12 classes, loaning equipment or materials to the local science museum, etc.

Undergraduate Education: Funds to support 8 undergraduates per year (6 at Georgia Tech, 2 at the State University of West Georgia) have been requested specifically for the purpose of enhancing research opportunities for undergraduates. Undergraduates from both institutions will work in conjunction with graduate students and senior personnel on the tasks described previously. Our goal is to have a student participate for at least 1 year in the research program. This is enough time for a good student to make a real contribution, and it is a sufficient basis for an advisor to write a meaningful letter of reference for graduate schools. The PIs will also continue to participate in the NSF-sponsored Research Experience for Undergraduates (REU) programs administered through the School of Physics and the School of Chemistry. In this program, undergraduate students from around the country participate in full-time research for one summer. At present typically 4 undergraduates participate in research of the PIs during the academic year, and an additional 2–4 during the summer through the REU programs.

Courses in Surface Chemistry and Solid State Chemistry are already offered at West Georgia and Georgia Tech, and seminars related to nano-electronics will be developed at West Georgia. At Georgia Tech, the Physics course under the NaST program (see below) is intended to be listed for credit at both senior undergraduate and graduate levels. Within the Microelectronics Research Center, courses in cleanroom procedures are open to all students, and courses in microfabrication are offered through the School of Electrical and Computer Engineering.

Impact on Educational Environment at West Georgia. Participation in this proposal will greatly impact the quality of the faculty-directed undergraduate research currently conducted by Prof. *Leavitt* with his students. The State University of West Georgia is a state comprehensive university located in rural Georgia, 50 miles west of Atlanta and Georgia Tech. The student body is 66% women and 33% men. Slightly over 26% of the student population is classified as non-white. Participation in this project will lead to a long-term exchange relationship between the faculty and students at West Georgia and Georgia Tech, thus providing a very unique experience to the students at West Georgia.

Additionally, students will take frequent and sustained trips to Georgia Tech, thus immersing themselves in the research environment. Undergraduate students who typically work with Prof. *Leavitt* routinely choose to attend graduate school based upon their research experiences.

Graduate Education: In addition to research training, several of the PIs and senior personnel have committed to teach or team-teach courses for a new graduate certificate program in Nanoscience and Technology (NaST; see `www.chemistry.gatech.edu/nast`). The courses will emphasize new and evolving paradigms, such as those described herein, that are likely to underly technologies of the future. In order to earn a degree certificate, a student will be required to complete 4 courses in different departments. This assures interdisciplinary training in the science, technology, and system architectures that will drive future technological advances.

Post-graduate Education: At the post-graduate level, the PIs will continue their participation in the Faculty Development Program (FDP) at Georgia Tech (`www.cos.gatech.edu`). The FDP provides in-state faculty in two- and four-year institutions an opportunity to engage in research and teaching activities during a one- to two-semester visit to Georgia Tech. The aim is to allow visiting faculty an opportunity to “re-tool” in their field and to establish mutually beneficial partnerships with faculty at Georgia Tech that will allow for continued participation in scholarly activities. The PIs/senior personnel have hosted 2 FDP participants since 1998. An FDP-initiated collaboration with *Leavitt,* has resulted in a stronger research team for this proposal. His prior research experience with graphite has been extremely beneficial. We anticipate similar continuing collaborations with future FDP participants.

5 Diversity in the Program

Our efforts with regard to greater inclusion of underrepresented groups fall naturally into the educational and research plans by virtue of the already diverse student body at Georgia Tech and at Atlanta area schools (the Atlanta school system consists of well over 50% minority students). Thus presentations to school groups and research experiences for teachers will impact an enormous number of minority students. At the college level, Georgia Tech already ranks first in the country in the number of graduate degrees awarded to students from under-represented minority groups and women, and has a similar rank for the number of minority undergraduate degrees in engineering. Part of our mission will be to attract a larger fraction of these highly-qualified students into fundamental materials research and that impacts nanotechnology. We intend to accomplish this through the educational programs outlined above and through more effective informal education (i.e. advertising). The PIs currently supervise eight students from groups traditionally underrepresented in the sciences and engineering (African-American, African, Hispanic, Asian-American, Female).

Integrating diversity into this research program requires active recruitment of graduate students from underrepresented backgrounds. Consequently, the participating academic units must have a strong commitment to recruiting a diverse pool of graduate students from which this program can draw. The School of Chemistry administers a Department of Education GAANN program (Graduate Assistantships in Areas of National Need) which focuses specifically on this issue, providing 11 fellowships per year for the recruitment and retention of graduate students from under-represented and financially disadvantaged backgrounds. Drawing largely from the Southeast, recent graduate student demographics in Chemistry were: 64% Caucasian, 18% Asian, 10% African-American, 4% Asian American, and 3% Hispanic. Additionally, 40% of Chemistry grad students are female.

The School of Physics has a GAANN proposal pending with the Department of Education, requesting 12 graduate assistantships, to be matched by 3 additional fellowships from Georgia Tech. In the recent past, the department has been successful at recruiting minority students into the Physics graduate degree programs: From 1994–1996 the School of Physics at Georgia Tech graduated 9 female students and 8 African-American/Hispanic students, with minority students coming primarily from undergraduate institutions in the Southeast. In those years, underrepresented groups accounted for 33%, 50%, and 25% of the total graduating class of the School. Graduate student numbers and diversity declined during the late 1990's, but have jumped well beyond expectations in the past two years (~ 70 new Physics grad students in the last 2 years). With the powerful stimulus afforded by the GAANN programs, we expect that the School of Physics will reproduce its previously demonstrated success in this area, thus adding to a diverse pool of graduate students for the research proposed here. Efforts to recruit women are already gaining momentum, with just under 1/3 of the entering graduate class this year consisting of women.

The Microelectronics Research Center is not an academic unit, so it does not directly recruit graduate students. However, it is closely tied to the College of Engineering and the School of Electrical and Computer Engineering, where *Meindl* and *Gaylord* are Professors. In the College of Engineering the record speaks for itself: Efforts toward training students from traditionally under-represented backgrounds have put Georgia Tech consistently in the top 1–2 institutions in number of engineering degrees granted to minority students.

6 Organization and management

On an annual basis, the project will employ 1 postdoc (2 in years 3 & 4), 8 graduate students (6 NSF funded, 2 GT funded) and 8 undergraduates (6 at GT, 2 at West Georgia) in addition to partial salary support for one senior researcher and minimal summer salary for three of the four PIs. Research responsibilities have been detailed in Sec. 3. Here we focus on the management of resources and students.

Overall organization and goals will be discussed at 6 formal meetings of all participants (2 per academic term). A substantial portion of these meetings will be devoted to student talks, on a rotating basis, with extensive time for comments and coaching in the art of good presentations. The PIs and senior participants (those at GT and West Georgia) will meet privately after student presentations to discuss financial matters and research directions. Out-of-state collaborators will be invited to participate in meetings via a conference speaker-phone, and we will work with technical staff to set up a web meeting link.

Since most of the participants have worked together in the past, no contentious problems are anticipated. However, the formal procedure for dealing with any potential issues will be first, a meeting of the PIs to try to reach a solution, and second, resolution by the Project Director (de Heer). Requests by participants for reallocation of resources will be considered by all 4 PIs. In the unlikely event that no consensus can be reached, the Project Director will make the final decision.

Students will typically work between two different labs, but with a single main advisor in their home department. Anticipated pairings are as follows (research responsibilities as in Sec. 3):

RA 1: *De Heer, Meindl*	**RA 5:** *Orlando, First*
RA 2: *Marchenkov, de Heer*	**RA 6:** *First, Gaylord*
RA 3: *First, de Heer*	**RA 7:** *Meindl, Gaylord*
RA 4: *Orlando, Leavitt*	**RA 8:** *Conrad, First*

Supervisory responsibility for postdocs will lie formally with the Project director, but this would be delegated depending on the most immediate needs of the project. Dr. Claire Berger will remain predominantly in de Heer's lab until she returns to CNRS in years 3 and 4.

Dissemination of results. Technical results of this research will be published in peer-reviewed journals. With the assistance of web authors in the various units, a distinct home page for this research will be constructed and used to facilitate access to publication links and to provide a more pedagogical presentation of the research. The pages will be useful for recruitment of students into nanoscience and engineering-related research and for dissemination of information to the general public.

6.1 Timetable and Milestones

Year 1: Primary material development

- High quality SiC(0001) surfaces by thermal treatment and H_2 etching.
- Extended high quality epitaxial graphite on SiC.
- Understanding and control of graphite thickness and growth properties.
- Simple patterned NG structures with crystallographic alignment control.
- Fundamental 2DEG transport properties of extended films.
- Low temperature CVD production of graphene films.

Year 2: Transport properties of NG structures down to 50 nm at low temperatures

- 1μm x 1μm high quality graphite on SiC; low transport properties of these layers.
- Low temperature transport properties of simple NG structures (ribbons and simple junctions).
- Size dependence of transport properties of NG at low temperatures.
- Demonstration of coherent transport in NG structures; Demonstration of methods. to produce graphite-interconnected as well as metal-contacted structures using conventional lithographic methods on the 50 nm size scale and larger.
- Fundamental 2DEG transport properties of extended films (continued) and of simple patterned structures.
- Chemical modification and electronic structure determination of graphene edges.

Year 3: Transport properties of NG structures below 50 nm up to room temperature

- STM modification of e-beam patterned structures to produce features down to 5 nm.
- Temperature dependence of the transport properties of NG ribbons between 5-100 nm in width.
- Electronic properties of loops and gated loops (EQUIDs) on the 10-50 nm scale.
- Transport and properties of novel device structures.

Year 4: Electronic devices; integration with Si

- Demonstrate a gated three terminal device: Conventional FET structures.
- Demonstration of a two terminal quantum interference device; Demonstration of a ballistic three terminal FET device.
- Demonstration of a coherent electronic switching device at low temperature.
- Demonstration of a room temperature ballistic FET; Method to graphitize SiC grown on electronics grade Si, for future integration of NG into Si based electronics.

7 Conclusion

A sound program has been presented integrating research, education, and strong efforts to promote diversity in nanoscience and nanotechnology research. The scientific program presented here is unique. It draws from a decade of experience in nanographite science and adds the critically essential ingredient of control. It fully recognizes that the exceptional electronic properties often attributed to carbon nanotubes are by no means unique to them. They are ultimately derived from graphite and are probably common to a large variety of nanographitic structures. In theory, many of the schemes proposed for nanotube electronics can be transferred to two-dimensional equivalents. The preliminary results presented here are the result of years of hard work by a dedicated team that is convinced of the necessity of this line of research. Their tireless effort is now starting to pay off. Basic sample preparation and characterization techniques have been mastered. Our recently obtained results clearly point to a new, relatively high temperature two dimensional quantum electron gas. This discovery, more dramatic than originally expected, clearly indicates that a wealth of new physics is around the corner. Still, a great deal of ground-breaking work must be done in many areas of this multi-faceted program in order to realize the potential of nanopatterned graphene. But the path to success is now clearly defined and we are certain our team is on the verge of opening the door to a new field of nano-science and technology.

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(12) **United States Patent**
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(54) **PATTERNED THIN FILM GRAPHITE DEVICES AND METHOD FOR MAKING SAME**

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(57) **ABSTRACT**

In a method of making graphite devices, a preselected crystal face of a crystal is annealed to create a thin-film graphitic layer disposed against selected face. A preselected pattern is generated on the thin-film graphitic layer. A functional structure includes a crystalline substrate having a preselected crystal face. A thin-film graphitic layer is disposed on the preselected crystal face. The thin-film graphitic layer is patterned so as to define at least one functional structure.

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