Caractérisation, mécanismes et applications mémoire des transistors avancés sur SOI

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UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

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Spécialité : **Nanoélectronique et Nanotechnologies**

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dans **l'École Doctorale EEATS**

Caractérisation, mécanismes et applications mémoire des transistors avancés sur SOI

(Characterization, mechanisms and memory applications of advanced SOI MOSFETs)

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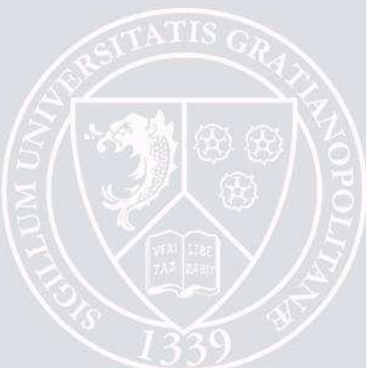

Characterization, Mechanisms and Memory Applications of Advanced SOI MOSFETs

General Introduction

For several decades, the goal of the semiconductor industry was to scale down the transistor size in order to increase integration density. But, the era of planar bulk-silicon CMOS is over. According to the International Technology Roadmap for Semiconductors (ITRS), there are two options for the next generations of CMOS circuits: fully depleted (FD) SOI (strongly supported in Grenoble by STMicroelectronics, Soitec, LETI and our laboratory) and FinFETs. These transistors will continue the miniaturization trends while also answering the requirement for low-power operation in portable electronic devices and embedded systems. The association of the legendary players (Si and SiO_2) with alternative semiconductors and dielectrics is equally envisioned for enriching the device functionality. A transistor can do more than just switching on and off.

In this context, the initial topic of this thesis was to explore innovative single-transistor memory devices fabricated with FDSOI and FinFET technologies. Our results on nonvolatile and volatile data retention are exposed in Chapters 4 and 5, respectively. We show how the transistor can store the charge and evolve into multi-bit flash memory and capacitorless DRAM. A novel concept of unified memory is demonstrated by advantageously combining these two memory modes.

The key mechanism enabling memory functions is the inter-channel coupling, mitigated by floating-body, short-channel and transport effects. For achieving our objectives, the PhD work has started with a detailed investigation of coupling and associated effects in state-of-the-art MOSFETs (Chapter 2). Our results in section 2.1 reveal the operation of FDSOI transistors by focusing on the impact of ultrathin SOI films (down to 5 nm thickness), back-gate biasing and low temperature. A similar study was conducted for FinFETs. In Section 2.2, we describe the role of the fin width and channel length. It is demonstrated that the 3D coupling mechanisms are different in triple-gate and double-gate FinFETs, the latter devices being more amenable to back-gate biasing schemes.

Since ZnO TFTs operate very much like SOI MOSFETs, we have attempted to apply the same methodology to these emerging devices as well. We have faced modeling and parameter extraction issues that were solved as described in Section 2.3.

It is less notorious that the inter-channel coupling does affect the carrier mobility behavior. For obtaining an accurate picture, our approach aimed at using the most

indisputable technique for mobility evaluation which is the geometric magnetoresistance. As this topic revealed to be very interesting and intriguing, we have developed the method for the characterization of FinFETs. The experimental data shown in Chapter 3 points on the failure of the ‘universal mobility’ law in both FDSOI and FinFETs.

Our work combines systematic measurements, numerical simulations and physics based models extending from the transistor to the memory device.

Table of Content

General Introduction

Chapter 1: General Introduction

1.1. Context of the Work

1.2. Silicon on Insulator Technology

1.2.1. Motivations of SOI transistor

1.2.2. Classical classification of SOI devices

1.3. Impact of Miniaturization on Transistor Performance

1.3.1. Series resistance effects

1.3.2. Velocity saturation

1.3.3. Short-channel effects

1.4. Advanced Device Architecture and Technology

1.4.1. High-K/Metal gate stack

1.4.2. Strain technology

1.4.3. Planar fully-depleted (FD) SOI transistor

1.4.4. 3-Dimensional fully-depleted (FD) SOI transistor

1.5. Conclusion

Chapter 2: Advanced Devices and Typical Effects

2.1. Typical Properties in FD SOI MOSFETs

2.1.1. Introduction

2.1.2. Parameter extraction techniques and typical properties

2.1.3. Si film and BOX thickness effects

2.1.4. Coupling effect

2.1.5. Temperature-dependent properties

2.1.6. Conclusion

2.2. Coupling Effects in Double-Gate FinFETs

2.2.1. Introduction

2.2.2. Typical properties

2.2.3. Coupling effects

2.2.4. Conclusion

2.3. Mobility Behavior and Models for Nanocrystalline ZnO TFTs

2.3.1. Introduction

2.3.2. ZnO TFT overview

2.3.3. Typical properties of our ZnO TFTs

2.3.4. Parameter extraction methods

2.3.5. Temperature-dependent characteristics

2.3.6. Conclusion

Chapter 3: Magnetoresistance Measurements and Unusual Mobility Behavior in FD SOI MOSFETs

3.1. Introduction

3.2. Theory of Magnetoresistance Mobility

3.3. Magnetoresistance Mobility in Planar FD SOI MOSFETs

3.3.1. Front-channel mobility

3.3.2. Back-channel mobility

3.4. Magnetoresistance Mobility in FD SOI Triple-gate FinFETs

3.4.1. Front-channel mobility

3.4.2. Back-channel mobility

3.5. Magnetoresistance Mobility in FD SOI Double-gate FinFETs

3.6. Conclusion

Chapter 4: Remote Carrier Trapping in ONO FinFETs for Innovative Flash Memory

4.1. Introduction

4.2. Nonvolatile Memory

4.2.1. Classification of nonvolatile memory

4.2.2. Flash memory cell

4.2.3. Future evolution of flash memory cell

4.2.4. Alternative nonvolatile memory

4.3. Charge Trapping in Si_3N_4 Buried Layer
4.4. Nonvolatile Memory Effects
4.4.1. Nonvolatile memory effects induced by back-gate bias stress
4.4.2. Nonvolatile memory effects induced by drain bias stress
4.4.3. Drain current hysteresis in dynamic mode
4.5. Conclusion

Chapter 5: FinFETs with ONO BOX for Multi-Bit Unified Memory
5.1. Introduction
5.2. Volatile Memory
5.2.1. Conventional volatile memory
5.2.2. Capacitorless 1T-DRAM
5.2.3. Unified RAM (URAM)
5.3. Volatile Operation as a Capacitorless 1T-DRAM
5.3.1. Multi-bit volatile operation combined with back-gate biasing
5.3.2. Multi-bit volatile operation combined with drain biasing
5.4. Conclusion

Conclusion

References

Publications

Résumé du Travail de la Thèse en Français

Acknowledgement

Chapter 1

General Introduction

1.1. Context of the Work

The number of circuit components on a microchip has sharply increased and the performance of a unit transistor has improved substantially thanks to the successful shrinking of bulk-Si MOSFETs (metal-oxide-semiconductor field effect transistors) since J. Kilby invented the concept of an integrated circuit (IC) in 1958. The scaling of the CMOS technology has followed “Moore’s Law”: In 1965, G. Moore anticipated that the IC device packing density will double every 18 months [1]. Moreover, C. G. Hwang suggested a new model for the memory industry: a two fold increase per year in memory density [2]. For the last forty years, silicon-based transistor has tracked these laws without any major change of the basic planar MOSFET structure. This architecture has been scaled down to gate length of $L_G \approx 20$ nm by involving more complicate and precise fabrication process.

Recently, however, such scaling has been slowed down because the conventional CMOS process has researched critical limits. For example, the complex doping profiles cause reliability, yield and cost issues. The unavoidable randomness of dopant atoms produces variations in device properties. Indeed, in a conventional bulk-Si CMOS technology, there is no additional methodology to enhance performance beyond the 22 nm technology node. Therefore, many technical solutions have been proposed to optimize the existing structures or to introduce new architectures for further scaling the transistor. According to the ITRS transistor architecture roadmap shown in Fig. 1-1 [3], two main candidates are considered in order to enable continued CMOS scaling: (i) the planar fully depleted (FD) SOI MOSFET with a thin buried oxide (BOX), thin silicon film (T_{si}) and heavily doped ground plane (GP) [4]; (ii) the (bulk-Si or SOI FD) FinFET with simplified 3D processing [5, 6]. Both structures provide high device performance and improved gate control.

Planar FD SOI MOSFET has evolved from the initial partially depleted SOI MOSFET technology. The fabrication process of the SOI device is rather similar to that of the conventional bulk-Si MOSFETs. Nevertheless, it offers excellent device performance. The device scalability and undesired parasitic effects are mainly governed by the thickness of silicon film and buried oxide. The GP (or substrate) bias V_{BG} can be an additional option to modulate the front-channel properties. Recently, A. Khakifirooz *et al.* [7] reported outstanding results in ultra-thin film (T_{si} = 3.5 nm) and short (down to 18 nm) device: good gate control, low off-state current (I_{OFF}) with reasonable on-state current (I_{ON}) and threshold voltage V_{TH} tuning by back-gate bias V_{BG}. Also, C. Fenouillet-Beranger *et al.* [8] described

more viable characteristics of FD SOI device with thin BOX (T_{BOX} = 20 nm). Obviously, these recently developed nanoscale SOI MOSFETs imply short-term feasibility of the SOI planar device in CMOS applications.

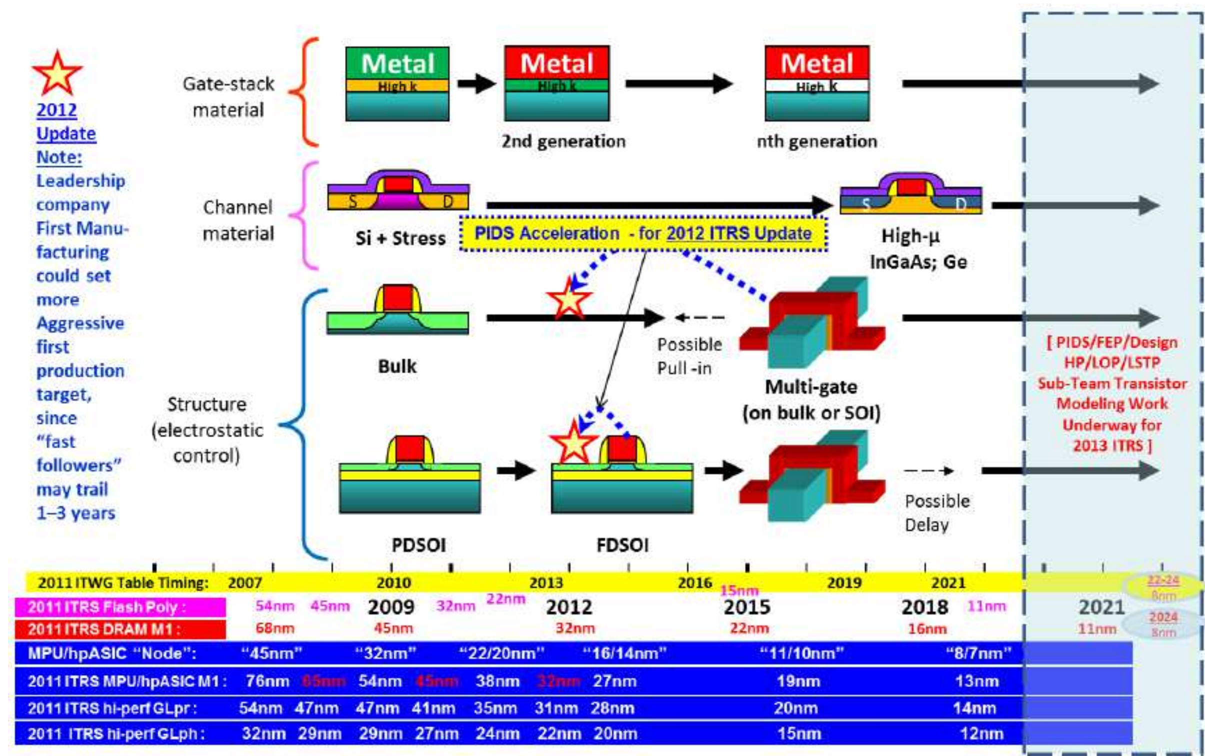

Fig. 1-1: ITRS transistor architecture roadmap. "Equivalent Scaling" process technologies Timing, MPU/High-performance ASIC Half Pitch and Gate Length Trends, and Industry "Nodes".

FinFET is more revolutionary and has more potential than planar FD SOI MOSFET from a long-term perspective. This novel structure was invented in 1991 by folding the planar MOSFET [5] and was further developed after 2000. This 3-D architecture requires etching process to define the fin but the overall fabrication sequence is not far from that of the planar MOSFETs. Basically, the FinFET has two lateral gates (*i.e.*, double-gate (DG) device). A third gate can also be switched on at the top of the fin. By co-operation of the three gates, good electrostatic control is achieved. Actually, Intel Corporation announced that FinFETs, or so-called triple-gate transistor [9, 10], are already adopted for their 22 nm technology node. Despite Intel uses bulk-Si substrate, scaling FinFETs down to 10 nm will probably demand SOI substrate. Recent works on FD SOI FinFET architecture reported promising performance for next generation CMOS circuits.

This thesis is dedicated to theoretical and experimental researches of several advanced

SOI FD MOSFETs. Electrical characterization, modeling and simulation were carried out in order to investigate the device properties, physical mechanisms and appropriate applications.

The first chapter will briefly cover SOI technology, short-channel effects (SCEs) and the technologies to improve device performance. The advanced planar FD SOI and FinFET architectures will also be introduced.

In the second chapter, the properties of several advanced FD SOI devices will be investigated and discussed. In planar FD SOI device, the impact of temperature, back-gate bias and Si film thickness on device performance will be presented through systematic measurement results. Next, the characteristics of advanced SOI FinFETs will be shown via measurement and 3-dimensional simulation results. Especially, coupling effect will be reported for a various range of fin width in vertical DG and triple-gate FinFETs. Particular mobility behavior in ZnO thin film transistor (TFT), which operates similarly to an SOI MOSFET, will also be shown through low-temperature measurements. Simple mobility models and parameter extraction techniques will be introduced.

In the third chapter, mobility behavior will be addressed by way of low-temperature geometrical magnetoresistance measurement in advanced planar FD SOI and FinFET. Unusual mobility behavior is demonstrated to be induced by the inter-action between front- and back-gate based on the variation of the inversion charge centroid.

In the forth chapter, flash memory application will be explored in FinFETs fabricated on alternative SOI wafers with ONO BOX. In the first part, the basic device characteristics will be introduced. Then, appropriate charge injection mechanisms will be reported for a various range of the fin width, gate length and temperature. The impact of bias condition on the charge injection efficiency will also be discussed.

In the final chapter, we will describe the capacitorless DRAM application with the same device used as in chapter 4. Therefore, we will see that two different memory functions, volatile and nonvolatile, can be performed in a single transistor. Above all things, multi-bit volatile memory is demonstrated by advantageously combining the nonvolatile and volatile memory modes. Experimental results reveal the impact of the geometrical parameter and bias condition on the volatile memory sensing margin.

1.2. Silicon on Insulator Technology

In a conventional bulk wafer, the thickness of active area (~ 10-100 nm) used for

fabrication and operation of the transistors is very small compared to the total wafer thickness (~ 800 μm). Unfortunately, the unused part of wafer, which serves as mechanical support, causes parasitic effects, degrading device performance. On the other hands, silicon-on-insulator (SOI) technology consists of a single crystalline Si film (active area) separated by SiO_2 layer or buried oxide (BOX) from the bulk substrate, reducing parasitic capacitance and leading to faster transistor switching [11, 12]. Beyond these benefits, there are many other motivations for utilizing SOI technology.

1.2.1. Motivations for SOI transistor

Historically, there have been several reasons for developing and using SOI technology. In the 1970s and 1980s, radiation hardness was the main motivation for choosing SOI substrate. The impact of ionizing radiation on device performance is minimized by the thin active Si film. For example, the majority of charges generated by an alpha particle encroaching on a Si substrate would be stopped by the buried oxide, hence reducing the current surge in the active film [11].

Recently, ultra large scale integration circuits (ULSIC) contain hundreds of millions of single transistors. In SOI technology, a single transistor is isolated from each other and from the silicon substrate. On one hand, the thin silicon film used as active area is protected by the vertical isolation from parasitic effects induced by bulky substrate: leakage currents, latch-up effects and radiation-induced photocurrents. On the other hand, the lateral isolation enables the separation of transistors by completing simple trench or well formation. Therefore, the entire technology and circuit design are significantly simplified and more compact chips can be obtained.

In addition, many semiconductor companies use SOI wafers in order to obtain high performance and low power consumption. Source and drain regions extend down to the buried oxide (BOX), achieving reduced junction capacitance and lower leakage current. As a result, SOI CMOS circuits offer improved speed and lower power dissipation in standby and operating modes.

The main advantage of SOI technology is the superior ability for the device scaling down. Unlike for the bulk technology, the SOI film and BOX thickness are tunable elements for device shrinking. Ultra-thin film SOI devices are less susceptible to SCEs originated from charge sharing between gate and junctions due to the limited extension of drain and source

regions. The drain-to-body field which causes drain-induced barrier lowering (DIBL) effect is also controlled by the thin silicon film. In parallel, SOI structure can be easily combined with innovative device, especially multi-gate transistor, to achieve better immunity against the SCEs.

1.2.2. Classical classification of SOI devices

According to the Si film thickness, the depletion region covers partially or completely the whole transistor body giving the names of partially-depleted (PD, Fig. 1-2a) and fully-depleted (FD, Fig. 1-2b) SOI MOSFETs, respectively.

(a) Partially-depleted (PD) SOI MOSFETs

In PD SOI MOSFETs, a neutral region exists in the transistor body as the film is not completely depleted. Therefore, coupling effects (modulation of the electrical properties of one channel by the applied bias at the opposite gate) disappear but floating-body effects arise. The kink effect is generated by collecting majority carriers in the neutral body. As a result, the body potential is increased, the threshold voltage is decreased and excess current is exhibited. The floating body also causes transient variations of body potential, threshold voltage and current. Current undershoot is generated when the gate is changed from strong to weak inversion: the drain current increases with time as the majority carriers are generated allowing the depletion depth to shrink when the gate voltage is raised. A reciprocal phenomenon can occur when the channel is activated. The majority carriers are expelled from the increasing depletion region and collected in the body. Thus, drain current overshoot occurs and then gradually decreases with time by electron-hole recombination [13].

(b) Fully-depleted (FD) SOI MOSFETs

In FD SOI MOSFETs, the Si film thickness is thinner than the maximum depth of the depletion region defined as $X_{dmax} = X_d(\phi_s = 2\phi_F) = \sqrt{4\varepsilon_{si}\phi_F/qN_d}$. This means that the depletion charge is constant and cannot enlarge with increasing gate bias. For this reason, FD SOI exhibits an excellent coupling between the gate bias and the inversion charge that improves the drain current and subthreshold swing. It is possible to obtain two inversion channels, one at the front interface and the other at the back interface.

FD devices exhibit several unique characteristics:

(i) When the opposite gate bias increases, the threshold voltage decreases between two plateaus corresponding to accumulation and inversion of the opposite channel (Fig. 2-14) [14].

(ii) The contribution of both front- and back-interface traps is reflected in the subthreshold slope. In case of front-channel, when the back-channel lies in depletion regime, the threshold slope becomes a maximum (60 mV/decade of current) [15].

(iii) The transconductance curve has a plateau when the opposite channel is inverted (Fig. 2-22a) [16].

(iv) The mobility and series resistance depend on the opposite gate bias due to the modulation of the effective vertical electric field [16].

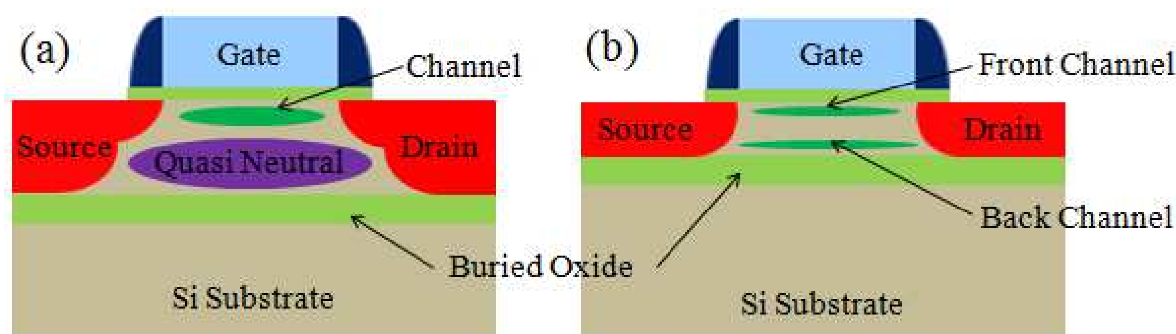

Fig. 1-2: Cross-section of the conventional (a) partially-depleted (PD) and (b) fully-depleted (FD) planar SOI transistors.

Both PD and FD SOI MOSFETs have their own advantages for various applications. In this thesis, we will focus on the characterization of several different types of advanced FD SOI MOSFETs. Also, their applications to memory devices will be discussed. The unique properties described above will be documented with measurement and simulation results in the following chapters.

1.3. Impact of Miniaturization on Transistor Performance

In an electronic circuit, there are two essential factors to be considered: one is the switching speed and the other is the power consumption. The switching time τ (or intrinsic delay) of a transistor is defined as:

$$\tau = \frac{V_{DD}C_{ox}}{I_{ON}} \tag{1.1}$$

where V_{DD} is supply bias, C_{ox} is oxide capacitance and I_{ON} is onset current corresponding to the applied V_{DD}.

The static power is defined as:

$$P_S = I_{OFF} V_{DD} \tag{1.2}$$

where I_{OFF} is current for $V_G = 0$ V.

The I_{OFF} current should be as low as possible in order to minimize the static power. On the other hand, it is essential to keep a high I_{ON} current to achieve a switching speed as short as possible. There are three methods to enhance I_{ON} current while short switching time is maintained:

(i) Increase supply bias V_{DD},
(ii) Reduce oxide thickness in order to increase oxide capacitance C_{ox},
(iii) Reduce channel length L_G.

The first approach is not suitable because of power dissipation. The reduction of channel length will successfully improve τ and I_{ON}. Moreover, integration density increases as the size of transistor is reduced. However, channel length scaling yields several undesired effects and requires modification of transistor features according to the scaling rules.

1.3.1. Series resistance effects

In a transistor, the total resistance is expressed as a sum of channel resistance, reduced with gate length, and source and drain series resistance (R_S and R_D) as shown in Fig. 1-3. In long channel device, the potential drop due to series resistance is relatively small and negligible compared with the drain bias V_D. However, the series resistance becomes no longer negligible in short device. In the ohmic regime, the effective voltage between source and drain (V_{RS}) is lower than the applied V_D. Therefore, the action of the series resistance should be considered when a short channel device is characterized.

$$V_{RS} = V_D - (R_S + R_D) I_D \tag{1.3}$$

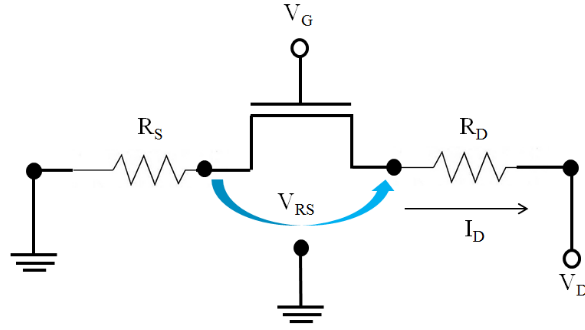

Fig. 1-3: Equivalent circuit showing the influence of series resistance on MOSFET.

1.3.2. Velocity saturation

In a transistor, electron transport is governed by electric field E and carrier scattering with the lattice, impurity atoms, surface and other carriers. At low electric field, the drift velocity is described as [17]:

$$v_d = \mu E \quad (cm/s) \tag{1.4}$$

where μ is carrier mobility. The drift velocity is proportional to the electric field.

However, at high field, this linear relationship does not hold due to the energy dependence of scattering relaxation time. The field dependent drift velocity is written as [18]:

$$v_d = \frac{\mu E}{1 + E/E_C} \quad for \quad E < E_C \tag{1.5}$$

$$v_d = v_{sat} \quad for \quad E > E_C \tag{1.6}$$

where the critical field E_C is approximately 10^4 V/cm for Si. Carrier velocity is saturated to v_{sat} when E is above E_C.

According to this consideration, the appropriate short-channel current model is:

$$v_d = v_{sat} = \mu E_C \quad for \quad E > E_C \tag{1.7}$$

$$V_{Dsat} = LE_C = Lv_{sat} / \mu \tag{1.8}$$

Therefore, the conventional drain current equation in nonlinear region:

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_G - V_{TH}) V_D - \frac{V_D{}^2}{2} \right] \tag{1.9}$$

is modified as:

$$I_{Dsat} = v_{sat} C_{ox} W \left[(V_G - V_{TH}) - \frac{V_{Dsat}}{2} \right] \tag{1.10}$$

1.3.3. Short-channel effects

With the scaling down of transistors, parasitic effects which can be neglected for long channel become significant elements. These unintended effects which limit the miniaturization and performance of devices are commonly named as short-channel effects (SCEs).

(a) Charge sharing

In a long channel device, the semiconductor channel is completely under the control of the gate. However, as the transistor is scaled down, source and drain junctions become closer to each other, causing a fraction of the depletion charge in the channel to lose control of gate electrode. In other words, the gate and source-drain biases share control of the charge density below the gate. Fig. 1-4 shows the shared depletion charge regions, with approximately triangular shape, near source and drain. This phenomenon is explained by the charge-sharing model [19].

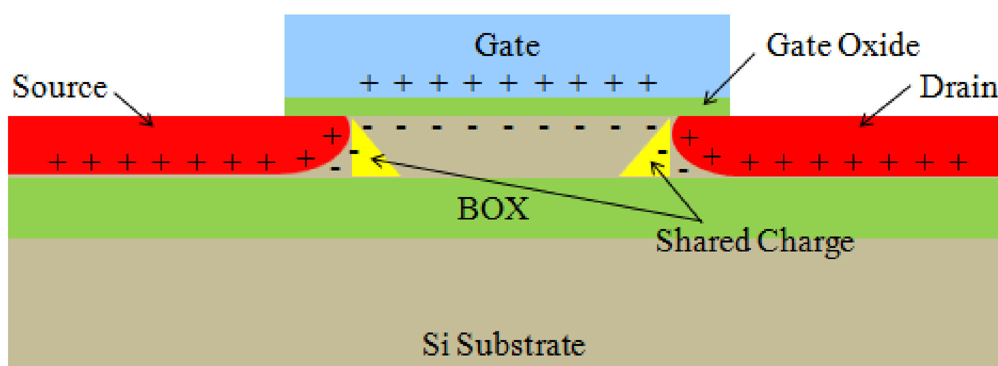

Fig. 1-4: Cross-section of SOI MOSFET along the length showing depletion charge sharing between the gate, source and drain.

This charge sharing effect has strong impact on subthreshold characteristics and

threshold voltage. Once, the width of S/D depletion regions becomes non negligible compared with the channel length, the depletion charge controlled by the gate is reduced. As a result, V_{TH} becomes lower (threshold voltage roll-off) [19].

(b) Hot carrier effect

If carriers gain high kinetic energy due to the electric field, their energy is partially transferred to the lattice through collisions with acoustic and optic phonons. When a strong electric field is applied, the carriers can gain more energy than they can transfer to the lattice. This can be described by using a Maxwell distribution as $T_P > T_r$, where T_P and T_r are the carrier and lattice temperature. Therefore, the carriers become "hot" thanks to the applied electric field [20]. In short device, when an electron travels from the source to the drain along the channel, it gains kinetic energy in the pinch-off region and becomes a hot carrier [17].

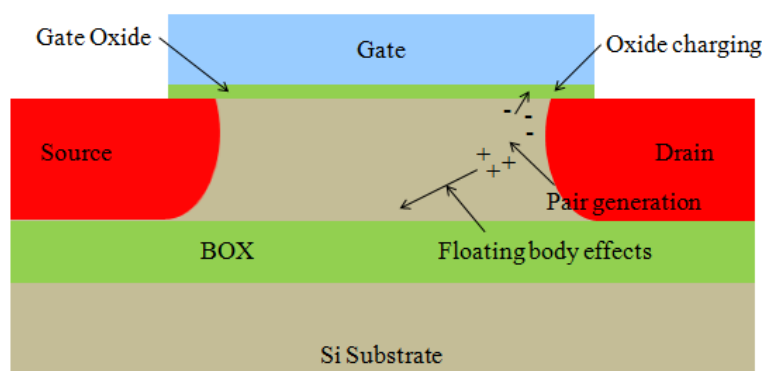

Fig. 1-5: Cross-section of SOI MOSFET along the length showing hot carrier generation (impact ionization) and its effects (floating body effects, gate oxide degradation and fixed oxide charge).

Several undesired effects induced by hot-carrier are summarized in Fig. 1-5. One of the major results of hot carrier effect is the generation of electron-hole pairs by impact ionization. This phenomenon occurs when carriers obtain enough energy to ionize atoms. In SOI MOSFETs, generated hole are stored in the body while electrons move to the drain, inducing floating body effect. Some of the hot carriers can go through the gate oxide and be collected as gate current. More importantly, some of these electrons can be trapped in the gate oxide and become fixed oxide charge. Thereby, the flat-band voltage and threshold voltage are changed and quality of the gate oxide is degraded [17].

(c) Drain induced barrier lowering (DIBL)

Fig. 1-6 shows a more detrimental SCE which is DIBL. When the drain bias is raised,

the conduction band edge (which reflects the electron energies in n-channel MOSFETs) in the drain is pulled down and the drain-channel depletion width expands. For a long channel device, the drain bias does not impact the source-to-channel potential barrier, which corresponds to the built-in potential of the source-channel p-n junction [21]. However, for a short device, as the drain bias is increased, the source-channel potential barrier is lowered due to DIBL [17]. DIBL is mainly caused by the lowering of the source-junction potential barrier below the built-in potential. This effect depends not only on the channel length and drain bias but also on the source/drain junction depth and channel doping.

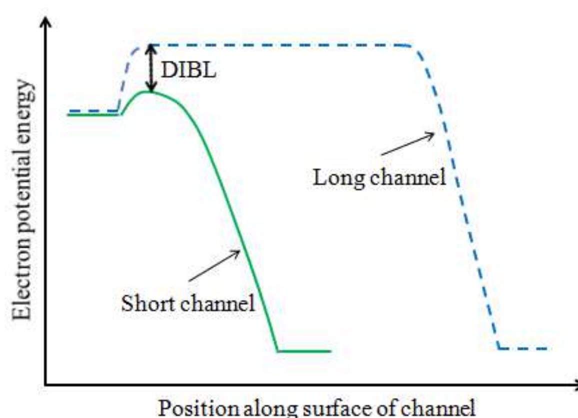

Fig. 1-6: Potential distribution along the channel for a long channel and short channel MOSFET showing drain-induced barrier lowering.

This phenomenon limits the maximum operation voltage of a device [22]. In order to avoid this problem, the source/drain junctions must be sufficiently shallow as the channel length is reduced. Therefore, a channel doping and/or a localized implant near source and drain known as halo (or pocket) implant [23] can be processed to reduce DIBL. It will decrease the source/drain depletion widths and prevent their interaction.

(d) Punchthrough effect

In short device, two depletion regions can be overlapped when the depletion region around the drain extends to the source (Fig. 1-7) [24]. This effect depends on the applied drain bias and junction depth [21]. Punchthrough occurs when drain bias impacts the formation of inversion layer, leading rapid increase of drain current and loss of gate control.

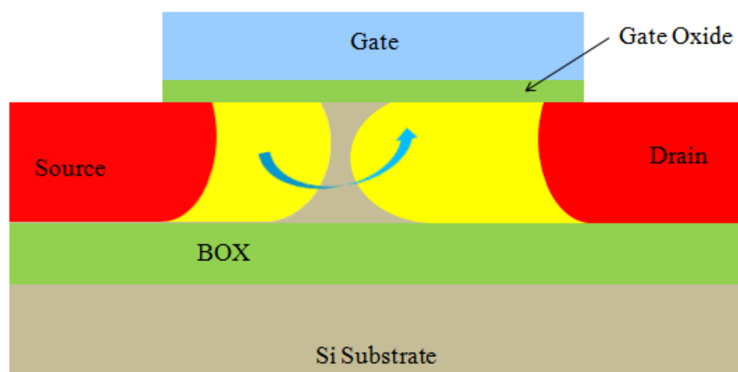

Fig. 1-7: Cross-section of SOI MOSFET along the length showing the punch-through effect.

1.4. Advanced Device Architecture and Technology

To overcome SCEs and improve the device performance, advanced MOSFET techniques have been studied. Thinner gate oxide and heavily doped channel were required for good gate control with decreasing gate length. However, they cause the degradation of the device reliability and mobility. Therefore, high-k/metal gate stack has been proposed to replace conventional SiO_2 gate dielectric. Strain techniques, new materials (Ge or III-V) and alternative substrate orientations offer enhanced carrier mobility and drain current without resulting in parasitic effects. Also, novel architectures have been introduced such as ultra-thin body and buried insulator (UTBB) SOI and multi-gate MOSFETs to obtain good gate control of SCEs.

1.4.1. High-K/Metal gate stack

When the SiO_2 used as gate insulator reaches its physical limit thickness (~ 1 nm), gate leakage current due to the quantum mechanical tunneling causes serious problems, increasing power consumption and degrading device reliability [25]. Therefore, replacement of the gate insulator from conventional SiO_2 to higher permittivity (high-k) dielectric material (Al_2O_3, La_2O_3, ZrO_2 and HfO_2) is essential and unavoidable [26-28]. By adopting high-k material, the physical thickness of gate insulator can be increased while electrical thickness is maintained. According to quantum mechanics, the tunneling probability exponentially decreases as the barrier thickness increases [29]. Thereby, gate leakage can be reduced without degradation of gate control.

However, dipoles in the high-k dielectric vibrate and generate vibration in the lattice of Si channel [29]. Thus, phonon scattering at its surface is large, becoming source of mobility degradation. To avoid this mobility reduction, an integrated combination of SiO_2 and high-k material has been proposed. Very thin SiO_2 layer located between Si body and high-k dielectric layer reduces carrier mobility deterioration [30].

In parallel, many researches have been performed to use metal gates. In metal gate electrode, the sheet resistance lowering problem is improved. The dipole vibration in high-k dielectric is also screened due to the significant increase of electrons. Metal electrode also allows an opportunity for modulating the threshold voltage of MOSFETs according to the work function engineering.

For these reasons, Intel has been using hafnium based gate insulator from 45 nm technology node [31]. Comparing to 65 nm node SiO_2/poly-Si stack, the gate leakage of 45 nm node was reduced 25 times in NMOS and 1000 times in PMOS.

1.4.2. Strain technology

Strain engineering is a key method to increase the carrier mobility and driving current. There are two approaches to obtain strain in the conducting channel of a MOSFET: strained substrate and process-induced strain.

(a) Strained substrate

The concept of this technology is to obtain a compressive/tensile strained substrate by growing a thin film with larger/smaller lattice constant, e.g. $Si_{1-x}Ge_x$/Si, on a substrate with smaller/larger lattice constant, e.g. Si/ $Si_{1-x}Ge_x$.

(i) Strained-SOI (SSOI) substrate: The strained-Si layer is obtained by epitaxial grown Si films on relaxed SiGe virtual substrates as shown in Fig. 1-8b. After smart-cut process, only the strained Si film subsists on the BOX. Enhanced electron and hole mobility are achieved [32].

(ii) SiGe-on-insulator (SGOI) substrate: Thin $Si_{1-x}Ge_x$ film layer can be obtained by the condensation technique (Fig. 1-8a) [32, 33]. Improved hole mobility is obtained while electron mobility is degraded with increasing Ge concentration. A strained-Si/SiGe dual channel architectures has been proposed by Lee at al [34] for both electron and hole mobility enhancement.

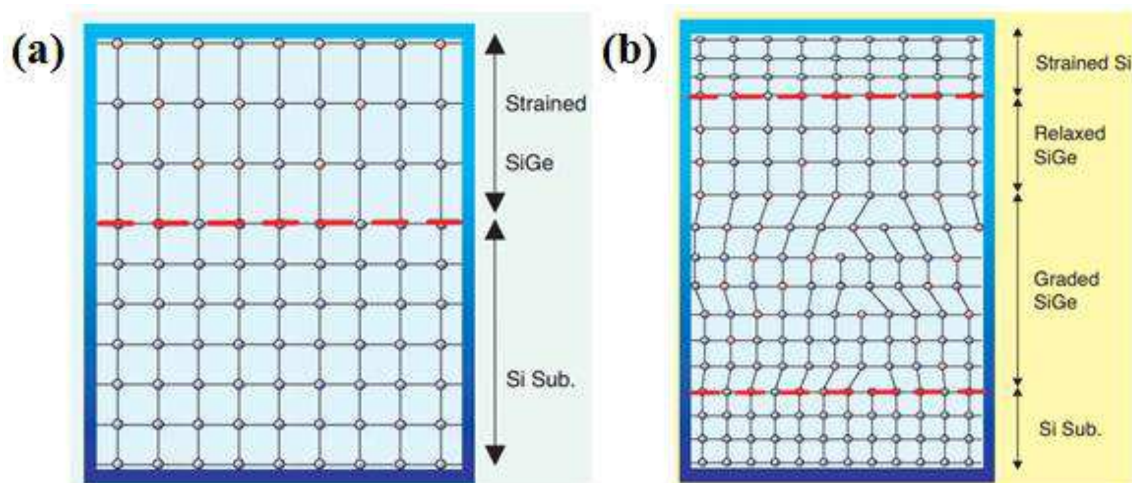

Fig. 1-8: Typical substrate strain technology [32]. A schematic diagram of lattice arrangement of (a) strained $Si_{1-x}Ge_x$ grown on Si and (b) strained Si layer on the virtual $Si_{1-x}Ge_x$ substrate.

(b) Process-induced strain

Process-induced strain is simple and low cost as an existing process can be used, offering a similar carrier mobility enhancement, as the strained substrate technology [35].

(i) Normally, silicon nitride film is deposited on a transistor for the contact-etch stop layer (CESL). This layer produces a high level of local stress. While tensile strain offers modest electron mobility enhancement, compressive strain provides outstanding hole mobility [36].

(ii) Selective epitaxial SiGe layer deposited for raised source/drain structure compresses the Si channel and improves hole mobility. Higher strain and hole mobility are achieved with increasing Ge concentration [37]. SiC source and drain can be used for N-channels.

1.4.3. Planar fully-depleted (FD) SOI transistor

As mentioned earlier, the planar FD SOI MOSFET is a good candidate for future nanoscale CMOS. FD planar MOSFETs have been fabricated on SOI wafer using UNIBOND or Smart-Cut^{TM} technology. Unlike for the bulk technology, channel doping and pocket implantation are not essential in SOI transistor. Instead, thin Si film and thin BOX are required in order to reduce SCEs. SiO_2/high-k (normally SiO_2/HfO_2) dielectric architecture processed by atomic layer chemical vapor deposition (ALCVD) or plasma enhanced

chemical vapor deposition (PECVD) is employed for good gate control and high mobility. Gate stack is completed by atomic layer deposition (ALD) for metal gate formation. A silicon-nitride spacer is then formed to protect the metal gate and isolate the gate stack from the subsequent formation of raised source/drain (S/D). A selective epitaxial growth is used for optimization of the S/D architecture and reduction of series resistance.

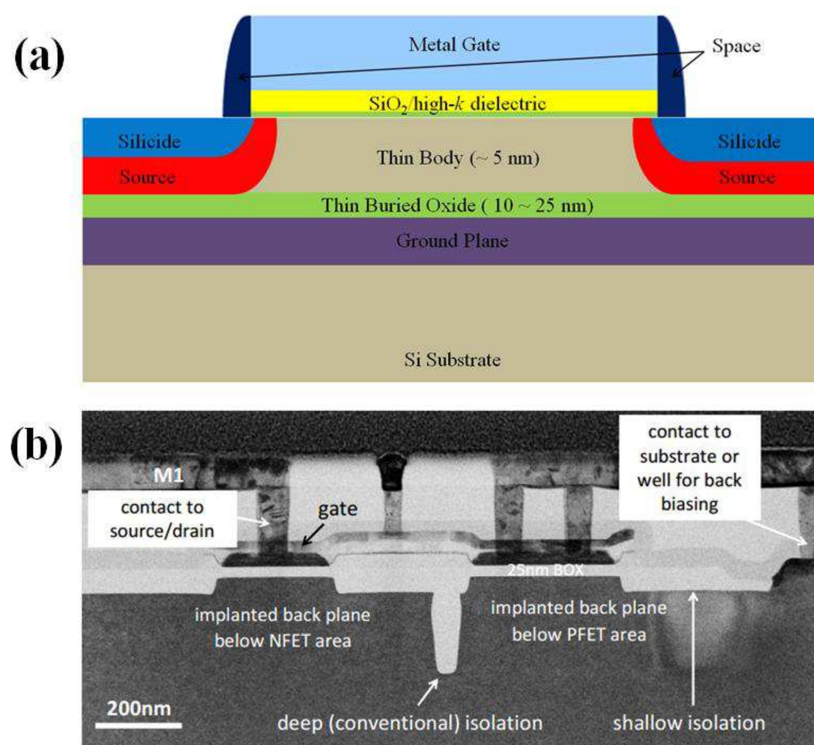

Fig. 1-9: State-of-the-art planar FD SOI MOSFETs. (a) Cross-section and (b) TEM image of advanced FD SOI device [38].

To reduce SCEs, tilted LDD implantation can be carried out prior to spacer formation and S/D implantation. Stressed-SiN CESL can also be stacked by CVD on top of the device to boost the device performance. High doped layer (ground plane) under BOX offers an opportunity to regulate front-channel properties and control SCEs. Fig. 1-9 shows the cross-section and TEM image of an advanced FD SOI transistor fabricated with state-of-the-art technology.

1.4.4. 3-Dimensional fully-depleted (FD) SOI transistor

Novel transistor architectures, particularly multi-gate structure, have been proposed [39] in order to achieve simultaneously high-channel performance and integration density.

Among them, planar double-gate (DG) MOSFET shown in Fig. 1-10a offers superior performance in terms of subthreshold swing and SCEs [39]. Four-gate architecture (Fig. 1-10b) exhibits enhanced functionality by independently biasing the four gates and immunity to radiations SCEs (Fig. 1-10b) [40]. However, the industrial development of these types of structures faces problems of misalignment between the gates and lower integration density than in vertical devices. Recently, junctionless transistor (JLT) has been attracting attention due to its simple fabrication process (Fig. 1-10c) [41, 42]. JLT requires high doping of the entire transistor. That causes carrier mobility degradation and requires to pay much attention to uniform doping of whole wafer, leading technological issues for industrial application [43].

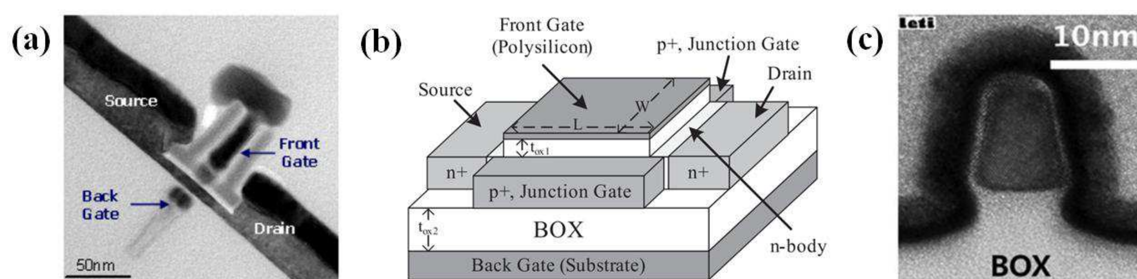

Fig. 1-10: 3-dimensional transistor architectures based on SOI technology. (a) Planar double-gate MOSFET [39], (b) four-gate MOSFET [40] and (c) junctionless transistor [41].

To the end, FinFET architecture is the most promising candidate for the next generation transistor. In FinFETs, the three sides (one top and two lateral) of silicon body are surrounded by the front-gate. The two lateral-gates are perfectly self-aligned and their enhanced control of the channel allows further scale down the gate length. A third channel at the top of the fin accentuates the gate control. FinFET can be fabricated not only on bulk wafer (bulk FinFET) but also on SOI substrate (SOI FinFET).

Bulk FinFETs are divided as junction-isolated or material-isolated according to the transistor isolation technique [44]. In junction-isolated FinFETs (the bottom of Fig. 1-11b), the etching of the fin is followed by an oxide deposition which should fill high aspect ratio trench without defects. Careful polishing and recess etching are then fulfilled to determine fin height. The field oxide provides isolation among the sidewalls of each fin. However, the transistors are still connected underneath the oxide. Therefore, a high dose angled implant at the bottom of the fin should be performed to create dopant junction and complete the isolation. On the other hand, the material-isolated FinFET is accomplished by the local oxidation which substitutes the high dopant implantation of the junction-isolated FinFETs.

Material-isolated technique demands more complicated and precise process steps.

By contrast, the SOI FinFET can more easily be fabricated. The BOX acts as etch stop layer and provides perfect isolation. Therefore, no additional isolation steps are required. The fin height is definitely defined by the silicon film thickness. As for planar SOI devices, the bottom interface of the body is contacted with the buried insulator and the back-channel can be activated by the back-gate biasing.

Except for the fin formation, FinFETs can basically be fabricated according to the conventional CMOS fabrication process. As we can see in Fig. 1-11a, the state-of-the-art CMOS fabrication technology, described in the previous section (1.4.3), can be adopted for FinFET processing.

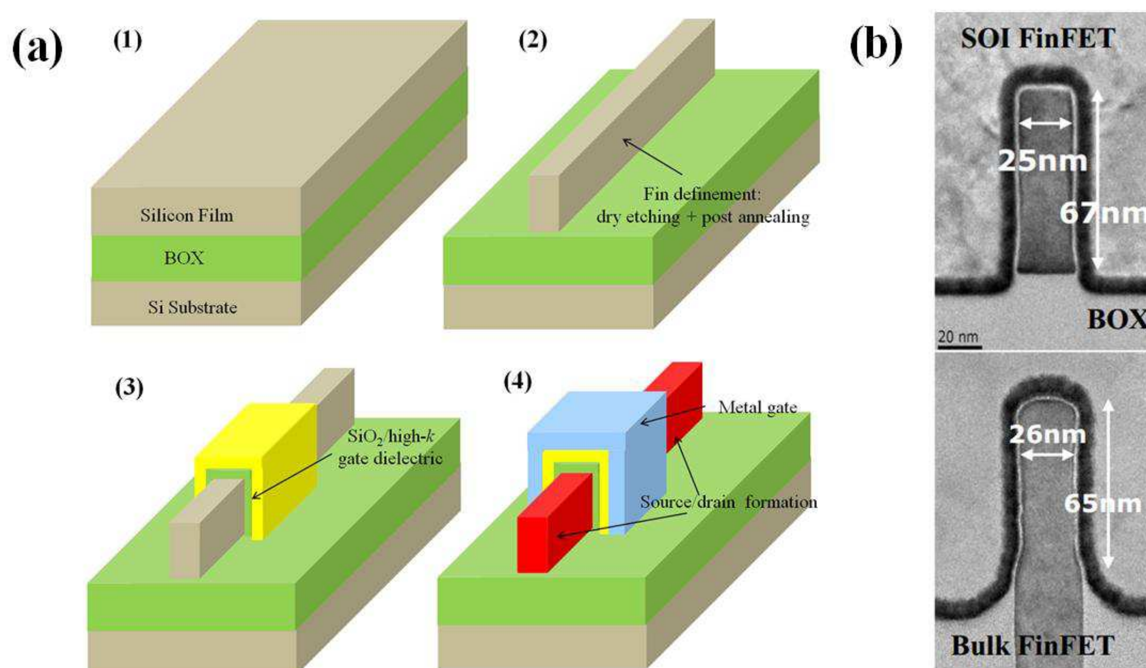

Fig. 1-11: (a) SOI FinFET fabrication flow: (1) SOI wafer is used as starting material. (2) Fin definition by dry etching and post-annealing to smooth fin side wall and reduce defects. (3) Gate insulator (SiO_2/high-*k*) deposition. (4) Gate metal deposition and source/drain formation. (b) TEM images of SOI and junction-isolated bulk FinFETs

1.5. Conclusion

The aim of this chapter was to review recent trend and related issues of Si-based MOSFETs. The device scaling down, the most critical issue, causes undesired effects: short-channel effects and performance limitation. In order to attenuate short-channel effects and acquire high-performance, several technical approaches have been proposed such as high-

k/metal gate architecture and strained-Si technology. In parallel, SOI technology was also introduced. Compared with bulk-Si technology, fully-depleted SOI offers higher performance, better scaling capability and diverse architecture thanks to its unique features. Novel device architectures have been studied based on SOI technology. FD SOI Planar MOSFETs and FinFETs are very promising candidates for beyond 22 nm technology node due to their benefits: (i) thin body and BOX; strong immunity to SCEs, (ii) undoped body; high carrier mobility, (iii) back-gate biasing; front-channel property modulation and (iv) FinFETs with excellent gate control. These advantages will be further investigated, based on our detailed measurements, in the following chapters.

Chapter 2:

Advanced Devices and Typical Effects

In this chapter, we present characterization and modeling results for three families of devices: planar FD SOI, FinFETs with double and triple-gate, and ZnO TFTs. We will focus on the intergate couling, transport and short-channel mechanisms.

2.1. Typical Properties in FD SOI MOSFETs

2.1.1. Introduction

SOI technology and its advantages were briefly introduced in the previous chapter. Very good gate control and high performance are obtained with the thin Si film and BOX. The typical properties of state-of-the-art MOSFET will be reported in this section by comparing our experimental results with theoretical models.

The structure of the planar devices fabricated at LETI and STMicroelectronics is shown in Fig. 2-1. The thickness of the buried insulator is T_{BOX} = 25 nm. Devices with different Si film thicknesses T_{si} (5 nm, 7 nm and 10 nm) and gate lengths L_G down to 30 nm were prepared to investigate the effect of the silicon film thickness on SCEs, mobility and coupling. SiO_2 and HfO_2 layers were deposited for front-gate insulators. The effective oxide thickness (EOT) was determined to be T_{EOT} = 1.6 nm. A ground plane (GP) was formed below the BOX in order to modulate the front-channel properties by GP bias. All devices have metal gate, undoped body and operate in fully-depleted mode. There is a protection diode between GP and front-gate. The turn-on voltage of this diode is around 0.8 V which prevents the application of higher bias.

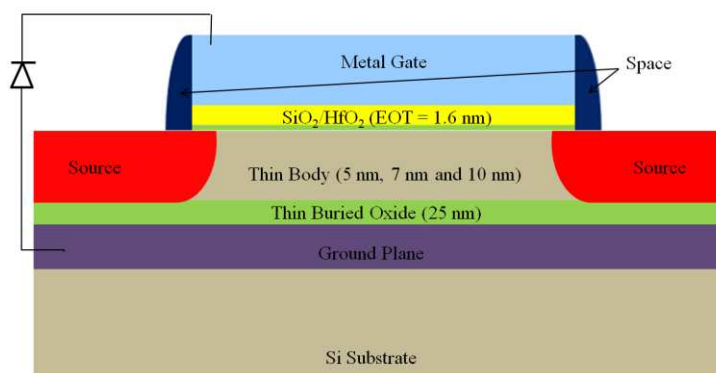

Fig. 2-1: Cross-section of the ultra-thin film SOI MOSFETs studied in Chapter 2.1.

2.1.2. Parameter extraction techniques and typical properties

Most of our measurements were performed at wafer level using a cryostat prober, connected HP 4155A semiconductor analyzer. The extracted electrical parameters (threshold voltage, carrier mobility, subthreshold swing and so on) from the experimental results reveal device performance. However, due to the device scaling down, undesired effects are generated and involved in the parameter extraction. In order to eliminate parasitic effects and find out precise device properties, several parameter extraction techniques have been evaluated [45-48].

(a) Linear extrapolation method

The first order approximation of the drain current in strong inversion and ohmic regime (at low drain bias) is expressed as:

$$I_D = \mu_{eff} C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \tag{2.1}$$

where I_D is drain current, W and L are gate width and length, C_{ox} is gate capacitance, V_D and V_G are drain and gate bias and V_{TH} is threshold voltage.

The effective mobility μ_{eff} in strong inversion regime is defined as:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_G - V_{TH})} \tag{2.2}$$

where μ_0 is the low-field mobility and θ is the mobility degradation factor at high vertical field. At a constant V_D, based on Eq. (2.1), the drain current variation with V_G is sub-linear because the effective mobility is degraded at high electric field.

The transconductance is defined as the derivative of Eq. (2.1) with respect to V_G:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} C_{ox} \frac{\mu_0}{[1 + \theta(V_G - V_{TH})]^2} V_D \tag{2.3}$$

The linear extrapolation method is very simple for the extraction of the threshold voltage, using a straight line fit to the drain curve as shown in Fig. 2-2. The intercept point with X-axis indicates the threshold voltage. The slope of the line yields the mobility. However, this method is sensitive to the mobility degradation and series resistance.

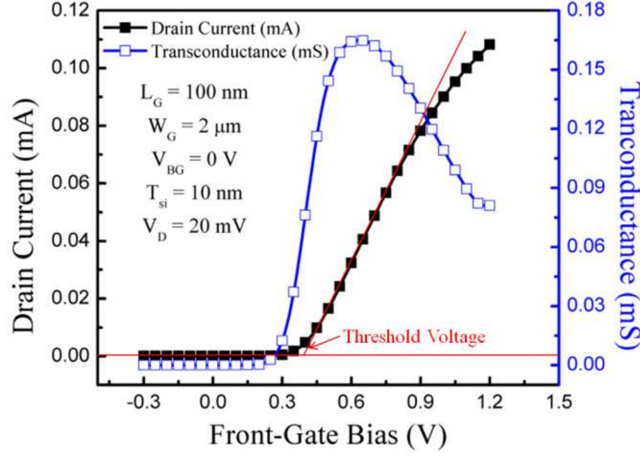

Fig. 2-2: Experimental drain current and transconductance curves as a function of front-gate bias showing the linear extrapolation method for threshold voltage. N-channel SOI MOSFET with L_G = 100 nm and T_{si} = 10 nm.

(b) Transconductance method

The *field-effect* mobility μ_{FE}, can be determined from the transconductance, defined by Eq. (2.3) [45]:

$$g_m = \frac{W}{L}\mu_{FE} C_{ox} V_D \tag{2.4}$$

The maximum *field-effect* mobility becomes:

$$\mu_{FE,\max} = \frac{L g_{m,\max}}{W C_{ox} V_D} \tag{2.5}$$

The *field-effect* mobility is strongly affected by θ factor and does not have physical meaning but is useful for circuit design.

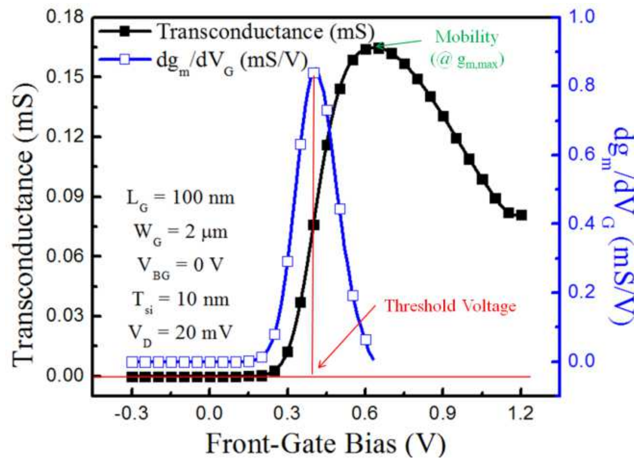

Fig. 2-3: Experimental transconductance and second derivative of drain current as a function of front-gate bias showing the extraction of *field-effect* mobility and threshold voltage.

Threshold voltage can be determined from the second derivative of current ($d^2I_D/d^2V_G = dg_m/dV_G$) at low drain voltage [45]. As we can see in Fig. 2-3, the gate voltage at the maximum value of the second derivative curve yields the threshold voltage. The maximum point is related to the threshold band-bending at $\phi_s = 2\phi_F$. This method is not affected by series resistance and mobility degradation.

(c) Y-function method

Y-function technique was proposed by Ghibaudo [46]. This method eliminates the mobility degradation factor θ by dividing the current I_D with $\sqrt{g_m}$, as defined by Eqs. (2.2) and (2.3):

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{ox} V_D \mu_0} (V_G - V_{TH}) \qquad (2.6)$$

Eq. (2.6) is linear as a function of V_G. The low-field mobility is extracted from the slope of the Y-function, whereas the intercept point with X-axis represents the threshold voltage as shown in Fig. 2-4.

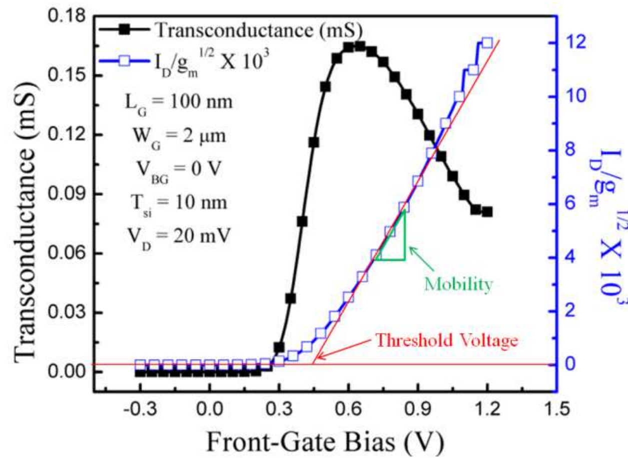

Fig. 2-4: Experimental transconductance and Y-function curves versus front-gate bias showing Y-function parameter extraction method.

The mobility degradation factor θ can be calculated from Eq. (2.1):

$$\theta = \frac{\mu_0 C_{ox} W V_D}{I_D L (V_G - V_{TH})} - \frac{1}{V_G - V_{TH}} \qquad (2.7)$$

This well known method efficiently removes the impact of series resistance. However, the effect of surface roughness at high field is emphasized in advanced MOSFETs. A second

attenuation factor θ_2 needs to be included in the current equation. Therefore, $Y(V_G)$ curve may become super-linear like in Fig. 2-4.

(d) McLarty method

In this parameter extraction method [47], drain current is expressed as [49, 50]:

$$I_D = \frac{W}{L} C_{ox}\mu_0 \frac{(V_G - V_{TH})V_D}{1+\theta_1(V_G - V_{TH}) + \theta_2(V_G - V_{TH})^2} \quad (2.8)$$

where θ_1 and θ_2 are the mobility degradation factors related to series resistance and surface roughness scattering.

Inverting Eq. (2.8) and taking the first and second derivatives results in the following two equations:

$$\frac{\partial}{\partial V_G}\left(\frac{1}{I_D}\right) = \frac{1}{A}\left(\theta_2 - \frac{1}{(V_G - V_{TH})^2}\right) \quad (2.9)$$

and

$$\frac{\partial^2}{\partial V_G{}^2}\left(\frac{1}{I_D}\right) = \frac{1}{A}\frac{2}{(V_G - V_{TH})^3} \quad (2.10)$$

where $A = C_{ox}\mu_0 V_D W/L$.

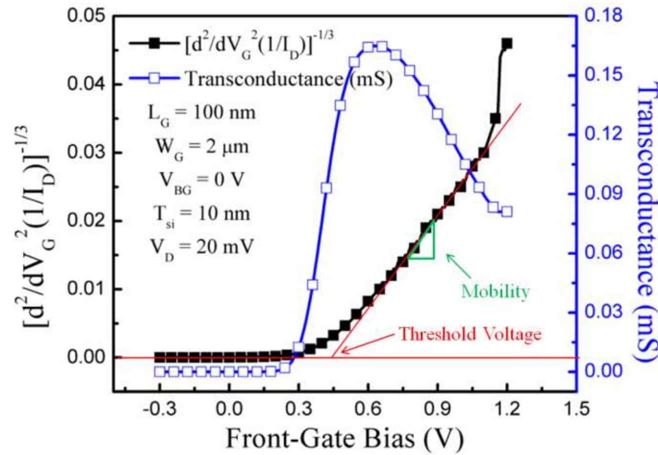

Fig. 2-5: Linear line from Eq. (2.11) and transconductance as a function of front-gate bias showing threshold voltage and carrier mobility extraction by McLarty method.

Threshold voltage and mobility can be obtained by plotting the following function versus V_G:

$$\left(\frac{\partial^2}{\partial V_G^{\ 2}} \left(\frac{1}{I_D} \right) \right)^{-1/3} = \left(\frac{2}{A} \right)^{-1/3} (V_G - V_{TH}) \tag{2.11}$$

In Fig. 2-5, threshold voltage is the intercept point with X-axis and the linear line (Eq. (2.11)) and mobility is calculated from the slope of the linear line. According to the second derivation of $1/I_D$, this method allows erasing the effect of series resistance θ_1 and surface roughness θ_2.

(e) Split C-V method

The mobile channel charge density measurement technique is named as the split C-V technique. The capacitance C_{GC} is measured between the gate and source-drain. This method was introduced by Koomen *et al.* [51] for the interface trap charge density and the substrate doping measurement. It was adapted to carrier mobility measurement [48] and to SOI.

As illustrated in Fig. 2-6, C_{GC} measurement is carried out using LCR meter. A small a.c. signal is applied at the gate electrode using the high cable. The source and drain are linked together and connected to the low-cable of the LCR meter. The substrate is grounded.

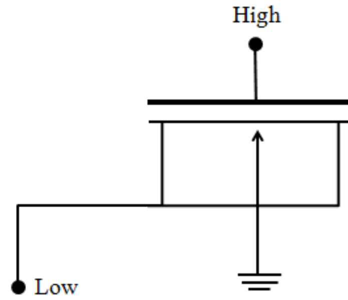

Fig. 2-6: Split C-V measurement arrangement.

From the capacitor measurement, the inversion charge Q_i is calculated by integration:

$$Q_i(V_G) = \int_{V_{G,acc}}^{V_G} C_{GC}(V)dV \tag{2.12}$$

In order to obtain the effective mobility, Eq. (2.12) should be combined with the drain current measurement:

$$\mu_{eff} = \frac{LI_D}{WV_D Q_i} \tag{2.13}$$

The effective mobility extracted by split C-V method depends on lattice scattering,

surface scattering and ionized impurity scattering. In our work, we mainly used the Y-function and replaced the split-CV with the magnetoresistance method developed in chapter 3.

Electrical characteristics were investigated in ultra-thin body (T_{Si} = 10 nm) SOI MOSFETs. In Fig. 2-7, $I_D(V_{FG})$ curves were measured for different gate lengths. In long channel device (L_G = 1 µm), excellent subthreshold swing (SS = 64 mV/dec) and high ON/OFF ratio (> 10^8) were achieved, reflecting good gate control and interface quality. Reasonable threshold voltage (V_{THF} = 0.52 V) and high mobility (330 cm^2/Vs) were also extracted by Y-function method [46]. Gate length dependence of extracted parameters is shown in Fig. 2-8.

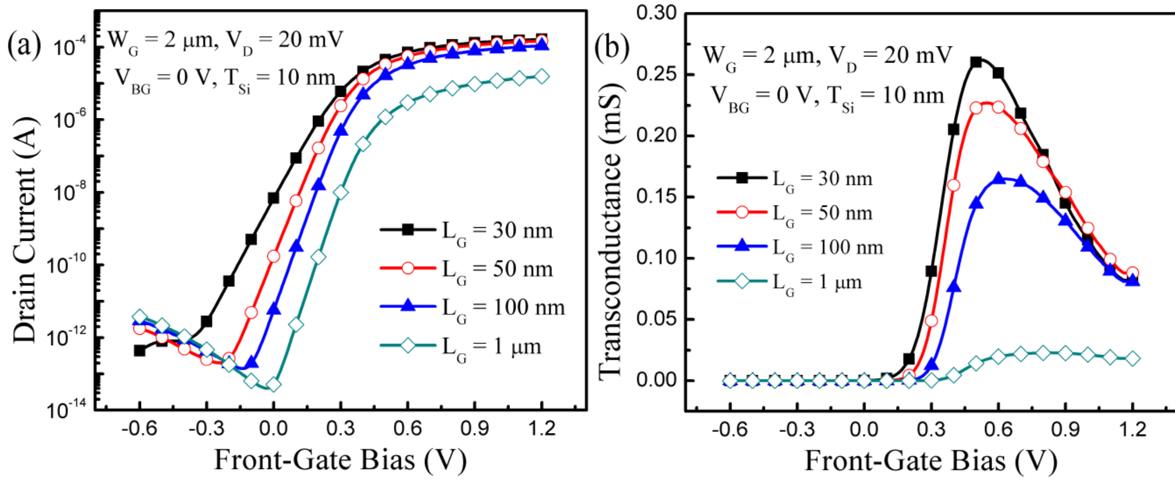

Fig. 2-7: Typical channel effects of ultra-thin body SOI MOSFETs. (a) Drain current and (b) transconductance curves as a function of front-gate bias for various gate lengths.

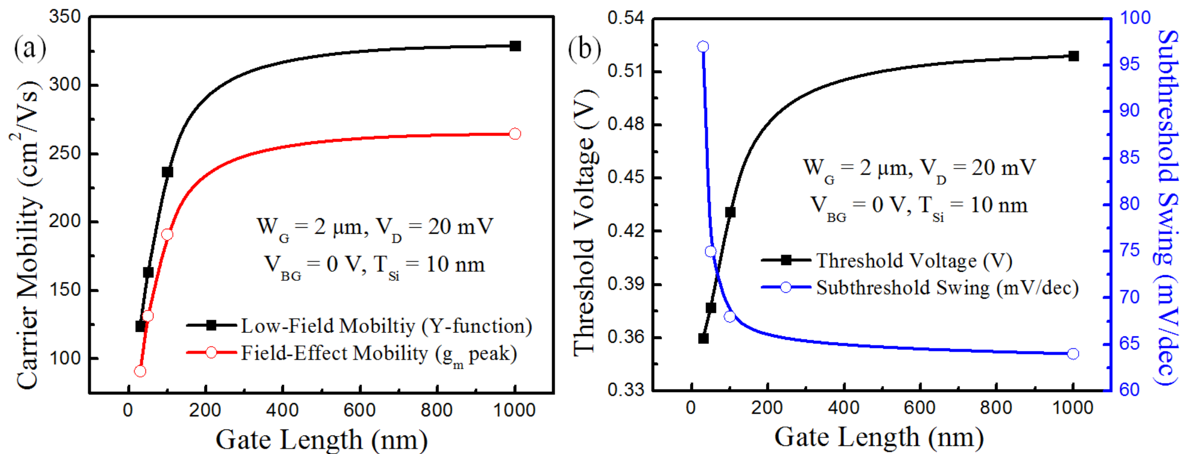

Fig. 2-8: Gate length dependence in ultra-thin body SOI MOSFETs. (a) Low-field mobility (extracted by Y-function), *field-effect* mobility (from g_m peak value), (b) threshold voltage (extracted by Y-function) and subthreshold swing as a function of gate length.

Ordinary short-channel effects were obtained. In short device, carrier mobility

decreases presumably due to the process-induced neutral defects [36]. The maximum *field-effect* mobility extracted from g_m peak value includes series resistance effect and is lower than the low-field mobility extracted by Y-function. However, their variation trend with channel length is identical. Threshold voltage (extracted by Y-function) roll-off and subthreshold swing (given by the Log $I_D(V_{FG})$ curves in subthreshold regime) were degraded by the charge sharing effect [19] in shorter devices.

2.1.3. Si film and BOX thickness effects

As described in Chapter 1, SCEs are the main sources of device performance degradation. The SCEs directly depend on the S/D junction depth as well as the depletion region extending into the substrate. Unlike for bulk-technology, in SOI devices, the SCEs can be effectively controlled by the reduction of silicon film and BOX thickness.

(a) Effect of buried oxide thickness

In long channel device with thick BOX (T_{BOX} = 100 nm ~ 200 nm), the transverse electric field in the BOX is overwhelmed by the fringing field from the source/drain (Fig. 2-9a) [52]. This field induces an increase of the potential at the Si/BOX interface and, by coupling, a drop of threshold voltage [53]. This phenomenon, named drain-induced vertical substrate biasing (DIVSB), leads a loss of gate control and accentuates the DIBL effect in short devices.

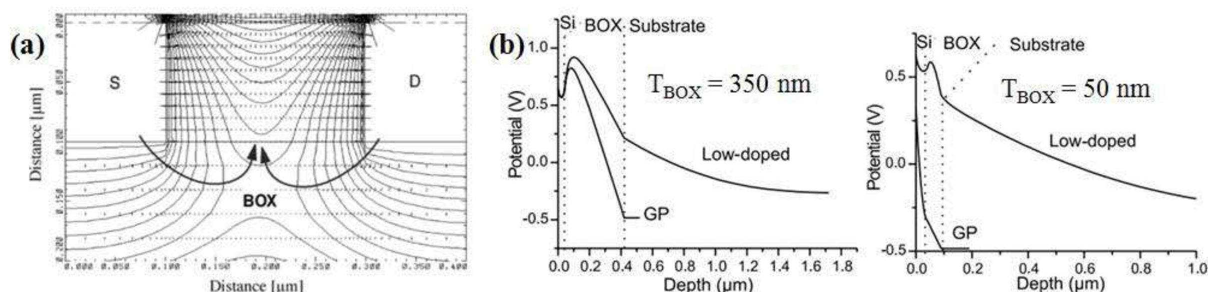

Fig. 2-9: (a) Numerical simulated equipotential contours and electric-field vectors showing the fringing field in the BOX of an L_G = 0.2 µm FD SOI MOSFETs: T_{si} = 100 nm, T_{BOX} = 350 nm and V_D = 50 mV. [52] (b) Vertical potential profile with conventional and GP configuration in thick (T_{BOX} = 350 nm) and thin (T_{BOX} = 50 nm) BOX; T_{si} = 20 nm [54].

In 2002, Ernst *et al*. discovered, analyzed and modeled the DIVSB [54]. The direct way to inhibit the fringing field effect is to thin down the BOX and use a ground plane (GP): the

potential peak is attenuated by GP and this advantage is remarkably enhanced in a thinner BOX (Fig. 2-9b). For nanoscale CMOS beyond the 22 nm node, $T_{BOX} < 25$ nm is required for good control of SCEs [55, 56]. Such BOX thinning has recently been realized in SOI wafer technology [57]. This BOX combined with GP more successfully restrains the depletion region extension down to the BOX. [8, 54]

(b) Effect of silicon film thickness

Thin film is the main condition to control SCEs in SOI device. There are very few publications so far on MOSFETs with 5 nm film thickness [8, 57]. In Fig. 2-10, the electric field in the body of the FD SOI device is governed by the silicon film thickness [58]. The potential lines are more flat in 5 nm thick body showing enhanced gate electrostatic control compared to the 25 nm thick body. An ultra-thin film physically confines the depletion region and S/D junctions depth. For excellent control of SCEs, the film thickness should be about 25 % of the channel length.

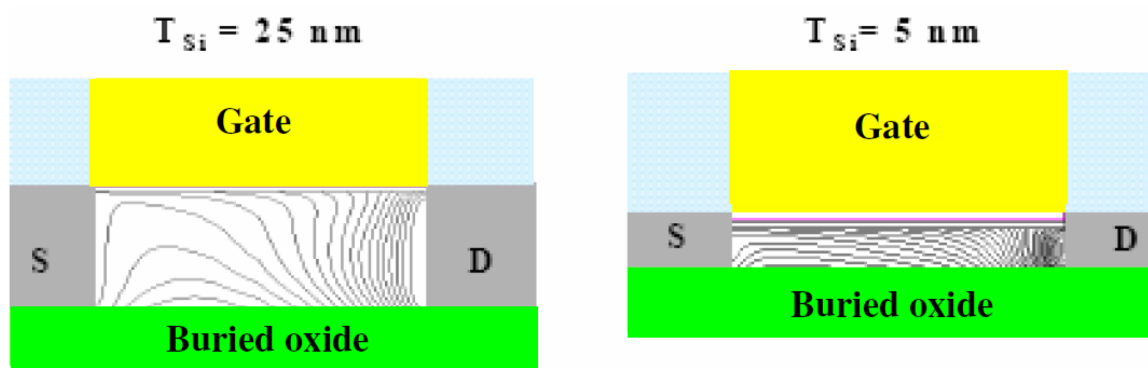

Fig. 2-10: Simulation of body potential for 25 nm and 5 nm thick SOI film at $V_G = V_D = 1$ V [58].

We have investigated the impact of silicon film thickness on the device performance. Fig. 2-11 shows good drain current behavior for various Si film thicknesses (5 nm, 7 nm and 10 nm) in short-length (L_G = 30 nm) FD SOI MOSFETs. Better subthreshold swing is obtained in thinner devices (Fig. 2-11a). On the other hand, the transconductance peak value is reduced in thinner film, suggesting mobility degradation (Fig. 2-11b) or series resistance increases.

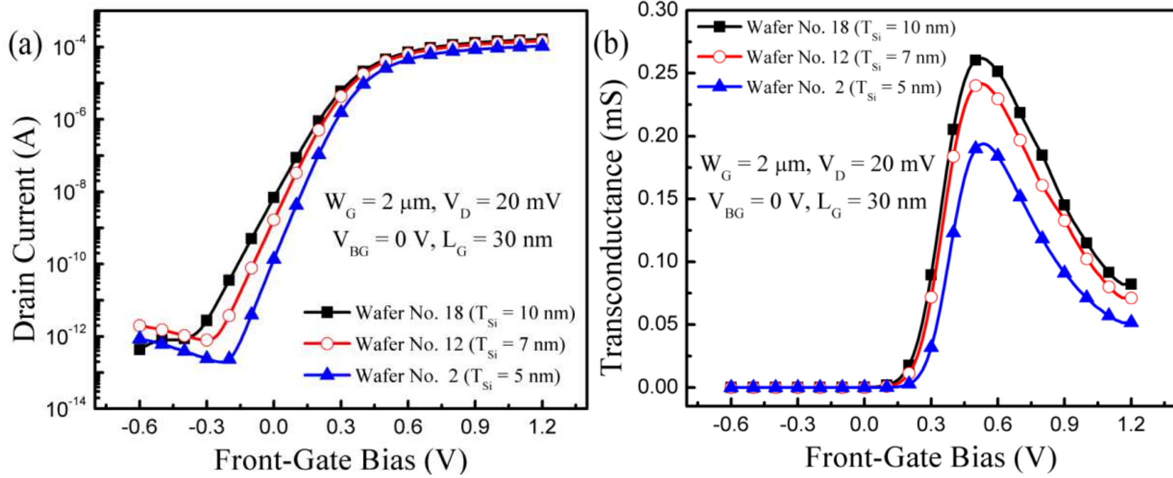

Fig. 2-11: Silicon film thickness dependence. (a) Drain current and (b) transconductance curves versus front-gate bias at different silicon film thickness device.

In order to compare the effect of Si film thickness on device performance and immunity to SCEs, the carrier mobility, threshold voltage and subthreshold swing were extracted for a range of gate length and thickness (Fig. 2-12). In thinner device, carrier mobility is lower by about 15 %. Note that the *field-effect* mobility shows the same tendency. In ultra-thin films, the inversion layer expends on the whole thickness of the silicon film (volume inversion) and carrier mobility is limited by phonon confinement and scattering [59]. This can explain the carrier mobility lowering. However, other reports have shown that the carrier mobility in long MOSFETs with optimized source and drain is constant in the thickness range 4-10 nm [60]. In our short channel devices, the mobility may decrease due to the defects induced by the implantation of source and drain and also by the occurring of semiballistic transport.

The threshold voltage dependence on film thickness (Fig. 2-12b) comes from quantum mechanical effects. In thinner film, quantum confinement leads to band splitting, raising the conduction band level. [61, 62]. Therefore, more energy for band-bending is necessary to get a desired inversion charge density. As a result, threshold voltage is increased with decreasing body thickness.

The degradation of the subthreshold swing in short channel (Fig. 2-12c) is much less in 5 nm film due to better gate control. When silicon film thickness reduces from 10 nm to 5 nm, the subthreshold swing is very close to the theoretical limit of 60 mV/dec that is achievable only in (perfect) FD transistors.

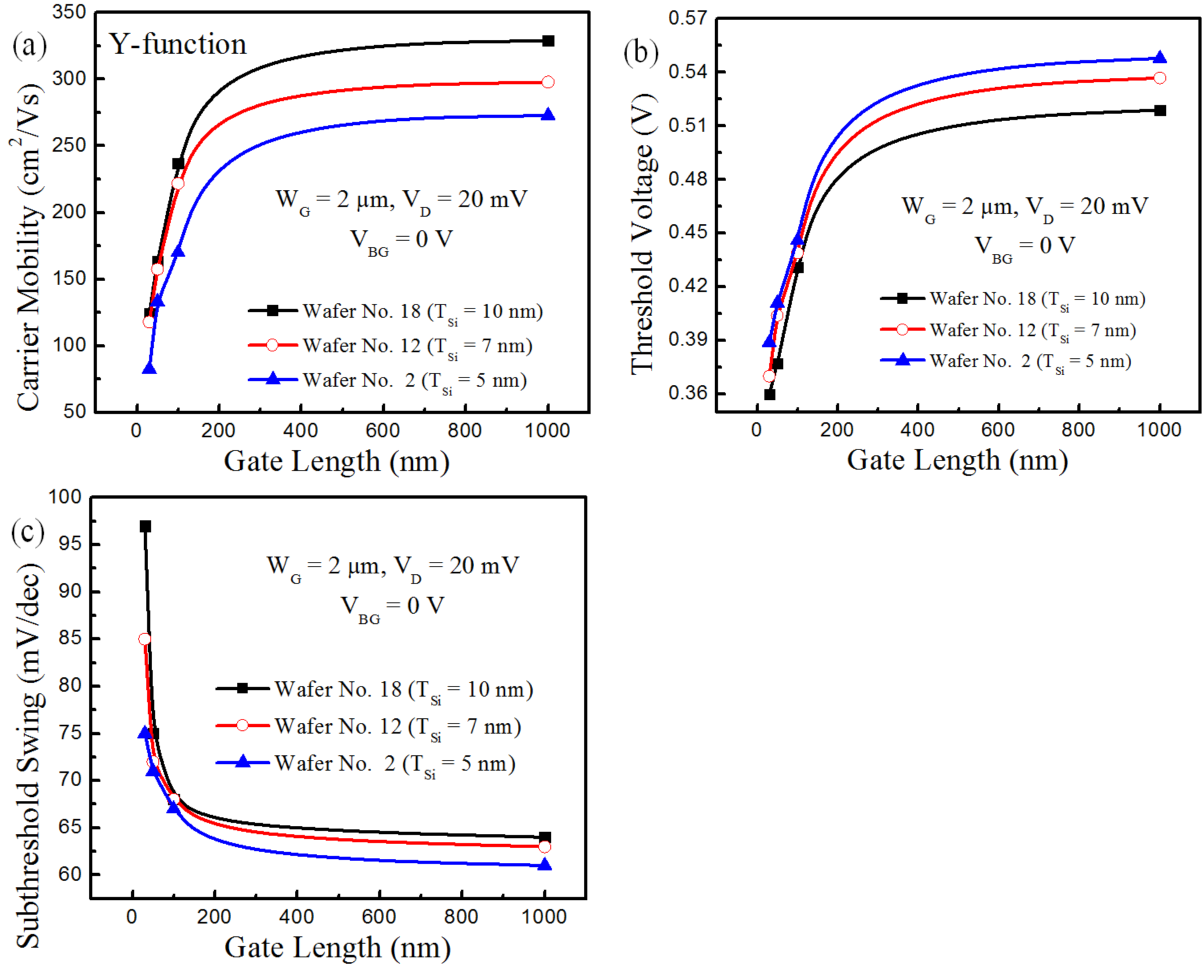

Fig. 2-12: Impact of silicon film thickness on device characteristics. (a) Carrier mobility, (b) threshold voltage and (c) subthreshold swing as a function of gate length for various thickness devices. Carrier mobility and threshold voltage were extracted by Y-function technique.

2.1.4. Coupling effect

Compared with bulk technology, there is a very particular but typical phenomenon in FD SOI devices, named "interface coupling". The back-gate bias can shift the front-gate threshold voltage and vice versa [4, 63]. Coupling effect reduces the sensitivity of threshold voltage to the thin silicon film [64] and is applicable to dynamic threshold voltage modulation [65, 66] to reduce power consumption: high V_{TH} in off state (smaller leakage current) and low V_{TH} in on state (increased drive current).

In conventional n-channel MOSFETs on bulk Si, threshold voltage V_{TH} is generally expressed as [67] :

$$V_{TH} = V_{FB} + 2\phi_B + \frac{Q_b(N_B)}{C_{ox}} \tag{2.14}$$

where V_{FB} is the flat-band voltage governed by the gate-body work function Φ_M difference, ϕ_B and Q_b (dependent on the doping density N_B) are the Fermi potential and the body depletion charge density at the threshold condition and C_{ox} defined as ε_{ox}/t_{ox} is the gate-oxide capacitance per unit area.

To examine the charge coupling, we first describe the depletion approximation for intrinsic-UTB device. Oxide and interface charges are neglected and, for the sake of clarity, symmetrical DG (SDG) nMOSFET is considered as shown in Fig. 2-13. According to the Gauss's law, in weak inversion regime, front-gate bias V_{FG} of an SDG nMOSFET is expressed as:

$$V_{FG} - \Phi_M = \phi_{sf} - \frac{Q_b + Q_i}{2C_{oxf}} \tag{2.15}$$

where ϕ_{sf} is the front-surface potential, C_{oxf} is front-gate oxide capacitance ($=\varepsilon_{ox}/T_{oxf}$), Q_b is the depletion charge density ($=-qt_{si}N_B$) defined by the film theickness, Q_i is the inversion-charge density and the factor 2 in the last term comes from the symmetry of the SDG device. When the body is intrinsic, $|Q_b| >> |Q_i|$ is clearly invalid. However, $|Q_i|/C_{oxf} << |\phi_{sf}|$ since typically $|Q_i| < q10^{11}$ C/cm^2 for subthreshold conditions. Therefore, the influence of subthreshold (or weak-inversion) charge density on ϕ_{sf} in Eq. (2.15) can be neglected irrespective of N_B. Finally, the charge-sheet approximation is unnecessary for subthreshold analysis.

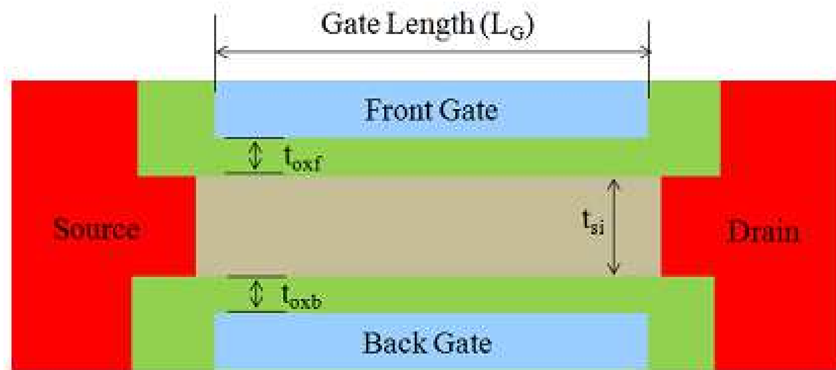

Fig. 2-13: Schematic of the symmetrical double-gate (SDG).

In weakly inverted intrinsic UTB device (N_B = 0), gate-to-gate coupling is well documented. The well known model of Lim and Fossum [14] was derived from depletion approximation and by solving the Poisson equation with Gauss's law.

$$V_{FG} - V_{FBf} = \left(1 + \frac{C_b}{C_{oxf}}\right)\phi_{sf} - \frac{C_b}{C_{oxf}}\phi_{sb}, \tag{2.16}$$

$$V_{BG} - V_{FBb} = \left(1 + \frac{C_b}{C_{oxb}}\right)\phi_{sb} - \frac{C_b}{C_{oxb}}\phi_{sf} \tag{2.17}$$

where ϕ_{sb} is the back-surface potential and C_b is the capacitance of the body ($=\varepsilon_{si}/T_{si}$): the subscripts f and b refer to front and back gates.

From Eqs. (2.16), (2.17) and $\phi_{sf} = 2\phi_B$ (for the nMOSFET), the front-channel threshold voltage (V_{THF}) when the back-surface lies in depletion regime is expressed as:

$$V_{THF} = V_{FBF} + \alpha V_{FBB} + (1+\alpha)2\phi_B - \alpha V_{BG} \tag{2.18}$$

where

$$\alpha = \frac{C_{oxb}C_b}{C_{oxf}(C_{oxb} + C_b)} \tag{2.19}$$

α is front-channel coupling coefficient. Therefore, V_{TH} depends on the front- and back-gate biases (V_{FG}, V_{BG}), flat-band voltages (V_{FBF}, V_{FBB}), oxide thicknesses (T_{oxf}, T_{oxb}) and silicon film thickness (T_{si}). Notice that when the back-surface is accumulated or inverted, free carriers efficiently block the vertical electric field induced by V_{BG}, pinning ϕ_{sb} and V_{THF} is independent of V_{BG}. In Fig. 2-14, $V_{THF}(V_{BG})$ is qualitatively shown, where V_{BG}^A and V_{BG}^I are the back-surface accumulation and inversion onset voltages, derived from Eq. (2.17), with $\phi_{sf} = 2\phi_B$ and $\phi_{sb} = 0$ or $\phi_{sb} = 2\phi_B$.

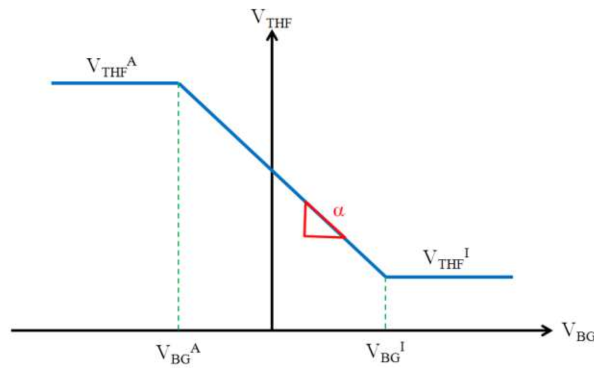

Fig. 2-14: Front-channel threshold voltage versus back-gate bias in SOI nMOSFET [67]. When the back-surface is depleted, $V_{THF}(V_{BG})$ varies linearly with slope α (Eq. (2.19)).

We have explored the coupling effect in our ultra-thin film MOSFETs. In Fig. 2-15,

drain current was measured at different back-gate bias (applied at the GP). The body potential is raised when the back-gate bias is increased. As a result, the front-channel threshold voltage linearly decreases with V_{BG} (Fig. 2-15b) and the drain current is enlarged (Fig. 2-15a).

Our results show that coupling effect depends on the Si film thickness. In thinner film, threshold voltage variation decreases, meaning less coupling effects. This will be further discussed with low-temperature measurement in Fig. 2-18 which provides additional insight.

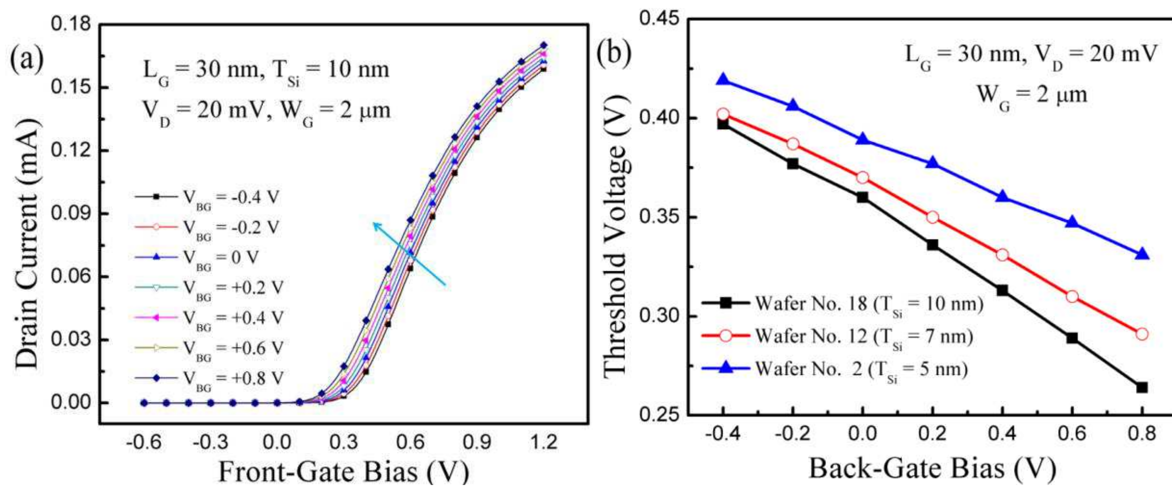

Fig. 2-15: The effect of back-gate bias on front-channel properties. (a) Drain current versus front-gate bias at different back-gate bias. (b) Front-channel threshold voltage versus back-gate bias for various Si film thicknesses.

2.1.5. Temperature-dependent properties

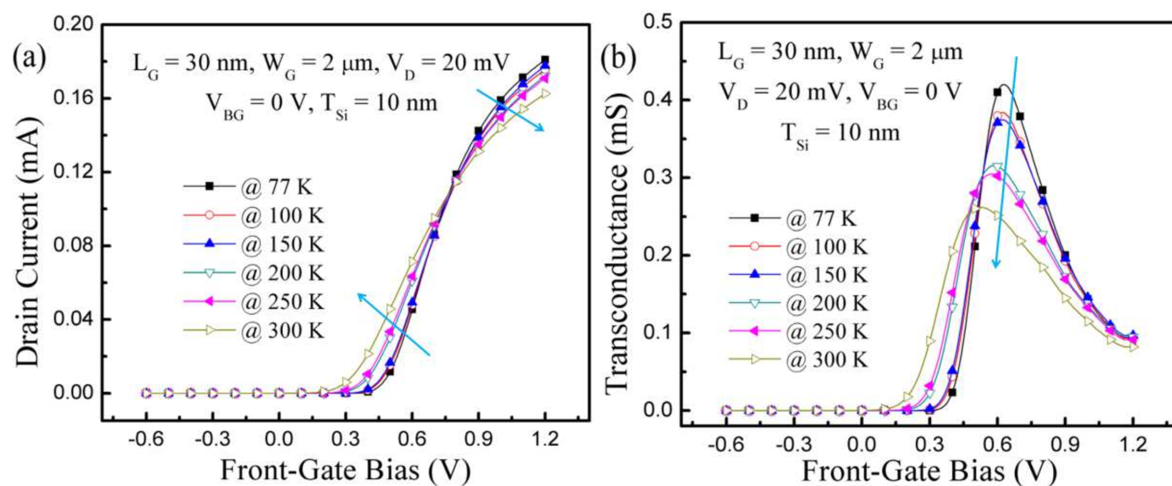

Fig. 2-16: Temperature dependence of typical device characteristics. (a) Drain current and (b) transconductance curves versus front-gate bias for a wide range of temperature.

Typical device characteristics were studied (Fig. 2-16) for a wide range of temperature (from 77 K to 300 K). At low temperature, front-channel threshold voltage is increased due to

the variation of the Fermi level. Higher drain current level and transconductance peak at low temperature mirror enhanced mobility. The overall trend of the device behavior is the same for different Si film devices.

The device properties were quantified by extracting the main parameters to evaluate the influence of temperature and physical mechanisms (Fig. 2-17). The effect of Si film thickness was already discussed and obeys the same trends as in Fig. 2-12. At higher temperature, carrier mobility is reduced due to increased phonon scattering [68, 69]. Front-channel threshold voltage decreases ($\Delta V_{THF}/\Delta T \approx 0.7$ mV/K) at higher temperature. This rate of change is much smaller than in bulk MOSFETs and promotes FD SOI for operation in a wide temperature range.

The threshold voltage is expressed by the linear combination of the flat-band voltage $V_{FB,}$ the Fermi potential $2\phi_B$ and the potential drop in the depletion region (Eq. (2.14)). In FD MOSFETs, the latter term is temperature independent, the main contribution arising from the Fermi level variation: $2\phi_B \times (1 + qD_{it} / C_{ox})$. While increasing the temperature, the Fermi surface potential approximated by $2\phi_B = 2(kT/q) \cdot \ln(N_a / N_i)$, decreases rather linearly with temperature because the intrinsic carrier density N_i exponentially increases.

At low temperature, subthreshold swing is decreases more or less linearly according to [17]:

$$SS = \ln 10 \left(\frac{kT}{q} \right) \left[1 + \frac{(C_{si} + C_{Dit})}{C_{ox}} \right] \tag{2.20}$$

where k is Boltzmann constant, T is absolute temperature, q is electron charge, C_{si}, C_{Dit} and C_{ox} are capacitances of silicon body, interface traps and gate oxide. In Eq. (2.20), kT/q reduces with temperature while the bracket term is constant, except when D_{it} increases. In our devices, the variation of D_{it} is basically masked by the high oxide capacitance. Notice that subthreshold swing variation is almost similar in 50 nm and 100 nm length device. This means that short channel effects do not occur above 50 nm gate length device.

We can extract interface trap density from the SS(T) [70]. Subthreshold swing is proportional to the temperature (Eq. (2.20)). Therefore, the expected value at 77K is around 25 mV/dec with L_G = 100 nm and T_{si} = 5 nm. However, extracted value from the measurement is 32 mV/dec which yields an interface trap density of $5.7 \cdot 10^{12}$ cm^2eV^{-1}. Interface trap density can also be extracted with Eq. (2.20) by using extracted SS value (SS = 68 mV/dec @ L_G = 100 nm, T_{si} = 5 nm and T = 300 K). The extracted value is $4.6 \cdot 10^{12}$

cm^2eV^{-1}. The two extracted interface trap densities are almost the same. These values are reasonable but their interpretation requires caution. Eq. (2.20) is an approximation which does not account for the influence of traps at the film-BOX interface. The effective D_{it} values include the back traps, however, their discrimination is very difficult.

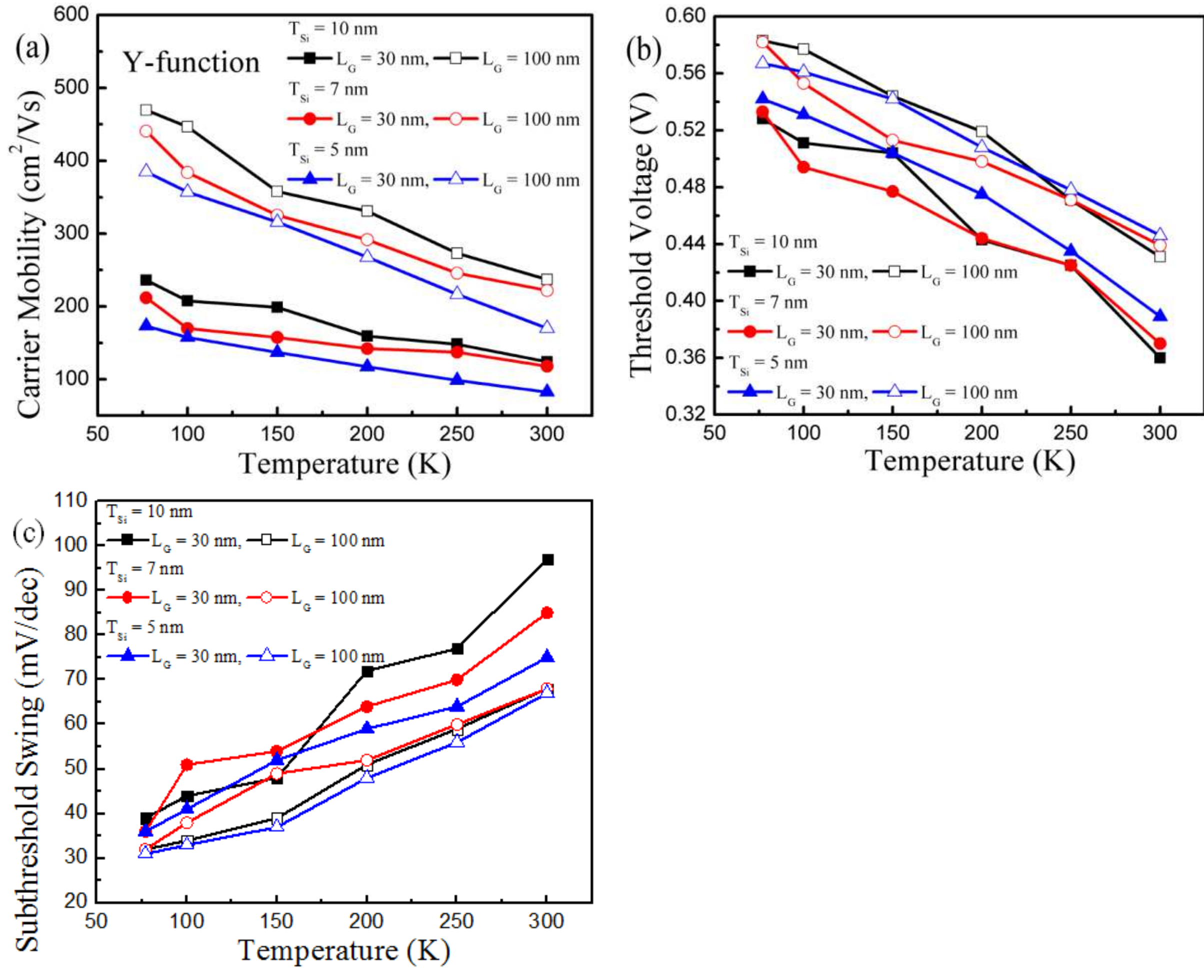

Fig. 2-17: Device characteristics for a wide range of temperature. (a) Mobility, (b) threshold voltage and (c) subthreshold swing as a function of temperature for various thickness of Si film. W_G = 2 µm, V_D = 20 mV and V_{BG} = 0 V.

We observed an unexpected effect in ultra-thin film device. Coupling effect appears to depend on temperature (Fig. 2-18). Actually, the coupling is a result of the competition between front-gate, back-gate and SCEs. In Fig. 2-18a, the lateral variation of transconductance curve is reduced at low temperature. Fig. 2-18b shows lower transconductance peak in thinner film device at 77 K like for the results obtained at room temperature. However, the lateral shift of transconductance is slightly larger in thinner device, which apparently contradicts the result of Fig. 2-15b.

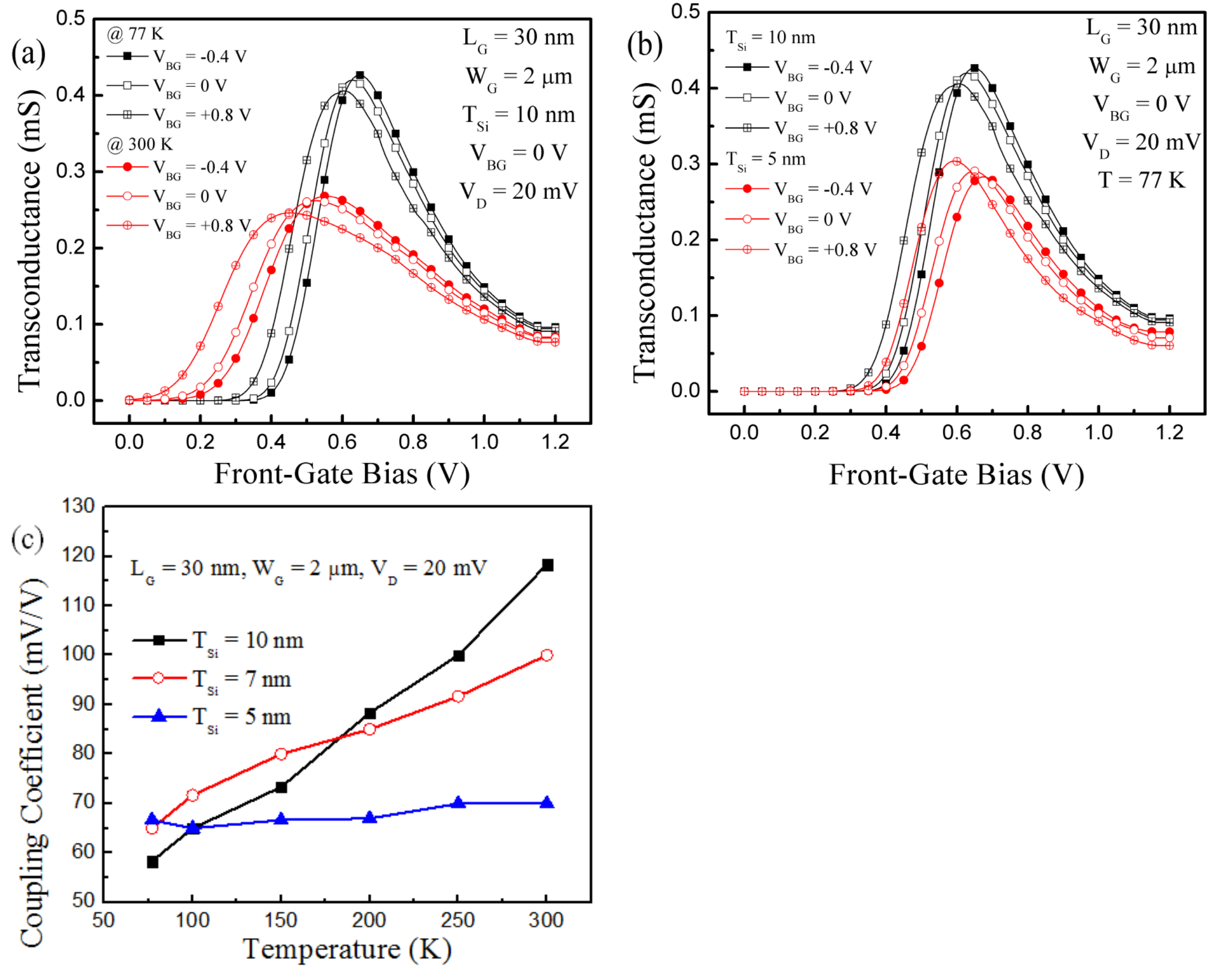

Fig. 2-18: Impact of temperature and film thickness on coupling effects in short device (L_G = 30 nm). Transconductance versus front-gate bias at (a) different temperature (T = 77 K and 300 K @ T_{si} = 10 nm) and (b) different film thickness (T_{si} = 5 nm and 10 nm @ 77 K). (c) Coupling coefficient as a function of temperature for various Si film thicknesses.

Fig. 2-18c shows the coupling coefficient defined as $\alpha = -\Delta V_{THF}/\Delta V_{BG}$ in order to quantify the coupling effect variation with temperature. First, at 77 K, coupling coefficient is a little larger in thinner device whereas it is much smaller at 300 K. The coupling effect normally increases with body capacitance (Eq. (2.19)). Therefore, the effective body capacitance and coupling effect increase in thinner device. At higher temperature, the SCEs become more noticeable on the device operation [71, 72] and enhance coupling effect [73]. Therefore, coupling effect increases in short MOSFETs with increasing temperature. On the other hand, the rate of change of coupling coefficient $\Delta\alpha/\Delta C_b$ is smaller in thinner device than in thicker one. Fig. 2-18c confirms that, in 5 nm film, coupling coefficient is almost constant for a wide range of temperature. The reason is that SCEs are clearly diminished in thinner film as shown in Fig. 2-12c. Thereby, the enlargement of coupling effect with increasing

temperature is prevented by the thinner film. As a result, at higher temperature, coupling effect is larger in thicker film and short device (Fig. 2-15b and Fig. 2-18c).

2.1.6. Conclusion

In this section, the properties of advanced ultra-thin FD SOI MOSFET were investigated for a wide range of temperature. Thanks to the state-of-the art MOSFET technology, high carrier mobility was achieved. Threshold voltage and SCEs are strongly dependent on Si film thickness: in thinner film, threshold voltage increases via quantum confinement, and SCEs are suppressed as the S/D junction depth and depletion region decrease. These results are very promising for beyond 22 nm technology node application.

Unlike for the conventional SOI MOSFETs, the competition between SCEs and Si film thickness causes unusual coupling effect. Coupling effect in short MOSFETs increases at higher temperature, more or less according to the Si film thickness. But, in devices thinner than 5-6 nm, the coupling tends to become practically insensitive to temperature. This implies that the same back-biasing scheme can be maintained for operation in a wide range of temperatures.

2.2. Coupling Effects in Double-Gate FinFETs

2.2.1. Introduction

Low power consumption and co-integration of various functionalities are the mainstream in today's VLSI circuit and system design due to the increasing demand for portable electronics and embedded system manufacturing. The size of the transistor has to be reduced as described in Chapter 1. However, as the channel length is reduced, the control of the current by the gate is jeopardized and increases the off-state leakage and power consumption. Dynamic threshold voltage modulation (*i.e.*, high V_{TH} in OFF state and low V_{TH} in ON state) is attractive to reduce the consumption and integrate different functions on the same chip [4, 74, 75]. In FD SOI technology, the back-gate bias and/or the non-volatile charge stored in ONO buried insulator can be used for threshold voltage modulation [4, 76].

Ultra-Thin Body and Buried Insulator (UTBB) and multiple-gate transistors are competing for CMOS downscaling [70, 77]. SOI FinFET is the most probable winnner thanks to its simple fabrication and enhanced electrostatic control [77-79].

We have seen that, in fully-depleted SOI MOSFETs, the front- or back-channel threshold voltage can be modified by using the opposite gate. The question is whether this back-biasing scheme also works in FinFETs. In FD SOI FinFETs, especially with narrow fin width, we have to consider the influence of the 'lateral' electric field between the two lateral gates on the 'vertical' substrate-to-channel coupling effect. We compared two different types of SOI FinFETs. Using experimental and 3D simulation results:

(i) Vertical DG FinFET: top-channel activation is suppressed by thick insulating layers at the top of the fin and only the two lateral-channels are activated by the front-gate biasing.

(ii) Triple-gate FinFET: top and lateral-channels are equally activated by applying front-gate bias.

Since coupling in triple-gate FinFETs have been documented [80], we focus on the coupling effect between lateral-gates (also referred to as 'front' gate) and back-gate in DG FinFETs. We highlight the enhanced front-channel threshold voltage variation by the back-gate bias which can be applicable for dynamic threshold voltage modulation in vertical DG FinFET. Triple-gate FinFETs are used to benchmark the two device structures. The effect of the fin width on the coupling effects is further investigated.

2.2.2. Typical properties

SOI wafers fabricated with the Smart-Cut^{TM} technology were used as starting material. The thickness of the buried SiO_2 insulator (BOX) is T_{BOX} = 140 nm. The silicon film thinned down to 40 nm defined the fin height H_F. SiO_2 (1 nm) and HfO_2 (2.5 nm) layers were stacked for lateral-gate insulators. The effective oxide thickness (EOT) was determined to be T_{ox} = 1.4 nm. At the top of the fin, thicker SiO_2 (5 nm) and nitride (10 nm) layers were deposited to prevent the top-channel conduction. The two lateral-gates are controlled by the same bias. Vertical DG FinFETs with different fin width W_F (down to 25 nm) and gate length L_G (down to 40 nm) were manufactured to investigate the geometrical issues. The width we will be referring to is the designed value. The real fin width after process completion is 20-25 nm narrower. The triple-gate FinFETs used for comparison have H_F = 20 nm silicon body height. Even though the vertical DG FinFETs are taller than the triple-gate FinFETs, they show enhanced sensitivity to the back-gate biasing, as discussed in section 2.2.3. All devices have undoped body, TiN metal gate and operate in fully-depleted mode. Fig. 2-19 shows the cross-section of the vertical DG FinFET fabricated at Sematech (USA).

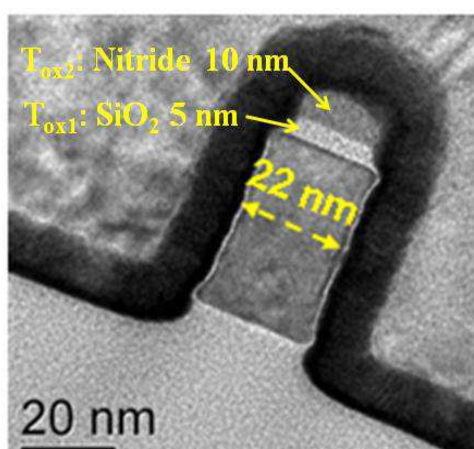

Fig. 2-19: TEM cross-section of vertical double-gate FinFET fabricated on SOI wafer.

The electrical transport properties depend on the device geometry and fin size (L_G, W_F). The effect of the gate length on the drain current $I_D(V_{FG})$ and transconductance $g_m(V_{FG})$ characteristics is depicted in Fig. 2-20. The $I_D(V_{FG})$ curves prove that an excellent gate control is achieved: (i) high ON/OFF current ratio (> 10^8) and (ii) low subthreshold swing (SS = 70 mV/dec at L_G = 0.5 μm). The front-channel threshold voltage V_{THF} value (V_{THF} = 0.17 V @ L_G = 0.5 μm) was extracted from the Y-function [46]. In shorter devices, the drain

current level and the transconductance peak value increase steadily which implies that the series resistance effects are not overwhelming and remain reasonable. The electron mobility, extracted from the transconductance peak [45], reaches relatively high value (~ 350 cm^2/Vs). These results reveal promising electrical properties of vertical DG FinFETs.

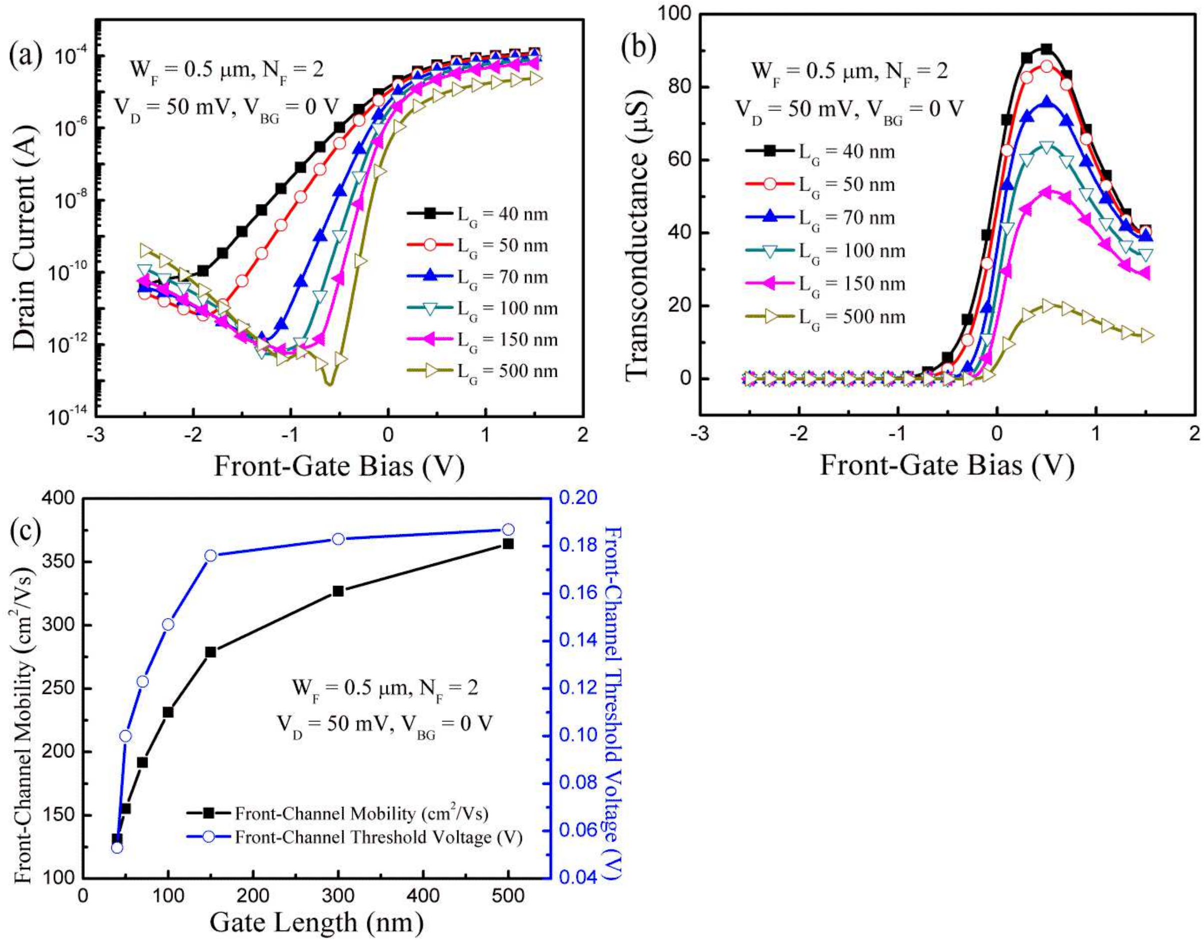

Fig. 2-20: Front-channel characteristics of vertical DG FinFETs. (a) Drain current and (b) transconductance as a function of the front-gate bias for different gate lengths. (c) Front-channel mobility and threshold voltage versus gate length.

In Fig. 2-20, we also observe the regular effects of shorter channel lengths: (i) subthreshold swing increase, (ii) V_{THF} roll-off and (iii) carrier mobility degradation. The mobility behavior is explained by the process-induced neutral defects located near the source and drain terminals which overlap in very short channels [36]. Only below 50 nm gate length, the threshold voltage and the subthreshold swing are significantly degraded due to the charge sharing effect [19]. Notice that, with narrower fin width, lower subthreshold swing (SS = 65 mV/dec @ W_F = 50 nm, L_G = 0.5 µm) and reduced short-channel effects are obtained. Indeed, the transversal component of the electric field is enhanced, improving the overall control of

the lateral-gates on the body. Back-channel characteristics were also assessed. Thanks to the good body/BOX interface quality [81], even higher mobility (~ 420 cm^2/Vs) than in the front channel was achieved. The extracted back-channel threshold voltage V_{THB} is around 1 V for L_G = 0.5 μm.

2.2.3. Coupling effects

(a) 3-Dimensional coupling model

In 2007, Akarvardar *at al*. in our group reported a two-dimensional coupling model to consider the influence of the fin width and back-gate on coupling effects in triple-gate SOI FinFETs [82]. The cross-section of a triple-gate FinFET, showing the axes and symbol conventions, is given in Fig. 2-21.

A parabolic potential variation between the two lateral gates was assumed:

$$\phi(x,y) = a(y)x^2 + b(y)x + c(y) \tag{2.21}$$

where $\phi(x,y)$ is the 2-D body potential in undoped body. The 2-D Poisson's equation is solved for full depetion and negligible body doping:

$$\frac{\partial^2 (x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = 0 \tag{2.22}$$

A constant surface potential is considered on the three sides:

$$\phi(\pm W_F/2, y) = \phi(x,0) = \phi_{S1}(y) \tag{2.23}$$

Corner effects, quantum-mechanical effects, substrate depletion (under the BOX) and drain bias effect are neglected. ϕ_{S2} is the extremum of the back-surface potential at $\phi(x, T_{si})$ at the fin-BOX interface.

The solution of Eq. (2.22) using Eqs. (2.21) and (2.23) is given by

$$\phi(x,y) = \phi_{S1} + \frac{f(y)}{f(T_{si})}\left(1 - \frac{4x^2}{W_F{}^2}\right)(\phi_{S2} - \phi_{S1}) \tag{2.24}$$

where $f(y)$ is defined as

$$f(y) = \sinh\left(2\sqrt{2}\frac{y}{W_F}\right) \tag{2.25}$$

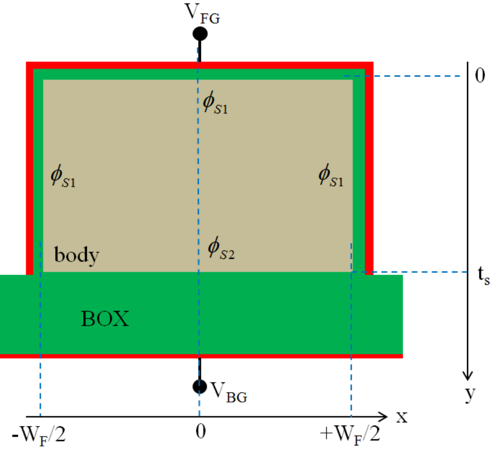

Fig. 2-21: Cross-section of the triple-gate SOI FinFETs (perpendicular to current flow direction) showing the boundary conditions and axes used in modeling.

The derivation of the threshold voltage from the potential model is straightforward. Like for the Lim and Fossum's model (Chapter 2.1.4) [14], ϕ_{S1} and ϕ_{S2} are first related to V_{FG} and V_{BG} as follows:

$$V_{FG} - V_{FBf} = \phi_{S1} + A\frac{C_w}{C_{oxf}}(\phi_{S1} - \phi_{S2}), \tag{2.26}$$

$$V_{BG} - V_{FBb} = \phi_{S2} + B\frac{C_w}{C_{oxb}}(\phi_{S2} - \phi_{S1}) \tag{2.27}$$

where

$$A = \frac{2\sqrt{2}}{sinh\left(2\sqrt{2}\,\frac{T_{Si}}{W_F}\right)}, \quad B = \frac{2\sqrt{2}}{tanh\left(2\sqrt{2}\,\frac{T_{Si}}{W_F}\right)} \quad and \quad C_w = \frac{\varepsilon_{Si}}{W_F}$$

Eqs. (2.26) and (2.27) are basic relations to describe the coupling effects between the front gate and substrate in a triple-gate FinFETs. The front- and back-channel threshold voltage can be obtained by replacing V_{FG}/V_{BG} with V_{THF}/V_{THB} and $\phi_S = \phi_F + \phi_T$ (where ϕ_T is band-bending at threshold voltage and (x,y)=(0,0)).

When the back-channel is depleted, ϕ_{S2} varies with V_{BG} in Eq. (2.27). Therefore, front-channel threshold voltage becomes:

$$V_{THF} - V_{FBF} = \alpha(V_{BG} - V_{FBB}) + \left(1 + A\frac{C_w}{C_{oxf}} - \alpha B\frac{C_w}{C_{ox}b}\right)(\phi_F + \phi_T) \tag{2.28}$$

where

$$\alpha = \left|\frac{dV_{THF}^{\;depb}}{dV_{BG}}\right| = \frac{A(C_w / C_{oxf})}{1 + B(C_w / C_{oxb})}$$

(2.29)

is the front-channel coupling coefficient in triple-gate FinFET.

This model reproduces the coupling in triple-gate FinFETs but, according to our measurements, does not match the data in DG FinFETs. Using the same principles, we have developed a sister model. The coupling coefficient in DG FinFETs is expressed as [83]

$$V_{THF} = \alpha_{dep}(V_{BG} - V_{FBb}) + (1-\alpha_{dep})\phi_{inv} + V_{FBf}, \quad Back\ interface\ depletion \tag{2.30}$$

with

$$F(y) = \frac{sinh[(y+T_{si}/2)/W_0] + \eta_1 cosh[(y+T_{si}/2)/W_0]}{(1+\eta_1\eta_3)sinh(T_{Si}/W_0) + (\eta_1+\eta_3)cosh(T_{Si}/W_0)} \tag{2.31}$$

where V_{FBf} and V_{FBb} are the flat-band voltages related to the front and back interfaces, respectively, $W_0 = \sqrt{\eta_2/2 + 1/8}W_F$, $\eta_1=\varepsilon_{Si}/(C_{tox}W_0)$, $\eta_2=\varepsilon_{Si}/(C_{lox}W_F)$, and $\eta_3=\varepsilon_s/(C_{BOX}W_0)$. C_{tox}, C_{lox} and C_{BOX} are the capacitances per unit area of the top-gate oxide, lateral-gate oxide and back-gate oxide layers. ε_{Si} is the permittivity of silicon. Coupling coefficients $\alpha_{dep}=[1-(\lambda F(-T_{Si}/2))^{-1}]^{-1}$ define the slope dV_{THF}/dV_{BG} when the back interface is depleted. λ can be formulated by $\lambda=[1+(4\eta_2)^{-1}]^{-1}$. This model was validated by experiments and simulations.

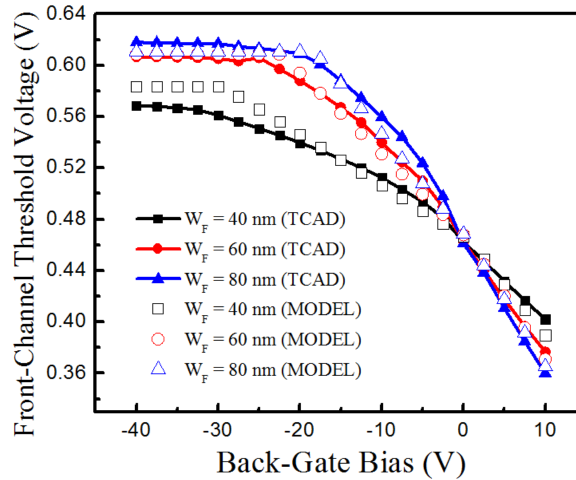

Fig. 2-22: Front coupling effect for various fin widths. Front-channel threshold voltage versus back-gate bias. The analytical model matches the TCAD simulations.

To verify the proposed analytical model, comparison with the simulated front gate threshold voltage as a function of the back gate bias is performed in Fig. 2-22. Y-function method [46] was employed to extract the threshold voltage from simulations. An overall

agreement between the analytical and simulated results can be observed. We see a smaller front-channel coupling coefficient α in narrower fin DG devices.

(b) Experimental results

The 'vertical' coupling effect between the two lateral-channels and the back-gate bias was systematically investigated in our fully-depleted vertical DG FinFETs. These devices can be operated with one, two and/or three channels by applying appropriate bias at front- and/or back-gates. In Fig. 2-23, we compare the front-channel transconductance curves at different back-gate bias (from -15 V to 15 V) in wide (W_F = 0.5 µm) and narrow (W_F = 80 nm) fins. As the fin width becomes sufficiently small (Fig. 2-23b), the influence of the two lateral-gates prevails attenuating the back-gate effect (smaller lateral shift of $g_m(V_{FG})$ curves with V_{BG}). The activation of the back-channel is barely visible for V_{BG} = +15 V where the transconductance plateau tends to disappear. When the back-channel is driven into accumulation [70], the transconductance peak is degraded due to the enlarged surface scattering induced by the increased vertical electric field.

For wide fin device (W_F = 0.5 µm, Fig. 2-23a), when the back-gate interface moves from accumulation to inversion regime, the potential is increased in the whole body and the lateral-channel threshold voltage decreases. Therefore, a large shift of the transconductance curve towards lower front-gate voltage is observed. At positive back-gate bias (> +3 V), a hump appears in the transconductance curve reflecting the early activation of the back-channel. This effect is similar to the case of planar FD MOSFETs. As the front-gate bias increases from -2 V to 0 V, the back-channel threshold voltage V_{THB} decreases and the back-channel is turned on (for $V_{FG} \approx -$ 1V, see curve at V_{BG} = +9 V in Fig. 2-23a) before the front-channel threshold voltage V_{THF} is eventually reached ($V_{THF} \approx$ -0.3 V).

At sufficiently negative back-gate bias (< -12 V), the gate-induced floating body effect (GIFBE) is switched on. When the back-interface is biased close to accumulation and the front-channel lies in strong inversion, the floating body is charged by direct tunneling through the lateral oxides with an excess of majority carriers [84], and a distinct GIFBE peak becomes visible in the transconductance curve (for $V_{FG} \approx$ +1 V, Fig. 2-23a). Notice that this specific transconductance peak, obtained when the back-channel is accumulated, is a pure floating-body effect and its higher value does not imply mobility improvement.

In narrower fin device (designed value: W_F = 80 nm, Fig. 2-23b), the transconductance hump shrinks and the GIFBE peak disappears. These trends again indicate the predominance

of the transversal field induced by the lateral-gates over the vertical field component generated by back-gate bias. For negative front-gate bias, the back-channel threshold voltage is increased, hence the back-channel inversion occurs for more positive V_{BG}, and the g_m hump is diluted. The transconductance peak reduction reflects an increase of the series resistance in narrower fins. On the other hand, the GIFBE vanishes simply because the back-interface cannot be accumulated.

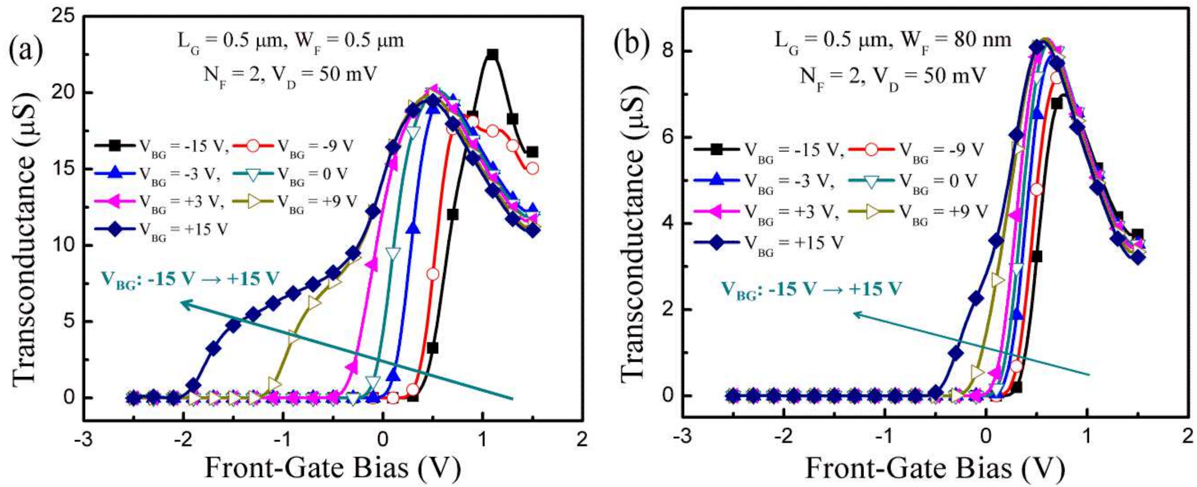

Fig. 2-23: Front-channel coupling effects in vertical DG FinFETs. Transconductance as a function of the front-gate bias at different back-gate bias in (a) wide (W_F = 0.5 µm) and (b) narrow (W_F = 80 nm) fin devices.

Fig. 2-24 highlights the reciprocal effect of the front-gate bias on the back-channel transconductance in wide (W_F = 0.5 µm) and narrow (W_F = 80 nm) fins. In a narrow FinFET, higher back-gate bias is required to overcome the lateral-gate influence. When the front-gate bias changes from accumulation to inversion (V_{FG} from -1V to 1 V), the body potential is increased and the back-channel threshold voltage is reduced. Unlike the front-channel transconductance characteristics shown in Fig. 2-23, the lateral shift is more pronounced in narrow fins where the sidewall gates dominate. Remark that for front-gate accumulation, the back transconductance peak is significantly degraded for two reasons. First, strong accumulation of the sidewalls depletes the edges of the back-channel so the effective width becomes inferior to the fin width. Second, the effective field is high and degrades the carrier mobility.

One peak only, corresponding to the back-channel activation, is observed on the transconductance curve at $V_{FG} \leq 0$ V (when the lateral-channels are depleted or accumulated). However, at positive front-gate bias ($V_{FG} \geq +0.6$ V, Fig. 2-24b), the transconductance curves show multiple features which suggest that the lateral-channel is not homogeneous along the

fin height. The upper region is activated before the lower region of the sidewalls which are in contact with the accumulated back-interface. The hump (at $V_{BG} \approx -15$ V) reflects the conduction in the lateral-channel regions located far from the back-interface. The next peak (at $V_{BG} \approx -3$ V) indicates the completion of the lateral-channels. The third peak ($V_{BG} > 0$ V) is generated by the activation of the back-channel.

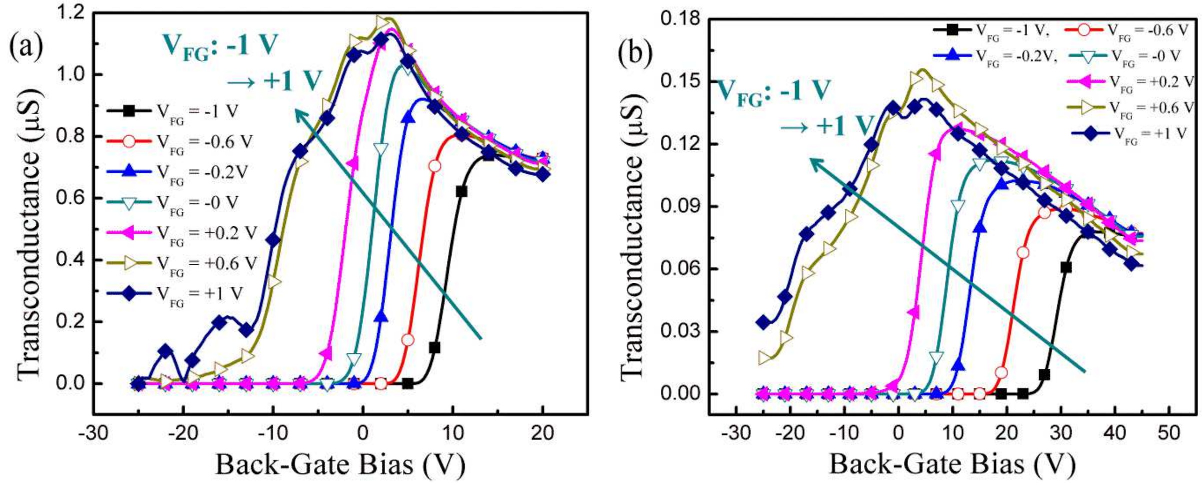

Fig. 2-24: Back-channel coupling effects in vertical DG FinFETs. Transconductance versus back-gate bias at different front-gate bias in (a) wide (W_F = 0.5 μm) and (b) narrow (W_F = 80 nm) fin device. L_G = 0.5 μm, V_D = 50 mV, two parallel fingers (N_F = 2).

These results demonstrate that the coupling effect is visible in vertical DG FinFET and the critical device parameter is the fin width. According to the formula proposed by [14] for FD planar MOSFET, front- and back-channel coupling effects can be approximated as:

$$\Delta V_{THF} \cong -\frac{T_{ox}}{T_{BOX}} \cdot \Delta V_{BG} \tag{2.31}$$

and

$$\Delta V_{THB} \cong -\frac{T_{BOX}}{T_{ox}} \cdot \frac{3T_{ox}}{3T_{ox} + T_{Si}} \cdot \Delta V_{FG} \tag{2.32}$$

where T_{BOX}, T_{ox} and T_{Si} are the thicknesses of the buried insulator, front-gate oxide and Si film. This well-known 1D model has recently been updated to include the contributions of interface traps, quantum effects in ultrathin films and short-channel effects [73]. However, the model applies to planar MOSFETs exclusively and cannot be directly adopted to FinFETs, where the coupling is 3D and involves the fin width. The Akarvandar's model (Eq. (2.29), [82]), proposed for the triple-gate FinFETs, is not acceptable either.

The effect of the fin width is investigated through the front- and back-threshold voltage

variations in Fig. 2-25. The threshold voltages were extracted with the Y-function method [46] and plotted versus the opposite gate bias and fin width. It is clear that, in wide fin devices, the front-channel coupling effect (V_{THF} vs. V_{BG}) is enhanced. We obtain a front-channel coupling coefficient, $\alpha = -\Delta V_{THF}/\Delta V_{BG} \approx 34$ mV/V, which is far from the value (α = 200 mV/V) given by Eq. (2.31). The latter value was calculated by considering the top oxide thickness (T_{ox} = 30 nm) which is reasonable in wide triple-gate FinFETs. The discrepancy is due to the fact that, in DG FinFETs, the top-channel just cannot be activated. Taking T_{OX} = 1.4 nm (lateral-gate oxide), the front-channel coupling coefficient is only α = 10 mV/V. The measured α is between the two extreme values.

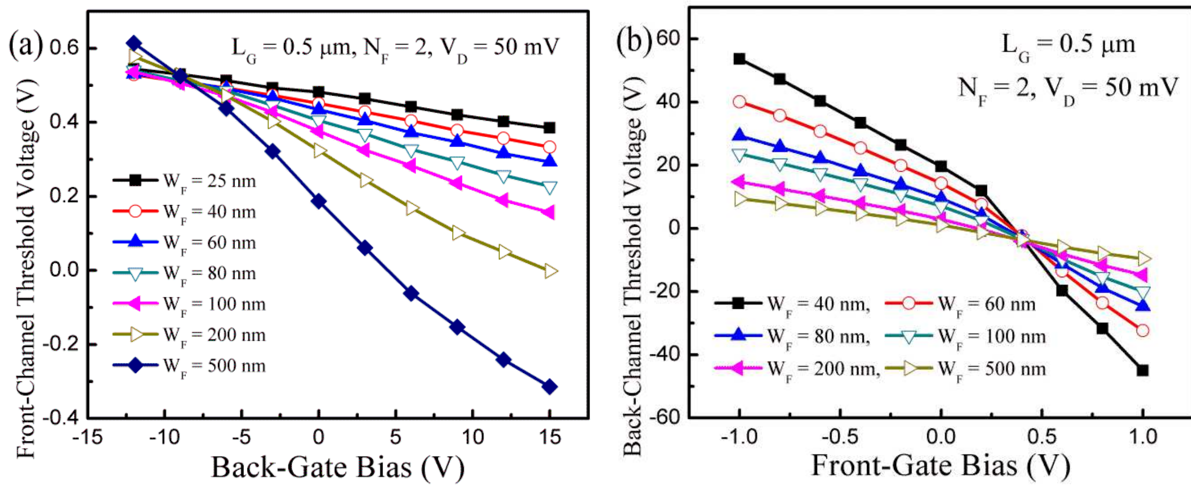

Fig. 2-25: Dependence of the coupling effect on the fin width. (a) Front-channel and (b) back-channel threshold voltage as a function of the opposite gate bias.

The front-channel coupling coefficient strongly decreases for narrow fin width: for W_F = 25 nm, we obtain $\alpha \approx 7.5$ mV/V. This trend is explained by 3D coupling effects [80]. In narrow fin devices, the lateral electric field induced by the two side gates is able to control the potential at the body/BOX interface. Therefore, the 'vertical' field from bottom to top, generated by the back-gate bias, is blocked by the enhanced 'lateral' field. Consequently, the capability of the back-gate to modulate the front-channel properties is declining in narrower fins. This is why the lateral shift and hump of the transconductance curves are reduced (Fig. 2-23 a and b) and the front-channel coupling effect is smaller (Fig. 2-25a) in the narrow device.

The reciprocal characteristics $I_D(V_{BG})$ and $g_m(V_{BG})$ are also very informative about the coupling effects. Fig. 2-24 shows that the lateral shift is accentuated in narrow fins. This behavior looks as contradicting the front-channel trends (Fig. 2-23) but it actually originates

from the same competition between 'lateral' and 'vertical' coupling. In a narrow fin, when the front-gate bias is more negative, the body/BOX interface tends to be accumulated too. This makes it more difficult for the back-gate to invert the back interface, hence the back-channel threshold voltage increases significantly. Therefore, the back-channel coupling coefficient (Fig. 2-25b) is increased, reaching $\beta = \Delta V_{THB}/\Delta V_{FG} \approx 73$ V/V in narrower FinFET. This coupling rate is in line with Eq. (2.32).

As the coupling effect depends on the device architecture, triple-gate FinFETs were compared with vertical DG devices in Fig. 2-26. In a triple-gate FinFET, the top section of the channel (under the horizontal gate) is directly influenced by V_{BG}, as in a FD SOI MOSFFET. It is known that in planar transistors, the 1D vertical coupling increases as the Si film thickness is reduced. Since our FinFETs feature smaller fin height (20 nm), we would expect a stronger coupling effect than in DG MOSFETs (40 nm). However, as we can see in Fig. 2-26a, when the back-gate bias changes from -15 V to 15 V, the lateral shift of the front-channel drain current is larger in the vertical DG FinFET, despite the fin height is lower in the triple-gate FinFET. Fig. 2-26b shows that the front-channel coupling coefficient α is clearly superior in the vertical DG FinFET. Why? We propose the following scenario. In triple-gate FinFETs, the control of the body potential is stronger due to the combined contributions of the lateral and top sections of the gate. Indeed, the vertical field induced by the back-gate is facing the antagonist vertical field originating from the top-gate. Another way of seeing this mechanism is that the front-gate opposes the straight penetration of the vertical field from the back-gate. In DG MOSFETs, the absence of the top section of the gate makes the vertical field from bottom to top more efficient.

The key conclusion is that front-channel coupling effect is enhanced in vertical DG FinFET, where the impact of the back-gate is more intense. In other words, the front-channel threshold voltage is more easily tuned by the back-gate bias in vertical DG FinFET. It follows that vertical DG FinFETs are more suitable candidates for dynamic threshold voltage adjustments than triple-gate FinFETs.

By contrast, the back-channel coupling coefficient β is larger in triple-gate than in vertical DG FinFET. Since three gates govern more efficiently the body potential than two gates, it is clear that the back-channel threshold voltage is more hardly achieved for $V_{FG} < 0$. However, at this stage, we cannot confirm that the larger back-channel coupling effect in triple-gate FinFET comes from the enhanced control of the front-gate, the thinner silicon film thickness or both. We will further discuss the origin of coupling by comparing the two

devices with 3D numerical simulations [85] in the following section.

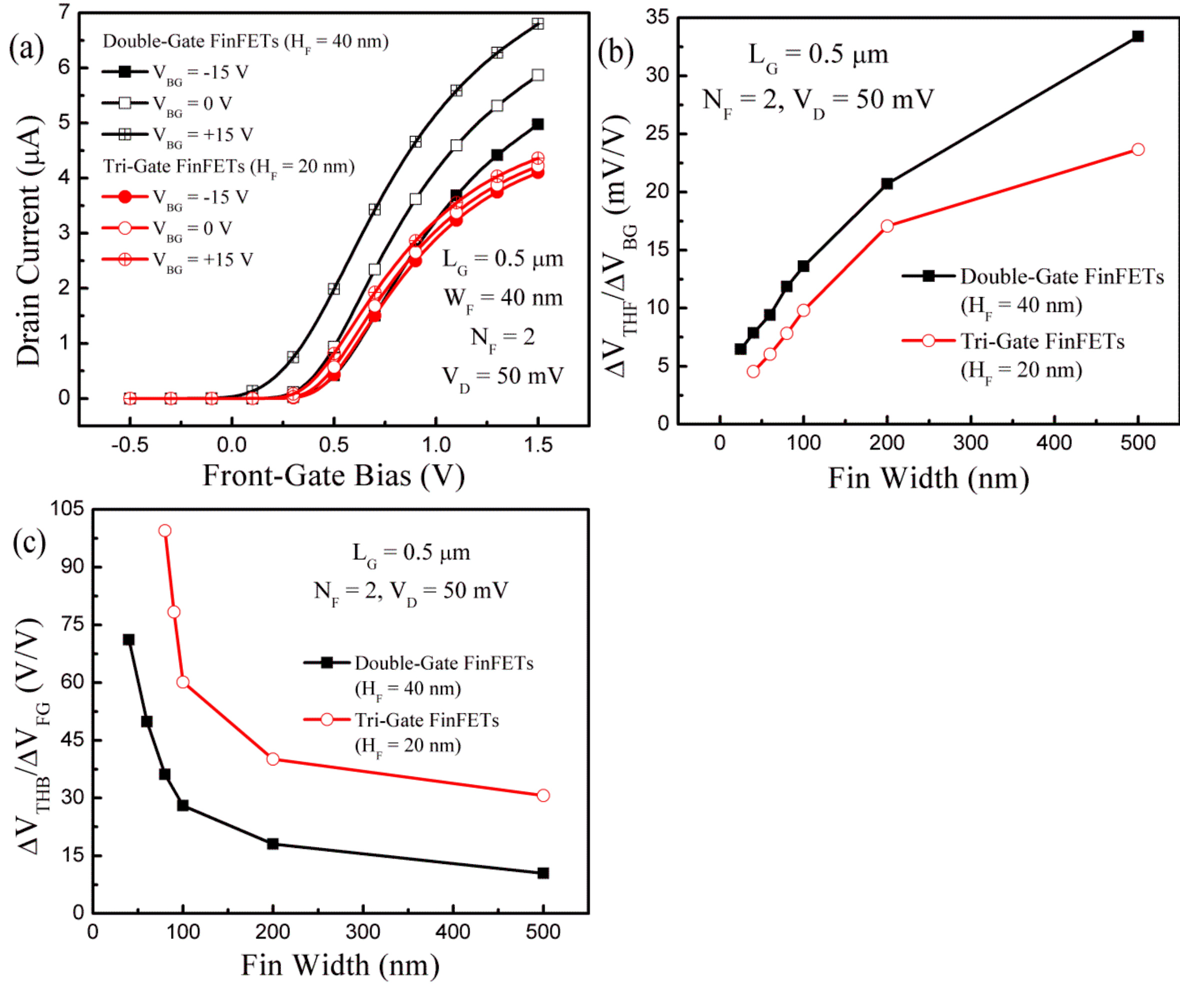

Fig. 2-26: Comparison of the coupling effects in vertical DG and triple-gate FinFETs. (a) Drain current versus front-gate bias at different back-gate bias. (b) Front-channel and (c) back-channel coupling coefficient as a function of fin width.

(c) 3-Dimensional simulation results

Front- and back-channel coupling effects were simulated to validate the effect of the fin width and to compare double-gate and triple-gate FinFETs with same fin height. In these simulations, only the Poisson and electron continuity equations were considered as the conduction mechanisms are essentially based on the electron drift-diffusion current. The structures have two different oxide thicknesses on top of the fin, 30 nm for the DG FinFET (top-channel deactivated) and 1.4 nm for the triple-gate FinFET. The lateral-gate oxide thickness (1.4 nm) and the Si fin height (40 nm) are the same for both structures.

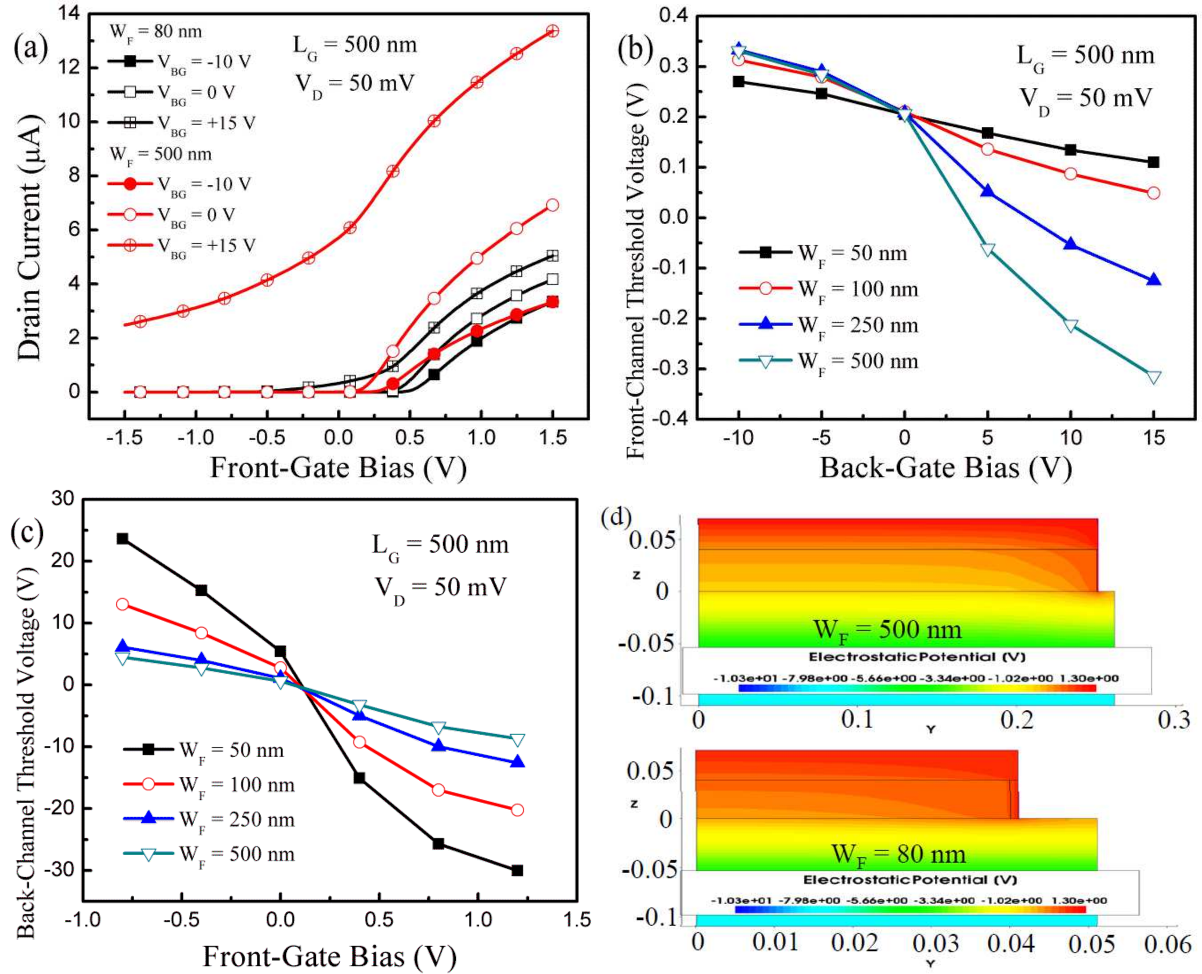

Fig. 2-27: Simulation of coupling effects in vertical DG FinFETs. (a) Drain current versus front-gate bias at various back-gate bias in wide (W_F = 0.5 μm) and narrow (W_F = 80 nm) devices. (b) Front-channel and (c) back-channel threshold voltage as a function of the opposite gate bias for different fin widths. (d) Potential profile in wide and narrow fins at V_{FG} = +1 V and V_{BG} = -10 V.

Fig. 2-27a shows $I_D(V_{FG})$ curves for DG FinFETs, simulated at different back-gate bias. In the narrow fin device (W_F = 80 nm), the lateral shift of the front-channel characteristics is much less than in wide device (W_F = 0.5 μm), confirming the measurement data of Fig. 2-23. Fig. 2-27 b and c show the decrease in front- and back-channel threshold voltage as the opposite-channel moves from accumulation towards inversion regime. Like in our experimental results, the front-channel coupling effect is reduced while the back-channel coupling is amplified in narrow FinFET. The origin of this asymmetry is confirmed in Fig. 2-27d by comparing the potential profiles in wide (W_F = 0.5 μm) and narrow (W_F = 80 nm) devices operated with positive front-gate bias (V_{FG} = +1 V) and negative back-gate bias (V_{BG} = -10 V). In the wide device, the body potential is much lower than in the narrower fin where the influence of the positively biased lateral-gates is prevailing and tends to mask the effect of the negative back-gate bias. In wide devices, the back-gate bias can more easily change the

front-channel threshold voltage due to enhanced penetration of the vertical electric field and less contribution of the lateral field. The simulated front-channel coupling effect (Fig. 2-27b) increases in wider fin device and matches the values of Fig. 2-25a. The back-channel coupling effect is always higher in narrow fins as illustrated in Figs. 2-27c.

A very good agreement between experimental and simulation results for vertical DG FinFET was obtained in a wide range of fin width. Small differences in very narrow fins may originate from the real size and shape of the fin. The etching process makes the fin smaller and less rectangular than the mask-defined values. As a result, the front-channel coupling effect is slightly smaller and the back-channel coupling coefficient is slightly larger in the experiment than in the simulation data.

The coupling effects in triple-gate FinFET were simulated for 40 nm fin height in order to simplify the comparison with vertical DG FinFETs. Typical transfer characteristics showing the effect of back-gate bias are reproduced in Fig. 2-28a. As expected from the experimental data, the horizontal shift of the drain current is smaller than in vertical DG FinFET. The experimental and simulated coupling coefficients in vertical DG and triple-gate FinFETs are compared for front-channel in Fig. 2-28b and for back-channel in Fig. 2-28c. Again the agreement is convincing, revealing the same trends. Electric potential (Fig. 2-28d) and field (Fig. 2-28e) profiles are shown for wide devices (W_F = 0.5 μm) with positive front-gate (V_{FG} = +1 V) and negative back-gate (V_{BG} = -10 V) biases. The body potential is higher, due to the stronger action of the top gate, in triple-gate than in vertical DG FinFET. In triple-gate FinFET, the vertical electric field from the top-gate to bottom blocks the penetration of the vertical electric field generated by the back-gate. Therefore, the effect of the back-gate on the front-channel characteristics is smaller in triple-gate FinFET. Since the front-channel coupling coefficient is reduced (Fig. 2-28b), a larger back-gate bias is needed to tune the front-channel threshold voltage. For exactly the same reason (*i.e.,* activation of the top section of the gate), the back-channel coupling shows the opposite behavior (Fig. 2-28c), being larger in triple-gate FinFET.

The impact of the fin height can be inferred by comparing measurements and simulations in triple-gate FinFET. The coupling rate for both the front- and back-channels is larger in experimental results (H_F = 20 nm) than in simulation results (H_F = 40 nm). This confirms that the special coupling effect in triple-gate FinFET (Fig. 2-26c) comes from combined actions of the top section of the gate and of thinner silicon film.

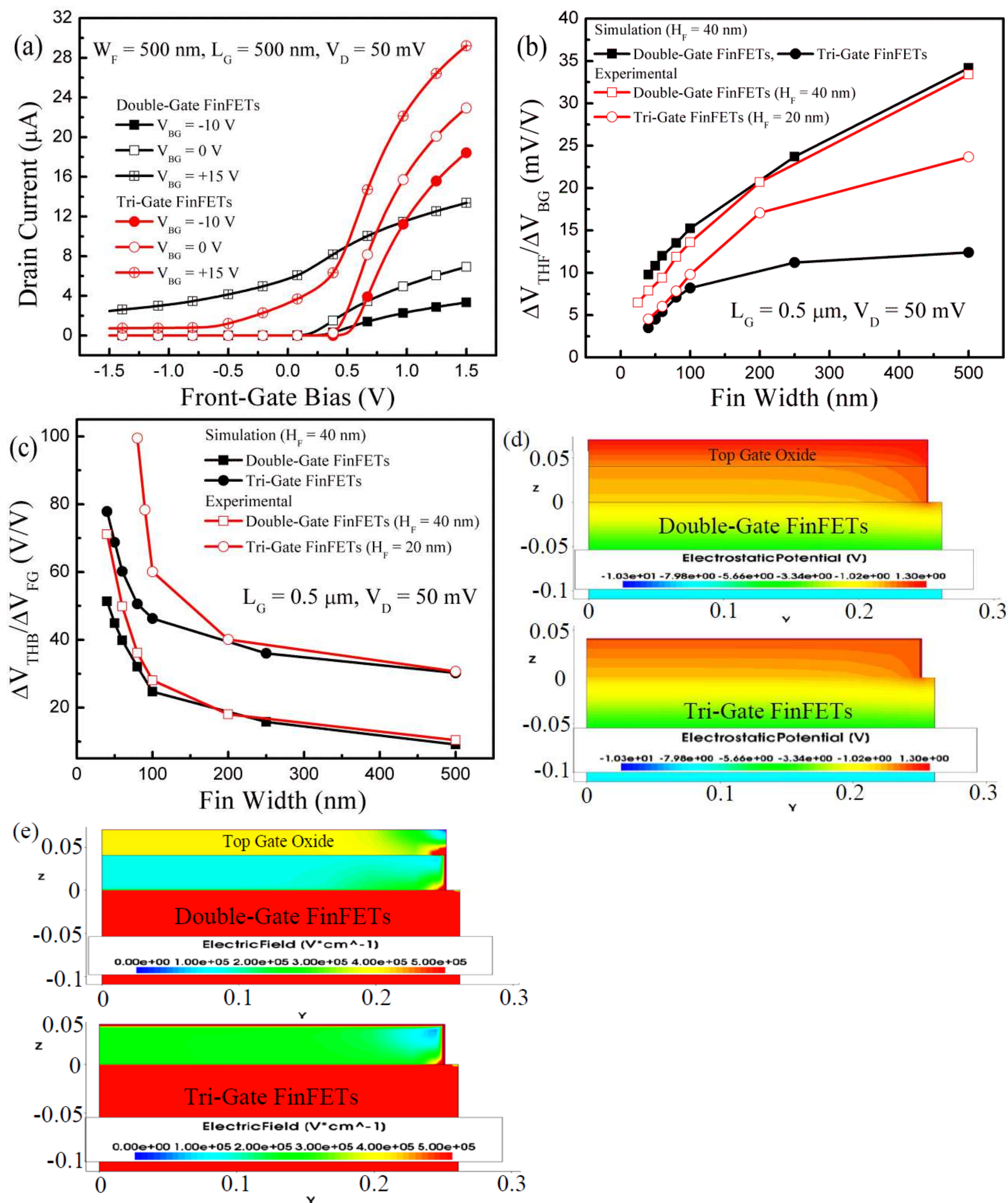

Fig. 2-28: Comparison of the simulated coupling effects in vertical DG and triple-gate FinFETs. (a) Drain current as a function of front-gate bias at different back-gate bias. (b) Front-channel and (c) back-channel coupling coefficient versus fin width comparing measurements and simulations. (d) Potential profile and (e) electric field profile in the body of DG and triple-gate FinFETs (V_{FG} = +1 V, V_{BG} = -10 V, W_F = 0.5µm).

In Fig. 2-29, we investigate the effect of the top-gate oxide thickness on the front-channel coupling in DG devices. The simulation conditions are the same as in Fig. 2-27, except the top-gate oxide layer thickness which varies from 30 nm (vertical DG FinFET)

down to 1.4 nm (triple-gate FinFET). In a wide fin, the front-channel coupling coefficient α decreases by a factor of 3. The coupling is stronger in devices with thicker top-gate oxide due to the reduction of the vertical electric field from top to bottom. The change in coupling efficiency from double-gate to triple-gate operation is less marked in narrower fins. The dotted line shows the coupling coefficient in FD planar device with 140 nm buried oxide, calculated with Eq. (2.31). Obviously, coupling effect is larger in planar device than in FinFETs. However, by using thicker top-gate insulator, we can enlarge the coupling effect which is an attractive solution for tuning the device performance via back-gate biasing.

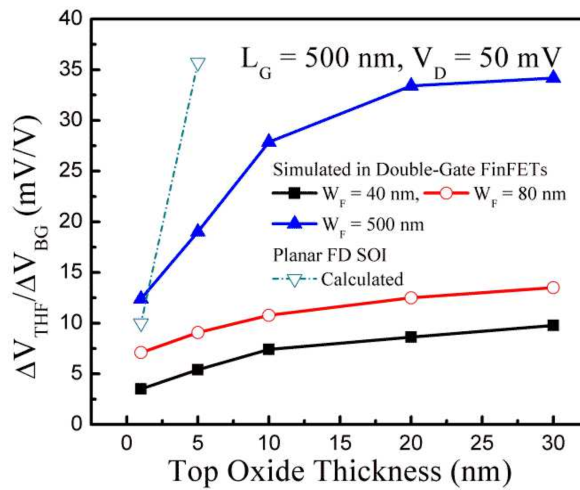

Fig. 2-29: Effect of the oxide thickness on the top of the body of DG transistors. Front-channel coupling coefficient as a function of the top oxide thickness for various fin widths.

2.2.4. Conclusion

The electrical properties of vertical DG FinFET were investigated. Good gate control by the two lateral-gates and high mobility were obtained. The 3D coupling effect between the lateral-gates and the back-gate was measured and simulated as a function of the fin width and device structure (double-gate or triple-gate FinFETs). A very good agreement was obtained between experimental, simulation and modeling results. In wider fin devices, the coupling of the front-channel to back-gate bias is increased whereas the opposite coupling effect (back-channel to front-gate bias) is decreased due to the gradual suppression of the lateral electric field. Thanks to the thick insulating layer at the top of the fin in vertical DG FinFET, the action of the vertical electric field from top to bottom is relaxed and the back-gate effect is enhanced. Therefore, vertical DG FinFETs are more sensitive to back-gate biasing than triple-gate FinFETs. The difference between these two transistor structures tends

to vanish in ultra-narrow fins. DG FinFETs with moderate fin width are suitable devices for dynamic threshold voltage control using thin BOX, ground plane and back-biasing schemes.

2.3. Mobility Behavior and Models for Nanocrystalline ZnO TFTs

We have studied ZnO TFTs because they attract high interest and operate like back-channel SOI MOSFETs. We applied our experimental methodology to investigate the carrier transport and reformulate the mobility models.

2.3.1. Introduction

Thin film transistors (TFT) are used in several applications such as the control circuits for large area display, flexible electronics and non-planar devices. The performance of TFTs based on amorphous Si or organic semiconductors is mostly limited by the poor electron mobility (0.1-1 cm^2/Vs) and insufficient control of threshold voltage. Nanocrystalline ZnO thin films are attractive for improving TFT performance to levels comparable to single crystal semiconductors. In the last decade, ZnO has generated interest due to its wide band-gap (E_g = 3.37 eV, supporting high electric fields and low leakage current) and its transparency to infrared and visible light, which makes it suitable for TFTs [80]. The recent improvement of deposition techniques led to good quality ZnO thin films as semiconducting material [87-90].

To improve the carrier mobility, several thin film deposition techniques have been used including Pulsed Laser Deposition (PLD), Atomic Layer Deposition (ALD), Chemical Vapor Deposition (CVD) and spin coating [89, 91-97]. Nevertheless, the carrier mobility was still not sufficient for high performance applications due to the large number of crystalline defects in the thin ZnO film [98]. To achieve high performance ZnO TFTs, not only must the quality of the ZnO layer be improved, but also attention should be paid to the properties of the gate insulator and interface [86, 99]. In this work, nanocrystalline ZnO thin films were formed by PLD on Plasma Chemical Vapor Deposited (PECVD) SiO_2 gate insulator to improve the carrier mobility [96, 99].

The carrier transport in a MOSFET channel is determined basically by drift/diffusion mechanisms. However, in nanocrystalline ZnO TFT, the grain boundary potential barrier, the grain size and the trap density at the boundaries affect the carrier transport. Several mobility models have been proposed in the past to account for the grain boundary effect in poly-Si TFT and ZnO TFT [100-105]. Although tested with numerical calculations, these models cannot reproduce the experimental results of the nanocrystalline ZnO TFT. Most of the proposed models for Si TFTs use curve fitting of experimental data to extract the device parameters. In shorter devices, hot electrons and enhanced effect of the contact resistance may impact the device performance [106]. Therefore, curve fitting method may lead to

unphysical parameter values and a possible lack of scalability of the model.

In this section, the carrier transport properties of nanocrystalline ZnO TFT are under investigations using low-temperature measurements. Based on the measurement data, simple mobility models are proposed to explain the carrier transport mechanism considering the effect of grain boundary and the mobility degradation due to surface carrier scattering at high field. The particular carrier transport mechanisms related to the grain boundary properties are explored with temperature-dependent measurements.

The proposed models are validated and benchmarked by comparison with experimental results and numerical calculations. We prioritized the models that enable simple parameter extraction methods from the experimental data. Key device characteristics such as threshold voltage, mobility and subthreshold slope were extracted and their variation at low temperature is reported.

2.3.2. ZnO TFT overview

In Si CMOS technology, performance improvement, low power consumption and cost reduction are driving forces. By contrast, thin film transistor (TFT) technology is appropriate for applications where low density circuitry is integrated across a large area [107]. Currently, hydrogenated amorphous silicon (a-Si:H) TFTs are dominatingly used for pixel drivers. However, threshold voltage instability and low mobility issues have generated interest in alternative such as metal oxide semiconductors.

(a) Properties of zinc oxide

ZnO is one of the best known II-VI compound semiconductors. For the last ten years, ZnO has gained sufficient attention as an attractive material for various applications due to its possibility to grow high-quality ZnO single-crystals and ZnO nanostructures. The recent interest in ZnO is motivated by various applications:

(i) *Transparent electronics*: The most desirable characteristic of ZnO is its wide band-gap (~3.4 eV). This corresponds to a wavelength of 365 nm which is in the near UV region. Therefore, ZnO is transparent to visible wavelengths and can be applied for the fabrication of transparent devices [108].

(ii) *Optical application*: ZnO is direct band-gap material with band-gap modulation (3~4 eV) available by alloying with magnesium and cadmium [109]. ZnO is

investigated for light-emitting diodes (LEDs) or laser diodes covering the blue and UV spectral range.

(iii) *Biosensing*: ZnO is non-toxic, environmentally friendly material, employed for biosensing applications or hybrid biological-semiconductor device concepts.

(iv) *Ferromagnets*: Doped ZnO is used to obtain a transparent room-temperature ferromagnet due to partial ionic bonding with magnetic impurities such as manganese, cobalt or nickel [110].

However, the relatively low mobility of ZnO is arguably its critical weakness. The typical maximum electron mobility (around 200 cm^2/Vs at room temperature) is much lower than that of conventional compound semiconductors [111].

(b) Thin film transistors

Hydrogenated amorphous silicon (a-Si:H) serves for inexpensive integration on a large-area substrate [112]. In 1972, amorphous silicon film prepared by the glow discharge decomposition of silane gas (SiH_4) was demonstrated by Spar and LeComber [112]. This amorphous silicon material is an amorphous silicon-hydrogen alloy including fairly large hydrogen concentration. The hydrogen atoms tie up a large amount of dangling bonds that are located in the amorphous silicon. Thus, the density of localized states is decreased in the energy gap. In the transport mechanism of amorphous Si:H, the localized states play a dominant role. Currently, a-Si:H TFTs are widely used for low cost, large area (several meters on a side) electronics and active matrix liquid crystal displays (AMLCD) [107]. They can be processed at low temperature (~ 250 °C), making them integrable on inexpensive substrate such as glass.

Fig. 2-30 shows a cross-sectional view of the basic TFT structure. The channel layer is a semiconductor such as a-Si, poly-Si, or ZnO. Source and drain contacts are formed at the top of the active layer. The gate electrode located at the bottom controls the transistor that is isolated from the active area by a thin dielectric film.

The device operation mechanism is basically same as conventional MOSFET. When the gate bias exceeds the threshold voltage V_{TH}, an inversion channel is induced in the active layer.

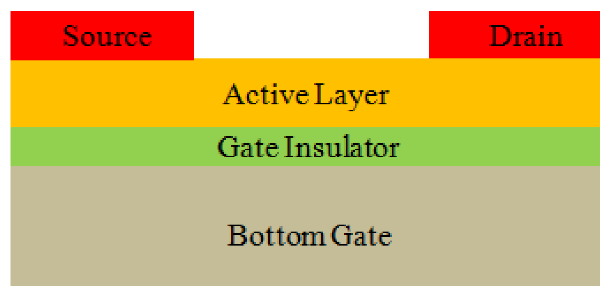

Fig. 2-30: Cross-section of a bottom gate TFT.

(c) ZnO thin film transistors

Combination of TFT structure and transparent material has a great interest in transparent electronics. The main reason is that the performance of transparent thin film transistors (TTFTs) will not be degraded with exposure to visible light unlike for amorphous or poly-Si TFTs [113]. High quality crystalline ZnO films (with good stability and mobility) can be grown at relatively low deposition temperature on amorphous glass substrate and are very suitable for TTFTs.

One of the earliest ZnO TFTs was demonstrated by Hoffman *et al.* [114]. Highly transparent ZnO TFT (around 75 % for visible light) was fabricated on glass (Fig. 2-31a). In order to form the bottom gate, a 200 nm thick layer of indium thin oxide (ITO) was sputtered. ITO was also used for source and drain electrode. A 220 nm thick layer of aluminum titanium oxide (ATO) was deposited by atomic layer deposition (ALD) as the gate insulator. ZnO active layer and ITO source/drain electrode were stacked by ion beam sputtering. The effective mobility and threshold voltage were modest: 0.45 cm^2/Vs and 10-15 V, respectively.

For low operating voltage and high mobility, ZnO TFTs fabricated on diverse gate dielectrics were reported by Carcia *et al.* (Fig. 2-31b) [115]. Heavily doped n-type wafer was employed as the bottom gate. HfO_2, $HfSiO_x$ and Al_2O_3 were deposited by ALD for the gate insulator (HfO_2 at 300 °C, $HfSiO_x$ at 400 °C, Al_2O_3 at 125, 200, 400 °C). All dielectrics were 25 nm thick except Al_2O_3 grown at 200 °C, for which the thickness was 100 nm. The 50 nm thick ZnO channel layer was grown by magnetron sputtering. To develop source and drain electrodes, Ti-Au (100 nm Au followed by 10 nm Ti) were patterned on the gate insulator by photolithography and evaporation.

Devices on HfO_2 scored a mobility of 12.2 cm^2/Vs, a threshold voltage of 2.6 V and a subthreshold swing of 0.5 V/decade. For 100 nm thick Al_2O_3 processed at 200 °C, ZnO TFT featured 17.6 cm^2/Vs mobility, 6 V threshold voltage and less than 0.1 nA gate leakage at 20 V. For the HfO_2 devices, the universal tendency is a lower threshold voltage, but a higher gate

leakage current.

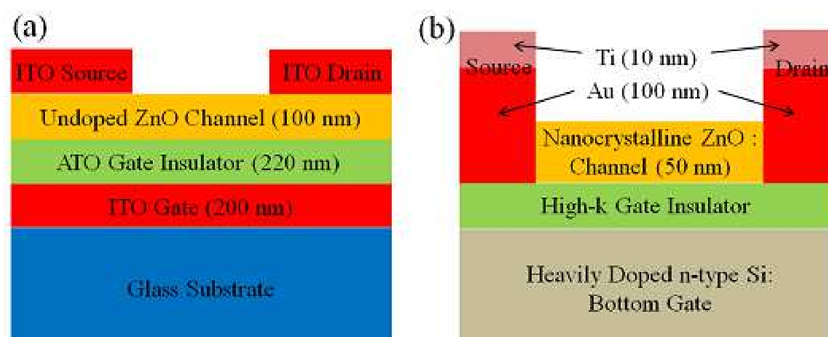

Fig. 2-31: Cross-section of ZnO TFT structures reported by (a) Hoffman *et al*. [114] and (b) Carcia *et al*. [115].

(d) ZnO deposition technology

As described above, low mobility was the main weakness of ZnO TFT for high performance applications. In order to improve mobility, high quality ZnO layer and interface between the ZnO and gate insulator are the critical factors. In this perspective, many ZnO deposition techniques have been studied.

(i) *RF magnetron sputtering*: DC, RF and reactive sputtering is one of the most popular ZnO growth technique. Especially, magnetron sputtering is frequently used due to its low temperature, low cost and simple processing [116]. Normally, ZnO film is grown by using a high-purity ZnO target in the ambient with $Ar+O_2$ at a pressure of 10^{-3}~10^{-2} Torr [109]. The RF power applied to the plasma is tuned to regulate the sputtering speed. Ar is the sputtering enhancing gas and O_2 acts as the reactive gas. Post-deposition annealing is commonly performed to reduce the stress and improve optical properties of the sputtered ZnO film [117].

(ii) *Molecular Beam Epitaxy (MBE)*: The advantages of MBE are the capability of precise control over the deposition parameters and in situ diagnostics [118]. Typically, Zn metal and O_2 are used as source materials. The processing temperature determines the growth rate and material properties.

(iii) *Chemical Vapor Deposition (CVD)*: CVD is an interesting method for uniform large-area films. ZnO deposition occurs as a result of chemical reactions of vapor-phase precursors on the substrate which are delivered to the growth zone by the carrier gas. In general, dimethyl zinc [$(CH_3)_2Zn$] (DMZ) or diethyl zinc [$(C_2H_5)_2Zn$] (DEZ) is combined with oxygen as a source material [119]. However, DEZ and DMZ easily react with oxygen, degrading the ZnO film quality. Improved ZnO film can be

formed by using special reactor design and mixing less-reactive precursors (zinc acetylacetonate) with oxygen [120].

Plasma enhanced CVD (PECVD) technique can also be utilized [121]. A film densification process induced by plasma bombardment and UV ray irradiation allows enhancing the quality of ZnO layers. Indeed, the reactants are decomposed by the plasma (not by thermal energy). Thereby, PECVD does not require a high temperature environment and make it possible to prepare ZnO film on organic material for flexible substrate [122].

(iv) *Atomic layer deposition (ALD)*: At relatively low temperature, ALD technique enables the growth of ZnO on large area flexible substrate [123] despite deposition rate is relatively low. A typical ALD process is composed of three steps: a metal precursor adsorption step, a purge step and finally exposure step to an oxidant to complete a single deposition cycle.

(v) *Pulsed Laser Deposition (PLD)*: PLD is a relatively simple deposition technique [124]. Thin film is obtained by vaporizing a material using high-energy laser pulses. This technique is suitable for high quality film and fabrication of discrete devices. Sintered ceramic targets, most commonly used for ZnO thin film deposition, are transferred instantaneously leading to a stoichiometic and non stoichiometic deposition.

2.3.3. Typical properties of our ZnO TFTs

Pulsed laser deposition (PLD) at low temperature (200 °C) [86] was used to grow our 50 nm thick nanocrystalline ZnO films. The 30 nm thick back gate oxide, separating the ZnO layer from Si substrate, was deposited by PECVD at 250 °C. The bottom gate is used to drive the drain current. The device operation is similar to back-channel SOI MOSFETs or pseudo-MOSFETs [125]. Ti/Au metal was stacked on top of the ZnO layer to form the source and drain. Each transistor design contains several fingers (N_F = 4-20) and features different gate widths and lengths to assess the effect of the geometrical parameters. Fig. 2-32 shows a schematic drawing of a typical nanocrystalline ZnO thin film transistor and a Transmission Electron Microscope (TEM) cross-sectional image of the transistor channel region. As seen in Fig. 2-32b, thin films consist of closely packed nanocolumns of ZnO with 30-50 nm diameters. ZnO nanocolumns were oriented in (002) direction as determined by X-ray

diffraction method [99].

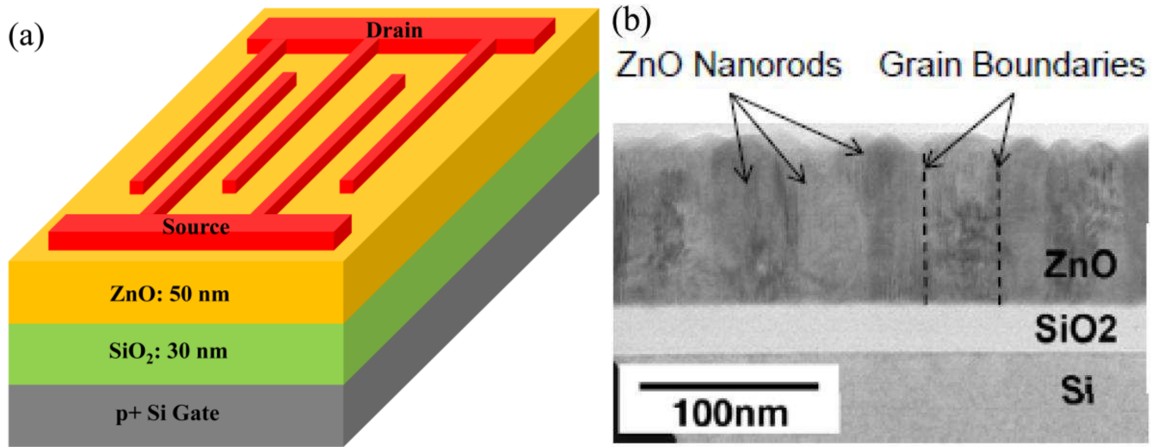

Fig. 2-32: (a) Device structure and (b) TEM cross-section image of nanocrystalline ZnO thin film transistor.

Fig. 2-33 shows the basic electrical characteristics of a nanocrystalline ZnO TFT measured at room temperature. These results indicate very promising properties: relatively low (and positive) threshold voltage (Fig. 2-33a), reasonable subthreshold swing and high ON/OFF current ratio (Fig. 2-33b). In amorphous or nanocrystalline materials, the definition of threshold voltage is different than in standard MOSFETs. In non-crystalline devices, such as amorphous-Si TFTs, the threshold voltage is estimated by extrapolating the linear plot of I_D vs. V_G curve measured at low drain bias (Fig. 2-33a) [126]. This is different from the threshold voltage determination using extrapolation of the $\sqrt{I_D}$ vs. V_G curves for MOSFETs operated in saturation (high V_D).

The peak value of the transconductance curve in Fig. 2-33c indicates a high mobility in these devices. A hump in the transconductance curve is observed for gate voltage of about 1 V due to the effect of the grain boundaries. The origin of the transconductance hump will be discussed in relation with Fig. 2-34.

The effective mobility μ_{eff} in amorphous TFTs is a function of the band mobility and of the number of trap states which are actually filled in the conduction band: $\mu_{eff} = \mu_n \cdot n_{free}/(n_{free}+n_{trapped})$, where μ_n is the band mobility (or the mobility in the extended states), n_{free} is the free electron concentration at SiO_2-ZnO interface and $n_{trapped}$ is the concentration of trapped electrons in the grain boundary. The effective mobility μ_{eff} is a weak function of the gate voltage in the subthreshold regime [100]. Indeed, both n_{free} and $n_{trapped}$ increase with increasing gate voltage, hence the factor $n_{free}/\left(n_{free}+n_{trapped}\right)$ is almost bias-independent.

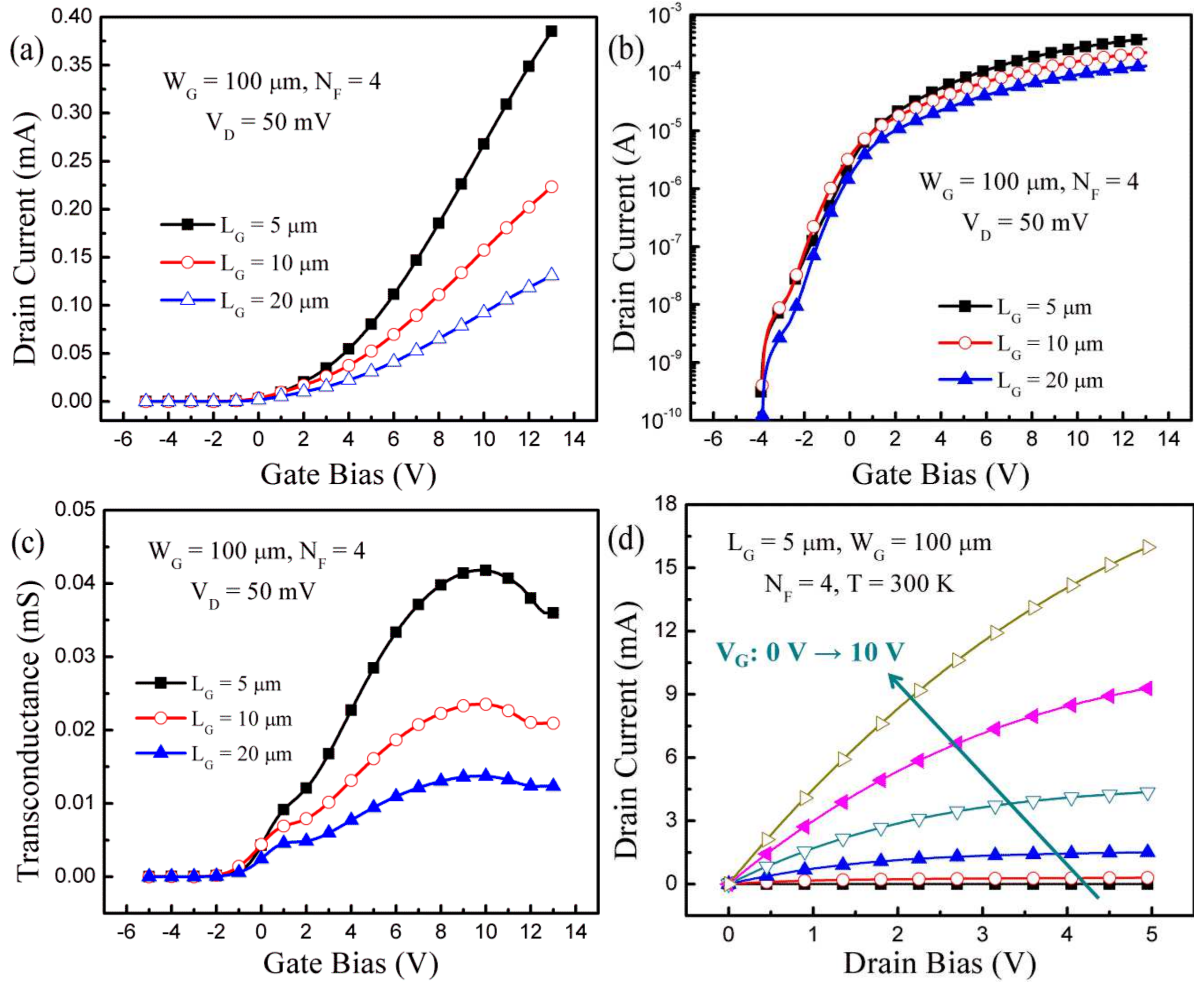

Fig. 2-33: Basic characteristics at room temperature. (a) Linear and (b) log scale drain current versus gate bias and gate length. (c) Transconductance as a function of gate bias and gate length. (d) Drain current as a function of drain bias.

For nanocrystalline TFTs, the mobility is significantly dependent on gate voltage because the $n_{trapped}$ states become filled at a much lower V_G and the number of filled n_{free} states increases roughly linearly with V_G. Thus, the TFT behaves similarly to a crystalline-Si MOSFET and [$n_{free} = (\varepsilon_{OX}/q \cdot T_{OX}) \cdot (V_G - V_{TR})$], where q is the electron charge; ε_{ox} and T_{ox} are the permittivity and thickness of the gate dielectric. V_{TR} is called the transitional threshold voltage and is approximately the point where all $n_{trapped}$ become filled. Hence, the mobility is quasi linearly dependent on the gate voltage, $\mu_{eff} = \mu_n \cdot M \cdot (V_G - V_{TR})$, where M is a constant coefficient [127]. This relationship holds until $n_{free} >> n_{trapped}$ when μ_{eff} reduces essentially to μ_n. Dosev reported a mobility of about $\mu_n \sim 1$ cm^2/Vs for nanocrystalline Si TFTs, dominated by the grain boundaries [128]. However, our devices behave more like a conventional MOSFET, in particular at low temperature where the traps are filled; the hump disappears and

the mobility is far higher than in amorphous or polycrystalline ZnO TFTs [129, 130].

For shorter devices, the drain current level and the transconductance peak value increase and show channel length modulation with the drain bias. Fig. 2-33d shows the measured $I_D(V_D)$ characteristics where no kink effect [131] is observed. In other words, the device is fully depleted (FD) at room and lower temperature. It can be expected from these experimental results (high transconductance, low threshold voltage) that a good quality interface exists between ZnO film and gate insulator.

As we mentioned above, the device operation properties look very similar with those in FD SOI MOSFETs. Threshold voltage roll-off is observed for shorter gate lengths. However, the temperature influence on the device properties is different. The origin of the difference in device performance between FD MOSFETs and our ZnO TFTs comes from the effect of the grain boundaries. This effect strongly depends on temperature and should be considered for the modeling of nanocrystalline ZnO TFT.

The temperature dependence of the drain current is shown in Fig. 2-34, which indicates that the current level increases slightly at higher temperatures. On the other hand, the comparison of Fig. 2-33c (300 K) and Fig. 2-34b (77 K and 300 K) shows that the field-effect mobility, deduced from the transconductance curve (μ_{FE} ~ g_m), also increases at higher temperature. This behavior is opposite of the usual mobility behavior found in SOI devices, where the threshold voltage and mobility increase as the temperature is lowered (see Chapter 2.1).

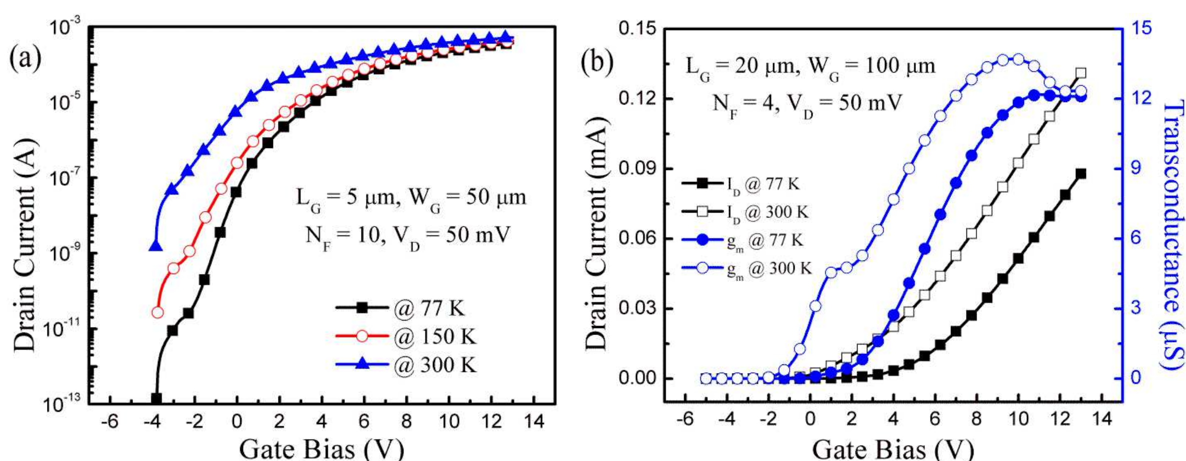

Fig. 2-34: Temperature-dependent characteristics of ZnO TFT. (a) Drain current versus gate bias and temperature. (b) Drain current and transconductance versus gate bias at 77 K and 300 K.

Similarly to the activation of the back-channel in SOI MOSFETs [132], a parasitic

channel hump can be observed in transconductance (see Fig. 2-33c). However, in nanocrystalline ZnO TFTs, this hump is due to the grain boundaries. This "parasitic" channel (or hump) is easily activated by increasing the thermal energy and therefore can be observed at room temperature (Fig. 2-34b, 300 K). As the temperature decreases, the hump in the transconductance decreases and totally vanishes below 100 K (Fig. 2-34b).

In section 2.3.5., the temperature dependence of the mobility, threshold voltage and subthreshold slope will be discussed in details (Fig. 2-40, 2-41, 2-42) with respect to the extraction methods described in the next section.

2.3.4. Parameter extraction methods

Many techniques for parameter extraction in bulk Si, amorphous Si, poly-Si and SOI FETs have been documented in the literature. After examining their capability to match the experimental data in our ZnO TFTs, four mobility models were retained and further developed. Other techniques were found to be either unfit to reproduce the measurements or contained too many adjustable parameters for a meaningful interpretation of mobility behavior.

(a) Y-function method

Y-function parameter extraction technique [46] addressed in Chapter 2.1.2 has been tested for ZnO TFTs. Fig. 2-35 shows the Y-function and the transconductance at 77 K. The tangent in strong inversion regime, where the effective mobility Eq. (2.2) holds, provides a threshold voltage of about 6 V, higher than expected from the turn-on $I_D(V_G)$ characteristics of Figs. 2-33 and 2-34. The MOSFET threshold voltage can also be evaluated from the linear extrapolation of $I_D(V_G)$ or, more accurately, from the peak of the second derivative of the current [45, 133]. Figs. 2-33 and 2-34 show that the positions of g_m inflection point and extrapolated V_{TH} tend to coincide.

Normally, the difference between transconductance peak voltage and threshold voltage is less than 1 V in Si MOSFETs and even in back-channel SOI MOSFETs. However, in ZnO TFT, there is a much larger gap (~ 6-8 V at 77 K and 300 K, Figs. 2-34b and 2-33c) between these voltages, which cannot be reproduced with Eqs. (2.1) and (2.2).

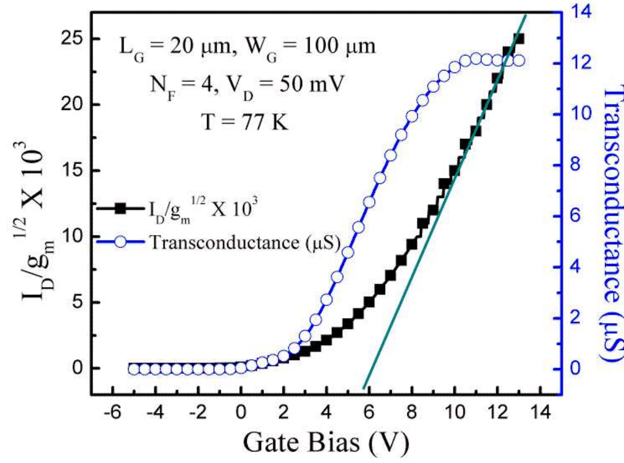

Fig. 2-35: Classic *Y-function*, $I_D/\sqrt{g_m}$, and transconductance versus gate bias at 77 K.

In other words, the *Y-function* technique cannot be used to extract accurate parameters despite the device operation mechanisms look similar in ZnO TFT and SOI MOSFET. This technique is unable to reproduce the large gap between the transconductance peak position and threshold voltage at either low temperature or at room temperature. Therefore, conclusion is that a different mobility model is required for the nanocrystalline ZnO TFTs.

(b) Modified Y-function method

A variant of the *Y-function* technique has been proposed for SOI MOSFETs operated in strong inversion regime and at low-temperature.

The effective mobility model was modified as [134]:

$$\mu_{eff} = \frac{2\mu_0}{\frac{Q_{inv}}{Q_0} + \frac{Q_0}{Q_{inv}}} = \frac{2\mu_0 \theta_m (V_G - V_{TH})}{1 + \theta_m^2 (V_G - V_{TH})^2} \tag{2.33}$$

where $Q_{inv} = C_{ox}(V_G\text{-}V_{TH})$ is the inversion charge, Q_0 is a critical charge and $\theta_m = C_{ox}/Q_0.$

The drain current Eq. (2.1) in ohmic regime becomes [70]:

$$I_D = 2\frac{W}{L} C_{ox} V_D \mu_0 \theta_m \frac{(V_G - V_{TH})^2}{1 + \theta_m^2 (V_G - V_{TH})^2} \tag{2.34}$$

The resulting transconductance equation is

$$g_m = \frac{\partial I_D}{\partial V_G} = 4\frac{W}{L} C_{ox} V_D \mu_0 \theta_m \frac{V_G - V_{TH}}{\left[1 + \theta_m^2 (V_G - V_{TH})^2\right]^2} \tag{2.35}$$

The derivative of the transconductance Eq. (2.35) yields the transconductance maximum $g_{m,max}$ value:

$$g_{m,\max} = \frac{3\sqrt{3}}{4}\frac{W}{L}C_{ox}V_D\mu_0 \qquad for\ V_G - V_{TH} = \frac{1}{\sqrt{3}\theta_m} \tag{2.36}$$

This model is able to match our experimental results. Fig. 2-36a shows a convincing numerical fit, using Eq. (2.34), of the measured $I_D(V_G)$ characteristics. The calculated and measured $g_{m,max}$ values are almost the same and, more importantly, the difference between V_{TH} and g_m peak voltage is accurately reproduced.

The *Y-function* [46, 70], *Y*, becomes:

$$Y = \sqrt{\frac{W}{L}C_{ox}V_D\mu_0\theta_m} \cdot (V_G - V_{TH})^{3/2} \tag{2.37}$$

The idea of this alternative extraction method consists in constructing a simple linear function by the proper combination of Eqs. (2.34) and (2.35). This is achieved by dividing the current squared by the transconductance and then by taking the cubic root.

To extract the parameters, we use the *modified Y-function*, Y_m, defined as:

$$Y_m = \left(\frac{I_D}{\sqrt{g_m}}\right)^{2/3} = \left(\frac{W}{L}C_{ox}V_D\mu_0\theta_m\right)^{1/3}(V_G - V_{TH}) \tag{2.38}$$

Fig. 2-36b shows the $Y_m(V_G)$ curve composed with the experimental results. It features a wide linear region, corresponding to Eq. (2.38) and useful for extracting the parameters. Similarly with the *Y-function* method, threshold voltage is the intercept point with X-axis and the mobility is extracted from the slope of the $Y_m(V_G)$ curve. Coefficient θ_m is determined from the gate voltage corresponding to the transconductance peak (Eq. (2.36)). Table 2.1 confirms that the parameters extracted with $Y_m(V_G)$ from the experimental data are essentially identical to those resulting from the numerical fit of the measured $I_D(V_G)$ curve (Fig. 2-36a).

Table 2.1. Comparison between the parameters extracted from the experiment with the *modified Y-function* and those resulting from the numerical fit of $I_D(V_G)$ curves in Fig. 2-36a (L_G = 20 µm, W_G = 100 µm, N_F = 4).

	θ_m	V_{TH} (V)	μ_0 (cm^2/Vs)
Extracted @ 77 K	0.072	3	79
Calculated @ 77 K	0.075	2.8	75

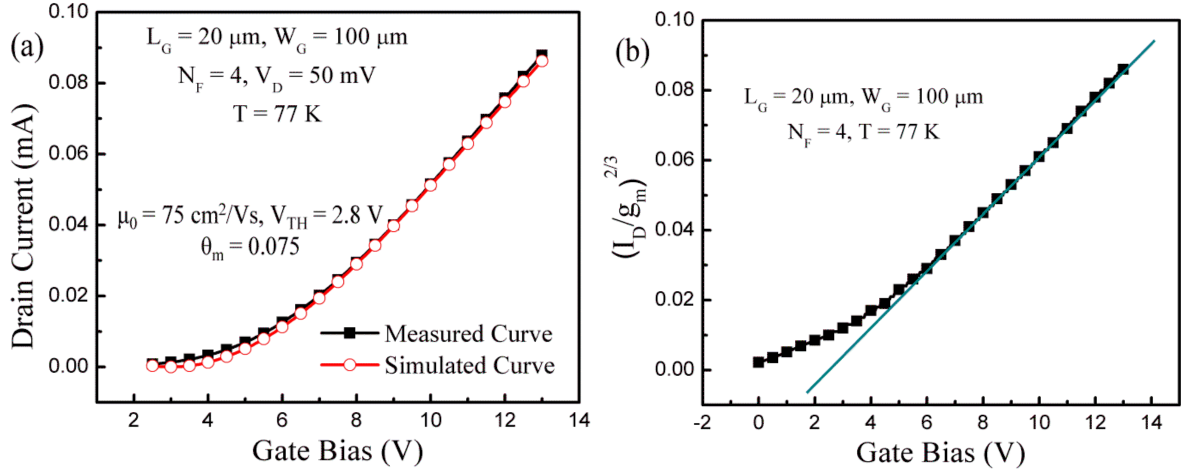

Fig. 2-36: (a) Measured and calculated drain current versus gate bias at 77 K. *Modified Y-function* model is used for the calculated drain curve. (b) Y_m curve calculated from measured data versus gate bias at 77 K.

This comparison validates the *modified Y-function* extraction technique. Nevertheless, this model does not consider the grain boundary effect, hence its application to nanocrystalline ZnO TFTs cannot be justified. Physics-based mobility models, which account for the grain boundaries, are presented in the following.

(a) Revised Shur's model

When several distinct conduction mechanisms govern the carrier transport, they can be combined according to Matthiessen's mobility law. Shur *et al*. [100] have originally proposed the following expression for the effective mobility in poly-Si TFTs:

$$\frac{1}{\mu_{eff}} = \frac{1}{k(V_G - V_{TH})^m} + \frac{1}{\mu_0} \tag{2.39}$$

where $k = 3.4$ cm^{2}V$^{-3.7}$s^{-1} and m = 2.7 are respectively the low-field constant and exponent of the power-law mobility, and μ_0 is the drift mobility. This equation predicts the saturation of the effective mobility at high V_G, which is not the case in ZnO TFTs. We propose a revised model which includes the mobility degradation at high vertical field:

$$\frac{1}{\mu_{eff}} = \left[\frac{1}{k(V_G - V_{TH})^m} + \frac{1}{\mu_0}\right]\left[1 + \theta(V_G - V_{TH})\right] \tag{2.40}$$

Coefficient θ summarizes the contributions of surface scattering and series resistance.

In this model, we take into account the regular carrier transport mechanism (via μ_0) as well as the variable effect of grain boundaries thanks to k and m coefficients, which have to be determined for each TFT. As shown in Fig. 2-37a, this revised mobility model was validated by fitting the experimental curve with Eq. (2.40) and the parameters listed in Table

2.2.

The device parameters can actually be determined without curve fitting. The proposed extraction method proceeds in two steps separating the dominant carrier transport mechanisms according to the gate bias regions.

Step 1. In the *low-field region*, the conduction mechanism is governed by the grain boundary activation. The power-law mobility was considered and the second term in the square brackets of Eq. (2.40) was neglected. The mobility degradation factor can also be ignored at this stage.

Eq. (2.40) simplifies to the following approximation:

$$\frac{1}{\mu_{eff}} \cong \frac{1}{k(V_G - V_{TH})^m} \tag{2.41}$$

The drain current and transconductance equations are given by:

$$I_D = Ak(V_G - V_{TH})^{m+1} \qquad \text{with } A = \frac{C_{ox}WV_D}{L} \tag{2.42}$$

and

$$g_m = Ak(m+1)(V_G - V_{TH})^m \tag{2.43}$$

Eqs. (2.42) and (2.43) yield:

$$\frac{I_D}{g_m} = \frac{1}{m+1}(V_G - V_{TH}) \tag{2.44}$$

From the Eq. (2.44), the tangent was plotted at low V_G as shown in Fig. 2-37b. From the slope of the linear I_D/g_m curve, the coefficient m was extracted. The intercept point with X-axis yields the threshold voltage. The coefficient k is calculated with the drain current value at V_G-V_{TH} = *1 V*, as suggested in Eq. (3.42).

Step 2. In the *high-field region*, the dominant effect on the carrier transport is regular drift-diffusion. Therefore, the first term in the square brackets in Eq. (2.40) is neglected, whereas the mobility attenuation factor has to be considered.

Eq. (2.40) takes the form:

$$\frac{1}{\mu_{\text{eff}}} \cong \frac{1+\theta(V_G - V_{TH})}{\mu_0} \tag{2.45}$$

The drain current equation is calculated with the Eq. (2.45):

$$\frac{1}{I_D} = \frac{1}{A\mu_0 (V_G - V_{TH})} + \frac{\theta}{A\mu_0} \tag{2.46}$$

The differentiation of Eq. (2.46) leads to the *high-field Y-function*:

$$\left[\left(-\frac{1}{I_D}\right)'\right]^{-0.5} = \frac{I_D}{\sqrt{g_m}} = Y = \sqrt{A\mu_0}(V_G - V_{TH}) \tag{2.47}$$

As shown in Fig. 2-37c, the experimental $Y(V_G)$ curve is indeed linear for $V_G > 8$ V. The mobility μ_0 is extracted from the slope.

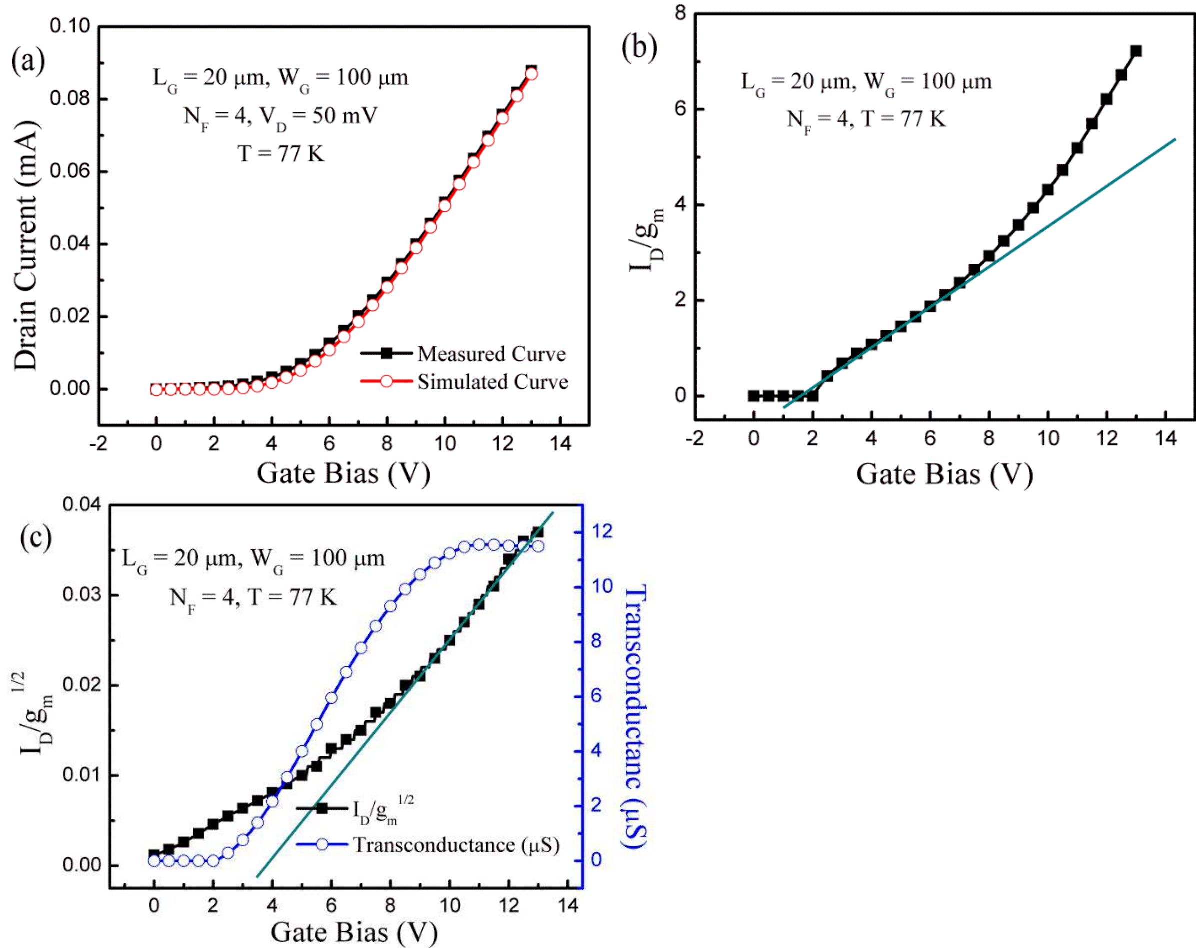

Fig. 2-37: (a) Measured and calculated drain current versus gate bias at 77 K. The revised Shur's model of Eq. (2.40) and the parameters listed in Table 2.2 were used for the calculated drain current. (b) I_D/g_m (V_G) and (c) $I_D/\sqrt{g_m}(V_G)$ curves composed with the experimental data. The lines show the linear extrapolations corresponding to Eqs. (2.44) and (2.47), respectively.

The mobility attenuation factor θ is determined by plotting $1/\sqrt{g_m}$

$$\frac{1}{\sqrt{g_m}} = \frac{1}{\sqrt{A\mu_0}}\left[1 + \theta(V_G - V_{TH})\right]$$

(2.48)

which also depends linearly on V_G at high field.

In order to confirm the validity of this method, the parameters extracted analytically with those resulting from numerical curve fitting are compared in Table 2.2. The agreement is good for coefficient *k* and very good for all other parameters.

Table 2.2. Comparison between the parameters extracted from the experiment with our revised Shur's model and those resulting from the numerical fit of $I_D(V_G)$ curves in Fig. 2-37a (L_G = 20 μm, W_G = 100 μm, N_F = 4).

	M	k	θ	V_{TH}	μ_0
Calculated @ 77 K	2.1	1.5	0.0025	1.5 V	95 cm^2/Vs
Extracted @ 77 K	2.2	2	0.0022	1.4 V	92 cm^2/Vs
Extracted @ 300 K	2.15	3.4	0.03	0.8 V	125 cm^2/Vs

(d) Revised Babis' model

Extending Levingson's work [135], Farmakis *et al.* [136] have proposed an exponential mobility (Babis' model) which accounts for the effect of grain boundaries at low field:

$$\mu_{GB} = \mu_g \cdot \exp\left(-\frac{q}{kT} \frac{t_{ZnO}}{\varepsilon_{ZnO}} \frac{(qN_{GB})^2}{8C_{ox}(V_G - V_0)} \right) \tag{2.49}$$

where μ_g is the grain-related mobility, N_{GB} is the number of grains, kT/q is the thermal energy, t_{ZnO} is the ZnO layer thickness and ε_{ZnO} is its permittivity.

Our approach is to simplify this model by reducing the number of parameters and adding the mobility degradation factor θ. The final expression for the effective mobility we propose is:

$$\frac{1}{\mu_{eff}} = \left[\frac{1}{\mu_g e^{-\frac{q}{kT} \bullet \frac{S}{V_G - V_{TH}}}} + \frac{1}{\mu_0} \right] [1 + \theta(V_G - V_{TH})] \tag{2.50}$$

where μ_g and S summarize the impact of grain boundaries and μ_0 is the inter-grain mobility.

As demonstrated in Fig. 2-38 by the comparison of measured and calculated $I_D(V_G)$ curves, this model is capable of correctly reproducing the experimental results. We attempted to develop a two-step extraction procedure similar to that exposed for the revised Shur's model. Unfortunately, at low V_G, the exponential dependence of the mobility makes the parameter extraction more complicated. No convincing analytical treatment, comparable with

Eqs. (2.41-2.44), could be devised for the low-field region. However, using numerical curve fitting (more or less accurate according to the V_G region used for extraction), we obtain parameter values comparable with those extracted with the previous models.

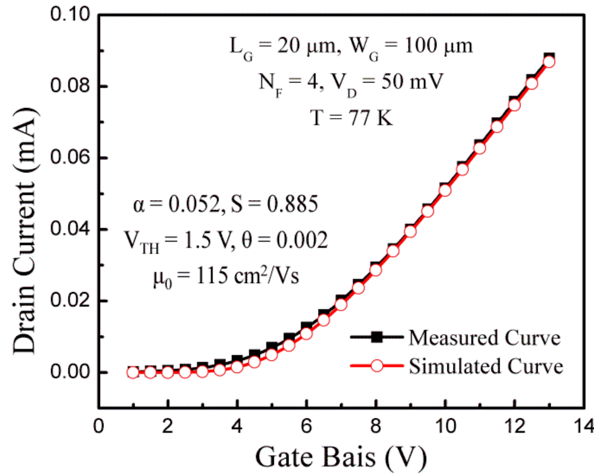

Fig. 2-38: Measured data and calculated $I_D(V_G)$ curve using the revised Babis' model of Eq. (2.50).

At high V_G, the exponential mobility term becomes negligible and we recover the case described by Eqs. (2.45-2.48).

2.3.5. Temperature-dependent characteristics

The proposed models and extraction methods have been applied to experimental data collected in a wide range of temperatures. We discuss the temperature dependent behavior of the main TFT parameters (subthreshold swing, threshold voltage and mobility) in the following.

(a) Subtreshold swing

Fig. 2-39 shows the subthreshold swing (*SS*) determined from the *Log* $I_D(V_G)$ curves between hump and threshold voltage. The swing decreases slowly with temperature, from 700 mV/decade at room temperature to less than 600 mV/decade at 77 K. The sub-linear *SS(T)* variation can be explained by the usual increase of the density of interface traps at low temperature and especially by the grain boundary action. The swing is large in TFTs compared to advanced MOSFETs mainly because the buried oxide is very thick (30 nm). Similar *SS* values are actually obtained by operating the back channel of fully depleted SOI

MOSFETs with thick BOX [137].

The subthreshold voltage swing values indicate a reasonable interface trap density (D_{it} < 10^{12} $cm^{-2}eV^{-1}$), calculated from: $SS \approx 2.3(kT/q)\cdot(1+qD_{it}/C_{ox})$. In this simplified relation, the coupling between the buried channel and the top surface ZnO defects is neglected which means that D_{it} is actually overestimated. Pseudo-MOSFET results in thin-film SOI wafers show that the defects at unpassivated surface (case of our ZnO TFTs) can dominate the swing value [138]. Nevertheless, the relatively low density of traps gives evidence of the good quality of the ZnO film and ZnO-SiO_2 interface.

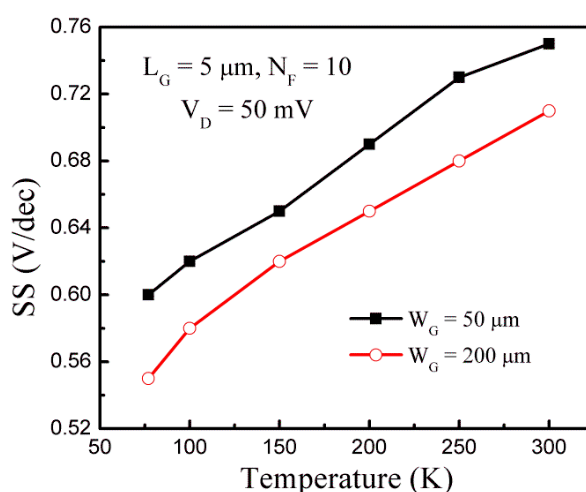

Fig. 2-39: Subthreshold swing versus temperature and gate width.

As shown in Fig. 2-33, an additional conduction mechanism is evident below the threshold voltage leading to humps in drain current and transconductance. Such humps reveal a parasitic channel behaving like the activation of the opposite channel in fully depleted SOI MOSFETs. However, in nanocrystalline ZnO TFT, the parasitic channels are formed along and across the grain boundaries [139]. Indeed, the grain boundaries have strong impact on the device operation in the subthreshold regime. The parasitic current paths are easily activated by increasing the thermal energy of free carriers. This is why the hump is notorious at room temperature and disappears at 77 K.

(b) Threshold voltage

Fig. 2-40 shows the threshold voltage obtained with two proposed parameter extraction methods. V_{TH} decreases at high-temperature same as in a bulk-Si and FDSOI devices (Fig. 2-17b). Indeed, the effect of the grain boundary potential barrier is also decreased when the

supply of the thermal energy increases at high temperature. The threshold voltage rate-of-change with temperature ($\Delta V_{TH}/\Delta T \approx 2.5$ mV/K) is small compared to back-channel SOI MOSFETs and can be further reduced by using thinner oxides and/or high-k dielectrics. This limited shift in V_{TH} indicates that the characteristics of nanocrystalline ZnO TFTs are relatively stable against variations in temperature, which is attractive for applications.

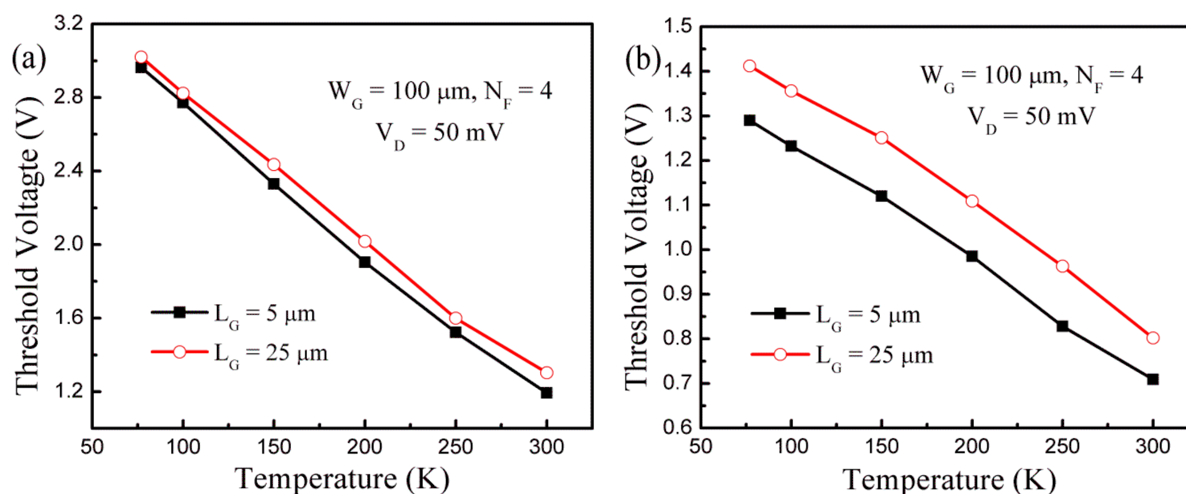

Fig. 2-40: Threshold voltage versus temperature and gate length. (a) *Modified Y-function* and (b) revised Shur's model were used for the extraction.

(c) Mobility

The mobility variation with temperature is informative about the carrier transport and scattering mechanisms. At low temperature, the dominant scattering process in MOSFETs is the Coulomb scattering due to ionized bulk impurities and surface defects [140]. As the temperature increases, the dominant scattering mechanism changes from Coulomb to phonon scattering. Therefore, the mobility is normally expected to decrease as the temperature rises from 100 K to room temperature as a result of phonon scattering with higher thermal energy. However, an opposite behavior is observed in nanocrystalline ZnO TFT.

Fig. 2-41 shows the mobility variation with temperature as obtained with our extraction techniques. The mobility is improved at room temperature despite the enhancement of phonon scattering. It follows that the transition from Coulomb-dominated to phonon-dominated scattering cannot be observed in nanocrystalline ZnO TFT. This difference between ZnO TFTs and SOI MOSFETs originates from the nanocrystal grain boundaries. In TFTs, the carriers have to cross the grain boundary potential barrier in order to contribute to the drain current. A higher thermal energy makes it easier for electrons to overcome the grain boundary potential barrier. As a result, the mobility increases at high-temperature.

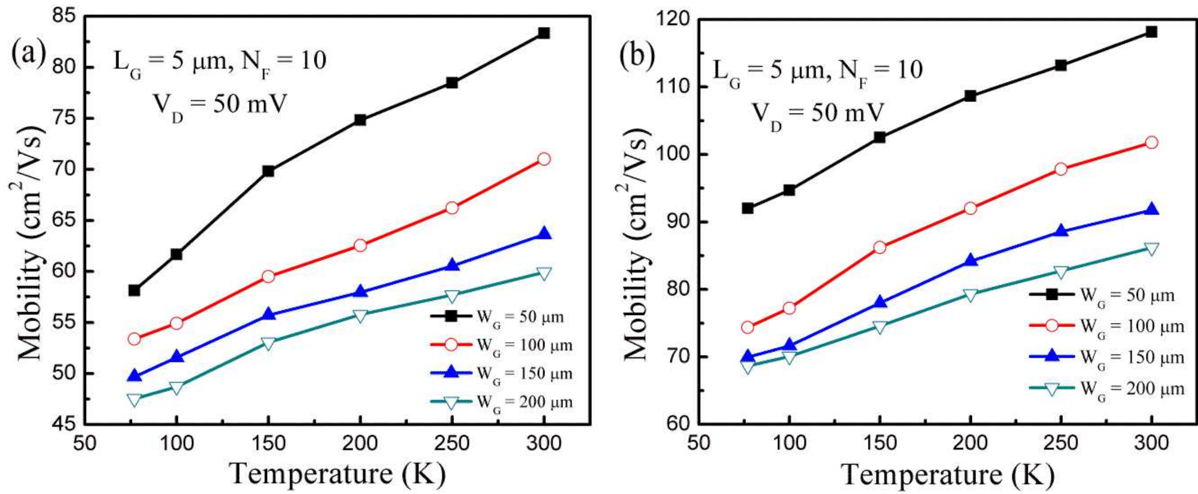

Fig. 2-41: Mobility versus temperature and gate width. (a) *Modified Y-function* and (b) revised Shur's model were used for mobility extraction.

2.3.6. Conclusion

We have investigated the electrical properties of the ZnO TFT in a wide temperature range in order to clarify the transport mechanisms. Fully depleted nanocrystalline ZnO TFT with bottom-gate structure shows very promising properties: high ON/OFF current ratio and carrier mobility (~ 100 cm^2/Vs which can be further improved by proper surface cleaning and passivation [86]), reasonable subthreshold slope (0.6 V/decade, to be minimized with thinner high-K dielectrics), and relatively small variations with temperature. These results all point on the good quality of the interface between ZnO and SiO_2 layers.

From the low-temperature measurements, appropriate mobility models and simple parameter extraction methods have been proposed for ZnO TFTs. These models and methods have been tested from 77 K to 300 K. Convincing curve fitting and reasonable parameters have been obtained with our models. The revised Shur's model (Eq. (3.40)), which considers the grain boundary effect, is reliable and easy to implement.

Chapter 3:

Magnetoresistance Measurements and Unusual Mobility Behavior in FD SOI MOSFETs

In this chapter, we show how the coupling effects can impact the carrier mobility behavior. In order to avoid any debate on the accuracy of mobility evaluation, we have selected the magnetoresistance technique.

3.1. Introduction

Advanced planar MOSFET and FinFET transistors fabricated on SOI wafers, which will sustain CMOS scaling, have been characterized under high magnetic field. In transistors with very thin and short body, the carrier mobility is a complex parameter because several channels, gates and interfaces coexist and interact. It has been shown that the effective mobility (i) can be enhanced by appropriate back-gate biasing [141], (ii) is different at front, back and sidewalls interfaces [142], and (iii) basically departs from the 'universal mobility' law [143].

In parallel, an interesting debate develops on the accuracy of mobility characterization. In short MOSFETs, series resistances impede the transconductance whereas parasitic capacitors affect the split-CV method. All techniques but one rely on critical assumptions like effective channel length and width, equivalent oxide thickness and dielectric constant, film and BOX thickness, etc. The exception is the geometrical magnetoresistance (MR) which stands as the most accurate and indisputable technique for mobility measurements.

Our results show that this method is also effective in both planar (FD-SOI) and vertical (FinFET) transistors with ultrathin body. For the first time, we apply the magnetoresistance for evaluating not only the properties of separate channels, but also their interaction mechanisms. Unconventional mobility curves with multi-branch aspect are recorded when two or more channels coexist. They are explained by the variations in effective field and centroid of the inversion charge [144]. A marked difference is observed between front and back channels as well as between planar and FinFET devices. The impact of temperature, gate length and fin width on the carrier mobility is also reported in this chapter.

The novelty of this work is to apply the geometrical MR technique for resolving the mobility behavior in state-of-the-art planar FD-SOI MOSFETs and vertical FinFETs with ultrathin body and multiple channels. We focus on the detailed study of mobility variations induced by the interplay of the various channels.

In this chapter, three different types of the advanced devices have been probed. Planar FD SOI MOSFETs, fabricated at LETI, feature 10 nm thick film and 145 nm BOX. HfO_2 (EOT = 1.75 nm) and TiN were deposited as gate oxide and gate metal. All devices have

undoped body and operate in fully-depleted mode. Also, the triple-gate and double-gate FinFETs, studied in Chapter 2.2, were tested for magnetoresistance mobility.

High magnetic field (1 – 11 T), supplied by a super-conducting magnet, was applied perpendicularly to the wafer surface. The I_D (V_{FG}) transfer characteristics were recorded with a semiconductor parameter analyzer (Agilent HP 4155). The drain bias was kept in the ohmic region of operation (V_D = 10 mV). The measurements were performed at low temperature to minimize the impact of phonon scattering. Small samples have been cut from the wafer and bonded on special home-made holder compatible with the cryostat dimentions.

3.2. Theory of Magnetoresistance Mobility

Hall and MR are dual effects. Under magnetic fields, carriers are submitted to the Lorentz force which is compensated by the Hall field. If the carriers are not deflected, a Hall voltage can be measured and the magnetoresistance is negligible. However, when the Hall field is inhibited, there is no Hall voltage and the magnetoresistance is maximum. Typical Hall effect structures require four or more contacts and long Hall bar (L >> W) shown schematically in Fig. 3-1a. As shown in Fig. 3-1b, when MOSFETs are short (L << W), the Hall electric field induced by an applied magnetic field is nearly shorted by the long end contacts. The Corbino disk shown in Fig. 3-1c is equivalent to an infinitely wide sample. It has one contact in the center of a circular sample and the other contact is at the periphery, eliminating the Hall field and voltage [145]. The geometries of Fig. 3-1 b and c make themselves well suited to magnetoresistance measurements.

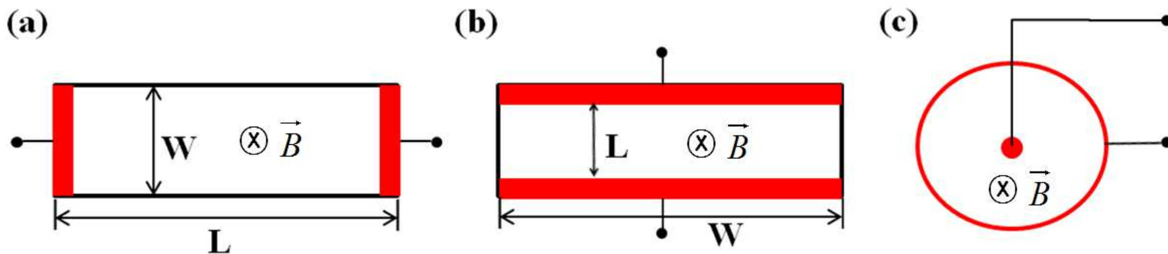

Fig. 3-1: Schematically illustration of the sample structures for Hall and magnetoresistance measurement: (a) Long sample (L >> W) for Hall measurement; (b) short sample (L << W) and (c) Corbino disk for magnetoresistance measurement.

(a) Basic magnetoresistance mobility

If the conduction is anisotropic, involving multiple-energy carriers and if carrier

scattering is energy dependent, the resistivity of a semiconductor generally increases when the sample is located in a magnetic field. This is the physical magnetoresistance effect (PMR). In a short and wide sample submitted to magnetic field, the carriers run off a medium straight line, raising the resistance of the sample. This phenomenon depends on the sample geometry and is known as the geometrical magnetoresistance (GMR). The magnetic field induced resistance change is due to resistivity changes of the semiconductor as well as to geometrical effects and is larger the higher the sample mobility is (Eq. (3.1)). Geometric effects are usually stronger. For example, in GaAs at room temperature and in a magnetic field of 1 T, the PMR is about 2 %, whereas the GMR is about 50 %. [45]. In long sample, the Hall field opposes the Lorentz force and MR is weak, simply reflecting the carrier energy distribution. In short MOSFETs or in Corbino disk, the Hall field is suppressed by the end contacts which enables the Lorentz force to deviate the carrier trajectory.

Such 'geometrical' MR is maximum, given by [146-150]:

$$R_B = R_0(1 + \mu_{MR}{}^2 B^2) \tag{3.1}$$

where R_0 is the channel resistance at zero magnetic field, R_B at high magnetic field and μ_{MR} is the magnetoresistance mobility.

The MR mobility is higher than the drift mobility, depending on the type of scattering mechanism. The basic Eq. (3.1) is valid for any combination of gate biases and free from considerations regarding the device architecture, oxide and film thickness, gate stack, doping, strain, etc. Plotting R_B/R_0 against the squared magnetic field results in a straight line (Fig. 3-2c), the slope of which yields μ_{MR}. The MR mobility is a pristine and robust parameter, most valuable for examining the transport mechanisms in MOSFETs [147-150]. The lone requirement is to utilize high magnetic field ($B \sim 1/\mu$) such as to obtain a measurable MR effect.

(b) Advanced magnetoresistance mobility

This method was developed in our group [150] in order to consider the effect of series resistance. When the series resistance R_S value is relatively larger ($\theta > 0.1\ V^{-1}$), it is needed to be considered in the device behavior. The coefficient θ can be extracted according to the Eq. (2.8) and expressed as:

$$\theta = \theta_i + \mu_0 \frac{W}{L} C_{ox} R_S \tag{3.2}$$

where θ_i depends on oxide properties and is normally small [70]. The total resistance $R_0 = V_0/I_0$, includes the gate modulated channel resistance R_C and the constant series resistance R_S: $R_0 = R_S + R_C$. There is no physical reason that R_S depends on magnetic field because the mobility in the heavily doped source and drain is modest. However, the channel resistance changes with B as shown in Eq. (3.1). Thereby, the total MR becomes:

$$R_B = R_S + R_C(1 + \mu_{MR}{}^2 B^2) \tag{3.3}$$

The MR ratio given by

$$\frac{R_B - R_0}{R_0} = \frac{R_C}{R_S + R_C} \cdot \mu_{MR}{}^2 B^2 \tag{3.4}$$

is certainly impacted by any significant series resistance. The basic MR mobility would be underestimated by the prefactor $\sqrt{R_C/(R_C + R_S)}$. The series resistance can be determined from the θ value at zero magnetic field, using Eq. (3.2). The method involves neglecting θ_i and using μ_0 extracted from the Y-function. Knowing the series resistance R_S and the total resistance R_0, the channel resistance R_C can be determined.

(c) Magnetotransconductance mobility

This method has been proposed for mobility extraction in GaAs MESFETs [151]. It uses the magnetotransconductance ratio which, from Eq. (2.3) and (3.1), gives as:

$$\frac{g_m(0)}{g_m(B)} = (1 + \mu_{MR}^2 B^2) \times \left[\frac{1 + \theta_B(V_G - V_{TH})}{1 + \theta_0(V_G - V_{TH})}\right]^2 \tag{3.5}$$

This technique offers an accurate value of the MR mobility only when coefficient θ is independent of magnetic field. Otherwise, the transconductance ratio is more severely affected by θ_B than the drain current ratio.

3.3. Magnetoresistance Mobility in Planar FD SOI MOSFETs

3.3.1. Front-channel mobility

Fig. 3-2 shows typical characteristics for planar SOI MOSFET in a range of magnetic

field. The threshold voltage V_{THF} (Fig. 3-2a) and subthreshold slope (inset of Fig. 3-2a) are hardly affected by the magnetic field whereas the drain current level (Fig. 3-2a) and transconductance (Fig. 3-2b) reduction reveal a clear MR effect, reflecting mobility degradation. The MR-induced reduction in mobility comes with a decrease of mobility degradation factor θ, deduced with Eg. (2.8), under high magnetic field (inset of Fig. 3-2b). The MR ratio R_B/R_0 is plotted versus B^2 which, as shown in Fig. 3-2c, results in straight lines being achieved for a range of front-gate bias V_{FG}. This confirms the GMR effect and Eq. (3.1). The carrier mobility is simply obtained from the slope and a typical curves of $\mu_{MR}(V_{FG})$ are reproduced in Fig. 3-2d.

The basic MR mobility curve, measured with grounded substrate ($V_{BG} = 0$ V), is shown in Fig. 3-2d. At low front-gate bias ($V_{FG} < 1.5$ V), the electron mobility is dominated by Coulomb scattering on ionized centers which are gradually screened by the formation of the strong inversion layer at front-channel. A maximum is reached (400 cm^2/Vs @ $V_{FG} = 1.5$ V) and then the mobility decreases due to higher vertical field.

Mobility curves extracted by other methods were also plotted in Fig. 3-2d. The variation of the effective mobility μ_{eff} and field-effect mobility μ_{FE} has been included for the sake of comparison. These curves have been calculated by taking $\mu_{eff} = \mu_0 /[1+\theta(V_G - V_{TH})] = \sqrt{\mu_0 \mu_{FE}}$ and $\mu_{FE} = \mu_0 /[1+\theta(V_G - V_{TH})]^2 = g_m L / W C_{ox} V_D$ with zero magnetic field. The parameters, μ_0, V_{TH} and θ are delivered by the Y-function and Eq. (2.8). As usual, the field-effect mobility is lower than the effective mobility measured under identical bias conditions. This discrepancy comes from the neglect of the electric field dependence of the mobility in the transconductance derivation [152, 153]. The field-effect mobility is lower because of the overestimated action of the vertical electric field (square bracket with θ factor).

Fig. 3-2d also presents an excellent correlation between μ_{MR} and μ_{eff} under strong inversion regime. In weak inversion, their behavior is quite different. The reason is that the effective mobility extraction is inaccurate in this range, where Y-function is no longer suitable.

The MR mobility is always higher than the effective mobility because the drift mobility is proportional to the mean relaxation time $\mu \sim \bar{\tau}$. Under high magnetic field, the carrier scattering and transport mechanisms are very complicated. The MR mobility changes as $\mu_{MR} \sim (\overline{\tau^3}/\bar{\tau})^{0.5}$, whereas the Hall mobility changes as $\mu_H \sim \overline{\tau^2}/\bar{\tau}$. The ratio between drift mobility and MR mobility $r_{MR} = (\overline{\tau^3}/(\bar{\tau})^3)^{0.5}$, can be determined for single-band

conduction and each type of scattering. For instance, under relatively weak magnetic field, $\mu_0^2 B^2 << 1$, we get $r_{MR} \cong 1.6$ for acoustic phonon scattering, $r_{MR} \cong 1.7$ for Coulomb scattering and $r_{MR} \cong 1$ for isoenergetic carriers [147, 154]. In ultra-thin film, several mechanisms (subband splitting, mixing of various scattering processes, band nonparabolicity, anisotropy of effective mass, relaxation time and so on) make more complex the physical scenario that is beyond the scope of this work. Nevertheless, our results in Fig. 3-2d indicate a scattering factor of $r_{MR} \cong 1.6 - 1.7$ in agreement with the theory.

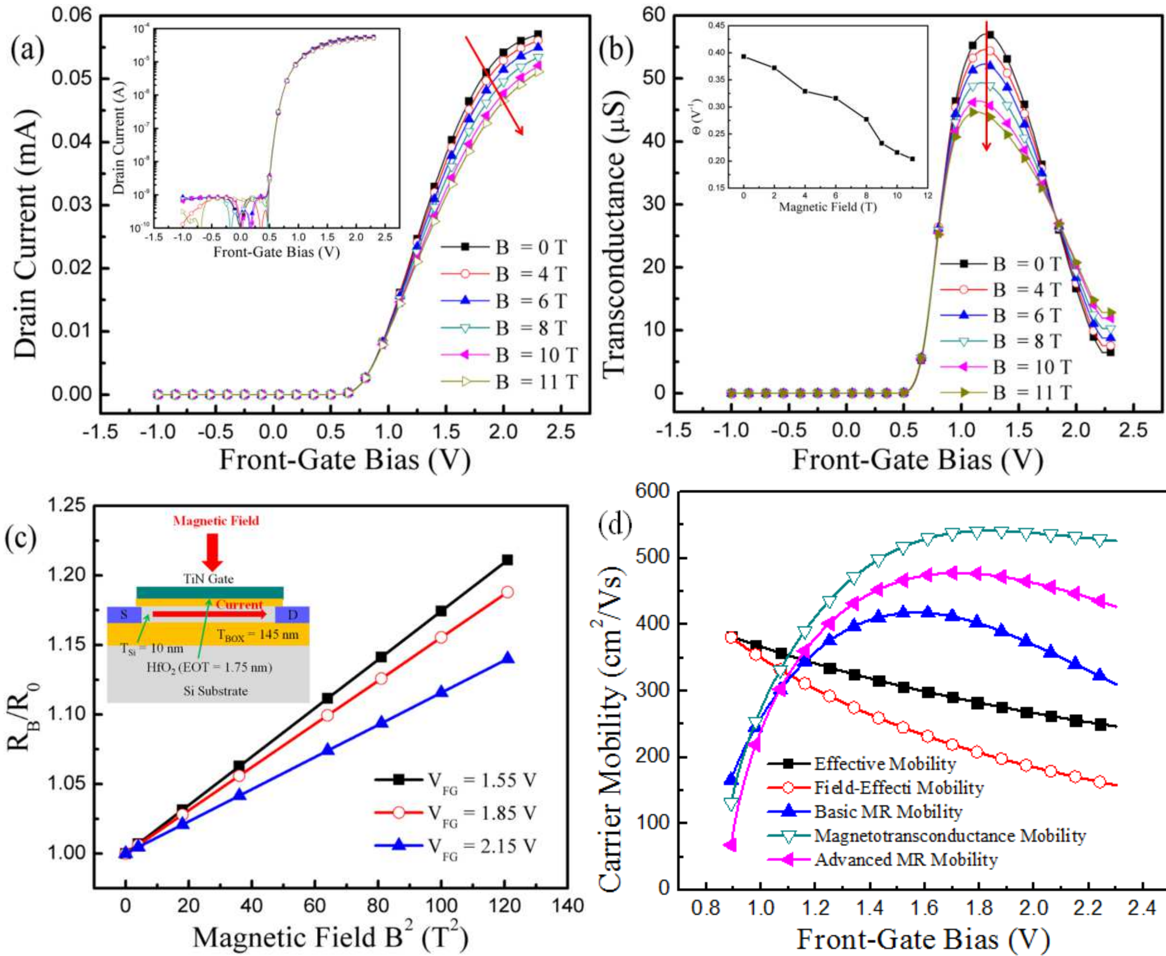

Fig. 3-2: Typical device behavior under high magnetic field and carrier mobility. (a) Drain current (linear scale) and (b) transconductance as a function of front-gate bias for a range of magnetic fields. Inset in Fig. 3-2a shows subthreshold Log $I_D(V_{FG})$ curves. Inset in Fig. 3-2b shows the mobility degradation factor versus magnetic field. (c) R_B/R_0 as a function of square of magnetic field at different front-gate bias. Inset of Fig. 3-2c shows cross-section of the FD SOI MOSFET and direction of applied magnetic field and current flowing. (d) Mobility curves extracted with various methods versus front-gate bias. Planar MOSFET with L_G = 1 μm, W_G = 10 μm, V_D = 10 mV, V_{BG} = 0 V, T = 100 K.

In our case, the relatively large series resistance ($\theta \approx 0.4$ V^{-1} @ B = 0 T) has an effect on carrier mobility. Therefore, when we compared basic MR and advanced MR, the latter

exhibits higher mobility peak and lower mobility degradation at high field due to the consideration of the channel resistance. As for the magnetotransconductance method, carrier mobility is dramatically overestimated in particular at high gate bias where the coefficient θ dominates. As mentioned above, this technique is acceptable only when coefficient θ is constant at different magnetic field. This is not our case (inset of Fig. 3-2b). Since θ decreases with B, the bracketed term including θ in Eq. (3.5) is smaller than 1 and becomes a source of errors. Therefore, the magnetotransconductance method is not accurate. For this reason, we will consider the basic MR and advanced MR methods in the rest of this chapter.

(a) Effect of the back-gate biasing on front-channel mobility

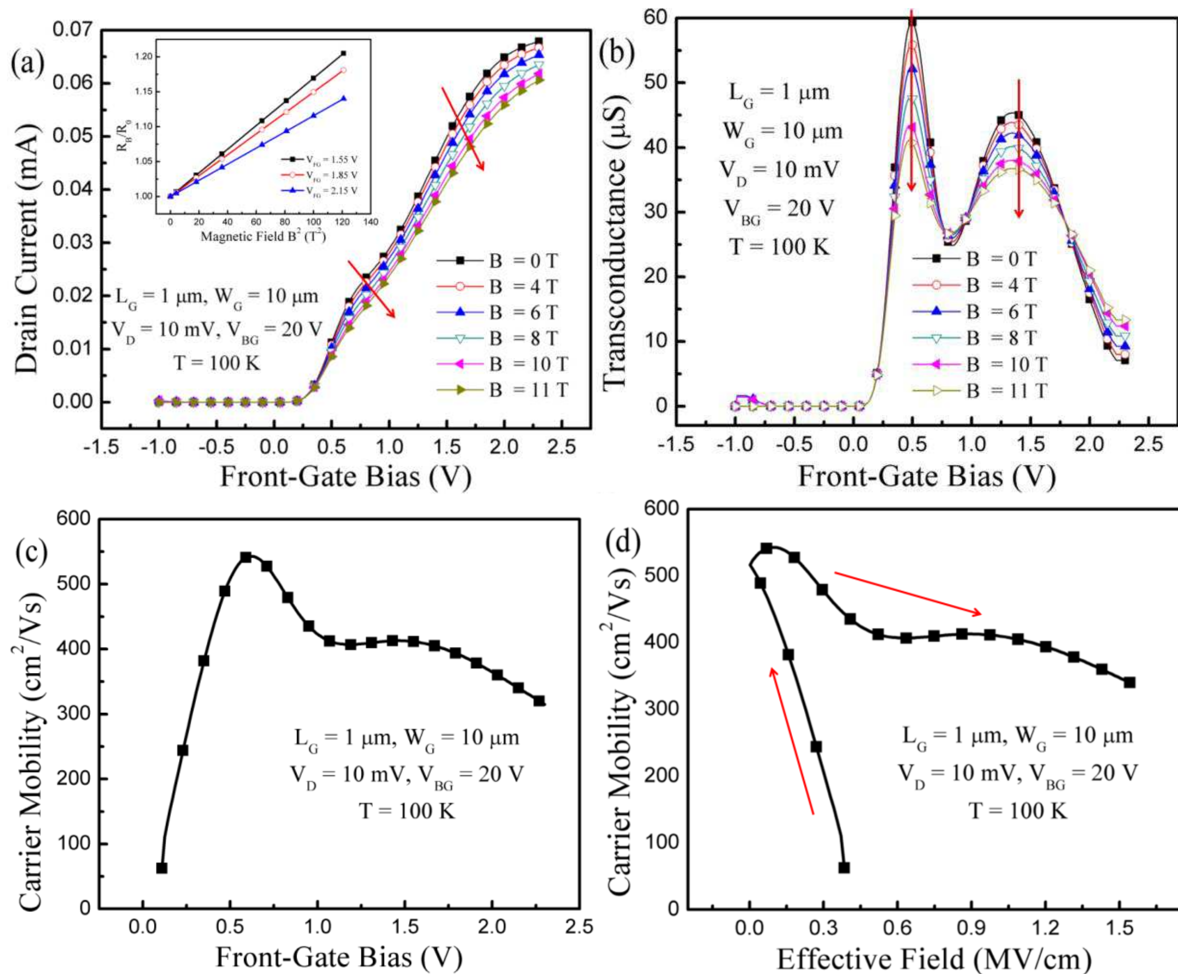

Fig. 3-3: Effect of back-gate bias (V_{BG} = +20 V). (a) Drain current and (b) transconductance as a function of front-gate bias for a range of magnetic fields. Inset in Fig. 3-3a shows R_B/R_0 versus the square of magnetic field at different front-gate bias. Electron mobility versus (c) front-gate bias and (d) effective field.

In chapter 2.1 and 2.2, the coupling effect was introduced based on the variation of the

threshold voltage with V_{BG}. Carrier mobility behavior also depends on the opposite-gate bias. A non-conventional mobility behavior is observed in Fig. 3-3 where the back-gate is based near inversion (V_{BG} = +20 V < V_{THB}). Drain current level (Fig. 3-3a) and transconductance peak (Fig. 3-3b) decrease with magnetic field. In the transconductance curve (Fig. 3-3b), there are two peaks. First peak reflects back-channel activation. When the V_{FG} increases, the back-channel threshold voltage V_{THB} is reduced by coupling effect [14] and back-channel is opened for $V_{FG} \approx 0.4$ V. Further increase of V_{FG} eventually turns on the front-channel, giving to the second transconductance peak. The resistance ratio R_B/R_0 linearly increases versus B^2 even if we have two channels (front- and back-channel) activated at the same time (inset Fig. 3-3a).

The mobility curve in Fig. 3-3c is explained as follows. The back-channel is first switched on and the mobility in the back-channel increases with V_{FG} because Coulomb scattering is screened by the forming inversion layer. Once the back-channel mobility reaches a peak (550 cm^2/Vs @ V_{FG} = 0.7 V), it starts decreasing. However, at $V_{FG} \approx 1$ V, the front-channel is being activated and then tends to dominate the total current. The combination of front- and back-channel mobilities results in a mild second peak (at V_{FG} = +1.5 V) before resuming a normal decrease at higher vertical field.

Fig. 3-3d shows the same mobility data as a function of the absolute value of the effective field $|E_{eff}|$, calculated as [143]:

$$E_{eff} \approx \frac{\eta Q_{inv} - C_{BOX}(V_{BG} - 2\phi_F)}{\varepsilon_{Si}} \tag{3.6}$$

where $Q_{inv} = C_{ox}(V_{FG} - V_{THF})$, $\eta = 0.5$; ε_{Si} and C_{BOX} are silicon permittivity and capacitance of the buried oxide; ϕ_F is the Fermi potential. A more accurate value of E_{eff} can be computed from numerical simulations as demonstrated in [143]. Even if Eq. (3.6) is rather crude, it points out a striking mobility behavior.

The plot in Fig. 3-3d is very informative, showing that two mobility values can correspond to the same field. This multi-branch mobility behavior confirms recent data obtained by split-CV method [144]. For $|E_{eff}| \approx 0.3$ MV/cm, the two mobility values are very different because they are associated with distinct carrier profiles within the body. The increasing and decreasing mobility regions reflect the electron transport at the back and front channels, respectively. The mobility peaks at minimum field ($E_{eff} \approx 0$). Note that the 'universal' mobility curve is totally different and fails to explain these features.

In Fig. 3-4, the mobility was measured at higher V_{BG} (V_{BG} = +40 V and 60 V). The impact of the magnetic field still leads to drain current (Fig. 3-4a) and transconductance peak (Fig. 3-4b) decrease. The carrier concentration in the back-channel (which now opens at lower $V_{FG} \approx 0$V) is increased and screens more efficiently the Coulomb scattering. As a result, the mobility peak is very large (750 cm^2/Vs). Again, the mobility reduction for $V_{FG} > 1$ V is slowed down by the activation of the front-channel. Further increase in V_{BG} (V_{BG} = +60 V, Fig. 3-4d) causes the mobility peak to decrease simply because the vertical field at the back-channel becomes stronger. However, the overall mobility behavior is similar with the previous case V_{BG} (V_{BG} = +20 V). In particular, two different mobility values can again be obtained at same field.

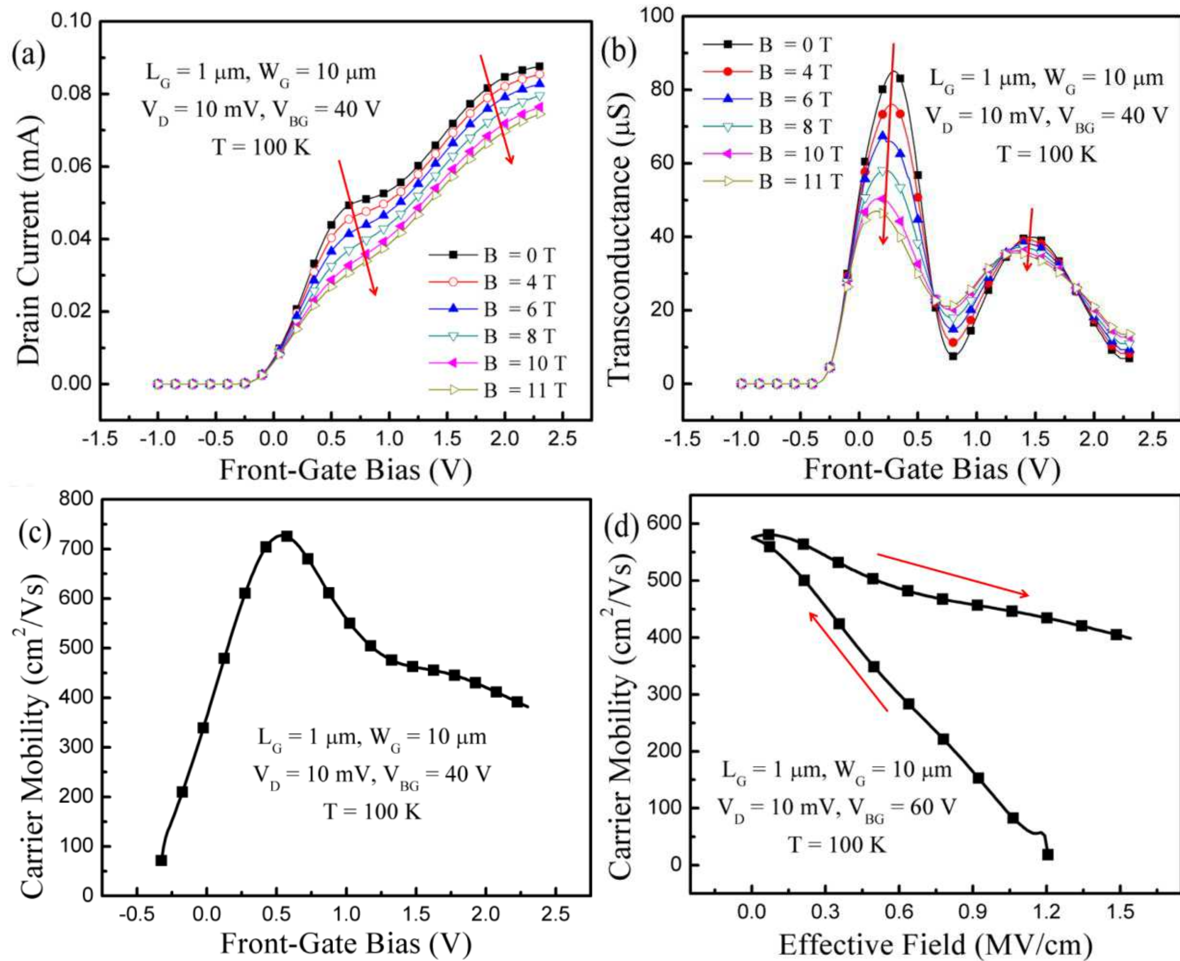

Fig. 3-4: Impact of high back-gate bias. (a) Drain current, (b) transconductance and (c) electron mobility versus front-gate bias at V_{BG} = +40 V. (d) Electron mobility as a function of effective field for V_{BG} = +60 V.

(b) Effect of gate length and temperature on front-channel mobility

Geometrical magnetoresistance mobility was measured in shorter (L_G = 350 nm)

device. Typical impact of magnetic field and mobility curves are reproduced in Fig. 3-5. Drain current level and mobility degradation factor were reduced with magnetic field. Compared with long device (Fig. 3-2d), lower mobility and threshold voltage were obtained in short device due to the process-induced neutral defects [155] and charge sharing effect [156], respectively. However, the general mobility tendency is similar to that obtained in long-channel device.

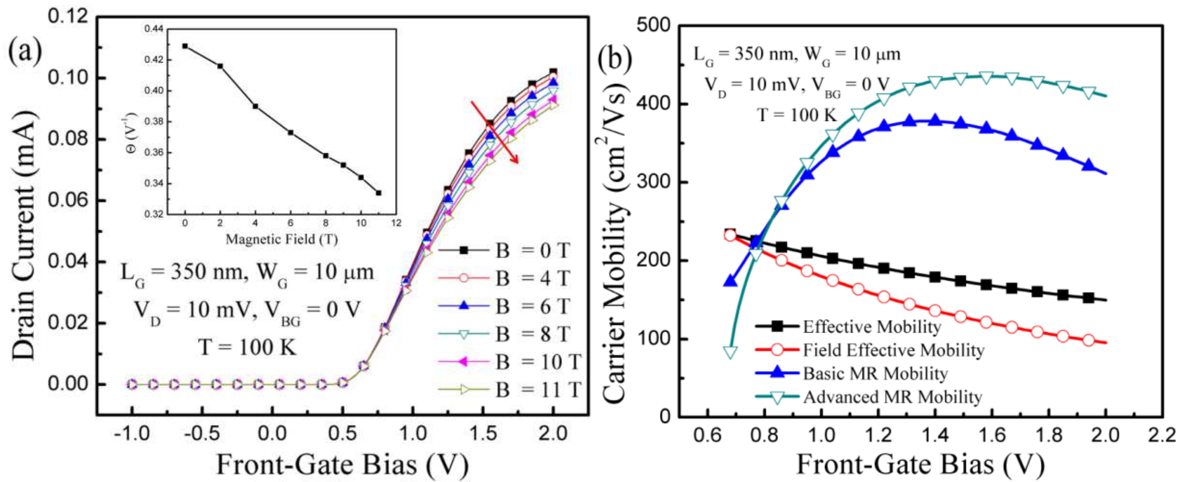

Fig. 3-5: Typical magnetoresistance effect in shorter length device (V_{BG} = 0 V). (a) Drain current and (b) electron mobility versus front-gate bias for a range of magnetic fields. Inset in Fig. 3-5a shows mobility degradation factor as a function of magnetic field.

The unusual mobility curve was also demonstrated in short device. Like for the long device, the influence of the applied magnetic field is obviously involved in current behavior (Fig. 3-6a) even when the two channels are simultaneously stimulated. Therefore, plotting the carrier mobility versus effective field, two different values can be produced at the same effective field according to the variation of carrier distribution centroid within the transistor body (Fig. 3-6b).

Carrier mobility curves obtained in short device were summarized in Fig. 3-7. Global trend of the mobility behavior is exactly as in long device. By the interrelation of the front- and back-channel, uncommon mobility curve shape was achieved. The maximum mobility value is determined by the strength of the vertical field (applied back-gate bias). When the front-channel prevails (V_{FG} > 1 V), all mobility curves tend to merge. But, in the region where the back-channel dominates (V_{FG} < 0.4 V), the carriers are very different according to the vertical field induced by the bottom gate.

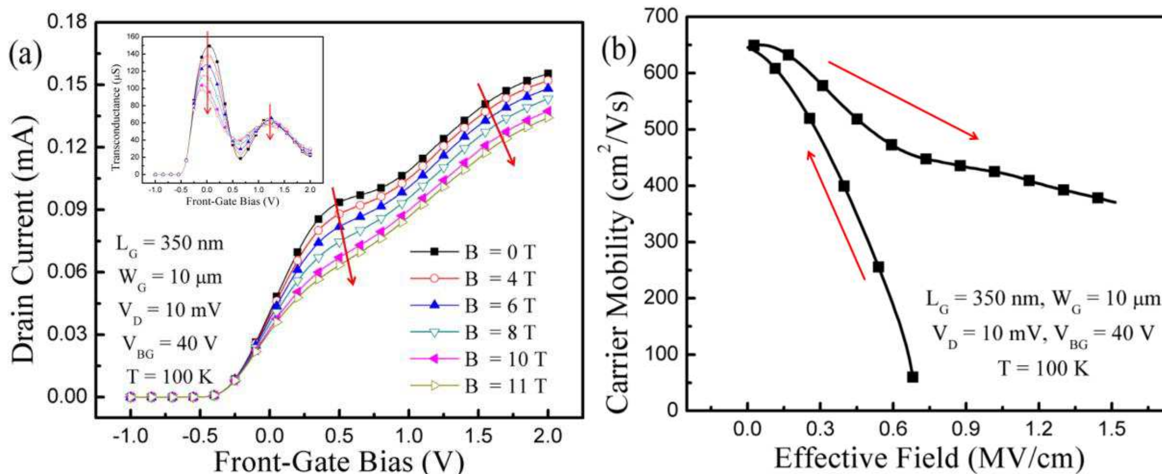

Fig. 3-6: Impact of back-gate bias in short device. (a) Drain current as a function of front-gate bias for a range of magnetic fields at V_{BG} = +40 V. Inset of Fig. 3-6a shows transconductance versus front-gate bias (b) Electron mobility versus effective field for V_{BG} = +40 V.

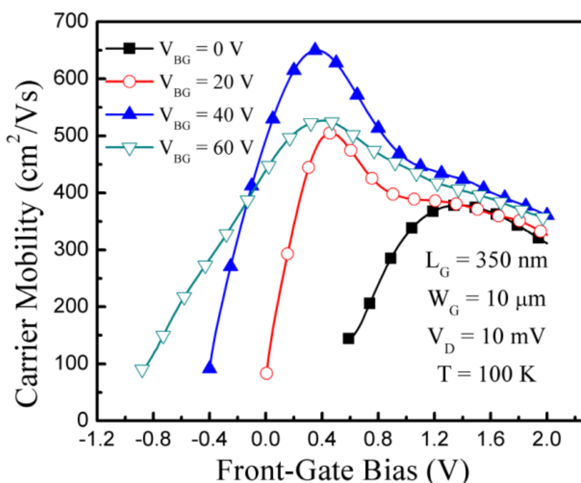

Fig. 3-7: Electron mobility as a function of front-gate bias at different back-gate bias in short (L_G = 350 nm) device. The left regions of the curves are very different as they depend on the vertical field induced by the back-gate voltage.

Carrier mobility also depends on temperature. In Fig. 3-8, the mobility curves were measured with various back-gate biases at higher temperature (T = 200 K). Carrier mobility is less than at lower temperature (T = 100 K, Fig. 3.2-3.4) due to enhanced phonon scattering [69]. The 'universal mobility' behavior is negated whatever the temperature when the back-channel is concurrently opened with the front-channel.

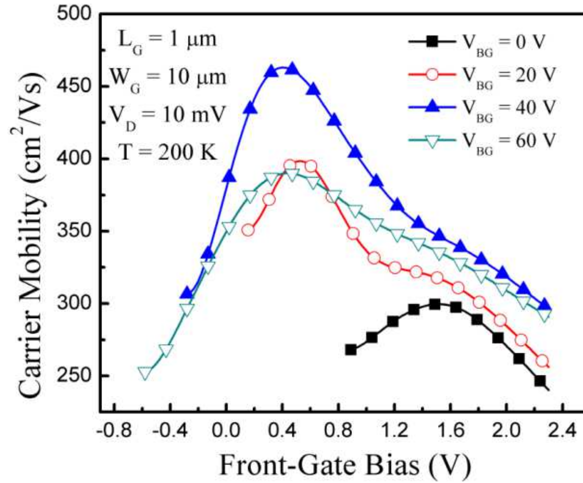

Fig. 3-8: Impact of temperature on magnetoresistance mobility. Electron mobility versus front-gate bias for various back-gate biases at T = 200 K.

3.3.2. Back-channel mobility

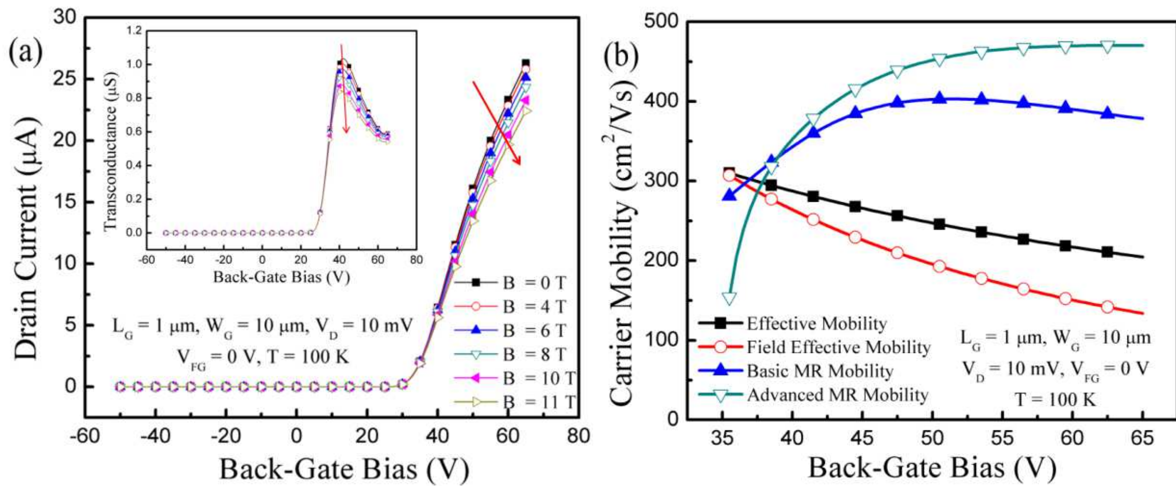

Fig. 3-9: Back-channel behavior under high magnetic field. (a) Drain current as a function of back-gate bias in a wide range of magnetic field at V_{FG} = 0 V. Inset of Fig. 3-9a shows the corresponding transconductance. (b) Back-channel mobility curves deduced with various methods as a function of back-gate bias at V_{FG} = 0 V.

Reciprocal experiments were conducted by probing the back-channel. Fig. 3-9a and inset of Fig. 3-9a show the impact of the magnetic field on the back-channel current and transconductance for V_{FG} = 0 V. In Fig. 3-9b, the correlation between several different methods of mobility measurement is presented. While the GMR trends are the same, the quantitative results may differ from the front-channel ones. The electron mobility is slightly larger at the back-channel than at front-channel (Fig. 2-3b) thanks to the better interface quality of the back Si-SiO_2 interface. Measurement at room-temperature, where phonon scattering is intense, showed a larger difference between front and back mobilities [142]. This

point will be verified by comparing front and back mobility values measured at higher temperature (T = 200 K, see Fig. 3-12b). Compared with front-channel, in back-channel, the mobility decreases more slowly for high V_{BG}. The reason is that mobility degradation factor θ of the back-channel (0.015 V^{-1} at B = 0 T) is smaller than in front-channel (inset Fig. 3-2b) due to the difference in oxide thickness.

(a) Coupling of back-channel mobility on front-gate bias

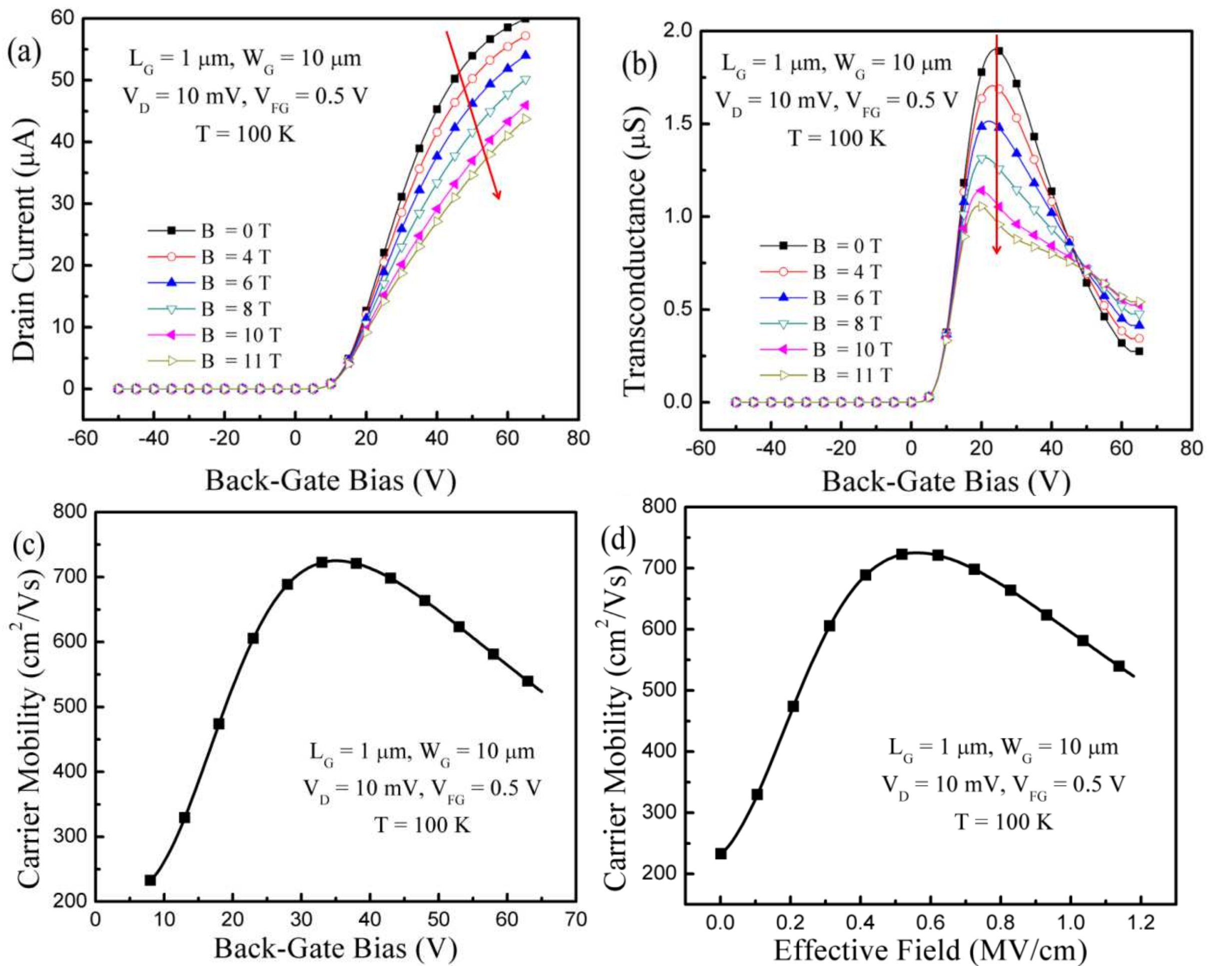

Fig. 3-10: The impact of front-gate bias (V_{FG} = +0.5 V) on back-channel behavior. (a) Drain current and (b) transconductance versus back-gate bias in a range of magnetic field for V_{FG} = 0.5 V. Electron mobility as a function of (c) back-gate bias and (d) effective field extracted from Fig. 3-10a.

Back-channel mobility depends on the applied bias at front-gate. Front-channel did not turned on for V_{FG} = +0.5 V: a single transconductance peak was observed at B = 0 T (Fig. 3-10b). A relatively strong effect of the magnetic field is shown in Figs. 3-10 a and b where the drain current and transconductance decrease more notably because the back-channel mobility is larger. However, by applying V_{FG} = +0.5 V, the vertical electric field is decreased and the

centroid of the inversion charges is moved to the middle of the silicon body. Therefore, the scattering at the back interface is less. This is why, the carrier mobility is improved compared with V_{FG} = 0 V (Fig. 3-9b). When carrier mobility is plotted versus effective field (Fig. 3-10d), the mobility behavior follows the 'universal mobility' plot because front-channel did not switch on.

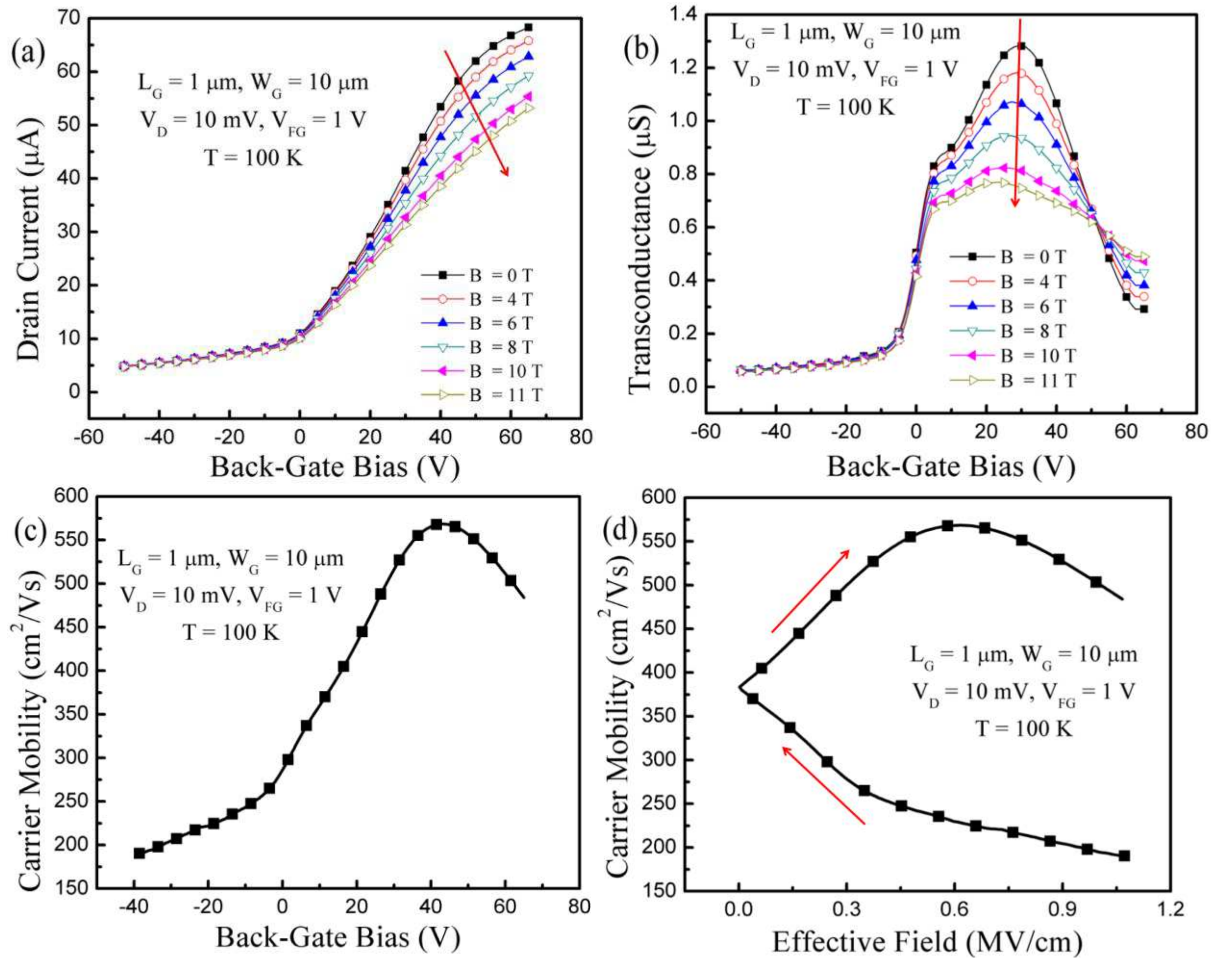

Fig. 3-11: Influence of high front-gate bias (V_{FG} = +1 V). (a) Drain current and (b) transconductance versus back-gate bias and magnetic field. Electron mobility as a function of (c) back-gate bias and (d) effective field.

An interesting case of coupling effect is observed for V_{FG} = 1 V (Fig. 3-11). Here, front-channel was slightly opened at the beginning of the measurement, providing small current and non-zero transconductance value at V_{BG} = -50 V (Fig. 3-11c and d). The front-channel inversion is gradually enriched as V_{BG} increases from -40 V to 0 V, reducing linearly V_{THF} but the mobility is still modest because the vertical field is very high. For $V_{BG} > +20$ V, the effects of field reduction and formation of back-channel cumulate, causing a clear mobility improvement by a factor of 3. Fig. 3-11d shows the mobility as a function of $|E_{eff}|$

calculated with the reciprocal of Eq. (3.6). We again observe a dual-branch plot, albeit its signature is different from that in Fig. 3-3d and Fig. 3-4d. The lower and upper branches respectively correspond to the front and back mobilities.

(b) *Effect of gate length and temperature on back-channel mobility*

The expected mobility variation with gate length and/or temperature was also measured for the back-channel. Compared with the nominal case (L_G = 1 μm at T = 100 K), mobility is degraded in short device (L_G = 350 nm at T = 100 K, Fig. 3-12a) or at high temperature (L_G = 1 μm at T = 200 K, Fig. 3-12b) with/without front-gate biasing. At 200 K, back interface mobility is quite higher than the front interface one (Fig. 3-8). This is evidence of better back-channel interface quality than at the front Si-high K interface.

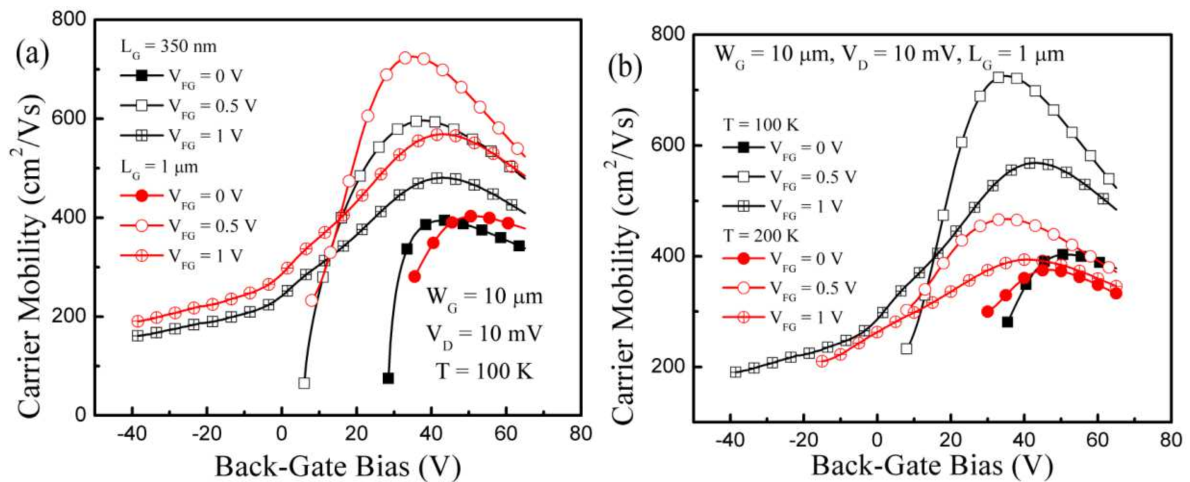

Fig. 3-12: Impact of gate length and temperature on back-channel mobility. (a) Electron mobility versus back-gate bias at different front-gate bias in short (L_G = 350 nm) and long (L_G = 1 μm) device. (b) Electron mobility as a function of back-gate bias for various front-gate biases in long device at different temperature (T = 100 K and 200 K).

3.4. Magnetoresistance Mobility in FD SOI Triple-Gate FinFETs

We now discuss, for the first time, the interesting case of FinFET operation under magnetic field.

3.4.1. Front-channel mobility

FinFETs are more complicated devices, where two lateral channels, a top channel, and even a back-channel (activated with $V_{BG} > V_{THB}$) coexist. The geometric MR is effective in the horizontal channels (if $W_F/L >> 1$) which behave as planar MOSFETs. Interestingly, the MR also develops in the vertical channels despite the aspect ratio ($H_F/L < 1$) is apparently unfavorable.

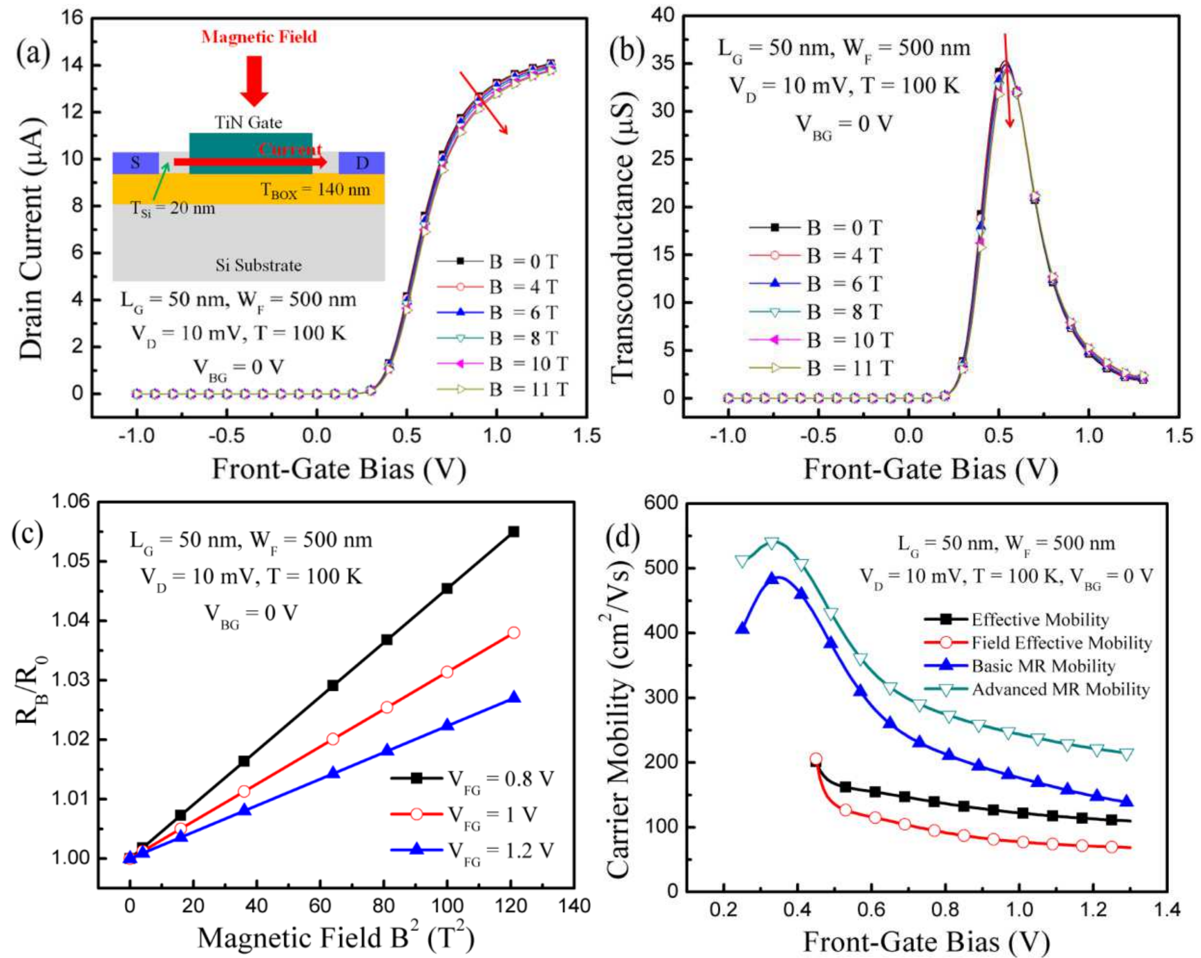

Fig. 3-13: Typical magnetoresistance effect on triple-gate SOI FinFET. (a) Drain current and (b) transconductance as a function of front-gate bias for a range of magnetic fields. Inset of Fig. 3-13a shows cross-section of the tir-gate SOI FinFET and direction of applied magnetic field and current flowing. (c) R_B/B_0 versus square of magnetic field at different front-gate bias. (d) Mobility curves extracted with different techniques versus front-gate bias.

As shown in Fig. 3-13, drain current and transconductance were reduced with magnetic field in SOI triple-gate FinFET. The resistance ratio (R_B/R_0) also linearly increases versus B^2 (Fig. 3-13c). These phenomena mirror typical effect of magnetic field and make possible to extract the MR mobility in our FinFET. As a result, a typical bell-shaped mobility curve is reproduced in Fig. 3-13d. The relationship between MR mobility, effective mobility and field-effect mobility curves at high electric field follows the explanation given for Fig. 3-2d.

The MR mobility is decent (500 cm^2/Vs) but smaller than in planar MOSFETs (Fig. 3-2). The dependence on gate voltage is accentuated suggesting a stronger effective field. Due to the 3D structure, it is difficult to compute E_{eff} and to discriminate the mobility values in the lateral and horizontal channels.

(a) *Effect of back-gate bias on front-channel mobility*

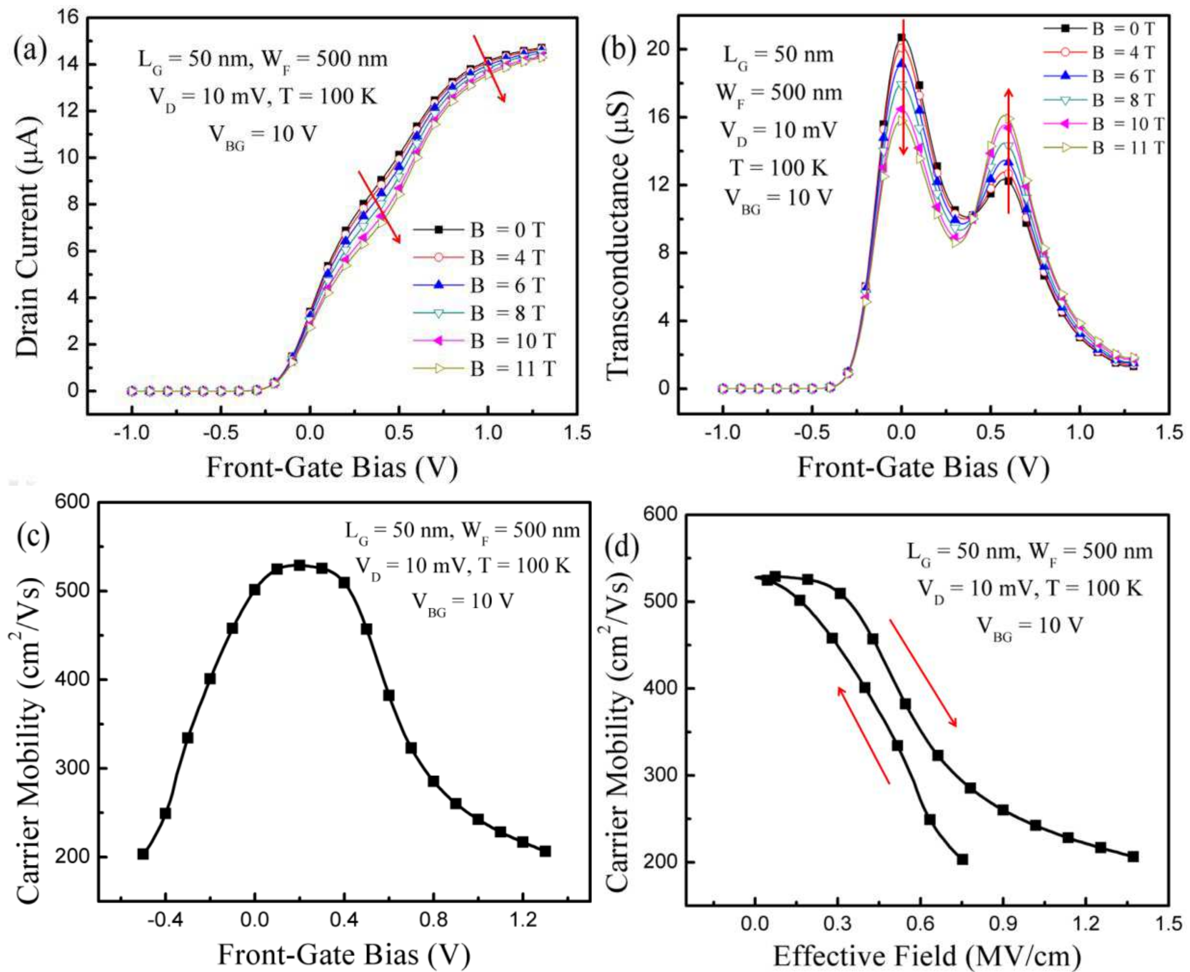

Fig. 3-14: Impact of back-gate bias (V_{BG} = +10 V). (a) Drain current and (b) transconductance versus front-gate bias and magnetic field. Electron mobility as a function of (c) front-gate bias and (d) effective field.

The shape of the curve changes qualitatively when the measurement is performed with positive V_{BG} (Fig. 3-14 and Fig. 3-15). In Fig. 3-14, a back-gate bias (V_{BG} = +10 V) slightly larger than the back-channel threshold voltage (V_{THB} = 7 V) was applied. The sequential opening of the back and front channels leads to a hump in $I_D(V_{FG})$ curves (Fig. 3-14a) and a double peak in transconductance (Fig. 3-14b). During the early activation of the back-channel, the mobility increases with bias up to V_{FG} = 0 V. Then, the opening of the front-channel

prevents the mobility to drop as rapidly as in Fig. 3-13d. Only for V_{FG} = 0.4 V does the effective field increases enough to degrade the mobility. An attempt to plot mobility versus effective field (still calculated with Eq. (3.6) given the large fin width) is shown in Fig. 3-14d. A multi-branch mobility basically similar to that in planar MOSFETs was observed.

The same measurement as in Fig. 3-14 was carried out with higher V_{BG} (V_{BG} = +20 V, Fig. 3-15). In this case, back-channel was switched on earlier than in the previous case (V_{BG} = +10 V, Fig. 3-14 c and d). Therefore, mobility starts to increase as the effective field drops for higher V_{FG}. A maximum is reached and then a wide, nearly flat area of mobility curve is visible before the front channel turns on. Finally the mobility, dominated by the top channel, decreases with field. Interestingly, we now observe a multi-branch mobility but the curve is anti-clock wise.

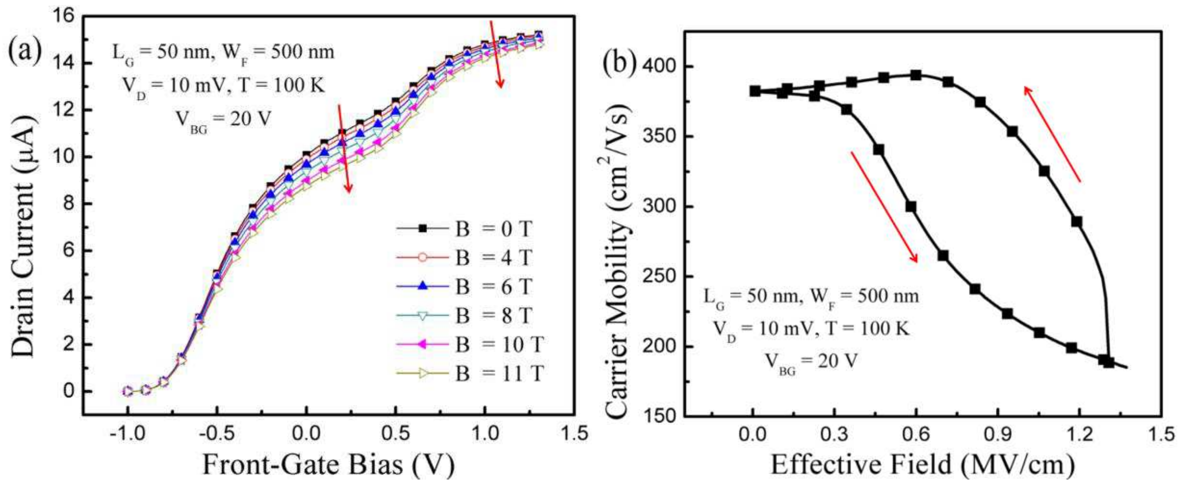

Fig. 3-15: Effect of high back-gate bias (V_{BG} = +20 V). (a) Drain current as a function of front-gate bias and (b) electron mobility versus effective field.

(b) Effect of gate length and temperature

In general, carrier mobility is improved in longer device and lower temperature as described several times. The same tendency was demonstrated in triple-gate SOI FinFETs in Fig. 3-16. As discussed in Fig. 3-14 and Fig. 3-15, the influence of the back-gate on front-channel mobility results in merging curves at high field and very different behavior when the back-channel dominates.

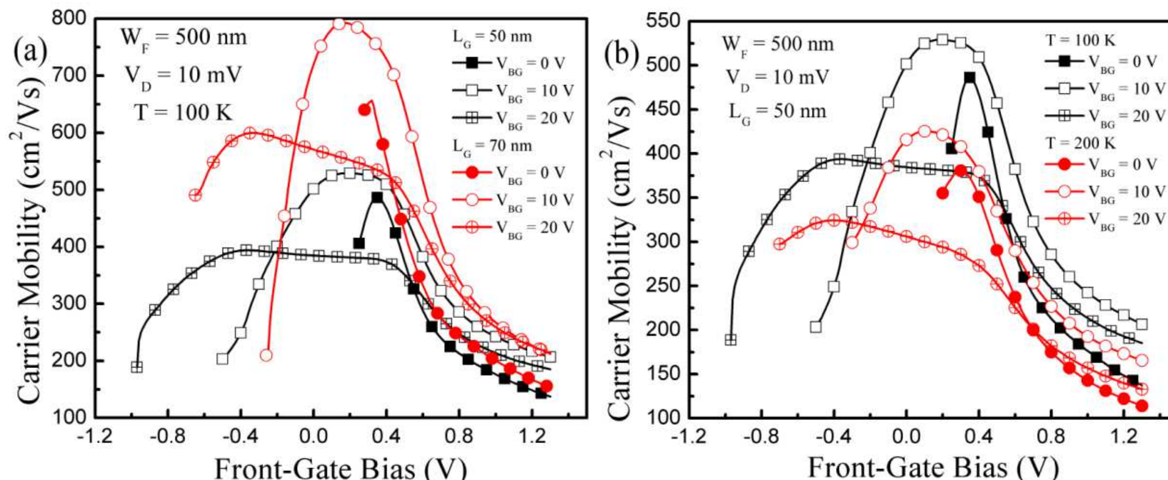

Fig. 3-16: Effect of gate length and temperature on carrier mobility in triple-gate SOI FinFET. Electron mobility as a function of front-gate bias for various back-gate biases at (a) different gate length (L_G = 50 nm and 70 nm) and (b) different temperature (T = 100 K and 200 K).

3.4.2. Back-channel mobility

Back-channel mobility in triple-gate SOI FinFETs shows typical shape curves for V_{FG} = 0 V (Fig. 3-17a). On the other hand, unusual coupling-induced mobility behavior is noted by applying front-gate bias. In Fig. 3-17b, front-channel was activated from the beginning of the measurement (for V_{BG} = 0 at V_{FG} = +0.5 V), resulting in a flat carrier mobility (275 cm^2/Vs). With increasing back-gate bias, vertical electric field decreases and mobility increases. At 0.4 MV/cm, back-channel is turned on and mobility records a maximum value of 450 cm^2/Vs. Then, according to the increase of vertical field by V_{BG}, mobility reduces again.

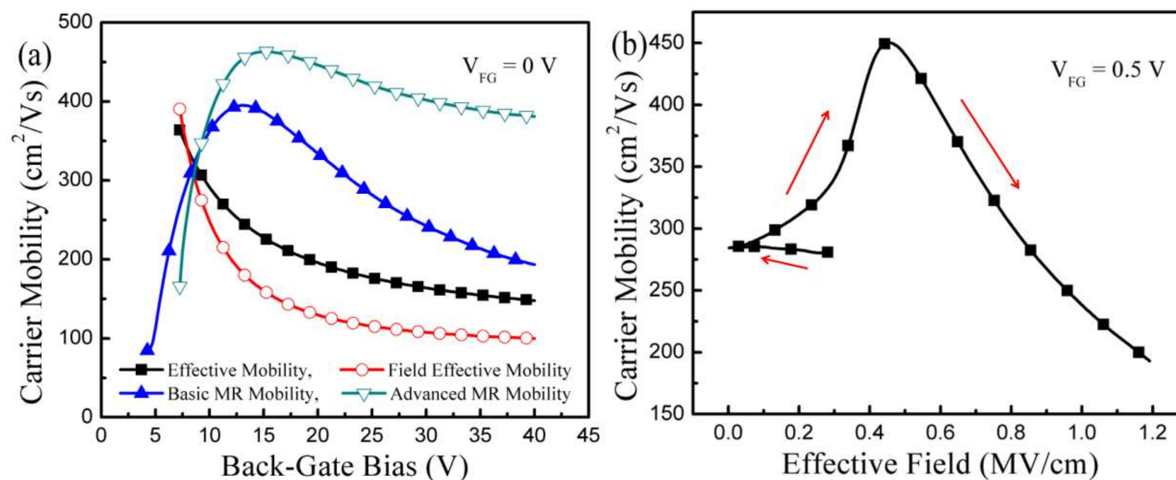

Fig. 3-17: Back-channel mobility in triple-gate SOI FinFET. (a) Mobility curves as a function of back-gate bias for V_{BG} = 0 V. (b) Mobility versus effective field for V_{FG} = 0.5 V. L_G = 50 nm, W_F = 500 nm, V_D = 10 mV, T = 100K.

The general trends of mobility variation with gate length and temperature are compiled in Fig. 3-18. They are consistent with our previous observations.

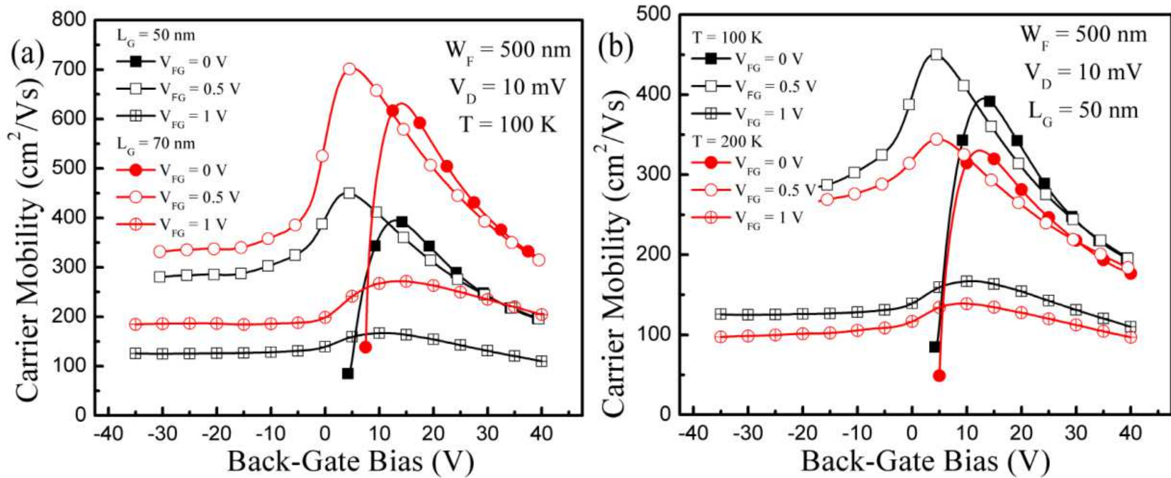

Fig. 3-18: Effect of gate length and temperature on back-channel mobility in triple-gate FinFET. Carrier mobility as a function of back-gate bias for various front-gate biases (a) at different gate length (L_G = 50 nm and 70 nm) and (b) temperature (T = 100 K and 200 K).

An intriguing question subsists: how can the lateral channels contribute to the geometrical MR for vertical magnetic field? In order to document the answer, we have simply removed the top gate and repeated the measurements in double-gate configuration. The details are presented in the next section.

3.5. Magnetoresistance Mobility in FD SOI Double-Gate FinFETs

The magnetic field is still applied perpendicular to the wafer surface. The field is in the plane of the inversion charge, perpendicular to the current flow (inset Fig. 3-13a). Vertical DG FinFET, introduced in Chapter 2.2, has only two lateral gates and they are laid in parallel with the magnetic field. Basically, when a channel is placed in parallel with magnetic field, there is no geometric magnetoresistance and the physical magnetoresistance in bulk MOSFETs is negligible. The transverse Lorentz force is indeed compensated by the Hall field. Nevertheless, the influence of the magnetic field is substantial and large enough for extracting MR mobility (Fig. 3-19). This in-plane MR is a unique effect in MOSFETs and looks as contradicting the Hall theory. Our interpretation is that geometric MR effect is here induced by the double-gate configuration.

In vertical DG FinFETs, the potential is equal at the two lateral gates as controlled by the same gate bias V_{FG}. Therefore, Hall effect is inhibited and the Lorentz force is free to deflect electrons. This DG effect is similar to a geometrical MR without constraints on the aspect ratio (H_F/L). The geometric MR is visible even when the channel length exceeds the fin width and height (see Fig. 3-20). An additional effect in DG MOSFETs is the location of the centroid of inversion charge at the middle of the body, which reduces carrier bumping on the Si/SiO_2 interface.

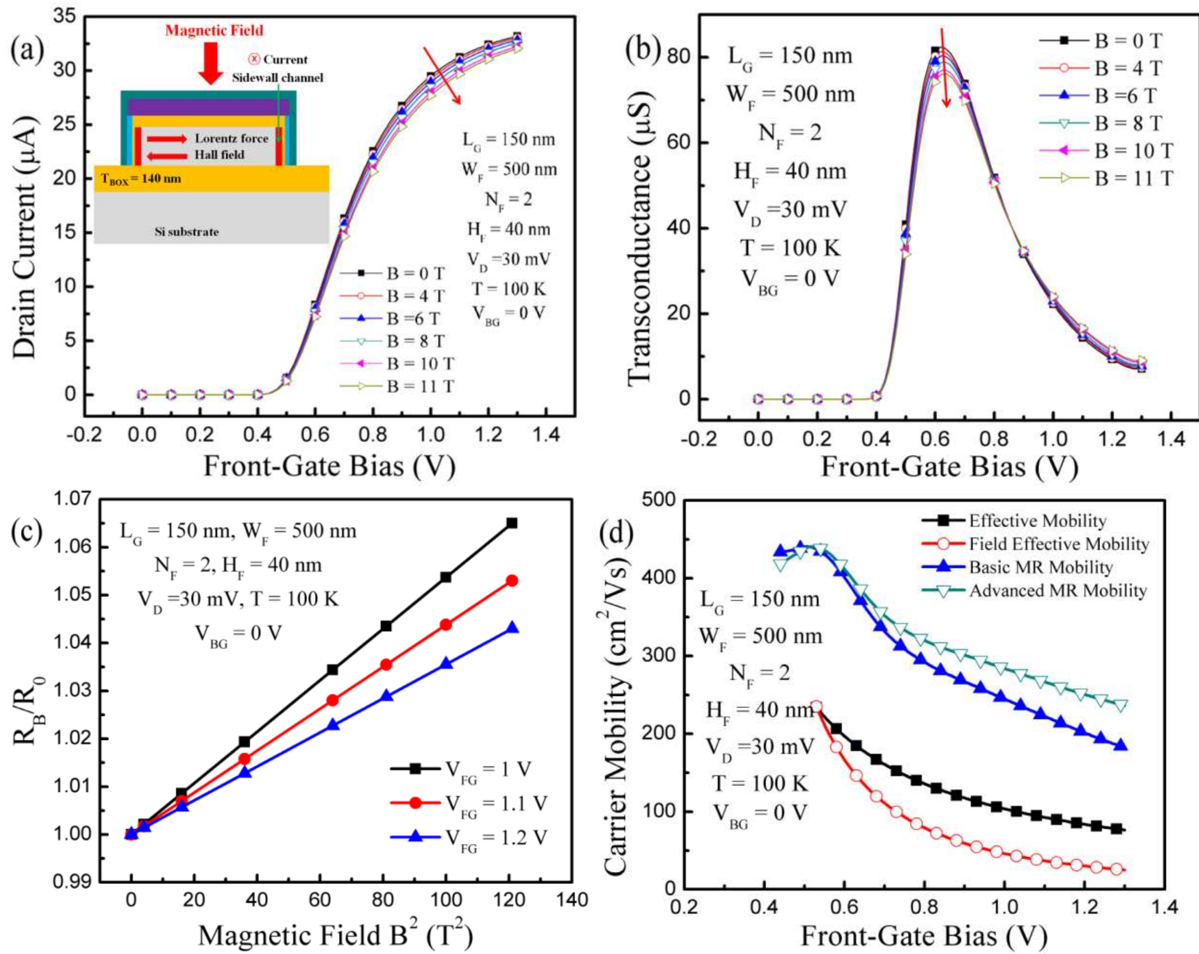

Fig. 3-19: Impact of magnetic field in vertical DG SOI FinFET. (a) Drain current and (b) transconductance versus front-gate bias and magnetic field. Inset of Fig. 3-19a shows cross-section of the vertical DG FinFET and direction of applied magnetic field, current flowing, Lorentz force and Hall field. (c) R_B/B_0 versus B^2. (d) Mobility curves extracted with different methods.

The MR mobility of the vertical DG FinFET, together with effective and field-effect mobilities, is shown in Fig. 3-19d. Their aspect and correlation are similar to other device architectures. The peak mobility is 20 % smaller than in triple-gate FinFETs as a consequence of an inferior quality of the high-k/Si interface on the sidewalls than on the top flat surface.

Additional measurements were performed in narrower devices and lower mobility was recorded (Fig. 3-20). This result suggests that in narrower FinFETs surface scattering is increased, causing mobility degradation.

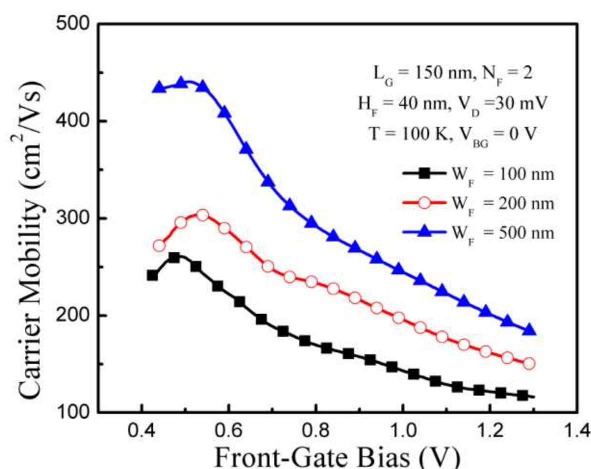

Fig. 3-20: Effect of fin width on MR mobility. Basic MR mobility as a function of front-gate bias for different fin width in vertical DG SOI FinFET.

3.6. Conclusion

Low-temperature magnetoresistance measurements, performed in advanced SOI MOSFETs, provide direct information on the carrier mobility behavior. The mobility curves have different signatures according to the channel under inspection: front, back, planar FD-SOI MOSFET, or FinFET. When more than one channel is activated, we observed dual-branch mobility curves which infirm the applicability of the 'universal mobility' model to ultrathin FD transistors. The electron mobility is in general large with variations related to the peculiar architecture, thickness and process flow of each transistor. We have demonstrated the feasibility of geometrical magnetoresistance even in advanced devices with ultrathin body and planar or vertical configuration. These results open the door to detailed study of scattering mechanisms in nano-size films.

The geometrical MR measured in FinFETs with triple-gate or double-gate is a striking result which deserves a theoretical investigation. Numerical simulations presented in [157] need to be enriched in order to confirm and fully understand the suppression of the Hall field. Another avenue to explore is the discrimination of front- and back-channel mobilities from our multi-branch curves. The "mobility spectrum" technique looks in this respect very attractive [158-159].

Chapter 4:

Remote Carrier Trapping in ONO FinFETs for Innovative Flash Memory

The goal of this thesis is to explore memory application in advanced SOI transistors by taking advantage of the coupling effects discussed in the previous chapters. We first investigate, in this chapter, non-volatile memory device that can be achived by modifying the SOI material such as the BOX can store permanent charges. We propose innovative mechanisms for memory programming and reading and demonstrate the performance and advantages of FinFET flash cells.

4.1. Introduction

Advanced SOI devices with alternative buried insulator (BOX) are investigated for several applications: self-heating reduction [160], strain transfer [161], fin etch definition avoiding undercut [162] and non-volatile charge storage [163, 164]. In this chapter, we study advanced FinFETs fabricated on SOI with a multi-stack SiO_2-Si_3N_4-SiO_2 (ONO) buried insulator, for innovating flash memory application with remote charge trapping.

Until now, various architectures of flash memory cell have been proposed [165-168]. Cells with a top floating gate for charge trapping are the most widely used structure [168]. The storage medium and the conduction interfaces are usually located within the same gate. For this reason, the trapped charges in the floating gate are disturbed during reading operation [169]. After many programming/erasing cycles, the stored information can gradually be lost by reading operation due to degraded tunneling oxide layer.

For the further evolution of flash memory cell, one of the most important issues is the cell downscaling. Beyond the 22 nm technology node, the channel length and the tunneling oxide thickness reduction will cause several critical problems. Shorter gate length, which requires thinner tunneling oxide to control the device, could compromise the cell reliability and the flash memory function. Thinner tunneling oxide improves the device controllability and allows faster programming/erasing time and operating bias lowering. But, the reduction of the tunneling oxide induces a degradation of the retention time.

A silicon-oxide-nitride-oxide-silicon (SONOS) structure, where the nitride film is used for charge storing, was proposed [163, 167. 170-173]. Usually, the SONOS device is made by stacked layers on Si substrate. The SONOS flash memory cell is attractive because the device fabrication process is simple and the nitride charge trapping layer provides good retention time. For these reasons, the SONOS devices are very promising candidates for flash memory cells.

In our work, the devices under test have thick ONO BOX and are not especially optimized for charge trapping and flash memory application. Indeed, a FinFET memory with ONO buried storage layer may need more complex control circuit and slightly larger silicon area if the back-gate is used as the second gate for programming/erasing operation. Nevertheless, this device has definite merits. The key advantage of FinFETs with buried ONO layer is that analog/logic and memory operations can be carried out within the same cell due to the decoupling of the storage and read operations. Another benefit of this technology is the separation of the programming interface from the reading interface. The charges are trapped in the buried nitride layer and remotely sensed at the front interface by gate coupling. As the device scales down, the degradation of the nonvolatile retention time is lessened. Indeed, the back tunneling oxide thickness can remain unchanged while the front-gate oxide can still be made thinner following the state-of-the-art MOS technology. Therefore, the separation of the two interfaces improves the reliability of the memory device and reduces the charge disturbance problems.

This work focuses on the principles and physical mechanisms as revealed by experimental data. We demonstrate that memory effects are induced by trapped/detrapped charges in the Si_3N_4 buried insulator. Two possible programming/erasing mechanisms are proposed. One is the carrier tunneling by applying a high back-gate bias and the other is the carrier injection obtained with a moderately high drain voltage. In the latter case, according to the polarity of the trapped charges and their location along the channel, four different current levels can be achieved leading to double-bit nonvolatile memory states. The drain current hysteresis induced by charge trapping/detrapping will be studied by scanning the back-gate bias. In order to clarify the charge trapping and coupling mechanisms, the temperature of operation was used as additional experimental parameter. Systematic measurements reveal that the memory effect depends on the bias condition, geometrical parameters and temperature.

4.2. Nonvolatile Memory

Nonvolatile memories (NVMs), like EPROM, EEPROM and Flash, retain stored information even when they are disconnected from power supply. In this section, the main different types of NVM and their programming mechanisms will be introduced. A special focus will be given on flash memories especially using nitride as storage medium. The last

part will briefly present the resistive memories which are considered as the best alternative to flash devices.

4.2.1. Classification of nonvolatile memory

Before describing each type of nonvolatile memory, it is essential to know the difference between Random-Access Memory (RAM) and Read-Only Memory (ROM). Basically, the read process of RAM and ROM are identical by having x-y address for each cell to distinguish it from other cells. As we describe below, some ROM devices have also rewriting capability despite they require a special procedure for programming/erasing. The main difference between RAM and ROM is the frequency of reading and writing. RAM has equal opportunity of reading and writing while a ROM has more frequent reading than rewriting.

Base on this background, several types of NVM are explained in brief.

- ROM: Once the memory content is fixed by the manufacturer, it cannot be changed permanently.
- Programmable ROM (PROM): It is also called fusible-link ROM. The setting of each bit is locked by fuse or antifuse. Rewriting is prevented and stored information is maintained permanently. The difference from ROM is that writing is performed after the device is fabricated.
- Erasable Programmable Read-Only Memory (EPROM): In order to program and erase, EPROM must be removed from circuit. EPROM is programmed electrically and erased by exposure to ultraviolet radiation.
- Electrically Erasable Programmable Read-Only Memory (EEPROM): Unlike for EPROM, information is stored and erased electrically in system. Not only can it be programmed/erased electrically, but also selectively by byte address.
- Flash Memory: Flash memory is a nonvolatile storage device that can be erased and programmed by electrical pulse. Flash memory was developed as combined features of EPROM and EEPROM. A block, sector or page consisting of a large number of memory cells can be programmed or erased at the same time.

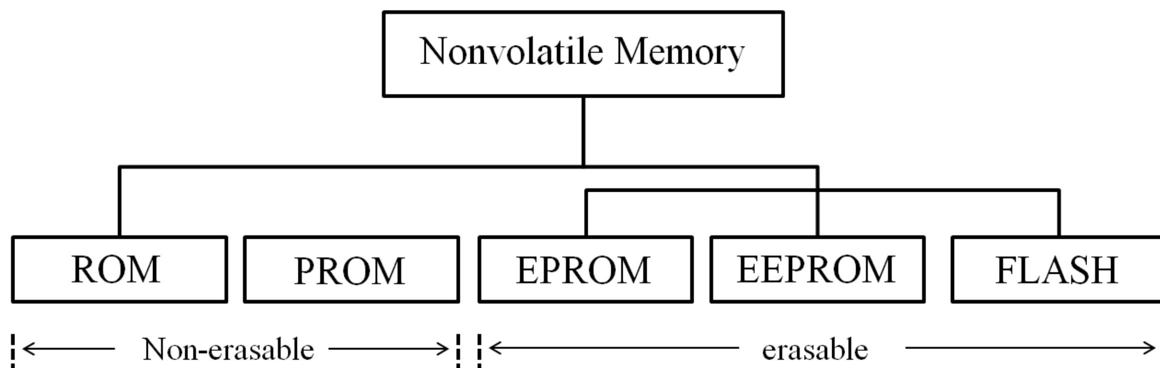

Fig. 4-1: Classification of nonvolatile memories.

4.2.2. Flash memory cell

Flash memory was invented by Masuoka at Toshiba in 1980. The name of "Flash" was suggested because the erasing operation takes place in a large block. Several types of flash architectures have been proposed [165-168]. They can be divided in terms of access type (parallel or serial) and programming/erasing mechanisms (Fowler-Nordheim tunneling, hot carrier injection, etc.). Among all of the flash architectures, nowadays two are considered as industry standards: (i) NAND flash which, provides only serial access but higher density and low cost [168, 174], therefore, it becomes the dominant technology for data storage and memory cards, and (ii) common ground NOR flash is a mainstream technology for embedded memories which require random memory access of the stored data [175, 176]. The "NOR" and "NAND" flash names are related to the way the cells are arranged in an array, through rows and columns in NOR/NAND like structure. Notice that NOR flash cell is usually programmed by hot carrier injection and erased by Fowler-Nordheim tunneling whereas NAND flash only utilizes Fowler-Nordheim tunneling for both programming and erasing.

(a) Conventional flash cell structure

Fig. 4.2 shows a conventional flash cell structure. This cell is composed by a floating gate (FG) surrounded by insulator and a transistor which is electrically governed by the coupled control gate (CG). The FG, electrically isolated, acts as the additional electrode for the flash cell: the charges injected and maintained in the FG lead to the modulation of the threshold voltage V_{TH} (seen from the CG) of the transistor. Once the charges are injected in the FG, the tunneling and blocking dielectrics become efficient potential barriers. Obviously, the reliability of the device is guaranteed by the quality of the dielectrics, especially the

tunneling oxide located between the FG and the transistor channel. In order to allow carrier tunneling through it with reasonable bias level while preserving the retention of the cell, its thickness is usually in the range of 6-7 nm.

The most successful device in flash memory category is the SONOS (Semiconductor-Oxide-Nitride-Oxide-Semiconductor) type architecture, in which the insulator consists of a silicon nitride layer enveloped by silicon oxide (SiO_2) layer. The main advantages of SONOS architecture are scalability and simple fabrication process [177]. The replacement of the floating gate with a trapping medium like nitride allows an easier integration (compared to the former poly-Si FG approach), preserving the storage medium from subsequent process. Moreover, the entire thickness of the gate stack is decreased, reducing voltage and time for the programming/erasing operation.

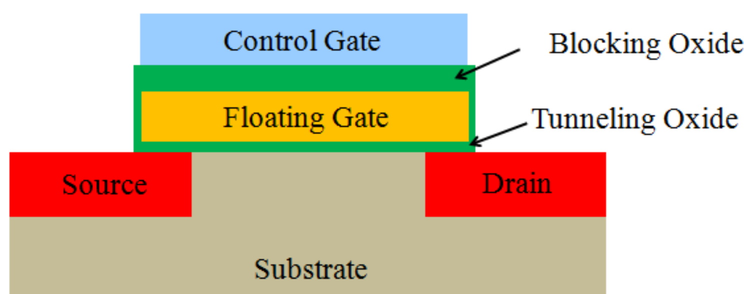

Fig. 4-2: Cross-section of a conventional floating gate flash cell.

(b) Reading operation

The stored information in a flash cell can be determined by measuring the threshold voltage of the transistor. The most common method is the reading of the current at a fixed control gate bias. As shown in Fig. 4-3, logic “1’ and “0” are determined according to the threshold voltage variation (ΔV_{TH}) that is proportional to the charges stored in the FG: “0” and ‘1’-states refer to erased and programmed states. Hence, once an appropriate amount of charges is stored and the corresponding ΔV_{TH} defined, the choice of the reading voltage can be performed. The current of the ‘1’-state is defined as the high level while the ‘0’-state or low level current is almost zero. Therefore, in flash cell, the logical state ‘1’ is achieved with positive stored charges (or no electron charge) in the FG providing a large reading current. By contrast, the logical ‘0’-state is completed with electron charge leading to zero reading current.

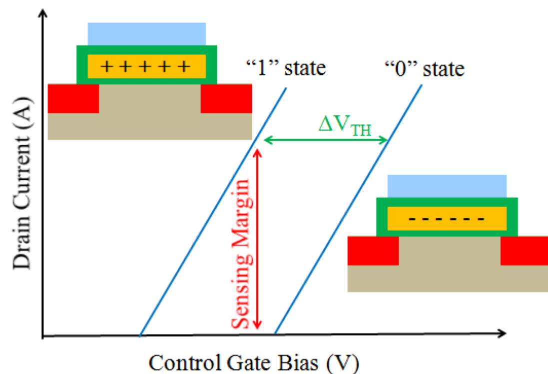

Fig. 4-3: Floating gate flash cell reading principal.

(c) Programming/Erasing operation

Today, two programming/erasing mechanisms are used for commercial standard: hot-carrier injection and Fowler-Nordheim tunneling.

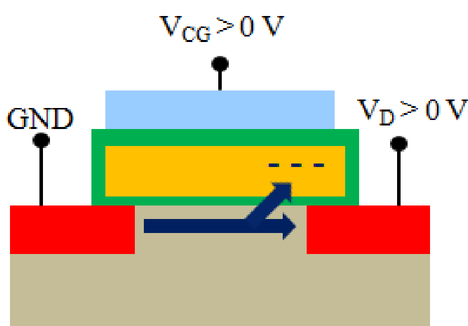

Fig. 4-4: Scheme of the hot carrier injection for NOR flash programming operation.

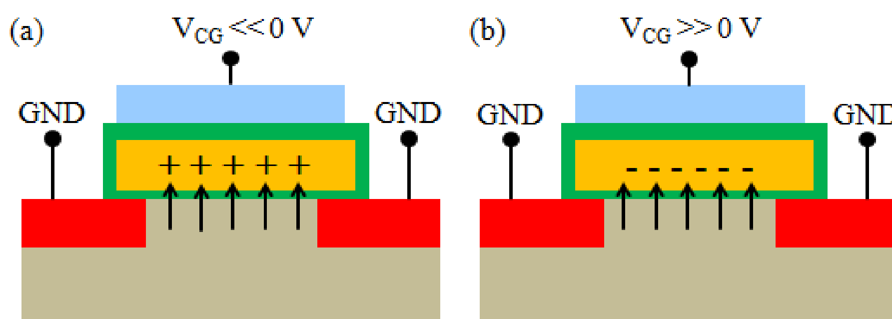

Fig.4-5: Scheme of the Fowler-Nordheim tunneling for NAND flash (a) programming and (b) erasing operation. NOR flash also use FN tunneling for erasing.

(i) Hot-Carrier Injection (Fig. 4-4): a bias is applied at the CG to activate the channel of the transistor while a high drain voltage allows to achieve the saturation mode ($V_D >> V_{CG} - V_{TH}$). When the electrons move from source to drain, if the drain voltage is

sufficiently high, they obtain enough energy to turn into hot carriers due to the longitudinal electric field induced in the drain pinch-off region. If their energy level exceeds the oxide-silicon energy barrier, they can be injected into the floating gate. Note that the injected electrons are mostly located near the drain terminal.

(ii) Fowler-Nordheim tunneling (Fig. 4-5): the quantum-mechanical tunneling through the insulator is induced by a strong vertical electric field. Charges can move from/into the body into/from FG across an oxide, the thickness of which is sufficiently thin to allow turning on tunneling transport without destroying its dielectical properties. Positive charges are injected by applying negative CG bias. Vice versa, positive CG bias leads negative charge injection into the FG.

(c) Reliability

Flash cell has to satisfy two main properties: one is endurance and the other is retention. Commercial specifications require that the cell still operates properly after 10^5 program/erase cycles and data retention longer than ten years.

(i) *Programming/Erasing endurance.* Cycling is known to cause a degradation of the cell properties, mainly due to the deterioration of the tunneling oxide, which limits the endurance characteristics [178]. Actually, endurance problems are mostly given by single-cell failure after program/erase cycles. The evolution of the programmed/erased threshold voltage mirrors the variation of the net fixed charge in the tunneling oxide. In particular, in NOR flash cells, the variation of the threshold voltage with cycling comes from the generated traps in the tunnel oxide and at the interface near the drain side of the channel [179]. This phenomenon is known as hot electron degradation. The damage generated by charge injection during F-N tunneling programming concerns the degradation of the NAND cells. Cycling wear-out should be reduced by appropriate device fabrication and by optimization of the tunneling oxide processing.

(ii) *Data retention.* The loss of stored charges in the FG should be as low as possible to obtain sufficient retention time. The main reason of charge loss is the defects in dielectrics (especially tunneling oxide) [179]. Primarily, the defects in the tunneling oxide are generated by the cell programming/erasing. The parasitic leakage current, caused by oxide defects, degrades the retention time. Therefore, the optimized processing of the tunneling oxide is an essential factor to achieve a reliable flash cell.

4.2.3. Future evolution of flash memory cell

The scaling of the flash cell has been straightforward in the last twenty years. However, both NOR and NAND flash cells face technological challenges for further scaling down to sub 22 nm technology node. Since many generations, a NOR cell is larger than a NAND one. The different cell size results from the array organization and the cell layout. In a NOR cell, every two cells share a contact for random access capability. Therefore, it needs more lithography to define the cell. Moreover, the hot-carrier injection programming does not permit an aggressive scaling of the cell gate length. On the other hand, the main physical limits that frustrate further scaling of the NAND cells are: (i) the cell to cell interference due to the parasitic capacitive coupling between two neighboring floating gates and (ii) the degradation of the cell driven by the control gate [180].

The channel shrinking will also be restricted by the tunneling oxide scaling and the inter gates oxide-nitride-oxide stack. Tunneling oxide thickness reduction is limited by cell reliability, primarily after many programming/erasing cycles. The thinning of the tunneling oxide layer improves the memory window and programming speed, but results in retention time degradation. A high field stress on thin oxide increases the leakage current density at low electric field that is known as stress-induced leakage current (SILC) [181, 182]. SILC is accentuated in thinner oxide (tunneling oxide in flash cell) and can give rise to bit failure and retention time degradation. Cell programming is also limited by erase saturation due to parasitic charge injection from the control gate through blocking oxide, balancing the hole injection from the substrate [183]. SONOS architecture is not free from these issues for sub 22 nm technology nodes.

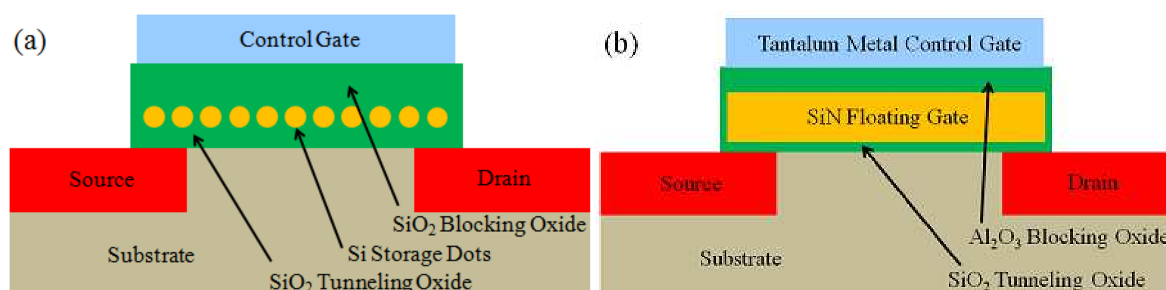

Fig. 4-6: Evolved architectures of floating gate flash cell: (a) the nanocrystal cell [184] and (b) the TANOS cell [187].

In order to overcome scaling limitations, while maintaining the high integration density, silicon nanocrystal floating gate architecture has been proposed (Fig. 4-6a) [184]. It exhibits deeper electron storage trap (~ 3 eV) than nitride (1~2 eV), longer charge retention time, less temperature sensitivity and fast programming/erasing speed. However, nanocrystal floating gate has several weaknesses like: (i) small threshold voltage shift, (ii) existence of percolation paths between source and drain, (iii) not enough nanocrystal dots when the channel length is shortened leading to retention degradation. This technology requires very complex fabrication procedure and careful control of the nano-dot size, dimension, shape and density because these are critical elements for the performance and reliability of the memory cell [185, 186].

In 2003, an evolved structure was reported based on SONOS concept [187]. The control gate and block oxide of SONOS device were replaced with tantalum metal gate and Al_2O_3 high-k materials. This structure prevents the gate electron injection during erasing operation, improving the erase saturation problems. According to the inventors, it allows a relatively thicker tunneling oxide and avoids the retention issue. However, the proposed structure is far from being straightforward since it includes the adoption of several new materials (high-k blocking oxide and metal gate). Careful optimization of the charge trapping cell is required for the success of next flash generation.

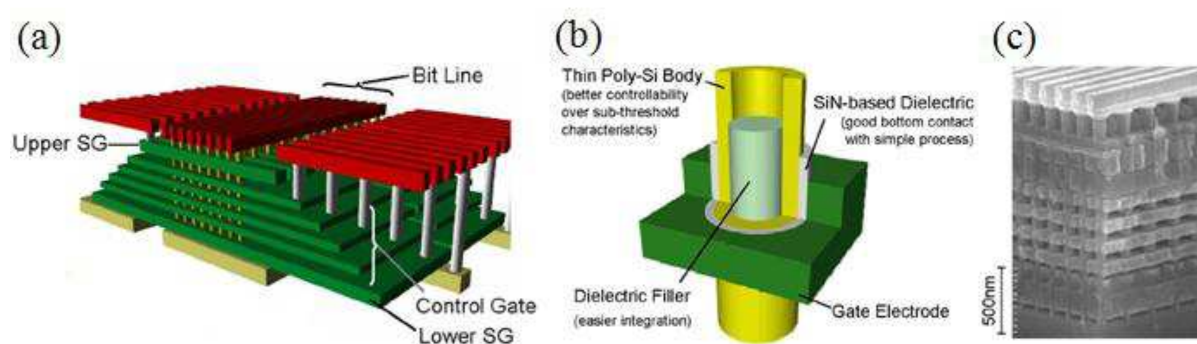

Fig. 4-7: 3D flash memory architecture [188]. (a) Birds-eye view of BiCS flash memory, (b) concept of 'Macaroni' body vertical FET and (c) birds-eye view SEM image of BiCS memory.

In 2007, in order to achieve ultra-high density, Bit-Cost Scalable (BiCS) flash memory was proposed by Toshiba [188]. Stacked electrode plates are connected all together by poly-silicon. Single-bit, selected by a bit line and select gate SG, is accessed at the cross point of a memory string and control gate plate. A series of vertical FETs is formed and NAND operation is possible with SONOS-type memories. Macaroni-shaped body is completed by

the deposition of very thin poly-silicon on the gate dielectric. At the center of the body, dielectric filler is employed for an easier integration process. Thinner body thickness provides better controllability of the subthreshold characteristics of depletion-mode polysilicon transistors. This architecture opens the path for three-dimensional integration for dense NAND arrays, but requires very complicate integration processing.

4.2.4. Alternative nonvolatile memory

In addition to charge trap flash memories, new physical mechanisms and new materials are under investigation today for nanoscale memories. In order to overcome the performance and scalability issues of the floating gate device, several innovative architectures have been proposed as alternative nonvolatile memories. They are briefly described to complete a wide-angle view of the NVM landscape.

(a) Ferroelectric RAM (FeRAM)

FeRAM has been commercialized despite the technology is more relaxed than for flash memory. Ferroelectric materials (PZT: $PbZr_xTi_{1-x}O_3$, SBT: $Sr_{1-y}Bi_{2+x}Ta_2O_9$, BLT: $Bi_{4-x}La_xTi_3O_{12}$) are spontaneously polarized by an electric field via lattice deformation. In PZT FeRAM, the polarization of Ti atoms can be changed by an electric field between two stable positions.

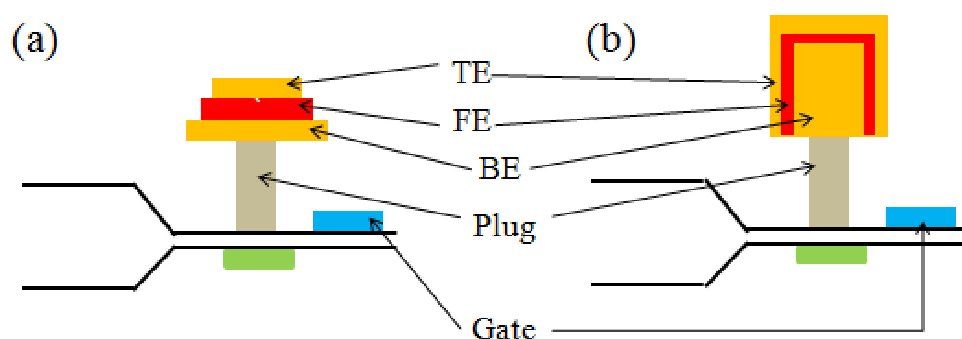

Fig. 4-8: FeRAM cell. (a) 2D FeCAP and (b) improved 3D FeCAP [189]. TE, FD and BE are the top electrode, the ferroelectric layer and the bottom electrode, respectively.

The cell architecture (Fig. 4-8) is similar with DRAM (1 Transistor / 1 Capacitor). FeRAM programming is accomplished by the voltage applied to the capacitor plates. According to the polarity, '1'- or '0'-state is set. The main benefits of FeRAM are fast read (<

100 nm) and programming (< 100 ps), good endurance (> 10^{12} cycles) and low-power consumption [189].

FeRAM faces scaling issues. Shrinking the cell size and capacitor surface degrades the read signal, leading to complicated 3D capacitor structure (Fig. 4-8b). In addition, the materials tend to stop being ferroelectric when they are too small [190]. Another challenge is the integration of ferroelectric layers into a standard CMOS process.

(b) Magnetoresistance RAM (MRAM)

MRAM use the permanent magnetization of a ferromagnetic material to store the data. MRAM is composed of a thin oxide pass transistor, a single magnetic tunnel junction (MTJ), top and bottom sense electrodes and tow orthogonal program (bit and digit) lines. The MTJ are formed by two ferromagnetic (pinned and free) layers, separated by a thin tunnel barrier. One plate (pinned layer) is a permanent magnet set to a particular polarity, the other (free layer) has the polarity changeable by external magnetic field generated by the current flowing in the bit and digit lines. Reading is performed by measuring the MJT electrical resistance. If the polarity of the two magnetic layers enters in parallel alignment, the resistance is low ('1'-state). By contrast, an anti-parallel alignment of the two layers results in a high resistance ('0'-state). Fig. 4-9 shows the MRAM architecture [191].

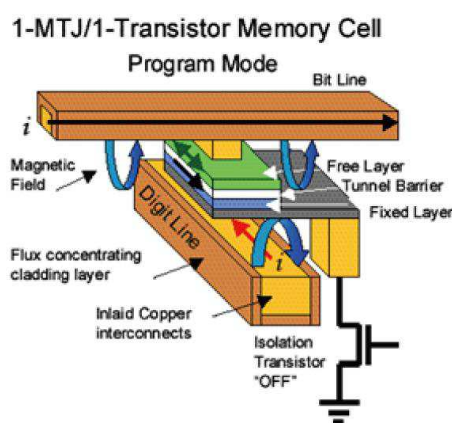

Fig. 4-9: MRAM cell, schematically showing the programming operation mode [191].

MRAM offers non-destructive read with a very fast access time, radiation hardness and excellent read/write endurance (> 10^{14} cycles for write-intensive storage). Main disadvantages are: high write current [185], power consumption and scaling. Data retention ability depends on the total volume of magnetic material in the free layer [185]. Additionally

in high density MRAM arrays, the induced field can overlap the adjacent cells, leading to potential false writes.

(c) Resistive RAM (RRAM)

RRAMs utilize various kinds of dielectric layers as an insulating or semiconducting component sandwiched between metal electrodes to make a capacitor-like structure [192]. The concept is that the current though the dielectric can be changed in a reversible fashion by applying short voltage (or current) pulse (< 100 ns). The mechanism is not completely clarified yet. According to the resistance of the storage layer, '1'- or '0'-state is distinguished. There are two types of RRAM, based on the unipolar/bipolar resistive switching in a binary oxide layer (Fig. 4-10a) [193] or on the bipolar dissolution of a conductive path into a solid electrolyte (Fig. 4-10b) [194].

RRAM exhibits a good read signal window and scalability [195]. The critical issues is the statistical variation of programming voltage/current and programmed resistance. Retention ability (for 10 years at 85 °C) has still to be demonstrated [185].

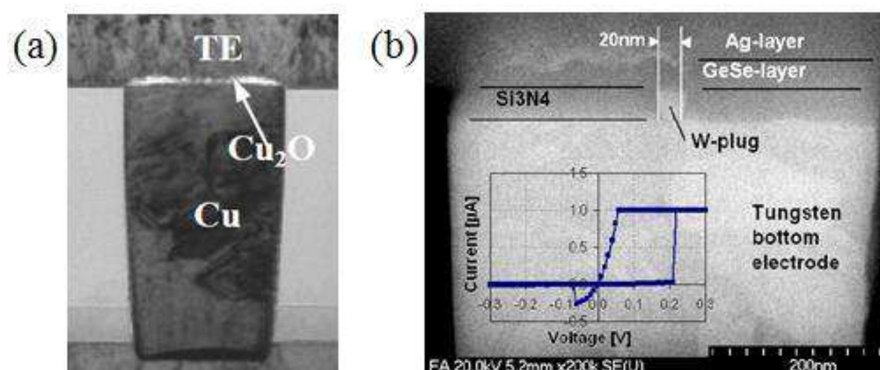

Fig. 4-10: TEM cross-sections of (a) a MRAM cell based on Cu_2O binary oxide [193] and (b) 20 nm conductive bridging RAM (CBRAM) with the corresponding I/V curve [194].

(d) Phase change memory (PCM)

PCM uses the unique ability of alloys based on chalocogenides (especially, GeSbTe) [196, 197] to be stable in both the crystalline (low resistance) and amorphous (high resistance) phases. The most fascinating property of this material is the reversible switch between two stable phases. Local temperature increase by Joule effect is employed to change the two states. Above the critical temperature, the crystal nucleation and growth occur and lead to the crystalline phase. The amorphous state is restored by increasing the temperature

over the melting point and subsequent quick cooling down. Therefore, programming requires a relatively high current to heat up and change the local phase. Basically, the PCM cell has 1 Transistor and 1 Resistor (1 T/1 R). Fig. 4-11 shows two different types of PCM cell architectures [198, 199].

PCM offers fast writing, good endurance (>10^{12}) [185], low-voltage reading and superior data retention (300 years at 85 °C) [200]. The integration of chalocogenide alloys into a standard CMOS process is still a challenge.

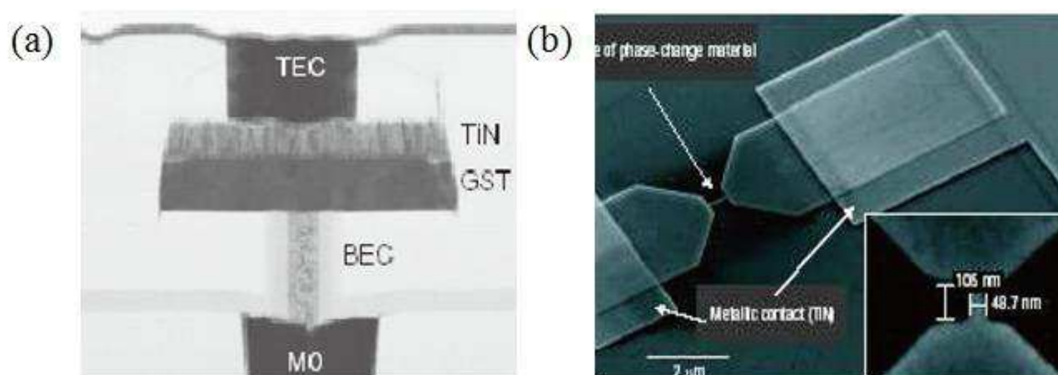

Fig. 4-11: PCM cell architecture proposed by (a) Horii *et al*. [198] and (b) Lankhorst *et al*. [199].

4.3. Charge Trapping in Si_3N_4 Buried Layer

In this section, we introduce the device structure under test: FinFETs fabricated on ONO buried layer. We also describe the action of the injected charges in the nitride buried layer on the drain current behavior.

SOI wafers with $SiO_2/Si_3N_4/SiO_2$ multi-layer buried insulator were used as starting material. Wafers with ONO BOX were fabricated with the Smart-Cut™ technology. The multi-layer BOX was composed of SiO_2 (2.5 nm), Si_3N_4 (20 nm) and SiO_2 (70 nm), from top to bottom. Si_3N_4 is an appropriate material for flash memory due to the large density of traps, but Si–Si_3N_4 interface degrades the transistor performance [162]. This is why the Si_3N_4 buried layer was sandwiched within two SiO_2 layers. The upper SiO_2 layer is very thin (2.5 nm) and enables carrier tunneling. The Si film thickness was 65 nm which defined the fin height. Hydrogen annealing was performed to smooth the fin sidewalls. The front-gate oxide thickness is 1.8 nm. TiSiN grown by LPCVD was used as gate material. The fabrication was completed with conventional CMOS process modules. To investigate the effects of geometrical parameters, FinFETs with variable gate lengths L_G and fin widths W_F were

processed at Texas Instruments (USA). The finished devices have fin widths narrower by about 45 nm than the masked-defined widths. The number of fingers N_F connected in parallel varies from 1 to 100. For direct comparison, reference FinFETs with standard SiO_2 BOX were processed in the same lot. All fabricated devices have undoped body and operate in fully-depleted mode. Fig. 4-12 shows the structure and TEM cross-section of the SOI FinFETs fabricated on the ONO buried layer.

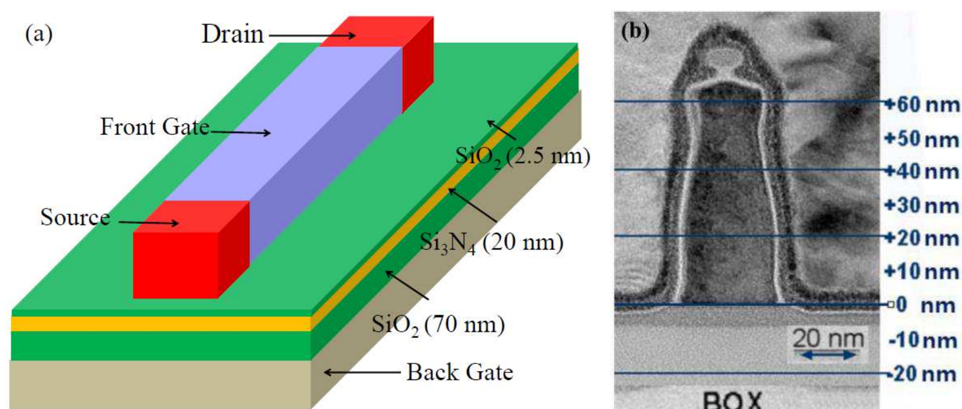

Fig. 4-12: (a) Device structure and (b) TEM cross-section of the SOI FinFET fabricated on the ONO buried layer. The ONO stack features SiO_2 (2.5 nm), Si_3N_4 (20 nm) and SiO_2 (70 nm) layers, from top to bottom.

The Si_3N_4 buried layer can trap charges according to the bias condition and fabrication process. These trapped charges in the nitride buried layer change the device characteristics such as threshold voltage, mobility and subthreshold swing [201]. In Fig. 4-13, we compare the characteristics of standard SiO_2 BOX and ONO buried insulator. In Fig. 4-13a, the front-channel threshold voltage observed in the ONO FinFET is lower than in standard SiO_2 BOX devices. Indeed, during the fabrication process, positive charges were trapped in the Si_3N_4 buried layer [162] making the body potential to increase and the front-channel threshold voltage to decrease.

In Fig. 4-13b, we can see a hump in the transconductance curve around $V_{FG} = 0$ V. This hump arises from the activation of the back-channel which can be easily turned on by the positive trapped charges in the Si_3N_4 buried insulator. This explains why the parasitic back-channel and the hump in the transconductance curve are observed only for ONO FinFET. The parasitic back-channel leads to a lateral shift (about 450 mV) of the subthreshold characteristics (Fig. 4-13a), larger than the actual shift of the front-channel threshold voltage (~ 150 mV) as we can deduce from Fig. 4-13b. The charges trapped in the Si_3N_4 layer during processing can be reset by using proper bias condition.

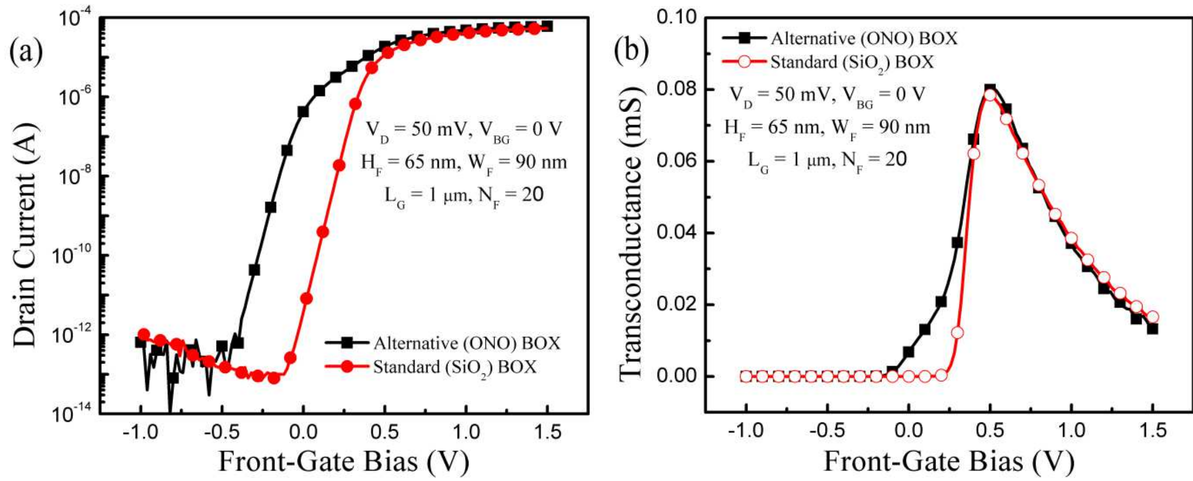

Fig. 4-13: Comparison of (a) drain current and (b) transconductance characteristics between FinFETs with standard (SiO_2) buried insulator and ONO buried insulator.

History effects can be generated by back-gate bias V_{BG} higher than ±15 V. In Fig. 4-14a, $I_D(V_{FG})$ curves are measured for different back-gate biases. The back-gate voltage is consecutively changed in the following sequence: 0 V, +15 V, 0 V, -15 V and 0 V. The front-channel threshold voltage V_{THF} is lower at positive back-gate bias (+15 V) due to the electrostatic coupling between the gates. Therefore, the drain current curve shifts to the left. By contrast, V_{THF} increases for a negative back-gate bias and the drain curve moves to the right. This behavior reflects the standard coupling effects in triple-gate FinFETs (Chapter 2.2) [82, 202].

The key point is that the $I_D(V_{FG})$ curves are not superposed when measured again at V_{BG} = 0 V. This demonstrates that nonvolatile charges are effectively trapped in the buried nitride layer. The charges, trapped in the ONO BOX during back-gate biasing, modify V_{THF} by electrostatic gate coupling. Negative charges are trapped in the Si_3N_4 buried insulator by applying a positive back-gate bias. The body potential drops and the front-channel threshold voltage V_{THF} is increased. Hence, the drain current curve is shifted to the right compared to the initial condition. When positive charges are trapped in the nitride layer with a negative back-gate bias, the body potential is raised and V_{THF} decreases. This is why the drain curves are not overlapped when repeating measurement at V_{BG} = 0 V after previous positive or negative back-gate biasing.

Fig. 4-14b shows the transient effect induced by a back-gate bias pulse sequence. We changed V_{BG} level as a function of time (positive, zero, negative and zero values). During a negative back-gate pulsing, the current is zero but positive charges are being trapped in the

nitride buried layer. Therefore, the drain current level is increased when subsequently measured, at V_{BG} = 0 V. During a positive back-gate pulsing, not only is the current high but also negative charges are trapped in the buried nitride. Due to the extra negative charges, the drain current level becomes negligible during the next reading at V_{BG} = 0 V. Consequently, when the back-gate bias is switched to zero from a positive value (body potential drop), the drain current level is much lower than for switching to zero from a negative bias (body potential increase). This is a typical history effect: the drain current level measured at V_{BG} = 0 V is affected by the previous back-gate condition. Another important feature is the dependence of drain current level at V_{BG} = 0 V on the magnitude of the previous back-gate pulse. This indicates that the amount of trapped charges is modulated by the value of back-gate voltage.

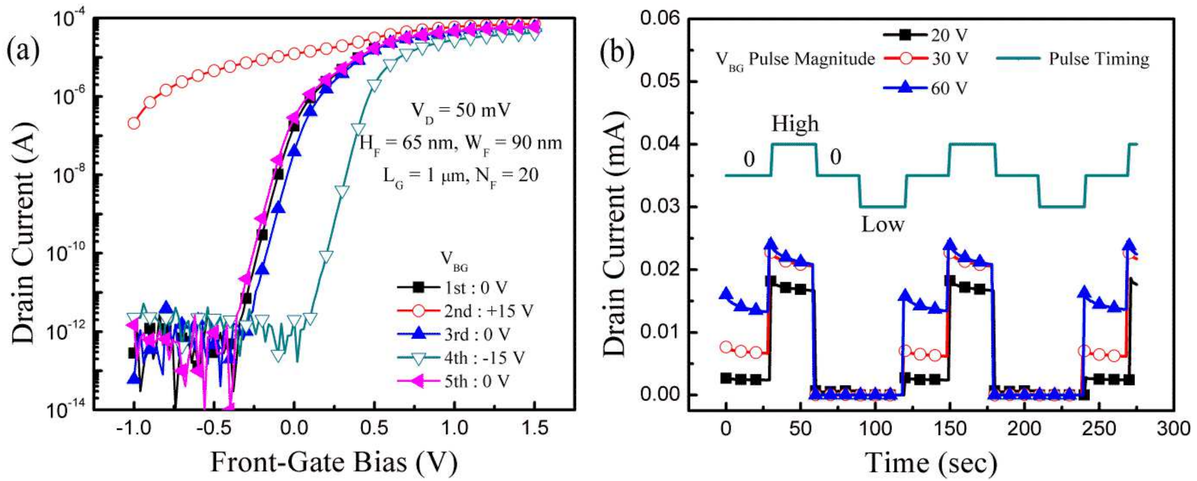

Fig. 4-14: History effects by charge trapping in nitride layer. (a) Drain current versus front-gate bias, measured five times as the back-gate bias was changed in order of 0 V, +15 V, 0 V, -15 V and 0 V. (b) Transient current after applying a sequence of pulses to the back-gate. V_{FG} = 0 V, V_D = 50 mV, W_F = 90 nm, L_G = 1 μm, N_F = 100.

In Fig. 4-14b, drain current overshoots occur when the back-gate bias is changed from 0 V to positive voltage or from negative voltage to 0 V. The front-gate is maintained at 0 V and the back-gate is driven into (strong) inversion. This overshoot is a well known floating-body effect (FBE) in SOI [43]. Actually, majority carriers, accumulated during the switch in the floating body and at the front-interface, cannot be removed instantly from the body. The body potential is increased and the back-channel threshold voltage is lowered due to the excess of majority carriers stored in the FinFET body. Thereby, a drain current excess flows temporarily. The drain current overshoot reflects not only the recombination process of excess holes [43] but also a reverse current at the body/drain (and body/source) junctions

when the device returns to steady-state.

4.4. Nonvolatile Memory Effects

4.4.1. Nonvolatile memory effects induced by back-gate bias stress

We have seen that the nitride layer can trap charges by high back-gate biasing. In that case, the charge trapping mechanism is Fowler-Nordheim (F-N) tunneling [203]. Tunneling occurs from/into the fin body into/from the nitride layer through the 2.5 nm thin SiO_2 buried layer. Applying a strong vertical electric field (by high back-gate bias) enables carrier tunneling through the 2.5 nm oxide layer without damaging its dielectric properties. The trapped charges primarily change the back-channel properties, in particular the back-channel threshold voltage [204-206]. As our devices are fully-depleted (FD SOI), the front-channel characteristics such as threshold voltage, mobility, subthreshold slope, etc can be modified via gate coupling effects [14], following the amount of trapped charges in the nitride layer. Especially, the shift of $I_D(V_G)$ curve, resulting from charge trapping/detrapping, will be applied for flash memory purpose.

Fig. 4-15 shows the memory effect induced by charge trapping in the ONO BOX. $I_D(V_{FG})$ curves were measured at V_{BG} = 0 V after charge trapping/detrapping into/from the Si_3N_4 layer (Fig. 2-15a). During the 30 s stress at V_{BG} = +50 V and -50 V, the charges (electrons) are respectively trapped and detrapped. The front-channel threshold voltage variation ΔV_{THF} after programming depends on the polarity and magnitude of the back-gate bias. After 30 s stress at V_{BG} = -50 V, the net positive charge in the nitride (*i.e.*, the detrapped electrons or trapped holes) makes the body potential increase. Therefore, the front-channel threshold voltage decreases. By contrast, stress at V_{BG} = +50 V results in a net negative charge (trapped electrons or detrapped holes) in the nitride which decreases the body potential, the front-channel threshold voltage increases.

Fig. 4-15b depicts the effect of trapped/detrapped charges on the $I_D(V_D)$ characteristics. Applying V_{BG} = -50 V, a high drain current (‘1’-state) is programmed by positive charge trapping. The ‘1’-state is erased by applying V_{BG} = +50 V. The difference of the drain current between ‘1’-state and ‘0’-state is large enough for flash memory operation (> 0.4 V, [207]). Note that the amount of positive charges trapped in the nitride dielectric for V_{BG} = -50 V is

sufficient to activate the back-channel.

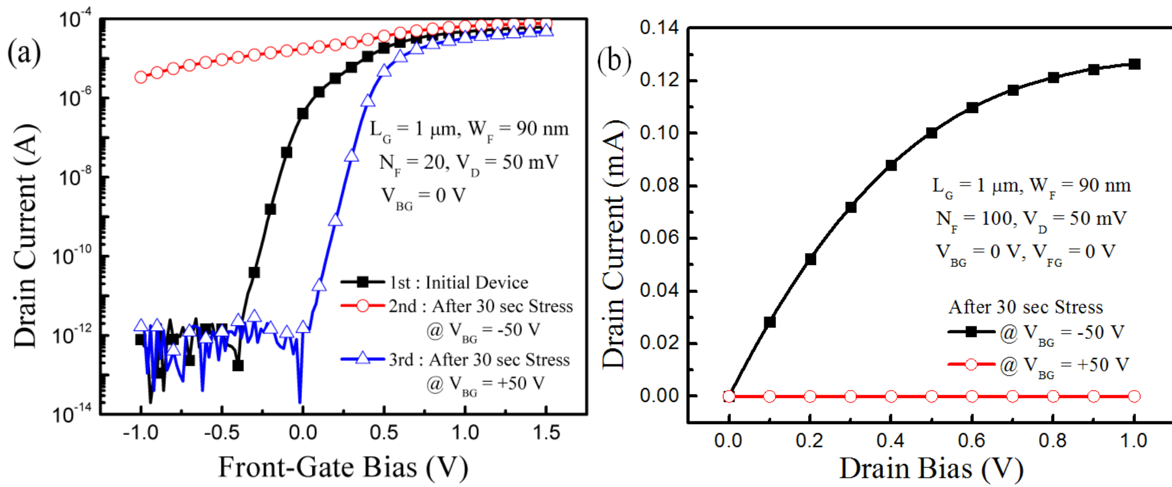

Fig. 4-15: Typical memory effects induced by back-gate biasing. (a) Drain current as a function of front-gate bias and (b) drain bias, measured at V_{FG} = V_{BG} = 0 V after programming with V_{BG} = ±50 V. Front-gate, drain and source were grounded during stress.

As a general remark, it is noted that the substrate voltage required to charge the nitride layer is very large simply because the BOX (not especially conceived for memory application) is too thick. We used high V_{BG} and long stress in order to maximize the trapped charge and clearly reveal the main mechanisms. Thinning down the BOX, which is the universal trend in advanced SOI technology, will naturally lower the substrate bias below 10-15 V. For example, the block-oxide thickness can be reduced by a factor of ten down (to 7-10 nm) and the nitride layer can be only 5-10 nm thick [208-210], bringing the total BOX thickness below 20 nm. The thickness optimization for the tunneling oxide (2-3 nm) is matter of trade-off between programming speed and long retention.

An important feature of our FinFlash is the impact of trapped charges which depends on the geometrical parameters. Fig. 4-16 shows the influence of the gate length L_G on the memory effect induced by high back-gate bias. After 30 s stress with V_{BG} = ±50 V, the drain current variation is much larger in 100 nm device than in 1 μm devices in Fig. 4-16a. The drain current sensing margin (ΔI_D), required for flash memory application, is defined as the difference between the two current levels measured at V_{FG} = 0 V after stress with V_{BG} = -50 V and V_{BG} = + 50 V. As shown in Fig. 4-16b, ΔI_D increases rapidly under 500 nm gate length.

These size effects can be explained by 3D coupling mechanisms [80, 211]. The ‘longitudinal’ coupling component is induced by drain bias. This mechanism, named drain-induced virtual substrate biasing (DIVSB) is due to the penetration of the longitudinal field

from drain/source into the BOX. DIVSB reduces the ability of the lateral gates to control the potential at the back interface (fin-BOX), especially near the drain terminal. Longitudinal coupling opposes the 'lateral' coupling (between the side gates) and therefore favors the 'vertical' coupling between back gate (or ONO charges) and front channel. This phenomenon is obviously increased in short device (see inset in Fig. 4-16b). Indeed, in short device, drain current level is larger than in long one, boosting the effect of injected charges. As a result, for shorter devices, the sensitivity of the back-surface potential to trapped charges is enhanced. The memory effect amplification observed for shorter device is an outstanding result for the memory scaling.

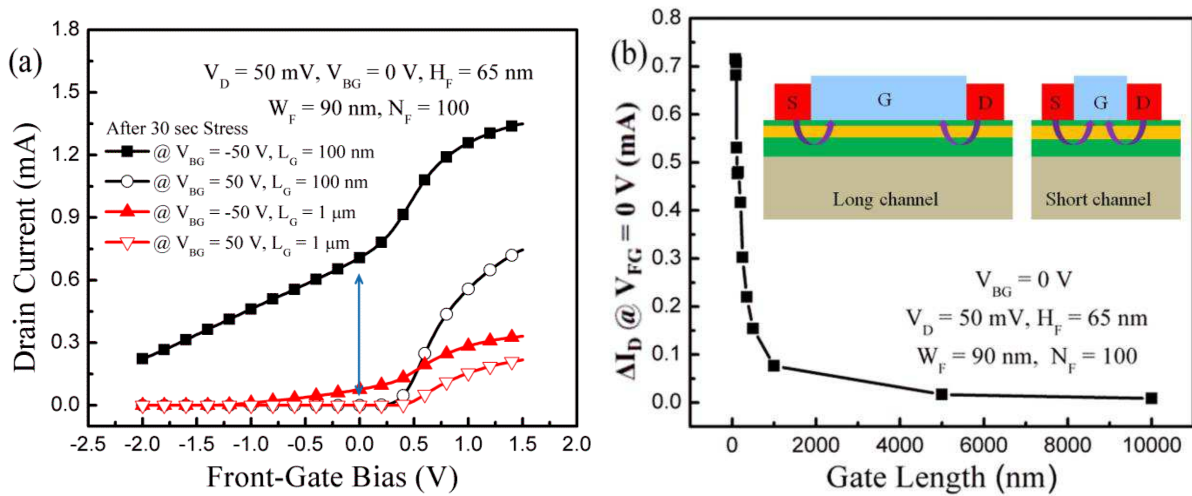

Fig. 4-16: Effect of gate length on sensing margin. (a) After charge trapping with $V_{BG} = \pm 50$ V, drain current versus front-gate bias and gate length. (b) Sensing margin versus gate length. The sensing margin is defined as the difference of post-stress drain current levels at $V_{FG} = V_{BG} = 0$ V. Inset in Fig. 4-16 is cross-section of ONO FinFET showing the effect of DIVSB in long and short channel.

The memory effect also depends on fin width as shown in Fig. 4-17. For wider fin device, ΔI_D is larger (Fig. 4-17a). The variation of the current sensing margin with width is illustrated in Fig. 4-17b. When the fin width increases, the origin of ΔI_D increase is twofold: (i) the area in the nitride buried layer which can trap the charges increases, improving the capture section and (ii) the lateral coupling is attenuated [80, 211]. In particular, the role of the two lateral gates is to control back-surface potential and block the effect of substrate biasing or trapped charges. For wider fin device, the lateral coupling component is reduced and the impact of trapped charges in the buried nitride is increased (see inset in Fig. 4-17b). Thereby, the memory effect increases for wider fins.

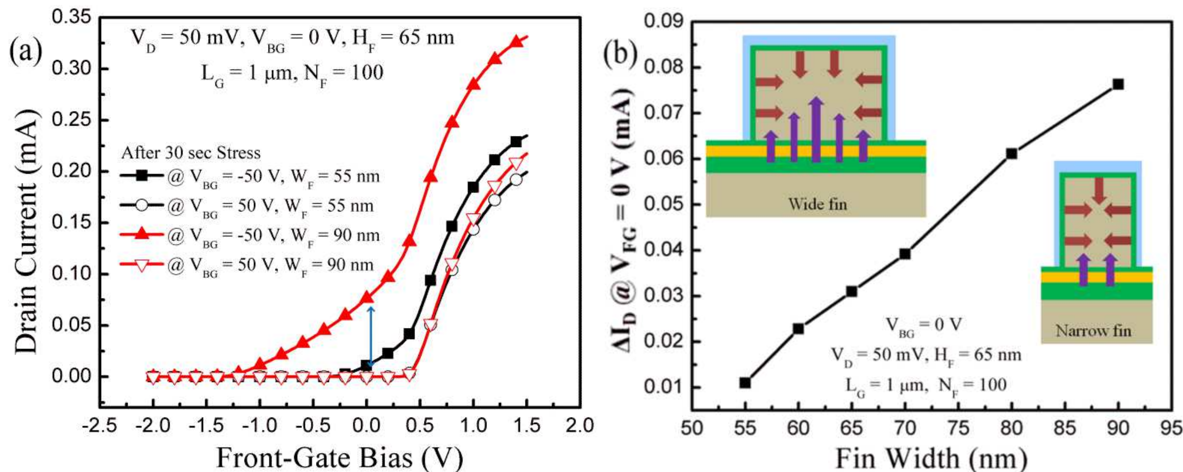

Fig. 4-17: Effect of fin width on sensing margin. (a) Drain current versus front-gate bias and fin width, measured at V_{BG} = 0 V after charge trapping with V_{BG} = ±50 V. (b) Sensing margin defined as in Fig. 4-16, versus fin width. Inset in Fig. 4-17 is cross-section of ONO FinFET showing the effect of injected charges in wide and narrow fin.

Fig. 4-18 shows the effect of trapped charges on the drain current *vs.* front-gate $I_D(V_G)$ characteristics at various temperatures when a high constant back-gate stress is applied. Like for the Fig. 4-15a, the drain current becomes ‘high’ after applying a negative back-gate bias due to the positive trapped charges in the nitride (Fig. 4-18a) and vice versa.

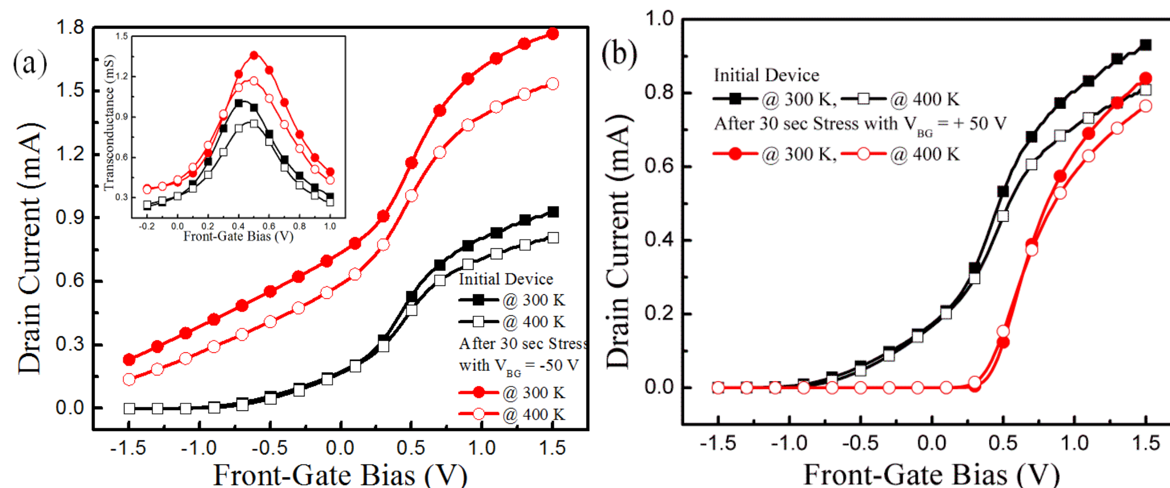

Fig. 4-18: Effect of back-gate biasing at different temperature. Drain current and transconductance (inset) versus front-gate bias measured at V_{BG} = 0 V after 30 sec stress with (a) V_{BG} = -50 V and (b) V_{BG} = +50 V. L_G = 80 nm, W_F = 90 nm, V_D = 50 mV, N_F = 100.

The shift of $I_D(V_G)$ curve depends on temperature. The drain current level is lower at 400 K than at 300 K, despite a decrease in threshold voltage. This phenomenon is clarified by the transconductance curve (inset Fig. 4-18a). At higher temperature, the transconductance maximum value is decreased. This indicates that phonon scattering is increased, reducing the

electron mobility and drain current level [212].

Fig. 4-19 shows the effect of the gate length and temperature on ΔI_D (measured at V_{FG} = 0 V). As for Fig. 4-16, ΔI_D increases in shorter length device due to enlarged DIVSB. However, ΔI_D decreases by about 20% between 300 K and 400 K. The variation of ΔI_D induced by high back-gate biasing depends essentially on the 'high' state current. The reason is that the 'high' state current is much above the 'low' state current which is almost zero as we can see in Fig. 4-18. As the temperature increases, the 'high' state current level is lessened due to enhanced carrier scattering. Consequently, the global sensing margin ΔI_D is also reduced at higher temperature. However, the ΔI_D value is still large enough, confirming that the difference between charge trapping and detrapping remains detectable at 400 K.

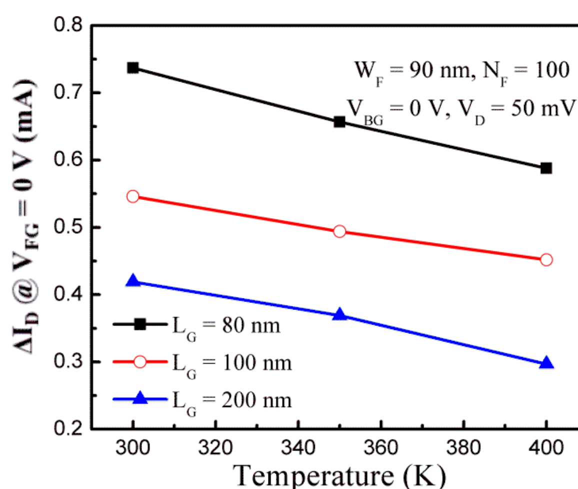

Fig. 4-19: Effect of temperature on the sensing margin induced by back-gate stressing. Sensing margin defined as in Fig. 4-16, versus temperature and gate lengths.

By measuring the transient drain current at V_{FG} = 0 V and V_{BG} = 0 V, the relaxation of trapped charge is monitored. As shown in Fig. 4-20, trapped charges in the buried nitride insulator are maintained for a long time (years), even if the devices were not optimized for flash memory. At higher temperature, the data retention characteristic is degraded by the Poole-Frenkel emission [213].

Such a long retention time is actually a benefit of using remote trapping in the BOX. The operation of our FinFlash with buried nitride differs from that of conventional flash cell where the charges trapped in the floating gate are sensed by the front-channel. In the case of FinFlash cell, the charges are trapped in the buried insulator while the sensing interface is located at front channel. This physical separation of the programming interface from the

reading interface can reduce the disturbance problem during reading of the memory, especially after many programming/erasing cycles.

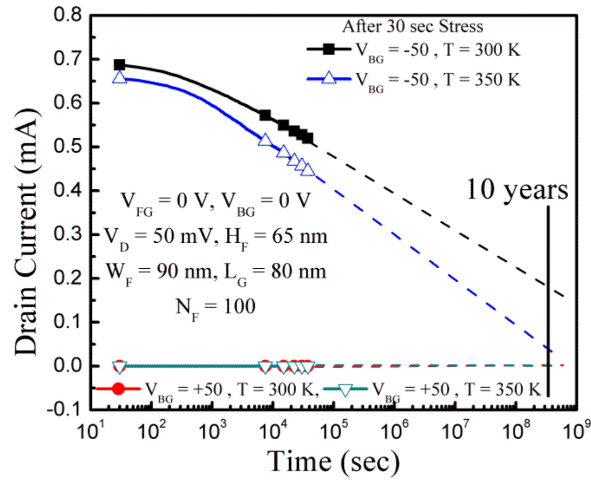

Fig. 4-20: Retention characteristics related to the release of trapped charges from the nitride layer. Drain current versus time, measured at T = 300 K and T = 350 K after charge trapping with $V_{BG} = \pm 50$ V.

4.4.2. Nonvolatile memory effects induced by drain bias stress

We discuss here another possible programming/erasing mechanism which avoids using high voltage substrate biasing. When an appropriate drain bias is applied ($|V_D| > 2$ V), the charges are injected/removed into/from the ONO BOX near the drain terminal. Carrier injection and trapping into the front-gate oxide is negligible as demonstrated by identical experiments performed on reference FinFETs with standard SiO_2 BOX. No variation in drain current was observed after identical stress, meaning that the memory effect is entirely attributable to the nitride layer.

This injection mechanism is somehow different from hot-carrier injection where positive drain and front-gate biases are needed to inject the electrons (*i.e.*, negative charges) into the floating gate. In our devices, the charges are efficiently injected into the buried nitride layer even when the front and back gates are grounded ($V_{FG} = V_{BG} = 0$ V, Fig. 4-21 ~ 4-28). Moreover, the polarity of the drain bias can define the type of trapped carriers. For positive drain bias (+2 V < $V_D \leq$ +3 V), positive charges are injected in the nitride insulator. In the opposite case, negative charges are injected by applying a negative drain bias (-3 V $\leq V_D <$ -2 V).

Fig. 4-21 shows $I_D(V_{FG})$ curves with two different injected charge polarities combined with two reading configurations. Positive and negative charges are injected by applying

respectively +2.5 V and -2.5 V at the drain terminal. Negative (resp. positive) injected charges lead to an increase (resp. decrease) in the front-channel threshold voltage V_{THF} locally, close to the drain. According to the polarity of the applied drain bias and the corresponding type (positive or negative) of injected charges, the front-channel drain current level turns into 'high' or 'low' state.

This carrier injection mechanism has two different origins following the drain bias polarity. When a positive V_D is applied (15 sec stress with V_D = +2.5 V), the FinFET operates next to the avalanche region and electron-hole pairs are generated by impact ionization. Hence, electrons are removed from the nitride by F-N tunneling and, simultaneously, hot holes can be injected into the nitride close to the drain region. The hot holes are injected into the Si_3N_4 buried insulator through the thin SiO_2 tunneling layer thanks to the local vertical electric field induced by the drain biasing.

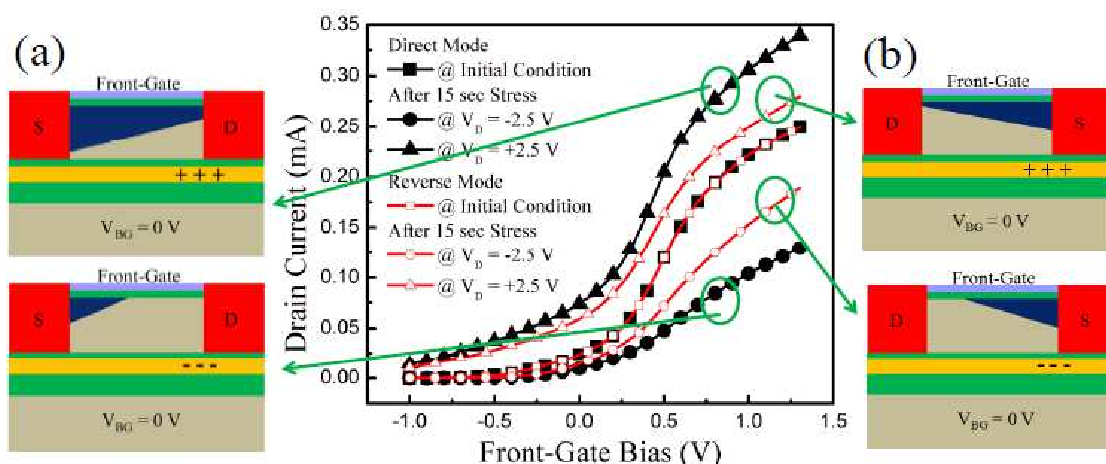

Fig. 4-21: Memory effect by drain bias. Drain current, measured in direct and reverse modes, as a function of front-gate bias at V_{BG} = 0 V, before and after 15 sec stress with V_D = ±2.5 V. During stress, front/back gates and source were grounded. (b) Reverse (drain-source) mode was measured after (a) direct (source-drain) mode. L_G = 100 nm, W_F = 90 nm, N_F = 16, V_{BG} = 0 V, V_D = 50 mV.

In the opposite case (V_D = -2.5 V), the drain-to-body junction is forward biased and the source-to-body junction is reverse biased (as in the parasitic bipolar transistor BJT used for the programming of capacitorless 1T-DRAM [214]). Impact ionization occurs near the source/body (collector/base) junction and in principle can also lead to carrier injection into the BOX. However, the vertical field near the grounded source is much lower than at the drain and insufficient to inject carriers into the nitride. In this respect, note that localized carrier trapping into the ONO is not visible, even near the drain terminal, for drain bias below +2 V. It is concluded that the dominant injection mechanism in our devices is electron

tunneling from N+ drain into the nitride. We will see that there is no experimental evidence from measured $I_D(V_{FG})$ (Fig. 4-21) and $I_D(V_D)$ (Fig. 4-22) curves for BJT-induced carrier injection near the source. Carrier trapping and threshold variation occur locally near the biased terminal (*i.e.*, drain or source or both).

These results differ from those obtained with carrier injection by high back-gate biasing, where the trapped charges were *uniformly* distributed under the channel region in the nitride layer. The charges trapped from source to drain could modify the back-surface potential by a constant amount in the whole device area. When drain-bias injection method is used, the injected charges are only located near the drain terminal. Hence, the surface potential near the source is barely disturbed.

If the source and drain terminals are interchanged during reading, double-bit nonvolatile operation can be carried out. The terms "*direct*" or "*reverse*" are used when a positive read biasing (50 mV) is applied to *drain* or *source* contacts respectively. Note that the nonvolatile charge is injected at the same terminal whatever read (reverse or direct) is performed. When positive (or negative) charges are injected in the nitride (with V_D = +2.5 V or V_D = -2.5 V) and the measurement is performed in direct mode (Fig. 4-21a), the post-stress drain current *variation* is larger than in reverse mode (Fig. 4-21b). This is because the injected charges are located near the drain terminal. In direct mode, the positive charges tend to prevent the channel pinch-off. Hence, the current saturation is delayed and the current continues to increase with V_D. In reverse mode, the charges are located near the virtual source and their impact on the pinch-off region is much lower. Consequently, in direct mode, the drain current is higher than in reverse mode (after 15 sec stress with V_D = +2.5 V). The opposite effect is observed after 15 sec stress at V_D = -2.5 V. The negative charges trapped near the drain accentuate the channel pinch-off and current saturation occurs at lower V_D. The current is clearly reduced in direct mode and lower than in reverse mode. This is the evidence of the non-uniform trapped charge distribution induced by drain biasing.

The advantage of this charge injection mechanism is two-fold: (i) double-bit operation is feasible according to the four configurations of the injected charges by changing reading terminal and the polarities of the stress bias and (ii) analog, logic and memory operations can be carried out within the same ONO FinFlash cell.

The localized charge injection is also obtained in Fig. 4-22, where $I_D(V_D)$ curves were measured at V_{FG} = 0 V and V_{BG} = 0 V. By applying stress with V_D = +3 V, the previous information is erased and '1'-state is programmed. The positive injected charges can activate

the back-channel. The '0'-state is programmed with a stress at V_D = -3 V: the negative charges tend to suppress the current. The variation of the drain current by changing the drain bias polarity is large enough for flash memory application. Comparable amounts of trapped charge are obtained with moderate drain bias or with high back-gate bias.

The comparison of $I_D(V_D)$ curves in direct mode and reverse modes indicates that the distribution of trapped charges is not symmetrical along the channel direction. Like for Fig. 4-21, the drain current difference between V_D = +3 V and V_D = -3 V stress is larger in direct mode than in reverse mode due to the enlarged role of the injected charges located near the drain terminal on the channel pinch-off.

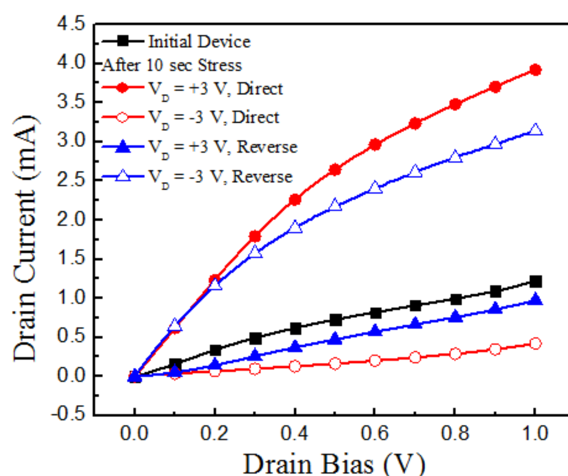

Fig. 4-22: Evidence of the localized charge injection. Drain current versus drain bias measured after 10 sec stress with $V_D = \pm 3$V. After measurement in direct mode, the channel direction was changed in reverse mode. W_F = 90 nm, L_G = 80 nm, N_F = 100m V_D = 50 mV, V_{FG}= 0 V, V_{BG} = 0 V.

Fig. 4-23 shows how the memory effect induced by drain biasing depends on geometrical parameters. Like in the case of programming with high back-gate bias, the memory effect increases for shorter and wider devices. This phenomenon is again related to 3D coupling effects in triple-gate FinFETs [80, 211]. The increase of the memory effect observed in shorter device is promising for the device scaling. Since the V_D-based programming results in a localized charge near the drain, the memory effect will remain efficient even for very short fin with reasonable width (> 10 ~ 15 nm).

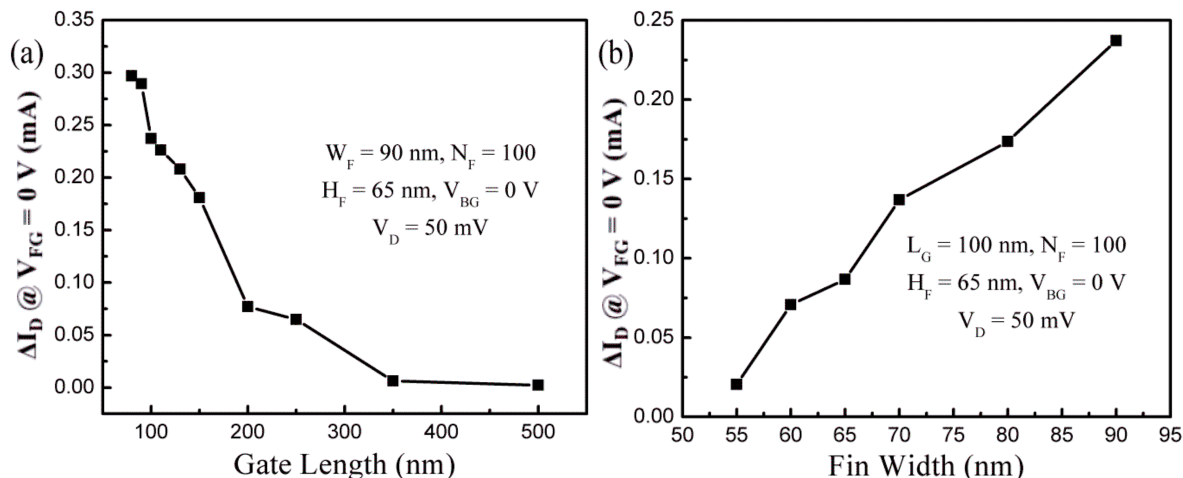

Fig. 4-23: Impact of device geometry on the sensing margin. Sensing margin, defined as in Fig. 4-16, versus (a) gate length and (b) fin width. After 10 sec stress with $V_D = \pm3$ V, we extracted the sensing margin defined as in Fig. 4-16b.

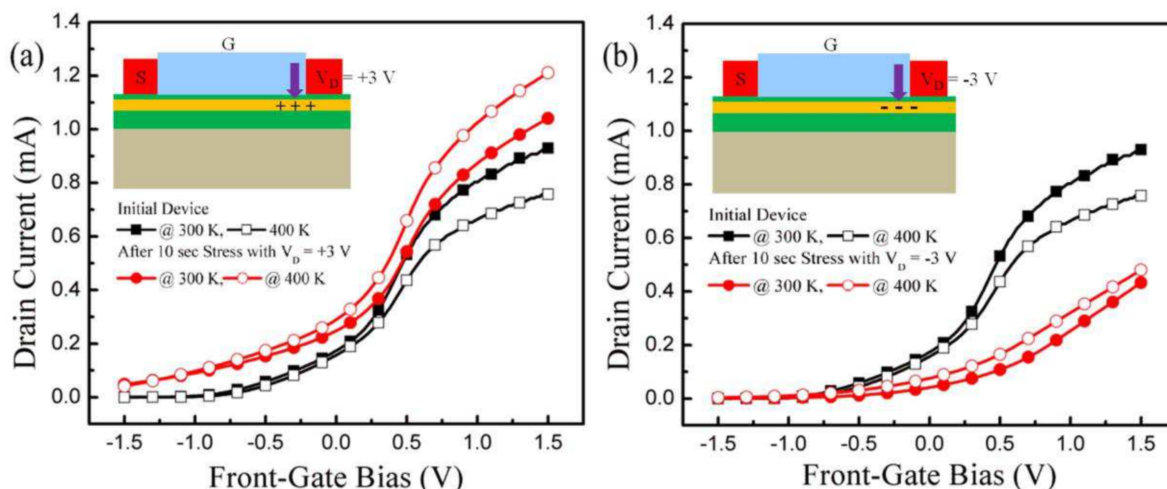

Fig. 4-24: Effect of carrier injection by drain biasing at various temperatures. Drain current versus front-gate bias measured after 10 sec stress with (a) V_D = +3 V and (b) V_D = -3 V. Insets in Fig. 4-24a and b shows the polarity of the injected charges according to the applied drain bias. L_G = 80 nm, W_F = 90 nm, V_D = 50 mV, N_F = 100, V_{BG} = 0 V.

Fig. 4-24 shows the effect of trapped charges achieved with drain biasing for different temperatures. During 10 seconds stress at V_D = +3 V (Fig. 4-24a), positive charges are injected into the Si_3N_4 buried layer, leading to enhanced drain current. The difference between pre-stress and post-stress currents is accentuated at high temperature for two reasons: (i) the pre-stress current is lower (mobility effect) whereas (ii) the carrier trapping efficiency is improved as the temperature increases [215]. Therefore, more positive charges are captured near the drain terminal in the nitride layer, being able to increase the post-stress current. By contrast, when negative charges are injected into the nitride (10 sec stress with V_D = -3 V, Fig. 4-24b), the body potential decreases and the drain current drops. The comparison

of injection efficiency between electrons and holes is complex. Not only are the trapping cross-sections different but also the drain-to-body diode is oppositely biased. For $V_D < 0$ V, the diode is forward biased and the potential drop extends into the body. We expect the electron trapping to be less localized than for holes.

Fig. 4-25 shows the dependence of the sensing margin ΔI_D on the gate length and temperature. For shorter devices, the drain current variation is amplified due to the 3D coupling effects [80, 211] like for back-gate induced trapping (Fig. 4-16 and Fig. 4-19). Note that the current variation is large (ΔI_D = 0.2 mA) in short FinFET (80 nm), if the fin width is reasonable (W_{eff} ~ 30 nm). The temperature rise has a modest effect on ΔI_D because of the trade-off between decreased mobility and improved injection/trapping efficiency.

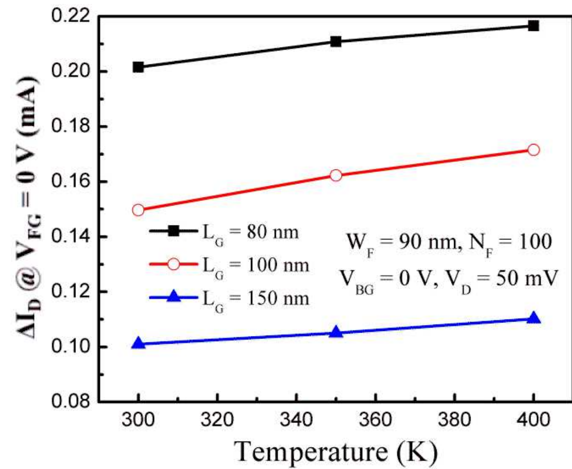

Fig. 4-25: Effect of temperature on the sensing margin induced by drain stressing. Sensing margin, defined as in Fig. 4-16, versus temperature for different gate lengths.

As we see in Fig. 4-24 and Fig. 4-25, drain current variation depends on temperature. The enlargement of ΔV_{THB} and ΔI_D at higher temperature is illustrated in Fig. 4-25 and explained as follows. When the electrons are removed from the nitride, the variation of the threshold voltage with temperature is usually associated with the increase of the Poole-Frenkel hoping in the nitride and thermal excitation [215]. If temperature increases, the thermal excitation is enhanced and more trapped electrons can move towards the nitride conduction band. The tunneling rate is weakly dependent of temperature but the increase of the free electron amount in the nitride and of the Poole-Frenkel conduction produces more tunneling of electrons from the nitride into the silicon body. When the electrons are injected into the nitride, the threshold voltage variation depends mainly on the efficiency of the electron tunneling from the silicon body into the nitride (the electrons are available

instantaneously from the inverted silicon interface).

In Fig. 4-26, the effect of the injected charges and temperature on the $I_D(V_D)$ curve is investigated. As for room temperature (Fig. 4-22), double-bit nonvolatile operation was demonstrated at 400 K (Fig. 4-26a) by changing the reading terminal and the polarity of the injected charges. A proper 'high' - 'low' state sensing margin is achieved. The sensing margin is defined here as the difference of the current level between direct and reverse modes at V_D = 1 V ($V_{FG} = V_{BG}$ = 0V) after positive or negative charge injection.

Fig. 4-26b shows the 'high' and 'low' state sensing margin as a function of the temperature up to 400 K for different channel lengths. ΔI_D for both hole injection ('high' state) and electron injection ('low' state) increases as the channel length shrinks even at high temperature.

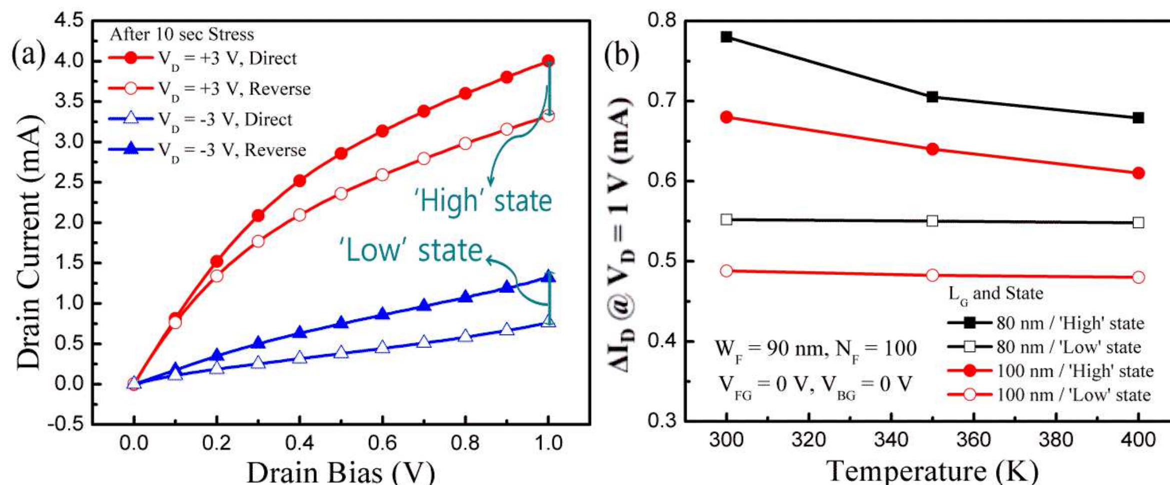

Fig. 4-26: Effect of temperature on $I_D(V_D)$ curves. (a) Drain current versus drain bias measured in direct and reverse mode after 10 sec stress with $V_D = \pm3$ V (T = 400 K). L_G = 80 nm, W_F = 90 nm, N_F = 100, V_{BG} = 0 V, V_{FG} = 0 V, T = 400 K. (b) Drain current difference between the direct and reverse modes as a function of temperature for different gate lengths. ΔI_D was measured at V_D = 1 V after hole trapping ('high' state) or electron trapping ('low' state).

In Fig. 4-27, we considered a more complex case of carrier injection at both terminals. A 10 seconds stress was applied to the source terminal, followed by 10 seconds stress on the drain. In this double-stress mode, the current variation is larger than for single-stress: the current increases more for positive charge and decreases more for negative charge trapping. This double-side (at source and drain) injection is more efficient than back-gate bias programming. An asymmetry in reverse and direct curves subsists. It is explained by the redistribution of the charge, initially localized near the source, during the subsequent drain-side stress. The injected charge concentration located near the source could be modulated by

the drain-side stress. Therefore, the impact of charges near source on the memory effect might be reduced.

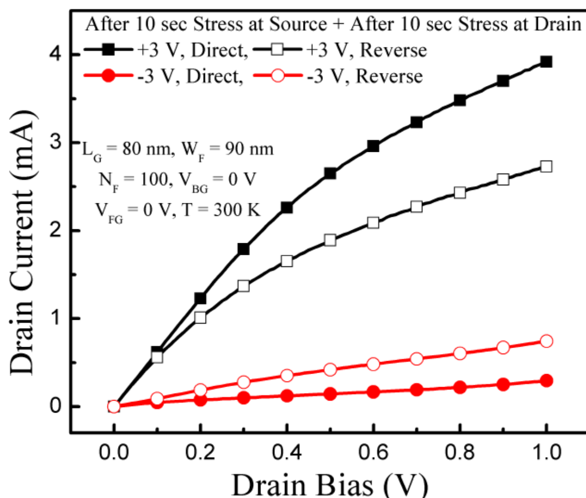

Fig. 4-27: $I_D(V_D)$ curves measured in direct and reverse mode after two-step stress: 10 sec stress with $V_S = \pm 3$ V followed by 10 sec stress with $V_D = \pm 3$ V (T=300 K).

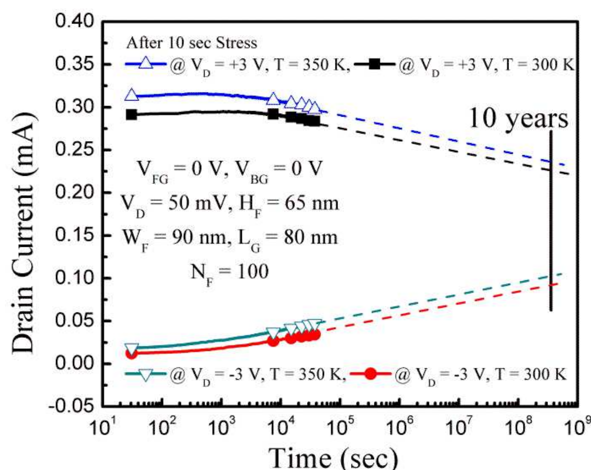

Fig. 4-28: Retention characteristics related to the release of trapped charges from the nitride layer. Drain current versus time, measured at T = 300 K and T = 350 K after charge trapping with $V_D = \pm 3$ V.

Fig. 4-28 shows the retention time achieved by using drain bias programming. The return towards equilibrium occurs as the injected charges are released from the nitride. In the same way as for programming with high back-gate biasing, the charges injected by applying a moderate drain bias are conserved sufficiently long and the difference between '1'- and '0'-states is suitable for flash memory application. The retention time is longer in the case of drain bias programming due to the strong effect of the injected charges located near the drain on the channel pinch-off. This result denotes the efficiency of the V_D programming method. Notice that drain bias used during the reading operation is sufficiently low and does not

deteriorate the retention capability of the cell.

4.4.3. Drain current hysteresis in dynamic mode

We have discussed above the memory effect resulting from permanent charge trapping. We now introduce another memory effect: the drain current hysteresis due to the 'dynamic' trapping of charges.

By scanning back-and-forth the back-gate bias from positive to negative value, a strong drain current hysteresis occurs (Fig. 4-29). This hysteresis, in other words the memory window, is due to the dynamic charge trapping/detrapping into/from the nitride buried insulator during the scanning of the back-gate voltage. The memory window is defined as the maximum shift of back-channel threshold voltage ΔV_{THB} (see horizontal arrow in Fig. 4-29). Starting at V_{BG} = +50 V and decreasing the back-gate bias, the trapped electrons are gradually removed from the nitride buried insulator and the back-channel threshold voltage decreases. This is why when coming back to positive V_{BG} values, a hysteresis and higher drain current are achieved. A similar hysteresis is obtained in the reciprocal case: starting at V_{BG} = -50 V and increasing the back-gate bias to less negative values, electrons are injected in the Si_3N_4 buried insulator and the back-channel threshold voltage increases.

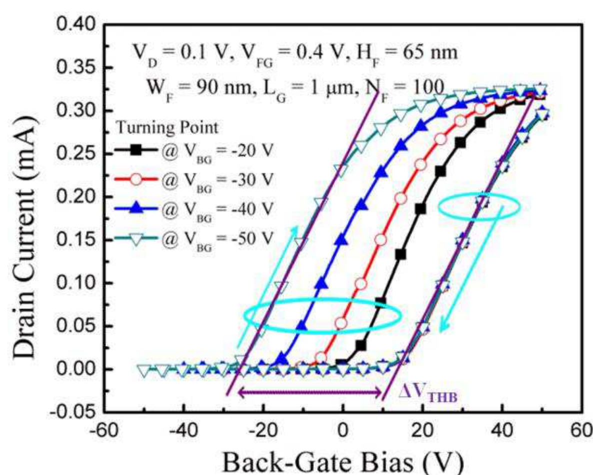

Fig. 4-29: Drain current hysteresis versus back-gate bias. The measurement started at V_{BG} = +50 V and the turning voltage was varied.

The memory window depends on the direction and amplitude of the back-gate scan. In Fig. 4-29, we measured the drain current as a function of the back-gate bias for different turning points. The measurement started at V_{BG} = +50 V. The initial stress time was 30 s.

When the back-gate bias turning point becomes more negative, the memory window is enlarged because of the amount of detrapped electrons increases.

When the measurement starts at V_{BG} = -50 V, we obtained a symmetrical result shown in Fig. 4-30. Positive charges are injected in the nitride layer during 30 seconds stress with V_{BG} = -50 V. While increasing back-gate bias, positive charges are removed from the Si_3N_4 layer, hence the back-channel threshold voltage increases. During the subsequent decreasing V_{BG} scan, the current is therefore lower. The memory window is larger for clockwise scan (Fig. 4-30b), and is also affected by the measurement starting point. The reason is the difference in charge injection efficiency of holes and electrons. Nevertheless, the overall tendency is qualitatively the same.

The memory window also depends on the magnitude of front-gate bias as shown in Fig. 4-30. For higher V_{FG}, the hysteresis and memory window decrease. This result is more prominent in narrow fins and results from the competition between the vertical coupling component, induced by trapped charges in the nitride layer, and the lateral coupling component between the two side gates [80, 211]. The lateral gates tend to pin the back-surface potential and remove the effect of trapped charges. For higher front-gate bias and narrow fins, the lateral gates prevail and the memory window (*i.e.*, ΔV_{THB}) decreases.

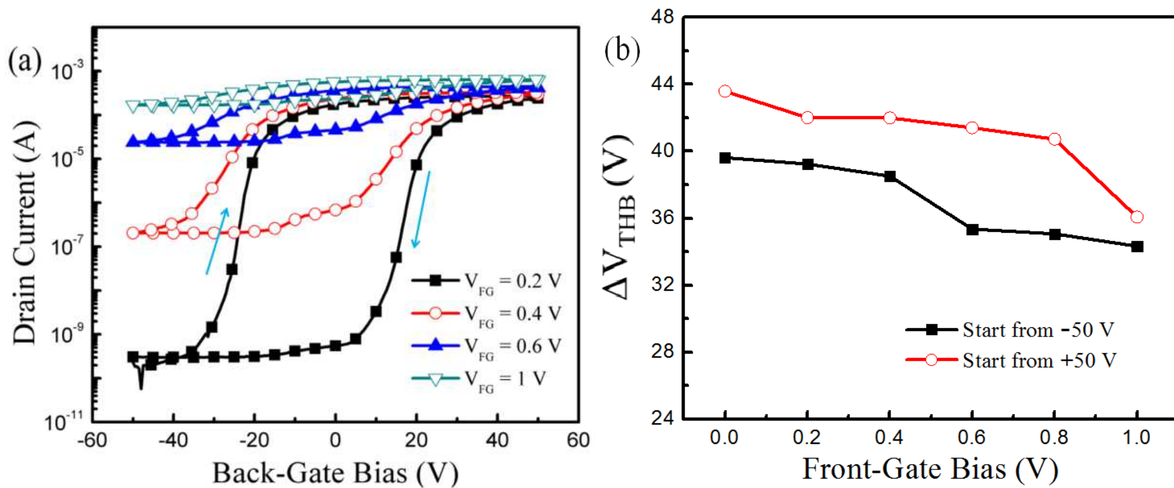

Fig. 4-30: Dependence of memory window on front-gate bias. (a) Drain current hysteresis versus back-gate and front-gate bias. (b) Back-channel threshold voltage variation (memory window) versus front-gate voltage and measurement starting bias (30 sec stress time). V_D = 0.1 V, W_F = 90 nm, L_G = 1 µm, N_F = 100.

Fig. 4-31 shows the memory window dependence on fin size. As already observed and explained in Fig. 4-16 and Fig. 4-17, the memory window increases for shorter and wider fin devices.

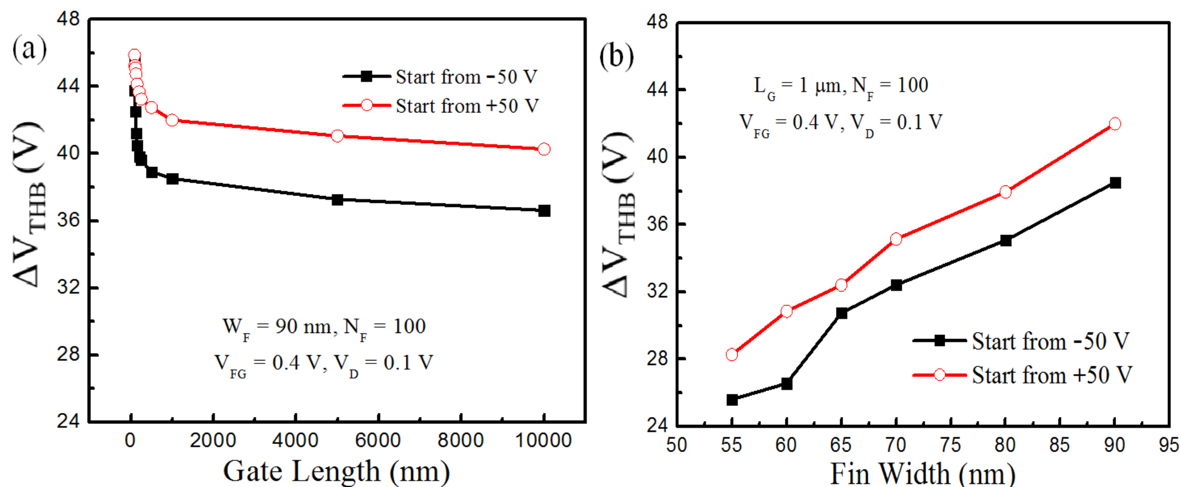

Fig. 4-31: Impact of device geometry on the memory window, defined as the variation of the back-channel threshold voltage. Memory window as a function of (a) gate length, (b) fin width and measurement starting bias.

Fig. 4-32a shows the drain current hysteresis measured at various temperatures. For higher temperature, the drain current level in strong inversion is smaller due to the mobility reduction. The variation of back-channel threshold voltage ΔV_{THB} (*i.e.*, the lateral shift of forward and reverse characteristics in Fig. 4-32a) is improved because the carrier trapping efficiency increases at higher temperature [215]. Note that a positive starting point (V_{BG} = +50 V) is illustrated in Fig. 4-32. However, when the starting point becomes negative (V_{BG} = -50 V), the trend is the same.

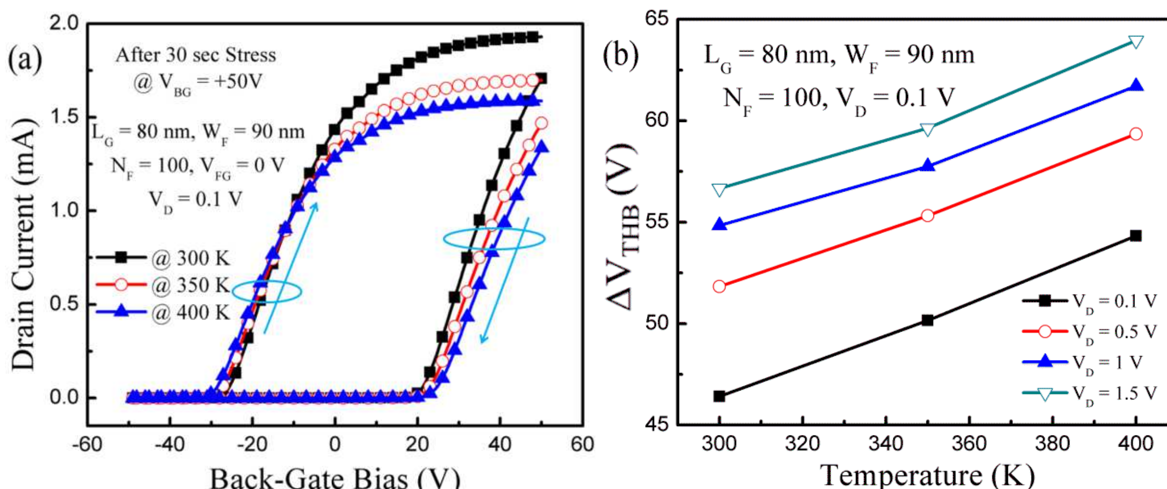

Fig. 4-32: Effect of temperature on the memory window. (a) Drain current hysteresis versus back-gate bias and temperature. (b) Memory window, defined as in Fig. Fig. 4-31, versus temperature for variable drain bias.

In Fig. 4-32b, the drain bias effect is highlighted: for higher V_D, ΔV_{THB} increases.

Again, this is due to the longitudinal coupling component, induced by the drain biasing, which reduces the capability of the lateral gates to control the back-surface potential and, therefore, enhances the influence of the trapped charge. The effect of longitudinal coupling component increases at higher drain bias and, consequently, ΔV_{THB} is enlarged.

4.5. Conclusions

The operation and performance of advanced FinFETs with buried ONO storage layer have been investigated for flash memory application. The Si_3N_4 buried layer can trap charges, by either Fowler-Nordheim tunneling using back-gate biasing or localized carrier injection induced by drain biasing, and efficiently hold them for a long time even at high temperature. The carrier injection efficiency is improved at high temperature due to Poole-Frenkel emission. A suitable memory effect results from the coupling effect between injected charges and back- and front-channels. From the experimental results, we found that the memory effect depends on the bias condition and dimensional parameters. We highlighted that the reduction of the channel length enhances charge trapping thanks to the DIVSB. Carrier injection via drain biasing enables charge storage localization near the drain or source or both. This phenomenon allows different configurations by choosing the charge injection region or sensing terminal and enables multi-bit nonvolatile memory operation. By the separation of the programming interface from the sensing interface, ONO FinFET provides improved reliability as the cell scales down.

Chapter 5:

FinFETs with ONO BOX for multi-bit unified memory

After having demonstrated the non-volatile memory operation of ONO FinFETs, we now explore their capability as volatile memory cell. The ultimate objective of this work is to study the feasibility of an unified memory where the volatile and non-volatile modes can be achived separately or combined in a single transistor.

5.1 Introduction

Co-integration of various functionalities in a single chip is suitable for advanced portable electronic devices and embedded systems. From this perspective, nonvolatile and volatile memory devices need to be integrated in the same block. But, these two different memory architectures bring additional process and high cost. Several solutions have been proposed to merge the two different functions in a single cell [216-218].

Most of these structures use the same interface/gate for the nonvolatile and volatile operations. Due to the cycling stress caused by the volatile memory programming, a deterioration of the nonvolatile charge retention time occurs as the gate oxide is damaged. This phenomenon is amplified when the device scales down because the tunneling oxide is thinner in order to maintain good control of the channel. Our FinFETs fabricated on ONO buried insulator (Chapter 4) are attractive due to (i) excellent scaling capability and (ii) separation of the programming and reading interfaces.

In this chapter, the ONO FinFETs are assessed as *volatile* capacitor-less single-transistor DRAM (1T-DRAM) [219-221] programmed by impact ionization. We highlight that nonvolatile charges stored in the nitride can remarkably modify the 1T-DRAM logic states without being disturbed by the volatile operation. Therefore, the two different memory operations can be performed without disturbing each other to achieve the *unified memory* concept (URAM) [216, 218]. Our experimental results intend to demonstrate a preliminary 'proof-of-concept' of a multi-bit volatile memory. The "multi" 1T-DRAM current levels can be achieved by performing nonvolatile programming/erasing before volatile operation. The impact of the location of the trapped nonvolatile charge on the 1T-DRAM sensing margin is also investigated. Especially, this study is performed by inter-changing the source and drain terminals during memory programming and/or reading.

5.2. Volatile Memory

5.2.1. Conventional volatile memories

Volatile memories are not able to keep information when the power supply is turned off. Their features are very fast writing and reading operations. The two main volatile memory families available on the market are the Static Random Access Memory (SRAM) and the Dynamic Random Access Memory (DRAM). In this introduction, special attention will be given to DRAM and 1T-DRAM.

(a) Static random access memory (SRAM)

SRAM cell does not need to be refreshed to renew the stored information and retains information when the memory is powered. As we can see in Fig. 5-1, a storage cell is made up with two cross-coupled inverters formed by four transistors (M1, M2, M3 and M4). During read and write operations, two additional access transistors (M5 and M6) allow to control the access of the storage cell.

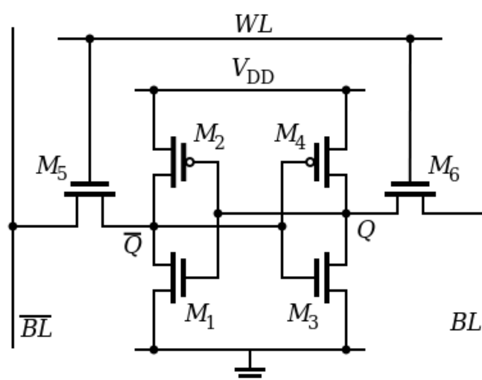

Fig. 5-1: Schematic representation of conventional 6T-SRAM.

A SRAM cell has three different states (standby, write and read). During standby (*i.e.*, the circuit is in idle mode), the word line is offset ($WL = 0$). Thus, the access transistors decouple the storage cell from the bit lines. The cross-coupled inverters feedback each other and hold the stored information. Writing operation is performed by applying the value to be written to the bit line. For example, for the '1'-state writing, '1' should be applied to the bit line (*i.e.*, $BL = 1$ and $\overline{BL} = 0$). The data is then stored by the WL (WL=1). Conversely, the '0'-state writing is carried out by applying $BL = 0$ and $\overline{BL} = 1$. The stored information

is read at Q. For reading operation, '1' is applied at BL, $\overline{BL}$ and WL. Assume that the stored information is '1'. '1'-state at Q is transferred to the bit line and $\overline{Q}$ is in '0'-state by discharging through M1. On the other hand, when the stored information is '0' at Q, '0'-state is transferred to the bit line (M3 is turned on and Q keeps '0'-state) and $\overline{Q}$ is in '1'-state. Conventional 6T-SRAM cells require relatively large real-estate on the silicon chip leading to low integration density, while they provide very high access speed [222].

(b) Dynamic random access memory (DRAM)

In conventional 1T-1C DRAM (Fig. 5-2), the information is stored in a separated capacitor. The two values, called '1'- and '0'-state, are obtained by charging or discharging the capacitor. The stored charges should be refreshed periodically to replenish the stored data due to the leakage through the selection transistor. The reading of the DRAM is destructive. Indeed, the word line is onset and the stored information is transferred to the bit line through the transistor discharges the capacitance.

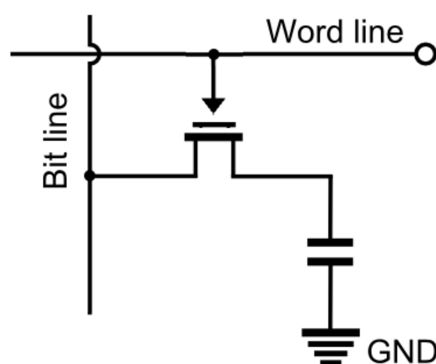

Fig. 5-2: Schematic representation of conventional 1T-1C DRAM.

Conventional 1T-1C DRAM exhibits much higher integration density and better reliability than 6T-SRAM. However, in DRAM, access speed is lower because it requires time to charge the capacitor. Moreover, capacitance must be above a certain level to distinguish the two different memory states while the transistor size continuously decreases. Therefore, the miniaturization of the capacitor is becoming a critical issue for further device scaling and integration density. Several solutions are being utilized such as 3D trench or stacked capacitors using high-k material [223, 225]. However, they are still subject to miniaturization problems, performance degradation and cost rising.

5.2.2. Capacitorless 1T-DRAM

Several years ago, capacitorless 1T-DRAMs were proposed as an alternative to conventional 1T-1C DRAM [220, 221, 226, 227]. These architectures use the floating body of SOI or SOI-like single transistors as medium to store the information. The isolated body provides an ideal storage environment to achieve competitive performances [219-221] (Fig. 5-3). In 1T-DRAM, a temporary generation of majority carriers stored in the body increases the body potential and drain current which corresponds to '1'-state. By contrast, for '0'-state, a lower current level reflects the purge of the majority carriers out from the body. As we can see in Fig. 5-3, the variation of the amount of majority carriers in the body is easily detected by measuring the drain current. By adopting the 1T-DRAM concept, one can save silicon area thanks to the isolated body used instead of the storage capacitor. Higher integration density, reduced process steps and lower cost are expected compared with conventional 1T-1C DRAM.

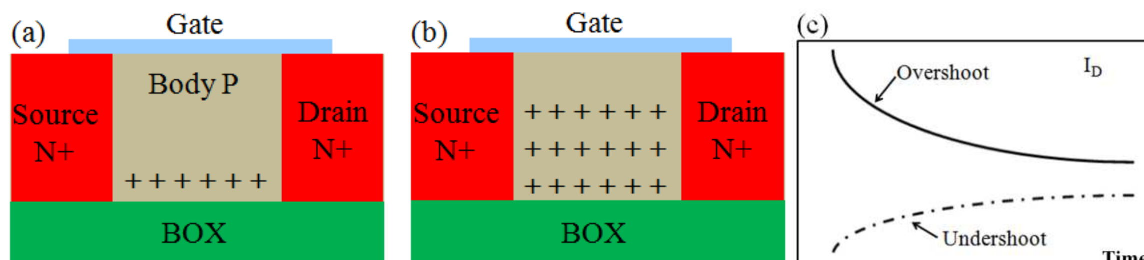

Fig. 5-3: Capacitorless 1T-DRAM concept. Schematic cross-section of a partially depleted (PD) SOI nMOSFET used as a 1T-DRAM. (a) Lack ('0'-state) and (b) excess ('1'-state) of majority carriers in the body. (c) Undershoot ('0'-state) and overshoot ('1'-state) of drain current resulting from the variation of majority carrier concentration with time.

(a) '1'-State Programming

During the '1'-state programming, excess holes (majority carriers) are stored in the body, leading to a dynamic threshold voltage reduction ($V_{TH} \rightarrow V_{TH} - \Delta V_{TH1}$) and an increase in the drain current (I_1): The threshold voltage shift ΔV_{TH1} comes from the body potential variation due to the stored holes. Several programming methods can be performed to inject the majority carriers into the body. They will be introduced in the next section as well as their advantages and drawbacks.

(i) *Impact ionization* is a frequently used method for the '1'-state programming [226-

231]. During the programming operation, the drain bias V_D is changed from a low value (~ mV) to a relatively high one (~ V) while the front-channel is in inversion regime ($V_{FG} > V_{THF}$), same as in holding and reading operation. Therefore, near the drain contact, electron-hole pairs are generated at the pinch-off region by impact ionization. The generated holes can be stored in the body as the body/drain junction is reverse biased. After programming, the floating body potential is higher than in steady-state (Fig. 5-4a). For the '1'-state reading, V_D is pushed back to a lower level (~ mV). The resulting threshold voltage is 'low' and the current level is 'high' due to excess holes remaining in the body. The body potential returns gradually (~ ms) downward to steady-state because the stored holes are slowly evacuated through the body/drain (or source) junctions. This causes a drain current overshoot and back to equilibrium with time.

Impact ionization method provides fast '1'-state programming and relatively large sensing margin. However, impact ionization induces hot-electron injection into the gate oxide, causing degradation of the oxide quality and retention time. Due to the charge trapped in the oxide, an unintended threshold voltage variation can also occur.

(ii) *Bipolar Junction Transistor (BJT)* effect in the floating body of SOI MOSFETs can be employed for the '1'-state programming. In this method, the source (N+), body (P) and (N+) correspond to the emitter (or collector), base and collector (or emitter) of the BJT. A hole current should be generated in the body (base) to switch on the BJT effect. Due to the floating base, the body potential increases by programming, providing a threshold voltage lowering and current rise. The BJT can be turned on with different bias schemes:

- ✓ The first introduced BJT method is generated by applying a high negative V_D pulse embedded into a negative front-gate V_{FG} pulse (Fig. 5-4b) [226, 227]. At the initial programming stage, the front interface becomes accumulated by using a negative V_{FG}. Then, V_D is driven to a high negative value. As a result, the body/source and body/drain junctions are reverse and forward biased respectively. If V_D is sufficiently large, impact ionization is turned on at source side. For better hole storage, the drain pulse returns to the reading value (~ 50-100 mV) while the gate bias is kept negative. In this method, the power consumption is reduced thanks to the low current flowing between the drain and source during programming at $V_{BG} < 0$ V.
- ✓ BJT effect can also be activated in a different way [214, 232]. A V_{FG} pulse is

embedded into a high positive drain V_D pulse (Fig. 5-4c). Electron-hole pairs are generated by impact ionization at the reverse biased body/drain junction if a sufficiently large V_D pulse is applied (close to the breakdown voltage of the parasitic BJT). However, BJT effect is not fully triggered if $V_{FG} < V_{FBF}$. In order to push the potential up to a value sufficient to turn on the bipolar current, the front gate is switched to a higher value ($V_{FG} > V_{FBF}$). Hence, the body potential is increased due to the dynamic gate coupling and the source/body junction becomes forward biased. As a result, impact ionization and hole base current are sharply increased. Therefore, electrons are moved into the body (base) from the source (emitter) and collected by the drain (collector). At the end of the programming sequence, the gate pulse V_{FG} is pushed back to negative value (prior to drain pulse V_D return to reading stage). The body potential maintains a high level due to the large base current and a sufficient amount of holes are stored in the body. During reading, V_{FG} remains at a negative value ($V_{FG} < V_{FBF}$) to slow down the evacuation of the stored holes from the body while a high pulse is applied at drain. The BJT is activated and a high current is obtained. Note that the high V_D pulse required to activate the BJT current allows to auto refresh the '1'-state during reading.

The BJT programming methods allow fast read and write operations (~ 2 ns) [214]. Moreover, holes can also be generated by band-to-band tunneling at the gate-to-drain (or source) overlap region as the net potential drop reaches up to 4 V at the gate edges [232]. Therefore, the programming speed and stabilization of the '1'-state current level are improved but retention time and device reliability can be degraded.

(iii) The hole generation by *Band-to-Band Tunneling (BTBT)* at the gate-to-drain overlap region can be applied for the '1'-state programming (inset of Fig. 5-4d) [233, 234]. In order to generate holes, the local electric field and the band-bending should be sufficiently large to make holes tunneling from conduction band into the valence band at the N^+-drain/oxide interface. A relatively high negative front-gate ($V_{FG} << V_{FBf}$) and positive drain biases are applied (Fig. 5-4d). The body potential decreases by dynamic gate coupling and enters in a deep depletion regime. As a result, the holes are stored and efficiently kept in the body. Indeed, as the body potential is more negative than at equilibrium (*i.e.*, accumulated front-interface), the barriers at the source(drain)-body junction are higher and the resulting body potential well deeper. Note that the deep depletion regime can be achieved because the front-interface

accumulation is a relatively long process.

During reading, V_{FG} is increased above V_{THf} and the stored holes are moved from the front-interface to the bottom interface (negatively biased in FD SOI). Compared with other techniques, the total signal swing ($|V_{FG}| + |V_D|$) should be increased by about 20% in order to obtain competitive programming speed [234]. However, the programming current taking place with the BTBT method is much lower than the one imposed by impact ionization. Consequently, the reliability and power consumption of the memory cell are significantly improved.

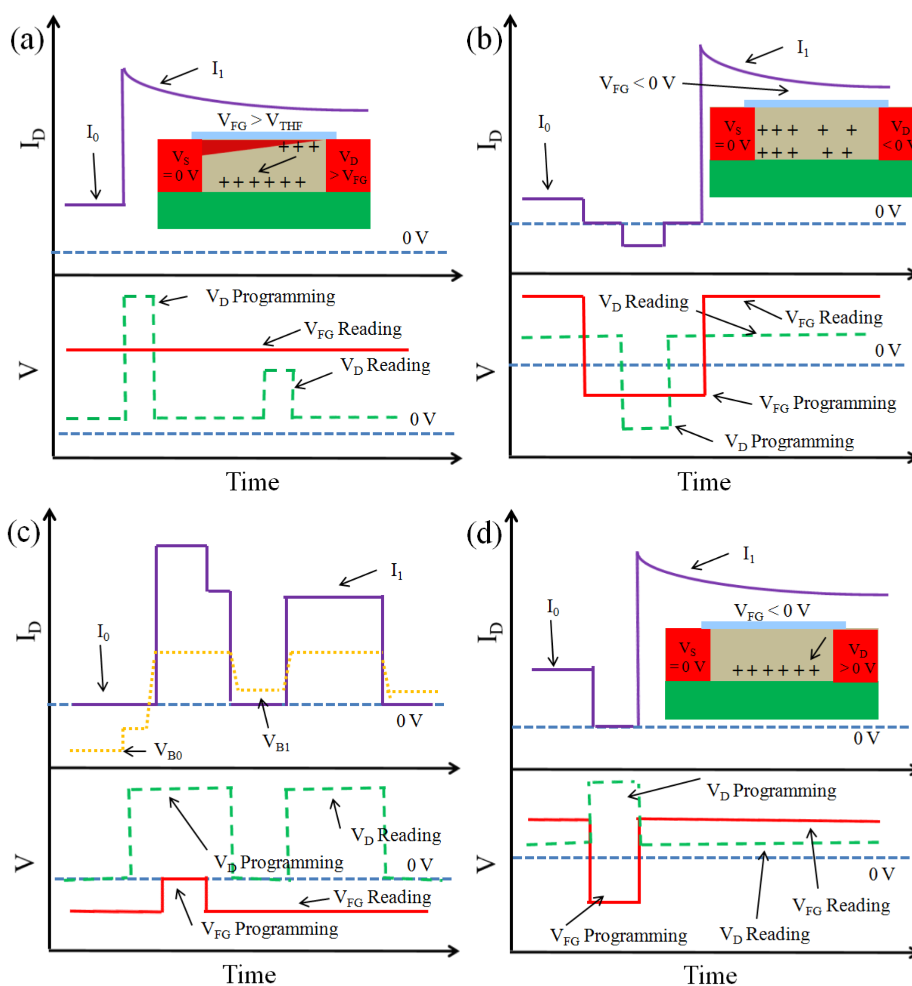

Fig. 5-4: External pulse sequence and schematics for ‘1’-state programming and reading by (a) impact ionization, (b) 1st BJT method, (c) 2nd BJT method and (d) band-to-band tunneling (BTB) method. Gate pulse V_{FG}, drain pulse V_D, body potential V_B and drain current I_D as a function of time.

(b) 0’-State Programming

The ‘0’-state programming (erasing operation) consists in removing holes from the body. The temporary lack of holes leads to a body potential drop and consequently the

threshold voltage is increased ($V_{TH} \rightarrow V_{TH} + \Delta V_{TH0}$) reducing the drain current. The two methods currently used for the '0'-state programming are introduced hereafter.

(i) *Forward biased junction* using a negative drain bias is applied to evacuate the stored holes (Fig. 5-5a) [226, 227, 229]. When the drain terminal voltage is negative, the body/source junction is reversed biased. Hence, the hole current flowing from the body to drain is much larger than the one originating from the source. This unbalanced current induces a dynamic lack of holes. On the other hand, as the body/drain junction is forward and negatively biased the whole body potential becomes negative. For the subsequent reading (or holding), V_D returns to a small positive value and the body/drain junction is again reversed biased. Thanks to the lack of holes, the body potential can remain temporarily in a non equilibrium state (*i.e.*, negative). The threshold voltage is increased and a low current level is obtained. In this technique, body potential variation is not very effective and the '0'-state current level is relatively high (despite fast erasing is achieved) due to the instant time response of the forward body/drain junction to the bias switch.

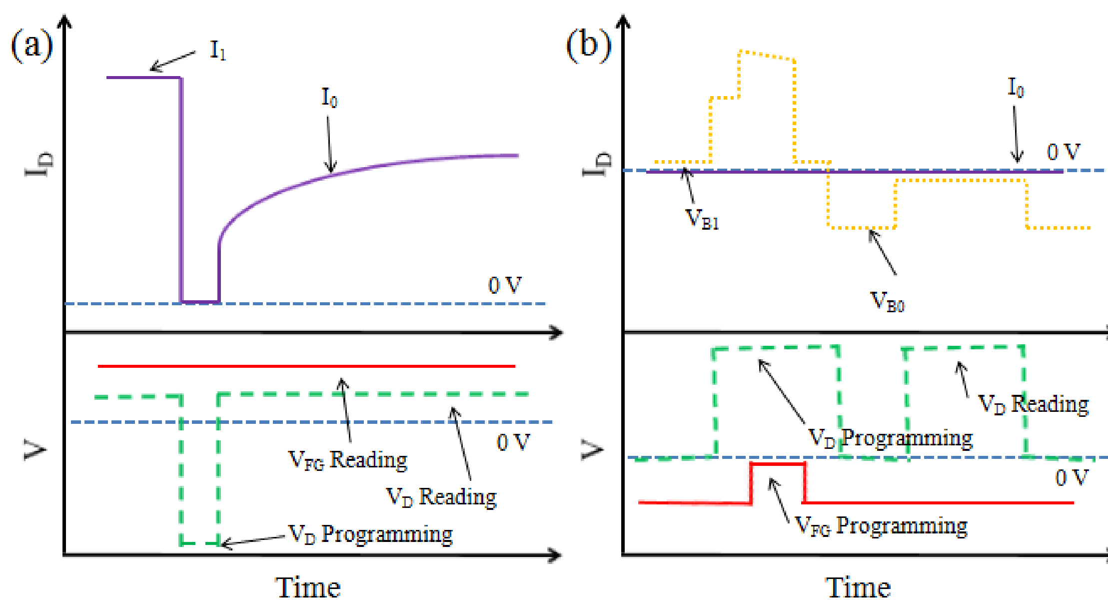

Fig. 5-5: External pulse sequence for '0'-state programming and reading by (a) forward-biased junction and (b) capacitive coupling method.

(ii) The *capacitive coupling* allows to remove the holes from the body by taking advantage of the deep depletion mechanism. At the first stage, the front-gate is pulsed from accumulation ($V_{FG} < V_{FBF}$) into inversion regime ($V_{FG} \sim V_{THF}$). The accumulated holes are instantaneously evacuated through the body/source(drain)

junctions. Next, the front-gate voltage is pulled down again to a negative value ($V_{FG} < V_{FBF}$). As the holes are not generated instantly, the accumulation layer is not built readily and the body potential becomes negative by dynamic gate capacitive coupling. The subsequent reading is performed with a negative front-gate voltage (usually slightly higher (less negative) than the programming voltage). Since the body potential is negative, the back threshold voltage is virtually increased (Fig. 5-5b) [214, 232]. Notice in Fig. 5-5b, during the '0'-state programming, the drain V_D pulse is relatively high for compatibility with the 2nd BJT method. It may cause the activation of BJT effect and the body charging. To avoid this, a small positive source voltage is applied.

(c) Scaling issue

The retention time and sensing margin $|I_1\text{-}I_0|$ or ΔV_{TH} are the critical issues for the 1T-DRAM down scaling. As the channel length decreases, the body volume where the holes can be stored is reduced, but the longitudinal electric field between source and drain is enhanced. Therefore, when impact ionization method is employed, '1'-state programming voltage and/or time can be reduced. However, the '0'-state retention time will be deteriorated due to parasitic hole generation. Moreover, short-channel effects (SCEs) also diminish the 1T-DRAM device performance. The drain-induced barrier lowering DIBL is another weakness, degrading the '1'-state programming. In shorter device, the body/source barrier is lowered. As a result, especially for the impact ionization method, the generated holes easily move through the source and the storage efficiency of state '0' is deteriorated. Note that, in BTBT technique, the DIBL is less significant because the body potential is negative during programming.

In PD SOI devices, the body doping increase can be used to improve the sensing margin [229, 230] by suppressing the SCEs as the effective potential barrier at the source/body junction is higher. Therefore, the hole leakage current to the source is reduced and the hole storage efficiency is enhanced. However, if the channel doping is too high, the junction leakage current I_{LEAK} is increased during reading and deteriorates the retention time. Also, a high body doping causes random dopant fluctuation (RDF) effect, leading to fluctuations in read current and random change in ΔV_{TH} [229].

In PD device, the threshold voltage variation ΔV_{TH} can be estimated by ΔV_B x (C_D/C_{OX}) [229], where ΔV_B corresponds to the body potential difference induced by the

stored hole. The depletion layer capacitance C_D and hence ΔV_{TH} can be increased by reducing depletion layer thickness. In this perspective, FD SOI MOSFET with accumulated back-channel induced by a proper negative back-gate bias V_{BG} is a more reasonable approach: the depletion layer thickness is limited by the small silicon film thickness.

In FD SOI MOSFET, SCEs are usually controlled by reducing the silicon film thickness. Therefore, channel-doping is not necessary preventing the random dopant fluctuation. Moreover, I_{LEAK} is reduced due to the thinner junction area. Thereby, the reliability and retention time can be improved in FD devices. ΔV_{TH} can be further enhanced by field plate engineering [230, 231] and thicker front-gate oxide ($C_{ox} \downarrow \rightarrow \Delta V_{TH} \uparrow$). However, the use of a common back-gate bias V_{BG} causes compatibility problems with peripheral circuits. On the other hand, feasible combination of the different '0'- and '1'-state programming is limited by the use of a common back-gate bias V_{BG}. If the back-gate bias is not sufficiently negative, the holes cannot be stored in the body efficiently. Conversely, when the back-gate bias is too negative, the stored holes cannot completely be removed during the '0'-state programming and the current sensing margin reduces.

For these reasons, double-gate (DG) SOI MOSFETs can be an interesting alternative [214, 228]. In order to take full advantage of the different programming techniques, the individual back-gates should control their own transistor.

In this perspective, different 1T-DRAMs variants using specific architectures or additional process steps were introduced. In the next section, a non exhaustive list of enhanced 1T-DRAM will be presented.

(i) *Toshiba approach*: A 128 Mb memory array with 90 nm technology node was experimentally demonstrated [230, 231]. Channel doping (3×10^{17} cm^{-3}), LDD and p-doped field plate were processed in order to improve the sensing margin and the retention time. For the '1'- and '0'-state programming, the impact ionization (V_{FG} = +1.5 V and V_D = +2.2 V) and forward biased junction method (V_{FG} = -2.3 V and V_D = -1.5 V) were used with a fixed field plate bias (V_{BG} = -2.5 V). Good memory performance was achieved (70 ms retention time, ΔV_{TH} = 420 mV @ 85 °C).

(ii) *Intel approach*: A FD SOI 1T-DRAM cell was fabricated at 45 nm technology node [235]. Programming methods and bias conditions were not presented in detail. However, the disturbance mechanisms were reported. Shockley-Read-Hall (SRH) recombination at the source edge disturbs the '1'-state level by causing hole loss. '0'-state is disturbed by band-to-band tunneling parasitic generation at the drain edge.

Thin undoped thin body (T_{si} = 22 nm) significantly reduces the RDF effects and the junction leakage current. A ΔV_{TH} of 400 mV was observed with a back-gate bias (V_{BG} = -2 V) and thin BOX (T_{BOX} = 10 nm). At the worst disturb condition, 25 ms retention time was achieved at 85 °C (L_G = 55 nm and W_G = 65 nm).

(iii) *Meta-Stable DRAM (MSDRAM) (Fig. 5-6a)*: This memory cell concept is based on meta-stable deep (MSD) hysteresis effect [236, 237]. Very wide memory window and large current ratio ($I_1/I_0 > 10^6$) were measured. The advantages of MSDRAM are the low power consumption and excellent reliability thanks to the BTB tunneling and dynamic gate coupling used for the '1'- and '0'-state programming, respectively. 2D simulations with a 30 nm gate length and thin BOX were performed to investigate the cell scalability. Superior retention time (14 s at I_1/I_0 = 10) was obtained with short programming time (5 ns). In small device (0.35 µm x 0.35 µm), the MSD effect is maintained but the sensing margin needs to be improved [238] by an appropriate fabrication process (recessed gate, thinner junctions, etc). Comparision with 1T-DRAM programmed by impact ionization showed the superiority of the MSDRAM concept [239].

(iv) *Vertical Channel 1T-DRAM (Fig. 5-6b)*: A vertical double-gate 1T-DRAM with two independent gates was proposed to obtain ultimate integration density ($4F^2$) [240, 241]. A gate-all-around MOSFET architecture, called surrounding-gate vertical channel (SGVC) cell, was employed. The SGVC 1T-DRAM was demonstrated on bulk Si substrates with a common source structure, which allows achieving excellent scalability. Impact ionization or BTB tunneling technique can be used for the '1'-state programming. However, the retention time (4 ms at room temperature) needs to be improved even if a suitable sensing margin was obtained (40 µA/µm).

(v) *Body engineered 1T-DRAM*: To enhance the cell performances, various body engineering techniques, innovative architectures and material combinations, were proposed to improve the hole storage efficiency [242-245]. In parallel, source/drain engineering methods were also investigated to increase the retention time [246, 247].

✓ The ARAM is attractive for low power consumption and embedded memory applications [242]. The supercoupling effect [248] occurring when the silicon body is thinner than 10 nm is bypassed. This body engineered architecture enables indeed the coexistence of electrons and holes by physically separating the silicon body with a thin oxide layer extended from source to drain. Two ultra-thin semi-bodies are

formed to isolate the electrons and holes via intermediate oxide (Fig. 5-6c). During '1'-state onset, excess holes generated by impact ionization or band-to-band tunneling are stored in the upper semi-body. These excess holes increase the upper semi-body potential and by electrostatic coupling, reduce the threshold voltage of the bottom semi-body. This concept was experimentally validated via device processing and measurements [243].

- ✓ The single transistor quantum well (QW) 1T-DRAM [244] was demonstrated by inserting a thin SiGe layer with narrow band-gap layer into the Si film (Fig. 5-6d). This layer or quantum well operates as storage well for the excess holes. For '1'-state programming, the holes generated by impact ionization are stored in this quantum well. In order to enhance the storage capability, a negative back-gate bias can be applied. This concept allows to modulate the spatial hole distribution within the device. It was demonstrated that higher V_{TH} shift and retention time are achieved by moving the storage pocket closer to the front gate.
- ✓ A convex channel 1T-DRAM architecture was proposed by simulations (Fig. 5-6e) [245]. The holes generated by BJT programming are stored efficiently in a physical well located beneath a raised gate. The charge storage ability could be improved by using smaller band-gap material such as silicon-germanium in the convex channel region, providing deeper potential well.
- ✓ Band-gap engineered source and drain 1T-DRAM was investigated via simulations to improve the retention time. By using wide band-gap silicon-carbon as source and drain (Fig. 5-6f) [246], a deeper potential well in the fully-depleted body is achieved. The silicon-carbon source/drain induces a valence band offset and more holes can be stored in the body. For the '1' and '0'-state programming, impact ionization and forward biased junction techniques were used, respectively. Less hole leakage (two or three orders) through the source-body junction than in traditional 1T-DRAM allows longer retention time (100 ms at 300 K) and good sensing margin (100 μA/μm).
- ✓ Another technique known as dopant segregated Schottky barrier (DSSB) including partially silicided layer at source and drain edges was proposed [247]. The body of the device provides an improved volatile storage medium for 1T-DRAM operation: because the partially silicided regions at the source/drain-body interface prevents the leak out of the accumulated holes from the body, leading to an improved retention

time (70 ms).

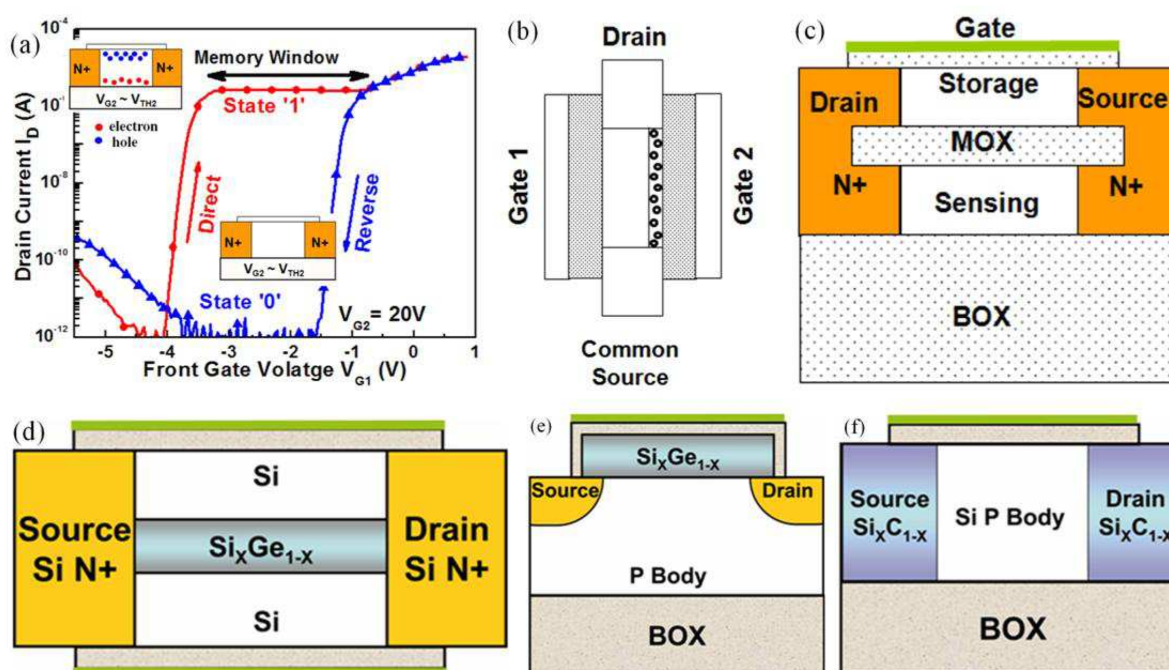

Fig. 5-6: Proposed 1T-DRAM architectures. (a) MSDRAM showing measured drain current and carrier distributions [237], (b) vertical 1T-DRAM [240], (c) ARAM [242], (d) quantum well 1T-DRAM [244], convex channel 1T-DRAM [245] and (f) band-gap engineered source and drain 1T-DRAM [246]

5.2.3. Unified RAM (URAM)

As we described in the introduction (Chapter 5.1.), co-integration of NVM and DRAM in a single chip requires additional process steps and high cost due to their distinct architectures. However, the users continuously demand more integration density and lower cost. The aim of URAM is to merge the two different memory functionalities in a single transistor. This fusion will lead to cost reduction, simpler fabrication procedure and higher yield and integration density.

Preliminary results of unified memories were published several years ago [216-218]. The flash memory operation is usually performed by using stacked oxide/nitride/oxide (ONO) layers at the top gate of the fin as a nonvolatile charge storage medium (Fig. 5-7a): Charges can be stored by Fowler-Nordheim tunneling or by hot-carrier injection mechanism. The volatile charges are stored in the isolated body of SOI FinFETs. By pushing the bottom of the fin body into the buried oxide (see Fig. 5-7a), volatile charge storage efficiency is improved.

Recently, other 1T-DRAM architectures with buried ONO layers have been proposed in our laboratory (Fig. 5-7b) [249, 250]. Buried nitride layer stores the nonvolatile charges by applying bias at the control gate (bottom gate) via Fowler-Nordheim tunneling. In this device, impact ionization technique and MSD effect have been successfully tested to store holes in the floating body for volatile operation.

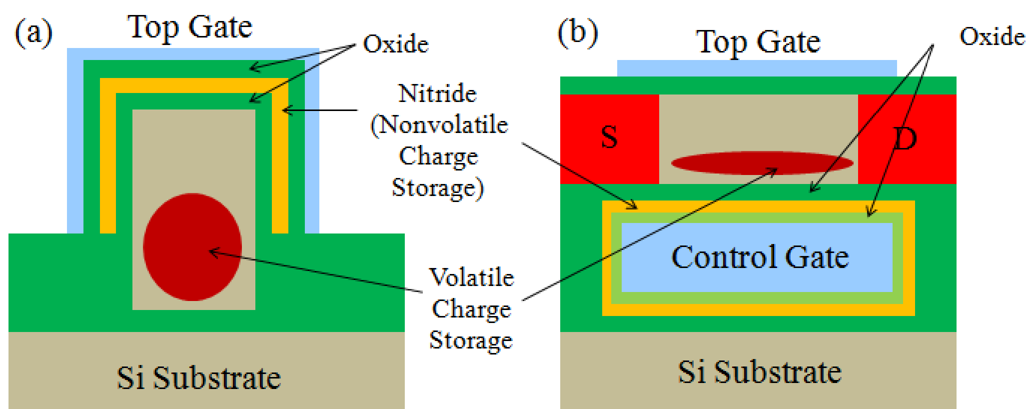

Fig. 5-7: Cross-section of already proposed unified memory cells. To store nonvolatile charges, ONO layers are located (a) at the top of the FinFETs [216] and (b) beneath the floating body [249]. The isolated body of the SOI MOSFET is used as the volatile storage medium.

While the unified memory is a promising concept in terms of density increase and cost per bit, it is difficult to avoid disturbance [249-252] between the two memory functions (NVM and 1T-DRAM), especially during programming and erasing. Moreover, the threshold voltage variation coming from each memory function must be de-correlated. For these reasons, unified memory needs to be further investigated.

5.3. Volatile Operation as a Capacitorless 1T-DRAM

In this section, a novel concept will be introduced demonstrating a unified and multi-bit volatile memory with FinFET architecture and buried ONO layer (Fig. 5-8). The originality of our URAM lies in the buried storage ONO layer combined with "standard" FinFET devices. Moreover, by combining wisely nonvolatile and volatile operations, several separated current levels, functional for a multi-bit DRAM application, will be demonstrated.

Nonvolatile charges will be stored by Fowler-Nordheim tunneling (back-gate biasing) or by localized carrier injection (drain biasing) and remotely sensed at the front-channel for flash memory operation (Fig. 5-8a). The holes generated by impact ionization for the volatile

memory operation are stored in the body (especially at front-interface) and sensed at the back-channel (Fig. 5-8b).

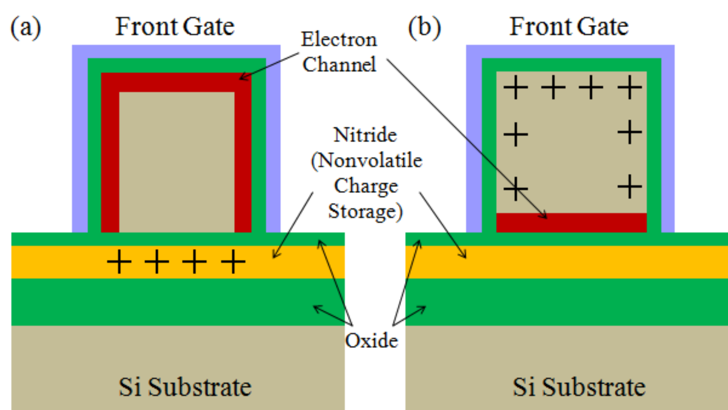

Fig. 5-8: A novel concept for unified memory with FinFETs fabricated on ONO buried insulator. (a) Nonvolatile charges are stored in the nitride layer and sensed at the front-channel. (b) Volatile charges are stored at the front interface and sensed at the back-channel.

In Fig. 5-9, we consider pure 1T-DRAM operation (programming and reading): the nitride is not charged and the back-channel is inverted (V_{BG} = +8 V > V_{THB} = +3.5 V) while the front interface is accumulated (V_{FG} = -1 V). The '1'-state (high current level) and the '0'-state (low current level) are programmed respectively by impact ionization [226-231] and forward biasing of the body-drain junction [226, 227, 229]. During the '1'-state programming (*i.e.*, generation of an excess of majority carriers (holes) inside the Si body), impact ionization is achieved by applying a positive drain pulse (V_D = +1.5 V). Notice that due to the negative front-gate bias, band-to-band tunneling at the gate-to-drain overlap region (V_D = +1.5 V, V_{FG} = -1 V) may also generate holes [233, 234]. The hot electrons move towards the drain contact whereas excess holes are kept inside the Si body thanks to the negative front-gate bias. As a result, during the reading operation, the current level is 'high' as the Si body potential was increased by the stored positive charges. For the '0'-state, negative drain (V_D = -0.5 V) and positive front-gate (V_{FG} = +0.8 V) voltages are applied. The body-drain junction is forward biased. The stored holes are expelled out of the body towards the drain contact and the current level switches to its 'low' state. Therefore, two distinct current levels are obtained (see Fig. 5-9b). A comfortable current level difference between the '0'- and '1'-state (*i.e.*, sensing margin) is achieved (ΔIS = 32 µA/µm).

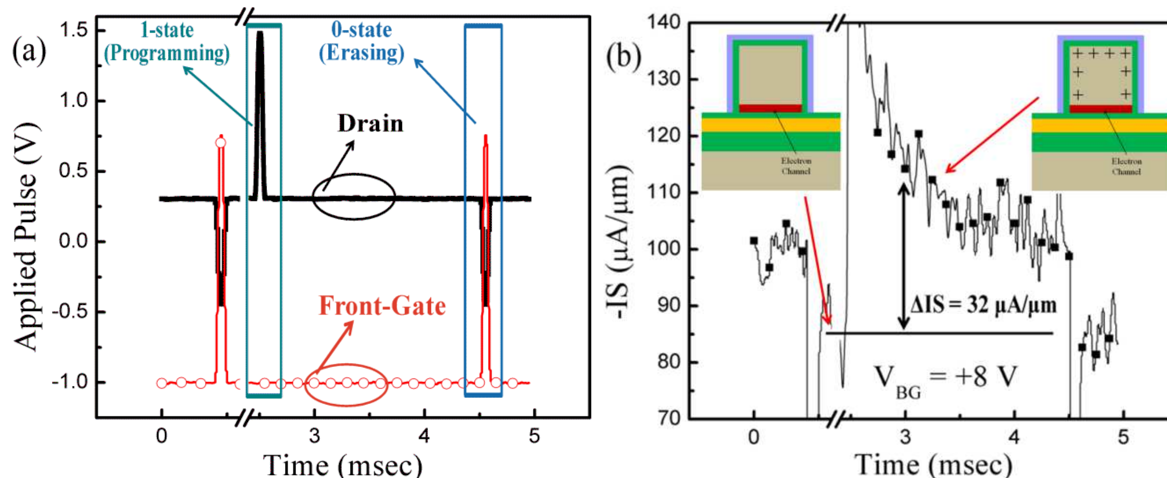

Fig. 5-9: (a) Applied pulses at drain and front-gate and (b) transient current for 1T-DRAM operation. L_G = 100 nm, W_F = 90 nm. Sensing margin ΔIS is defined as the source current difference between the '0'- and '1'-states after 0.5 ms reading.

5.3.1. Multi-bit volatile operation combined with back-gate biasing

The device structure is the same as the ONO FinFET discussed in Chapter 4. Transient drain currents are measured Keithley 4200 analyzer connected to a wafer probe station. Voltage pulses on drain and gate are applied with the analyzer so they are limited to the μsec range. Two different pulse patterns at drain and front-gate are applied simultaneously with a constant back-gate bias. A current to voltage converter (DHPCA-100, FEMTO) and oscilloscope (LeCroy 424, Iwatsu test instrument crop.) are connected in series at source for the source current sensing.

According to the polarity and amount of the charges stored in the buried nitride layer, the transient current shown in Fig. 5-9 is changed via remote coupling effect. In this section, we will demonstrate the multi-bit DRAM induced by the variation of the nonvolatile charge. According to the 'unified memory' concept, a single device (like our ONO FinFETs) can be operated either in volatile or in nonvolatile mode. On the other hand, the nonvolatile BOX charging promotes the 1T-DRAMs from single-bit to multi-bit volatile capability. The several '0'- and '1'-states of the 1T-DRAM result from the combination with the nonvolatile memory storage.

Fig. 5-10 compares transient current measurements in 1T-DRAM mode for positive, negative and zero trapped charge. The charge storage in the nitride is here performed by back-gate bias stress (charge injection mechanism is Fowler-Nordheim tunneling [203], see Chapter 4). When the back-channel threshold voltage is lowered with positive trapped

charges, the current level in both ‘0’ and ‘1’-states increases due to the coupling effects [14]. By contrast, if negative charges are trapped, the current decreases significantly because the effective V_{BG} is reduced. The current levels in Fig. 5-10 are separated enough for an easy identification of the ONO charge (positive or negative) and 1T-DRAM states (‘0’ or ‘1’). Fig. 5-10 ~ 5-14 show in more details how the trapped charges in the nitride layer modify quantitatively the dependence of the 1T-DRAM sensing margin on biasing and dimensional parameters.

According to the type of ONO trapped charges and their amount (modulated by back-gate stress), more than two current levels can be achieved with a sufficient sensing margin for multi-bit memory application (30 μA/μm ~ 45 μA/μm, Fig. 5-10). We verified that $I_D(V_{FG})$ curves, before and after many 1T-DRAM memory cycles (>10^5), remain unchanged. This clearly indicated that the multi-bit unified memory operation can be achieved without disturbance of the charges trapped in the nitride layer.

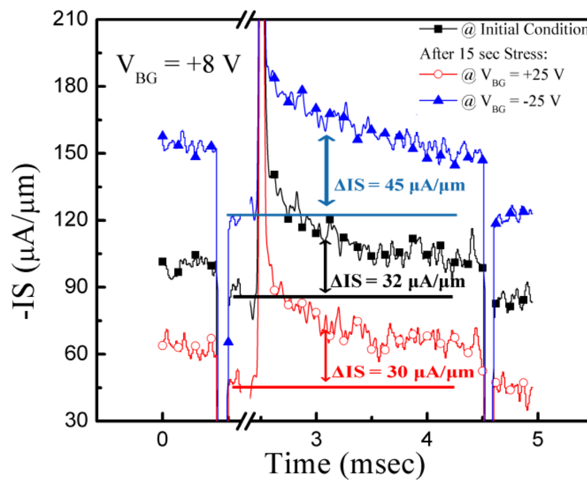

Fig. 5-10: Transient current for 1T-DRAM with prior nonvolatile ONO charging. Distinct current levels are obtained confirming multi-bit capability. Bias condition and device dimension as in Fig. 5-9. V_{FG} = -1V, V_D = +0.3 V, V_{BG} = +8 V.

Systematic measurements were performed with special attention paid to the sensing margin and its dependence on the biasing conditions. Fig. 5-11 shows the impact of the back-gate bias. At higher back-gate bias during reading operation, both ‘0’- and ‘1’-state current levels are increased due to stronger inversion of back-channel (Fig. 5-11a). Fig. 5-11b shows that, for$V_{BG} > V_{THB}$, the sensing margin sharply increases.

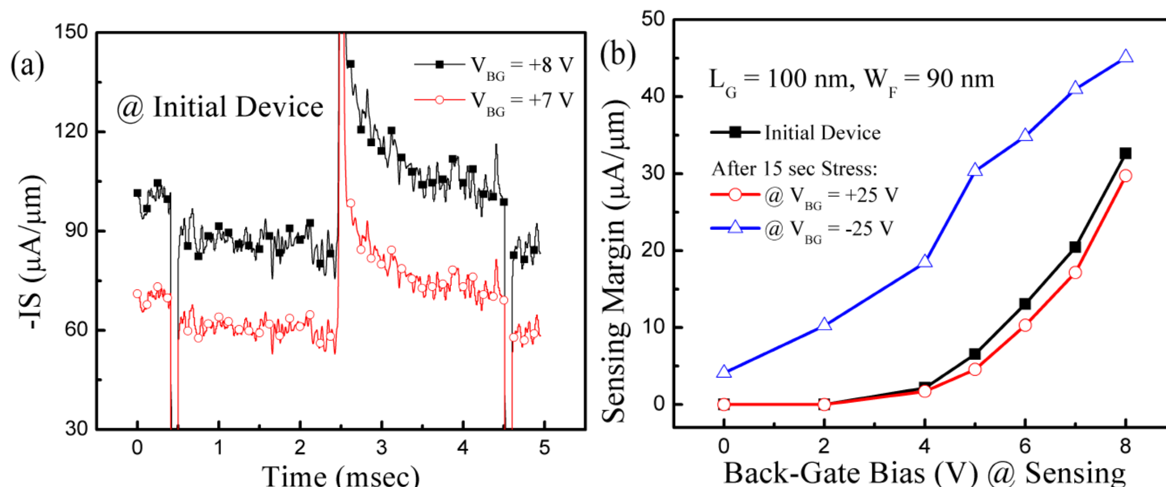

Fig. 5-11: Effect of back-gate bias on 1T-DRAM operation. (a) Transient current as a function of time for initial device (no charge stored in ONO BOX). (b) Impact of trapped charges and back-gate bias on volatile sensing margin. Definition of sensing margin, bias conditions and device dimension as in Fig. 5-9. V_{FG} = -1V, V_D = +0.3 V.

At higher V_D during '1'-state programming (Fig. 5-12a), more electron-hole pairs are generated by impact ionization and band-to-band tunneling at the top gate-to-drain overlap region. Therefore, the amount of stored holes is enlarged and '1'-state current level is increased as well as the sensing margin. For memory erasing, positive V_{FG} and negative V_D pulses are combined. When V_D is more negative, the cell erase is more efficient due to the stronger forward biased body-drain junction: '0'-state current level is reduced, further increasing the sensing margin (Fig. 5-12b).

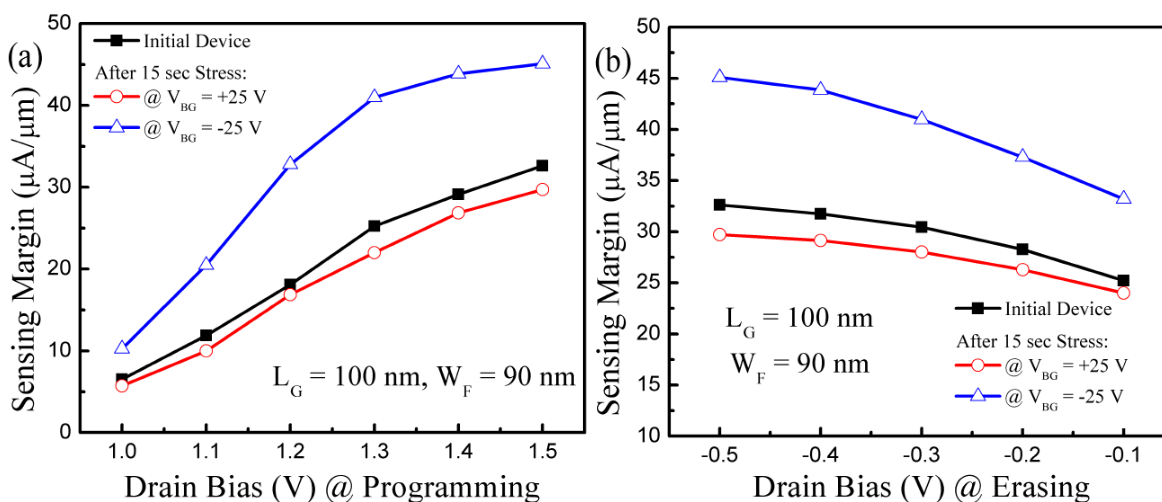

Fig. 5-12: Effect of trapped charges and drain pulses used for (a) programming and (b) erasing operation on the 1T-DRAM sensing margin. Definition of sensing margin and bias conditions as in Fig. 5-9.

For more negative V_{FG} during programming, more holes are stored in the body and the sensing margin is increased (Fig. 5-13a). For 'erase', the holes purge is accentuated by applying a less negative V_{FG}: the '0'-state current level is reduced and again the sensing margin is enlarged (Fig. 5-13b).

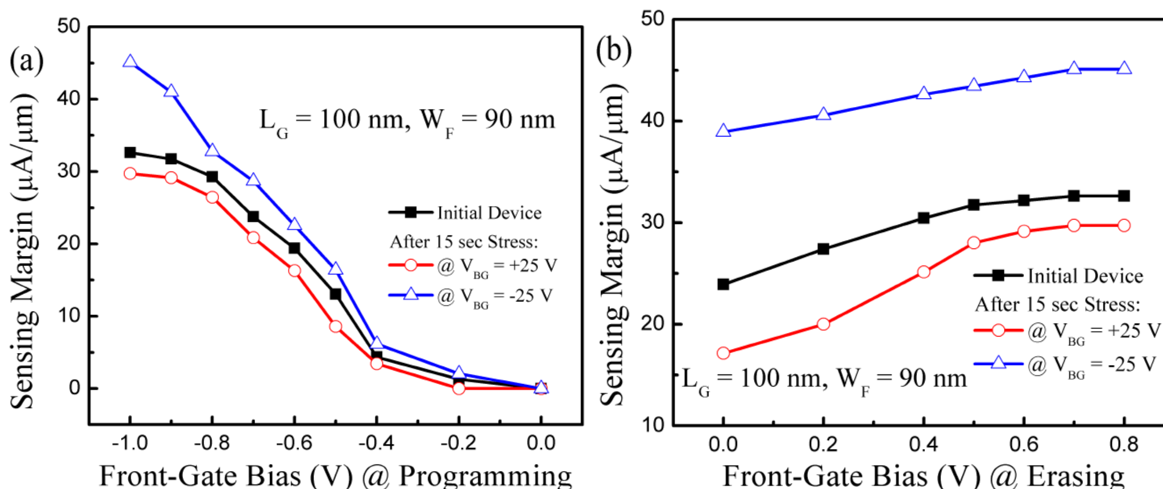

Fig. 5-13: Effect of trapped charges and front-gate pulses used for (a) programming and (b) erasing operation on the 1T-DRAM sensing margin. Definition of sensing margin and bias conditions as in Fig. 5-9.

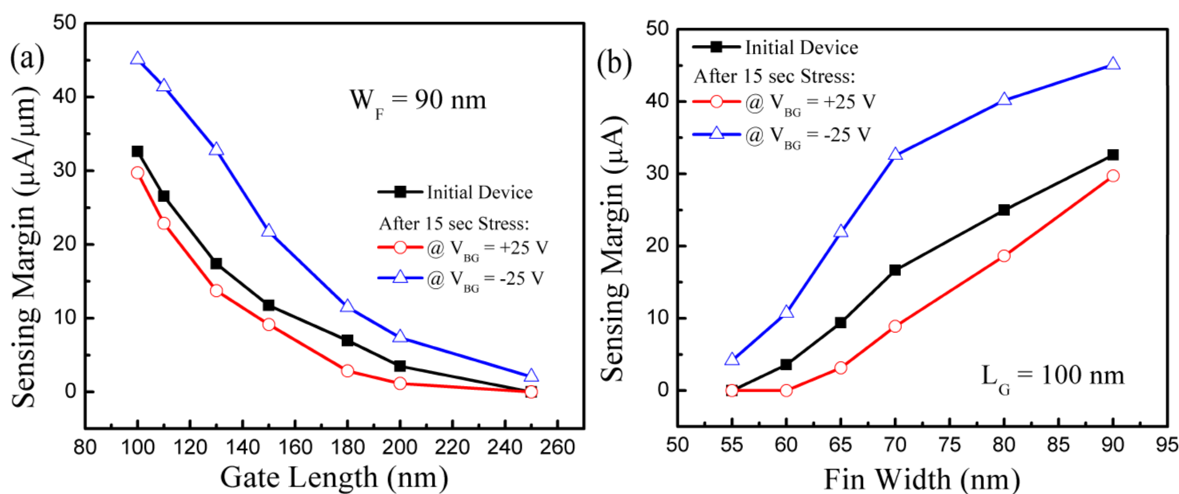

Fig. 5-14: Impact of trapped charges, (a) gate length and (b) fin width on the 1T-DRAM sensing margin.

The impact of FinFET geometrical parameters on the sensing margin is summarized in Fig. 5-14:

(i) In short devices, since the impact ionization rate and current level are higher, the sensing margin is improved (Fig. 5-14a). This result is promising for device scaling albeit it has to be mitigated with a degraded retention time.

(ii) In very narrow fins, the body volume is reduced and less holes can be stored;

moreover, the lateral field between the two sidewalls gates tends to control the potential at the body-BOX interface inhibiting the V_{BG} action [80, 211]. The effect of stored holes is also partially masked so the memory effect is reduced. (Fig. 5-14b). Wider fins exhibit better memory margin.

The trapped charges in the nitride, induced by the back-gate biasing, can "substitute" the back-gate bias during reading. Fig. 5-15a shows $I_D(V_{BG})$ curves before and after 15 sec stress at V_{BG} = ±25 V. The back-channel threshold voltage variation ΔV_{THB} between initial condition and after 15 sec stress with V_{BG} = -25 V is 2.5 V at V_{FG} = -1 V, V_D = 0.3 V. As seen in Fig. 5-15b, the two transient current levels measured in initial state (at V_{BG} = +8 V) and after 15 sec stress with V_{BG} = -25 V (measurement at V_{BG} = +5.5 V) are equal. The applied back-gate bias difference (*i.e.*, 2.5 V) for the volatile operation exactly corresponds to the ΔV_{THB}.

The transient currents after stress with V_{BG} = -25 V are identical in direct and reverse modes. This result gives evidence for the laterally uniform charge trapping induced by the back-gate stress. In the next section, where the non volatile charges will be injected with drain biasing, the non uniformity of the charge distribution will be highlighted.

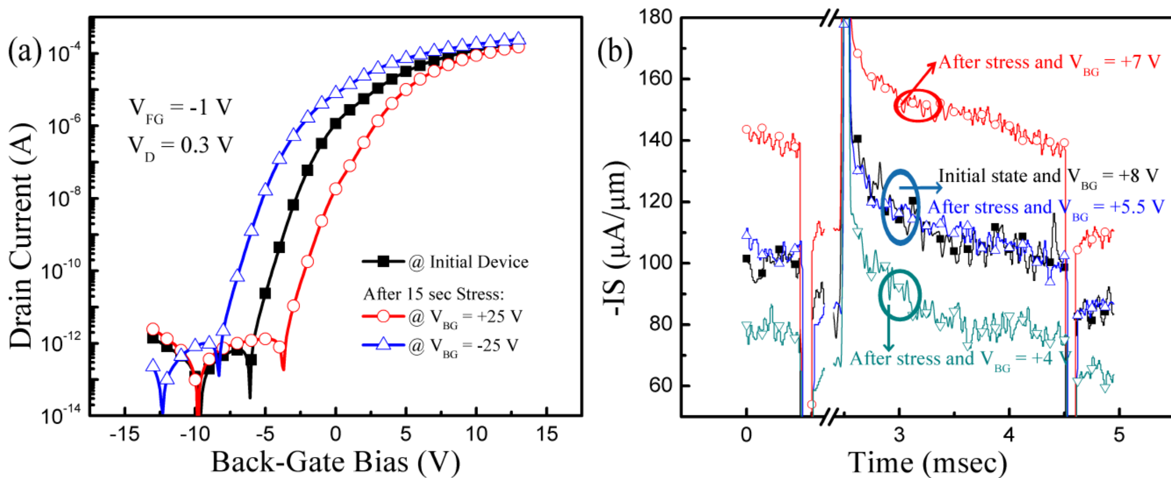

Fig. 5-15: Impact of uniformly stored charges in the nitride layer. (a) Drain current as a function of back-gate bias before and after 15 sec stress with V_{BG} = ±25 V. (b) Initial transient current at V_{BG} = +8 V (before stress) and after 15 sec stress with V_{BG} = -25 V (measured for several back-gate biases). Bias conditions as in Fig. 5-9. L_G = 100 nm, W_F = 90 nm, N_F = 16, V_{BG} = 0 V, V_D = 50 mV.

5.3.2. Multi-bit volatile operation combined with drain biasing

The multi-bit unified memory can also be operated by taking advantage of localized carrier injection via drain bias stress (see section 4.4.2). In Fig. 5-16a, the volatile transient

current after drain-induced carrier injection is evaluated. Like for the charge trapping with back-gate stress (Fig. 5-10), various volatile stages were achieved according to the injected charges. By comparing transient current in direct and reverse modes, we confirm again that the injected carriers are located near the drain contact (Fig. 5-16b). After 15 sec stress with V_D = +2.5 V, the ‘high’ and ‘low’ state current levels measured in direct mode are both higher than in reverse mode (due to the enhanced role of the positive injected charges located near the drain terminal). The sensing margin is slightly superior in direct mode.

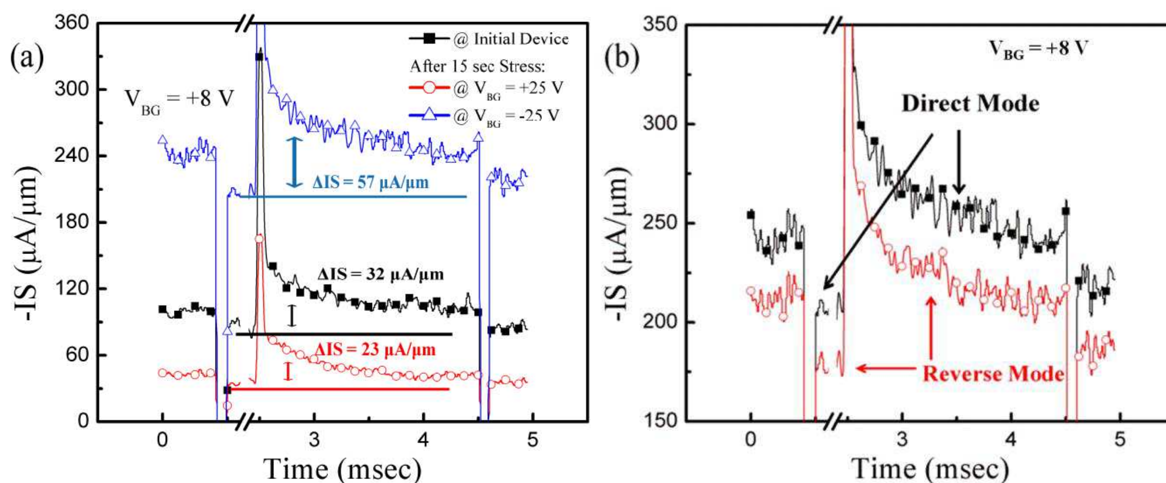

Fig. 5-16: Impact of charges injected into ONO BOX by drain biasing on 1T-DRAM behavior. (a) Distinct transient current levels with and without prior nonvolatile charges stored in the nitride buried layer (by 15 sec stress with V_D = ±2.5 V). (b) 1T-DRTAM transient current in direct and reverse modes after 15 sec stress with V_D = +2.5 V. Bias conditions and device dimension as in Fig. 5-15.

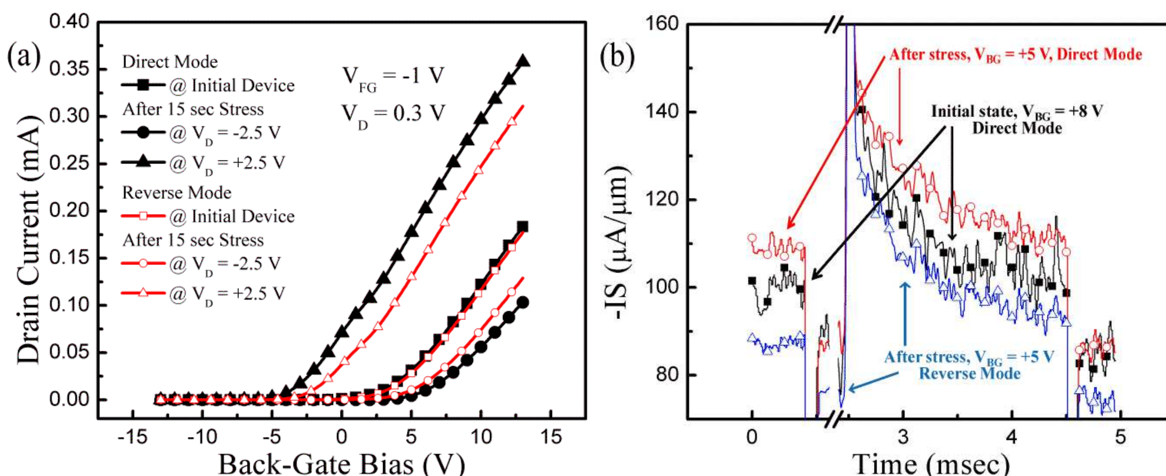

Fig. 5-17: Effect of locally injected charges in the Si_3N_4 layer on 1T-DRAM operation. (a) Drain current as a function of back-gate bias before and after 15 sec stress with V_D = ±2.5 V in direct and reverse mode. (b) Initial transient current measured in direct mode (at V_{BG} = +8 V) before stress and measured in direct and reverse mode (at V_{BG} = +5 V) after 15 sec stress with V_D = +2.5 V.

Unlike the case of uniform charge trapping, localized injected carriers cannot

compensate the effect of back-gate bias during read operation. In Fig. 5-17a, $I_D(V_{BG})$ curves in direct and reverse modes were measured before and after carrier injection by drain biasing. Double-bit nonvolatile memory is obtained, like for the front-channel (Fig. 4-21). In direct mode, we measured ΔV_{THB} = 7 V between virgin device and after stressing at V_D = +2.5 V at V_{FG} = -1 V. After stress, the 'low' state current level at V_{BG} = +5 V corresponds to that in the initial 'low' state at V_{BG} = +8 V (Fig. 5-17b). The back-gate bias difference is only 3 V, far smaller than ΔV_{THB} = 7 V. In addition, no match can be achieved for the 'high' state current level. It follows that the effect of the localized nonvolatile charge cannot be entirely compensated by adjusting V_{BG}.

Fig. 5-18 shows the extracted sensing margin of the volatile memory (1T-DRAM) after 15 sec stress at V_D = +2.5 V as a function of the back-gate bias in direct and reverse modes. When a higher back-gate bias is used for the readout of the volatile states, impact ionization is enhanced because the back-channel is more strongly inverted. Therefore, the current level in 'high' state and the sensing margin increase. In direct mode, both '0'- and '1'-state current levels are higher than in reverse mode due to the stronger effect of positive charges injected near drain side pinch-off region. As a result, in direct mode, the sensing margin is only 10 % larger at V_{BG} = +8 V than in reverse mode, despite these levels are quite different (see Fig. 5-16b). The charges located near the drain contact have a marginally larger influence on the sensing margin.

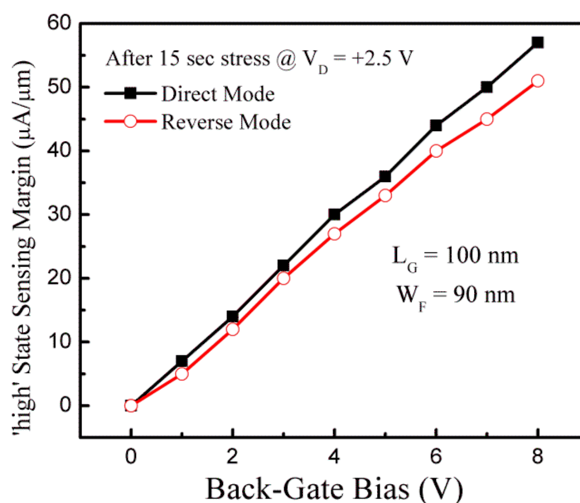

Fig. 5-18: 'High' state sensing margin of the volatile 1T-DRAM as a function of back-gate bias during readout in direct and reverse modes. Although the curves are rather identical, the current levels are very different.

5.4. Conclusion

The 1T-DRAM operation was investigated to evaluate the viability of the combination of volatile and nonvolatile memory modes in FinFETs fabricated on ONO multi-layer BOX. Our results not only confirm the reliability of our unified memory concept but also show the optimization trends. An improvement of the sensing margin in shorter devices with moderately wide fins was observed. Multi-bit unified memory operation was carried out as a preliminary ‘proof-of-concept’ without disturbance of the trapped charges. The sensing margin of the 1T-DRAM depends on the distribution of the trapped charges and is improved for nonvolatile charges located near the drain terminal. Another advantage of FinFETs with ONO BOX is the reconfigurability: analog, logic, nonvolatile and volatile memory operations can be combined within the same cell.

Conclusion

The evolution of electronic systems and portable devices requires innovation in both circuit design and transistor architecture. During last fifty years, the main issue in MOS transistor has been the gate length scaling down. The reduction of power consumption together with the co-integration of different functions is a more recent avenue. In bulk-Si planar technology, device shrinking seems to arrive at the end due to the multiplication of parasitic effects. The relay has been taken by novel SOI-like device architectures.

In this perspective, this manuscript presents the main achievements of our work obtained with a variety of advanced fully depleted SOI MOSFETs, which are very promising candidates for next generation MOSFETs. Their electrical properties have been analyzed by systematic measurements and clarified by analytical models and/or simulations. Ultimately, appropriate applications have been proposed based on their beneficial features.

In the first chapter, we briefly addressed the short-channel effects and the diverse technologies to improve device performance.

The second chapter was dedicated to the detailed characterization and interesting properties of SOI devices. We have demonstrated excellent gate control and high performance in ultra-thin FD SOI MOSFET. The SCEs are efficiently suppressed by decreasing the body thickness below 7 nm. We have investigated the transport and electrostatic properties as well as the coupling mechanisms. The strong impact of body thickness and temperature range has been outlined. A similar approach was used to investigate and compare vertical double-gate and triple-gate FinFETs. DG FinFETs show enhanced coupling to back-gate bias which is applicable and suitable for dynamic threshold voltage tuning. We have proposed original models explaining the 3D coupling effect in FinFETs and the mobility behavior in ZnO TFTs. Our results pointed on the similarities and differences in SOI and ZnO transistors. According to our low-temperature measurements and new promoted extraction methods, the mobility in ZnO and the quality of ZnO/SiO_2 interface are respectable, enabling innovating applications in flexible, transparent and power electronics.

In the third chapter, we focused on the mobility behavior in planar SOI and FinFET devices by performing low-temperature magnetoresistance measurements. Unusual mobility curve with multi-branch aspect were obtained when two or more channels coexist and

interplay. Another original result in the existence of the geometrical magnetoresistance in triple-gate and even double-gate FinFETs.

The operation of a flash memory in FinFETs with ONO buried layer was explored in the forth chapter. Two charge injection mechanisms were proposed and systematically investigated. We have discussed the role of device geometry and temperature. Our novel ONO FinFlash concept has several distinct advantages: double-bit operation, separation of storage medium and reading interface, reliability and scalability.

In the final chapter, we explored the avenue of unified memory, by combining nonvolatile and 1T-DRAM operations in a single transistor. The key result is that the transient current, relevant for 1T-DRAM operation, depends on the nonvolatile charges stored in the nitride buried layer. On the other hand, the trapped charges are not disturbed by the 1T-DRAM operation. Our experimental data offers the proof-of-concept for such advanced memory. The performance of the unified/multi-bit memory is already decent but will greatly improve in the coming years by processing dedicated devices.

References

[1] G. E. Moore. "Progress in digital integrated electronics", Electron Devices Meeting, 1975, IEEE International, vol. 21, pp. 11-13, 1975.

[2] C. G. Hwang. "Nanotechnology enables a new memory growth model", Proceedings of the IEEE, vol. 91(11), pp. 1765-1771, 2003.

[3] International Technology Roadmap for Semiconductors. Site: http://www.itrs.net/Links/2012Winter/1205%20Presentation/Metrology_12052012.pdf

[4] Q. Liu, A. Yagishita, N. Loubet, A. Khakifirooz, P. Kulkarnim, *et al*. "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond", VLSI Technology, 2010 Symposium on, pp. 61-62, 2010.

[5] D. Hisamoto, T. Kaga, E. Takeda. "Impact of the vertical SOI 'DELTA' structure on planar device technology', Electron Device, IEEE Transactions on, vol. 38(6), pp. 1419-1424, 1991.

[6] N. Lindert, L. Chang, Y.-K. Choi, E. H. Anderson, W.-C. Lee, *et al*. "Sub 60 nm quasi-planar FinFETs fabricated using a simplified process", Electron Device Letters, IEEE, vol. 22(10), pp. 487-489, 2001.

[7] A. Khakifirooz, K. Cheng, P. Kulkarni, J. Cai, S. Ponoth, *et al*. "Challenges and opportunities of extremely thin SOI (ETSOI) CMOS technology for future low power and general purpose system-on-chip applications", VLSI Technology Systems and Applications, 2010 International Symposium on, pp. 110-111, 2010.

[8] C. Fenouillet-Beranger, S. Denorme, P. Perreau, C. Buj, O. Faynot, *et al*. "FDSOI devices with thin BOX and ground plane integration for 32 nm node and below", Solid-State Electronics, vol. 53(7), pp. 730-734, 2009.

[9] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, *et al*. "A 22 nm high performance and low-power CMOS technology featuring fully-depleted triple-gate transistors, self-aligned contacts and high density MIM capacitors", VLSI Technology, 2012 Symposium on, pp. 131-132, 2012.

[10] K. J. Kuhn. "CMOS scaling for the 22 nm node and beyond: Device physics and technology", VLSI Technology, Systems and Applications, 2011 International Symposium on, pp. 1-2, 2011.

[11] G. K. Celler, S. Cristoloveanu. "Frontiers of silicon-on-insulator", Journal of Applied Physics, vol. 93(9), pp. 4995-4978, 2003.

[12] C. Fenouillet-Beranger, S. Denorme, B. Icard, F. Beouf, J. Coignus, *et al*. "Fully-depleted SOI technology using high-k and single-metal gate for 32 nm node LSTP applications featuring 0.179 μm^2 6T-SRAM bitcell", Electron Devices Meeting, 2007. IEEE International, pp. 267-270, 2007.

[13] D. Munteanu, D. A. Weiser, S. Cristoloveanu, O. Faynot, J.-L. Pelloie, *et al*. "Generation-recombination transient effects in partially depleted SOI transistors: systematic experiments and simulations", Electron Devices, IEEE Transactions on, vol. 45(8), pp. 1678-1683, 1998.

[14] H.-K. Lim, J. G. Fossum. "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's", Electron Devices, IEEE Transactions on, vol. 30(10), pp. 1244-1251, 1983.

[15] B. Mazhari, S. Cristoloveanu, D. E. Ioannou, A. L. Caviglia. "Properties of ultra-thin wafer-bonded silicon-on-insulator MOSFET's", Electron Device, IEEE Transactions on, vol. 38(6), pp. 1289-1295. 1991.

[16] T. Ouisse, S. Cristoloveanu, G. Borel. "Influence of series resistances and interface coupling on the transconductance of fully-depleted silicon-on-insulator MOSFETs", Solid-State Electronics, vol. 35(2), pp. 141-149, 1992.

[17] B. G. Streetman, S. Banerjee. *Solid state electronics 6th edition*. Prentice Hall series in solid state physical electronics 2006, Upper Saddle River, N. J.: Pearson/Prentice Hall.

[18] W. Muller, I. Eisele. "Velocity saturation in short channel field effect transistors", Solid-State Communications, vol. 34(6), pp. 447-449, 1980.

[19] L. D. Yau. "A simple theory to predict the threshold voltage of short-channel IGFET's", Solid-State Electronics, vol. 17(10), pp. 1059-1063, 1974.

[20] J. E. Chung, M.-C. Jeng, J. E. Moon, P.-K. Ko, C. Hu. "Low-voltage hot-electron currents and degradation in deep-submicrometer MOSFETs", Electron Device, IEEE Transactions on, vol. 37(7), pp. 1651-1657, 1990.

[21] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand. "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits", Proceedings of the IEEE, vol. 91(2). pp. 305-327, 2003.

[22] N. Kotani, S. Kawazu. "Computer analysis of punch-through in MOSFETs", Solid-State Electroncis, vol. 22(1), pp. 63-70, 1979.

[23] R. J. E. Hueting, A. Heringa. "Analysis of the subthreshold current of pocket or halo- implanted nMOSFETs", Electron Devices, IEEE Transactions on, vol. 53(7), pp. 1641-1646, 2006.

[24] J. J. Barnes, K. Shimohigashi, R. W. Dutton. "Short-channel MOSFET's in the punchthrough current mode", Electron Devices, IEEE Transactions on, pp. 446-153, vol. 26(4), 1979.

[25] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, *et al*. "High-k/metal gate stack and its MOSFET characteristics", Electron Device Letters, IEEE, vol. 25(6), pp. 408-410, 2004.

[26] T. M. Klein, D. Niu, W. S. Epling, W. Li, D. M. Maher, *et al*. "Evidence of aluminum silicate formation during chemical vapor deposition of amorphous Al_2O_3 thin films on Si (100), Applied Physics Letters, vol. 75(25), pp. 4001-1003, 1999.

[27] J. Kwo, M. Hong, A. R. Kortan, K. T. Queeney, Y. J. Chabal, *et al*. "High epsilon gate dielectrics Gd2O3 and Y2O3 for silicon, Applied Physics Letters, vol. 77(1), pp. 130-132, 2000.

[28] S. Guha, E. Cartier, M. A. Gribelyuk, N. A. Borjarczuk, M. A. Copel. "Atomic beam deposition of lanthanum- and yttrium-based oxide thin film for gate dielectrics", Applied Physics Letters, vol. 77(17) pp. 2710-2712, 2000.

[29] M. T. Bohr, R. S. Chau, T. Chani, K. Mistry. "The high-k solution", Spectrum, IEEE, vol. 44(10), pp. 29-35, 2007.

[30] G. D. Wilk, R. M. Walliace, J. M. Anthony. "High-k gate dielectrics: current status and materials properties considerations", Journal of Applied Physics, vol. 89(10), pp. 5243-5275, 2001.

[31] www.intel.com.

[32] C. Wee, S. Maikap, C. Y. Yu. "Mobility enhancement technologies", Circuits and Devices Magazine, IEEE, vol. 21(3), pp. 21-36, 2005.

[33] Q. T. Nguyen, J. F. Damlencourt, B. Vincent, L. Clavelier, T. Morand, P. *et al*. "High quality germanium-on-insulator wafers with excellent hole mobility", Solid-State Electronics, vol. 51(9), pp. 1172-1179, 2007.

[34] M. H. Lee, P. S. Chen, Y. T. Tseng, Y. M. Hsu, S. W. Lee, *et al*. "Performance enhancement in strained-Si NMOSFETs on SiGe virtual substrate", Proceeding, Symposium, Nano Device Technology, pp. 28-31, 2003.

[35] S. Thompson, G. Sun, K. Wu, J. Lim, T. Nishida. "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs, Electron Device Meeting, 2004, IEEE Technical Digest, IEEE International, pp. 221-224, 2004.

[36] L. Pham-Nguyen, C. Renouillet-Beranger, G. Ghibaudo, T. Skotnicki, S. Cristoloveanu. "Mobility enhancement by CESL strain in short-channel ultrathin SOI MOSFETs", Solid-State Electronics, vol. 54(2), pp. 123-130, 2010.

[37] J. P. Douglas. "Si/SiGe heterostuctures: from material and physics to devices and circuits", Semiconductor Science and Technology, vol. 19(10), pp. R75-R108, 2004.

[38] L. Grenouillet, M. Vinet, J. Gimbert, B. Giraud, J. P. Noel, *et al*. "UTBB SOI transistors with dual STI for a multi-Vt strategy at 20 nm node and below", Electron Devices Meeting, 2012 IEEE International, pp. 3.6.1-3.6.4, 2012.

[39] W. Chaisantikulwat, M. Mouis, G. Ghibaudo, S. Cristoloveanu, J. Widiez, *et al*. "Experimental evidence of mobility enhancement in short-channel ultra-thin body double-gate MOSFETs by magnetoresistnace technique", Solid-State Electronics, vol. 51, pp. 1494-1499, 2007.

[40] B. Dufrene, K. Akavardar, S. Cristoloveanu, B. J. Blalock, P. Gentil, *et al*. "Investigation of the four-gate

action in G4-FETs", Electron Deivce, IEEE Transactions on, vol. 51(11), pp. 1931-1935, 2004.

[41] D.-Y. Jeon, S. J. Park, M. Mouis, M. Berthome, S. Barraud, *et al*. "Revisited parameter extraction methodology for electrical characterization of junctinoless transistors", Solid-State Electronics, vol. 81, pp. 113-118, 2013.

[42] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Tan, *et al*. "Nanowire transistors without junctions", Nature Nanotechnology, vol. 5, pp. 225-229, 2010.

[43] R. Rios, A. Capellani, M. Armstrong, A. Budrevich, H. Gomez, *et al*. "Comparison of junctionless and conventional trigate transistors with L_g down to 26 nm", Electron Devices Letters, IEEE, vol. 32(9), pp. 1170-1172, 2011.

[44] A. J. Strojwas. "Is the bulk vs. SOI battle over?", VLSI Technology, Systems and Applications, 2013, International Symposium on, pp. 1-2, 2013.

[45] A. K. Schroder. *Semiconductor material and device characterization*, John Wiley & Sons, 2006.

[46] G. Ghibaudo. "New method for the extraction of MOSFET parameters", Electronics Letters, vol. 24(9), pp. 543-545, 1988.

[47] P. K. MaLarty, S. Cristoloveanu, O. Faynot, V. Misra, J. R. Hauser, *et al*. "A simple parameter extraction method for ultra-thin oxide MOSFETs", Solid-State Electronics, vol. 38(6), pp. 1175-1177, 1995.

[48] C. G. Sodini, T. W. Ekstedt, J. L. Moll. "Charge accumulation and mobility in thin dielectric MOS transistors", Solid-Sate Electronics, vol. 25(9), pp. 833-841, 1982.

[49] G. Merckel, J. Borel, N. Z. Cupcea. "An accurate large-signal MOS transistor model for use in computer-aided design", Electron Device, IEEE Transactions on, vol. 19(5), pp. 681-690, 1872.

[50] C. Hao, B. Cabon-Till, S. Cristoloveanu, G. Ghibaudo. "Experimental determination of short-channel MOSFET parameters", Solid-State Electronics, vol. 28(10), pp. 1025-1030, 1985.

[51] J. Koomen. "Investigation of the MOST channel conductance in weak inversion", Solid-State Electronics, vol. 16(7), pp. 801-810, 1973.

[52] P. C. Yeh, J. G. Fossum. "Physical subthreshold MOSFET modeling applied to viable design of deep-submicrometer fully depleted SOI low-voltage CMOS technology", Electron Devices, IEEE Transactions on, vol. 42(9), pp. 1605-1613, 1995.

[53] T. Ernst, D. Munteanu, S. Cristoloveanu, T. Ouisse, S. Horiguchi, *et al*. "Investigation of SOI MOSFETs with ultimate thickness", vol. 48(4), pp. 339-342, 1999.

[54] T. Ernst, C. Tinella, C. Raynaud, S. Cristoloveanu. "Fringing fields in sub-0.1μm fully depleted SOI MOSFETs: optimization of the device architecture", Solid-State Electronics, vol. 46(3), pp. 373-378, 2002.

[55] T. Numate, S. Takagi. "Device design for subtheshold slope and threshold voltage control in sub-100 nm fully depleted SOI MOSFETs", Electron Devices, IEEE Transactions on, vol. 51(2), pp. 2161-2167, 2004.

[56] A. Vandooren, D. Jovanovic, S. Egley, M. Sadd, B. Y. Nguyen, *et al*. "Scaling assessment of fully-depleted SOI technology at the 30 nm gate length generation", SOI Conference, IEEE International, pp. 25-27, 2002.

[57] C. Maleville. "Extending planar device roadmap beyond node 20 nm through ultra thin body technology", VLSI Technology, Systems and Applications, 2011 International Symposium on, pp. 1-4, 2011.

[58] C. Gallon. Solutions alternatives avancées pour les prochaines générations de transistor CMOS SOI complètement déplété à simple grille, dissertation-INPG, 2007.

[59] F. Gamiz, J. B. Roldan, J. A. Lopez-Villanueva. "Phonon-limited electron mobility in ultrathin silicon-on-insulator inversion layers", Journal of Applied Physics, vol. 83(9), pp. 4802-4806, 1998.

[60] N. Xu, F. Andrieu, J. Jeon, X. Sun, O. Weber, *et al*. "Stress induced performance enhancement in Si ultra-thin body FD-SOI MOSFETs: Impacts of scaling", VLSI Technology, 2011 Symposium, pp. 162-163, 2011.

[61] Y. Omura, S. Horiguchi, M. Tabe, K. Kishi. "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs", Electron Device Letters, IEEE, vol. 14(12), pp. 569-571, 1993.

[62] H. S. P. Wong, D. J. Frank, P. M. Solomon. "Device design considerations for double-gate, ground-plane and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation", Electron Devices Meeting, 1998 Technical Digest. International, pp. 407-410, 1998.

[63] J. P. Denton, G. W. Neudeck. "Fully depleted dual-gated thin-film SOI P-MOSFETs fabricated in SOI islands with an isolated buried polysilicon backgate", Electron Device Letters, IEEE, vol. 17(11), pp. 509-511, 1996.

[64] P. C. Yeh, J. G. Fossum. "Viable deep-submicron FD/SOI CMOS design for low-voltage applications", SOI Confence, 1994, Proceedings, IEEE International, pp. 23-24, 1994.

[65] W. Liqiong, C. Zhanping, K. Roy. "Double gate dynamic threshold voltage (DGDT) SOI MOSFETs for low power high performance designs", SOI Conference, 1997, Proceedings, IEEE International, pp. 82-83, 1997.

[66] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, *et al*. "A dynamic threshold voltage MOSFET (DTMOS) for ultra-thin voltage operation", Electron Devices Meeting, 1994, Technical Digest, IEEE International, pp. 809-812, 1994.

[67] Y. Taur, T. H. Ning. *Fundamentals of modern VLSI devices*. Cambridge University Press, New York, NY, USA, 1998.

[68] K. Tachi, S. Barraud, K. Kakushima, H. Iwai, S. Cristoloveanu, *et al*. "Comparison of low-temperature electrical characteristics of gate-all-around nanowire FETs, FinFETs and fully-depleted SOI FETs", Microelectronics Reliability, vol. 51, pp. 885-888, 2011.

[69] K. Uchida, J. Koga, S. Takagi. "Experimental study on electron mobility in ultrathin-body silicon-on-insulator metal-oxide-semiconductor filed-effect transistors", Journal of Applied Physics, vol. 102(7): 074510, 2007.

[70] S. Cristoloveanu, S. S Li. *Electrical characterization of silicon-on-insulator materials and devices*, Kluwer Academic Publishers, 1995.

[71] M. J. Deen, Z. X. Yan. "DIBL in short-channel NMOS devices at 77 K", Electron Devices, IEEE Transactions on, vol. 39(4), pp. 908-915, 1992.

[72] J. C. S. Woo, J. D. Plummer. "Short-channel effects in MOSFET's at liquid-Nitrogen temperature", Electron Devices, IEEE Transactions on, vol. 33(7), pp. 1012-1019, 1986.

[73] V. P. Trivedi, J. G. Fossum, W. Zhang. "Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra-thin bodes", Solid-State Electronics, vol. 51. pp. 170-178, 2007.

[74] O. Weber, F. Andrieu, J. Mazurier, M. Casse, X. Garros, *et al*. "Work-function engineering in gate first technology for multi-V_T dual-gate FDSOI CMOS on UTBOX", Electron Device Meeting (IEDM), 2010 IEEE International, pp. 3.4.1-3.4.4, 2010.

[75] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J. –P. Noel, *et al*. "Low leakage and low variability Ultra-Thin Body and Buried Oxide (UT2B) SOI technology for 20nm low power CMOS and beyond", VLSI Tech. (VLSIT), 2010 Symposium on, pp. 57-58, 2010.

[76] P. Nguyen, F. Andrieu, X. Garros, J. Widiez, G. Molas, *et al*. "Ultra-thin buried nitride integration for multi-V_T, low-variability and power management in planar FDSOI CMOSFETs", VLSI Tech. (VLSIT), Symposium on, 2010, pp. 164-165, 2011.

[77] J. –P. Colinge. Solid-State Electronics, "Multiple-Gate SOI MOSFETs", vol. 48(6), pp. 897-905, 2004.

[78] X. Huang, W. –C. Lee, C. Kuo, D. Hisamoto, L. Chang, *et al*. "Sub-50 nm P-channel FinFET", Electron Devices, IEEE Transactions on, vol. 48(5), pp. 880-886, 2001.

[79] R. Chau, B. Doyle, J. Kavalieros, D. Barlage, A. Murthy, *et al*. "Advanced depleted-substrate transistors: single-gate, double-gate and triple-gate", ISSDMC Nagoya Japan, 2002.

[80] K. –I. Na, S. Cristoloveanu, Y. –H. Bae, P. Patruno, J. –H. Lee. "Short channel, floating body, and 3D coupling effects in triple-gate MOSFET", Int. J. High Speed Electron. Sys., vol. 18(4), pp. 773-782, 2008.

[81] A. Ohata, S. Cristoloveanu, M. Casse. "Mobility comparison between front and back channels in ultrathin silicon-on-insulator metal-oxide-semiconductor field-effect transistor by the front-gate split capacitance-voltage method", Applied Physics Letters, vol. 89(3), 032104, 2006.

[82] K. Akarvardar, A. Mercha, S. Cristoloveanu, P. Gentil, E. Simoen, *et al*. "A two-dimensional model for interface coupling in triple-gate transistors", Electron Devices, IEEE Transactions on, vol. 54(4), pp. 767-775, 2007.

[83] S.-J. Chang, M. Bawedin, Y. Guo, F. Liu, K. Akarvardar, *et al*. "Enhanced coupling effects in vertical double-gate FinFETs" under review for Solid-State Electronics.

[84] M. Casse, J. Pretet, S. Cristoloveanu, T. Poiroux, C. Fenouillet-Beranger, *et al*. "Gate-induced floating-body effect in fully-depleted SOI MOSFETs with tunneling oxide and back-gate biasing", Solid-State Electronics, vol. 48(7), pp. 1242-1247, 2004.

[85] Sentaurus Workbench version F-2011.09, Synopsys.

[86] B. Bayraktaroglu, K. Leedy, R. Neidhard. "ZnO Nanocrystalline High Performance Thin Film Transistors", Int. J. High Speed Electronics and Systems, vol. 20(1), pp. 171-182, 2011.

[87] K. Minegishi, Y. Koiwai, Y. Kikuchi, K. Yano, M. Kasuga, *et al*. "Growth of p-type zinc oxide films by chemical vapor deposition", Jpn. J. Appl. Phys. vol. 36(2), pp. L1453-L1455, 1997.

[88] M. Joseph, H. Tabata, T. Kawai. "p-Type Electrical Conduction in ZnO Thin Films by Ga and N Codoping", Jpn. J. Appl. Phys. vol. 38, pp. L1205-L1207, 1999.

[89] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, T. Hitoshi, *et al*. "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties", J. Appl. Phys., vol. 93(3), pp. 1624-1630, 2003.

[90] J.-I. Song, J.-S. Park, H. Kim, Y.-W. Heo, J.-J. Kim. "Transparent amorphous indium zinc oxide thin-film transistors fabricated at room temperature", Appl. Phys. Lett., vol. 90(2), 022106, 2007.

[91] O. Yutaka, N. Tsukasa, B. Takayuki, T. Yasutaka. "Thin film transistor of ZnO fabricated by chemical solution deposition", Jpn. J. Appl. Phys., vol. 40(1), pp. 297-298, 2001.

[92] F. X. Xiu, Z. Yang, L. J. Mandalapu, D. T. Zhao, J. L. Liu, *et al*. "High-mobility Sb-doped p-type ZnO by molecular-beam epitaxy", Appl. Phys. Lett., vol. 87(15), 152101, 2005.

[93] M. C. Fortunato Elvira, M. C. Barquinha Pedro, C. M. B. G. Pimentel Ana, M. F. Goncalves Alexandra, J. S. Marques Antonio, *et al*. "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature", Appl. Phys. Lett., vol. 85(13), pp. 2541-2543, 2004.

[94] D. Redinger, V. Subramanian. "High-performance chemical-bath-deposited zinc oxide thin-film transistors", Electron Devices, IEEE Transactions on, vol. 54(6), pp. 1301-1307, 2007.

[95] D. A. Mourey, D. A. Zhao, J. Sun, T. N. Jackson. "Fast PEALD ZnO thin-film transistor circuits", Electron Devices, IEEE Transactions on, vol. 57(2), pp. 530-534, 2010.

[96] S. Yoshizawa, K. Nishimura, T. Sakurai. "Preparation of ZnO thin film by newly designed horizontal-typed MOCVD chamber", J. Phys. Conf. Series, vol. 100(8), 2008.

[97] B. J. Norris, J. Anderson, J. F. Wager, D. A. Keszler. "Spin-coated zinc oxide transparent transistors", J. Phys. D Appl. Phys. vol. 36(20), pp. L105-L107, 2003.

[98] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, *et al*. "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", Nature, vol. 432, pp. 488-492, 2004.

[99] B. Bayraktaroglu, K. Leedy. "Pulsed laser deposited ZnO for thin film transistor applications", ECS Trans., vol. 16, pp. 61-73, 2008.

[100] M. D. Jacunski, M. S. Shur, M. Hack. "Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFTs", Electron Device, IEEE Transaction on, vol. 43(9), pp. 1433-1440, 1996.

[101] A. T. Hatzopoulos, D. H. Tassis, C. A. Dimitriadis, G. Kamarinos. "Analytical on-state current model of polycrystalline silicon thin-film transistors including the kink effect", Appl. Phys. Lett. vol. 87, 064501, 2005.

[102] M. D. Jacunski, M. S. Shur, A. A. Owusu, T. Ytterdal, M. Hack, *et al*. "A short-channel DC SPICE model for polysilicon thin-film transistors including temperature effects", Electron Devices, IEEE Transactions on, vol. 46(6), pp. 1146-1158, 1999.

[103] M. Wang, M. Wong. "An effective channel mobility-based analytical on-current model for polycrystalline silicon thin-film transistors", IEEE Trans. Electron Device, vol. 54(4), pp. 869-874, 2007.

[104] R. L. Hoffman. "ZnO-channel thin-film transistors: Channel mobility", J. Appl. Phys. vol. 95, 5813, 2004.

[105] F. Torricelli, J. R. Meijboom, E. Smits, A. K. Tripathi, M. Ferroni, *et al*. "Transport Physics and Device Modeling of Zinc Oxide Thin-Film Transistors Part I: Long-Channel Devices", IEEE Trans. Electron Devices, vol. 58(8), pp. 2610-2619, 2011.

[106] F. Torricelli, E. Smits, J. R. Meijboom, A. K. Tripathi, G. H. Gelinck, *et al*. "Transport physics and device modeling of zinc oxide thin-film transistors—Part II: Contact resistance in short channel devices ", IEEE Trans. Electron Devices, vol. 58(9), pp. 3025-3033, 2011.

[107] J. Jang. C. R. Kagan. P. Andry. "Thin Film Transistors", Marcel Dekker, New York, pp. 35-65, 2003.

[108] M. Grundmann, H. Frenzel, A. Lajn, M. Lorenz, F. Schein, *et al*. "Transparent semiconducting oxides: materials and devices", Physica Status Solidi (a), vol 207(6), pp. 1437-1449, 2010.

[109] U. Oezguer, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, *et al*. "A comprehensive review of ZnO materials and devices", Journal of Applied Physcis, vol. 98: 041301, 2005.

[110] C. Klingshirn. "ZnO: material, physics and applications", European Journal of Chemical Physics and Physical Chemistry, vol. 8(6), pp. 782-803, 2007.

[111] A. R. Hutson. "Hall effect studies of doped zinc oxide single crystals", Physical review, vol. 108(2), pp. 222-230, 1957.

[112] M. S. Shur, *Physics of Semiconductor Device*, Prentice Hall, Englewood Cliffs, New Jersey, 1990.

[113] C. Jagadish, S. Pearton. *Zinc oxide bulk, thin films and nanostructures: processing, properties, and applications*, Elsevier, Oxford, UK. 2011.

[114] R. L. Hoffman, B. J. Norris, J. F. Wager. "ZnO-based transparent thin-film transistors", Applied Physics Letters, vol. 82(5), pp. 733-735, 2003.

[115] P. F. Carcia, R. S. Mclean, M. H. Reilly. "High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition", Applied Physics Letter, vol. 88(12): 123509, 2006.

[116] J. L. Vossen. P. Chaudhari, H. Raether. *Physics of thin films*, Academic Press, New York, 1997.

[117] R. J. Lad, P. D. Funkenbusch, C. R. Aita. "Postdeposition annealing behavior of RF sputtered ZnO films", Journal of Vacuum Science and Technology, vol. 17(4), pp. 808-811, 1980.

[118] P. Fons, K. Iwata, S. Niki, A. Yamada, K. Matsubara, *et al*. "Uniaxial locked growth of high quality epitaxial ZnO films on (1 1 /2 0)α-Al_2O_3", Journal of Crystal Growth, vol. 209(2-3), pp. 532-536, 2000.

[119] C. K. Lau, S. K. Tiku, K. M. Lakin. "Growth of epitaxial ZnO thin films by organometallic chemical vapor deposition", Journal of Electrochemical Society, vol. 127(8), pp. 1843-1847. 1980.

[120] Y. Kashiwaba, K. Haga, H. Watanabe, B. P. Zhang, Y. Segawa, *et al*. "Structures and photoluminescence properties of ZnO films epitaxially grown by atmospheric pressure MOCVD", Physica Status Solidi (b), vol. 229(2), pp. 921-924, 2002.

[121] J. J. Robbins, J. Esteban, C. Fry, C. A. Wolden. "An investigation of the plasma chemistry involved in the synthesis of ZnO by PECVD", Journal of Electrochemical Society, vol. 150(10), pp. C693-C698, 2003.

[122] B. S. Li, Y. C. Liu, D. Z. Shen, Y. M. Lu, J. Y. Zhang, *et al*. "Growth of high quality ZnO thin films at low temperature on Si(100) substrates by plasma enhanced chemical vapor deposition", Journal of Vacuum Science & Technology A: Vacuum, Surface, and Films, vol. 20(1), pp. 265-269, 2002.

[123] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, J. Peter, *et al*. "Stable ZnO thin film transistors by fast open air atomic layer deposition", Applied Physics Letters, vol. 92(19):192101, 2008.

[124] D. B. Christey, G. K. Hubler. Pulsed laser deposition of thin films, Wiley-VCH, 2003.

[125] S. Cristoloveanu, D. Munteanu, M. S. T. Liu. "A review of the pseudo-MOS transistor in SOI wafers: operation, parameter extraction, and applications", IEEE Transactions on, vol. 47(5), pp. 1018-1027, 2000.

[126] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, T. Ytterdal. “SPICE models for amorphous silicon and polysilicon thin film transistors”, Journal of Electrochemical Society, vol. 144(8), pp. 2833-2839, 1997.

[127] D. J. Grant. *Physics and Modeling of Nanocrystalline Silicon Thin-Film Transistors*, Department of Electrical & Computer Engineering University of Wateloo, 2003.

[128] D. Dosev, T. Ytterdal, J. Pallares, L. F. Marsal, B. Iniquez. “DC SPICE model for nanocrystalline and microcrystalline silicon TFTs”, IEEE Trans. Electron Device, vol. 49(11), pp. 1979-1984, 2002.

[129] T. Hirao, M. Furuta, T. Hiramatsu, T. Matsuda, C. Furuta, H. *et al*. “Bottom-gate zincoxide thin-film transistors (ZnO TFTs) for AM-LCDs,” IEEE Trans. Electron Devices, vol. 55(11), pp. 3136–3142, 2008.

[130] R. Navamathavan, C. K. Choi, E. J. Yang, J. H. Lim, D. K. Hwang, *et al*. “Fabrication and characterization of ZnO thin film transistors prepared by using radio frequency magnetron sputtering,” Solid State Electron., vol. 52(5), pp. 813–816, 2008.

[131] S. Cristoloveanu, “State-of-the-art and future of silicon on insulator technologies, materials, and devices”, Microelectronics Reliability, vol. 40(4), pp. 771-777, 2000.

[132] T. Elewa, F. Balestra, S. Cristoloveanu, I. M. Hafez, J. P. Colinge, *et al*. “Performance and physical mechanisms in SIMOX MOS transistors operated at very low temperature”, IEEE Trans. Electron Device, vol. 37(4), pp. 1007-1019, 1990.

[133] H. S. Wong, M. H. White, T. J. Krutsic, R. V. Booth. “Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's“, Solid-State Electronics, vol. 30(9), pp. 953-968, 1987.

[134] A. Emrani, F. Balestra, G. Ghibaudo. “Low temperature electrical characterization of metal-nitrided oxide-silicon field effect transistors”, IEEE Trans. Electron Devices, vol. 40(3), pp. 1821-1831, 1993.

[135] J. Levinson, F. R. Shepherd, W. D. Westwood, G. Este, M. Rider. “Conductivity behavior in polycrystalline semiconductor thin film transistors”, Journal of Applied Physics, vol. 53(2). pp. 1193-1202, 1982.

[136] F. V. Farmakis, J. Brini, G. Kamarinos, C. T. Angelis, C. A. Dimitriadis, *et al*. “On-current modeling of large-grain polycrystalline silicon thin-film transistors”, IEEE Trans. Electron Device, vol. 48(4), pp. 701-706, 2001.

[137] N. Rodriguez, S. Cristoloveanu, F. Gamiz. “Revisited pseudo-MOSFET models for the characterization of ultrathin SOI wafers”, IEEE Trans. Electron Device, vol. 56(7), pp. 1507-1515, 2009.

[138] G. Hamaide, F. Allibert, H. Hovel, S. Cristoloveanu. “Impact of free-surface passivation on silicon on insulator buried interface properties by pseudotransistor characterization”, Journal of Applied Physcis, vol. 101(11), pp. 114513: 1–6, 2007.

[139] A. T. Hatzopoulous, D. H. Tassis, N. A. Hastas, C. A. Dimitriadis, G. Kamarinos. “On-state drain current modeling of large-grain poly-Si TFTs based on carrier transport through latitudinal and longitudinal grain boundaries”, IEEE Trans. Electron Device, vol. 52(8), pp. 1727-1733, 2005.

[140] M. Mouis, G. Ghibaudo, S. Cristoloveanu, J. Widiez, M. Vinent, *et al*. “Experimental evidence of mobility enhancement in short-channel ultra-thin body double-gate MOSFETs”, Proc. EESDERC, pp. 367-370, 2006.

[141] A. Ohata, Y. Bae, C. Fenouillet-Beranger, S. Cristoloveanu. “Mobility enhancement by back-gate biasing in ultrathin SOI MOSFETs with thin BOX”, Electron Device Letters, IEEE, vol. 33(3), pp. 348-350, 2012.

[142] L. Pham-Nguyen, C. Fenouillet-Beranger, A. Vandooren, T. Skotnicki, G. Ghibaudo, *et al*. “In-situ comparison of Si/High-K and Si/SiO_2 channels properties in SOI MOSFETs”, Electron Device Letters, IEEE, vol. 30(10), pp. 1075-1077, 2009.

[143] S. Cristoloveanu, N. Rodriguez, F. Gamiz. “Why the universal mobility is not”, Electron Devices, IEEE Transactions on, vol. 57(6), pp. 1327-1333, 2010.

[144] C. Navarro, N. Rodriguez, A. Ohata, F. Gamiz, F. Adrieu, *et al*. “Multibranch mobility analysis for the characterization of FD SOI transistors”, Electron Device Letter, IEEE, vol. 33(8), pp. 1102-1104, 2012.

[145] O. M. Corbino. “Electomagnetic effects resulting from the distortion of the path of ions in metals produced by a filed”, Physik, Zeitschr, vol. 12, pp. 561-568, 1911.

[146] S. Lakeou, S. Cristoloveanu, A. Chovet. "Magnetoresistance effect in near intrinsic semiconductors. Influence of sample geometry. A new method for the determination of carrier densities and mobilities", Physica Status Solidi(a), vol. 43(1), pp. 213-222, 1977.

[147] Y. M. Meziani, J. Lusakowski, W. Knap, D. Dyakonova, F. Teppe, *et al*. "Magnetoresistance characterization of nanometer Si metal-oxide-semiconductor transistors", Journal of Applied Physics, vol. 96(10), pp. 5761-5765, 2004.

[148] W. Chaisantikulwat, M. Mouis, G. Ghibaudo, C. Gallon, C. Fenouillet–Beranger, *et al*. "Differential magnetoresistance technique for mobility extraction in ultra-short channel FDSOI transistors", Solid-State Electronics, vol. 50(4), pp. 637-643, 2006.

[149] M. Casse, F. Rochette, L. Thevenod, N. Bhouri, F. Andrieu, *et al*. "A comprehensive study of magnetoresistance mobility in short channel transistors: Application to strained and unstrained silicon-on-insulator field-effect transistors", Journal of Applied Physics, vol. 105(8): 084503, 2009.

[150] S. Cristoloveanu, T. V. Chandrasekhar Rao, Q. T. Nguyen, J. Antoszewsk, H. Hovel, *et al*. "The Corbino Pseudo-MOSFET on SOI: measurement, model and applications", Electron Devices, IEEE Transactions on, vol. 56(3), pp. 474-482, 2009.

[151] P. R. Jay, R. H. Wallis. "Magnetotransconductance mobility measurements of GaAs MESFETs", Electron Device Letters, IEEE, vol. 2(10), pp. 265-267, 1981.

[152] K. Chen, H. C. Wann, P. K. Ko, C. Hu. "The impact of device scaling and power supply change on CMOS gate performance", Electron Device Letters, IEEE, vol. 17(5), pp. 202-204, 1996.

[153] J. T. Watt, J. D. Plummer. "Universal mobility-field curve for electrons and holes in MOS inversion layers", VLSI Technology, 1987. Digest of Technical Papers. Symposium on, pp. 81-82, 1987.

[154] L. Donetti, F. Gamiza, S. Cristoloveanu. "Monte Carlo simulation of Hall and magnetoresistance mobility in SOI devices", Solid-State Electronics, vol. 51(9), pp. 1216-1220, 2007.

[155] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, *et al*. "Unexpected mobility degradation for very short devices: A new challenge for CMOS scaling", Electron Devices Meeting, 2006, International, pp. 1-4, 2006.

[156] L. D. Tau. "A simply theory to predict the threshold voltage of short-channel IGFET's", Solid-State Electronics, vol. 17(10), pp. 1059-1063, 1974.

[157] A. L. Perin, R. Giacomini. "Sensing magnetic fields in any direction using FinFETs and L-Gate FinFETs", SOI Conference, 2012 IEEE International, pp. 1-2, 2012.

[158] W. A. Back, J. R. Anderson. "Determination of electrical transport properties using a novel magnetic field-dependent Hall technique", Journal of Applied Physics, vol. 62(2), pp. 541-554, 1981.

[159] I Vurgaftman, J. R. Meyer, C. A. Hoffman, D. Redfern, J. Antoszewski, *et al*. "Improved quantitative mobility spectrum analysis for Hall characterization", Journal of Applied Physics, vol. 84(9), pp. 4966-4973, 1998.

[160] K. Oshima, S. Cristoloveanu, B. Guillaumot, H. Iwai, S. Deleonibus. "Advanced SOI MOSFETs with buried alumina and ground plane: self-heating and short-channel effects", Solid-State Electronics, vol. 48(6), pp. 907-917, 2004.

[161] S. Cristoloveanu, G.K. Celler. *in Handbook of Semiconductor Manufacturing Technology*, CRC Press, London, 2007.

[162] P. Patruno, M. Kostrzewa, K. Landry, W. Xiong, C. R. Cleavelin, *et al*. "Study of Fin Profiles and MuGFETs built on SOI Wafers with a Nitride-Oxide Buried Layer (NOx-BL) as the Buried Insulator Layer", 2007 IEEE International SOI Conference, pp. 51-52, 2007.

[163] R. Ranica, A. Villaret, P. Mazoyer, S. Monfray, D. Chanemougame, *et al*. "A new 40-nm SONOS structure based on backside trapping for nanoscale memories", Nanotechnology, IEEE Transactions on, vol. 4(5), pp. 581-587, 2005.

[164] H. Silva, S. Tiwari. "A nanoscale memory and transistor using backside trapping", Nanotechnology, IEEE Transactions on, vol. 3(2), pp. 264-269, 2004.

[165] Sung Hwan Kim, Hyun Jum Bae, Sung In Hong, Yong Lack Choi, Eun Jung Yoon, *et al*. "High performance Silicon-on-ONO (SOONO) cell array transistors (SCATs) for 512Mb DRAM cell array application", Electron Devices Meeting, 2007, IEEE International, pp. 35-38, 2007.

[166] A. Hubert, E. Nowak, K. Tachi, V. Maffini-Alvaro, C. Vizioz, *et al*. "A stacked SONOS technology, up to 4 levels and 6nm crystalline nanowires, with gate-all-around or independent gates (Φ-Flash), suitable for full 3D integration", Electron Devices Meeting, 2009, IEEE International, pp. 1-4, 2009.

[167] Chang Woo Oh, Na Young Kim, Sung Hwan Kim, Yong Lack Choi, Sung In Hong, *et al*. "4-bit double SONOS memories (DSMs) using single-level and multi-level cell schemes", Electron Devices Meeting, 2006, IEEE International, pp. 1-4, 2006.

[168] S. Aritome. "Advanced flash memory technology and trends for file storage application", Electron Devices Meeting, 2000. IEDM Technical Digest. International, pp. 763-766, 2000.

[169] I. W. Cho, B. R. Lim, J.-H. Kim, S. S. Kim, KC Kim, *et al*. "Full integration and characterization of Localized ONO Memory (LONOM) for embedded flash technology", VLSI Technology, 2004. Digest of Technical Papers, 2004 symposium on, pp. 240-241, 2004.

[170] C. C. Yeh, W. J. Tsai, T. C. Lu, H. Y. Chen, H. C. Lai, *et al*. "Novel operation schemes to improve device reliability in a localized trapping storage SONOS-type Flash memory", Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International, pp. 7.5.1-7.5.4, 2003.

[171] S.-K. Sungm I.-H. Park. C.-J. Lee, Y. K. Lee, J. D. Lee, *et al*. "Fabrication and program/erase characteristics of 30 nm SONOS nonvolatile memory devices", Nanotechnology, IEEE Transactions on, vol. 2(4), pp. 258-264, 2003.

[172] H. C. Wann, C. Hu. "High endurance ultra thin tunneling oxide in MONOS device structure for dynamic memory application" Electron Device Letters, IEEE, vol. 16(11), pp. 491-493, 1995.

[173] S.-I. Minami, Y. Kamigaki. "A novel MONOS nonvolatile memory device ensuring 10 year data retention after 10^7 erase/write cycles", Electron Device, IEEE Transactions on, vol. 40(11), pp. 2011-2017, 1993.

[174] F. Masuoka, M. Momodomi, Y. Iwata, R. Shirota. "New ultra high density EPROM and Flash with NAND structure cell", Electron Devices Meeting, 1987 International, pp. 552-555, 1987.

[175] S. Lai. "Flash memories: Where we were and where we are going", Electron Devices Meeting, 1998, Technical Digest. International, pp. 971-973, 1998.

[176] P. Pavan, R. Bez, P. Olivo, E. Zanoni. "Flash memory cells-An overview", Proceedings of the IEEE, vol. 85(8), pp. 1248-1271, 2002.

[177] Y. Shin, J. Choi, C. Kang, C. Lee, K.-T. Park, J.-S. *et al*. "A novel NAND-type MONOS memory using 63 nm process technology for multi-gigabit flash EEPROMs", Electron Device Meeting, 2005, Technical Digest. IEEE International, pp. 327-330, 2005.

[178] P. Cappelletti, R. Bez, D. Cantarelli, L. Fratin. "Failure mechanisms of flash cell in program/erase cycling", Electron Devices Meeting, 1995, Technical Digest. International, pp. 291-294, 1994.

[179] C. Clementi, R. Bez. "Non volatile memory technologies: Floating gate concept evolution", MRS Proceedings, vol. 830, pp. D1.2.1-D1.2.12, 2004.

[180] K. Kim, J. Choi, "Future outlook of NAND flash technology for 40 nm node and beyond", Non-Volatile Semiconductor Memory Workshop, 2006, pp. 9-11, 2006.

[181] K. Naruke, S. Taguchi, M. Wada. "Stress induced leakage current limiting to scale down EEPROM tunnel oxide thickness", Electron Device Meeting, Technical Digest, IEEE International, pp. 424-427, 1988.

[182] J. S. Witters, G. Groeseneken, H. E. Maes. "Degradation of tunnel oxide floating gate EEPROM of thin gate oxide", Electron Devices, IEEE Transactions on, vol. 36(9), pp. 1663-1682, 1989.

[183] C.-Y. Lu, K.Y. Hsieh, R. Liu. "Future challenges of flash memory technologies", Microelectronic Engineering, vol. 86, pp. 283-286, 2009.

[184] B. De Salvo, C. Gerardi, S. Lombardo, T. Baron, L. Perniola, D. *et al*. "How far will silicon nanocrystals push the scaling limits of NVMs technologies?", Electron Device Meeting, 2003, Technical Digest. IEEE International, pp. 26.1.1-26.1.4, 2003.

[185] R. Bez, E. Camerlenghi, A. Pirovano. “Materials and processes for non-volatile memories”, Material Science Forum, vol. 608, pp. 111-132, 2009.

[186] K.-H. Joo, X. Wang, J. H. Han, S.-H. Lim, S.-J. Baik, *et al*. ”Novel transition layer engineered Si nanocrystal flash memory with MHSOS structure featuring large V_{th} window and fast P/E speed”, Electron Device Meeting, 2005, Technical Digest. IEEE International, pp. 765-868, 2005.

[187] C. H. Lee, K. I. Choi, M. Cho, Y. Song, K. Park, *et al*. “A novel SONOS structure of $SiO_2/SiN/Al_2O_3$ with TaN metal gate for multi-gigabit flash memories”, Electron Device Meeting, 2003, Technical Digest. IEEE International, pp. 613-616, 2003.

[188] Y. Fukuzumi, Y. Matsuoka, M. Kito, M. Kido, M. Sato, *et al*. “Optimal integration and characteristics of vertical array devices for ultra-high density, bit-cost scalable flash memory”, Electron Devices Meeting, 2007, IEEE International, pp. 449-452, 2007.

[189] F. Pellizzer, R. Bez. “Non-volatile semiconductor memories for nano-scale technology”, Nanotechnology (IEEE-NANO), 2010, IEEE conference on, pp. 21-24, 2010.

[190] J. E. Spanier, A. M. Kolpak, J. J. Urban, I. Grinberg, L.Ouyang, *et al*. “Ferroelectric phase transition in individual single-crystalline $BaTiO_3$ Nanowires”, Nano Letter, vol. 6(4), pp. 735-739, 2006.

[191] S. Tehrani, J. M. Slaughter, M. DeHerrera, B. N. Engel, N. D. Rizzo, *et al*. “Magnetoresistive random access memory using magnetic tunnel junctions”, Proceedings of IEEE, vol. 91(5), pp. 703-714, 2003.

[192] M. Kawasaki, A. Sawa, Y. Tokura. “Mechanism of resistance switching memory effect in oxides”, International conference on solid state devices and materials, pp. 286-287, 2006.

[193] A. Chen, S. Haddad, Y.-C. Wu, T.-N. Fang, Z. Lan, *et al*. “Non-volatile resistive switching for advanced memory applications”, Electron Devices Meeting, 2005, Technical Digest. IEEE Internatinoal, pp. 746-749. 2005.

[194] M. Kund, G. Beitel, C.-U. Pinnow, T. Rohr, J. Schumann, *et al*. “Conductive bridging RAM (CBRAM): An emerging non-volatile memory technology scalable to sub 20 nm”, Electron Devices Meeting, 2005. Technical Digiest. IEEE International, pp. 754-757, 2005.

[195] I. G. Baek, D. C. Kim, M. J. Lee, H.-J. Kim, E. K. Yim, *et al*. “Multi-layer cross-point binary oxide resistive memory (OxRAM) for post-NAND storage application”, Electron Devices Meeting, 2005. Technical Digiest. IEEE International, pp. 750-753, 2005.

[196] S. Lai, T. Lowrey, “OUM-A 180nm nonvolatile memory cell element technology for stand alone and embedded applications”, Electron Devices Meeting, 2001, Technical Digest. International, pp. 36.5.1.-36.5.4, 2001.

[197] M. Gill, T. Lowrey, J. Park. “Ovonic unified memory-a high-performance nonvolatile memory technology for stand-alone memory and embedded applications”, Solid-State Circuits Conference, 2002. Digest of Technical papers. IEEE International, pp. 202-459, 2002.

[198] H. Horii, J. H. Yi, J. H. Park, Y. H. Ha, I. G. Baek, *et al*. “A novel cell technology using N-doped GeSbTe films for phase change RAM”, VLSI technology, 2003, Digest of Technical papers. Symposium on, pp. 177-178, 2003.

[199] M. H. R. Lankhorst, B. W. S. M. M. Ketelaars, R. A. M. Wolters. “Low-cost and nanoscale non-volatile memory concept for future silicon chips”, Nature Materials, vol. 4, pp. 347-352, 2005.

[200] A. Pirovano, A. Redaelli, F. Pellizzer, F. Ottogalli, M. Tosi, *et al*. “Reliability study of phase-change nonvolatile memories”, Device and Material Reliability, IEEE Transactions on, vol. 4(3), pp. 422-427, 2004.

[201] S.-J. Chang, K.-I. Na, M. Bawedin, Y.-H. Bae, K.-H. Park, *et al*. “Investigation of hysteresis memory effects in SOI FinFETs with ONO buried insulator”, SOI Conference (SOI), 2010 IEEE International, pp. 1-2, 2010.

[202] F. Dauge, J. Pretet, S. Cristoloveanu, A. Vandooren, L. Mathew, *et al*. “Coupling effects and channels separation in FinFETs”, Solid-State Electronics, vol. 48, pp. 535-542, 2004.

[203] R. Bez, E. Camerlenghi, A. Modelli, A. Visconti. “Introduction to flash memory”, Proc, IEEE, vol. 91(4), pp. 489-502, 2003.

[204] T. Ouisse, S. Cristoloveanu, G. Borel. "Hot-carrier-induced degradation of the back interface in short-channel silicon-on-insulator MOSFETS", Electron Device Letters, IEEE, vol. 12(6), pp. 290–292, 1991.

[205] S. Cristoloveanu, "A review of the electrical properties of SIMOX substrates and their impact on device performance", J. Electrochem. Soc., vol. 138(10), pp. 3131–3139, 1991.

[206] T. Ouisse, S. Cristoloveanu, G. Borel. "Electron trapping in irradiated SIMOX buried oxides", Electron Device Letters, IEEE, vol. 12(6), pp. 312–314, 1991.

[207] M. Grossi, M. Lanzoni, R. Ricco. "Program schemes for multilevel flash memories", Proc, IEEE, vol. 91(4), pp. 594-601, 2003,

[208] Y. Wang, M.H. White. "An analytical retention model for SONOS nonvolatile memory devices in the excess electron state", Solid-State Electronics, vol. 49(1), pp. 97-107, 2005.

[209] D-H. Lee, W-D. Kim, J-H. Lee, B-G. Park. "Thickness-dependence of oxide-nitride-oxide erase property in SONOS flash memory", Semiconductor Device Research Symposium, ISDRS '09, pp. 1-2, 2009.

[210] S-H. Gu, C-W. Hsu, T. Wang, W-P. Lu, Y-H-J Ku, *et al*. "Numerical simulation of bottom oxide thickness effect on charge retention in SONOS flash memory cells", Electron Devices, IEEE Transactions on, vol. 54(1), pp. 90-97, 2007.

[211] Y.-H. Bae, K.-I. Na, S. Cristoloveanu, W. Xiong, C. R. Cleavelin, *et al*. "Special effects in triple gate MOSFETs fabricated on silicon-on-insulator (SOI)", Semiconductor Conference, 2009, CAS 2009, International, pp. 51-56, 2009.

[212] Deok-Su Jeon, Dorothea E. Burk, "MOSFET electron inversion layer mobilities – A physically based simi-empirical model for a wide temperature range", Electron Devices, IEEE Transactions on, vol. 36(8), pp. 1456-1463, 2002.

[213] W.J. Tsai, N.K. Zous, C.J. Liu, C.C. Liu, C.H. Chen, *et al*. "Data retention behavior of a SONOS type two-bit storage Flash memory cell", Electron Devices Meeting, 2001, Technical Digest, International, pp. 32.6.1-32.6.4, 2001.

[214] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni. "New generation of Z-RAM", Electron Devices Meeting, 2007, IEEE International, pp. 925-928, 2007.

[215] H.S. Seo, G.-C. Kang, S.R Kang, Y.K. Young, S. Lee, *et al*. "Dynamic bias temperature instability-like behaviors under Fowler–Nordheim program/erase stress in nanoscale silicon-oxide-nitride-oxide-silicon memories", Applied Physics Letters, vol. 92, pp. 133508, 2008.

[216] J.-W. Han, S.-W. Ryu, C.-J. Kim, S. Kim, M. Im, *et al*. "Partially depleted SONOS FinFET for unified RAM (URAM)—Unified function for high-speed 1T DRAM and nonvolatile memory", Electron Device Letters, IEEE, vol. 29(7), pp. 781-783, 2008.

[217] J.-W. Han, S.-W. Ryu, S. Kim, C.-J. Kim, J.-H. Ahn, *et al*. "Energy band engineered unified-RAM (URAM) for multi-functioning 1T-DRAM and NVM", Electron Device Meeting, 2008, IEEE International, pp. 1-4, 2008.

[218] Dong-Il Bae, S.-W. Ryu, B. Gu, Y.-K. Choi. "A new approach to cell size scaling with a multi-dual cell and a buffer/background programming of unified RAM", Microelectronic Engineering, vol. 87(2), pp. 135-138, 2010.

[219] M. Bawedin, S. Cristoloveanu, A. Hubert, J.H. Park, F. Martinez. "Floating-body SOI Memory: the scaling tournament", in *Semiconductor-On-Insulator Materials for Nanoelectronic Applications*, A. Nazarov, J. P. Colinge, F. Balestra, J. P. Raskin, F. Gamiz and V. Lysenko, Editors, pp. 393-421, Springer, Heidelberg, 2011.

[220] R. Ranica, A. Vilaret, C. Fenouillet-Beranger, P. Malinge, P. Mazoyer, *et al*. "A capacitor-less DRAM cell on 75nm gate length, 16nm thin fully depleted SOI device for high density embedded memories", Electron Device Meeting, 2004, Technical Digest, IEEE International, pp. 277-280, 2004.

[221] M. S. Kim, Won-Ju Cho. "Characteristics of Fully Depleted Strained-Silicon-On-Insulator Capacitorless Dynamic Random Access Memory Cells", Electron Device Letters, IEEE, vol. 30(12), pp. 1356-1358, 2009.

[222] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, *et al*. "Stable SRAM cell design for the 32 nm node and beyond", VLSI Technology, 2005, Dig. Technical Papers, pp. 128-129, 2005.

[223] T. Eimori, Y. Ohno, H. Kimura, J. Matsufusa, S. Kishimura, A. Yoshida, *et al*. “A newly designed planar stacked capacitor cell with high dielectric constant film for 256 MBIT DRAM”, Electron Device Meeting, 1993, Technical Digest. International, pp. 631-634, 1993.

[224] C. J. Radens, S. Kudelka, L. Nesbit, R. Malik, T. Dyer, *et al*. “An orthogonal 6F^2 trench-sidewall vertical device cell for 4GB/16GB DRAM”, Electron Deivce Meeting, 2000. Technical Digest, International. pp. 349-352, 2000.

[225] G. Aichmayr, A. Avellan, G. S. Duesberg, F. Lreupl, S. Kudelka, *et al*. “Carbon/high-k trench capacitor for the 40 nm DRAM generation”, VLSI Technology, 2007, IEEE Symposium on, pp. 186-187, 2007.

[226] S. Okhonin, M. Nagoga, J. M. Sallese, P. Fazan. “A SOI capacitor-less 1T-DRAM concept”, SOI Conference, 2001, IEEE International, pp. 153-154, 2001.

[227] S. Okhonin, M. Nagoga, J. M. Sallese, P. Fazan. “A SOI capacitor-less 1T-DRAM cell”, Electron Device Letters, IEEE, vol. 23(2), pp. 85-87, 2002.

[228] C. Kuo, T.-J. King, C. Hu, “A capacitorless double gate DRAM technology for sub-100 nm embedded and stand-alone memory applications”, Electron Devices, IEEE Transactions on, vol. 50(12), pp. 2408-2416, 2003.

[229] T. Shino, T. Ohsawa, T. Higashi, K. Fujita, N. Kusunoki, *et al*. “Operation voltage dependence of memory cell characteristics in fully depleted floating-body cell”, Electron Devices, IEEE Transactions on, vol. 52(10), pp. 2220-2226, 2005.

[230] T. Hamamoto, Y. Minami, T. Shino, N. Kusunoki, H. Nakajima, *et al*. “A floating-body cell fully compatible with 90-nm CMOS technology node for a 128-Mb SOI DRAM and its scalability”, Electron Devices, IEEE Transactions on, vol. 54(3), pp. 563-571, 2007.

[231] T. Hamamoto, T. Ohsawa. “Overview and future challenges of floating body RAM (FBRAM) technology for 32nm technology node and beyond”, Solid-State Electronics, vol. 53(7), pp. 676-683, 2009.

[232] K.-W. Song, H. Jeong, J.-W. Lee, S. I. Hong, K.-T. Nam, *et al*. “55 nm capacitor-less 1T DRAM cell transistor with non-overlap structure”, Electron Devices Meeting, 2008, IEEE International, pp. 1-4, 2008.

[233] S. Okhonin, P. Fazan, M.-E. Jones. “Zero capacitor embedded memory technology for system on chip”, Memory Technology, Design and Testing, 2005, IEEE International Workshop on, pp. xxi-xxv, 2005.

[234] E. Yoshida, T. Tanaka. “A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory”, Electron Devices, IEEE Transactions on, vol. 53(4), pp. 692-697, 2006.

[235] U. E. Avci, I. Ban, D. L. Kencke, P. L. D. Chang. “Floating body cell (FBC) memory for 16-nm technology with low variation on thin silicon and 10-nm BOX”, SOI Conference, 2008, IEEE International, pp. 29-30, 2008.

[236] M. Bawedin, S. Cristoloveanu, D. Flandre. “A capacitorless 1T-DRAM on SOI based on dynamic coupling and double-gate operation”, Electron Device Letters, IEEE, vol. 29(7), pp. 795-798, 2008.

[237] M. Bawedin, S. Cristoloveanu, Y. G. Yun, D. Flandre. “A new memory effect (MSD) in fully depleted SOI MOSFETs”, Solid-State Electonics, vol. 49(9), pp. 1547-1555, 2005.

[238] M. Bawedin, S. Cristoloveanu, D. Flandre, C. Renaux, A. Crahay. “Double-gate floating-body memory device”, Patent WO2009087125 (A1), 2008.

[239] A. Hubert, M. Bawedin, G. Guegan, S. Cristoloveanu, T. Ernst, *et al*. “Experimental comparision of programming mechanisms in 1T-DRAM cells with variable channel length”, Solid-State Device Research Conference, 2010, Proceedings of the European, pp. 150-153, 2010.

[240] H. Jeong, K.-W. Song, I. H. Park, T.-H. Kim, Y. S. Lee, *et al*. “A new capacitorless 1T DRAM cell: Surrounding gate MOSFET with vertical channel (SGVC cell)A new capacitorless 1T DRAM cell: Surrounding gate MOSFET with vertical channel (SGVC cell)”, Nanotechnology, IEEE Transactions on. Vol. 6(3), pp. 352-0357, 2007.

[241] H. K. Chung, H. Jeong, Y. S. Lee, J. Y. Song, J. P. Kim, *et al*. “A capacitor-less 1T-DRAM cell with vertical surrounding gates using gate-induced drain-leakage (GIDL) current”, Silicon Nanoelectronics Workshop, 2008, IEEE, pp. 1-2, 2008.

[242] N. Rodriguez, F. Gamiz, S. Cristoloveanu, “A-RAM memory cell: concept and operation”, Electron Device Letters, IEEE, vol. 31(9), pp. 972-974, 2010.

[243] N. Rodriguez, C. Navarro, F. Gamize, F. Andrieu, O. Faynot, *et al*. “Experimental demonstration of capacitorless A2RAM cells on silicon-on-insulator” Electron Device Letters, IEEE, pp. 1717-1719, 2012.

[244] M. G. Ertosun, P. Kapur, K. C. Saraswat. “A highly scalable capacitorless double gate quantum well single transistor DRAM: 1T-QW DRAM”, Electron Device Letters, IEEE, vol. 29(12), pp. 1405-1407, 2008.

[245] M. H. Cho, C. Shin, T. J. K. Liu, “Convex channel design for improved capacitorless DRAM retention time”, Simulation of semiconductor processes and devices, 2009, International Conference on, pp. 1-4, 2009.

[246] T. Poren, H. Ru, W. Dake, “Performance improvement of capacitorless dynamic random access memory cell with band-gap engineered source and drain”, Jpn. J. Appl. Phys. vol. 49. 04DD02, 2010.

[247] Y.-K. Choi, J.-W. Han, S. Kim, D.-H. Kim, M.-G. Jang, *et al*. “High speed flash memory and 1T-DRAM on dopant segregated Schottky barrier (DSSB) FinFET SONOS device for multi-functional SoC applications”, Electron Device Meeting, 2008, IEEE International, pp. 1-4, 2008.

[248] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata, G. Ghibaudo. “Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects”, Solid-State Electronics, vol. 51(2), pp. 239-244, 2007.

[249] K.-H. Park, M. Bawedin, J.-H. Lee, Y.-H. Bae, K.-I. Na, *et al*. “Fully depleted double-gate MSDRAM cell with additional nonvolatile functionality”, Solid-State Electronics, vol. 67(1). pp. 17-22. 2012.

[250] K.-H. Park, C. M. Park, S.H. Kong, J.-H. Lee. “Novel double-gate 1T-DRAM cell using nonvolatile memory functionality for high-performance and highly scalable embedded DRAMs”, Electron Devices, IEEE Transactions on, vol. 57(3), pp. 614-619, 2010.

[251] J.-W. Han, S.-I. Choi, D.-H. Kim, D.-I. Moon, Y.-K. Choi. “Gate-to-source/drain nonoverlap device for soft-program immune unified RAM (URAM)”, Electron Device Letters, IEEE, vol. 30(5), pp. 544-546, 2009.

[252] S.-J. Choi, C.-J. Kim, S. Kim, Y.-K. Choi. “Improvement of the sensing window on a capacitorless 1T-DRAM of a finFET-based unified RAM”, Electron Devices, IEEE Transactions on, vol. 56(12), pp. 3228-3231, 2009.

Publications

Journal Papers

1. **S.-J. Chang**, M. Bawedin, W. Xiong, J.-H. Lee, S. Cristoloveanu. "Hysteresis Effects in FinFETs with ONO Buried Insulator", ECS Transaction, 2011, Vol. 35(5), pp. 79-84.
2. **S.-J. Chang**, M. Bawedin, W. Xiong, S.C. Jeon, J.-H. Lee, S. Cristoloveanu. "A FinFET memory with remote carrier trapping in ONO buried Insulator", Microelectronic Engineering, 2011, Vol. 88, pp. 1203-1206.
3. **Sung-Jae Chang**, Maryline Bawedin, Wade Xiong, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu. "FinFlash with buried storage ONO layer for flash memory application", Solid-State Electronics, 2012, Vol. 70, pp. 59-66.
4. **Sung-Jae Chang**, Maryline Bawedin, Wade Xiong, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu. "Remote carrier trapping in FinFETs with ONO buried layer: Temperature effects", Microelectronics Reliability, 2013, Vol. 53, pp. 386-393.
5. **Sung-Jae Chang**, Muthupandian Cheralathan, Maryline Bawedin, Benjamin Iniguez, Burhan Bayraktaroglu, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu, "Mobility Behavior and Models for Fully Depleted Nanocrystalline ZnO Thin Film Transistors" will be published in Solid-State Electronics.
6. **Sung-Jae Chang**, Maryline Bawedin, Wade Xiong, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu. "FinFETs with ONO BOX for Multi-Bit Unified Memory", Microelectronic Engineering, 2013, Vol. 109, pp. 330-333.
7. **Sung-Jae Chang**, Maryline Bawedin, Wade Xiong, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu. "Multi-Bit Unified Memory Concept in FinFETs with ONO Buried Insulator", ECS Transaction, 2013, Vol. 54(1), pp. 321-328.
8. **Sung-Jae Chang**, Maryline Bawedin, Yufeng Guo, Fanyu Liu, Kerem Akarvardar, Jong-Hyun Lee, Jung-Hee Lee, Irina Ionica, Sorin Cristoloveanu. "Enhanced Coupling Effects in Vertical Double-Gate FinFETs", Solid-Sate Electronics, 2013. (Under review)

Conference Papers

1. **S.-J. Chang**, K.-I. Na, M. Bawedin, Y.-H. Bae, K.-H. Park, J.-H. Lee, W. Xiong. S.

Cristoloveanu. “Investigation of Hysteresis Memory Effects in SOI FinFETs with ONO Buried Insulator”, IEEE SOI Conference 2010, San Diego, USA, 2010

2. **S.-J. Chang**, M. Bawedin, W. Xiong, J.-H. Lee, S. Cristoloveanu. “Scaling of SOI FinFlash Memory with Buried Storage ONO Layer”, EUROSOI 2011, Granada, Spain, 2011.
3. **S.-J. Chang**, M. Bawedin, W. Xiong, J.-H. Lee, S. Cristoloveanu. “Analysis of Hysteresis Effects in FinFETs with ONO Buried Insulator”, 219th ECS Meeting, Montreal, Canada, May, 2011.
4. **S.-J. Chang**, M. Bawedin, B. Bayraktaroglu, J.-H. Lee, S. Cristoloveanu. “Low-Temperature Properties of ZnO on Insulator MOSFETs”, 2011 IEEE International SOI Conference, AZ, USA, 2011.
5. **S.-J. Chang**, M. Cheralathan, M. Bawedin, B. Iniguez, B. Bayraktaroglu, J-H. Lee, S. Cristoloveanu. “Mobility behaviour and models for ZnO TFTs”, International Advanced Workshop on ‘Frontiers in Electronics’ (WOFE’11), San Juan, Puerto Rico, 2011.
6. **S.-J. Chang**, M. Cheralathan, M. Bawedin, B. Iniquez, B. Bayraktaroglu, J.-H. Lee, J.-H. Lee, S. Cristoloveanu. “Mobility Model for SOI-like Nanocrystalline Zinc Oxide Thin-Film Transistor”, EuroSOI 2012 Conference, Montpellier, France, 2012.
7. **S.-J. Chang**, M. Cheralathan, M. Bawedin, K. Akavardar, J.-H. Lee, J.-H. Lee, S. Cristoloveanu. “Coupling Effects in Vertical Double-Gate SOI MOSFETs”, EuroSOI 2013 Conference, Paris, France, 2013.
8. **Sung-Jae Chang**, Mayline Bawedin, Wade Xiong, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu. “FinFET with ONO BOX for Nonvolatile and Unified Memory”, 20th Korean Conference on Semiconductor 2013, Korea, 2013.
9. **Sung-Jae Chang**, Mayline Bawedin, Wade Xiong, Jong-Hyun Lee, Jung-Hee Lee, Sorin Cristoloveanu. “Multi-bit unified memory concept in FinFETs with ONO buried insulator”, 4th international conference on semiconductor technology for ultra large scale integrated circuits and thin film transistors, France, 2013. **(BEST POSTER AWARD)**
10. **Sung-Jae Chang**, Maryline Bawedin, Jong-Hyun Lee, Jung-Hee Lee, S. Mukhopadhyay, B.A. Piot, Sorin Cristoloveanu. “Magnetoresistance measurements and unusual mobility behavior in FD MOSFETs”, Solid-State Device Research Conference (ESSDERC), 2013, Proceedings of the European, pp. 296-299, 2013.

Résumé du Travail de la Thèse en Français

Chapitre 1: Introduction générale

La miniaturisation des transistors conventionnels sur Si massif a atteint ses limites ce qui ouvre la voie aux technologies alternatives. Les deux principales technologies CMOS en compétition sont le FinFET et le FDSOI planaire (privilégié à Grenoble). Ces deux types de transistors partagent des effets similaires : désertion totale (FD), canaux multiples, couplage des interfaces, substrat flottant, etc. Leur miniaturisation est basée sur l'amincissement du corps du transistor.

Notre sujet de thèse était initialement orienté vers les dispositifs mémoires sur SOI (chapitres 4 et 5). L'étude des effets "mémoire" sur FDSOI et FinFET nous a naturellement menés vers les mécanismes de couplage, de transport et de canal court. Nous avons noté des aspects inédits qui méritaient une analyse détaillée faisant appel à des mesures en basse température et à fort champ magnétique. Ces résultats font l'objet des deux chapitres suivants.

Notre travail est fondé sur la combinaison de mesures systématiques, de modélisations physiques et de simulations numériques pour la validation des résultats et des concepts.

Chapitre 2: Dispositifs avancés et effets typiques

2.1. Propriétés typiques des transistors FD SOI

La structure des transistors planaires FD SOI est illustrée en Fig. 1. L'oxyde enterré est mince (T_{BOX} = 25 nm) et le film de Si est ultra-mince (t_{si} = 5 nm, 7 nm and 10 nm) au meilleur état de l'art. La longueur de grille descend jusqu'à L_G = 30 nm, afin d'étudier l'influence de l'épaisseur sur les effets de canal court (SCE), de transport et de couplage des canaux. Le diélectrique de grille (SiO_2 et HfO_2) a une épaisseur effective EOT de 1.6 nm. Un plan de masse (ground plane ou GP) a été implanté sous le BOX afin de pouvoir moduler la tension de seuil (stratégie de back-biasing). Tous les dispositifs ont une grille métal au-dessus du film non-implanté. Ces transistors présentent d'excellentes performances.

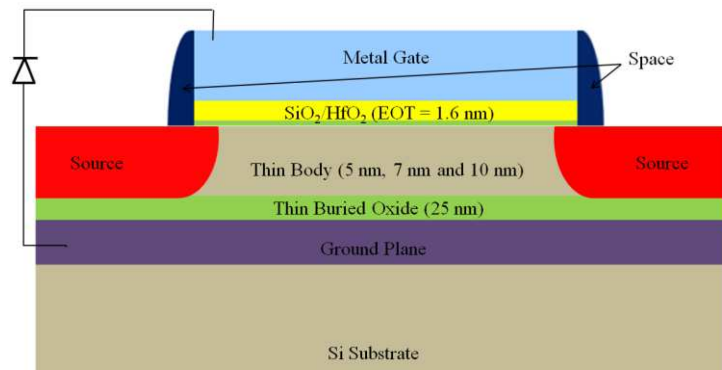

Fig. 1: Schéma d'un transistor ultra-mince FD SOI.

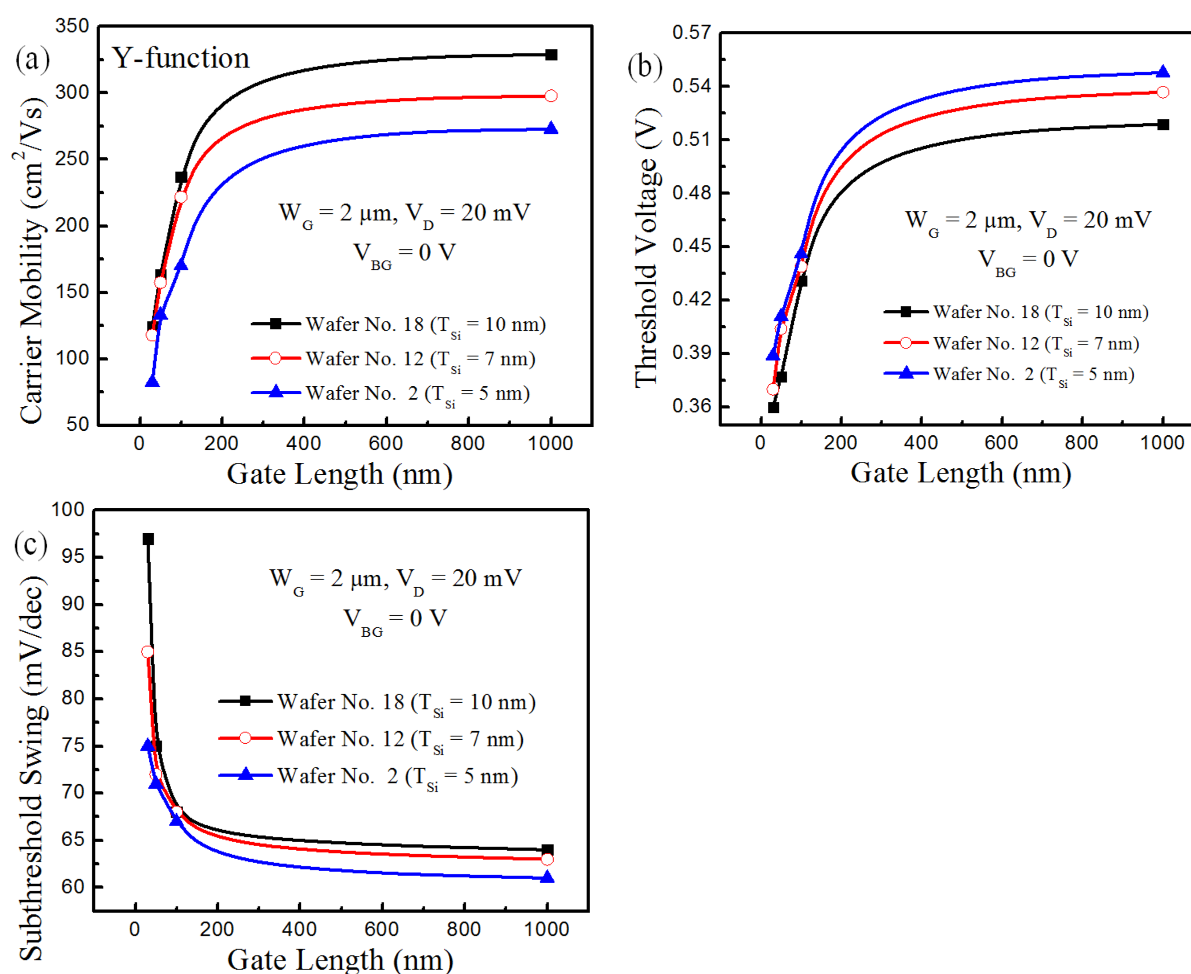

Fig. 2: Impact de l'épaisseur du film et de la longueur de grille sur les caractéristiques des transistors FD SOI. (a) Mobilité des électrons, (b) tension de seuil et (c) 'swing'. La mobilité et la tension de seuil ont été extraites par la méthode de la fonction Y.

La Figure 2 montre les effets conventionnels de canal court en fonction de l'épaisseur du film. La mobilité électronique décroit avec L_G en raison des défauts localisés induits lors de l'implantation de source et drain (Fig. 2a). Dans les transistors plus minces, la mobilité est

légèrement réduite par le confinement des phonons et les collisions sur les surfaces.

La tension de seuil et la pente en inversion faible (ou le ‘swing’) sont normalement dégradées dans les transistors courts en raison du partage de charge (Fig. 2b and 2c). En réduisant l’épaisseur, le confinement quantique se traduit par une plus forte énergie nécessaire pour atteindre la même charge d’inversion ; en d’autres termes, la tension de seuil augmente (Fig. 2b). Néanmoins, l’effet de canal court est atténué par la réduction de l’épaisseur des jonctions et de la région de désertion. Cette amélioration est clairement visible sur le ‘swing’ en Fig. 2c.

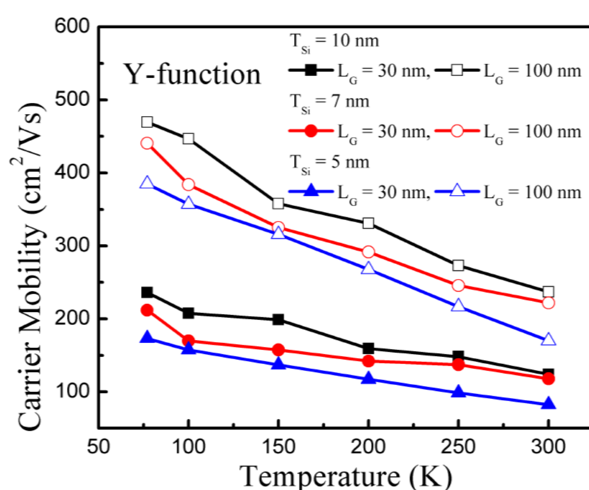

Fig. 3: Mobilité en fonction de la température pour différentes épaisseurs du transistor. $W_G = 2$ µm, $V_D = 20$ mV et $V_{BG} = 0$ V.

La Figure 3 montre la mobilité mesurée dans une large gamme de température (77 - 300 K). On note l’augmentation de la mobilité en basse température due à la réduction des collisions avec les phonons.

Un effet inédit est la variation du coefficient de couplage entre les deux canaux, défini comme $\alpha = -\Delta V_{THF}/\Delta V_{BG}$, avec la température (Fig. 4). A 77 K, le couplage est un peu plus fort dans les transistors plus minces où la capacité du film est plus élevée. En augmentant la température on observe une augmentation du couplage qui reflète sa dépendance aux effets de canal court. Les SCE sont plus fort à haute température et dans les dispositifs plus épais ce qui conduit à une amplification du couplage. Pour cette raison, l’effet de couplage dans les films très minces est relativement insensible à la température ce qui est intéressant pour la conception de circuits SOI à tension de seuil modulable par effet de grille arrière.

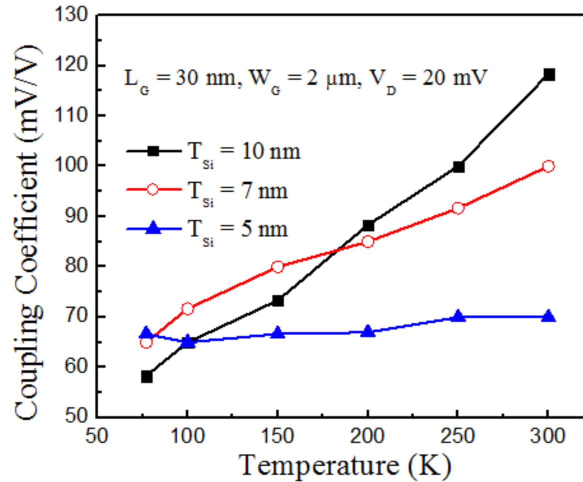

Fig. 4: Coefficient de couplage en fonction de la température pour différentes épaisseurs de transistors très courts.

2.2. Effets de couplage dans les FinFET à double-grille

Afin de réduire la consommation tout en améliorant la vitesse des circuits, il est important d'examiner la possibilité de moduler la tension de seuil également dans les FinFET. Les effets de couplage 3D ayant été déjà analysés dans les FinFET triple-grille, nous nous sommes penchés sur les transistors à double grille. Nos dispositifs, fabriqués à Sematech, ont T_{BOX} = 140 nm, EOT = 1.4 nm et un fin de hauteur H_F = 40 nm (Fig. 5). Au-dessus du fin, des couches épaisses de SiO_2 (5 nm) et de nitrure (10 nm) ont été déposées pour empêcher l'activation du canal supérieur. Les deux canaux latéraux sont contrôlés par la même tension de grille.

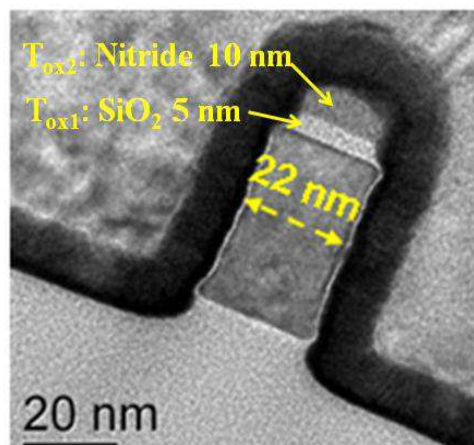

Fig. 5: Image TEM d'un FinFET double-grille (DG) sur SOI.

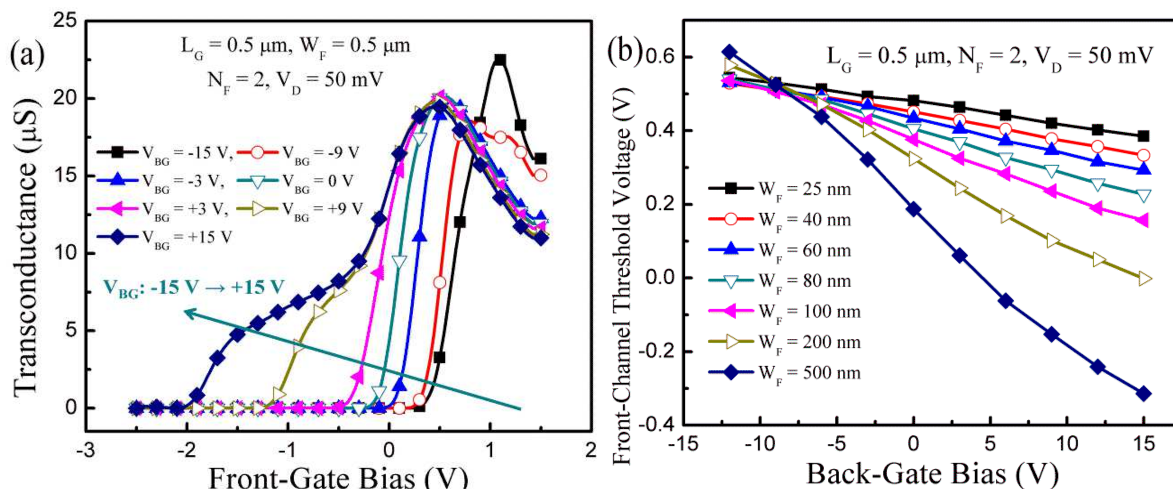

Fig. 6: Effets de couplage mesurés sur DG FinFETs. (a) Transconductance et (b) tension de seuil en fonction de la tension arrière pour différentes largeurs du fin (W_F).

Le couplage 'vertical' entre les canaux latéraux et la tension arrière (V_{BG}) a été étudié systématiquement. Lorsque l'interface fin-BOX change de l'accumulation vers l'inversion, le potentiel électrique dans le film augmente et la tension de seuil diminue (Fig. 6a). Le pic de la transconductance est déplacé vers la gauche. A forte tension arrière ($V_{BG} > +3$ V), un plateau devient visible sur la transconductance, indiquant l'activation prématurée du canal arrière. Par contre, à tension suffisamment négative ($V_{BG} < -12$ V), l'effet GIFBE (gate-induced floating body effect) se manifeste par une augmentation du pic.

La Figure 6b montre que la largeur du fin a une importance capitale sur l'effet du couplage. Le coefficient de couplage $\alpha = -\Delta V_{THF}/\Delta V_{BG}$ diminue considérablement dans les FinFETs étroits, où le couplage 'vertical' se trouve en compétition avec le couplage 'latéral'. En effet, les grilles latérales tentent également de contrôler le potentiel à l'interface fin-BOX, réduisant ainsi l'impact de la tension substrat jusqu'à l'éliminer. Dans ce cas extrême de fin très étroit (< 20 nm), la grille arrière ne peut plus moduler convenablement la tension de seuil du transistor. Un autre résultat intéressant, que nous avons expliqué par la même compétition 'latéral-vertical', est l'augmentation du couplage inversé ($\Delta V_{THB}/\Delta V_{FG}$) dans les fins étroits.

La comparaison entre FinFETs double et triple grille est montrée en Fig. 7. La grille supplémentaire au-dessus du fin s'oppose à la pénétration du champ vertical issu du substrat et renforce ainsi l'effet des grilles latérales. Le coefficient de couplage est nettement réduit, raison pour laquelle nous préconisons l'utilisation des FinFET double-grille dans les circuits à modulation par la tension de substrat.

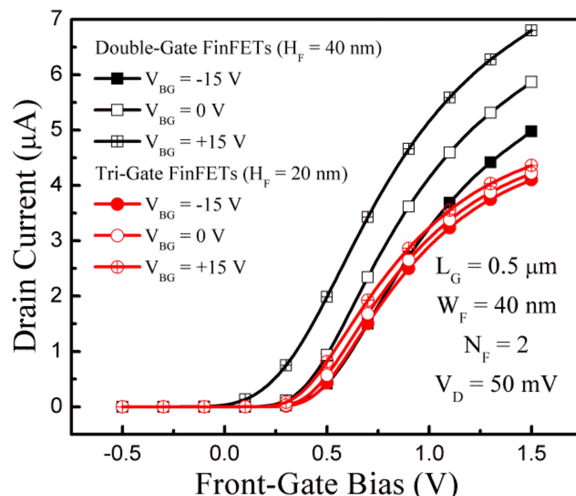

Fig. 7: Comparaison du couplage entre le courant de drain et la grille arrière dans des FinFET à double-grille et à triple-grille.

2.3. Etude de la mobilité dans les transistors TFT sur ZnO

Puisque les TFT fonctionnent comme le canal arrière des MOSFETs sur SOI, nous les avons étudiés, par notre méthodologie SOI, dans le cadre d'une coopération avec Air Force Laboratory (USA). Les TFT en ZnO présentent un grand intérêt, en particulier pour les écrans plats et les composants déformables. Notre mission était double : (i) trouver une méthode fiable pour la détermination de la mobilité et (ii) analyser les performances en basse température.

Les dispositifs ont été fabriqués sur des couches de ZnO nanocrystallin déposées par PLD (pulsed laser deposition) à 200°C [2.49]. La grille, située en face arrière, est séparée du film par 30 nm de SiO_2. La Figure 8 montre une image TEM du canal du transistor.

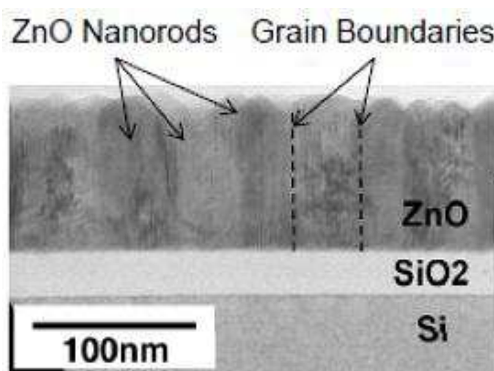

Fig. 8: Image TEM d'un TFT sur ZnO nanocrystallin.

Après une campagne de mesures, nous avons examiné et testé les modèles de mobilité proposés dans la littérature. Les méthodes basées sur l'ajustement des courbes via de multiples paramètres ajustables ont été déclassées au profit de modèles plus physiques. La méthode classique de la fonction Y s'avère inapplicable aux TFT car elle ne peut pas reproduire le fort écart entre les tensions de seuil et du pic de transconductance (~ 6-8 V à 77 K, voir Fig. 9c).

Deux modèles ont été retenus, le préféré étant celui de *Shur* pour des raisons de simplicité. Nous l'avons revisité en introduisant le facteur de dégradation de mobilité θ et en laissant libres les paramètres m et k :

$$\frac{1}{\mu_{eff}} = \left[\frac{1}{k(V_G - V_{TH})^m} + \frac{1}{\mu_0} \right] \left[1 + \theta (V_G - V_{TH}) \right]$$

Notre modèle prend en compte le transport conventionnel dans les couches d'inversion ainsi que l'effet variable (selon V_G) des joints de grains, résumé par m et k. La Figure 9a montre la parfaite superposition du modèle aux courbes mesurées pour m = 2.1, k = 1.5, θ = 0.0025, V_{TH} = 1.5 V and μ_0 = 95 cm^2/Vs.

Afin de déterminer expérimentalement ces paramètres, nous avons mis au point une méthode d'extraction originale. Les deux mécanismes principaux de transport sont séparés suivant la tension de grille. Dans une première étape, à faible V_G, la conduction est gouvernée par l'activation progressive des joints de grains (μ_0 et θ sont négligeables). La courbe mesurée $I_D/g_m(V_G)$ étant linéaire, on extrait le coefficient m de la pente et la tension de seuil de l'intersection avec l'axe horizontal. Le coefficient k est donné par le courant de drain mesuré à $V_G - V_{TH} = 1\ V$ (Fig. 9b).

Dans la seconde étape, à fort V_G, le transport est dominé par drift-diffusion. On peut alors utiliser la fonction Y pour déduire la mobilité μ_0 et le facteur θ :

$$\left[\left(-\frac{1}{I_D} \right)' \right]^{-0.5} = \frac{I_D}{\sqrt{g_m}} = Y = \sqrt{A\mu_0} (V_G - V_{TH})$$

Cette méthode est détaillée en section 2.3. Notre modèle est dorénavant utilisé pour l'optimisation des TFT.

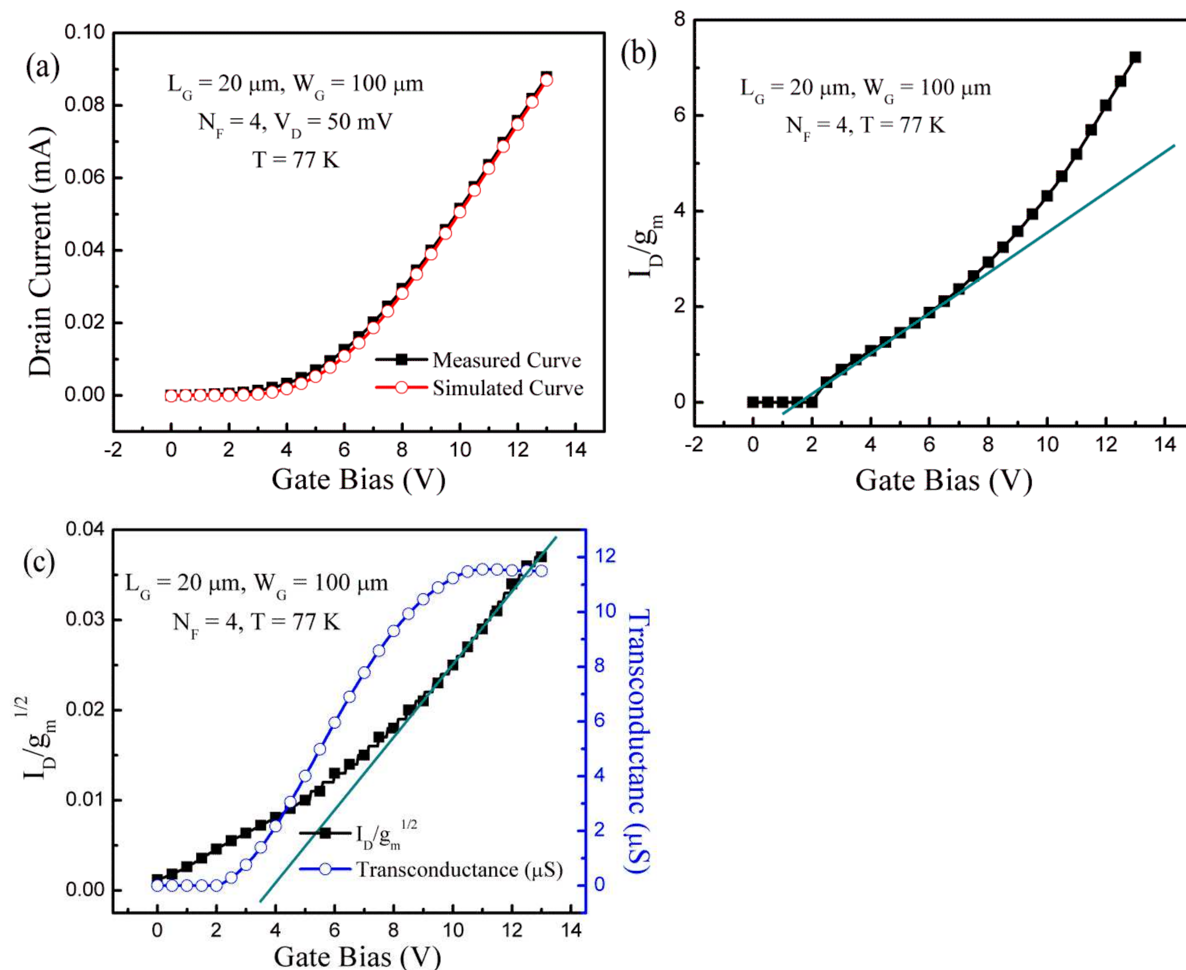

Fig. 9: (a) Courant de drain en fonction de la tension de grille (mesures et modèle). (b,c) Courbes $I_D/g_m(V_G)$ et $I_D/\sqrt{g_m}(V_G)$. Les lignes montrent l'extrapolation linéaire des paramètres.

Les mesures en basse température indiquent les variation de la tension de seuil, de la pente en inversion faible et de la mobilité μ_0 qui est fortement dépendante du taux de collisions avec les phonons.

Chapitre 3: Magnétorésistance géométrique et courbes inhabituelles de mobilité

Dans les transistors FD, la mobilité des porteurs est un paramètre complexe car plusieurs canaux, grilles et interfaces coexistent et interagissent. Afin de l'étudier en détail, nous avons choisi la plus précise et irréfutable méthode qui existe : la magnétorésistance géométrique. Rappelons que l'effet Hall et la magnétorésistance sont des mécanismes jumeaux. Lorsque le champ de Hall empêche la déflection Lorentzienne des porteurs, la

magnétorésistance est pratiquement négligeable. Par contre, si le champ de Hall est court-circuité, comme dans les MOSFETs courts et larges, la magnétorésistance (appelée géométrique) est maximale :

$$R_B = R_0(1 + \mu_{MR}^{\,2} B^2)$$

Cette relation est indépendante de toute approximation ou paramètre technologique (longueur et largeur effectives, épaisseurs du film et des diélectriques, etc) ce qui la rend inopposable. Il suffit de tracer la variation de la résistance en fonction du carré du champ magnétique B pour obtenir, de la pente, la mobilité μ_{MR} à différentes tensions de grille (Fig. 10b). Nous avons mesuré une variété de transistors FD-SOI planaires et des FinFET en utilisant les équipements du laboratoire LCMI du CNRS à Grenoble.

La Figure 10 montre les caractéristiques typiques d'un transistor FD SOI dans la gamme 0–11 T. La tension de seuil V_{THF} et la pente en inversion faible sont peu affectées par le champ magnétique B, alors que la transconductance et le courant diminuent notablement. Le coefficient de dégradation de mobilité θ décroit également avec B (insertion Fig. 10a).

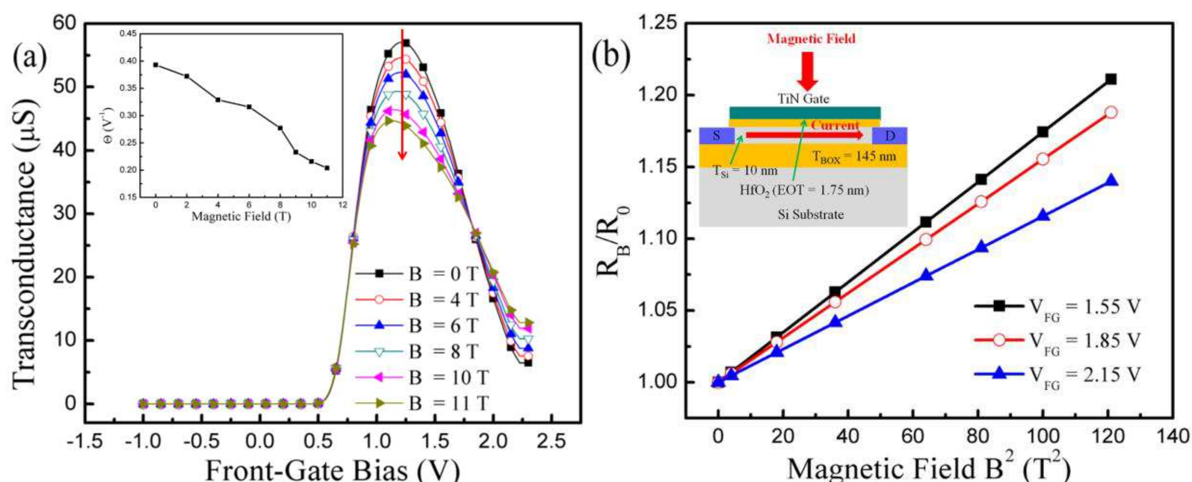

Fig. 10: Caractéristiques typiques d'un MOSFET SOI sous champ magnétique intense. (a) Transconductance en fonction de la tension de grille (l'insertion montre la variation du facteur θ). (b) R_B/R_0 en fonction du carré du champ. Transistor FD SOI (image) avec L_G = 1 µm, W_G = 10 µm, V_D = 10 mV, V_{BG} = 0 V, T = 100 K.

Nous avons ainsi démontré que les mobilités des canaux avant et arrière étaient élevées malgré la faible épaisseur du film SOI. Nous nous sommes concentrés sur l'impact du couplage de ces deux canaux. Pour cela, nous avons tracé la mobilité en fonction du champ électrique effectif, calculé à partir des tensions appliquées sur les deux grilles. La Figure 11 est

remarquable dans le sens qu'elle infirme le concept de *mobilité universelle*. On observe une double branche qui s'explique par le déplacement du profil des porteurs de l'interface arrière vers l'interface avant. Par exemple, pour $|E_{eff}| \approx 0.3$ MV/cm, deux valeurs distinctes de mobilité sont mesurées. Au début de la courbe, la mobilité dans le canal arrière augmente avec V_G car le champ électrique vertical diminue (moins de collisions sur la surface). Dès qu'une valeur maximum est atteinte, le canal avant s'ouvre et prend le contrôle du transistor. La mobilité retrouve une décroissance plus conventionnelle avec le champ électrique. Des mesures supplémentaires et des explications détaillées sont fournies en section 3.3.

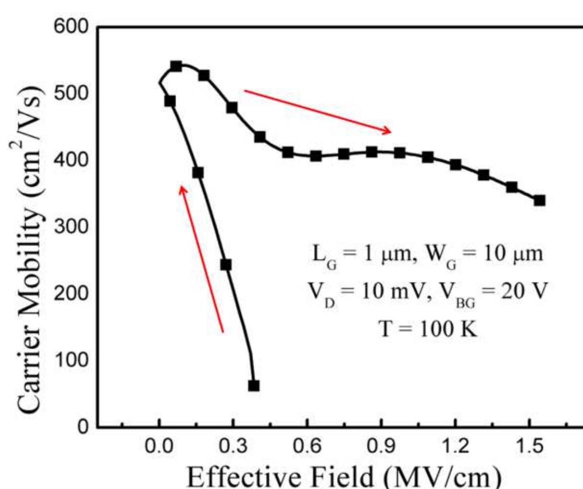

Fig. 11: Mobilité en fonction du champ électrique effectif. La grille arrière est polarisée en inversion (V_{BG} = +20V) et le canal avant s'ouvre graduellement.

Pour la première fois, nous avons mesuré la mobilité, via la magnétorésistance géométrique, dans les FinFET. L'influence du champ magnétique sur les canaux verticaux et horizontaux est différente, néanmoins la mobilité a pu être déterminée. Nous avons comparé la mobilité dans les divers canaux et montré des multiples courbes non-universelles.

Le cas le plus intriguant est celui des FinFET double-grille. Comme la largeur du canal (épaisseur du film) est inférieure à la longueur de grille, on s'atteindrait à une magnétorésistance géométrique négligeable car le champ magnétique est toujours perpendiculaire à la plaquette, donc parallèle au plan du courant. Cette hypothèse, très raisonnable et confirmée sur des transistors planaires, a été niée par les mesures. On obtient en effet une mobilité respectable dans les canaux latéraux (Fig. 12). Pour confirmer la validité de ces résultats, nous les avons comparés aux courbes de mobilité effective (μ_{eff}) et de mobilité effet de champ (μ_{FE}) déduites des caractéristiques mesurées en l'absence du champ

magnétique. Nous avons également corrigé la méthode de la magnétorésistance en incluant l'effet de la résistance série dans les canaux courts. Les diverses courbes sont présentées en Fig. 12a. Les variations sont parallèles ce qui confirme chacune des méthodes. La différence entre les mobilités μ_{MR} et μ_{eff} est parfaitement normale et représente la signature des mécanismes de collisions dominants (dans notre cas, collisions de type Coulombien).

L'évaluation de la mobilité dans des FinFETs à largeur variable a conduit aux résultats présentés en Fig. 12b. On note une certaine dégradation de la mobilité dans les fins étroits, liée à l'augmentation des collisions sur les défauts des flancs latéraux.

Mais pourquoi peut-on mesurer une magnétorésistance géométrique alors que les conditions 'géométriques' ($L \ll W = H_F$) ne sont apparemment pas remplies ? Nous pensons qu'il s'agit d'un pur effet double grille. La force de Lorentz tend à dévier les porteurs perpendiculairement aux flancs, d'une grille vers la grille opposée. Le champ de Hall, qui devrait s'opposer à cette déflection et annuler la magnétorésistance, ne peut pas s'établir entre les deux flancs ; leurs potentiels sont en effet identiques car la même tension est appliquée sur les deux grilles latérales. Le court-circuit de l'effet Hall, à l'origine de la magnétorésistance géométrique, n'est plus assuré par la géométrie du transistor mais par sa configuration DG FinFET.

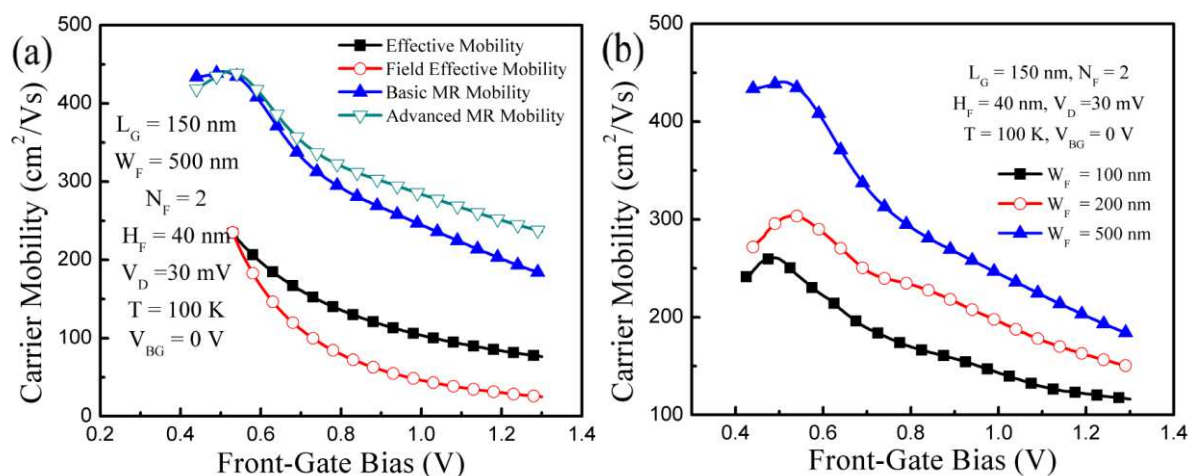

Fig. 12: Mobilité résultant des mesures de magnétorésistance dans des FinFET à double grille. (a) Mobilité en fonction de la tension de grille, extraite par différentes méthodes. (b) Courbes de mobilité MR montrant l'impact de la largeur du fin.

En conclusion, nous avons démontré la faisabilité et l'intérêt des mesures de magnétorésistance géométrique sur des films nanométriques et surtout sur des transistors 3D tels que les FinFET. Nos résultats ouvrent la porte vers d'études plus approfondies sur

l'identification des mécanismes de collision et sur la discrimination de la mobilité dans les différents canaux qui coopèrent au transport de charge.

Chapitre 4: Nouvelle mémoire non-volatile sur ONO FinFETs

Dans ce chapitre, nous étudions des dispositifs FinFETs fabriqués sur couche ONO enterrée pour une application mémoire flash innovante où les charges sont piégées dans la couche de nitrure enterré et détectées/lues à l'interface opposée par effet de couplage. Grâce à cette configuration spécifique, l'épaisseur d'oxyde tunnel arrière peut rester suffisamment épaisse pour conserver de bonnes performances en terme de rétention, alors que celle de l'oxyde avant (où l'état de la mémoire est lu) peut suivre les critères de miniaturisation des dispositifs à l'état de l'art. De plus, la séparation des deux interfaces améliore la fiabilité de la mémoire et réduit les problèmes de perturbation de charge survenant lors du cyclage en programmation.

Des plaques SOI avec un empilement $SiO_2/Si_3N_4/SiO_2$ ont été utilisées comme matériau de départ. Cet isolant multicouche est composé de SiO_2 (2,5 nm), Si_3N_4 (20 nm) et SiO_2 (70 nm). La couche mince supérieure de SiO_2 (2,5 nm) permet le transport par effet tunnel. L'épaisseur du film de silicium est de 65 nm et le TiSiN déposé par LPCVD a été utilisé comme matériau pour la grille.

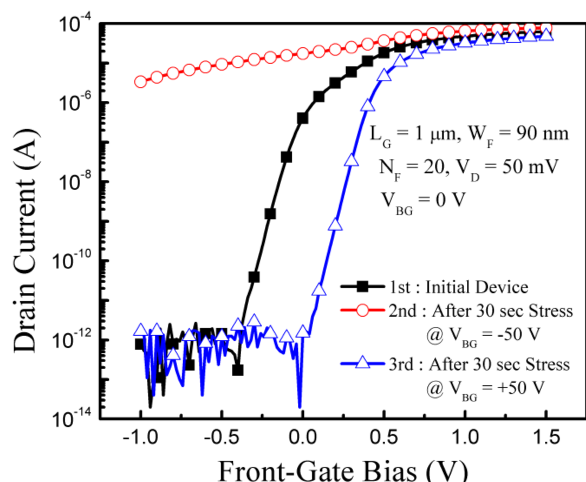

Fig. 13: Effets typiques mémoire induits par polarisation de grille arrière. (a) Courant de drain en fonction de la tension de grille avant, mesuré à $V_{FG} = V_{BG} = 0$ V après programmation à $V_{BG} = \pm 50$ V. La grille avant, le drain et la source sont mis à la masse pendant le stress.

Les charges peuvent être injectées et piégées dans le nitrure notamment en appliquant une tension sur la grille arrière V_{GB} (Fig. 13) ou sur le drain (Fig. 14). Lorsque la méthode de programmation par tension de grille arrière est utilisée, le mécanisme d'injection est de type Fowler-Nordheim (FN). Les charges piégées peuvent modifier les caractéristiques du canal face avant par couplage. Le changement d'état (haut et bas) résultant du piégeage/dépiégeage de charge est mesuré à $V_{BG} = 0$ V.

Lorsque la mémoire est programmée à l'aide d'un tension appliquée sur le drain ($|V_D| > 2$ V), les charges sont injectées/extraites dans/de l'ONO enterré à proximité de ce même terminal grâce à l'efficacité du champ électrique vertical. La Figure 14 illustre les courbes $I_D(V_{FG})$ résultant de polarités opposées appliquées au drain combinées avec deux configurations de lecture. Des charges positives et négatives sont injectées en appliquant respectivement 2.5 V et -2.5 V au drain. Si les terminaux source et drain sont échangés au cours de la lecture, une opération non volatile "multi-bit" peut être réalisée. Les termes "direct" ou "inverse" sont utilisés quand une polarisation de lecture positive (50 mV) est appliquée aux contacts de source ou drain respectivement. Notons que la charge non volatile reste injectée à la même borne (au drain) quelque soit le mode de lecture. En mode direct, l'effet des charges injectées situées près du drain a un plus fort impact sur le pincement de canal qu'en mode inverse. Par conséquent, l'exploitation de ce phénomène permet de rendre réalisable une opération sur quatre configurations des charges injectées en inversant les polarités aux bornes de lecture et en utilisant la source et/ou le drain pour injecter les charges.

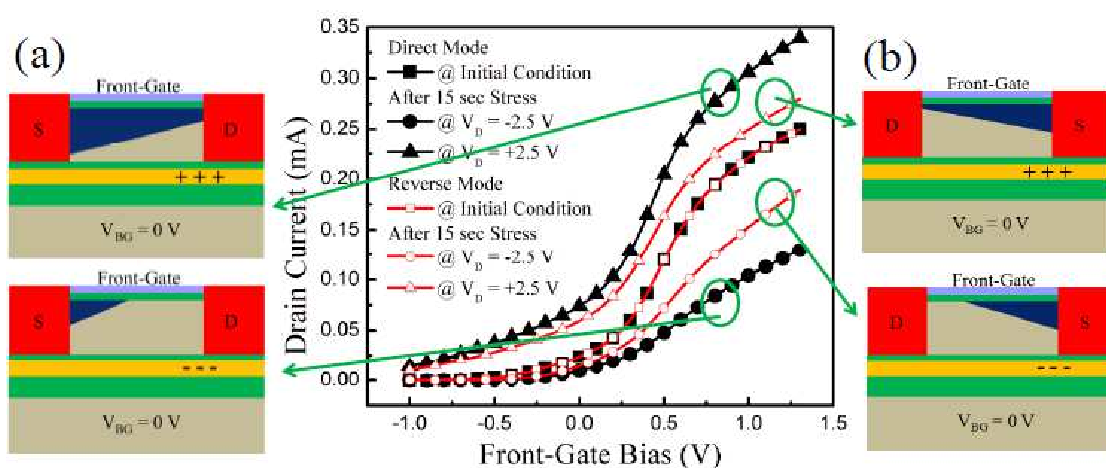

Fig. 14: Effet mémoire par polarisation de drain. Le courant de drain est mesuré en mode direct et inverse, en fonction de la tension de grille à $V_{BG} = 0$ V, avant et après 15 secondes de stress à $V_D = \pm 2{,}5$ V. Lors du stress, grille avant, source et drain ont été mis à la masse. (b) Le mode inversé (drain-source) a été mesuré après (a) le mode direct (source-drain). $L_G = 100$ nm, $W_F = 90$ nm, $N_F = 16$, $V_{BG} = 0$ V, $V_D = 50$ mV.

La Figure 15a met en évidence l'effet de la longueur de grille sur la marge de courant non volatile après programmation. Nous avons montré que l'effet mémoire pour des dispositifs plus courts (avec une largeur de fin raisonnable, > 10–15 nm) est amplifié grâce au champ électrique longitudinal généré par la polarisation de drain. Cette amplification est attribuée à un effet plus connu sous le nom de "fringing fields". Ce résultat apporte un éclairage nouveau pour une voie future de l'amélioration des performances mémoire lorsqu'une miniaturisation encore plus poussée sera envisagée. La Figure 15b illustre le temps de rétention obtenu en utilisant la programmation par polarisation de drain. Alors que les dispositifs de test n'ont pas été spécifiquement optimisés, la rétention obtenue est compétitive et appropriée pour une application mémoire flash.

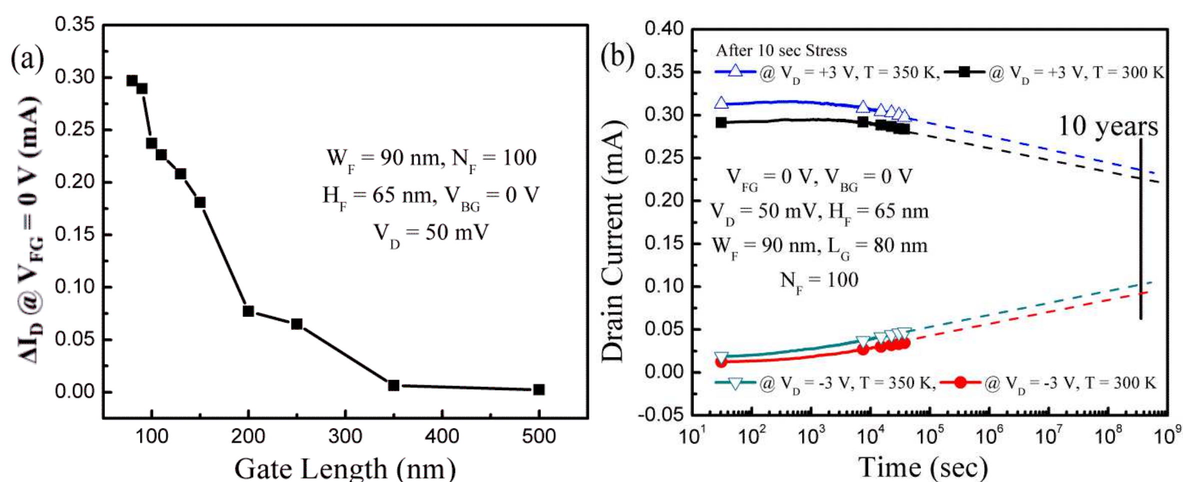

Fig. 15: (a) Marge de détection, définie comme étant la différence des niveaux de courant à $V_{FG} = V_{BG} = 0$ V avant et après stress, en fonction de la longueur de grille. (b) Caractéristique de rétention liée à la décharge des pièges de la couche de nitrure. Courant de drain en fonction du temps à T = 300 K et T = 350 K, montrant la marge de détection et le temps de rétention après 10 sec de stress à V_D = +3 V.

En plus de la démonstration de la faisabilité d'opérations double-bit effectuée grâce à l'injection localisée de porteurs, cette mémoire fournit une fiabilité améliorée par le biais de la séparation de l'interface de programmation et de l'interface de détection/lecture.

Chapitre 5: Mémoire Multi-Bit Unifiée à ONO FinFETs

Les dispositifs FinFETs sur ONO ont été évalués en tant que mémoire DRAM à seul transistor (1T-DRAM). L'étude de la coexistence des opérations volatile et non volatile au sein de la même cellule a démontré que le concept de mémoire unifiée (URAM) pouvait être

également une option à forte potentialité. Nos résultats expérimentaux ont révélé aussi la faisabilité d'une mémoire volatile multi-bit.

Un concept original de mémoire unifiée volatile et multi-bit avec une architecture FinFET sur couche ONO enterré est présenté (Fig. 16). Les charges non volatiles sont stockées de façon uniforme par injection Fowler-Nordheim (par polarisation de grille arrière), ou par injection de porteurs localisée (polarisation de drain). La variation de charge non volatile est détectée à l'interface avant par couplage capacitif (Fig. 16a). Pour le fonctionnement de la mémoire volatile 1T-DRAM, les charges (trous générés par ionisation par impact) sont stockées dans le corps du FinFET (en particulier à l'interface avant) et détectées par le canal d'inversion en face arrière (Fig. 16b).

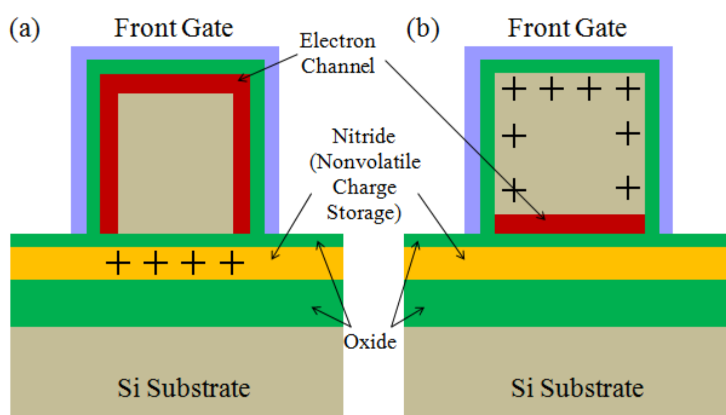

Fig. 16: Nouveau concept de mémoire unifiée avec FinFET fabriqués sur isolant ONO enterré. (a) Les charges non volatiles sont stockées dans la couche de nitrure et détectées au canal avant ; (b) les charges volatiles sont stockées à l'interface avant et détectées au canal arrière.

La Figure 17 résume la séquence de programmation/lecture de la 1T- DRAM multi-bit. L'état '1' (niveau de courant haut) et l'état '0' (faible niveau de courant) sont programmés respectivement par ionisation par impact (V_{BG} = +8 V et V_D = 1.5 V) et en polarisant la jonction body-drain en direct (V_D = -0.5 V et V_{FG} =+0.8 V) (Fig. 17a). Les niveaux de courant transitoire en mode 1T–DRAM pour différentes polarités de charge non-volatile — positive, négative et native (ONO non chargé) — sont comparés à la Figure 17b. Les niveaux obtenus sont suffisamment distincts pour une identification aisée de la charge ONO (positive ou négative) et des niveaux '0' ou '1' de la 1T-DRAM. Selon le type de charges piégées et leur quantité (modulée par le stress de grille arrière), plus de deux niveaux de courant peuvent être atteints avec une marge de détection suffisante pour une application mémoire multi-bits (30–45 µA/µm).

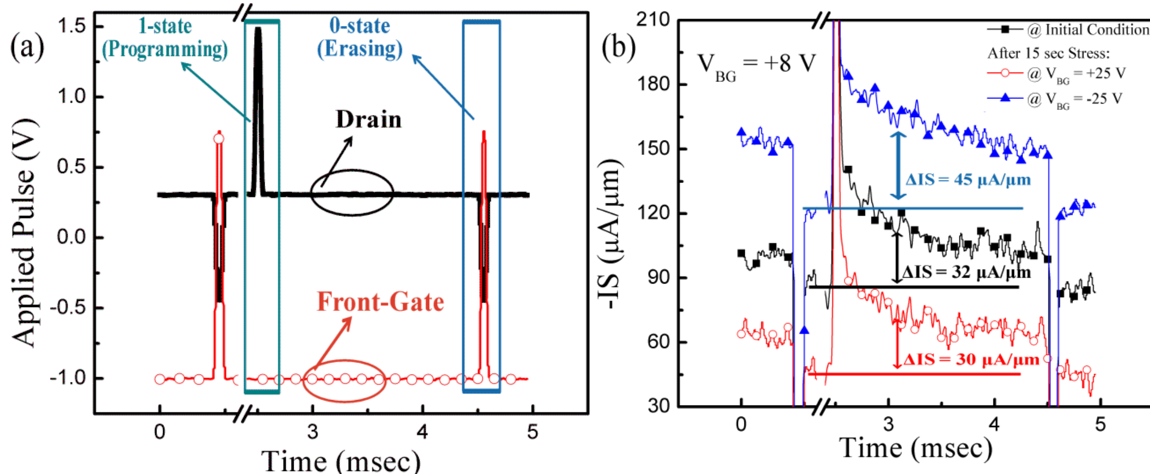

Fig. 17: (a) Impulsions appliquées au drain et à la grille avant. (b) Courant transitoire de la 1T-DRAM avant et après charge du ONO. Les niveaux de courant distincts obtenus confirment la capacité de l'application multi-bits. La marge de détection ΔIS est définie comme la différence de courant entre les états '0' et '1' après 0.5 ms de lecture. L_G = 100 nm, W_F = 90 nm.

L'impact des paramètres géométriques du FinFET sur la marge de détection est résumé à la Figure 18. Dans les dispositifs à canaux courts, puisque le taux d'ionisation par impact et le niveau de courant sont plus élevés, la marge de détection est améliorée (Fig. 18a). Dans les dispositifs très étroits, le volume de stockage est réduit. De plus, l'effet de la variation dynamique du potentiel (liée à l'excès en trous) est partiellement masqué par le champ électrique latéral accru. Par conséquent, l'effet mémoire est détérioré (Fig. 18b).

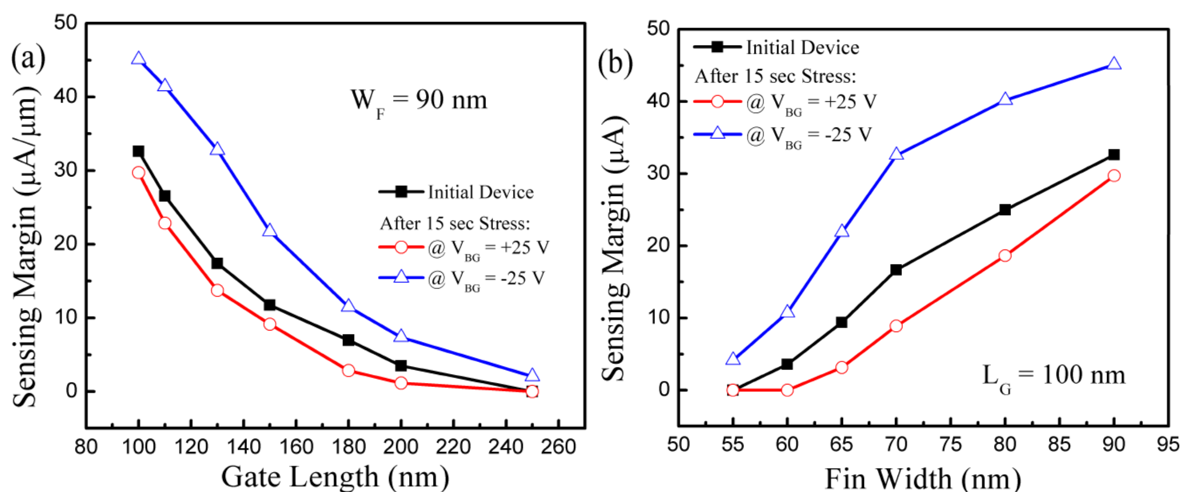

Fig. 18: Impact de (a) la longueur et (b) largeur de grille sur la marge de détection 1T-DRAM définie comme en Figure 17.

L'opération en mode 1T-DRAM a été étudiée afin d'évaluer la viabilité de la combinaison des modes mémoire volatile et non volatile dans les dispositifs FinFETs

fabriqués sur ONO enterré. Une amélioration de la marge de détection des dispositifs à canaux courts a été mise en évidence. Finalement, le fonctionnement en mémoire unifiée multi-bits a pu être réalisé sans perturbation des charges piégées dans le ONO.

Conclusion

Ce travail présente les principaux résultats obtenus avec une large gamme de dispositifs SOI avancés, candidats très prometteurs pour les futurs générations de transistors MOSFETs. Leurs propriétés électriques ont été analysées par des mesures systématiques, agrémentées par des modèles analytiques et/ou des simulations numériques. Nous avons également proposé une utilisation originale de dispositifs FinFETs fabriqués sur ONO enterré en fonctionnalisant le ONO à des fins d'application mémoire non volatile, volatile et unifiées.

Après une introduction sur l'état de l'art des dispositifs avancés en technologie SOI, le deuxième chapitre a été consacré à la caractérisation détaillée des propriétés de dispositifs SOI planaires ultra- mince (épaisseur en dessous de 7 nm) et multi-grille. Nous avons montré l'excellent contrôle électrostatique par la grille dans les transistors très courts ainsi que des effets intéressants de transport et de couplage.

Une approche similaire a été utilisée pour étudier et comparer des dispositifs FinFETs à double grille et triple grille. Nous avons démontré que la configuration FinFET double grille améliore le couplage avec la grille arrière, phénomène important pour des applications à tension de seuil multiple. Nous avons proposé des modèles originaux expliquant l'effet de couplage 3D et le comportement de la mobilité dans des TFTs nanocristallin ZnO. Nos résultats ont souligné les similitudes et les différences entre les transistors SOI et à base de ZnO. Des mesures à basse température et de nouvelles méthodes d'extraction ont permis d'établir que la mobilité dans le ZnO et la qualité de l'interface ZnO/SiO_2 sont remarquables. Cet état de fait ouvre des perspectives intéressantes pour l'utilisation de ce type de matériaux aux applications innovantes de l'électronique flexible.

Dans le troisième chapitre, nous nous sommes concentrés sur le comportement de la mobilité dans les dispositifs SOI planaires et FinFET en effectuant des mesures de magnétorésistance à basse température. Nous avons mis en évidence expérimentalement un comportement de mobilité inhabituel (multi-branche) obtenu lorsque deux ou plusieurs canaux coexistent et interagissent. Un autre résultat original concerne l'existence et

l'interprétation de la magnétorésistance géométrique dans les FinFETs.

L'utilisation de FinFETs fabriqués sur ONO enterré en tant que mémoire non volatile flash a été proposée dans le quatrième chapitre. Deux mécanismes d'injection de charge ont été étudiés systématiquement. En plus de la démonstration de la pertinence de ce type mémoire en termes de performances (rétention, marge de détection), nous avons mis en évidence un comportement inattendu : l'amélioration de la marge de détection pour des dispositifs à canaux courts. Notre concept innovant de FinFlash sur ONO enterré présente plusieurs avantages: (i) opération double-bit et (ii) séparation de la grille de stockage et de l'interface de lecture augmentant la fiabilité et autorisant une miniaturisation plus poussée que des Finflash conventionnels avec grille ONO.

Dans le dernier chapitre, nous avons exploré le concept de mémoire unifiée, en combinant les opérations non volatiles et 1T-DRAM par le biais des FinFETs sur ONO enterré. Comme escompté pour les mémoires dites unifiées, le courant transitoire en mode 1T-DRAM dépend des charges non volatiles stockées dans le ONO. D'autre part, nous avons montré que les charges piégées dans le nitrure ne sont pas perturbées par les opérations de programmation et lecture de la 1T-DRAM. Les performances de cette mémoire unifiée multi-bits sont prometteuses et pourront être considérablement améliorées par optimisation technologique de ce dispositif.

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This thesis is dedicated to my family and my wife.