Comparison of De-embedding Methods for Long Millimeter and Sub-Millimeter-Wave Integrated Circuits

Vipin Velayudhan, Emmanuel Pistono, Jean-Daniel Arnould

Comparison of De-embedding Methods for Long Millimeter and Sub-Millimeter-Wave Integrated Circuits

Vipin VELAYUDHAN, Emmanuel PISTONO and Jean-Daniel ARNOULD

IMEP-LAHC Institut de Microélectronique, Electromagnétisme et Photonique Laboratoire d'Hyperfréquences et de Caractérisation
Grenoble Institute of Technology – Grenoble INP, Minatec : 3, rue Parvis Louis Néel, CS 50257, 38016 Grenoble, France

Vipin.Velayudhan@minatec.grenoble-inp.fr

Abstract— **This paper compares several de-embedding methods over millimeter and sub-millimeter wave frequencies in integrated technology. These methods are compared for S-CPW transmission lines considered as device under test. From these comparisons we propose an effective way to de-embed transmission lines. A method called “Half-Thru de-embedding method” is especially discussed. The SCPW transmission line model and results are obtained from Ansys HFSS Simulations in BiCMOS 55-nm integrated technology.**

Index Terms— **De-embedding methods, characterization, millimeter wave, sub-millimeter wave , integrated circuits, SCPW transmission lines.**

I- Introduction

Nowadays, measurement and characterization of devices in millimeter and sub-millimeter wave frequency range is always a challenge. The applications of millimeter and sub-millimeter wave frequency circuits (Video-streaming 57-66 GHz, 76-81 GHz automotive radar, medical imaging 140 GHz ...) are among the main research area in communications domain. Since considering the high frequency and thus the small size of the devices, efficient de-embedding methods must be considered to obtain accurate measurement results.

The general measurement system for on-wafer device under test (DUT) is shown in Figure 1. The DUT is connected to the PADs with on-wafer interconnects. To eliminate the effects of the external interconnects (coaxial cables or waveguides) and probes, a VNA calibration is considered. Then we need to move the measurement reference plane close to DUT by de-embedding pads and on-wafer interconnects to remove their effects.

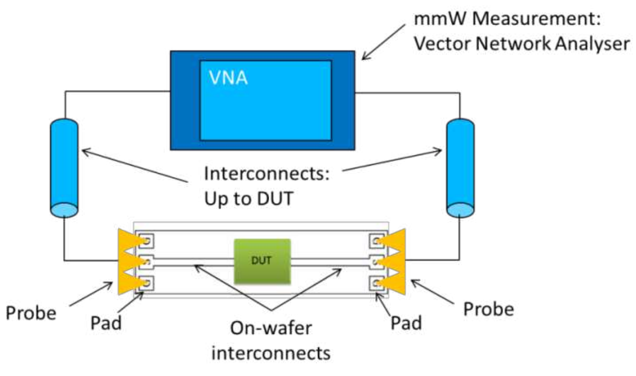

Figure 1. *Measurement setup of a device under test*

De-embedding methods [1-8] induce modifications of the design of passive and active circuits in the millimeter and sub-millimeter frequencies. Today, no solution provides a reliable and reproducible measurement of circuits in the silicon integrated technology for sub-millimeter wave frequencies, beyond the 100 GHz. Indeed beyond this frequency, environmental measure around the DUT is very critical and the effects of the pads and the substrate are no longer simple localized parasitic elements de-embedded. The de-embedding methods can be classified [1] into three types according to the size of the DUT and range of the frequency:

1. Lumped equivalent circuit model
2. Cascaded Matrix Based
3. Mixed models - matrix + lumped model

Lumped equivalent circuit methods [1, 2] are used to de-embed small feeding lines lengths (as compared to considered wavelengths) and remain effective to de-embed the devices at low frequency since transmission lines are considered as lumped models. Thus, these methods are no more valid at high frequencies since feeding lines can be longer than λ/10. In the lumped circuit equivalent method the parasitic effects of the pads and interconnects are modeled as lumped elements as exhibited for example in [1]-[3] and shown in the Figure 2.

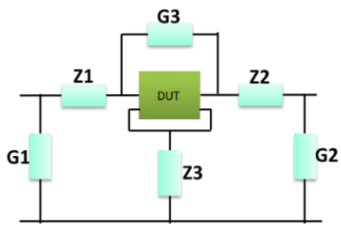

Figure 2. *Lumped equivalent Circuit Model*

Cascaded equivalent model is more accurate since feeding lines are considered as transmission lines. In the cascaded matrix based methods [3-5], the whole test structure is taken as cascaded network, as shown in Figure 3, which is more suitable for higher frequencies.

Figure 3. *Cascaded Matrix representation*

Mixed methods [4-6] considered a combination of both cascaded matrices and lumped equivalent model circuits, shown in the Figure 4. These methods are used to accurately de-embed both the feeding transmission lines and couplings between input/output DUT devices.

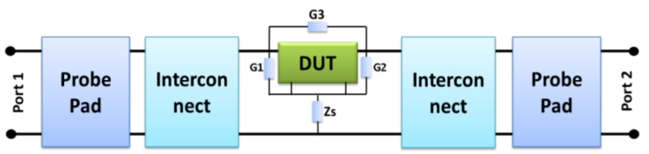

Figure 4. *Mixed model - matrix + lumped circuit model*

All these methods have been investigated for frequencies up to 65 or 170 GHz but not more. In our study, we will compare the efficiency of these methods with the “Half-thru de-embedding method” up to 250 GHz. After having explained briefly the Half-thru de-embedding method, comparison results will be done by considering fullwave electromagnetic simulations with Ansoft HFSS.

II- HALF-THRU DE-EMBEDDING METHOD

Half-thru de-embedding method is a method based on matrix calculation without any electrical model. The model of measured DUT to perform the half-thru de-embedding is shown in Figure 5.

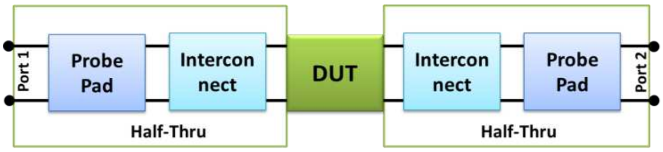

Figure 5. *Half-thru De-embedding method*

In this method the pad- interconnects parasitics are modeled as half-thru sections. The aim of this method is to well take the parasitic effects of the half-thru (pad and on-wafer feeding interconnect) of the DUT into account. The goal is to eliminate the effects of the access lines and contact pads from the measured circuit. Three de-embedding test fixtures must be considered to obtain our de-embedding as shown in Figure 6. In our case, DUT is a long S-CPW transmission line [7].

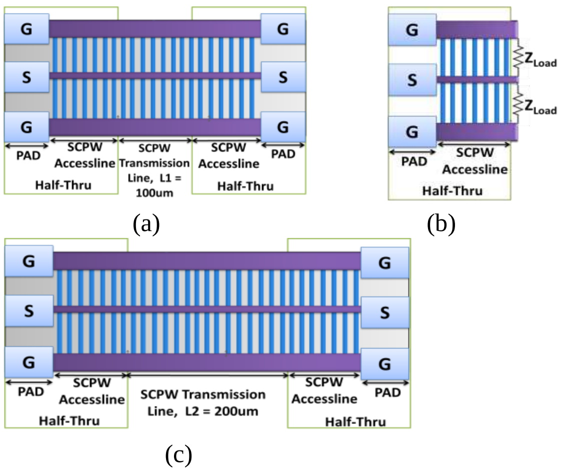

Figure 6. *Test fixtures circuits: (a) TL1, (b) feeding line+Load (c) TL2 = 2.TL1*

In order to obtain the real parasitic effects induced by each half-thru from both sides of the DUT, this method must consider first two test fixtures called TL_1 and TL_2 (double length compared to TL_1) to obtain the thru S-parameters and the reflection coefficient Γ of a half-thru loaded by a known load Z_L of 100 Ω, to derive the equivalent model of the demi-thru (pad and access line) of the DUT.

II-1- Theoretical analysis

In order to obtain the real parasitic effects induced by each half-thru from both sides of the DUT, this method must consider first two test fixtures called TL_1 and TL_2. Each of these test fixtures TL_1 and TL_2 consists of the on-wafer pads with a transmission line of same transversal physical dimensions that the on-wafer feeding interconnects (same characteristic impedance Zc, propagation constant γ) and a physical length L_1 or L_2, where L_2= 2. L_1. The equivalent model of a thru can be derived from the ABCD Matrix of TL_1 and TL_2 by converting the [S] matrices of TL_1 and TL_2 into [ABCD] matrices [11]. This procedure is illustrated in the following

$$\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix}_{\mathbf{Thru}} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix}_{\mathbf{L1}} \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix}_{\mathbf{L2}}^{-1} \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix}_{\mathbf{L1}} \quad (1)$$

Then, to derive the equivalent model of the half-thru (pad + access line) of the DUT, it is necessary to measure the reflection coefficient Γ of a half-thru loaded by a known load Z_L of 100Ω. From the Signal flow graph theory (Masons Rule) [11], we can extract the effects of Pad and access line from the thru and load.

$$S_{22} = \frac{S_{11L} - S_{21T}.\Gamma - S_{11T}}{S_{11L}.\Gamma - S_{11T}.\Gamma - S_{21T}} \quad (2)$$
$$S_{21} = S_{12} = \sqrt{S_{21T}.(1 - S_{22}^2)} \quad (3)$$
$$S_{11} = S_{11T} - S_{21T}.S_{22} \quad (4)$$

S_{11L} is the reflection coefficient of the Load through the feeding line (Figure 6.b). S_{11T}=S_{22T} and S_{21T}=S_{12T} is the S-parameters of the THRU derived from (1).

II-2- Extraction of Load value

The most challenging part of the Half-Thru de-embedding is the extraction of the load value in the load de-embedding test structure. For extracting the load value, we must de-embed the load test fixture. For de-embedding the load value we can use different de-embedding methods such as Open, Open-Short, thru de-embedding [1] which all promises good de-embedding, since the parasitics effects are considered as a small PAD. The de-embedding structures for open-short de-embedding for extracting the load value is shown in Figure 7.

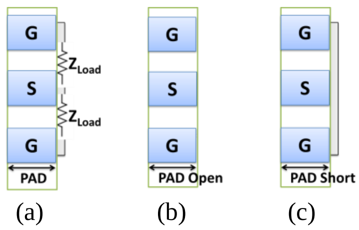

Figure 7. *Test fixtures for Load value extraction: (a) Load as DUT, (b) Open (c) Short*

The S –Parameters of the de-embedding structures are converted into Y parameters in order to obtain the Z_{LOAD} as

$$Z_{LOAD} = (Y_{DUT} - Y_{OPEN})^{-1} - (Y_{SHORT} - Y_{OPEN})^{-1} \quad (5)$$

III- SIMULATION RESULTS AND DISCUSSION

The half-thru de-embedding and the comparisons of other de-embedding methods are performed for a 400-um SCPW-transmission-line length by using Ansys HFSS. The back-end-of-line of the 55-nm BiCMOS integrated technology. Slow-wave coplanar waveguides [9],[10] are based on conventional coplanar CPW transmission lines with a patterned floating shield, including floating metallic strips under the line, as shown in Figure 8.

The dimensions of the coplanar strips are given by: a signal width of the SCPW W= 4 µm, a ground width W_g = 12 µm and a gap between the signal and ground G=40µm. The fingers have strip width of SL=0.16 µm and are separated by a distance of SS=0.2 µm. The characteristic impedance of the line is about 70Ω.

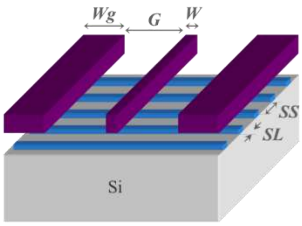

Figure 8. *SCPW Transmission line.*

The measurement set up of the device is shown in the Figure 9. The SCPW DUT is connected with pad and transmission line interconnects.

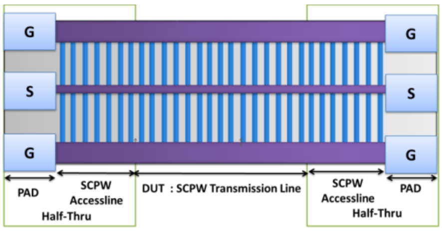

Figure 9. *Measurement setup of Half-Thru De-embedding*

The de-embedded results for SCPW transmission line are plotted in Figure 10, to Figure 12 by comparing the "half-thru method" with other existing methods (Vandamme [2], Mangan [4], L2L Methods [3,6], Thru only de-embedding method [5]) and TRL [7]. The red curve correspond to simulations of the DUT without any access lines and PADs in order to know the true parameters of this DUT. The S-Parameters and the characteristic impedance of the SCPW transmission line are calculated. Since the pads and interconnects are not approximated with lumped circuit elements, half-thru de-embedding is more efficient than other ones.

From the S-parameter de-embedded results (Figure 10 to Figure 12), the half-thru de-embedding method allows to obtain better results than other de-embedding methods especially concerning the characteristic impedance which is dropping off when the frequency increases. Concerning the three step method of Vandamme, the limitations appear at very low frequencies, due to lumped circuit modelling. In Mangan method the pad is assumed as a parallel admittance inducing too bad results above 100 GHz. In the cascaded matrix-based method [3-5], no approximation of pads and interconnects is done, but the method is good for only symmetrical pad structures and even if symmetrical PADs are considered herein, poor results are obtained above 100 GHz especially concerning the characteristic impedance because of the discontinuity between pads and access lines. TRL calibration technique [7] de-embedding promises good results over the 200 GHz. But the limitation of de-embedding with TRL is that multiple lines are required to cover the wide frequency band.

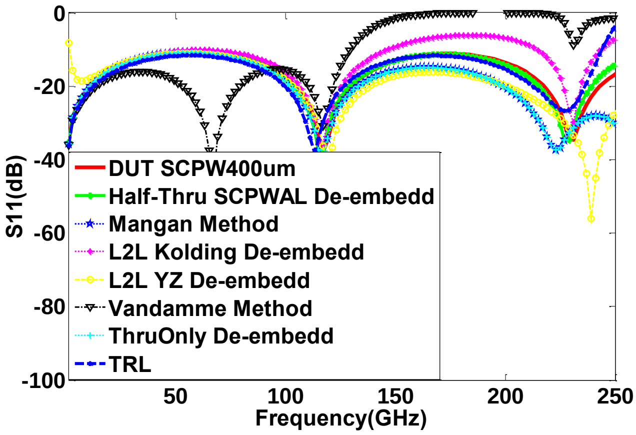

Figure 10. *Reflection coefficient of SCPW line*

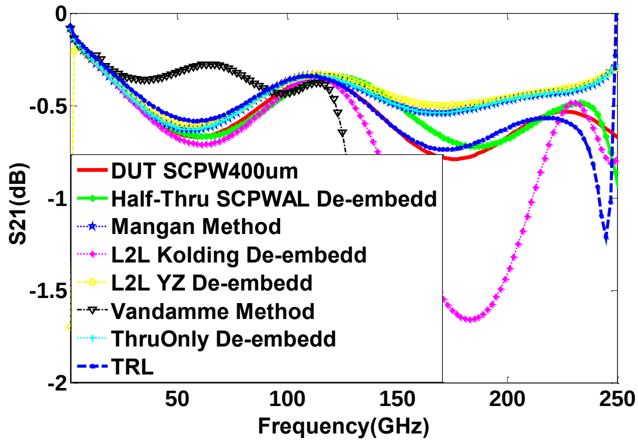

Figure 11. *Transmission coefficient of SCPW line*

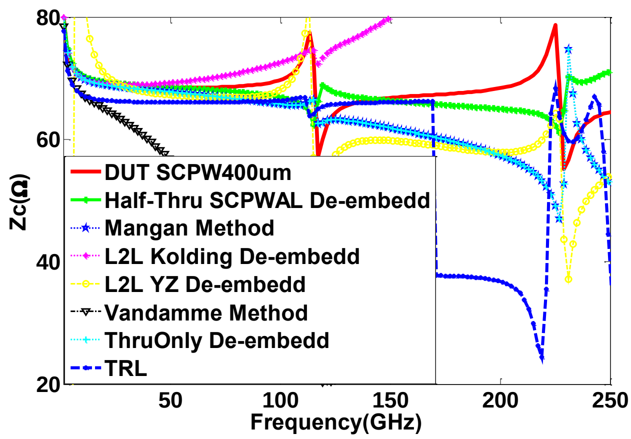

Figure 12. *Characteristic impedance of the SCPW transmission line*

III-1-De-embedding with and without SCPW accessline

There are two kinds of de-embedding devices in the literatures. Firstly, when the DUT is directly connected to the PAD [4], [6]. Secondly, when the DUT is connected to the PAD with interconnecting lines [3], [5], such as transmission lines. In this part we are comparing the de-embedding with and without the accesslines, means whether the long interconnects is required to characterize the DUT in the millimeter and sub-millimeter wave frequency range. From the plots of S_{21}, S_{11} and the characteristic impedance vs frequency plots (Figure 13 to

Figure 15), it is clear that a better de-embedding is obtained from the DUT when accesslines are considered. If the DUT is directly connecting to the pad without interconnects, the discontinuity between the PAD and the DUT will not well de-embedded. This will affects the accuracy of the de-embedding, especially for very high frequencies. For a good de-embedding there should be good continuity of wave propogation in front of the DUT.

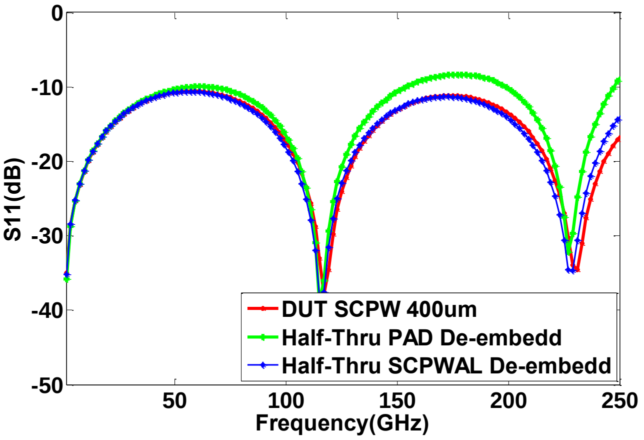

Figure 13. *Comparison of reflection coefficient*

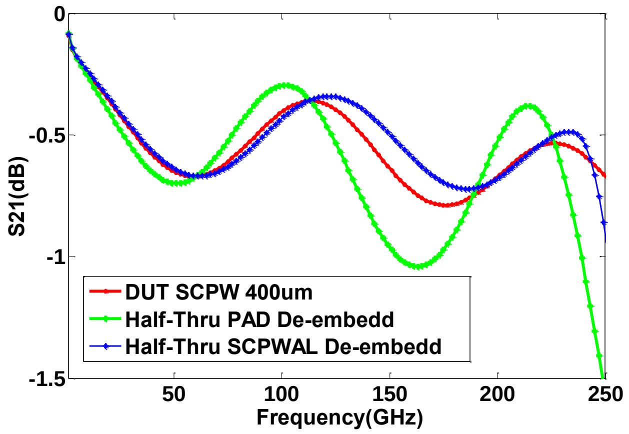

Figure 14. *Comparison of transmission coefficient*

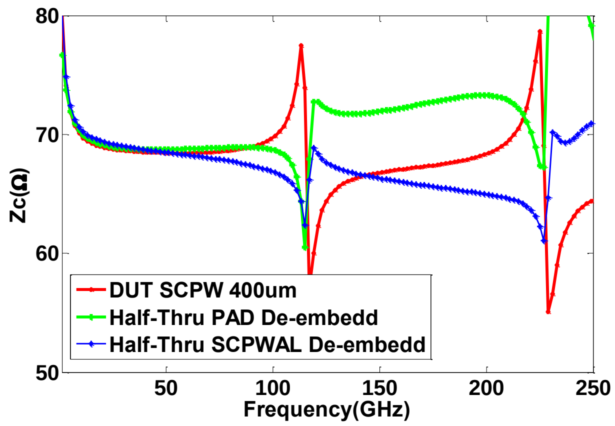

Figure 15. *Characteristic impedance of the SCPW Transmission line vs Frequency*

IV-Conclusions and Perspective

An effective de-embedding method (Half-thru De-embedding) for SCPW transmission line de-embedding at millimeter and sub-millimeter wave frequencies in the integrated technology is proposed. In this method, there is no approximation for the parasitics of the pads and interconnects. Also an effective way of de-embedding the SCPW transmission line is presented. For a good de-embedding, there should be a good continuity in the wave propagation through DUT is required.

We now need to realize and measure these devices to consolidate our electromagnetic simulation results.

V- Acknowledgement

The work presented here has been performed in the RF2THZ SiSoC project of the EUREKA program CATRENE in which the French partners are funded by the DGCIS.

References

[1] Zhang, Bo, Yong-Zhong Xiong, Lei Wang, Sanming Hu, and J.L.-W. Li. "On the De-Embedding Issue of Millimeter-Wave and Sub-Millimeter-Wave Measurement and Circuit Design." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 2, no. 8 (2012): 1361–1369.

[2] Vandamme, E.P., D.M.M. Schreurs, and C. Van Dinther. "Improved Three-Step de-Embedding Method to Accurately Account for the Influence of Pad Parasitics in Silicon on-Wafer RF Test-Structures." *IEEE Transactions on Electron Devices* 48, no. 4 (2001): 737–742.

[3] Kolding, T.E. "On-Wafer Calibration Techniques for Giga-Hertz CMOS Measurements." In *Proceedings of the 1999 International Conference on Microelectronic Test Structures, 1999. ICMTS 1999*, 105–110, 1999.

[4] Mangan, A.M., S.P. Voinigescu, Ming-Ta Yang, and M. Tazlauanu. "De-Embedding Transmission Line Measurements for Accurate Modeling of IC Designs." *IEEE Transactions on Electron Devices* 53, no. 2 (2006): 235–241.

[5] Goto, Yosuke, Youhei Natsukari, and Minoru Fujishima. "New On-Chip De-Embedding for Accurate Evaluation of Symmetric Devices." *Japanese Journal of Applied Physics* 47, no. 4 (2008): 2812–2816.

[6] Ning Li, Kota Matsushita. "Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design." *IEICE Transactions* 93-A (2010): 431–439.

[7] Engen, Glenn F., and Cletus A. Hoer. "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer." *IEEE Transactions on Microwave Theory and Techniques* 27, no. 12 (1979): 987–993.

[8] Deng, Zhiming, and A.M. Niknejad. "The "load-Thru" (LT) de-Embedding Technique for the Measurements of Mm-Wave Balanced 4-Port Devices." In *2010 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 207–210, 2010.

[9] Franc, A. -L, E. Pistono, D. Gloria, and P. Ferrari. "High-Performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Bandpass Filters." *IEEE Transactions on Electron Devices* 59, no. 5 (2012): 1219–1226.

[10] Franc, A. -L, E. Pistono, N. Corrao, D. Gloria, and P. Ferrari. "Compact High-Q, Low-Loss mmW Transmission Lines and Power Splitters in RF CMOS Technology." In *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*, 1–4, 2011.

[11] Microwave Engineering, 4th Edition David M. Pozar