Flex readout study for the ATLAS Alpine Staves layout.

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FLEX READOUT STUDY FOR THE ATLAS ALPINE STAVES LAYOUT.

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Abstract:

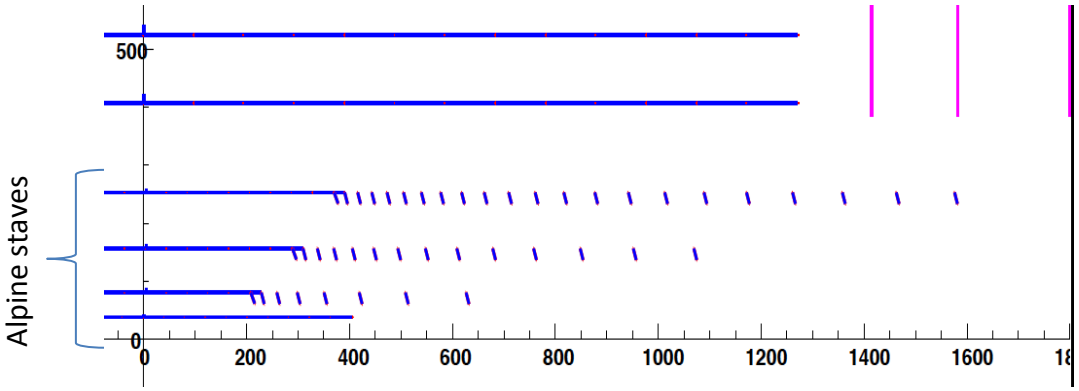
LAPP is involved in the phaseII upgrade the ATLAS pixels tracker [1]: the group is currently designing a pixel detector layout called Alpine Staves. This layout should save matter in the detector. The silicon detectors should also cover a very high angle in the forward region. The pixel modules data should be serialized at the end of the staves and the transmission between pixels and serializer is an issue.
The aim of this study is to estimate the feasibility of data transmission and powering of the front-end thanks to a flex according to the foreseen data rates and the available technology.
The High data rates will need high speed transmissions as optical fibers but the high radiation doses and the matter budget imply to move optical transceivers to the end of staves.

Summary:

1- Specifications and principles.

1-1 The Alpine Stave layout.

The principle of the Alpine Stave layout is to place pixels modules at high η with an inclination angle, a combination of barrel and end-cap.
The incident particles are (quite) perpendicular to the silicon sensors for forward angles. This design allows to save substantially matter and silicon surface in the detector (5.2m² instead of 8.2m²). Two areas can be distinguished: the plains areas (barrel-like), parallel to the beam and the mountains.
Even if several designs are currently studied, a first layout is proposed as follows:

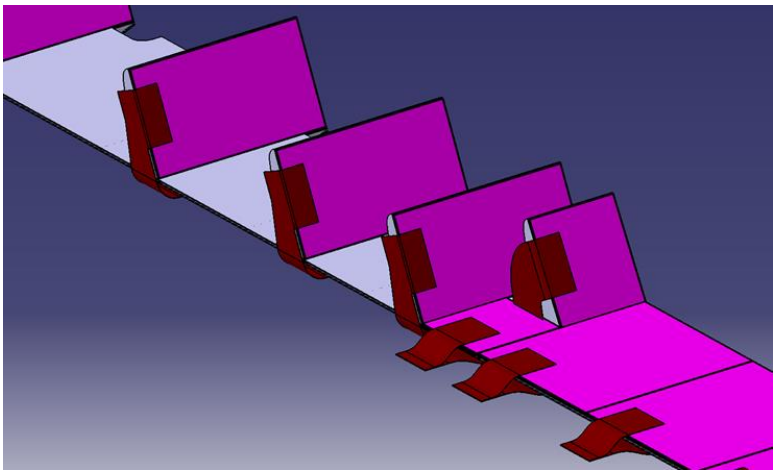


This geometry also removes the need for end cap detectors.
Even other layouts are studied including disks and moving barrel (Everest velo-like), the starting specifications in term of data rates don't change.
All calculations in this document are based on the presented layout but can be transposed to new developments.

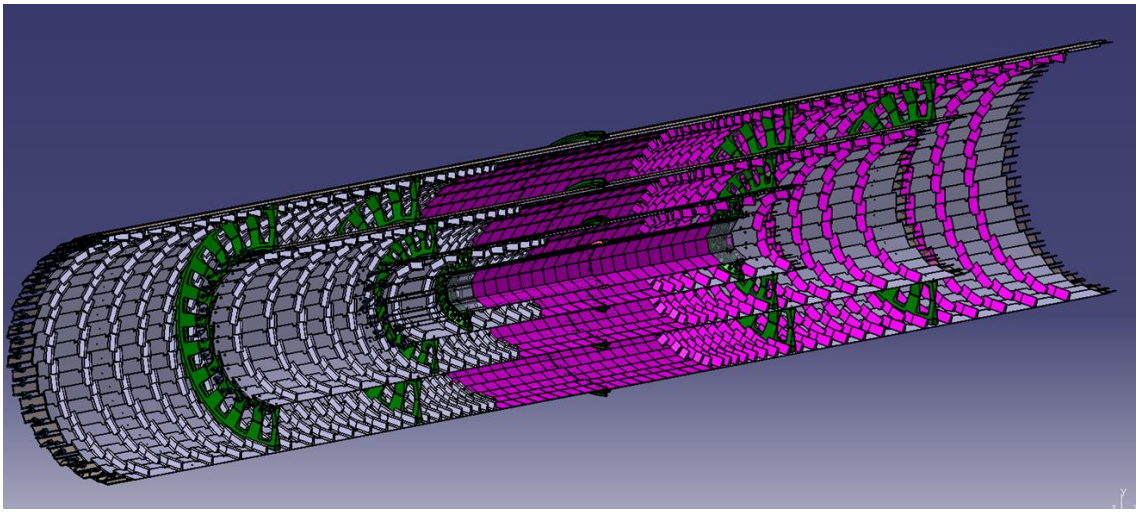
This layout deals with different technical challenges: stiff and cooling mechanical structure, electrical integration (data, power supplies…), installation…

The Alpine layout includes 4 layers. These layers are designed with plains and mountains modules. Modules are the future bricks of the detector, foreseen to be glued on the mechanical structure.
A module will be basically composed by a pixel sensor, a read-out electronics chip and a polyimide flex as a substrate. Different modules are foreseen depending on the location in the staves. The layout geometry has been studied with the already existing modules components, currently used for IBL. We will see that these components will have to evolve in order to reach the future specifications.
Current available components are IBL [2] pixel sensor and front-end FEI4 [3].
There are ~20x19mm² silicon chips bump-bonded. For IBL, there are glued and wire-bonded on a flex module.

On Plains, **M4** (quad modules) are composed by **4** sensor-FE assemblies, so about **40x40mm²** modules.
On mountains, **M2** (dual modules) are composed by **2** sensor-FE assemblies, so about **40x20mm²** modules.
On the plains-mountains transition area, **M1** (single module) are composed by **1** sensor-FE assemblies. They are associated and should form a single module.
The three modules are showed in the following artist view:

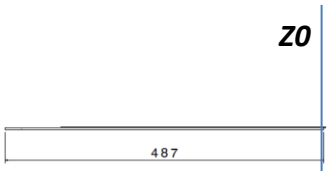


Mechanical studies have shown the feasibility of a carbon foam structure with its integrated cooling.
A CAD picture of the half layout (z axis) follows:

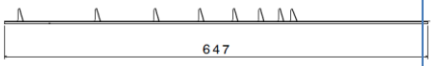


The 4 layers can be detailed from center to the outside as follows: the picture represents only the half detector on the z axis. Z0 the detector center.

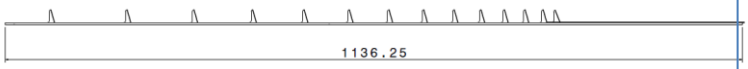
Layer 0: only plains
10 M4 per half detector stave; stave length **487mm**;
8 staves for the half detector (φ=2π);
Total: **16** staves, **160 M4**.
A total of **640** FE.



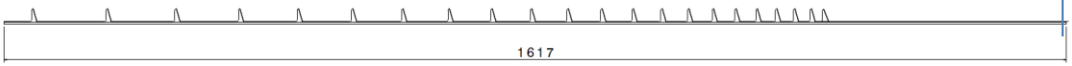
Layer 1:
5 M4 + 2 M1 + 7M2 per half detector stave; stave length **647mm**;
16 staves for the half detector (φ=2π);
Total: **32** staves, **160 M4, 64 M1, 224M2**.
A total of **1152** FE.



Layer 2:
7 M4 + 2 M1 + 13 M2 per half detector stave; stave length **1136.25**mm;
32 staves for the half detector (φ=2π);
Total: **64** staves, **448 M4, 128 M1, 832 M2**.
A Total of **3584** FE.



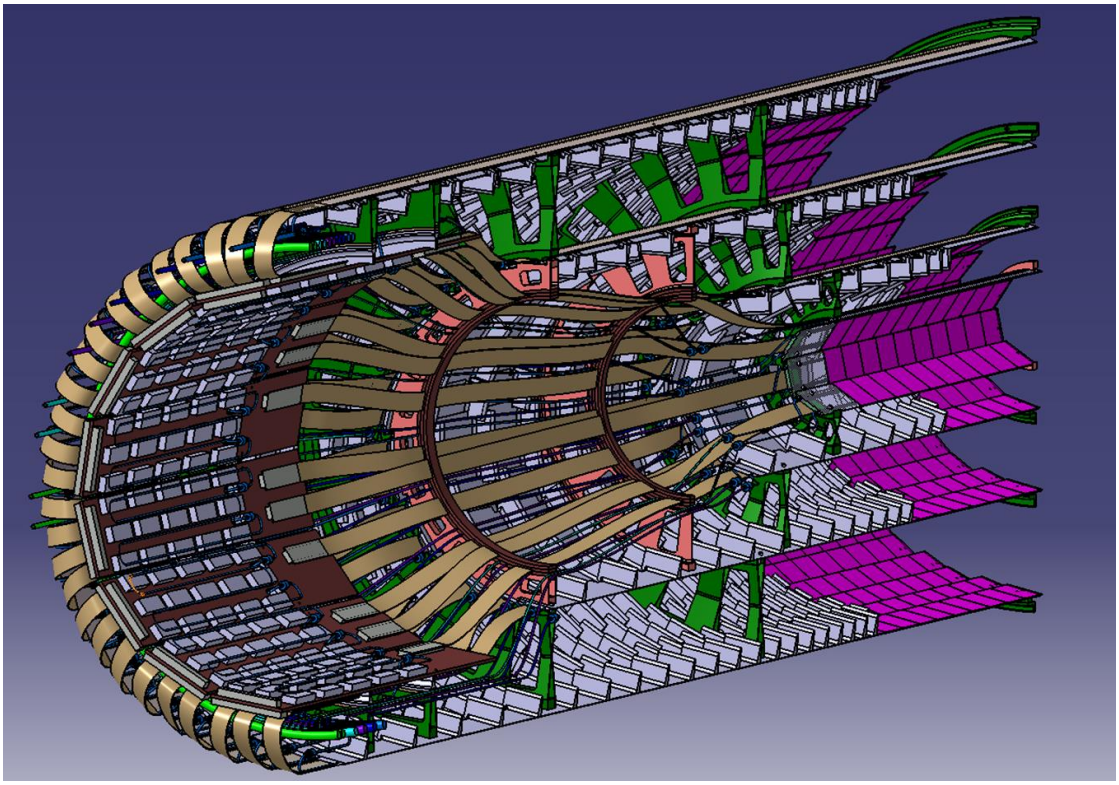
Layer 3:
9 M4 + 2 M1 + 21 M2 per half detector stave; stave length **1617mm**;
52 staves for the half detector (φ=2π);
Total: **104** staves, **936 M4, 208 M1, 2184 M2**.
A total of **8320** FE.



Finally, the total number of modules is: 1704 M4 + 400 M1 + 3240 M2.
M1 transition modules will be interfaced by pair like M2 modules, so the number of flex modules will be 1704 M4 + 200 M1 + 3240 M2= **5144.**
Assuming the use of standard detectors (~20x19mm²), the total pixels+front-end assemblies should be: (1704x4)+400+(3240x2)=**13696**.
The total active area should be around **5.2m².**

Even if pixel detectors and FE evolve, the modules dimensions should be as presented, whatever the number of juxtaposed pixels-FE assemblies: four 20x20mm² or one 40x40mm² are the same concerning data rates.

All the front-end digital data have to be serialized and send to the control system.
The high rates and the number of channels imply the use of optical fibers.
The serializer and optical transceiver should be the closer as possible to the FE electronics in order to insure the data recovery but in the same time their location is limited to the high forward angles because of radiations and matter budget.
A board, called **VIP** (Vertex Interconnection Panel) should host these functionalities and also the local powering of the staves.
Versatile link [4] developed at CERN could be a good solution for this application.
Transceivers should be the most critical component and VTRX could be resistant up to 50Mrad.
The currently foreseen link between FEs and VIP is based on a polyimide flex solution.
Mechanical studies have concluded that the VIP board location should be at the end of staves, for smallest η angle, as showed on the following pictures:



With this solution, the lengths of the flex ribbons, from z=0 to the VIP board are the following:

Layer 0: **1370mm.**
Layer 1: **1370mm.**
Layer 2: **1370mm.**
Layer 3: **1940mm.**

Remark: total number of channels.
The possible future pixels could be **50x50µm²**. It represents 640000 channels for a 40x40mm² M4 module, 320000 for a 40x20mm² M2 module and 160000 for a M1 module. So, a total 13696x160000=**2.19E9** channels for the full detector.

1-2 Specifications on staves modules and transmission.

- Rates:

The next pixel technology hasn't been chosen yet. The expected pixel dimensions should be rectangular 125x25µm² or, which is better according to the alpine layout, square 50x50µm².
With the foreseen HL-LHC occupancy and the expected granularity, data rates have been calculated for the different layers [1].
These rates can be calculated per ~20x20mm² pixels-FE assemblies (independent from the type of module):

Layer 0: **1280Mb/s** per FE.
Layer 1: **640Mb/s** per FE.
Layer 2&3: **160Mb/s** per FE.

- Radiations: the simulations show that the FE electronics should stand **1Grad** TID for the foreseen period of **10 years**.

- Matter budget: the expected maximum particles energy loss should be **2-3‰** on a 20mm flex layer. The staves are 20mm wide under the mountains and so flexes should not exceed this width.

- Power supplies: the foreseen power consumption for the standard FE (20x20mm²) is about **1W**, so a global **~14kW**. The cooling system will have to be able to cool the detector to about **-40°C** and so losses have to be minimized. An important point is also the differential dilatation of the carbon staves and of the flexes. We will see in the powering chapter that a serial powering of the modules is mandatory in order to keep an acceptable efficiency.

- High voltage: pixels will be biased with about **-1500V**. Isolation should ensure break-downs.

Remark: total rate.
For layer0, the total rate for the detector should be 640x1280Mb/s=**819.2Gb/s**.
For layer1, the total rate for the detector should be 1152x640Mb/s=**737.3Gb/s**.
For layer2, the total rate for the detector should be 3584x160Mb/s=**573.4Gb/s**.
For layer3, the total rate for the detector should be 8320x160Mb/s=**1331.2Gb/s**.
So a total of **3461.1Gb/s** for the full detector.

1-3 Strategy.

Discussions between physics and technology are currently validating the possible future granularity of the pixels detectors. So, whatever the next pixels-FE assembly technology and dimensions, we can already estimate the data rates that we will encounter.
To the layout point of view, we have to find solutions for modules integration on the stages and for their data transmissions to end of stave boards.
FE5 are currently under development in order to reach the foreseen granularity. The TSMC 65nm technology is today's best candidate.
The transmission mode is not chosen yet. It will depend on the matter budget, on the possible line rates, on the impedance control and losses… Two issues are linked and have to be solved: the transmission type (drivers-receivers) and the physical transmission line. The lines length will be typically from 1370mm to 1940mm.
Whatever the chosen layout, the layer0 data rate will be the most critical. Several scenari are possible, from fast CLM to LVDS/SLVS and from flex to twisted pairs and microcoax.
By experience, it seems to be difficult to go over 500Mb/s on flex differential pairs. Tests in [5] showed that twisted pairs could reach rates up to 1Gb/s over 1-2m.
Powering modules in a serial configuration imply to use AC coupled lines and DC balanced protocol (as much 1 as 0).

CML (current mode logic) is a very high speed 50Ω matched transmission standard. It is 16mA current based and should be reserved for matched twisted pairs.
Both drivers and receivers are 50Ω matched and the issue should be to match lines impedance to 50Ω.

LVDS or SLVS are high speed differential transmission lines, current based, usually 100Ω matched.

We will see in the stack-up chapter that it is difficult to design 100Ω matched differential lines with the studied polyimide-copper flex solution
Nevertheless, a solution could be to end each LVDS or SLVS lines with its line impedance. Only the reception sensibility should be affected if impedance is different from 100Ω.

In our study, we think that LVDS/SLVS on differential pairs over flexes are more realistic for several reasons:

- Data concentration should be performed using CERN's rad-hard GBT chip. It is currently designed for these specific applications. It will include slow control utilities too.
- The use of flexes for powers and cables for data make the feasibility harder.
- LVDS/SLVS transmissions are current based transmissions. In a limited number of copper layers configuration, impedances will be difficult to match. A solution can be a specific matching for each transmission line.
- High speed transmissions over twisted pairs have to prove the high transmission rates without exceeding the matter budget, typically 42AWG. Twisted pairs do not dispense the powering and so the implementation of two different technologies. 42AWG cables are hard to implement (connection, very fragile).

- Calculation of the twisted pairs losses:

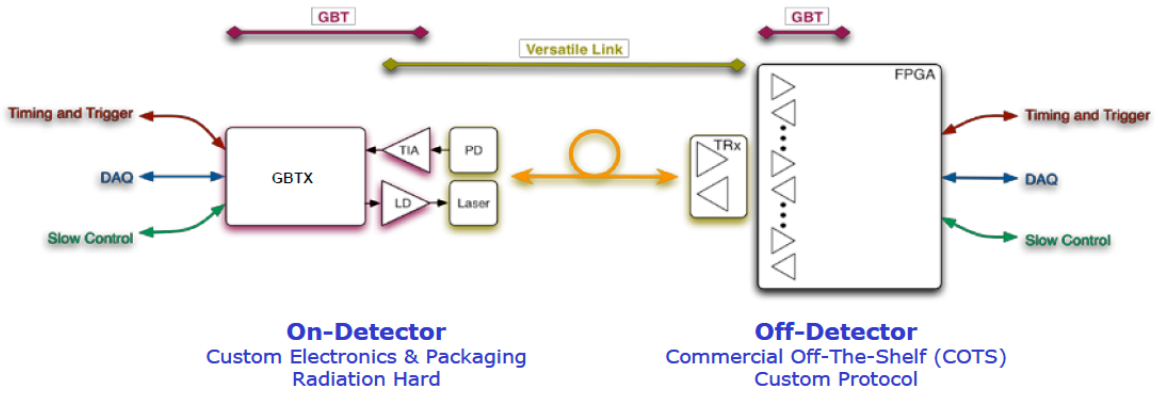
The specification on energy loss is maximum 2-3‰ radiation length for a 2cm wide flex. Gauge 38 (100µm copper diameter) twisted pairs have been studied. The total copper section is about $S=2.\pi.(100/2)^2 \approx 15708 \mu m^2$.
The layer0 includes 10 M4 modules. Each FE will need a 1280Mb/s transmission. Assuming that 38 AWG twisted pairs are able to reach this rate, we should implement 4 twisted pairs per module so a total of 40 twisted pairs at the most concentrated area. It represents a total section of $40 \times 15708 \approx 63000 \mu m^2$.
Bringing this section to an equivalent 2cm wide flex, it represents a 31µm solid copper layer.
The copper radiation length is 1.44cm and so the corresponding loss is 31µm/1.44cm=**2.2‰**.
Powering the modules with a 5µm copper flex (100µm minimum polyimide, 28cm radiation length), the loss due to the flex should be:
(5µm/1.44cm)+(100µm/28cm)=**0.7‰**.

Finally the total loss is **2.9‰**, which is not so far from specification.
Assuming that gauge 42 (65µm diameter) reach rates, the loss should be **1.7‰.**

Twinax is also a candidate. It can reach up to 6Gb/s but its diameter is 250µm.
We should need 10 twinax cable per layer0 stave. Loss should be about **4.2‰.**

- CERN PH GBT [6].

The GBTX is a radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links for high-energy physics experiments. The link provides three “distinct” data paths for Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information. These three logical paths are merged on a single optical link, the versatile link. This link is used simultaneously for data readout, trigger data, timing control distribution, and experiment slow control and monitoring.
The GBTX (DAQ part) is a serdes allowing up to 40 parallel links for front-ends @80Mb/s. These links, called e-links, include three lines: data upstream, data downstream and clock, all synchronous with the machine. The e-links can be grouped up to 4 in order to reach **320Mb/s** data rates.



PH division is currently studying a possible specific low power upgrade of the GBTX (LPGBTX). E-links should reach **640Mb/s** data rate. The optical fiber speed should be also doubled.

e-links are based on SLVS levels. GBTX receivers can receive both SLVS and LVDS and drivers only drive SLVS. These links have been tested with success on several meters distances.

We decided to study the use of flex with GBTX data recovering because we think this system corresponds exactly to the purpose.
As the next FE5 interface stages are not yet developed, we started our study assuming the possibility to implement in the future the needed number of parallel differential lines in the pixel FE, in **320Mb/s** and **640Mb/s** versions. These numbers of lines will depend on the layers and on the modules.

2- Constrains and geometry.

2-1 Constrains.

- Energy particles losses:

The most restrictive specification for the flexes is the **2-3‰** maximum radiation length per **20mm** wide flex. The copper radiation length is **1.44cm** and the polyimide radiation length is **28.6cm**. So the copper is stopping about 20 times more particles than polyimide.
We will see that as the number of signals is huge, we will need the maximum layers as possible in the flex, so the thinner copper laminates as possible.
Thinner copper laminates over polyimide available are **5µm**: **50µm** polyimide core double-sided with **5µm** copper layers. The corresponding bondply is epoxy 25µm – polyimide 25µm –epoxy 25µm, so **75µm** wide.
Even if the polyimide is ~20 times more "transparent" to particles, its thickness is not negligible with 5µm copper laminates.
Assuming that we should have about 40% tracks occupancy on flex layers for signals and powers/references, we can estimate to **6** the maximal number of copper layers in a flex.
A low number of layers also reduce the stiffness of the flex that could be a concern for the bended parts between the staves and the VIP board.

- Transmission bandwidth:

The minimum bandwidth is commonly calculated using a maximal rise/fall time (tr) on a transition signal.
Typically BW(-3dB)=0.35/tr(10-90%) with tr the maximal 10-90% rise/fall time for the third of the period T.
For a **320Mb/s** rate, T=3.125ns. Taking tr=1ns, BW(-3dB)=0.35/1ns=**350MHz**.
For a **640Mb/s** rate, BW(-3dB)=**700MHz**.

2-2 Flex geometry.

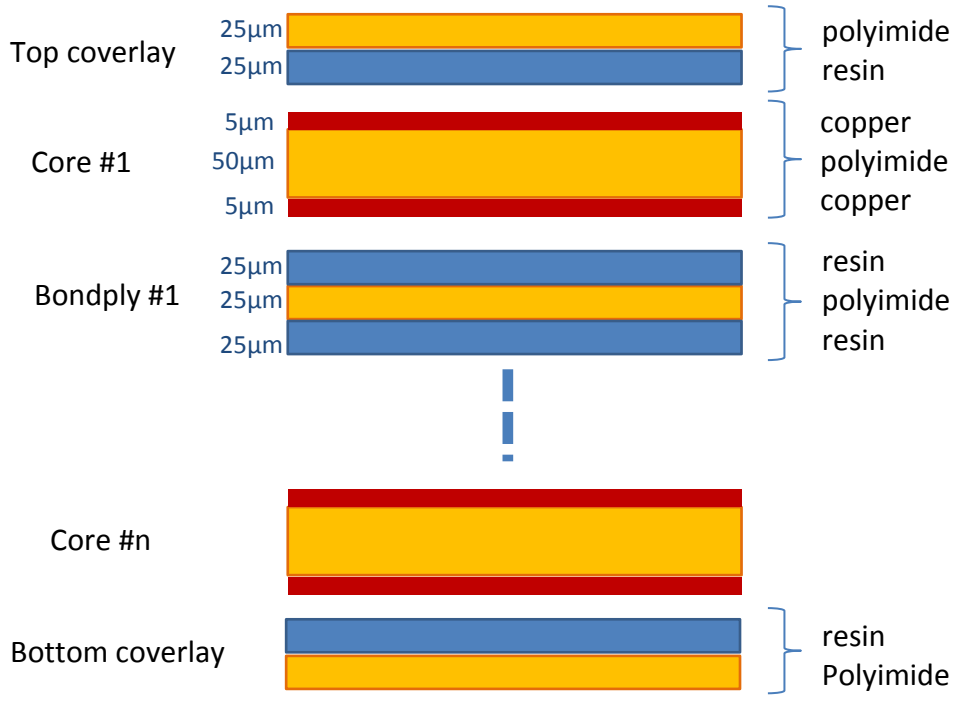
Remark: we will distinguish the detector layers from the inside flex copper layers. We will talk about *flex layers* for the inside flex layers and *layers (or detector layers)* for the detectors layers0, 1...

The flexes are foreseen to be between **1370mm** and **1940mm** long.
They should include up to **6** copper layers.
After discussions with several producers, we based the study on the CERN TS DEM propositions and advices.
In radiations environment, experience showed that epoxy resin is more reliable than acrylic resin.

The stack up is based on different available materials:

- cores: 5µm copper – 50µm polyimide – 5µm copper.
  Equivalent dielectric constant **ε=3.2**. UPISEL-N (UBE industries).
- Bondplys: 25µm epoxy resin – 25µm polyimide - 25µm epoxy resin.
  Equivalent dielectric constant **ε=4.03**. akaflex KDF (Krempel).
- Coverlays: 25µm polyimide - 25µm epoxy resin.
  Equivalent dielectric constant **ε=4.03**. akaflex KDF (Krempel).

Typical stack-up:

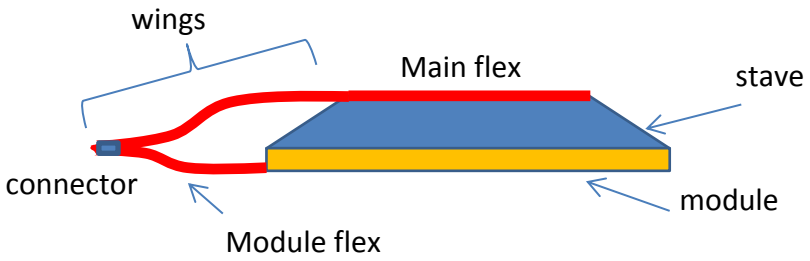


Breakdown voltage is about **6.9kV** for **25µm** of polyimide.

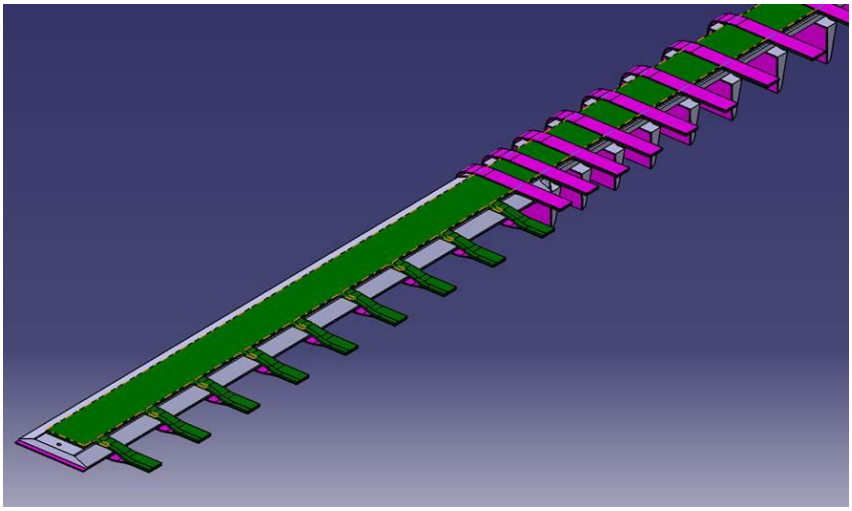
The number of cores in the stack-up is not limited if there is no interconnection using plated holes. All the flex layers have to be aligned and hot pressed during assembly.
A limitation occurs for long flexes: interconnection holes can shift from a flex layer to another up to 1-2mm at the end of the flex. If needed the holes will be designed oblong.
For ~2m flex, the minimum etching width is 100µm.

A first geometry is possible: pixel modules connected to the flex with connectors on the flex. This geometry needs to pull up the internal signals on the top coverlay, so needs to implement plated holes for each module connector. Oblong holes should take too much place and should be too difficult to perform on a 2m flex. It should also be expensive and should reduce the possibility for the other modules lines inside the flex.
We will prefer the wings geometry: a main flex with no interconnections between the layers, only wings for each module. As we plan to distribute powers and data on different layers, each module should be connected to two wings: one for data and one for powers. These wings are built on different internal copper layers but can be connected on a single flex module. The connections should be done by micro-connectors at the end of the wings.
Flex layers will be specific for data and for powers/HV, so for each module two adjacent wings will be connected to the module flex. Even adjacent, these wings will come out from a different flex layer.
Depending on the detector layer we will see that we will implement one or two HV/supplies flex layers.

Cross section of the stave with module and flex:

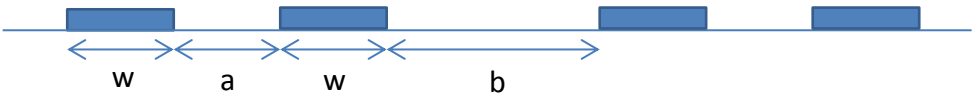


Data flex layers will be filled with signals from several modules and signals from a single module will not be split on different layers.
The following picture shows an example main flex with plains modules wings (green) and mountains wings (pink).



Mountains and plains flex modules are not connected on the same side of the main flex wings.
If copper layers are not alternatively signals and references(as ground), plated holes should be necessary in order to keep connectors on the same side. It should not be a problem if performed locally on the wing.

As we decided to use LVDS/SLVS standards for data transmissions, we will implement differential pairs. The common differential tracks separation use to be as follows:



With a=w and b=2w. With **w=100µm**, we can estimate a typical occupation width for a differential pair of **5w=500µm**, including the isolation from an adjacent pair.

The mechanics CAD estimate the total wings flex width to **30mm** for plains and **20mm** for mountains. The distribution of this width between the data wing and the powers wing will depend on the layer and on the module type: number of pair varies and so the needed width. Nevertheless, we will try to have a limited number of configurations because of connectors occupancies considerations and for standardization. We will see these distributions in the powering and countering chapters.
We can estimate the wings length to **30mm**.

2-3 dimensions and thermal considerations.

Main flexes will be attached to staves with enough freedom that they will be able to retract when cooled down. Carbon staves will be cooled from +20°C to -40°C.
Flexes will be obviously attached to staves at ambient temperature.
With CTEs (Coefficient of thermal expansion):
Carbon: αc=-7.6E-7 (1/K).
Flex: $\alpha f \approx$20E-6 (1/K).

We can calculate ΔS and ΔF, the staves and flexes lengths variations with a maximum -60°C temperature variation and for the different detector layers (length with contact between stave and flex):

Layers 0: contact length=487mm, ΔS=22µm, ΔF=-584µm.
Layers 1: contact length=647mm, ΔS=30µm, ΔF=-776µm.
Layers 2: contact length=1136mm, ΔS=52µm, ΔF=-1.36mm
Layers 3: contact length=1617mm, ΔS=74µm, ΔF=-1.94mm

We can see that staves and flexes have different expansions, ~2mm in the worst case. It will be difficult to make them physically dependent.
We should produce flexes taking into account the retraction lengths.
In another hand, It is very difficult to foresee the temperature of a flex not fully attached to the stave. Its temperature will depend on its power consumption and the thermal exchanges with the contact points of the staves and with the detector gaz. We can assume that its temperature will be higher than the stave one and so the contraction should be reduced.

3- Powering.

The baseline layout already foresaw serial powering because of ohmic losses over cables. The power consumption specification for the next FE5 is the same than for the current FEI4, 1W per 20x20mm² pixels-FE assembly.
In such a serial powering scheme, a protection module (MPC) [7,8] should allow to shunt a failing module and to allow the powering of the others in the chain. This MPC will need a specific signal (see 4-).

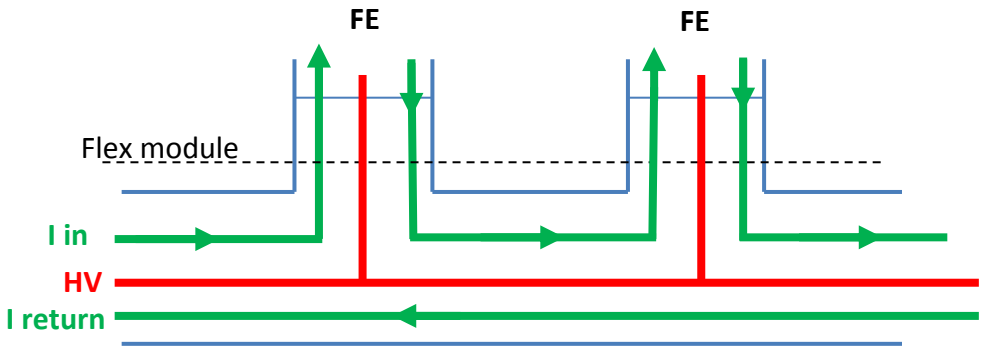
We foresee 13696 20x20mm² pixels-FE assemblies or equivalent, so a total power consumption about **13.7kW**.
The serial powering is based on the use of shunt-LDO. Shunt LDO allows to drive a constant current over the power line and to provide regulated voltages to the local electronics. The estimated current for modules is **0.6A**.

- **Serial powering vs parallel powering:**

The ohmic loss is $\mathbf{P=RI^2}$ with **R** the resistance of the track and **I** the supplied current. I is the same whatever the mode of powering, **0.6A**.
We can estimate the shunt-LDO drop voltage between input and output to about **1.7V**.
Powering n modules in parallel needs a number of n tracks in parallel on the flex layer. With a standard flex layer, tracks will be n times thinner and the resistance will be n times higher. So, the parallel power consumption will be n times higher too.
On a other hand, serial powering needs current power supply with an available voltage n times higher.
Typically the number of serialized modules will be **n=7** to **10**, depending on detector layers.
We will see that consumption efficiency is about **~80%** with serial powering. This number should decrease to **~30%** with parallel powering which is not acceptable for electric and thermic issues.

Serial powering avoids the use of several flex layers and plated holes because tracks never cross. Current sources should be ideally implemented and controlled on the VIP board, at the end of the stave.

As pixels HV return current is made by the front-end, parallel HV powering is also possible without crossing tracks:



The voltage capability of the source will depend on the number of serialized modules.

Remark on serial powering and HV powering: with serial powering the modules will be powered with different voltage references. The HV will be different for each of them, typically 1.7V from one to the next. This difference is over about 1500V, so will be tinny and should be calibrated.

- **Thermic simulations on staves:**

Staves will be cooled to -40°C thanks CO2 pipes included in the core.
Specification for the maximum temperature rise is **7°C**, so **-33°C**.
Cooling system will be sized in order to be able to reach these specifications according to modules power consumption, losses and VIP end of stave boards .

- **Thermic influence on resistance:**

Even if flexes are not in continuous contact with the staves, the tracker is closed and we can assume that the temperature will be constant and continuous in a steady state.
Copper resistivity depends on temperature: ρ[-40°C]=13E-6 Ω.mm and ρ[20°C]=17E-6 Ω.mm.
The difference is slight and as discussed in 2-3, we are not able to foresee the copper temperature. We will take ρ=15E-6 Ω.mm for calculations. It corresponds to a temperature of -5°C.

Tracks resistance formula, with l the length and s the cross-section surface:

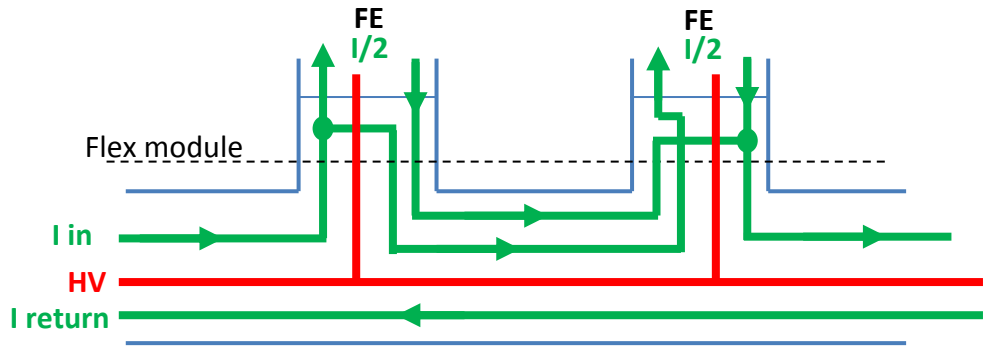
$$R = \rho \frac{l}{s}$$

- **Module association:**

On the different types of modules, the different numbers of pixels/FE are supplied in parallel. A 20x20mm² pixel/FE assembly current consumption is **0.6A** , so, the current module depends on the number of FE on the module: **0.6A for M1, 1.2A for M2, 2.4A for M4**.
Except for the layer0 (only M4 modules), the three types of modules are used in the three other detector layers.

A first solution is to dedicate three different serial powering to the three different types of modules. It corresponds to a semi-parallel powering for the M1 and M2 modules. This solution requires three different current sources which is not interesting because of the sources efficiencies and because of the routing.

A good solution should be to implement only M4 current sources (2.4A) and to associate locally M2 modules by pairs:



M1 modules are only present at the transition area by pairs and will be processed like M2 modules. With this architecture, we can count the number of equivalent M4 modules for each detector layer:

2M1≈1M2; 2M2≈1M4

Layer0: ***10 M4***.
Layer1: 5 M4 + 2 M1 + 7M2 ≈ ***9 M4***.
Layer2: 7 M4 + 2 M1 + 13 M2 ≈ ***14 M4***.
Layer3: 9 M4 + 2 M1 + 21 M2 ≈ ***20 M4***.

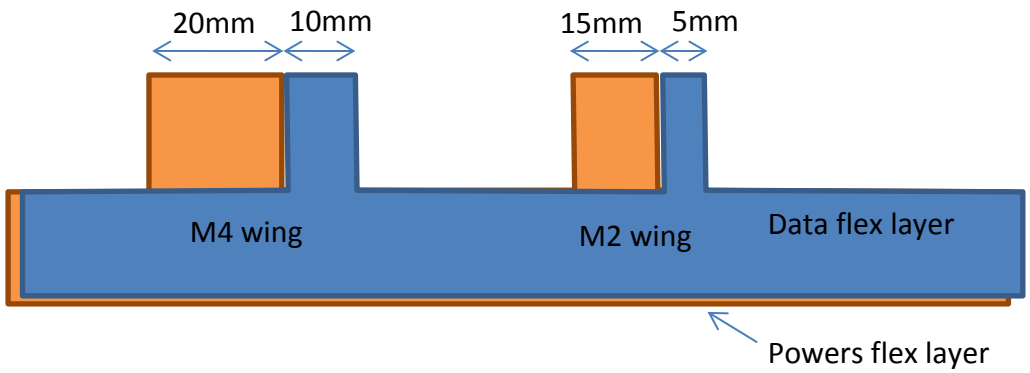
The number of serialized modules would depend on the current source available output voltage and on the available number of flex layers. Even serialized, a module fail should not affect the others because of the MPC protection.

Calculations in the chapter 4- show that the number of data differential pairs only allows 1 power flex layer for layer0&1 and 2 power flex layers for layer2&3.
The most relevant maximum number of serialized module is **10**.
With 1.7V shunt-LDO drop voltage, the current source will be able to supply the chain with a wide output voltage range, typically from 11.9V (7 M4) to 17V (10 M4).
As the HV current returns by FEs, the distribution is parallel. We can group modules for reliability, typically by five. Occupation is not an issue because of low current and so small tracks width.

- **Tracks distribution on flex:**

We will implement the tracks on the flexes by using the maximum possible copper width. HV tracks and isolations have not been tested yet but 500µm for both seems to be enough in theory. The spare width will be shared for serial powers. As the current is constant on the serial line, the incoming track and returning track should have the same width.
Tracks will be distributed on 20mm linear sections of main flexes but also on the two kind of wings. We estimated these widths to **30mm** for plains and **20mm** for mountains.
The needed widths for data wing and powers wing depend on the detector layer and on the module type. For external detector layers the number of data lines will be lower than for internal ones. We could implement wider power wings and thinner data wings in order to limit the power losses but module flex should be no more standard. We will see that M4-layer0 is fixing the data wing width to **~10mm** and M2 data wing is fixed to **~5mm** for connector issues.
For calculations we estimated the wings lengths to **30mm** but this number could be reduced.

The following sketch illustrates the flex concept with one powers layer and one data layer.



3-1 Detector layer 0: see annex A

10 M4; I=2.4A; P≈40W; **30mm** plains wings.

Serializing 10 modules, we can implement a single power line on a single flex layer. We can implement two HV lines.

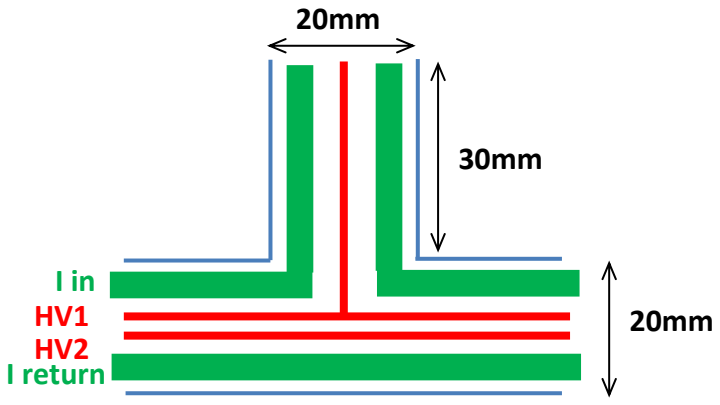
- Linear part of the main flex: **1370mm**

With 0.5mm tracks for HVs and isolations, we can implement (20-(7x0.5))/2=**8.25mm** power lines for a total copper width of 17.5mm .
The total round trip is 1370x2=2740mm, so the resistance is

$$Rlin = \frac{2740 \times 15.10^{-6}}{0.005 \times 8.25} = 1\Omega$$

- wings: **30mm** long; double with the module flex, so **60mm**.

The total wing width is **30mm**. Data transmission will need 20 differential pairs (cf. 4-1) for M4 modules, so ~20x0.5=10mm for the data wing and 20mm for the powers wings. In order to standardize module flexes, M4-layer0 module is fixing M4 data wing width to **10mm** because it will be the wider.
We can implement (20-(5x0.5))/2=**8.75mm** power lines.



The total length is 120mm per module, 1200mm for the 10 modules flex.
Total wing resistance is

$$Rw = \frac{1200 \times 15.10^{-6}}{0.005 \times 8.75} = 0.4\Omega$$

- <u>total resistance and power loss:</u>

The total resistance is 1+0.4=**1.4Ω.**
So a power loss Pl=1.4x2.4²=**8W** and a voltage drop of 1.4x2.4=**3.4V.**
We will need a current source with a voltage ability about (10x1.7)+3.4=**20.4V.**
The efficiency is (40/40+8)*100=**83.3%.**

<u>Remark on a 2x5 modules serial powered:</u>
With a 2x5 modules serial powered configuration, the power loss is about 20W. Even if the tracks are only doubled on the first 5 modules part of the flex, the power loss is more than the twice because of isolations.

<u>3-2 Detector layer 1: see annex B.</u>

5 M4 + 2 M1 + 7M2 ≈ ***9 M4***.
I=2.4A; P≈36W; 30mm plains wings and **20mm** mountain wings.

For M2 and M1 modules, we will use the technic described in *module association pg.18*. Serializing a total of 9 equivalent M4 modules, we can implement a single power line.
We can implement two HV lines, one for the 5 M4 modules and one for the M2&M1 modules.
Powering will be implemented on a single flex layer.

- <u>Linear part of the main flex</u>: **1370mm**

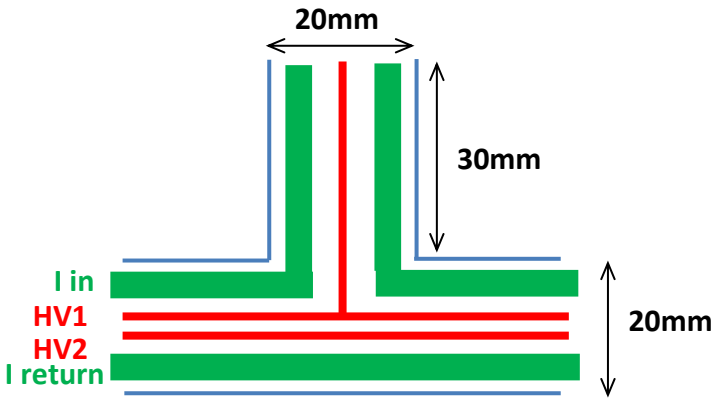
For simpler calculation, we can neglect the 500µm additional isolation between two coupled M2 modules.
With 0.5mm tracks for HVs and isolations, we can implement (20-(7x0.5))/2=8.25mm power lines.
The total round trip is 1370x2=2740mm, so the resistance is

$$Rlin = \frac{2740.15.10^{-6}}{0.005.8.25} = 1\Omega$$

- wings: 30mm long; double with the module flex, so 60mm.

The total wing width is **30mm** for plains (M4) and **20mm** for mountains (M2).

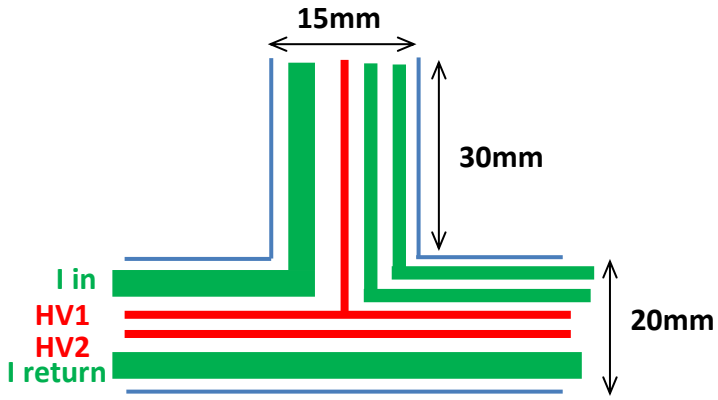
- *5 Plains (M4)*: data transmission will need 10 differential pairs + 1 track (cf. 4-2), so ~(10x0,5)+0,2=5,2mm. Taking
  Taking 10mm as a standard for the data wing and 20mm for the powers wings, we can implement (20-(5x0,5))/2=8,75mm power lines.



The total length is ~120mm per module, 600mm for the 5 modules flex.
Total plains wing resistance is

$$Rwp = \frac{600 \times 15.10^{-6}}{0{,}005 \times 8{,}75} = 0{,}2\Omega$$

- *8 (7+1) mountains (M2 & M1)*: data transmission will need 6 differential pairs + 1 track (cf. 4-2), so ~(6x0.5)+0.2=3.2mm.
  Taking 5mm as a minimum for the data wing and 15mm for the powers wings, we can implement (15-(6x0.5))/2=6mm power lines (we neglect the isolation between the two associated modules lines).



The total length is 120mm per module, 960mm for the 8 modules flex.

Total mountains wing resistance is

$$Rwm = \frac{960 \times 15.10^{-6}}{0.005 \times 6} = 0.48\Omega$$

- <u>total resistance and power loss:</u>

The total resistance is **1.68Ω**.
So a power loss Pl=1.68x2.4²=**9.7W** and a voltage drop of 1.68x2.4=**4V.**
We will need a current source with a voltage ability about (9x1.7)+4=**19.3V**.
The efficiency is (36/36+9.7)*100=**79%.**

3-3 Detector layer 2: see annex C

7 M4 + 2 M1 + 13M2 ≈ ***14 M4***.
I=2.4A; P≈56W; 30mm plains wings and **20mm** mountain wings.

For M2 and M1 modules, we will use the technic described in *module association pg.18*. We fixed to 10 the maximum number serialized modules, so here we will need two serial powering lines. With 14 equivalent M4 modules, we will implement one line for the 7 M4 modules (plains) and one line for the 13 M2 + 2 M1 modules (mountains).
Two solutions have been compared: the two lines implemented on one flex layer or each on a dedicated flex layer. On the detector layer 2, the data rates decrease a lot and so the number of differential pairs. In 4-2, we can see that four flex layers are enough in order to transmit data.
Two available flex layers should allow to reduce the power loss.
We can implement one HV line for the M4 modules layer and two for the M2/M1 modules.

3-3-1 Powering layer for 7 M4:

- <u>Linear part of the main flex</u>: 1370mm

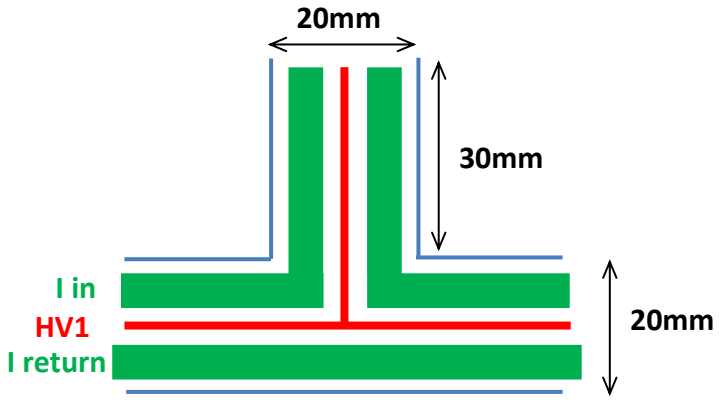
With 0.5mm tracks for HV and isolations, we can implement (20-(5x0.5))/2=8.75mm power lines.

The total round trip is 1370x2=2740mm, so the resistance is

$$Rlin = \frac{2740 \times 15.10^{-6}}{0.005 \times 8.75} = 0.94\Omega$$

- Wings for 7 M4: 30mm long; double with the module flex, so 60mm.

The total plain wing width is 30mm. Data transmission will need 6 differential pairs + 1 track (cf. 4-3), so ~(6x0.5)+0.2=3.2mm.
Taking 10mm as a standard for the data wing and 20mm for the powers wings, we can implement (20-(5x0.5))/2=8.75mm power lines.



The total length is ~120mm per module, 840mm for the 7 modules flex.
Total wing resistance is

$$Rwp = \frac{840 \times 15.10^{-6}}{0.005 \times 8.75} = 0.29\Omega$$

- total resistance and power loss for 7 M4 flex layer:

The total resistance is 1.2Ω.
So a power loss Pl=1.2x2.4²=6.9W and a voltage drop of 1.2x2.4=2.9V.
We will need a current source with a voltage ability about (7x1.7)+2.9=14.8V.

3-3-2 Powering layer for 2 M1 + 13M2:

The power consumption is equivalent to 7 M4 modules.

- Linear part of the main flex: the power lines are not covering the full length of the main flex but only the part for mountains: 1370-278=1090mm

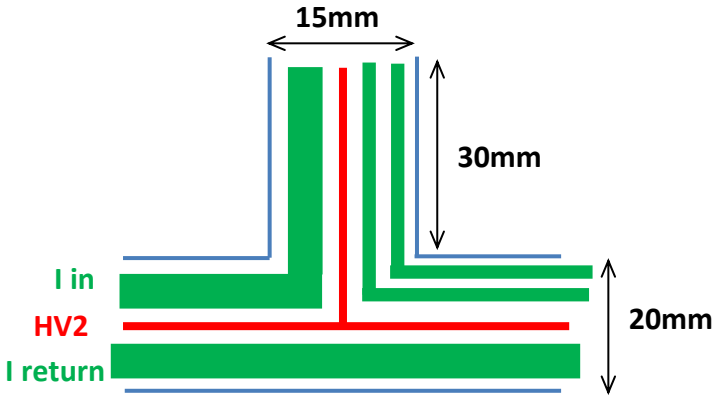
With 0.5mm tracks for HV and isolations, we can implement (20-(5x0.5))/2=8.75mm power lines.

The total round trip is 1090x2=2180mm, so the resistance is

$$Rlin = \frac{2180 \times 15.10^{-6}}{0.005 \times 8.75} = 0.75\Omega$$

- Wings for 2 M1 + 13M2: 30mm long; double with the module flex, so 60mm.

The total mountain wing width is 20mm. Data transmission will need 4 differential pairs + 1 track (cf. 4-3), so ~(4x0.5)+0.2=3.2mm.
Taking 5mm as a minimum for the data wing and 15mm for the powers wings, we can implement (15-(6x0.5))/2=6mm power lines (we neglect the isolation between the two associated modules lines).



The total length is ~120mm per module, 1680mm for the 14 modules flex.
Total wing resistance is

$$Rwp = \frac{1680 \times 15.10^{-6}}{0.005 \times 6} = 0.84\Omega$$

- total resistance and power loss for 2 M1 + 13M2:

The total resistance is 1.6Ω.
So a power loss Pl=1.6x2.4²=9.2W and a voltage drop of 1.6x2.4=3.84V.
We will need a current source with a voltage ability about (7x1.7)+3.84=15.7V.

Total power loss for the layer2:

The total power loss Pl=9.2+6.9=**16.1W** and the efficiency is (56/56+16.1)*100=**78%.**

3-4 Detector layer 3: see annex D

9 M4 + 2 M1 + 21 M2 ≈ ***20 M4***.
I=2.4A; P≈80W; 30mm plains wings and **20mm** mountain wings.

For M2 and M1 modules, we will use the technic described in *module association pg.18*. We fixed to 10 the maximum number serialized modules.
As for detector layer 2 we will need two serial powering lines on two flex layers:

- one serial power line for 9 M4 modules + 2 M1 + 1 M2 modules and 2 HV lines.
- one serial power line for the 20 remaining and 2 HV lines.

3-4-1 Powering layer for 9 M4 modules + 2 M1 + 1 M2:

The power consumption is equivalent to 10 M4 modules.

- Linear part of the main flex: 1940mm

With 0.5mm tracks for HV and isolations, we can implement (20-(7x0.5))/2=8.25mm power lines.

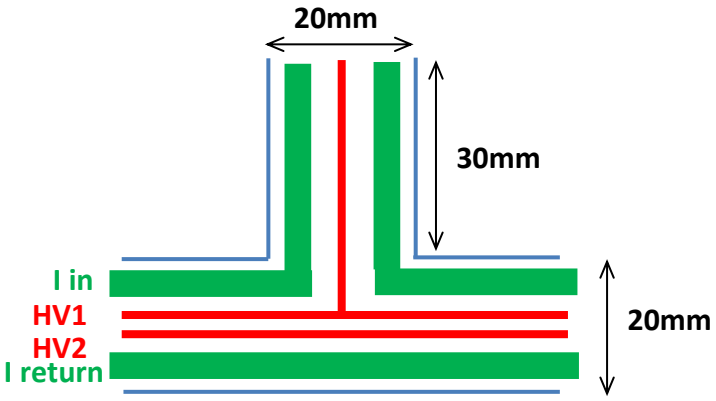
The total round trip is 1940x2=3880mm, so the resistance is

$$Rlin = \frac{3880 \times 15.10^{-6}}{0.005 \times 8.25} = 1.4\Omega$$

- Wings for 9 M4 modules + 2 M1 + 1 M2:

The M1 and M2 modules will be connected using the technic described in *module association pg.18*. We can neglect the isolation between the two modules and estimate the resistance for 11 equivalent M4 modules.
Wings 30mm long; double with the module flex, so 60mm.

The total plain wing width is 30mm. Data transmission will need 6 differential pairs + 1 track (cf. 4-4), so ~(6x0.5)+0.2=3.2mm.
Taking 10mm as a standard for the data wing and 20mm for the powers wings, we can implement (20-(5x0.5))/2=8.75mm power lines.



The total length is ~120mm per module, 1320mm for the 11 modules flex.
Total wing resistance is

$$Rwp = \frac{1320 \times 15.10^{-6}}{0.005 \times 11} = 0.45\Omega$$

- total resistance and power loss for 9 M4 modules + 2 M1 + 1 M2:

The total resistance is 1.85Ω.
So a power loss Pl=1.85x2.4²=10.7W and a voltage drop of 1.85x2.4=4.45V.
We will need a current source with a voltage ability about (10x1.7)+4.45=21.45V.

3-3-2 Powering layer for 20 M2:

The power consumption is equivalent to 10 M4 modules.

- Linear part of the main flex: the power lines are not covering the full length of the main flex but only the part for mountains: 1940-400=1540mm

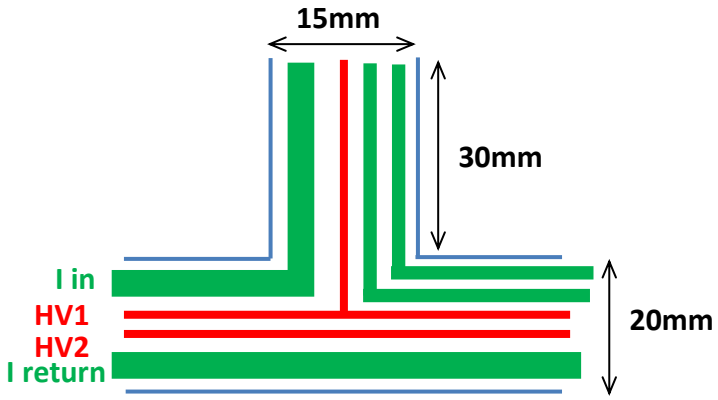
With 0.5mm tracks for HV and isolations, we can implement (20-(7x0.5))/2=8.25mm power lines.

The total round trip is 1540x2=3080mm, so the resistance is

$$Rlin = \frac{3080 \times 15.10^{-6}}{0.005 \times 8.25} = 1.1\Omega$$

- Wings for 20 M2: 30mm long; double with the module flex, so 60mm.

The total mountain wing width is 20mm. Data transmission will need 4 differential pairs + 1 track (cf. 4-4), so ~(4x0.5)+0.2=3.2mm.
Taking 5mm as a minimum for the data wing and 15mm for the powers wings, we can implement (15-(6x0.5))/2=6mm power lines (we neglect the isolation between the two associated modules lines).



The total length is ~120mm per module, 2400mm for the 14 modules flex.
Total wing resistance is

$$Rwp = \frac{2400 \times 15.10^{-6}}{0.005 \times 6} = 1.2\Omega$$

- total resistance and power loss for 20 M2:

The total resistance is 2.3Ω.
So a power loss Pl=2.3x2.4²=13.25W and a voltage drop of 2.3x2.4=5.5V.
We will need a current source with a voltage ability about (10x1.7)+5.5=22.5V.

Total power loss for the layer3:

The total power loss Pl=10.7+13.25≈**24W** and the efficiency is (80/80+24)*100=**77%.**

3-5 Serial powering conclusions.

For one stave:
Layer0: one flex power layer, 40W consumption, power loss Pl=8W; voltage drop 3.4V, current source voltage ability 20.4V.
Layer1: one flex power layer, 36W consumption, power loss Pl=9.7W; voltage drop 4V, current source voltage ability 19.3V.
Layer2: two flex power layers, 56W consumption, power loss Pl=16.1W.
- power loss Pl=6.9W; voltage drop 2.9V, current source voltage ability 14.8V.
- power loss Pl=9.2W; voltage drop 3.8V, current source voltage ability 15.7V.

Layer3: two flex power layers, 80W consumption, power loss Pl=24W.
- power loss Pl=10.7W; voltage drop 4.45V, current source voltage ability 21.45V.
- power loss Pl=13.25W; voltage drop 5.5V, current source voltage ability 22.5V.

For the full detector:
Layer0: 16 staves, 640W consumption, power loss Pl=128W.
Layer1: 32 staves, 1152W consumption, power loss Pl=310W.
Layer2: 64 staves, 3584W consumption, power loss Pl=1030W.
Layer3: 104 staves, 8320W consumption, power loss Pl=2496W.

So a total **13696W** consumption and **3964W** power loss.
Total efficiency: (13969/13969+3964)*100=**77.6%.**
An efficiency of about 78% should be a good result and corresponds to estimations [7].
All the presented calculations are based on estimated resistivity or power consumptions for future electronics. Nevertheless, numbers should allow to guide developments.

Current sources: the voltages abilities are from 15V to 22.5V. VIP boards should host the current sources and local standard power supplies should be 24V.

Power dissipation: the static simulations of the staves with the foreseen cooling show good results with power consumptions about 50% higher than calculated. Flexes should not be in contact with staves for contraction issues. We even though can assume that temperature should be homogenous in a steady-state.

4- Front-ends signals, counting and matter budget @320Mb/s.

We started the study with the FEI4 chip specifications in order to estimate the possible routing of signals and so their occupation:

- Only one FE control routed per module, whatever M4, M2 or transition module.
- Only one clock routed per module, whatever M4, M2 or transition module.
- The maximum foreseen data transmission rate is 320Mb/s. The total rate will be distributed in the necessary number of lines.
- A single track routed for MPC (cf.[8]) or later PSPP.
- Signals from the same module will not be routed on different flex layers.
- A differential pair occupancy width can be estimated to 500µm, including isolations.
- All tracks widths are estimated to 100µm.
- Coverlay's thickness is 50µm, bondply's thickness is 75µm, core polyimide thickness is 50µm, cooper layer thickness is 5µm.

We decided to use AC coupled differential pairs for all the signals: data, clocks, controls.
A specific AC coupled single track should be used for MPC. Will be noted ST (single Track). The M1 modules in transition regions will be treated as M2 modules because they will be implemented on the same flex module.
We don't foresee Hit_OR FEI4 signal and temperature sensor lines because we assumed that FE5 should include these features in the future.
Isolations will be noted I.
Radiation lengths are: **1.44cm** for copper and **28.6cm** for polyimide-resin.

- Matter budget and ground planes considerations:

We will calculate for each detector layer the number of needed copper layers. The matter budget should allow a maximum **2-3‰** energy loss.
For differential pairs impedance control, the best solution should be to implement reference layers between signals layers. If solid, these layers should represent an important amount of matter and should increase a lot the stiffness of the flex.
A solution is to hatch the plane, typically with 50% of copper occupancy.

- Rates of the different layers:

Data rates are **320Mb/s** on **layer0&1** and **160Mb/s** on **layers1&2**.
Implementing data multiplexing on layers2&3 would allow to standardize 320Mb/s.
Consequences: M2 & M1 modules should be different for these two layers. The number of pairs should be reduced, especially for layer3. Multiplexing 160Mb/s FEI4 signals has already been tested with success.

4-1 Layer0: 10M4, 320Mb/s differential pairs. See annex A.

- Counting:

The foreseen FE data rate for Layer0 is **1280Mb/s**.
One FE needs 1280/320=**4** data lines.
One M4 needs 4x4=16 data lines + 1 clock + 1 control + 1ST=**18 pairs + 1 ST**
For the full layer: **180 pairs + 10 ST**

The routing occupancy width of a module can be estimated to:
100µm*(I)*+(500µmx18)+100µm*(ST)*+100µm*(I)*=**9.3mm.**

On a flex layer, **2** modules can be distributed (18.6mm routing width).
The full data distribution needs **5** flex layers.
Powering needs **1** layer, so a total of **6** copper layers.

- Matter budget estimation with **6** layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=**400µm**,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
180pairs + 10ST ≈ **370** tracks, so a total **37mm** copper width.
20mm equivalent flex copper thickness: (37/20)x5µm=**9.25µm**
Powering layer 20mm equivalent copper thickness: (17.5/20)x5µm=**4.375µm**

So a total of ~**16.6µm** copper thickness, so a (16.6E-6/1.44E-2)=**1.15‰** energy loss.
Total energy loss on the flex: (16.6E-6/1.44E-2)+(400E-6/28.6E-2)=**2.55‰**.

Remark: the matter budget does not allow the addition of reference layers for impedance control. The layer0 rates are the most critical and so if we manage to transmit signals without reference layer, we will have no need to implement reference layers on others detector layers.

Conclusion: layer0 should be routed with **6** copper layers without reference.

4-2 Layer1: 5M4, 7M2, 2M1, 320Mb/s differential pairs. See annex B.

- Counting:

The foreseen FE data rate for Layer1 is **640Mb/s.**
One FE needs 640/320=**2** data lines.

M4: one M4 needs 2x4=8 data lines + 1 clock + 1 control + 1ST=**10 pairs + 1 ST**
For 5 M4: **50 pairs + 5 ST**

M2 & M1: one M2 needs 2x2=4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 7M2 + 2M1 ≈ 8M2: **48 pairs + 8 ST**

For the full layer: **98 pairs + 13 ST**

Powering needs **1** layer.
The routing occupancy width of a M4 can be estimated to:
100µm*(I)*+(500µmx10)+100µm*(ST)*+100µm*(I)*=**5.3mm.**

The routing occupancy width of a M2 can be estimated to:
100µm*(I)*+(500µmx6)+100µm*(ST)*+100µm*(I)*=**3.3mm.**

On the first flex layer, **3** M4 can be distributed (15.9mm).
On the second flex layer, **2** M4 + **2** M2can be distributed (17.2mm routing width).
The **6** remaining M2 could be distributed on a third layer (19.8mm routing width).

The full data distribution needs **3** flex layers.
Powering needs **1** layer, so a total of **4** copper layers.

- Matter budget estimation with **4** layers:

4 copper layers imply the use of **2** cores, **2** coverlays and **1** bondply.
Total polyimide+resin thickness of (2x50)+(1x75)+(2x50)=275µm,
so a (275E-6/28.6E-2)=**1‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
98pairs + 13ST ≈ **209** tracks, so a total 20.9mm copper width.
20mm equivalent flex copper thickness: (20.9/20)x5µm=**5.225µm**
Powering layer 20mm equivalent copper thickness: (17.5/20)x5µm=**4.375µm**

So a total of ~9.6µm copper thickness, so a (9.6E-6/1.44E-2)=**0.67‰** energy loss.
Total energy loss on the flex: (9.6E-6/1.44E-2)+(275E-6/28.6E-2)=**1.7‰**.

- Matter budget estimation with **6** layers:

Powering layer can be seen as a reference plane. Adding a core allows to implement 2 layers more.
6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=400µm,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.
We can estimate the 2 reference layers, 50% hatched to one full 200mm layer, so a **5µm** copper layer.
So finally, 20mm equivalent flex copper thickness: (20.9/20)x5µm+5µm=**10.225µm**
Powering layer 20mm equivalent copper thickness: (17.5/20)x5µm=**4.375µm**

So a total of ~14.6µm copper thickness, so a (14.6E-6/1.44E-2)=**1‰** energy loss.
Total energy loss on the flex: (14.6E-6/1.44E-2)+(400E-6/28.6E-2)=**2.4‰**.

Conclusion:
The use of 4 layers is determined by the estimated number of signals: the third layer is **19.8/20mm** occupied. Adding signals should imply to use 3 cores and so 6 layers.
As discussed in 4-1, if we manage to transmit signals without reference layer on layer0, we will have no need to implement reference layers on others detector layers.
The final solution should be chosen during the design.

4-3 Layer2: 7M4, 13M2, 2M1, 160Mb/s differential pairs. See annex C.

- Counting:

The foreseen FE data rate for Layer2 is **160Mb/s**.
One FE needs 1 data lines.

M4: one M4 needs 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 7 M4: **42 pairs + 7 ST**

M2 & M1: one M2 needs 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 13M2 + 2M1 ≈ 14M2: **56 pairs + 14 ST**

For the full layer: **98 pairs + 21 ST**

Remark: pairs could be saved if signals are multiplexed on the module up to 320Mb/s.

Powering needs **2** layers.
The routing occupancy width of a M4 can be estimated to:
100µm*(I)*+(500µmx6)+100µm*(ST)*+100µm*(I)*=**3.3mm.**

The routing occupancy width of a M2 can be estimated to:
100µm*(I)*+(500µmx4)+100µm*(ST)*+100µm*(I)*=**2.3mm.**

On the first flex layer, **6** M4 can be distributed (19.8mm routing width).
On the second flex layer, **1** M4 + **6** M2 can be distributed (17.1mm routing width).
The **8** remaining M2 could be distributed on a third layer (18.4mm routing width).

The full data distribution needs **3** flex layers and powering needs **2** layer, so a total of **5** copper layers. Because of double-faced cores, we will implement **6** layers.
This sixth layer can be used for reference layer or to distribute signals.
As for layer1, the use of 4 layers is determined by the estimated number of signals. Adding signals should imply to use 6 layers for signals. The final solution should be chosen during the design.

- Matter budget estimation with **6** signals layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=400µm,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
98pairs + 21ST ≈ **217** tracks, so a total 21.7mm copper width.
20mm equivalent flex copper thickness: (21.7/20)x5µm=**5.425µm**
2 powering layers 20mm equivalent copper thickness: (36/20)x5µm=**9µm**
So a total of ~14.5µm copper thickness, so a (14.5E-6/1.44E-2)=**1‰** energy loss.
Total energy loss on the flex: (14.5E-6/1.44E-2)+(400E-6/28.6E-2)=**2.39‰**.

- Matter budget estimation with **5** signals layers + **1** reference layer:

The 50% hatched layer should represent a 2.5µm thick equivalent 20mm solid layer, a loss about (2.5E-6/1.44E-2)=**0.17‰**
So a total energy loss on the flex: **2.56‰**.

- Matter budget estimation with multiplexed data:

M4: one M4 needs 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 7 M4: **28 pairs + 7 ST**

M2 & M1: one M2 needs 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 13M2 + 2M1 ≈ 14M2: **42 pairs + 14 ST**

For the full layer: **70 pairs + 21 ST.**
The routing occupancy width of a M4 can be estimated to:
100µm(I)+(500µmx4)+100µm(ST)+100µm(I)=**2.3mm**.

The routing occupancy width of a M2 can be estimated to:
100µm(I)+(500µmx3)+100µm(ST)+100µm(I)=**1.8mm**.

The total width is (7x2.3)+(14x1.8)=**41.3mm**. We will need more than 2 copper layers for all the signals. Multiplexing layer2 signals allows to reduce the matter but not to introduce reference layers and not to implement only 4 flex layers.
Conclusion:

As discussed in 4-1, if we manage to transmit signals without reference layer on layer0, we will have no need to implement reference layers on others detector layers. The final solution should be chosen during the design.

4-4 Layer3: 9M4, 21M2, 2M1, 160Mb/s differential pairs. See annex D.

- Counting:

The foreseen FE data rate for Layer3 is **160Mb/s.**
One FE needs 1 data lines.

M4: one M4 needs 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 9 M4: **54 pairs + 9 ST**

M2 & M1: one M2 needs 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 21M2 + 2M1 ≈ 22M2: **88 pairs + 22 ST**

For the full layer: **142 pairs + 31 ST**

Powering needs **2** layers.
The routing occupancy width of a M4 can be estimated to:
100µm*(I)*+(500µmx6)+100µm*(ST)*+100µm*(I)*=**3.3mm.**

The routing occupancy width of a M2 can be estimated to:
100µm*(I)*+(500µmx4)+100µm*(ST)*+100µm*(I)*=**2.3mm.**

The total width is (9x3.3)+(22x2.3)=**80.3mm.**

We can see that it is impossible to distribute 160Mb/s differential pairs over four 20mm layers. Two solutions can be considered: the use of 8 layers-4 cores or the multiplexing on 6 layers-3 cores.

- 8 layers distribution:

The FE data rate is **160Mb/s**.
One FE needs 1 data lines.
Even with 6 signal layers, we will not be able to introduce 2 reference layers.
Several distributions over 5 or 6 layers can be tested.
8 copper layers imply the use of **4** cores, **2** coverlays and **3** bondplys.
Total polyimide+resin thickness of (2x50)+(3x75)+(4x50)=525µm,
so a (525E-6/28.6E-2)=**1.85‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
142pairs + 31ST ≈ **315** tracks, so a total 31.5mm copper width.
20mm equivalent flex copper thickness: (31.5/20)x5µm=**7.875µm**
2 powering layers 20mm equivalent copper thickness: (35/20)x5µm=**8.75µm**

So a total of ~16.6µm copper thickness, so a (16.6E-6/1.44E-2)=**1.15‰** energy loss.
Total energy loss on the flex: (16.6E-6/1.44E-2)+(525E-6/28.6E-2)=**3‰**.
The foreseen loss represents the maximum specification.
Even with 8 layers, we will not be able to add reference planes.

- 6 layers multiplexed distribution:

The FE data rate is **320Mb/s**.
Two FE needs 1 data lines.

M4: one M4 needs 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 9 M4: **36 pairs + 9 ST**

M2 & M1: one M2 needs 1 data lines + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 21M2 + 2M1 ≈ 22M2: **66 pairs + 22 ST**

For the full layer: **102 pairs + 31 ST**

The routing occupancy width of a M4 can be estimated to:
100µm*(I)*+(500µmx4)+100µm*(ST)*+100µm*(I)*=**2.3mm.**

The routing occupancy width of a M2 can be estimated to:
100µm*(I)*+(500µmx3)+100µm*(ST)*+100µm*(I)*=**1.8mm.**

The total width is (9x2.3)+(22x1.8)=**60.3mm.**

On the first flex layer, **7** M4 can be distributed (16.1mm routing width).
On the second flex layer, **2** M4 + **6** M2 can be distributed (15.4mm routing width).
On the third and fourth flex layers, **8** M2 can be distributed (14.4mm routing width).

- Matter budget estimation with **6** signals layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=400µm,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
102pairs + 31ST ≈ **235** tracks, so a total 23.5mm copper width.
20mm equivalent flex copper thickness: (23.5/20)x5µm=**5.875µm**
2 powering layers 20mm equivalent copper thickness: (35/20)x5µm=**8.75µm**

So a total of ~14.6µm copper thickness, so a (14.6E-6/1.44E-2)=**1‰** energy loss.
Total energy loss on the flex: (16.6E-6/1.44E-2)+(400E-6/28.6E-2)=**2.39‰**.

Conclusion:
In order to save matter budget, the better solution should be to implement multiplexing over 6 layers. The final solution should be chosen during the design.

4-5 Conclusions and remarks on signals layers.

We can notice that the major losses are in polyimide, typically **1.4%** for a 6 layers flex. Different prototypes will have to be tested in order to compare multiplexed solutions with higher rates (and possible reference planes) and lower rates.
GBT probably will evolve to LP-GBT with 640Ms/s to 1Gs/s rates. It will reduce the number of lines and reference planes could be implemented. Tests will show if higher rates are possible in this configuration.
Critical layers are layers0&3 with high numbers of signals.
We did not fix any specifications and constrains on wings matter budget and connectors. It will be discussed in the future.
The proposed solutions will evolve with the layout: an introduction of end cap detectors would allow a number of signals reduction by a shortening of the staves.
The most critical issue is the data transmission and the work will focus on the impedance control.

4-6 Impedance matching and flex module considerations

First simulations show that we should have very different characteristic impedances depending on the flex layers.
Implementing reference layers also shows that characteristic impedance can be fixed but always differ from 100Ω because of topology. We saw that most of the time, it is impossible to implement reference layers because of the high number of signals.
The solution could be to tune the reception impedances. A standard way should to implement the tuned resistors on the module. The drawback is that we should produce a lot of different modules. The second way is to implement resistors on the wing, just before connection. It should be a drawback in term of matching but the way to standardize the flex modules.

Modules of a same type (M4,M2) need different numbers of differential pairs depending on the different detector layers.
Because of feasibility on a large number of modules, we should design three standard modules. The connectors should be chosen with the most constraining modules specifications. Data and powers connectors could be different from M4 to M2 modules. Data connector should be partially occupied on external layers.
Two solutions are possible for powers connectors:

- Using the minimum number of pins, current dimensioned. Connector should be large.
- Using several pins for currents and HV. Connector should be smaller but isolation should be lower between pins.

Module standardization implies also a standardized wing width distribution between powers and data.

5- Front-ends signals, counting and matter budget @640Mb/s.

The previous calculations using 320Mb/s rates showed that the high number of signals avoid the implementation of reference planes and so a standardized impedance matching.
We should be able to implement plated holes on wings because of the use of a single core but having all the layers signals on the connector side should be easier to produce.
As GBT is foreseen to evolve to LP-GBT with e-links rates up to 640Mb/s, it is interesting to estimate the corresponding occupancy of the signals and the possibility to implement reference planes.
We foresaw the production of prototypes in order to test the process and the data rates. This prototype will include the standard 320Mb/s architecture and the 640Mb/s one. The tests will show if the higher rate is possible.
Reference planes are usually 50% cross-hatched for flexibility.

5-1 Layer0: 10M4, 640Mb/s differential pairs. See annex A.

- Counting:

The foreseen FE data rate for Layer0 is **1280Mb/s**.
One FE needs 1280/640=**2** data lines.
One M4 needs 4x2=8 data lines + 1 clock + 1 control + 1ST=**10 pairs + 1 ST**
For the full layer: **100 pairs + 10 ST**

The routing occupancy width of a module can be estimated to:
100µm*(I)*+(500µmx10)+100µm*(ST)* =**5.2mm.**

On a flex layer, **3** modules can be distributed (15.6mm routing width).
The full data distribution needs **4** flex layers.

- Matter budget estimation with **6** layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=**400µm**,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
100pairs + 10ST ≈ **210** tracks, so a total **21mm** copper width.
20mm equivalent flex copper thickness: (21/20)x5µm=**5.25µm**
Powering layer 20mm equivalent copper thickness: (17.5/20)x5µm=**4.375µm**

So a total of ~**9.625µm** copper thickness, so a (16.6E-6/1.44E-2)=**0.67‰** energy loss.
Total energy loss on the flex: **2.06‰**.

We could route 4 modules signals on one layer in order to include reference planes between signals layers: etching should be reduced to **~96µm** or the main flex width should be increased to **21mm**. Both solutions are possible.
Finally, the possible stack-up :

Layer#1: 1 power line + 2 HV lines.
Layer#2: 4xM4.
Layer#3: reference.
Layer#4: 3xM4.
Layer#5: reference.
Layer#6: 3xM4.

We can estimate the 2 reference layers loss: 50% hatched, so a **5µm** copper layer, so a (5E-6/1.44E-2)= **0.35‰** energy loss.
Finally the total loss should be 2.06+0.35=**2.41‰** which is a good result.
Remark: we can notice that it will be impossible to avoid plated holes on wings.

5-2 Layer1: 5M4, 7M2, 2M1, 640Mb/s differential pairs. See annex B.

- Counting:

The foreseen FE data rate for Layer1 is **640Mb/s.**
One FE needs **1** data line.

M4: one M4 needs 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 5 M4: **30 pairs + 5 ST**

M2 & M1: one M2 needs 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 7M2 + 2M1 ≈ 8M2: **32 pairs + 8 ST**

For the full layer: **62 pairs + 13 ST**

Powering needs **1** layer.
The routing occupancy width of a M4 can be estimated to:
100µm*(I)*+(500µmx6)+100µm*(ST)*+100µm*(I)*=**3.3mm.**

The routing occupancy width of a M2 can be estimated to:
100µm*(I)*+(500µmx6)+100µm*(ST)*+100µm*(I)*=**2.3mm.**

On the first flex layer, **5** M4 can be distributed (16.5mm).
On the second flex layer, **2** M1 + **7** M2 can be distributed (18.4mm routing width).
We can implement 3 reference planes so:

Layer#1: 1 power line + 2 HV lines.
Layer#2: reference.
Layer#3: 5xM4.

Layer#4: reference.
Layer#5: 2xM1+7xM2.
Layer#6: reference.
Remark: we can notice that it will be possible to avoid plated holes on wings.

- Matter budget estimation with **6** layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=400µm,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.
We can estimate the copper thickness on a 20mm equivalent solid layer:
62pairs + 13ST ≈ **137** tracks, so a total 13.7mm copper width.
20mm equivalent flex copper thickness: (13.7/20)x5µm=**3.425µm**
Powering layer 20mm equivalent copper thickness: (17.5/20)x5µm=**4.375µm**

So a total of ~7.8µm copper thickness, so a (7.8E-6/1.44E-2)=**0.54‰** energy loss.
Total energy loss on the flex: **1.93‰**.
We can estimate the 3 reference layers loss: 50% hatched, so a **7.5µm** copper layer, so a (7.5E-6/1.44E-2)=**0.52‰** energy loss.

Total energy loss on the flex: **2.45‰,** which is a good result.

5-3 Layer2: 7M4, 13M2, 2M1, 640Mb/s & 320Mb/s differential pairs. See annex C.

- Counting:

The foreseen FE data rate for Layer2 is **160Mb/s**.
Multiplexing data on modules allows to reduce the number of data lines: four M4 FE's could be multiplexed (640Mb/s) and two M2 FE's (320Mb/s).

M4: one M4 needs 1 data lines + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 7 M4: **21 pairs + 7 ST**

M2 & M1: one M2 needs 1 data lines + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 13M2 + 2M1 ≈ 14M2: **42 pairs + 14 ST**

For the full layer: **63 pairs + 21 ST**

Powering needs **2** layers.
The routing occupancy width of a M4 or M2 can be estimated to:
100µm*(I)*+(500µmx3)+100µm*(ST)*+100µm*(I)*=**1.8mm.**

The total equivalent 21 modules can be distributed on three flex layers:

Layer#1: 1 power line + 1 HV lines.
Layer#2: 7xM4
Layer#3: 1 power line + 1 HV lines.
Layer#4: 2xM1 + 6xM2.
Layer#5: reference.
Layer#6: 7xM2.

For the three data layers 7 modules are distributed, so 12.6mm routing width.

Remark: we can notice that it will be impossible to avoid plated holes on wings.

- Matter budget estimation with **6** signals layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=400µm,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
63pairs + 21ST ≈ **147**tracks, so a total 14.7mm copper width.
20mm equivalent flex copper thickness: (14.7/20)x5µm=**3.675µm**
2 powering layers 20mm equivalent copper thickness: (36/20)x5µm=**9µm**
So a total of 12.7µm copper thickness, so a (12.7E-6/1.44E-2)=**0.88‰** energy loss.
Energy loss on the flex: **2.27‰**.

We can estimate the reference layers loss: 50% hatched, so a **2.5µm** copper layer, so a (2.5E-6/1.44E-2)= **0.175‰** energy loss.

Total energy loss on the flex: **2.45‰,** which is a good result.

5-4 Layer3: 9M4, 21M2, 2M1, 640Mb/s & 320Mb/s differential pairs. See annex D.

- Counting:

The foreseen FE data rate for Layer3 is **160Mb/s**.
Multiplexing data on modules allows to reduce the number of data lines: four M4 FE's could be multiplexed (640Mb/s) and two M2 FE's (320Mb/s).

M4: one M4 needs 1 data lines + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 9 M4: **27 pairs + 9 ST**

M2 & M1: one M2 needs 1 data lines + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 21M2 + 2M1 ≈ 22M2: **66 pairs + 22 ST**

For the full layer: **93 pairs + 31 ST**

Powering needs **2** layers.
The routing occupancy width of a M4 or M2 can be estimated to:
100µm*(I)*+(500µmx3)+100µm*(ST)*+100µm*(I)*=**1.8mm.**

On the first flex layer, **9** M4 + **2** M1 + **1** M2 (≈11 modules) can be distributed (19.8mm routing width).
On the second flex layer, **10** M2 can be distributed (18mm routing width).
On the third flex layer, **10** M2 can be distributed (18mm routing width).

We can implement 1 reference plane so:

Layer#1: 1 power line + 2 HV lines.
Layer#2: 9xM4 + 2xM1 + 1xM2.
Layer#3: 1 power line + 2 HV lines.
Layer#4: 10xM2.
Layer#5: reference.
Layer#6: 10xM2.

Remark: we can notice that it will be impossible to avoid plated holes on wings.

- Matter budget estimation with **6** signals layers:

6 copper layers imply the use of **3** cores, **2** coverlays and **2** bondplys.
Total polyimide+resin thickness of (2x50)+(2x75)+(3x50)=400µm,
so a (400E-6/28.6E-2)=**1.39‰** energy loss.

We can estimate the copper thickness on a 20mm equivalent solid layer:
93pairs + 31ST ≈ **217**tracks, so a total 21.7mm copper width.
20mm equivalent flex copper thickness: (21.7/20)x5µm=**5.425µm**
2 powering layers 20mm equivalent copper thickness: (36/20)x5µm=**9µm**
So a total of ~14.43µm copper thickness, so a (14.43E-6/1.44E-2)=**1‰** energy loss.
Energy loss on the flex: **2.39‰**.

We can estimate the reference layers loss: 50% hatched, so a **2.5µm** copper layer, so a (2.5E-6/1.44E-2)= **0.175‰** energy loss.

Total energy loss on the flex: **2.57‰,** which is a good result.

5-5 Conclusions and remarks on 640Mb/s rates.

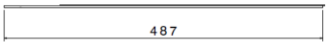
Whatever the detector layer, we can see that reference planes could be implemented in the stack up in order to better match impedances.
We can notice that the losses match always the specifications.
Plated holes on wings will not be avoided.
Tests on comparative prototypes will allow to define the possible transmissions and so the possible FE in-out stages.

6- Conclusions and perspectives.

We estimated the feasibility of the modules read-out for the four layers of the Alpine Staves layout. We show in this study that serial powering and 6 copper layers should be mandatory. Data transmission should be the critical issue and tests in the future should determine what rate should be possible.
We plan to design a first prototype in a snake configuration that allows to compare the two solutions (320Mb/s or 640Mb/s).

Annex A: Detector layer0.

Stave length **487mm**
8 staves for the half detector (φ=2π), total: **16** staves for the full detector.
Total detector: **160 M4, 640 FE**.
Total data rate: **819.2Gb/s.**



One stave:
10 M4; I=2.4A; P≈40W.
Flex length: **1370mm.**
1 FE data rate: **1280Mb/s**.

- ***320Mb/s lines:***
  4 data lines **@320Mb/s** per FE.
  For 1 M4: 16 data lines + 1 clock + 1 control + 1ST=**18 pairs + 1 ST.**
  For the full layer: **180 pairs + 10 ST.**

6 layers distribution:
Layer#1: 1 power line + 2 HV lines.
Layer#2: 2xM4.
Layer#3: 2xM4.
Layer#4: 2xM4.
Layer#5: 2xM4.
Layer#6: 2xM4.

Total energy loss: **2.55‰**.

- ***640Mb/s lines:***
  2 data lines **@640Mb/s** per FE.
  For 1 M4: 8 data lines + 1 clock + 1 control + 1ST=**10 pairs + 1 ST.**
  For the full layer: **100 pairs + 10 ST.**

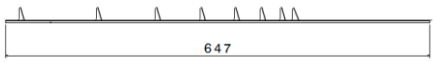
Layer#1: 1 power line + 2 HV lines.
Layer#2: 4xM4.
Layer#3: reference.
Layer#4: 3xM4.
Layer#5: reference.
Layer#6: 3xM4.

Total energy loss: **2.41‰**.

Power loss: **8W.**
Voltage drop **3.4V.**
Current source voltage ability: **20.4V.**
Serial powering efficiency: **83.3%.**

Annex B: Detector layer1.

Stave length **647mm**
16 staves for the half detector (φ=2π), total: **32** staves for the full detector.
Total detector: **160 M4, 64 M1, 224M2, 1152 FE**.
Total data rate: **737.3Gb/s**.



One stave:
5 M4 + 2 M1 + 7M2 ≈ ***9 M4***.
I=2.4A; P≈36W.
Flex length: **1370mm.**
1 FE data rate: **640Mb/s.**

- ***320Mb/s lines:***

2 data line **@320Mb/s** per FE.
For 1 M4: 8 data lines + 1 clock + 1 control + 1ST=**10 pairs + 1 ST**
For 5 M4: **50 pairs + 5 ST**
For 1 M2: 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 7M2 + 2M1 ≈ 8M2: **48 pairs + 8 ST**
For the full layer: **98 pairs + 13 ST**

4 or 6 layers distribution:
Layer#1: 1 power line + 2 HV lines.
Layer#2 to layer#4 or layer#6: to be designed.
Total energy loss: 4 layers **1.7‰;** 6 layers **2.4‰**.

- ***640Mb/s lines:***

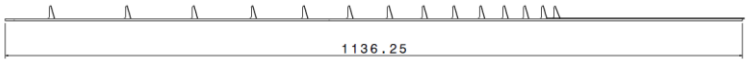
1 data line **@640Mb/s** per FE.
For 1 M4: 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 5 M4: **30 pairs + 5 ST**
For 1 M2: 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 7M2 + 2M1 ≈ 8M2: **32 pairs + 8 ST**
For the full layer: **62 pairs + 13 ST**

6 layers distribution:
Layer#1: 1 power line + 2 HV lines.
Layer#2: reference.
Layer#3: 5xM4.
Layer#4: reference.
Layer#5: 2xM1+7xM2.
Layer#6: reference.
Total energy loss: **2.45‰**.

Power loss: **9.7W.**
Voltage drop **3.95V.**
Current source voltage ability: **19.3V.**
Serial powering efficiency: **79%.**

Annex C: Detector layer2.

Stave length **1136.25**mm
32 staves for the half detector (φ=2π), total: **64** staves for the full detector.
Total detector: **448 M4, 128 M1, 832 M2, 3584 FE**.
Total data rate: **573.4Gb/s**.



One stave:
7 M4 + 2 M1 + 13M2 ≈ ***14 M4***.
I=2.4A; P≈56W.
Flex length: **1370mm.**
1 FE data rate: **160Mb/s.**

- ***160-320Mb/s lines:***

Non-multiplexed data:
1 data line **@160Mb/s** per FE.
For 1 M4: 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 7 M4: **42 pairs + 7 ST**
For 1 M2: 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 13M2 + 2M1 ≈ 14M2: **56 pairs + 14 ST**
For the full layer: **98 pairs + 21 ST**

Multiplexed data:
1 data line **@320Mb/s** for two FE.
For 1 M4: 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 7 M4: **28 pairs + 7 ST**
For 1 M2: 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 13M2 + 2M1 ≈ 14M2: **42 pairs + 14 ST**
For the full layer: **70 pairs + 21 ST.**

6 layers distribution:
Layer#1: 1 power line + 1 HV lines.
Layer#2: 1 power line + 1 HV lines.
Layer#3 to layer#6: to be designed.
Total energy loss 6 layers signals: **2.4‰**.

- ***640Mb/s lines:***

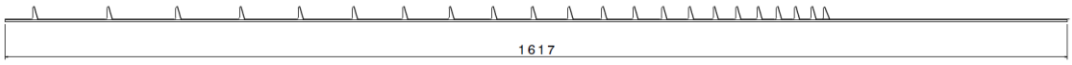
M4: **1** data line **@640Mb/s** for four FE.
For 1 M4: 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 7 M4: **21 pairs + 7 ST**
M2: **1** data line **@320Mb/s** for two FE.
For 1 M2: 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 13M2 + 2M1 ≈ 14M2: **42 pairs + 14 ST**
For the full layer: **63 pairs + 21 ST.**

6 layers distribution:
Layer#1: 1 power line + 1 HV lines.
Layer#2: 7xM4
Layer#3: 1 power line + 1 HV lines.
Layer#4: 2xM1 + 6xM2.
Layer#5: reference.
Layer#6: 7xM2.
Total energy loss: **2.45‰**.

Power loss: **16.1W.**
Voltage drop: power layer#1 **2.9V**, power layer#2 **3.85V.**
Current source voltage ability: layer#1 **14.8V**, layer#2 **15.7V.**
Serial powering efficiency **78%.**

Annex D: Detector layer3.

Stave length **1617mm**;
52 staves for the half detector (φ=2π), total: **104** staves for the full detector.
Total detector: **936 M4, 208 M1, 2184 M2, 8320 FE**.
Total data rate: **1331.2Gb/s**.



One stave:
9 M4 + 2 M1 + 21M2 ≈ ***20 M4***.
I=2.4A; P≈80W.
Flex length: **1940mm.**
1 FE data rate: **160Mb/s**

- ***160-320Mb/s lines:***

Non-multiplexed data: 8 layers
1 data line **@160Mb/s** per FE.
For 1 M4: 4 data lines + 1 clock + 1 control + 1ST=**6 pairs + 1 ST**
For 9 M4: **54 pairs + 9 ST**
For 1 M2: 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 21M2 + 2M1 ≈ 22M2: **88 pairs + 22 ST**
For the full layer: **142 pairs + 31 ST**

Multiplexed data: 6 layers
1 data line **@320Mb/s** for two FE.
For 1 M4: 2 data lines + 1 clock + 1 control + 1ST=**4 pairs + 1 ST**
For 9 M4: **36 pairs + 9 ST**
For 1 M2: 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 21M2 + 2M1 ≈ 22M2: **66 pairs + 22 ST**
For the full layer: **102 pairs + 31 ST**

6 or 8 layers distribution:
Layer#1: 1 power line + 2 HV lines.
Layer#2: 1 power line + 2 HV lines.
Layer#3 to layer#6 or layer#8: to be designed.
Total energy loss: 6 layers **2.4‰;** 8 layers **3‰**.

- ***640Mb/s lines:***

M4: **1** data line **@640Mb/s** for four FE.
For 1 M4: 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 9 M4: **27 pairs + 9 ST**
M2: **1** data line **@320Mb/s** for two FE.
For 1 M2: 1 data line + 1 clock + 1 control + 1ST=**3 pairs + 1 ST**
For 21M2 + 2M1 ≈ 22M2: **66 pairs + 22 ST**
For the full layer: **93 pairs + 31 ST.**

6 layers distribution:
Layer#1: 1 power line + 2 HV lines.
Layer#2: 9xM4 + 2xM1 + 1xM2.
Layer#3: 1 power line + 2 HV lines.
Layer#4: 10xM2.
Layer#5: reference.
Layer#6: 10xM2.
Total energy loss: **2.57‰**.

Power loss: **24W.**
Voltage drop: power layer#1 **4.45V**, power layer#2 **5.5V.**
Current source voltage ability: power layer#1 **21.45V**, power layer#2 **22.5V.**
Serial powering efficiency **77%.**

References:

[1] Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment.
http://cds.cern.ch/record/1502664?ln=fr

[2] ATLAS Insertable B-Layer Technical Design Report.
https://cds.cern.ch/record/1291633/

[3] The FE-I4A Integrated Circuit Guide.
fei4 link

[4] Versatile link project.
https://espace.cern.ch/project-versatile-link/public/default.aspx

[5] Bandwidths of micro twisted-pair cables and fusion spliced SIMM-GRIN fiber and radiation hardness of PIN/VCSEL arrays.
http://www.sciencedirect.com/science/article/pii/S0920563207005890#

[6] GBT project.
https://espace.cern.ch/GBT-Project/default.aspx

[7] System implications of the different powering distributions for the ATLAS Upgrade strips tracker.
https://indico.cern.ch/event/102998/session/22/contribution/275

[8] A serial powering scheme for the ATLAS pixel
detector at sLHC.
http://iopscience.iop.org/1748-0221/5/12/C12002?fromSearchPage=true