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Preference for oral presentation

Evidence of relationship between mechanical stress and leakage current in AlGaN/GaN transistor after storage test

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Abstract

In this paper, leakage current signatures in AlGaN HEMT are studied after storage at 300°C. By comparing gate pad topology and by localized FIB cuts, Optical Beam Induce Resistance Change (OBIRCh) analysis was used to localize current path. Results tend to indicate that mechanical stresses in the gate structure strongly influences the leakage current of the transistor. Electrical characterization of the gate to source diode over temperatures supports the discrimination of the conduction mechanisms like thermionic field emission, Fowler-Nordheim or Poole-Frenkel. The OBIRCh analysis technique, widely used in silicon technology, appears to be a very efficient tool to localize leakage paths, in particular for HEMT topology with source terminated field plate.

1. Introduction

AlGaN/GaN-HEMTs have emerged as very attractive candidates with promising device performances and reliability for next generation mobile communications applications due to improvement in processing technology and epitaxial growth [1]. However to further improve the long-term stability of these devices, the reduction of drain and gate leakage currents are required.

There are several leakage paths identified in the HEMT mainly related to electrons injected via tunneling mechanisms at high gate-drain voltage operation. As electron transport in this device is also coupled with traps or surface states interaction, polarization and piezoelectric effects, the identification of the preeminent leakage path is still challenging [2].

For this reason, an electrical and physical failure analysis flow has been implemented to understand the mechanisms affecting the leakage currents of AlGaN/GaN HEMTs during long-term life tests.

2. Device and technology description [3]

The devices were fabricated on a 3 inch SiC substrate. The epitaxial structure is composed of an AlN buffer layer, an undoped GaN layer and an undoped AlGaN barrier layer capped with unintentionally doped GaN. A 0.5µm Ni/Au based gate is formed using E-Beam lithography. The ohmic contacts are Ti/Al/Ni/Au/Ti/Pt evaporated stacks. A source terminated field plate covers the gate finger.

The 100µm gate width HEMT structures under test in this study present two different topologies referenced as M13 and M33. This difference is related to the interconnection layout between the gate bus and the pad as described in Fig. 1. Indeed, compared to the M13 pattern, the M33 structure presents an additional gate head metal as pad-to-gate bus gold metal interconnection (not shown in Fig. 1).

3. Storage test description and electrical parameter drift

The devices under test have sustained storage at 300°C. While no significant drift is observed on DC parameters like the threshold voltage (V_{th}) or the drain saturation current (I_{dss}), a large increase of the subthreshold drain leakage current (measured @ V_{DS}=50V, V_{GS}=-7V) after the 1000 hours storage test is observed for the M13 structure (Fig. 2). A similar evolution is observed on the reverse gate current under the same biasing condition [3].

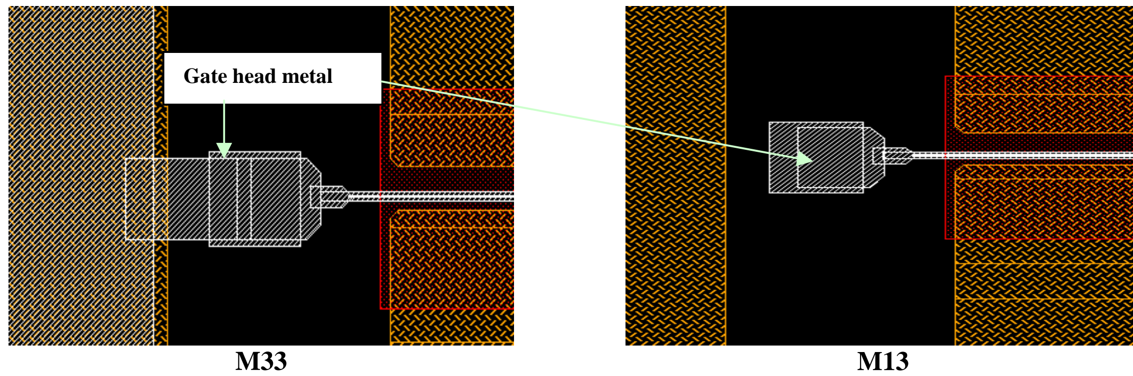


Fig. 1: Layout showing the difference in the gate bus / pad interconnection topology of the M13 and M33 test structures (the gold metal interconnection layer is not represented in these schematic)

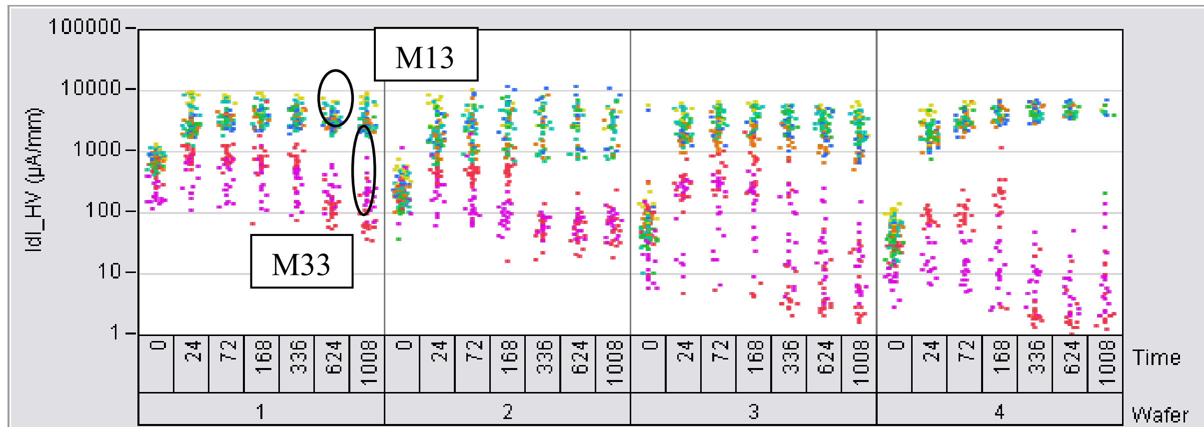


Fig. 2: Evolution of the drain leakage current (measured @ V_{DS}=50V, V_{GS}=-7V) for M33 and M13 test structures (of 4 different wafers) after a storage test at 300°C up to 1000 hours

This increase of the drain leakage current is characterized by a rapid evolution within the first 24 hours of the storage test followed by stabilization.
On the contrary to the M13 test structures, the M33 test structures exhibited an evolution of the subthreshold current of less than one decade.

4. Physical characterization

A failure analysis flow has been carried out to localize the root cause of this phenomenon. The assumption built up along the analysis was to explain that the leakage currents are induced by some mechanical stresses in the devices. Indeed, the different gate interconnection topologies may induce a difference in the mechanical stress in the gate metal deposited onto the semiconductor. Thus, the defined analysis flow was focused to validate this assumption. Meanwhile, evidence of any other root cause was considered.

The first part of the study was dedicated to electrically isolate the origin of the leakage on the M13 HEMT structure, which may be located in the active area of the transistor or at the gate pad. Then, near infra-red (NIR) emission microscopy and the OBIRCh technique were used to localize potential defects in the structure possibly linked to leakage current paths. As the source terminated field plate is covering the gate area, emission microscopy was proved to be inefficient [4].

Therefore, the OBIRCh technique was implemented to detect resistive leakage paths in the structure. It consists in locally heating the HEMT sample under biasing by means of a 1340 nm laser and record the subsequent modification of the sample local resistance. The localization is performed by synchronizing the laser displacement over the sample and the electrical detection. The spatial resolution is close to the 1µm spot diameter. Laser stimulation highlights differences in thermal characteristics between regions with defects and regions which are defect-free. When the laser locally heats a defective region on a metal line which is carrying a current, the resulting resistance change is detected by monitoring the input current to the device.

OBIRCh analyses have been performed in three different wafer sites on M33 structures, on reference M13 structures and M13 ones modified by FIB as described below. The first result is that the M33 structures do not present any OBIRCh signature which can be explained by their low drain and gate leakage currents.

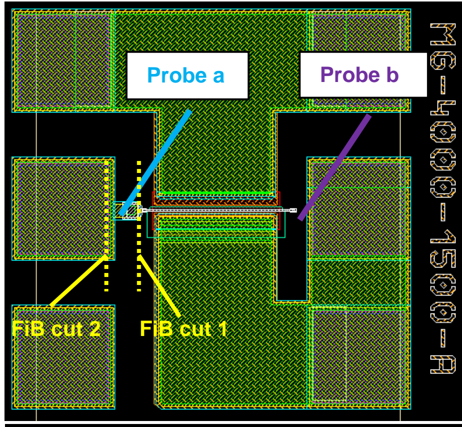


Fig. 3: Layout of the M13 structure
Location of the two different FIB cuts and contact probe sites for electrical measurements

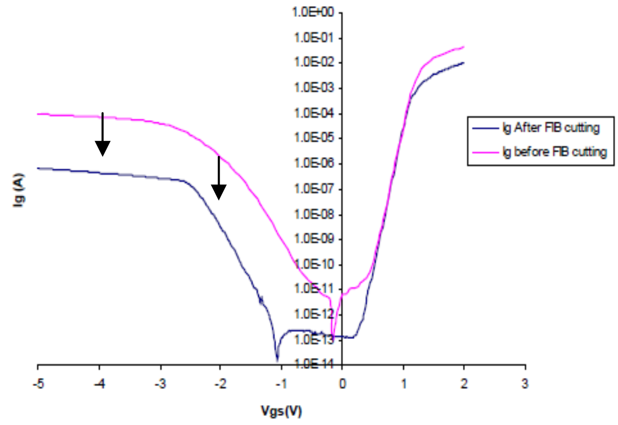
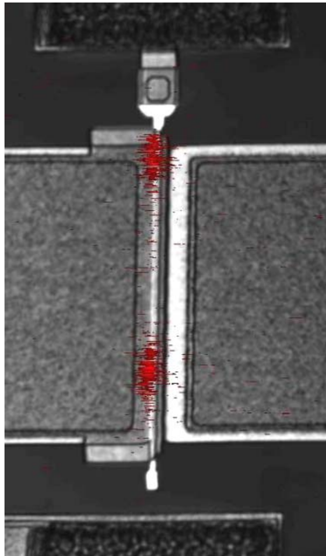


Fig. 4: I_g-V_{gs} characteristics of the gate to source diode in M13 structure before (pink) and after (blue) FIB cut 1



M13-site R85 X50, Before FIB 1 cut
Contact probe on the gate pad
V_{GS} = -4.89V, I_G = 12.4µA
2 local spots are detected inside the active area

M13-site R85, X50, After F1B 1 cut
Contact probe at the end of the gate finger
V_{GS} = -4.89V, I_G = 420 nA
1 local spot detected and shifted towards the biasing location

Fig. 5: OBIRCh signature modification of the M13 structure by FIB cut (laser power 130mW, 8 frames integration)

On the M13 structure, the gate interconnection was cut by FIB in two different sites (Fig.3) to isolate the location of the leakage path and the gate current was measured hereafter on wafer. This simple modification of the device under test was then validated by comparing the gate current characteristics with the contact probe placed on the gate pad (Probe a) or at the end of the gate metallization (Probe b).

Whatever the position 1 or 2 of the FIB cut, leakage path has been localized in the active area of the device and not at the pad level. A significant decrease of the gate leakage current (Fig.4) was also observed on the isolated M13 HEMT by the FIB cut 1 between the gate interconnect and the gate metallization. The reverse gate current recovers its level measured before the storage test. On the contrary, the FIB cut 2 between the gate interconnect and the pad had no effect. This experiment has been repeated on three different sites of the wafer leading to the same result.

It was then assumed that the FIB cut 1 reduced the leakage current because of mechanical stress modification on the gate contact. It is why OBIRCh signatures obtained before and after different FIB cuts of the gate interconnect level were compared. For the FIB cut 2, the OBIRCh signature is not modified if the contact probe is placed on the gate interconnect (Probe a). This result is in agreement with the electrical measurement as no gate current decrease was observed in this case.

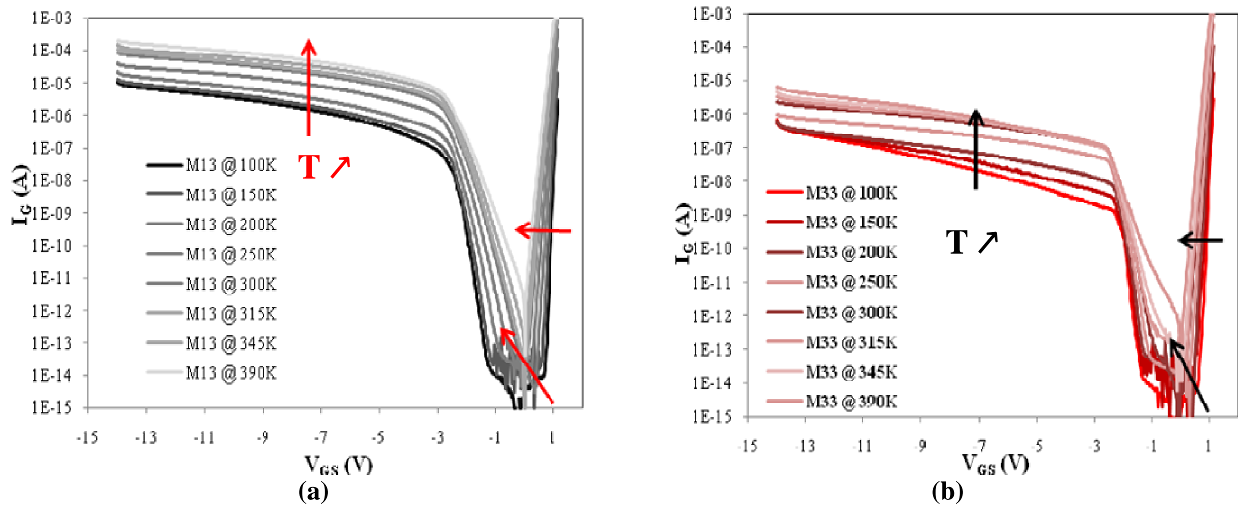


Figure 6: $I_G(V_{GS})$ measurements carried out at different temperatures
for two types of gate pad topology : (a) "leaky" M13 and (b) "non leaky" M33 HEMT structures

On the contrary, the OBIRCh signature of the modified M13 structure with the FIB cut 1 has changed (Fig. 5). The spot located at the beginning of the gate disappeared with the decrease of the leakage current and the other spot shifted to the end of the gate metallization. This clearly demonstrates that the leakage path is changed by modifying the mechanical stress in the structure. This change of the mechanical stress is assumed to be induced by cutting the gate metallization, by the pressure of the contact probe when it is placed at the end of the gate finger (Probe b), and also by a possible relaxation of the stress in the passivation layer [5].

5. Electrical characterization

Electrical characterization was carried out aiming to identify the conduction mechanisms taking place in the structure which contribute to the gate leakage current. So, I-V gate to source characteristics of the M13 and M33 structures were measured in the 100K and 390K temperature range and compared.

Fig. 6 shows the comparison of the I-V gate-source characteristics of the "leaky" M13 and "non leaky" M33 devices over temperature. The temperature dependence of the forward characteristics is similar for both devices, as well as the gate diode barrier height and ideality factor evolution with temperature (Fig. 7). In reverse bias, the gate current obviously presents two regions; a first one down to V_{GS}=-3V (which is close to the threshold voltage of the HEMT) and a second one below V_{GS}=-3V.

In forward and low reverse bias, the preeminent conduction mechanism can be attributed to thermionic field emission (TFE) having a large V_{GS} dependence. As stated in Refs [6], [7], [8], the electron tunneling probability through the Schottky barrier to the GaN layer is enhanced as the barrier gets thinner and is also associated in this case to the pinning of the Fermi level due to a thin defect-rich interfacial layer.

At higher reverse V_{GS} bias (V_{GS}<-3V), the gate leakage current presents a low V_{GS} dependence. Electron tunneling through the Schottky barrier is still controlled by the electron energy at the gate metal-semiconductor interface but the tunneling probability is maximum and pinned at the metal Fermi level [7].

Therefore, the gate leakage current is higher for the M13 structure than for the M33 one but its temperature dependence as well as its characteristic parameters are similar for the two structures under test. The difference in the reverse gate current level in the two structures can only be attributed to local inhomogeneities of the defect and/or charge density in the interface barrier layer.

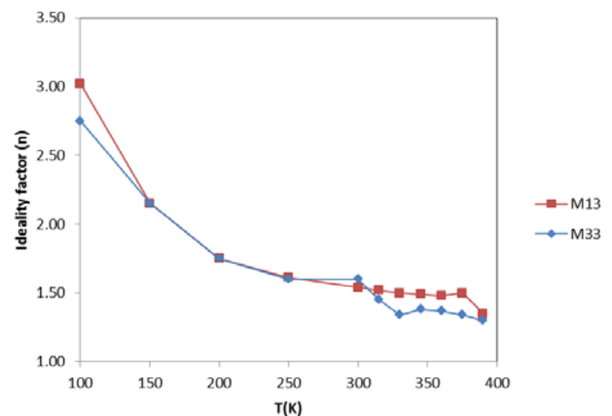


Figure 7: Temperature dependence of the ideality factor for the M13 and M33 structures after storage test.

6. Discussion

The OBIRCH analysis pointed out the relationship between mechanical stresses on the gate leakage current

path. It is assumed that the modification of the mechanical stresses along the gate finger induces local modifications of either the surface state density or the barrier height thanks to the piezoelectric effect in the structure ([9], [10]). Comparing the evolution of the leakage currents in the M13 and M33 structures after storage indicate that the gate finger topology and the surrounding area are important parameters to take in to account in the design for electrical stability and reliability of the AlGaN/GaN HEMT. The M33 interconnection topology seems to prevent some mechanical stresses evolution upon storage at 300°C. It is possibly and simply explained by the stress state of the gate finger which is maintained in the M33 topology thanks to the large gate head metallization present at one edge of the gate finger.

7. Conclusion

In this paper, leakage current signatures in AlGaN/GaN HEMTs are studied after storage test at 300°C. Electrical characterization of the gate to source diode as a function of the temperature does not allow identifying significant difference in the electron transport mechanisms in the two different HEMT topologies under test. In forward and low reverse bias, the preeminent conduction mechanism can be attributed to thermionic field emission (TFE).

By comparing gate pad topologies and by localized FIB cuts, OBIRCh analysis results tend to indicate that mechanical stress in the gate structure strongly influences the leakage current of the transistor. The OBIRCh analysis technique, widely used in silicon technology, appears to be a very efficient tool to localize leakage paths, in particular for HEMT topology with source terminated field plate.

Acknowledgements

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