E-25 6MX
1

Interim Report for Period: 08/2005 - 04/2006
Submitted on: 04/20/2006
Principal Investigator: Sitaraman, Suresh K.
Award ID: 0539023
Organization: GA Tech Res Corp - GIT
Title:
SGER: Innovative Off-Chip Interconnects for 45-nm and sub-45-nm Node ICs

Project Participants

Senior Personnel

Name: Sitaraman, Suresh
Worked for more than 160 Hours: Yes
Contribution to Project:

Name: Swaminathan, Madhavan
Worked for more than 160 Hours: Yes
Contribution to Project:

Post-doc

Graduate Student

Undergraduate Student

Technician, Programmer

Other Participant

Research Experience for Undergraduates

Organizational Partners

Other Collaborators or Contacts

Activities and Findings

Research and Education Activities: (See PDF version submitted by PI at the end of the report)

Findings: (See PDF version submitted by PI at the end of the report)

Training and Development:
-PhD student, Karan Kacker, has gained valuable experience in the design, fabrication, assembly, and testing of compliant interconnects; gained extensive training in cleanroom skills and modeling expertise
- MSME students, Greg Ostrowicki and Thomas Sokol, have gained extensive traing microelectronics cleanroom operations and modeling expertise
- The findings from this project have been integrated in graduate and undergraduate course lectures dealing with microsystems packaging

Outreach Activities:

Journal Publications

Karan Kacker, George Lo and Suresh K. Sitaraman, "Low-K Dielectric Compatible Wafer-Level Compliant Chip-to-Substrate Interconnects", IEEE Transactions - Components, Packaging, and Manufacturing Technologies, p. , vol. , ( ). Submitted

Books or Other One-time Publications

Karan Kacker, George Lo, and Suresh K. Sitaraman, "Wafer-Level, Compliant, Off-Chip Interconnects for Next-Generation Low-K Dielectric/Cu ICs", (2006). Conference, Submitted
Bibliography: ASME - International Mechanical Engineering Congress and Exposition

Web/Internet Site

Other Specific Products

Product Type:

Other inventions

Product Description:

We have found that varying compliance will significantly benefit from both mechanical and electrical perspectives. Accordingly, we are working on an invention disclosure that will detail how one can achieve a heterogeneous array of interconnects that will have optimum electrical and mechanical performance.

The invention disclosure will be filed in the near future.

Sharing Information:

1) Microelectronics industry can use our invention for their off-chip interconnects
2) Packaging industry can use our invention as potential chip-to-substrate interconnects
3) Testing industry can use our invention as microelectronics test probes

Contributions

Contributions within Discipline:

- The compliant interconnects developed in this work present a paradigm shift; by combining both electrical and mechanical design aspects, the compliant interconnects address one of the critical bottlenecks facing next-generation microsystems development
- The developed interconnects do not crack or delaminate the dielectrics in the die, and at the same time, are reliable and robust
- The interconnect design is unique and innovative; invention discloures for varying compliance are being planned.

Contributions to Other Disciplines:

- The proposed interconnects can be scaled down and used for bio-sensing applications. For example, the scaled-down interconnects can be used for antigen detection associated with cancer diagnosis, treatment, and remission evaluation
- The interconnects when assembled using lead-free solder material can be environmentally friendly
- The interconnects can be fabricated in a large-area format, and therefore, they are cost-effective

Contributions to Human Resource Development:

- Next-generation microsystems will significantly benefit from the ongoing work.
- The findings from the work will be published in at least one journal and one conference; invention disclosures are also planned
- We will also explore using undergraduate students in the research program

Contributions to Resources for Research and Education:

- The findings and methods from the work are being integrated into undergraduate and graduate classes dealling with microsystems packaging

Contributions Beyond Science and Engineering:

- The proposed interconnects can be scaled down and used for bio-sensing and biomedical engingering applications
- By using lead-free solder, the proposed interconnects are environmentally friendly
- By using wafer-level fabrication techniques, the interconnects are cost-effective
- The proposed interconnects lend themselves for miniaturized microsystems, thus saving material and cost

Categories for which nothing is reported:

Organizational Partners

Activities and Findings: Any Outreach Activities

Any Web/Internet Site

NSF GRANT PROGRESS REPORT

SGER: INNOVATIVE OFF-CHIP INTERCONNECTS FOR 45-NM AND SUB-45-NM NODE ICs

ECS-0539023 – Electronics, Photonics, and Device Technologies

Period Covered: August 2005 – March 2006

Suresh K. Sitaraman
Professor
The George W. Woodruff School of Mechanical Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0405
Email: suresh.sitaraman@me.gatech.edu
404-894-3405 (voice); 404-894-9342 (Fax)

BACKGROUND

Power and latency are fast becoming major bottlenecks in the design of high performance microprocessors and computers. Power relates to both consumption and dissipation, and therefore, effective power distribution design and thermal management solutions are required. Latency is caused by the global interconnects on the IC that span at least half a chip edge due to the RC and transmission line delay. Limits to chip power dissipation and power density and limits on hyper-pipelining in microprocessors threaten to impede the exponential growth in microprocessor performance. In contrast, multi-core processors can continue to provide a historical performance growth on most consumer and business applications provided that the power efficiency of the cores stays within reasonable power budgets. To sustain the dramatic performance growth, a rapid increase in the number of cores per die and a corresponding growth in off-chip bandwidth are required. Furthermore, to reduce the RC and transmission line delay, low-K dielectric/Cu and ultra-low-K dielectric/Cu interconnects on silicon will become increasingly common. In such ICs, the thermo-mechanical stresses induced by the chip-to-substrate interconnects could crack or delaminate the dielectric material causing reliability problems. Thus, there is a compelling and immediate need to explore high-risk, high-payoff chip-to-package off-chip interconnects keeping in perspective the electrical and thermo-mechanical requirements.

The ongoing SGER effort, accordingly, aims to design and fabricate innovative compliant off-chip interconnects (Figure 1) that are optimized for electrical, thermal, and mechanical performance and that are wafer-level, scalable, and cost-effective. The strategic objectives of the compliant interconnects are: 1) To have high mechanical compliance (more than 7 mm/N) in the three orthogonal directions to be able to accommodate the differential displacement induced due to the CTE mismatch between a die and an organic substrate without requiring an underfill material; 2) To induce low force on the die bonding pads under thermo-mechanical loading so that the interconnect will not crack or delaminate low-K dielectric in the current and future dies; 3) To be able to be scaled with future evolution in microelectronic systems; 4) To be cost-effective through wafer-level and no-underfill processes and through using existing wafer fab infrastructure; 5) To provide a lead-free interconnect solution; and 6) To be reliable with acceptable electrical, mechanical, and thermal properties.

Approach

A systematic approach consisting of Mechanical and Electrical Design, Fabrication, Assembly, and Testing is being carried out to realize the compliant interconnects.

Figure 1: *Fabricated Compliant Interconnects (with and without solder)*

1. *Mechanical Design*: Analytical and numerical models have been developed to determine the mechanical compliance of the compliant interconnects in the three orthogonal directions. Models have been developed to determine the stress/strain distribution in the compliant interconnects under thermo-mechanical loading. Models have also been developed to illustrate the compatibility of these interconnects with Low-K / Cu dies.
2. *Electrical Design*: Analytical models and numerical models have been developed to determine the electrical parasitics (i.e. resistance, inductance) of the interconnects at DC as well as up to 10 GHz frequency.
3. *Design Optimization*: Since the geometric parameters of the compliant interconnect have opposite effects on the desired mechanical and electrical performance, geometry optimization was done to meet both the mechanical and electrical performance targets and requirements.
4. *Fabrication:* Using LIGA-like fabrication process, compliant interconnects were fabricated at a 100μm pitch (Figure 1).
5. *Assembly and Testing:* Silicon wafers with compliant interconnects were singulated into individual chips, and these chips were assembled on organic substrates through solder attachment of compliant interconnects. The thermo-mechanical reliability was assessed through subjecting the assemblies to thermal cycling and monitoring the interconnect electrical resistance.

TASK STATUS

Task 1: Design Optimization of Off-Chip Interconnects

It was observed that the geometry parameters that enhance the mechanical compliance typically increase the inductance and the resistance. Hence a design trade-off between electrical and mechanical properties was determined through an optimization study. Several parameters were used as target values for the electrical and mechanical design. For example, the compliance in the three orthogonal directions should be greater than 7 mm/N. The stress in the interconnect under thermo-mechanical loading should be preferably less than the yield stress of the interconnect material. The electrical resistance can be greater than 1 mΩ (solder bump value); however, should not exceed 100 mΩ. The electrical inductance should be between 20 and 100 pH. Response surface methodology and non-linear optimization was used to determine the radius, width, thickness, and height of the compliant interconnects that will meet all of these design targets. Based on the optimization study, it is seen that the compliant interconnects geometry can be designed to meet the mechanical and electrical requirements.

Task 2: Test Vehicle Design, Fabrication, Assembly, and Testing

Fabrication of Compliant Interconnects

The fabrication process of the wafer-level compliant interconnects is schematically illustrated step by step in Figure 2. On a given clean wafer, a Ti/Cu/Ti seed layer is first sputtered. The bottom and the top Ti layers are applied to improve the adhesion between wafer/Cu and Cu/applied photoresist interfaces. Then a thick photoresist is spun, soft baked, UV patterned, post-exposure baked and developed. After etching away the top Ti layer of the seed layer, the bottom copper post is electroplated. This sequential process of photolithography and electroplating is repeated to create the three-layer compliant interconnect structure. The top photoresist is back-etched using Reactive Ion Etching, and Au/Ni or solder/Ni was then electroplated on the exposed tip region of the copper column as illustrated in Figure 2g. Once the steps are completed, the surrounding photoresist and the seed layers are completely etched layer by layer. Thus, the free-standing wafer-level compliant interconnects are fabricated. SEM micrographs of compliant interconnects fabricated at 100-um pitch are shown in Figure 3. Figure 3a shows the compliant interconnects with electroplated Au/Ni and Figure 3b shows the SEM micrograph of the compliant interconnects with electroplated eutectic Pb/Sn solder bumps.

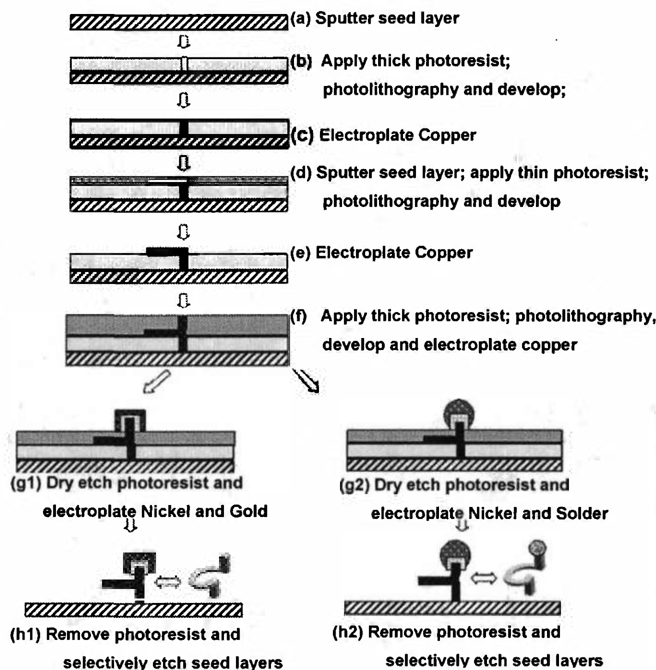
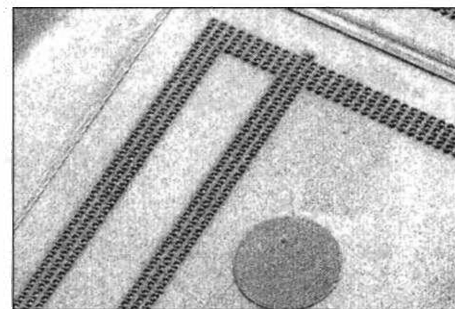
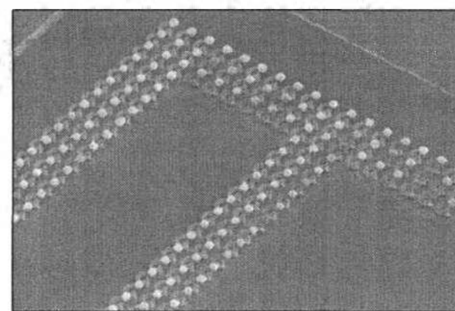


Figure 2: Compliant Interconnects - Fabrication Process Steps



(a)



(b)

Figure 3: Fabricated Compliant Interconnects

Mechanical Characterization

A. Out-of-plane Mechanical Compliance

For fine pitch packages, good out-of-plane compliance is desired to compensate for the non-planarity of the organic substrate and to ensure a reliable contact during assembly and probing. The out-of-plane (*y* direction) compliance of the free-standing compliant interconnect was characterized using a nanoindenter. Using the nanoindenter a displacement was applied on the interconnect in the out-of-plane direction and the

corresponding force in the out-of-plane direction was measured. Figure 4 shows the experimental displacement versus load curve. The slope of the curve provides the out-of-plane compliance of the compliant interconnect and was calculated to be 14.7mm/N. Finite-element simulations were also performed to determine the out-of-plane compliance of the interconnect. It is seen that the compliance values measured through experiments and determined through numerical simulations are of the same order of magnitude, and more importantly, the compliance values exceed the target value of 7 mm/N, recommended by industry experts.

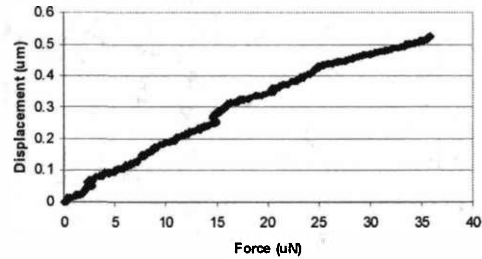


Figure 4: Force vs Displacement

B. Interconnect Robustness

To demonstrate its robustness, the compliant interconnect was intentionally deformed as depicted in Figures 5 and 6. As seen from Figure 5, the compliant interconnect is robust against excessive deformation. When the arcuate beam was bent backwards, there was no cracking or delamination in the interconnect. Also, when the free-standing structure was pushed sideways, the interconnect structure did not break or delaminate from the silicon wafer. The figures also highlight the strong adhesion between the three mask layers, especially between the base post and the silicon substrate. It should be noted that these excessive deformations were applied to demonstrate the robustness of the compliant interconnect structure, and are not representative of the actual thermo-mechanical deformations experienced by the interconnects in a packaging assembly.

Figure 5: Robustness Demonstration 1

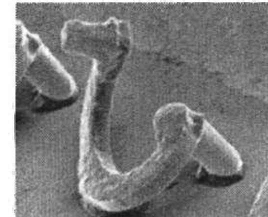


Figure 6: Robustness Demonstration 2

Interconnect Assembly

A. Interconnect Fabrication for Assembly

For purposes of flip chip assembly on organic substrates, the tip region of the top post of the interconnect should have suitable metallurgy. Accordingly, as described in Figure 2(g), a part of the top post of the interconnect is exposed by dry etching the third layer photoresist in a reactive ion etchant. The appropriate metallurgical interface can then be plated on the exposed copper post. Two metallurgical interfaces were explored. The first choice, as shown in Figure 2(g2) involved plating a nickel barrier layer followed by 60Sn/40Pb solder plating. The plated solder can then be utilized for assembling the interconnects on the substrate. However, due to reasons discussed later, an alternative metallurgical interface was employed. In this alternative approach, after dry etching the third layer photoresist, layers of nickel and gold were plated on the tip of the interconnect, as illustrated in Figure 2(g1). The gold layer serves as an anti-oxidation barrier layer. The solder is now electroplated or stencil-printed on the substrate pads for the purpose of assembly. The purpose of the current study was to demonstrate the assembly reliability of the compliant interconnects, and therefore, Pb/Sn solder is employed in this work. In the ongoing work, we will explore the assembly using lead-free solder alloys.

B. Organic Substrate Design

A low-CTE (α_{FR-4} = 11 ppm/°C) FR-4 substrate was utilized for the purpose of assembly. A daisy-chain test structure is utilized to assess the interconnect reliability. The daisy chain structure and the probe pads are designed such that the failure location can be narrowed down to one to few pairs of interconnects. The substrate pad was solder-mask defined with a pad opening of 35 - 40µm in diameter. The thickness of the soldermask was 3 – 4µm on top of the copper pads. The copper pads had an electroless nickel gold (ENIG) finish and a subsequent layer of electroplated 60Sn/40Pb solder.

C. Assembly Process

Free-standing compliant interconnects were fabricated on Si wafer, and the wafer was singulated into dies with 100µm pitch compliant interconnects. The dies were then assembled onto substrates. Prior to the assembly of the compliant interconnects onto organic substrates, the interconnects were assembled onto glass substrates with a stack of Ti, Cu, and 60Sn/40Pb layers. Assembly on glass substrates provided a quick and easy way to inspect the assembly. Critical parameters identified for the assembly process were:

1) Metallurgical Interface: Two different metallurgical interfaces, Ni/SnPb or Ni/Au, can be plated on the tip of the interconnects for the purpose of assembly. Initial assemblies performed utilizing the Ni/SnPb interface resulted in poor yield on assembly. This was believed to be due to the RIE etch of the SU8 photoresist during the release of the interconnects. The RIE process results in excessive oxidation of the solder impacting assembly yield. Utilizing a Ni/Au interface with the Au serving as an anti-oxidation barrier resulted in a significant improvement in assembly yield. Solder for the purposes of assembly in this case was now plated on the substrate pads.

2) Flux Volume: Sufficient flux must be dispensed to reduce the oxides on the surface of the solder and to provide a deoxidized surface for the solder to wet. However excessive flux would prevent the solder from wetting the interconnects. Therefore, a suitable flux volume was determined during assembly process development.

3) Compressive Force Profile: A certain amount of compressive force must be applied to allow all of the interconnects to make contact with the substrate pads and to overcome the non-planarity of the substrate. However, it was also observed that if a large force was applied it would excessively deform the compliant interconnects, causing the arcuate beam to contact the neighboring pad on the substrate. This in turn would cause the solder from the neighboring pad to wick onto the arcuate beam during reflow resulting in misalignment.

4) Temperature Profile: The temperature profile for solder reflow can be divided into four stages: pre-heat, thermal soak, reflow, and cool down. Each of the four stages must be optimized as it impacts assembly yield as well the subsequent reliability of the solder joint.

Figure 7: Cross-Section of Assembled Compliant Interconnects

Using the developed assembly process, the compliant interconnects were subsequently assembled on organic substrates. The alignment of the interconnects with the corresponding pads on the substrate was verified through X-Ray imaging. A cross-section of the assembled compliant interconnect on an organic substrate is shown in Figure 7.

Experimental Reliability Assessment

The compliant interconnects assembled on organic substrate were subjected to JEDEC (JESD22-A104-B), test condition J thermal profile – cycling between 0 and 100 °C with 10 minute dwell times.

The assemblies were taken out at various intervals during thermal cycling and the daisy chain resistance was measured. The thermal cycling results are presented in Figure 8. The vertical axis correspond to the number of working probing pads calculated as a percentage of the number of working probing pads after assembly but prior to thermal cycling. The assembly process still needs further refinement to enhance the yield and the overall reliability of the test vehicle.

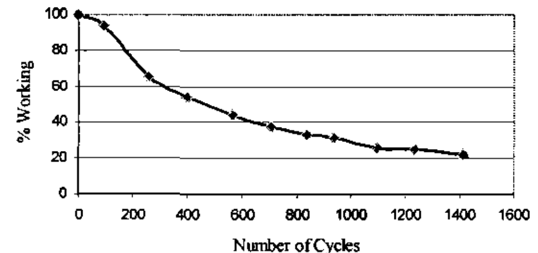


Figure 8: % Working vs Number of Cycles

Compatibility with Low-K Dielectric

Numerical simulations were done to examine if the developed interconnects will be beneficial for ICs with low-K dielectric material. To demonstrate this, a generalized plane-deformation (GPD) finite-element model was developed for a die on an organic substrate. The interconnects, die pads, and solder attach were also modeled. The solder reflow temperature was taken as the stress-free temperature, and the assembly was simulated to be cooled down from the reflow temperature to -55°C. It was observed that the stresses introduced in the die are less than 5 MPa. As the compliant interconnects create significantly lower stresses in the die by decoupling the die from the substrate, the low-K dielectric material is not likely to crack or delaminate. On the other hand, for flip-chip on organic board assemblies with underfills, our simulations with identical die/substrate dimensions indicate that the die stresses will be of the order of 140 MPa; such high stresses are likely to lead to low-K dielectric cracking or delamination. Similarly when the interfacial peel and shear stresses are examined at the die pad/interconnect interfaces, it is seen that the stresses are less than 10 MPa. This indicates that the interconnects are less likely to delaminate or crack from the die pads under typical thermo-mechanical loading.

Integrative Solution

The compliant interconnects provide excellent opportunities for I/O customization based on electrical and mechanical requirements. In general, the interconnects near the center of the die need not have a high mechanical compliance as the differential displacement between the die and the substrate due to CTE mismatch is low near the center of the die. Thus, the interconnects at the center of the die can be fabricated in the shape of a column structure, while the interconnects near the edge of the die can be fabricated with compliant interconnect structure. In other words, the three-mask process can be used to create interconnects that vary in shape from the center to the edge of a die: from column to low-compliance interconnects to high-compliance interconnects, and still maintaining the 100-um pitch through the entire array. The central columns can be beneficial from a number of perspectives: (1) They can be used predominantly as ground-power interconnects with the ability to carry higher current, (2) They can provide high enough rigidity against potential vibration or drop induced damage on the compliant interconnects, (3) They can act as a stopper to prevent damage to the compliant interconnects when an excessive force is inadvertently applied either during assembly and/or when a heat sink is attached. As these columns are located near the center of the die where the CTE-induced differential thermal expansion is low, these columns will neither fatigue fail nor exert excessive force on the low-K dielectric to crack or to delaminate. The interconnects away from the center of the die can be fabricated with increasing magnitude of compliance as one traverses to the corner/edge of the die. Typically, near the corner of the die, the CTE-induced differential thermal deformation is high, and therefore, higher compliance is needed to reduce the force induced on the die pads by the interconnect. The interconnects in the middle can have "low" compliance and still will not delaminate or crack the low-K dielectric. When the mechanical compliance is low (smaller arc radius or wider interconnect), the electrical parasitics will improve, and thus the compliant interconnects will provide a unique opportunity to tailor the system performance by balancing electrical requirements against thermo-mechanical reliability concerns.

To demonstrate the advantages of such an approach, finite element models were developed to represent three different packages. In the first package (*Package 1*), column interconnects with a square cross-section (20μm x 20μm) were populated throughout the die in a similar 100x100 area-array configuration. In the second package (*Package 2*), identical high-compliance interconnects were populated throughout the die in a 100x100 area-array configuration. In the third package (*Package 3*), the center of the die was populated with column interconnects, the peripheral rows were populated with high-compliance interconnects, and the area in-between was populated with low-compliance interconnects. The interconnects formed a 100x100 array with the columns near the die center forming a 20x20 area-array, the low-compliant interconnects forming the intermediate 15 rows, and the high-compliant interconnects forming the outer 25 rows. Generalized Plane Displacement (GPD) models were developed for each of the three packages taking into consideration the silicon die, the interconnects, the solder attach, and the organic substrate. An example GPD model of *Package 3*, comprising of a heterogeneous combination of interconnects is shown in Figure 9.

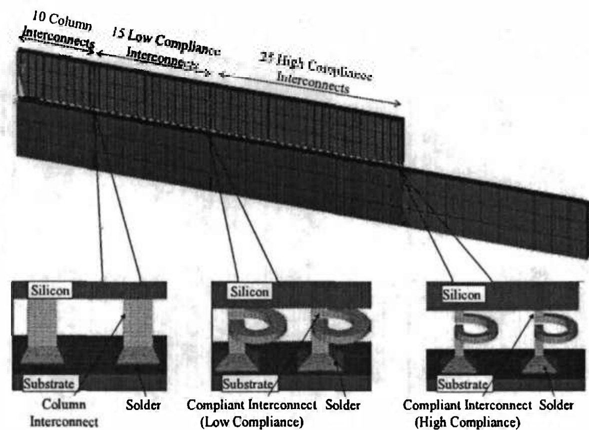
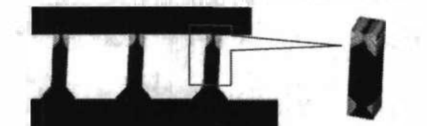
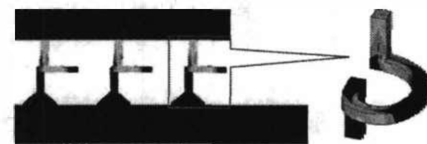


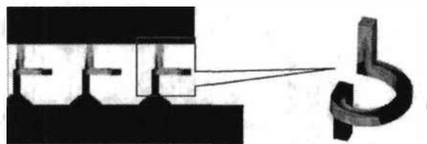
Figure 9: FEA Model of Variable Interconnect Configuration



(a) Package 1 – Column Interconnects



(b) Package 2 – High-Compliant G-Helix Interconnects



(c) Package 3 – Heterogenous Interconnects

Figure 10: Equivalent Plastic Strain Distribution at the End of 3rd Thermal cycle

The plastic strain distribution for all three packages after thermal cycling between 0 and 100 C was determined. In both *Package 1* and *Package 2*, the maximum plastic strain is observed in the outermost interconnect (Figure 10). This is also true of *Package 3*, in which the maximum plastic strain is observed in the outermost high-compliance interconnect rather than the outermost low-compliance interconnect or the outermost column interconnect. From the plastic strain component in various parts of the assembly, the fatigue life of the compliant interconnect as well as the solder joint was determined, and it was found that the compliant interconnect is likely to fail first compared to the solder joint, as intended in the design. In other words, the compliant interconnects are designed to accommodate the differential displacement induced through the CTE mismatch between the die and the substrate and are designed to alleviate the high plastic deformation in the solder joints.

It is seen that the package with compliant interconnects and the package with compliant plus column interconnects will have a mean fatigue life of over 2700 cycles, while the package with column interconnects will have a fatigue life of about 750 cycles. This shows that the proposed integrative solution with varying compliance is a viable option.

SUMMARY

- Excellent progress has been made in the design, fabrication, assembly, and testing of compliant interconnects.
- The compliant interconnects appear to be a viable solution to meet the next-generation packaging requirements.
- Aggressive interconnect layout and additional assembly and reliability testing are required to understand the potential of the proposed interconnects. Such a layout design and test procedures are being explored.
- One invention disclosure is planned to be submitted based on the program. At least two papers (one conference and one journal) are likely to be published based on the findings of the program.
- The principal investigator gratefully acknowledges the funding from NSF to carry out this innovative research program which is critical for the development of next-generation microelectronics systems.

NSF GRANT PROGRESS REPORT

ACTIVITIES

Mechanical and Electrical Design, Fabrication, Assembly, and Testing have been carried out to realize the compliant interconnects.

Figure 1: *Fabricated Compliant Interconnects (with and without solder)*

1. *Mechanical Design*: Analytical and numerical models have been developed to determine the mechanical compliance of the compliant interconnects in the three orthogonal directions. Models have been developed to determine the stress/strain distribution in the compliant interconnects under thermo-mechanical loading. Models have also been developed to illustrate the compatibility of these interconnects with Low-K / Cu dies.
2. *Electrical Design*: Analytical models and numerical models have been developed to determine the electrical parasitics (i.e. resistance, inductance) of the interconnects at DC as well as up to 10 GHz frequency.
3. *Design Optimization*: Since the geometric parameters of the compliant interconnect have opposite effects on the desired mechanical and electrical performance, geometry optimization was done to meet both the mechanical and electrical performance targets and requirements.
4. *Fabrication:* Using LIGA-like fabrication process, compliant interconnects were fabricated at a 100µm pitch (Figure 1).
5. *Assembly and Testing:* Silicon wafers with compliant interconnects were singulated into individual chips, and these chips were assembled on organic substrates through solder attachment of compliant interconnects. The thermo-mechanical reliability was assessed through subjecting the assemblies to thermal cycling and monitoring the interconnect electrical resistance.

FINDINGS

- Compliant interconnects at a 100 μm pitch were fabricated on a silicon wafer, and the silcon wafer was singulated to form individual dies. The compliant interconnects do not crack or delaminate from the silicon wafer under various types of mechanical loading.
- Numerical simulations and thermal cycling experiments show that the interconnects are thermo-mechanically reliable. Additional thermal cycling experiments are also planned.
- The out-of-plane compliance of the interconnects was characterized utilizing a nanoindenter, and it was seen that the interconnects exceed the target value of 7 mm/N, recommended by industry experts.
- It was demonstrated that the die stresses induced by the compliant interconnects are an order of magnitude lower than the die stresses in FCOB assemblies, and hence the compliant interconnects are not likely to crack or delaminate low-K dielectric material.
- An innovative approach to compliant interconnects utilizing a heterogeneous combination of column-like interconnects near the center of the die and helix-interconnects with increasing level of compliance toward the edge the die was also studied. These heterogeneous array of interconnects appear to provide a balanced combination of mechanical and electrical performance without compromising the thermo-mechanical reliability. It is seen that the package with compliant plus column interconnects will have a mean fatigue life of over 2700 cycles
- Overall, the compliant interconnects appear to be a viable solution to meet the next-generation packaging requirements.